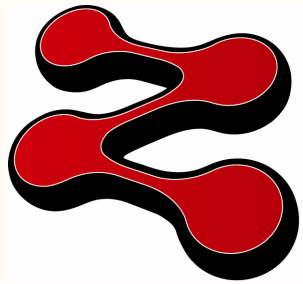
ZedBoard	
Digilent	
www.zedboard.org	
Function	**Sheet Number**
Cover Sheet	1
FMC, AMS Connectors	2
PMODS, General I/O	3
Audio Codec	4
HDMI, VGA	5
Ethernet, OLED, SD Card	6
USB, UART	7
FPGA Configuration	8
FPGA Banks	9
DDR, MIO Banks	10
FPGA Power	11
USB Programming	12
DDR3 Memory	13
DDR Termination	14
Power Regulation	15
Power Regulation	16
Power Regulation	17



ZedBoard

04 Mar 2013

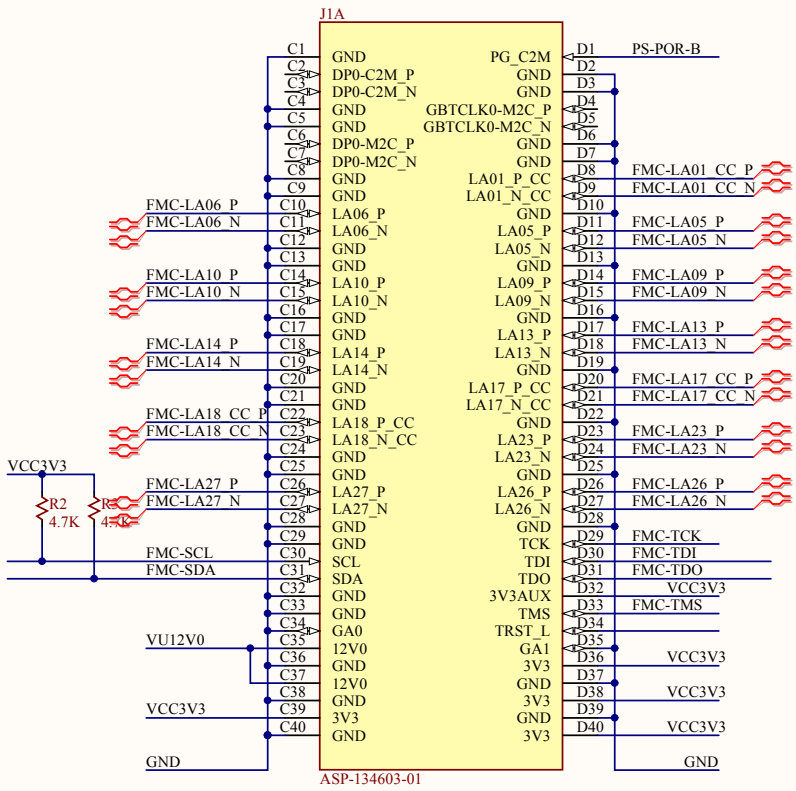
3:33:55 PM

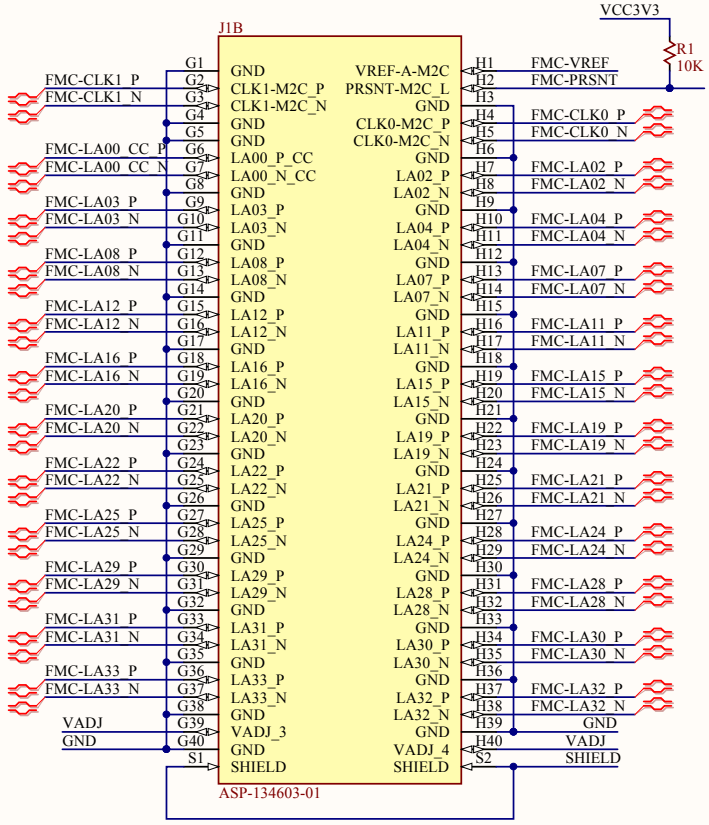
www.zedboard.org

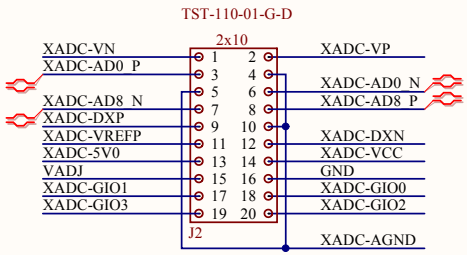
Copyright 2013, Digilent, Inc. All Rights Reserved.
This material may not be reproduced, distributed, republished, displayed, posted, transmitted or copied in any form or by any means without the prior written permission of Digilent, Inc. DIGILENT and the Digilent logo are registered trademarks of Digilent, Inc. All trademarks and trade names are the properties of their respective owners and Digilent, Inc. disclaims any proprietary interest or right in trademarks, service marks and trade names other than its own. Digilent is not responsible for typographical or other errors or omissions or for direct, indirect, incidental or consequential damages related to this material or resulting from its use. Digilent makes no warranty or representation respecting this material, which is provided on an "AS IS" basis. DIGILENT HEREBY DISCLAIMS ALL WARRANTIES OR LIABILITY OF ANY KIND WITH RESPECT THERETO, INCLUDING, WITHOUT LIMITATION, REPRESENTATIONS REGARDING ACCURACY AND COMPLETENESS, ALL IMPLIED WARRANTIES AND CONDITIONS OF MERCHANTABILITY, SUITABILITY OR FITNESS FOR A PARTICULAR PURPOSE, TITLE AND/OR NON-INFRINGEMENT. This material is not designed, intended or authorized for use in medical, life support, life sustaining or nuclear applications or applications in which the failure of the product could result in personal injury, death or property damage. Any party using or selling products for use in any such applications do so at their sole risk and agree that Digilent is not liable, in whole or in part, for any claim or damage arising from such use, and agree to fully indemnify, defend and hold harmless Digilent from and against any and all claims, damages, loss, cost, expense or liability arising out of or in connection with the use or performance of products in such applications.

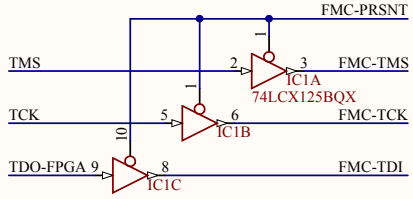
Title	Rev
ZED	D.2
	Copyright 2013
Circuit: Title Page	
Doc#: 500-248	
Engineer: EG	
Author: GMA	
Date: 3/4/2013	
Sheet# 1 out of 17	

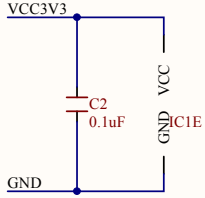
DIGILENT® BEYOND THEORY

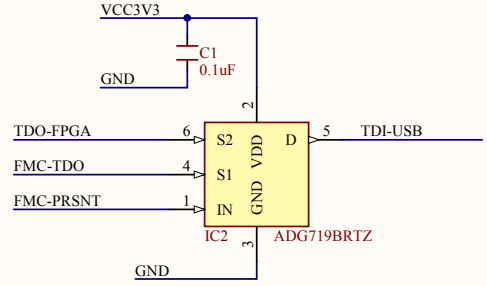












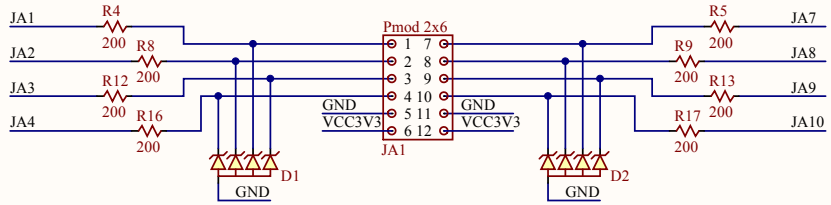
Foot F1
Foot F2
Foot F3
Foot F4

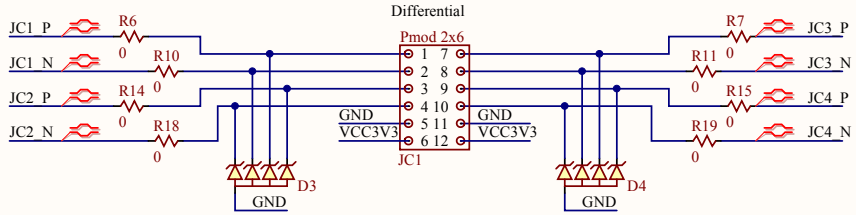
ZED Board

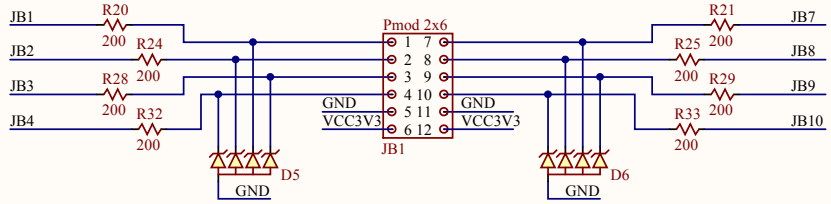
Digilent Inc. ROHS Chinese ROHS Avnet CE

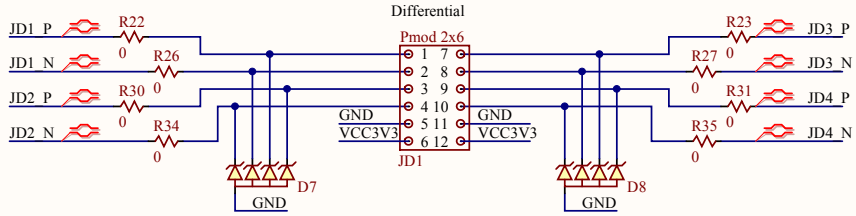
Title	ZED
Rev	D.2
Copyright	2013
Circuit	FMC and AMS Connector
Doc#	500-248
Engineer	EG
Author	GMA
Date	3/4/2013
Sheet#	2 out of 17

DIGILENT BEYOND THEORY

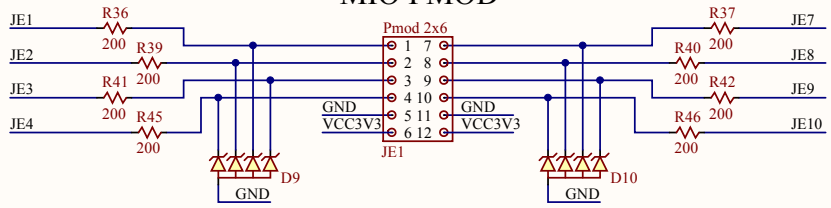




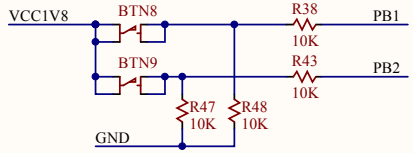


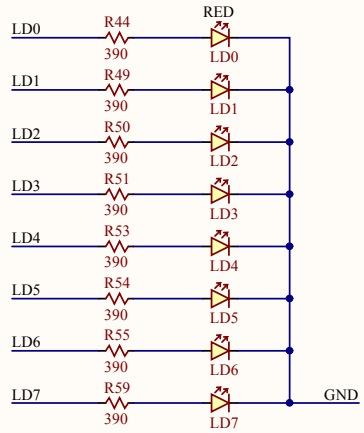


MIO PMOD

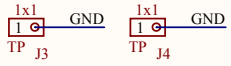


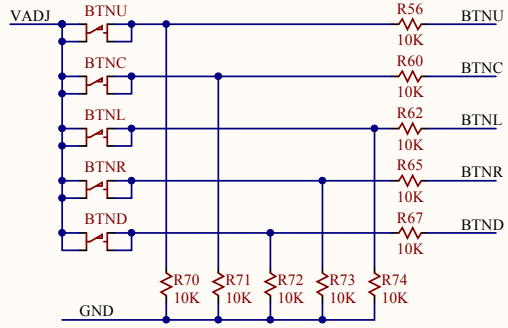
MIO BUTTON

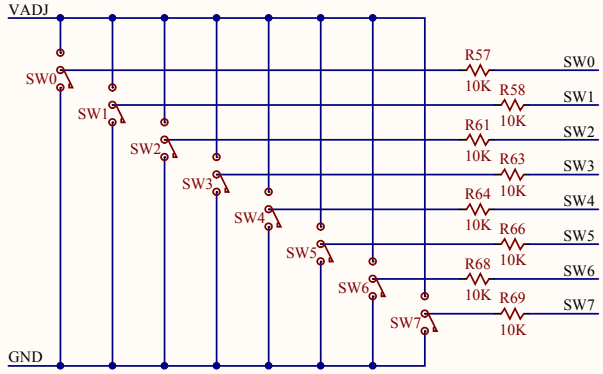




MIO LED

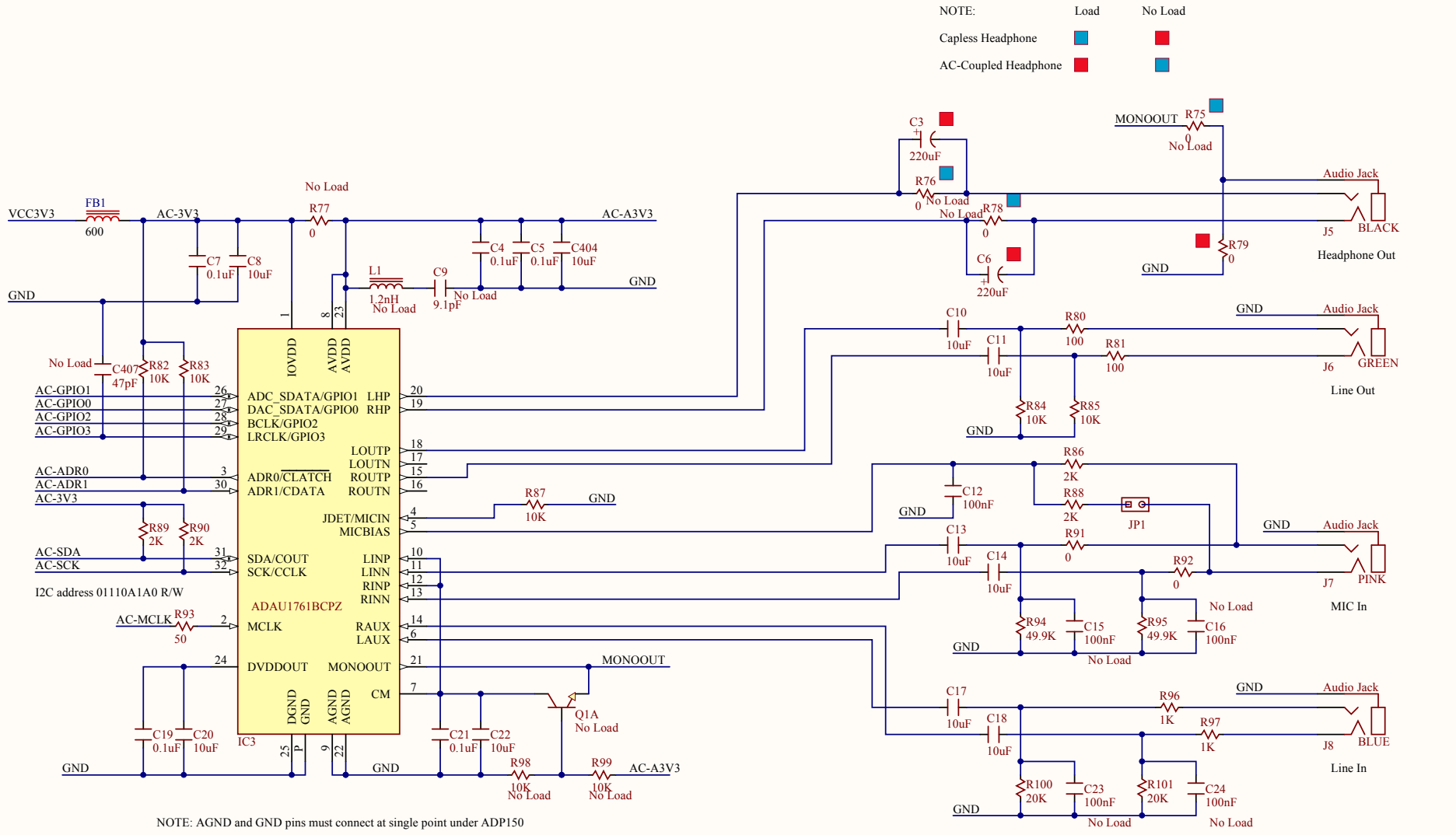


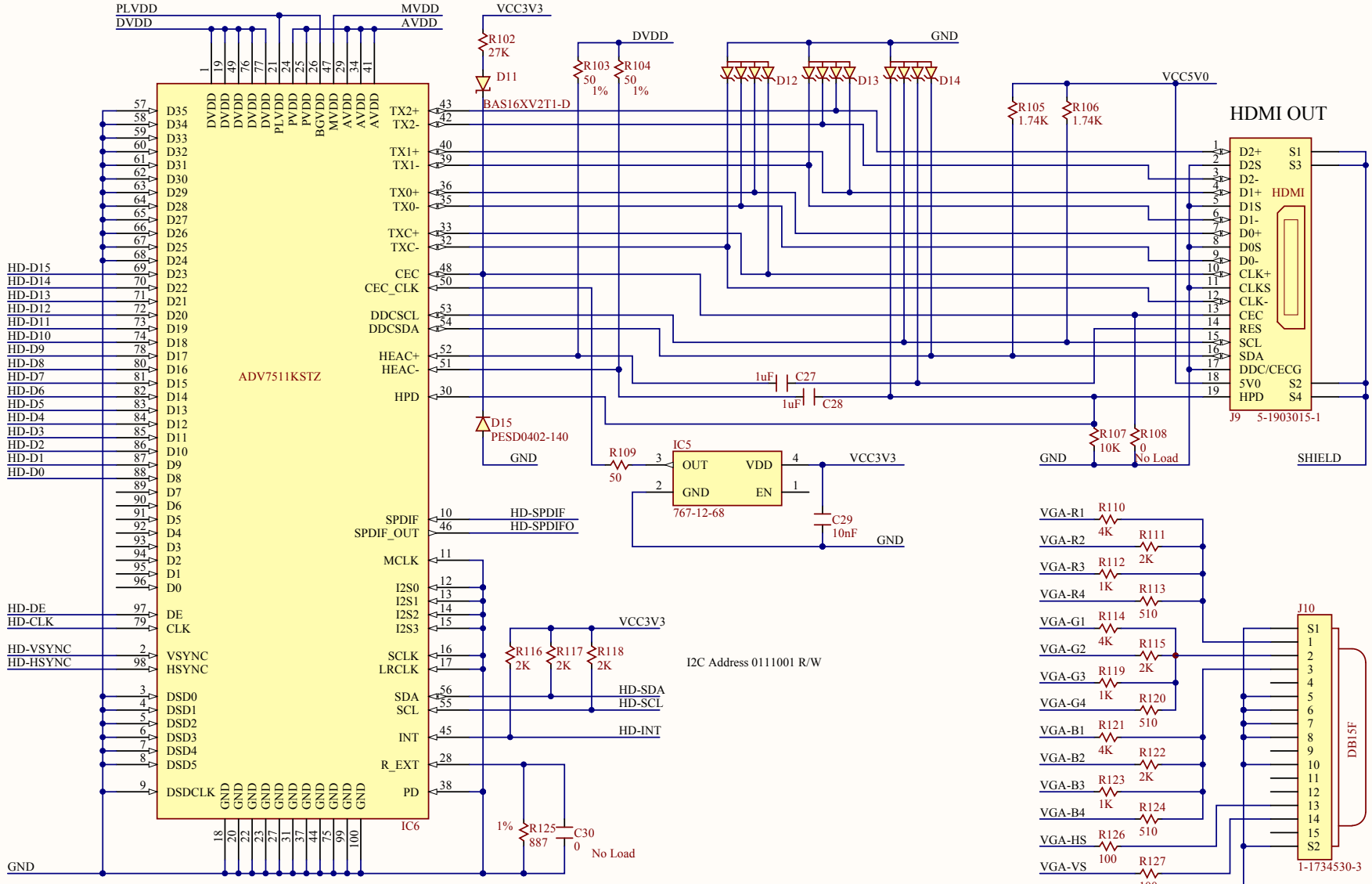


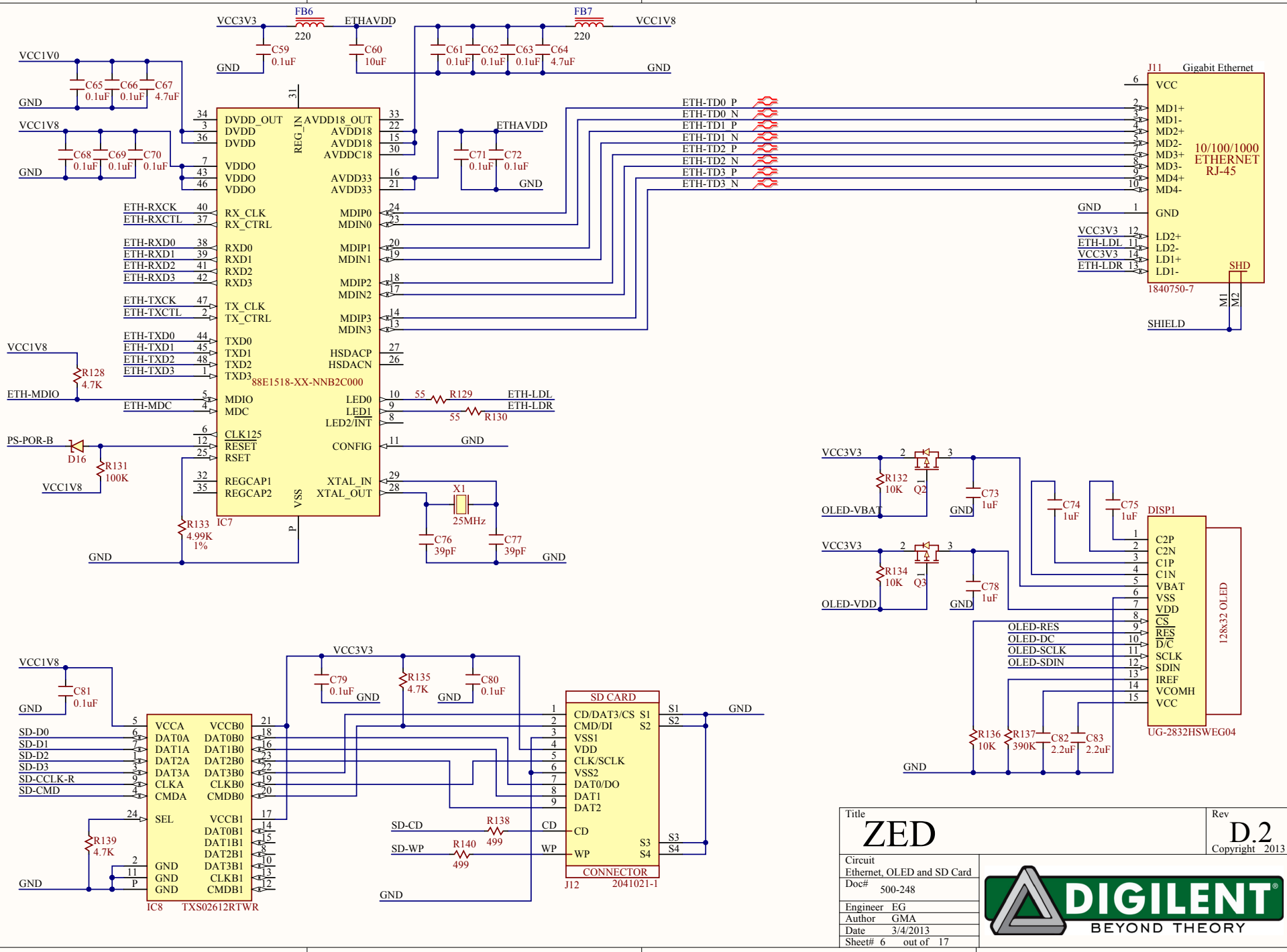


Title	ZED
Rev	D.2
Copyright	2013
Circuit	PMODs andGeneral I/O
Doc#	500-248
Engineer	EG
Author	GMA
Date	3/4/2013
Sheet#	3 out of 17

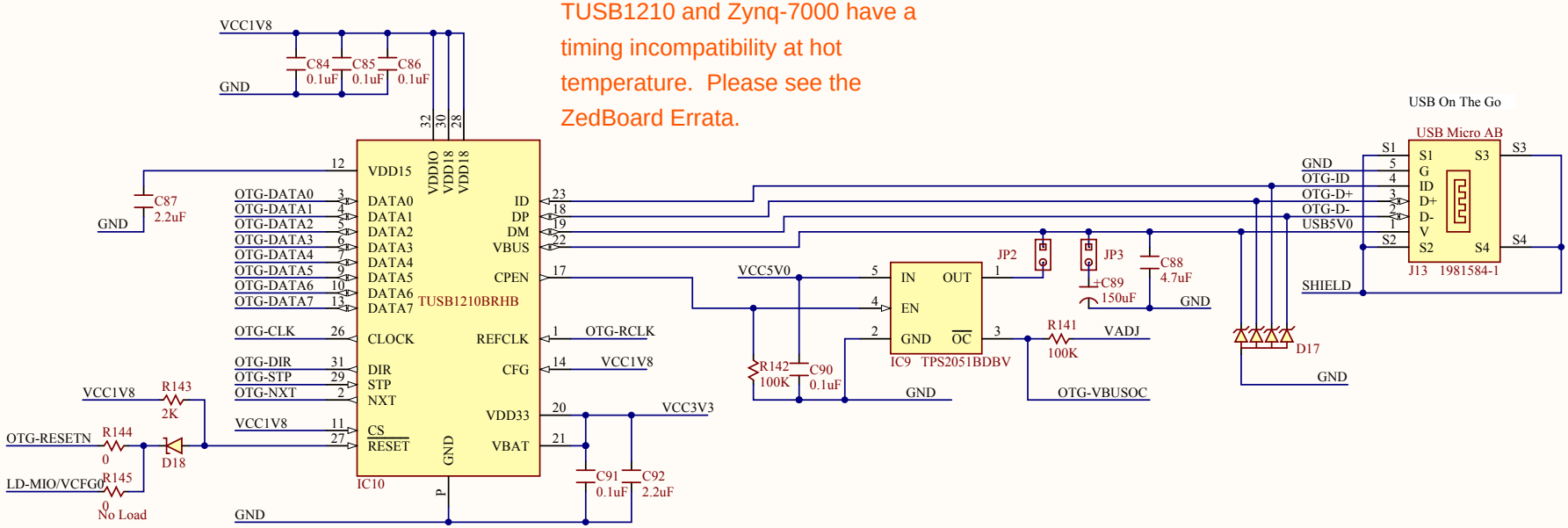
DIGILENT
BEYOND THEORY

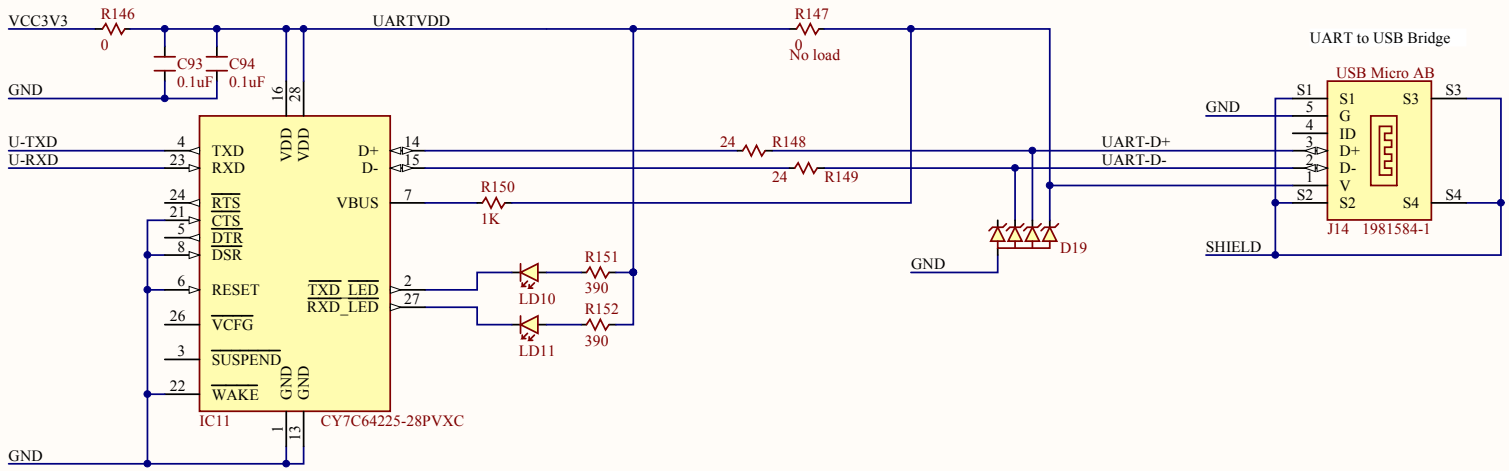

NOTE:
Load
No Load
Capless Headphone
AC-Coupled Headphone
VCC3V3
FB1
600
AC-3V3
No Load
R77
0
AC-A3V3
C7
0.1uF
C8
10uF
C4
0.1uF
C5
0.1uF
C404
10uF
GND
L1
1.2nH
No Load
C9
9.1pF
No Load
IOVDD
AVDD
AVDD
ADC_SDATA/GPIO1
DAC_SDATA/GPIO0
BCLK/GPIO2
LRCLK/GPIO3
ADR0/CLATCH
ADR1/CDATA
JDET/MICIN
MICBIAS
SDA/COUT
SCK/CCLK
MCLK
DVDDOUT
DGND
GND
AGND
AGND
LHP
RHP
LOUTP
LOUTN
ROUTP
ROUTN
LINP
LINN
RINP
RINN
RAUX
LAUX
MONOOUT
CM
ADAU1761BCPZ
IC3
No Load
C407
47pF
R82
10K
R83
10K
AC-GPIO1
AC-GPIO0
AC-GPIO2
AC-GPIO3
AC-ADR0
AC-ADR1
AC-3V3
R89
2K
R90
2K
AC-SDA
AC-SCK
I2C address 01110A1A0 R/W
AC-MCLK
R93
50
R87
10K
C19
0.1uF
C20
10uF
C21
0.1uF
C22
10uF
Q1A
No Load
R98
10K
No Load
R99
10K
No Load
NOTE: AGND and GND pins must connect at single point under ADP150
C3
220uF
R76
0
No Load
C6
220uF
R78
0
No Load
MONOOUT
R75
0
No Load
R79
0
Audio Jack
J5
BLACK
Headphone Out
C10
10uF
C11
10uF
R80
100
R81
100
R84
10K
R85
10K
J6
GREEN
Line Out
C12
100nF
R86
2K
R88
2K
JP1
C13
10uF
C14
10uF
R91
0
R92
0
R94
49.9K
C15
100nF
No Load
R95
49.9K
C16
100nF
No Load
J7
PINK
MIC In
C17
10uF
C18
10uF
R96
1K
R97
1K
R100
20K
C23
100nF
No Load
R101
20K
C24
100nF
No Load
J8
BLUE
Line In
IC4
VCC5V0
A1
B1
VIN
VOUT
EN
GND
A2
B2
ADP150ACBZ-3.3
C405
10uF
C25
1uF
C26
1uF
C406
10uF
AC-A3V3
Title
ZED
Rev
D.2
Copyright 2013
Circuit
Audio Codec
Doc#
500-248
Engineer EG
Author GMA
Date 3/4/2013
Sheet# 4 out of 17
DIGILENT
BEYOND THEORY

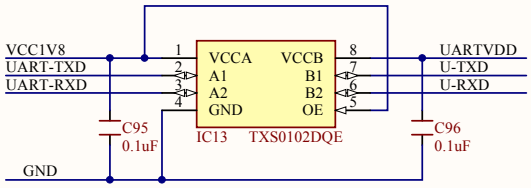

PLVDD
DVDD
MVDD
AVDD
VCC3V3
R102 27K
D11
BAS16XV2T1-D
R103 50 1%
R104 50 1%
DVDD
D12
D13
D14
GND
R105 1.74K
R106 1.74K
VCC5V0
HDMI OUT
ADV7511KSTZ
IC6
HD-D15
HD-D14
HD-D13
HD-D12
HD-D11
HD-D10
HD-D9
HD-D8
HD-D7
HD-D6
HD-D5
HD-D4
HD-D3
HD-D2
HD-D1
HD-D0
HD-DE
HD-CLK
HD-VSYNC
HD-HSYNC
TX2+
TX2-
TX1+
TX1-
TX0+
TX0-
TXC+
TXC-
CEC
CEC_CLK
DDCSCL
DDCSDA
HEAC+
HEAC-
HPD
SPDIF
SPDIF_OUT
MCLK
I2S0
I2S1
I2S2
I2S3
SCLK
LRCLK
SDA
SCL
INT
R_EXT
PD
1uF C27
1uF C28
D15
PESD0402-140
R107 10K
R108 0
No Load
J9 5-1903015-1
SHIELD
R109 50
IC5
OUT
VDD
GND
EN
767-12-68
C29 10nF
HD-SPDIF
HD-SPDIFO
R116 2K
R117 2K
R118 2K
HD-SDA
HD-SCL
HD-INT
I2C Address 0111001 R/W
R125 887
C30 0
No Load
VGA-R1
VGA-R2
VGA-R3
VGA-R4
VGA-G1
VGA-G2
VGA-G3
VGA-G4
VGA-B1
VGA-B2
VGA-B3
VGA-B4
VGA-HS
VGA-VS
R110 4K
R111 2K
R112 1K
R113 510
R114 4K
R115 2K
R119 1K
R120 510
R121 4K
R122 2K
R123 1K
R124 510
R126 100
R127 100
J10
DB15F
1-1734530-3
VCC1V8
FB2 600
DVDD
C31 10nF
C32 10nF
C33 10nF
C34 10nF
C35 10nF
C36 0.1uF
C37 0.1uF
C38 0.1uF
C39 1uF
C40 10uF
FB4 600
AVDD
C46 10nF
C47 10nF
C48 10nF
C49 10nF
C50 10nF
C51 0.1uF
C52 0.1uF
C53 0.1uF
C54 1uF
C55 10uF
FB3 600
PLVDD
C41 10nF
C42 10nF
C43 0.1uF
C44 1uF
C45 10uF
FB5 600
MVDD
C56 10nF
C57 0.1uF
C58 10uF
Title
ZED
Rev
D.2
Copyright 2013
Circuit
HDMI and VGA
Doc#
500-248
Engineer EG
Author GMA
Date 3/4/2013
Sheet# 5 out of 17
DIGILENT
BEYOND THEORY

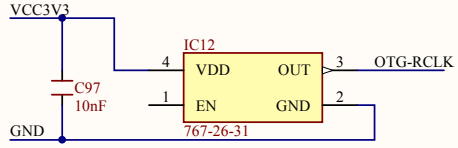

VCC3V3
FB6
220
ETHAVDD
C59 0.1uF
C60 10uF
GND
FB7
220
VCC1V8
C61 0.1uF
C62 0.1uF
C63 0.1uF
C64 4.7uF
VCC1V0
C65 0.1uF
C66 0.1uF
C67 4.7uF
C68 0.1uF
C69 0.1uF
C70 0.1uF
C71 0.1uF
C72 0.1uF
DVDD_OUT
DVDD
VDDO
REG_IN
AVDD18_OUT
AVDD18
AVDD33
AVDDC18
RX_CLK
RX_CTRL
RXD0
RXD1
RXD2
RXD3
TX_CLK
TX_CTRL
TXD0
TXD1
TXD2
TXD3
MDIO
MDC
CLK125
RESET
RSET
REGCAP1
REGCAP2
VSS
MDIP0
MDIN0
MDIP1
MDIN1
MDIP2
MDIN2
MDIP3
MDIN3
HSDACP
HSDACN
LED0
LED1
LED2/INT
CONFIG
XTAL_IN
XTAL_OUT
88E1518-XX-NNB2C000
IC7
ETH-RXCK
ETH-RXCTL
ETH-RXD0
ETH-RXD1
ETH-RXD2
ETH-RXD3
ETH-TXCK
ETH-TXCTL
ETH-TXD0
ETH-TXD1
ETH-TXD2
ETH-TXD3
ETH-MDIO
ETH-MDC
ETH-TD0 P
ETH-TD0 N
ETH-TD1 P
ETH-TD1 N
ETH-TD2 P
ETH-TD2 N
ETH-TD3 P
ETH-TD3 N
R128 4.7K
R129 55
R130 55
ETH-LDL
ETH-LDR
PS-POR-B
D16
R131 100K
R133 4.99K 1%
X1
25MHz
C76 39pF
C77 39pF
J11 Gigabit Ethernet
VCC
MD1+
MD1-
MD2+
MD2-
MD3+
MD3-
MD4+
MD4-
GND
LD2+
LD2-
LD1+
LD1-
SHD
M1
M2
SHIELD
10/100/1000 ETHERNET RJ-45
1840750-7
R132 10K
R134 10K
Q2
Q3
OLED-VBAT
OLED-VDD
C73 1uF
C74 1uF
C75 1uF
C78 1uF
DISP1
C2P
C2N
C1P
C1N
VBAT
VSS
VDD
CS
RES
D/C
SCLK
SDIN
IREF
VCOMH
VCC
128x32 OLED
UG-2832HSWEG04
OLED-RES
OLED-DC
OLED-SCLK
OLED-SDIN
R136 10K
R137 390K
C82 2.2uF
C83 2.2uF
C81 0.1uF
C79 0.1uF
C80 0.1uF
R135 4.7K
SD-D0
SD-D1
SD-D2
SD-D3
SD-CCLK-R
SD-CMD
SEL
R139 4.7K
VCCA
DAT0A
DAT1A
DAT2A
DAT3A
CLKA
CMDA
VCCB0
DAT0B0
DAT1B0
DAT2B0
DAT3B0
CLKB0
CMDB0
VCCB1
DAT0B1
DAT1B1
DAT2B1
DAT3B1
CLKB1
CMDB1
IC8
TXS02612RTWR
SD CARD
CD/DAT3/CS
CMD/DI
VSS1
VDD
CLK/SCLK
VSS2
DAT0/DO
DAT1
DAT2
CD
WP
S1
S2
S3
S4
CONNECTOR
J12
2041021-1
SD-CD
SD-WP
R138 499
R140 499
Title
ZED
Rev
D.2
Copyright 2013
Circuit
Ethernet, OLED and SD Card
Doc# 500-248
Engineer EG
Author GMA
Date 3/4/2013
Sheet# 6 out of 17
DIGILENT
BEYOND THEORY

TUSB1210 and Zynq-7000 have a timing incompatibility at hot temperature. Please see the ZedBoard Errata.



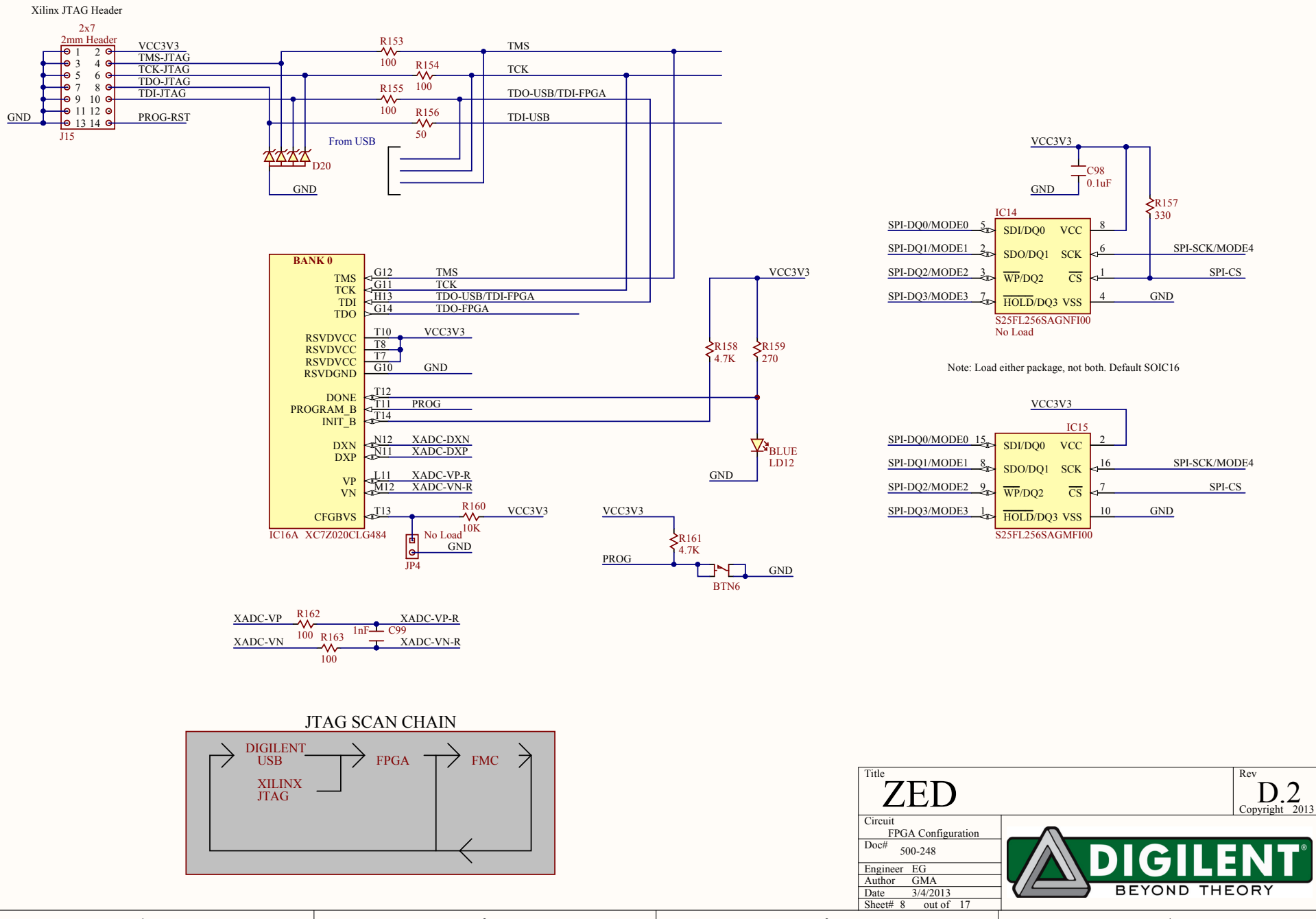


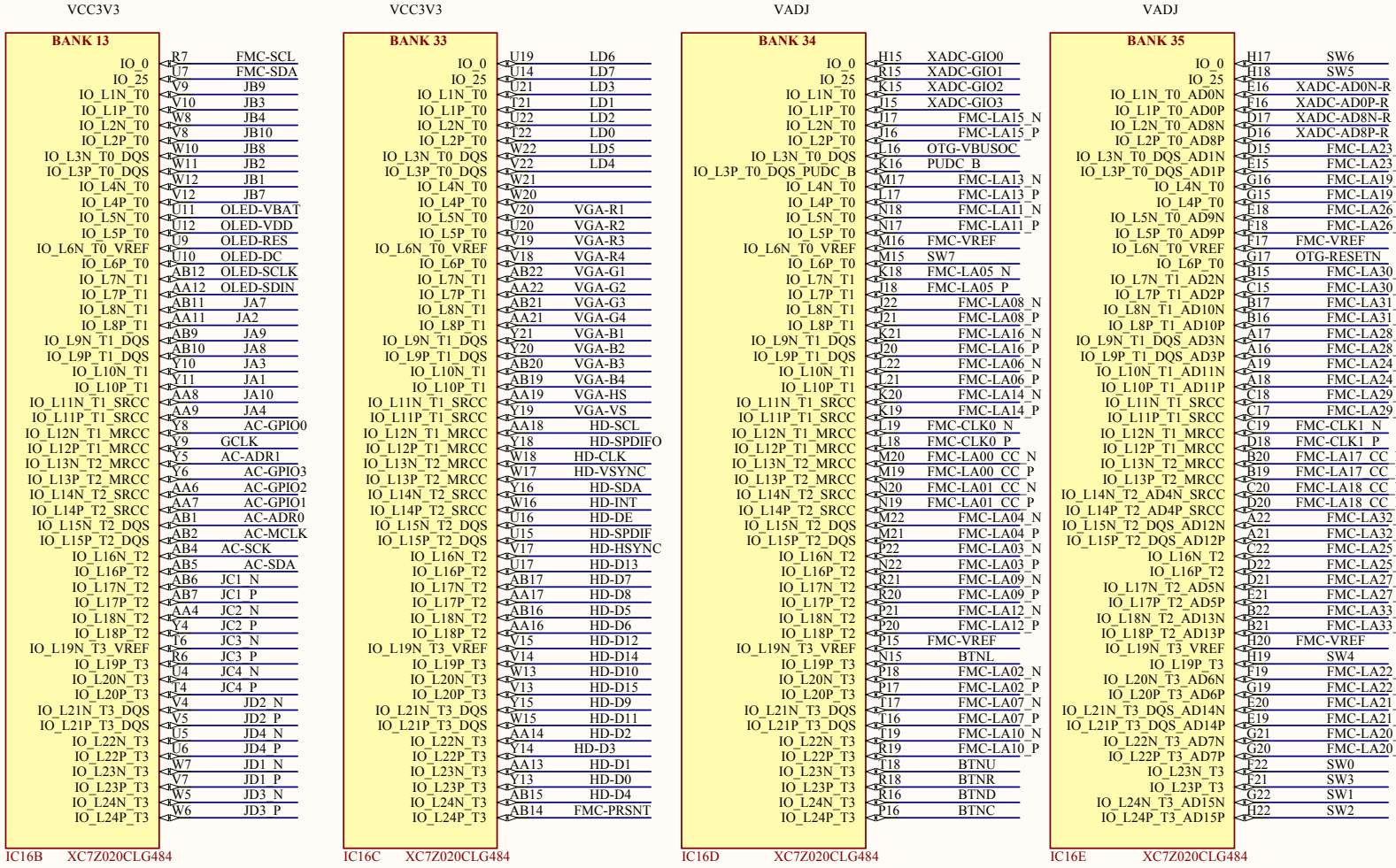


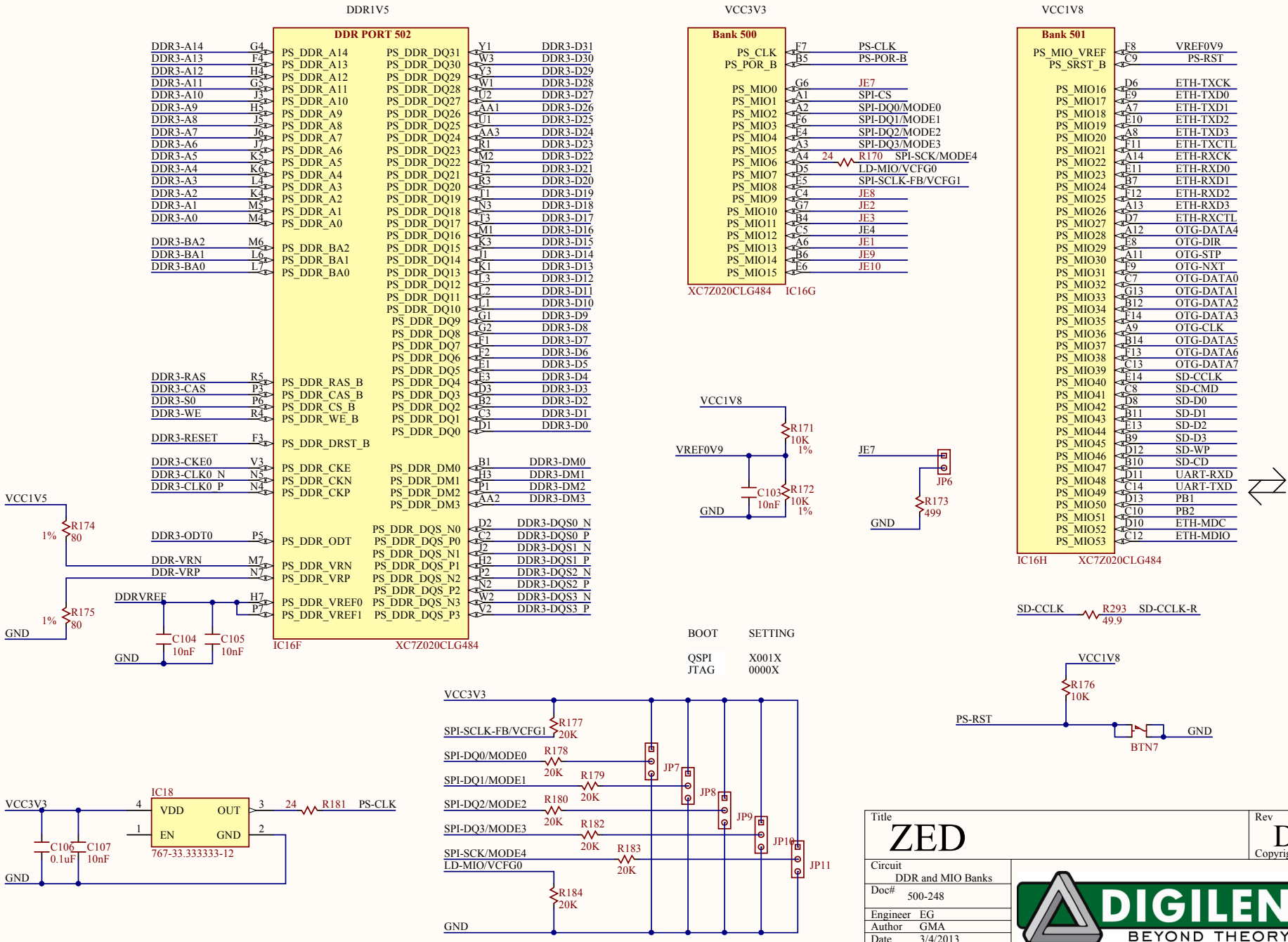


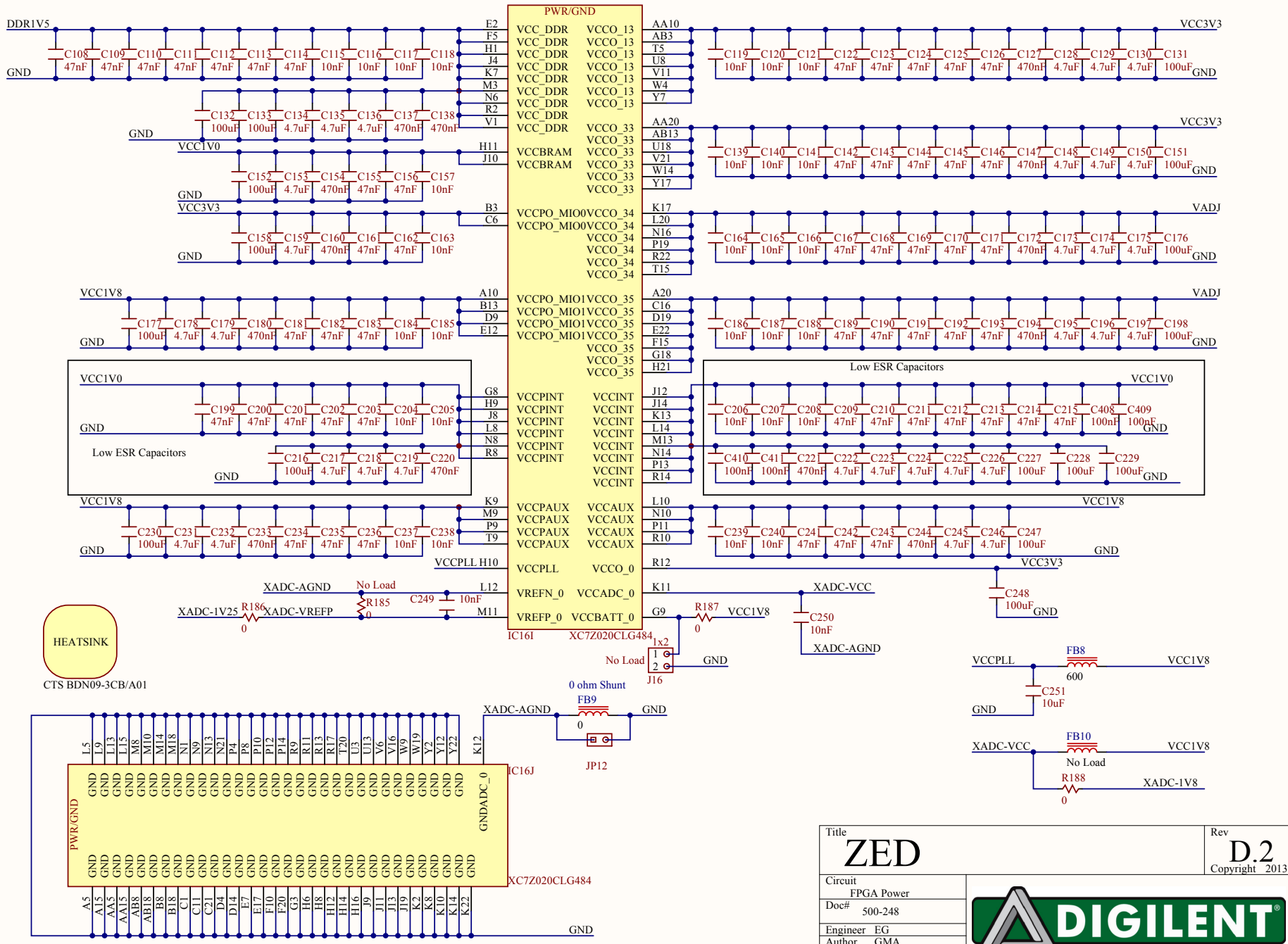
Title	ZED
Rev	D.2
Copyright	2013
Circuit	USB and UART
Doc#	500-248
Engineer	EG
Author	GMA
Date	3/4/2013
Sheet#	7 out of 17

DIGILENT BEYOND THEORY


Xilinx JTAG Header
2x7
2mm Header
J15
VCC3V3
TMS-JTAG
TCK-JTAG
TDO-JTAG
TDI-JTAG
PROG-RST
GND
R153
100
R154
100
R155
100
R156
50
TMS
TCK
TDO-USB/TDI-FPGA
TDI-USB
From USB
D20
GND
BANK 0
TMS
TCK
TDI
TDO
RSVDVCC
RSVDVCC
RSVDVCC
RSVDGND
DONE
PROGRAM_B
INIT_B
DXN
DXP
VP
VN
CFGBVS
G12 TMS
G11 TCK
H13 TDO-USB/TDI-FPGA
G14 TDO-FPGA
T10 VCC3V3
T8
T7
G10 GND
T12
T11 PROG
T14
N12 XADC-DXN
N11 XADC-DXP
L11 XADC-VP-R
M12 XADC-VN-R
T13
IC16A XC7Z020CLG484
R160
10K
No Load
JP4
VCC3V3
R158
4.7K
R159
270
BLUE
LD12
GND
VCC3V3
R161
4.7K
PROG
BTN6
GND
XADC-VP
R162
100
XADC-VP-R
1nF
C99
XADC-VN
R163
100
XADC-VN-R
VCC3V3
C98
0.1uF
GND
R157
330
IC14
SPI-DQ0/MODE0
SPI-DQ1/MODE1
SPI-DQ2/MODE2
SPI-DQ3/MODE3
SDI/DQ0
SDO/DQ1
WP/DQ2
HOLD/DQ3
VCC
SCK
CS
VSS
SPI-SCK/MODE4
SPI-CS
GND
S25FL256SAGNFI00
No Load
Note: Load either package, not both. Default SOIC16
VCC3V3
IC15
SPI-DQ0/MODE0
SPI-DQ1/MODE1
SPI-DQ2/MODE2
SPI-DQ3/MODE3
SDI/DQ0
SDO/DQ1
WP/DQ2
HOLD/DQ3
VCC
SCK
CS
VSS
SPI-SCK/MODE4
SPI-CS
GND
S25FL256SAGMFI00
JTAG SCAN CHAIN
DIGILENT
USB
XILINX
JTAG
FPGA
FMC
Title
ZED
Rev
D.2
Copyright 2013
Circuit
FPGA Configuration
Doc#
500-248
Engineer EG
Author GMA
Date 3/4/2013
Sheet# 8 out of 17
DIGILENT
BEYOND THEORY

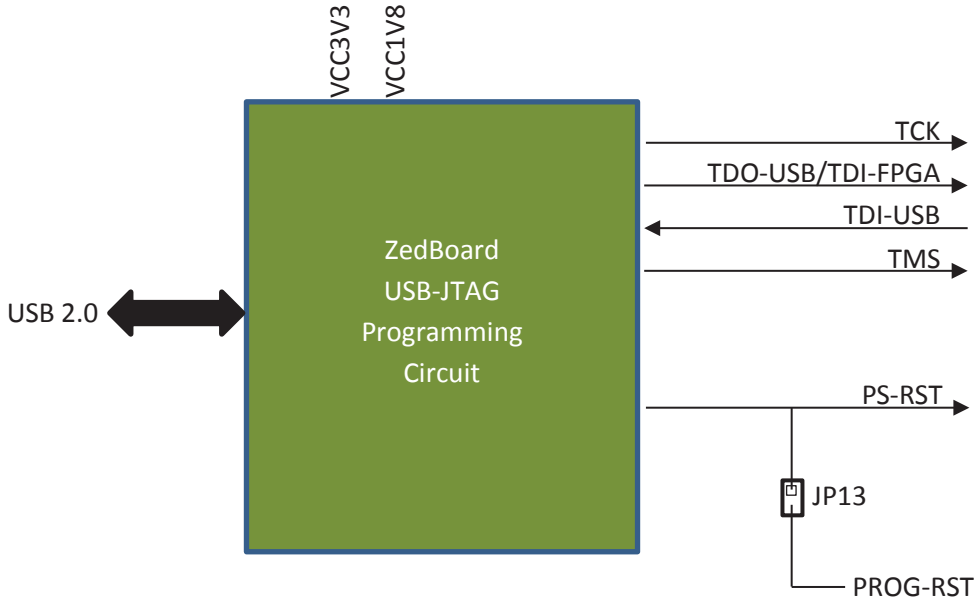

VCC3V3
BANK 13
IO_0 R7 FMC-SCL
IO_25 U7 FMC-SDA
IO_L1N_T0 V9 JB9
IO_L1P_T0 V10 JB3
IO_L2N_T0 W8 JB4
IO_L2P_T0 Y8 JB10
IO_L3N_T0_DQS W10 JB8
IO_L3P_T0_DQS W11 JB2
IO_L4N_T0 W12 JB1
IO_L4P_T0 V12 JB7
IO_L5N_T0 U11 OLED-VBAT
IO_L5P_T0 U12 OLED-VDD
IO_L6N_T0_VREF U9 OLED-RES
IO_L6P_T0 U10 OLED-DC
IO_L7N_T1 AB12 OLED-SCLK
IO_L7P_T1 AA12 OLED-SDIN
IO_L8N_T1 AB11 JA7
IO_L8P_T1 AA11 JA2
IO_L9N_T1_DQS AB9 JA9
IO_L9P_T1_DQS AB10 JA8
IO_L10N_T1 Y10 JA3
IO_L10P_T1 Y11 JA1
IO_L11N_T1_SRCC AA8 JA10
IO_L11P_T1_SRCC AA9 JA4
IO_L12N_T1_MRCC Y8 AC-GPIO0
IO_L12P_T1_MRCC Y9 GCLK
IO_L13N_T2_MRCC Y5 AC-ADR1
IO_L13P_T2_MRCC Y6 AC-GPIO3
IO_L14N_T2_SRCC AA6 AC-GPIO2
IO_L14P_T2_SRCC AA7 AC-GPIO1
IO_L15N_T2_DQS AB1 AC-ADR0
IO_L15P_T2_DQS AB2 AC-MCLK
IO_L16N_T2 AB4 AC-SCK
IO_L16P_T2 AB5 AC-SDA
IO_L17N_T2 AB6 JC1_N
IO_L17P_T2 AB7 JC1_P
IO_L18N_T2 AA4 JC2_N
IO_L18P_T2 Y4 JC2_P
IO_L19N_T3_VREF T6 JC3_N
IO_L19P_T3 R6 JC3_P
IO_L20N_T3 U4 JC4_N
IO_L20P_T3 T4 JC4_P
IO_L21N_T3_DQS Y4 JD2_N
IO_L21P_T3_DQS V5 JD2_P
IO_L22N_T3 U5 JD4_N
IO_L22P_T3 U6 JD4_P
IO_L23N_T3 W7 JD1_N
IO_L23P_T3 V7 JD1_P
IO_L24N_T3 W5 JD3_N
IO_L24P_T3 W6 JD3_P
IC16B XC7Z020CLG484
VCC3V3
BANK 33
IO_0 U19 LD6
IO_25 J14 LD7
IO_L1N_T0 U21 LD3
IO_L1P_T0 T21 LD1
IO_L2N_T0 T22 LD2
IO_L2P_T0 R22 LD0
IO_L3N_T0_DQS W22 LD5
IO_L3P_T0_DQS V22 LD4
IO_L4N_T0 W21
IO_L4P_T0 W20
IO_L5N_T0 V20 VGA-R1
IO_L5P_T0 U20 VGA-R2
IO_L6N_T0_VREF V19 VGA-R3
IO_L6P_T0 V18 VGA-R4
IO_L7N_T1 AB22 VGA-G1
IO_L7P_T1 AA22 VGA-G2
IO_L8N_T1 AB21 VGA-G3
IO_L8P_T1 AA21 VGA-G4
IO_L9N_T1_DQS Y21 VGA-B1
IO_L9P_T1_DQS Y20 VGA-B2
IO_L10N_T1 AB20 VGA-B3
IO_L10P_T1 AB19 VGA-B4
IO_L11N_T1_SRCC AA19 VGA-HS
IO_L11P_T1_SRCC Y19 VGA-VS
IO_L12N_T1_MRCC AA18 HD-SCL
IO_L12P_T1_MRCC Y18 HD-SPDIFO
IO_L13N_T2_MRCC W18 HD-CLK
IO_L13P_T2_MRCC W17 HD-VSYNC
IO_L14N_T2_SRCC Y16 HD-SDA
IO_L14P_T2_SRCC W16 HD-INT
IO_L15N_T2_DQS U16 HD-DE
IO_L15P_T2_DQS U15 HD-SPDIF
IO_L16N_T2 V17 HD-HSYNC
IO_L16P_T2 U17 HD-D13
IO_L17N_T2 AB17 HD-D7
IO_L17P_T2 AA17 HD-D8
IO_L18N_T2 AB16 HD-D5
IO_L18P_T2 AA16 HD-D6
IO_L19N_T3_VREF Y15 HD-D12
IO_L19P_T3 V14 HD-D14
IO_L20N_T3 W13 HD-D10
IO_L20P_T3 V13 HD-D15
IO_L21N_T3_DQS Y15 HD-D9
IO_L21P_T3_DQS W15 HD-D11
IO_L22N_T3 AA14 HD-D2
IO_L22P_T3 Y14 HD-D3
IO_L23N_T3 AA13 HD-D1
IO_L23P_T3 Y13 HD-D0
IO_L24N_T3 AB15 HD-D4
IO_L24P_T3 AB14 FMC-PRSNT
IC16C XC7Z020CLG484
VADJ
BANK 34
IO_0 H15 XADC-GIO0
IO_25 R15 XADC-GIO1
IO_L1N_T0 K15 XADC-GIO2
IO_L1P_T0 J15 XADC-GIO3
IO_L2N_T0 J17 FMC-LA15_N
IO_L2P_T0 J16 FMC-LA15_P
IO_L3N_T0_DQS L16 OTG-VBUSOC
IO_L3P_T0_DQS_PUDC_B K16 PUDC_B
IO_L4N_T0 M17 FMC-LA13_N
IO_L4P_T0 L17 FMC-LA13_P
IO_L5N_T0 N18 FMC-LA11_N
IO_L5P_T0 N17 FMC-LA11_P
IO_L6N_T0_VREF M16 FMC-VREF
IO_L6P_T0 M15 SW7
IO_L7N_T1 K18 FMC-LA05_N
IO_L7P_T1 J18 FMC-LA05_P
IO_L8N_T1 J22 FMC-LA08_N
IO_L8P_T1 J21 FMC-LA08_P
IO_L9N_T1_DQS K21 FMC-LA16_N
IO_L9P_T1_DQS J20 FMC-LA16_P
IO_L10N_T1 L22 FMC-LA06_N
IO_L10P_T1 L21 FMC-LA06_P
IO_L11N_T1_SRCC K20 FMC-LA14_N
IO_L11P_T1_SRCC K19 FMC-LA14_P
IO_L12N_T1_MRCC L19 FMC-CLK0_N
IO_L12P_T1_MRCC L18 FMC-CLK0_P
IO_L13N_T2_MRCC M20 FMC-LA00_CC_N
IO_L13P_T2_MRCC M19 FMC-LA00_CC_P
IO_L14N_T2_SRCC N20 FMC-LA01_CC_N
IO_L14P_T2_SRCC N19 FMC-LA01_CC_P
IO_L15N_T2_DQS M22 FMC-LA04_N
IO_L15P_T2_DQS M21 FMC-LA04_P
IO_L16N_T2 P22 FMC-LA03_N
IO_L16P_T2 N22 FMC-LA03_P
IO_L17N_T2 R21 FMC-LA09_N
IO_L17P_T2 R20 FMC-LA09_P
IO_L18N_T2 P21 FMC-LA12_N
IO_L18P_T2 P20 FMC-LA12_P
IO_L19N_T3_VREF P15 FMC-VREF
IO_L19P_T3 N15 BTNL
IO_L20N_T3 P18 FMC-LA02_N
IO_L20P_T3 P17 FMC-LA02_P
IO_L21N_T3_DQS J17 FMC-LA07_N
IO_L21P_T3_DQS J16 FMC-LA07_P
IO_L22N_T3 J19 FMC-LA10_N
IO_L22P_T3 R19 FMC-LA10_P
IO_L23N_T3 T18 BTNU
IO_L23P_T3 R18 BTNR
IO_L24N_T3 R16 BTND
IO_L24P_T3 P16 BTNC
IC16D XC7Z020CLG484
VADJ
BANK 35
IO_0 H17 SW6
IO_25 H18 SW5
IO_L1N_T0_AD0N E16 XADC-AD0N-R
IO_L1P_T0_AD0P F16 XADC-AD0P-R
IO_L2N_T0_AD8N D17 XADC-AD8N-R
IO_L2P_T0_AD8P D16 XADC-AD8P-R
IO_L3N_T0_DQS_AD1N D15 FMC-LA23_N
IO_L3P_T0_DQS_AD1P E15 FMC-LA23_P
IO_L4N_T0 G16 FMC-LA19_N
IO_L4P_T0 G15 FMC-LA19_P
IO_L5N_T0_AD9N E18 FMC-LA26_N
IO_L5P_T0_AD9P F18 FMC-LA26_P
IO_L6N_T0_VREF F17 FMC-VREF
IO_L6P_T0 G17 OTG-RESETN
IO_L7N_T1_AD2N B15 FMC-LA30_N
IO_L7P_T1_AD2P C15 FMC-LA30_P
IO_L8N_T1_AD10N B17 FMC-LA31_N
IO_L8P_T1_AD10P B16 FMC-LA31_P
IO_L9N_T1_DQS_AD3N A17 FMC-LA28_N
IO_L9P_T1_DQS_AD3P A16 FMC-LA28_P
IO_L10N_T1_AD11N A19 FMC-LA24_N
IO_L10P_T1_AD11P A18 FMC-LA24_P
IO_L11N_T1_SRCC C18 FMC-LA29_N
IO_L11P_T1_SRCC C17 FMC-LA29_P
IO_L12N_T1_MRCC C19 FMC-CLK1_N
IO_L12P_T1_MRCC D18 FMC-CLK1_P
IO_L13N_T2_MRCC B20 FMC-LA17_CC_N
IO_L13P_T2_MRCC B19 FMC-LA17_CC_P
IO_L14N_T2_AD4N_SRCC C20 FMC-LA18_CC_N
IO_L14P_T2_AD4P_SRCC D20 FMC-LA18_CC_P
IO_L15N_T2_DQS_AD12N A22 FMC-LA32_N
IO_L15P_T2_DQS_AD12P A21 FMC-LA32_P
IO_L16N_T2 C22 FMC-LA25_N
IO_L16P_T2 D22 FMC-LA25_P
IO_L17N_T2_AD5N D21 FMC-LA27_N
IO_L17P_T2_AD5P E21 FMC-LA27_P
IO_L18N_T2_AD13N B22 FMC-LA33_N
IO_L18P_T2_AD13P B21 FMC-LA33_P
IO_L19N_T3_VREF H20 FMC-VREF
IO_L19P_T3 H19 SW4
IO_L20N_T3_AD6N F19 FMC-LA22_N
IO_L20P_T3_AD6P G19 FMC-LA22_P
IO_L21N_T3_DQS_AD14N E20 FMC-LA21_N
IO_L21P_T3_DQS_AD14P E19 FMC-LA21_P
IO_L22N_T3_AD7N G21 FMC-LA20_N
IO_L22P_T3_AD7P G20 FMC-LA20_P
IO_L23N_T3 F22 SW0
IO_L23P_T3 F21 SW3
IO_L24N_T3_AD15N G22 SW1
IO_L24P_T3_AD15P H22 SW2
IC16E XC7Z020CLG484
PUDC_B
R164 1K
R165 10K
VADJ
No Load
JP5
GND
VCC3V3
C101 10nF
IC17
VDD
OUT
EN
GND
767-100-136
GCLK
GND
XADC-AD0_N
XADC-AD0_P
XADC-AD8_N
XADC-AD8_P
R166 100
R167 100
R168 100
R169 100
1nF C100
1nF C102
XADC-AD0N-R
XADC-AD0P-R
XADC-AD8N-R
XADC-AD8P-R
Title
ZED
Rev
D.2
Copyright 2013
Circuit
FPGA Banks
Doc# 500-248
Engineer EG
Author GMA
Date 3/4/2013
Sheet# 9 out of 17
DIGILENT
BEYOND THEORY


DDR1V5
DDR PORT 502
DDR3-A14 G4
DDR3-A13 F4
DDR3-A12 H4
DDR3-A11 G5
DDR3-A10 J3
DDR3-A9 H5
DDR3-A8 J5
DDR3-A7 J6
DDR3-A6 J7
DDR3-A5 K5
DDR3-A4 K6
DDR3-A3 L4
DDR3-A2 K4
DDR3-A1 M5
DDR3-A0 M4
DDR3-BA2 M6
DDR3-BA1 L6
DDR3-BA0 L7
DDR3-RAS R5
DDR3-CAS P5
DDR3-S0 P6
DDR3-WE R4
DDR3-RESET F3
DDR3-CKE0 V3
DDR3-CLK0_N N5
DDR3-CLK0_P N4
DDR3-ODT0 P5
DDR-VRN M7
DDR-VRP N7
DDRVREF H7
P7
PS_DDR_A14
PS_DDR_A13
PS_DDR_A12
PS_DDR_A11
PS_DDR_A10
PS_DDR_A9
PS_DDR_A8
PS_DDR_A7
PS_DDR_A6
PS_DDR_A5
PS_DDR_A4
PS_DDR_A3
PS_DDR_A2
PS_DDR_A1
PS_DDR_A0
PS_DDR_BA2
PS_DDR_BA1
PS_DDR_BA0
PS_DDR_RAS_B
PS_DDR_CAS_B
PS_DDR_CS_B
PS_DDR_WE_B
PS_DDR_DRST_B
PS_DDR_CKE
PS_DDR_CKN
PS_DDR_CKP
PS_DDR_ODT
PS_DDR_VRN
PS_DDR_VRP
PS_DDR_VREF0
PS_DDR_VREF1
PS_DDR_DQ31
PS_DDR_DQ30
PS_DDR_DQ29
PS_DDR_DQ28
PS_DDR_DQ27
PS_DDR_DQ26
PS_DDR_DQ25
PS_DDR_DQ24
PS_DDR_DQ23
PS_DDR_DQ22
PS_DDR_DQ21
PS_DDR_DQ20
PS_DDR_DQ19
PS_DDR_DQ18
PS_DDR_DQ17
PS_DDR_DQ16
PS_DDR_DQ15
PS_DDR_DQ14
PS_DDR_DQ13
PS_DDR_DQ12
PS_DDR_DQ11
PS_DDR_DQ10
PS_DDR_DQ9
PS_DDR_DQ8
PS_DDR_DQ7
PS_DDR_DQ6
PS_DDR_DQ5
PS_DDR_DQ4
PS_DDR_DQ3
PS_DDR_DQ2
PS_DDR_DQ1
PS_DDR_DQ0
PS_DDR_DM0
PS_DDR_DM1
PS_DDR_DM2
PS_DDR_DM3
PS_DDR_DQS_N0
PS_DDR_DQS_P0
PS_DDR_DQS_N1
PS_DDR_DQS_P1
PS_DDR_DQS_N2
PS_DDR_DQS_P2
PS_DDR_DQS_N3
PS_DDR_DQS_P3
Y1 DDR3-D31
W3 DDR3-D30
Y3 DDR3-D29
W1 DDR3-D28
U2 DDR3-D27
AA1 DDR3-D26
U1 DDR3-D25
AA3 DDR3-D24
R1 DDR3-D23
M2 DDR3-D22
T2 DDR3-D21
R3 DDR3-D20
T1 DDR3-D19
N3 DDR3-D18
T3 DDR3-D17
M1 DDR3-D16
K3 DDR3-D15
J1 DDR3-D14
K1 DDR3-D13
L3 DDR3-D12
L2 DDR3-D11
L1 DDR3-D10
G1 DDR3-D9
G2 DDR3-D8
F1 DDR3-D7
F2 DDR3-D6
E1 DDR3-D5
E3 DDR3-D4
D3 DDR3-D3
B2 DDR3-D2
C3 DDR3-D1
D1 DDR3-D0
B1 DDR3-DM0
H3 DDR3-DM1
P1 DDR3-DM2
AA2 DDR3-DM3
D2 DDR3-DQS0_N
C2 DDR3-DQS0_P
J2 DDR3-DQS1_N
H2 DDR3-DQS1_P
P2 DDR3-DQS2_N
N2 DDR3-DQS2_P
W2 DDR3-DQS3_N
V2 DDR3-DQS3_P
IC16F
XC7Z020CLG484
VCC1V5
R174 1% 80
R175 1% 80
GND
C104 10nF
C105 10nF
VCC3V3
Bank 500
PS_CLK F7
PS_POR_B B5
PS_MIO0 G6
PS_MIO1 A1
PS_MIO2 A2
PS_MIO3 F6
PS_MIO4 E4
PS_MIO5 A3
PS_MIO6 A4
PS_MIO7 D5
PS_MIO8 E5
PS_MIO9 C4
PS_MIO10 G7
PS_MIO11 B4
PS_MIO12 C5
PS_MIO13 A6
PS_MIO14 B6
PS_MIO15 E6
PS-CLK
PS-POR-B
JE7
SPI-CS
SPI-DQ0/MODE0
SPI-DQ1/MODE1
SPI-DQ2/MODE2
SPI-DQ3/MODE3
24 R170 SPI-SCK/MODE4
LD-MIO/VCFG0
SPI-SCLK-FB/VCFG1
JE8
JE2
JE3
JE4
JE1
JE9
JE10
XC7Z020CLG484 IC16G
VCC1V8
R171 10K 1%
VREF0V9
C103 10nF
R172 10K 1%
GND
JE7
JP6
R173 499
GND
VCC1V8
Bank 501
PS_MIO_VREF F8
PS_SRST_B C9
PS_MIO16 D6
PS_MIO17 E9
PS_MIO18 A7
PS_MIO19 E10
PS_MIO20 A8
PS_MIO21 F11
PS_MIO22 A14
PS_MIO23 E11
PS_MIO24 B7
PS_MIO25 F12
PS_MIO26 A13
PS_MIO27 D7
PS_MIO28 A12
PS_MIO29 E8
PS_MIO30 A11
PS_MIO31 F9
PS_MIO32 C7
PS_MIO33 G13
PS_MIO34 B12
PS_MIO35 F14
PS_MIO36 A9
PS_MIO37 B14
PS_MIO38 F13
PS_MIO39 C13
PS_MIO40 E14
PS_MIO41 C8
PS_MIO42 D8
PS_MIO43 B11
PS_MIO44 E13
PS_MIO45 B9
PS_MIO46 D12
PS_MIO47 B10
PS_MIO48 D11
PS_MIO49 C14
PS_MIO50 D13
PS_MIO51 C10
PS_MIO52 D10
PS_MIO53 C12
VREF0V9
PS-RST
ETH-TXCK
ETH-TXD0
ETH-TXD1
ETH-TXD2
ETH-TXD3
ETH-TXCTL
ETH-RXCK
ETH-RXD0
ETH-RXD1
ETH-RXD2
ETH-RXD3
ETH-RXCTL
OTG-DATA4
OTG-DIR
OTG-STP
OTG-NXT
OTG-DATA0
OTG-DATA1
OTG-DATA2
OTG-DATA3
OTG-CLK
OTG-DATA5
OTG-DATA6
OTG-DATA7
SD-CCLK
SD-CMD
SD-D0
SD-D1
SD-D2
SD-D3
SD-WP
SD-CD
UART-RXD
UART-TXD
PB1
PB2
ETH-MDC
ETH-MDIO
IC16H XC7Z020CLG484
SD-CCLK R293 49.9 SD-CCLK-R
VCC1V8
R176 10K
PS-RST
BTN7
GND
BOOT SETTING
QSPI X001X
JTAG 0000X
VCC3V3
SPI-SCLK-FB/VCFG1 R177 20K
SPI-DQ0/MODE0 R178 20K
SPI-DQ1/MODE1 R179 20K
SPI-DQ2/MODE2 R180 20K
SPI-DQ3/MODE3 R182 20K
SPI-SCK/MODE4 R183 20K
LD-MIO/VCFG0 R184 20K
JP7
JP8
JP9
JP10
JP11
GND
VCC3V3
IC18
VDD OUT
EN GND
767-33.333333-12
24 R181 PS-CLK
C106 0.1uF
C107 10nF
GND
Title
ZED
Rev
D.2
Copyright 2013
Circuit
DDR and MIO Banks
Doc# 500-248
Engineer EG
Author GMA
Date 3/4/2013
Sheet# 10 out of 17
DIGILENT
BEYOND THEORY



Title	ZED
Rev	D.2
Copyright	2013
Circuit	FPGA Power
Doc#	500-248
Engineer	EG
Author	GMA
Date	3/4/2013
Sheet#	11 out of 17

DIGILENT BEYOND THEORY



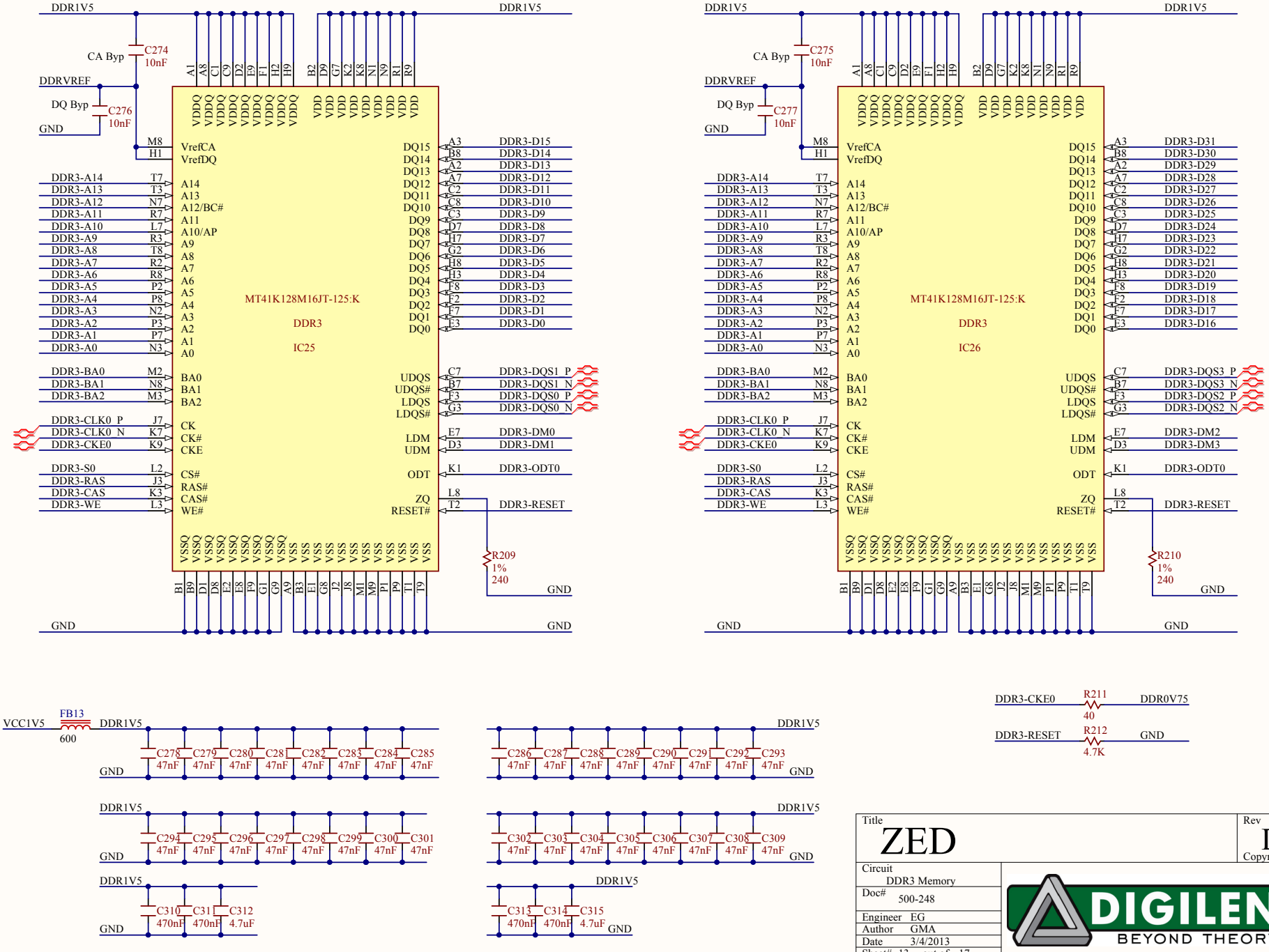
The ZedBoard contains a proprietary USB-JTAG circuit which is obscured on this sheet. This circuit contains IC19, IC20, IC21, IC22, IC23, IC24, JP13, and J17, along with a number of resistors and capacitors. The firmware for this circuit is not publicly available. However, the firmware does come pre-programmed in the SMT2 USB-JTAG module available from Digilent and Avnet. For more information, please see

www.em.avnet.com/jtagsmt2

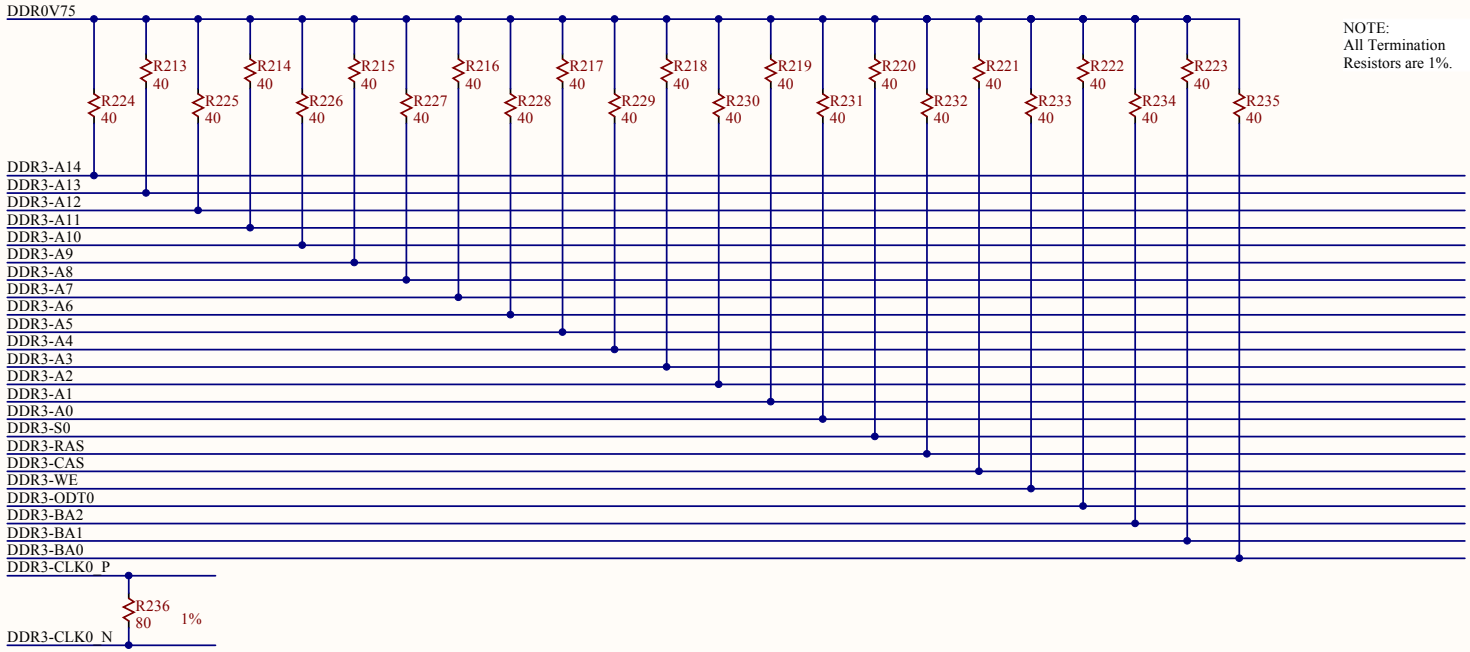
Title	ZED
Rev	D.2
Circuit	USB Programming
Doc#	500-248
Engineer	EG
Author	GMA
Date	3/4/2013
Sheet#	12 out of 17

Copyright 2013

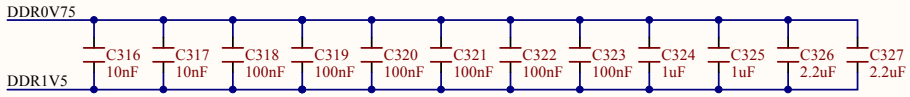
DIGILENT
BEYOND THEORY


DDR1V5
CA Byp
C274
10nF
DDRVREF
DQ Byp
C276
10nF
GND
MT41K128M16JT-125:K
DDR3
IC25
VrefCA
VrefDQ
A14
A13
A12/BC#
A11
A10/AP
A9
A8
A7
A6
A5
A4
A3
A2
A1
A0
BA0
BA1
BA2
CK
CK#
CKE
CS#
RAS#
CAS#
WE#
DQ15
DQ14
DQ13
DQ12
DQ11
DQ10
DQ9
DQ8
DQ7
DQ6
DQ5
DQ4
DQ3
DQ2
DQ1
DQ0
UDQS
UDQS#
LDQS
LDQS#
LDM
UDM
ODT
ZQ
RESET#
DDR3-A14
DDR3-A13
DDR3-A12
DDR3-A11
DDR3-A10
DDR3-A9
DDR3-A8
DDR3-A7
DDR3-A6
DDR3-A5
DDR3-A4
DDR3-A3
DDR3-A2
DDR3-A1
DDR3-A0
DDR3-BA0
DDR3-BA1
DDR3-BA2
DDR3-CLK0_P
DDR3-CLK0_N
DDR3-CKE0
DDR3-S0
DDR3-RAS
DDR3-CAS
DDR3-WE
DDR3-D15
DDR3-D14
DDR3-D13
DDR3-D12
DDR3-D11
DDR3-D10
DDR3-D9
DDR3-D8
DDR3-D7
DDR3-D6
DDR3-D5
DDR3-D4
DDR3-D3
DDR3-D2
DDR3-D1
DDR3-D0
DDR3-DQS1_P
DDR3-DQS1_N
DDR3-DQS0_P
DDR3-DQS0_N
DDR3-DM0
DDR3-DM1
DDR3-ODT0
DDR3-RESET
R209
1%
240
GND
C275
10nF
C277
10nF
IC26
DDR3-D31
DDR3-D30
DDR3-D29
DDR3-D28
DDR3-D27
DDR3-D26
DDR3-D25
DDR3-D24
DDR3-D23
DDR3-D22
DDR3-D21
DDR3-D20
DDR3-D19
DDR3-D18
DDR3-D17
DDR3-D16
DDR3-DQS3_P
DDR3-DQS3_N
DDR3-DQS2_P
DDR3-DQS2_N
DDR3-DM2
DDR3-DM3
R210
1%
240
VCC1V5
FB13
600
C278 C279 C280 C281 C282 C283 C284 C285
C286 C287 C288 C289 C290 C291 C292 C293
C294 C295 C296 C297 C298 C299 C300 C301
C302 C303 C304 C305 C306 C307 C308 C309
C310 C311 C312
C313 C314 C315
47nF
470nF
4.7uF
DDR3-CKE0
R211
40
DDR0V75
DDR3-RESET
R212
4.7K
Title
ZED
Rev
D.2
Copyright 2013
Circuit
DDR3 Memory
Doc#
500-248
Engineer EG
Author GMA
Date 3/4/2013
Sheet# 13 out of 17
DIGILENT
BEYOND THEORY

DDR3 TERMINATION



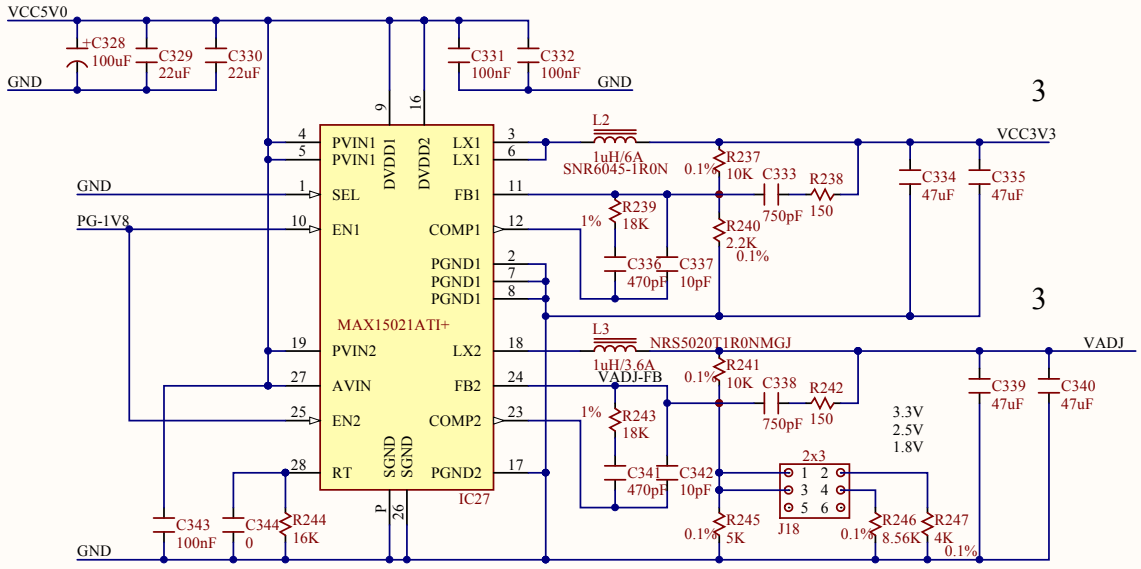
NOTE:
All Termination Resistors are 1%.

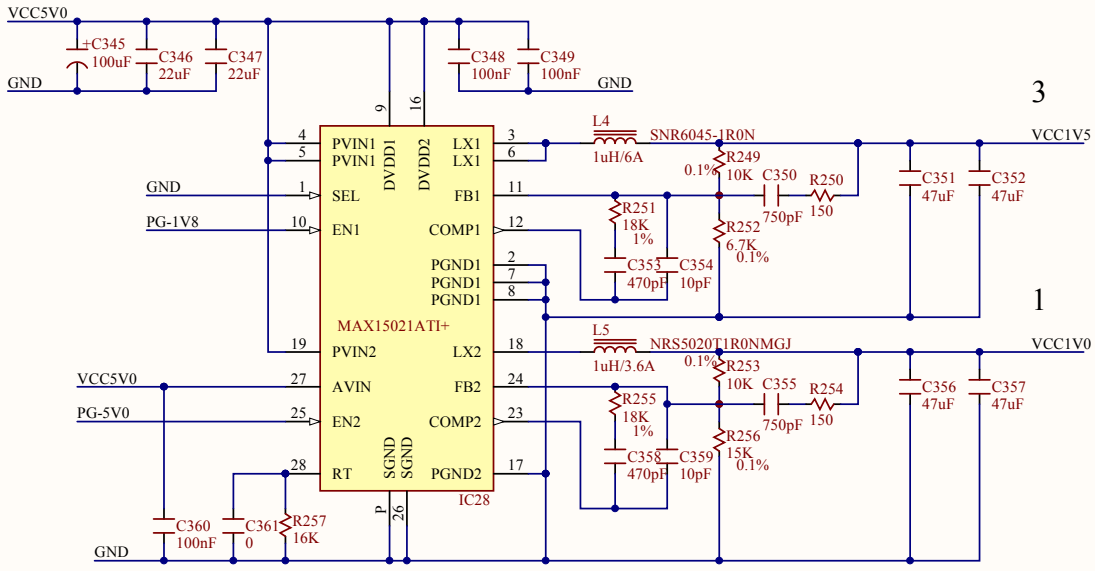


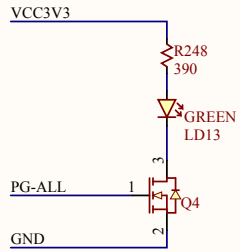
Title	ZED
Rev	D.2
Circuit	DDR3 Termination
Doc#	500-248
Engineer	EG
Author	GMA
Date	3/4/2013
Sheet#	14 out of 17

Copyright 2013

DIGILENT® BEYOND THEORY

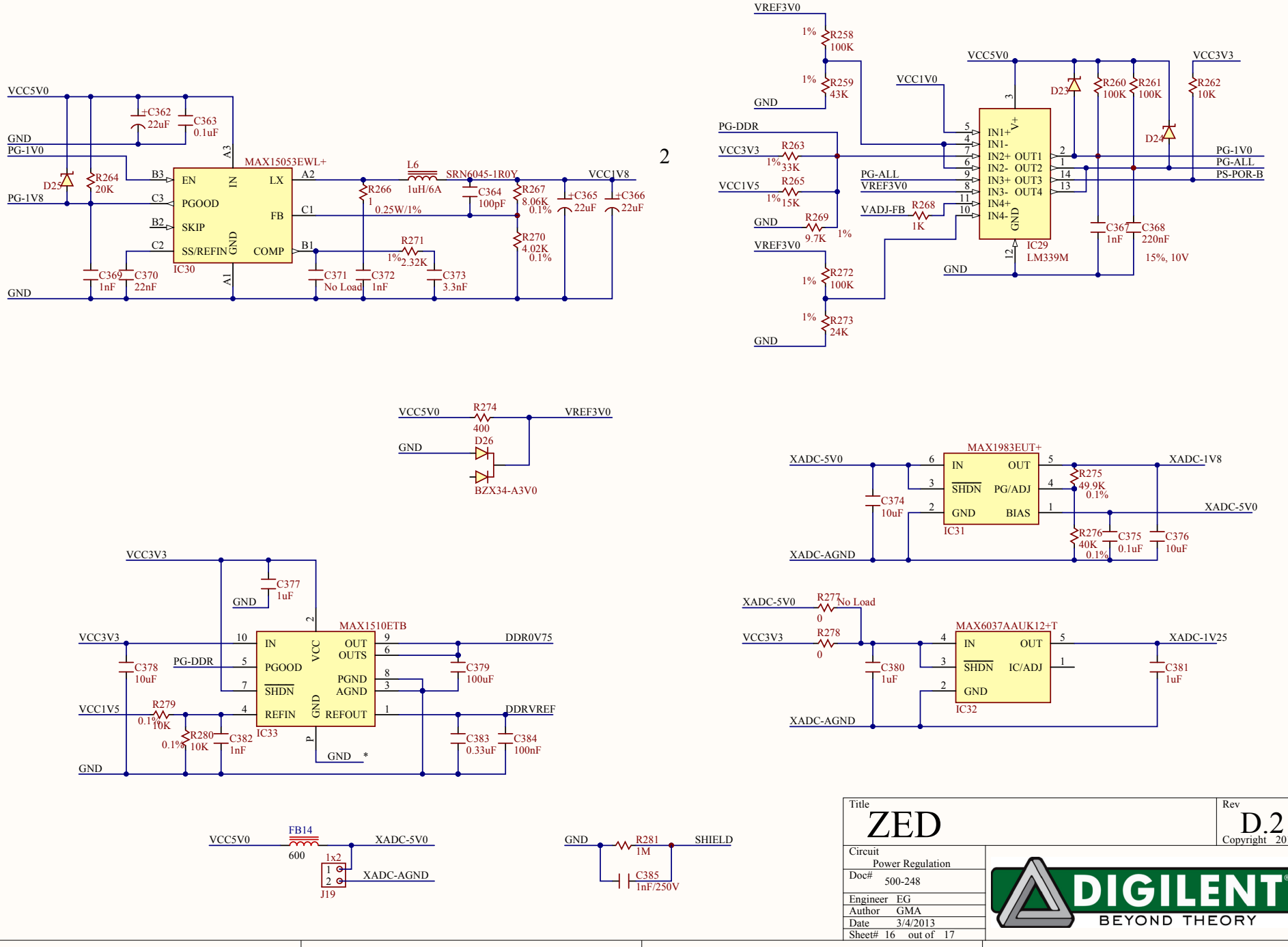






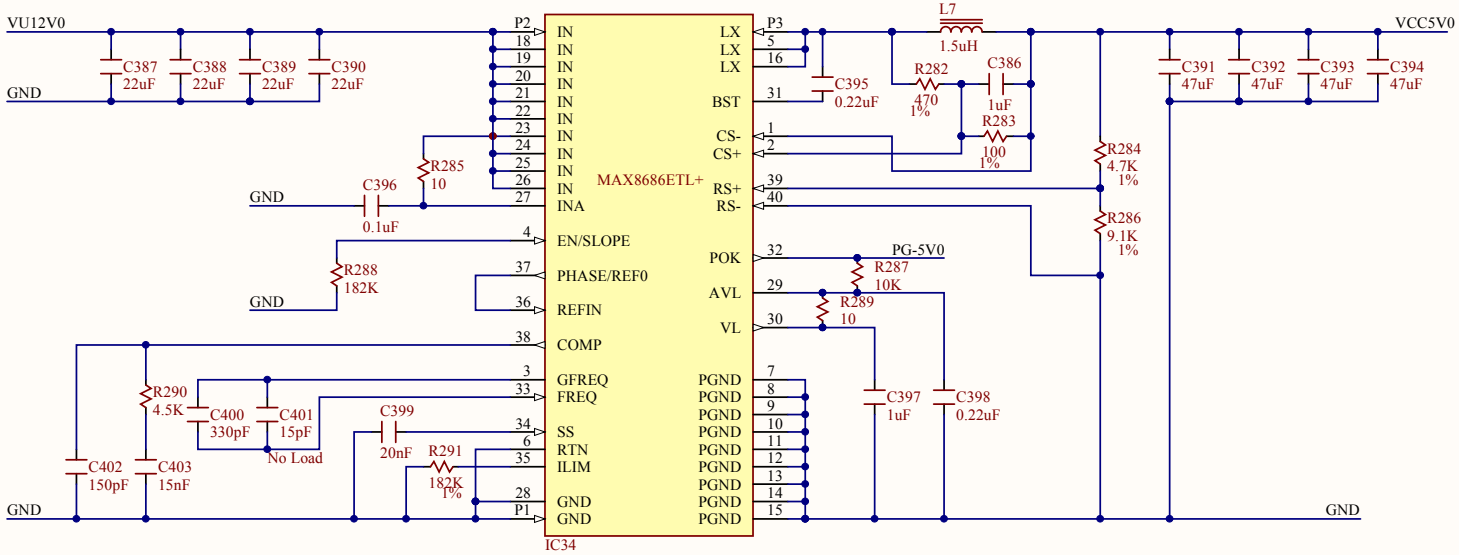
Title	ZED
Rev	D.2
Copyright	2013
Circuit	Power Regulation
Doc#	500-248
Engineer	EG
Author	GMA
Date	3/4/2013
Sheet#	15 out of 17

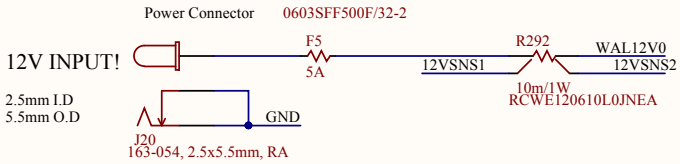
DIGILENT BEYOND THEORY

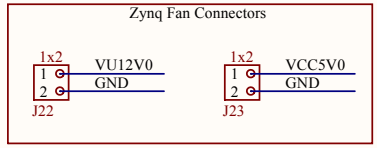


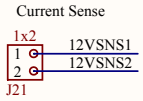
Title	ZED
Rev	D.2
Copyright	2013
Circuit	Power Regulation
Doc#	500-248
Engineer	EG
Author	GMA
Date	3/4/2013
Sheet#	16 out of 17

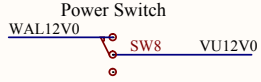
DIGILENT BEYOND THEORY











Title	ZED
Rev	D.2
Copyright	2013
Circuit	Power Regulation
Doc#	500-248
Engineer	EG
Author	GMA
Date	3/4/2013
Sheet#	17 out of 17

DIGILENT® BEYOND THEORY

Rev C.1 to D.2 Change History

Issue: Update Zynq to Production Silicon

PCB: no change.
Parts: load IC16 with XC7Z020-1CLG484C

Issue: Update DDR3 to newer device

PCB: no change.
Parts: load IC25 and IC26 with MT41K128M16JT-125:K

Issue: IC31 IN oscillates due to insufficient decoupling

PCB: change C374 pad size to 0603.
Parts: load C374 with 10uF 10V.

Issue: C89 incorrect value

PCB: no change
Parts: Load C89 with 150uF tantalum (already implemented)

Issue: Two DDR3 power/termination pins not in schematic part

PCB: fix DDR3 part to include two missing pins
Parts: no change

Issue: CKE signal pull-down revised

PCB: add 0402 resistor from CKE to VTT.
Parts: Load new resistor with 40ohm resistor.

Issue: SD Card clock requires termination resistor

PCB: add series termination resistor to SD Clock.
Parts: load new resistor with 50ohm resistor.

Issue: Heat issues

PCB: add two 1x2 pin headers (5V/GND and 12V/GND) to power a fan if needed
Parts: load headers; add heat sink

Issue: VBUS must connect to power pin on USB connector

PCB: move existing 0402 resistor between USB power pin and VBUS
Parts: no change

Issue: Parts not fitting pads (J12, L7)

PCB: Extended pads on L7 to accommodate larger parts
Parts: load only specified parts

Issue: HDMI signals radiate energy causing CE testing to fail

PCB: no change
Parts: add ferrite to HDMI cable

Issue: Replace RJ-45

PCB: no change.
Parts: load J11 with 1840750-7