# MT7687F DATASHEET

**Version:** 1.06

**Release date:** 23 May 2017

# Document Revision History

| Revision | Date | Description |
|---|---|---|
| 1.00 | 12 January 2016 | Initial version. |
| 1.01 | 10 May 2016 | 1. Modify section 1.2.3 for adding SIP flash information.<br>2. Modify table 4.2 for wider temperature specification.<br>3. Modify table 5.8 for wider temperature specification. |
| 1.02 | 04 November 2016 | Add the power performance summary. |
| 1.03 | 8 December 2016 | 1. Add SPI Slave description.<br>2. Update Auxilliary ADC specifications of Table 4-6 |
| 1.04 | 5 April 2017 | 1. Update GPIO description. |
| 1.05 | 5 May 2017 | 1. Remove SPI-M DMA description.<br>2. Updated Clock Generation Block Diagram. |
| 1.06 | 23 May 2017 | 1. Remove XTAL note in Boot Strap Test Mode of Chip Mode.<br>2. Updated Power States for CM4 Subsystem Wake-up time table.<br>3. Update I2S for Stereo & 44.1KHz/48KHz. |

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# 1 System Overview

## 1.1 General Description

MT7687F is a highly integrated single chip which features an application processor, a low power 1x1 11n single-band Wi-Fi subsystem, and a Power Management Unit. The application processor subsystem contains an ARM Cortex-M4 with floating point MCU. It also includes many peripherals, including UART, I2C, SPI, I2S, PWM, IrDA, and auxiliary ADC. It also includes embedded SRAM/ROM and a 2MB serial flash in package .

The Wi-Fi subsystem contains the 802.11b/g/n radio, baseband, and MAC that are designed to meet both the low power and high throughput application. It also contains a 32-bit RISC CPU that could fully offload the application processor.

## 1.2 Features

### 1.2.1 Technology and package

- 8mm x 8mm 68-pin QFN package.

### 1.2.2 Power management and clock source

- Integrate high efficiency power management unit with single 3.3V power supply input
- 40/26/52MHz source crystal clock support with low power operation in idle mode

### 1.2.3 Platform

- ARM Cortex-M4 MCU with FPU with up to 192MHz clock speed
- Embedded 352KB SRAM and 64KB boot ROM
- 2MB Quad Peripheral Interface (QPI) mode SIP serial Flash. Can also suppport external serial flash up to 16MB
- Supports eXecute In Place (XIP) on flash
- 32KB cache in XIP mode
- Hardware crypto engines including AES, DES/3DES, SHA2 for network security
- 28 General Purpose IOs  multiplexed with other interfaces
- Two UART interfaces with hardware flow control and one UART for debug, all multiplexed with GPIO
- One SPI master interface multiplexed with GPIO
- One SPI slave interface multiplexed with GPIO
- Two I2C master interface multiplexed with GPIO
- One I2S interface multiplexed with GPIO
- Four channel 12-bit ADC multiplexed with GPIO
- 28 PWM multiplexed with GPIO
- 25 channels DMA

- Low power RTC mode with 32KHz crystal support

### 1.2.4 WLAN

- Dedicated high-performance 32-bit RISC CPU N9 up to 160MHz clock speed
- IEEE 802.11 b/g/n compliant
- Supports 20MHz, 40MHz bandwidth in 2.4GHz band
- Dual-band 1T1R mode with data rate up to 150Mbps
- Supports STBC, LDPC
- Greenfield, mixed mode, legacy modes support
- IEEE 802.11e support
- Security support for WFA WPA/WPA2 personal, WPS2.0
- Supports 802.11w protected managed frames
- QoS support of WFA WMM
- Integrated LNA, PA, and T/R switch
- Optional external LNA and PA support.
- RX diversity support with additional RX input

### 1.2.5 Miscellaneous

- Integrates 4Kbit efuse to store device specific information and RF calibration data.

## 1.3 Applications

MT7687F is designed for Internet-of-Things based on the Mediatek's low power technology and Wi-Fi design.

## 1.4 Block Diagram

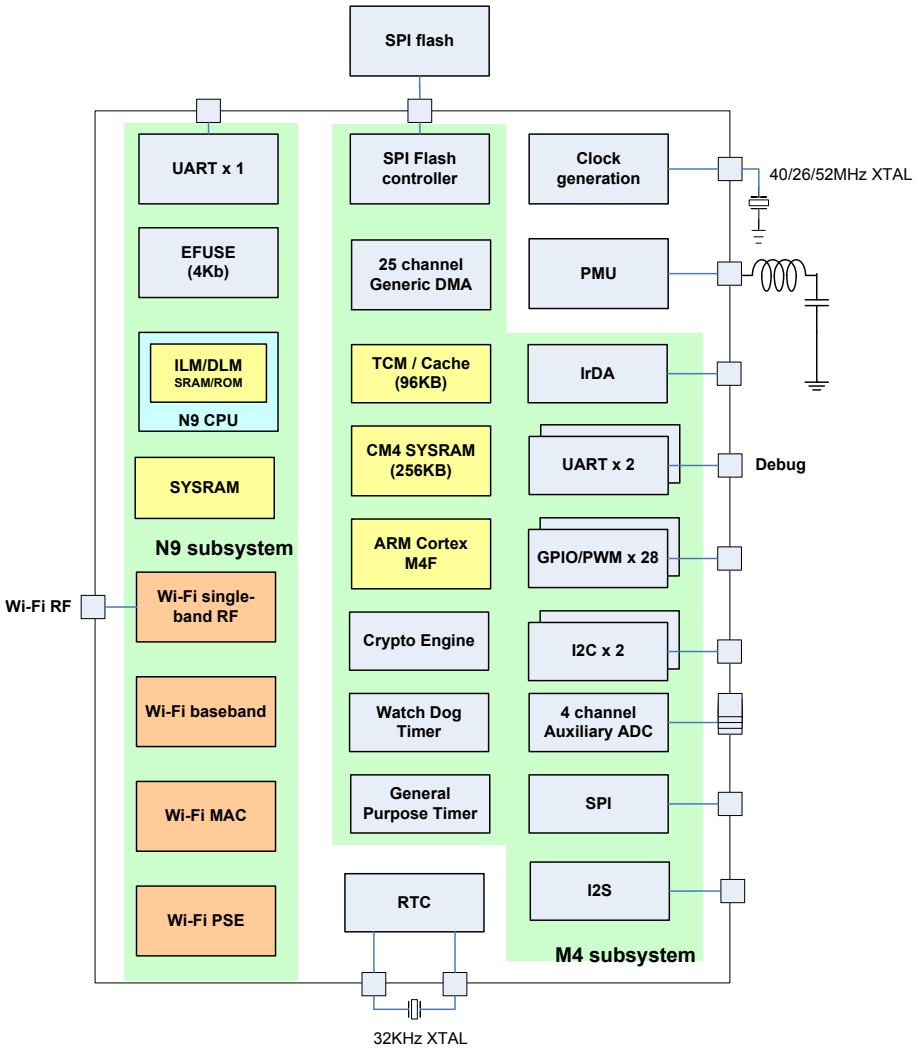



***Figure 1-1. System-on-Chip Block Diagram***

# 2 Functional Description

## 2.1 Overview

## 2.2 Power Management Unit

A single regulated 3.3V power supply is required for the MT7687F. It could be from DC-DC converter to convert higher voltage supply to 3.3V or boost from a lower voltage supply to 3.3V.

The Power Management Unit (PMU) contains Under-Voltage Lockout (UVLO) circuit, several Low Drop-out Regulators (LDOs), a highly efficient buck converter, and a reference band-gap circuit. The circuits are optimized for low quiescent current, low drop-out voltage, efficient line/load regulation, high ripple rejection, and low output noise.

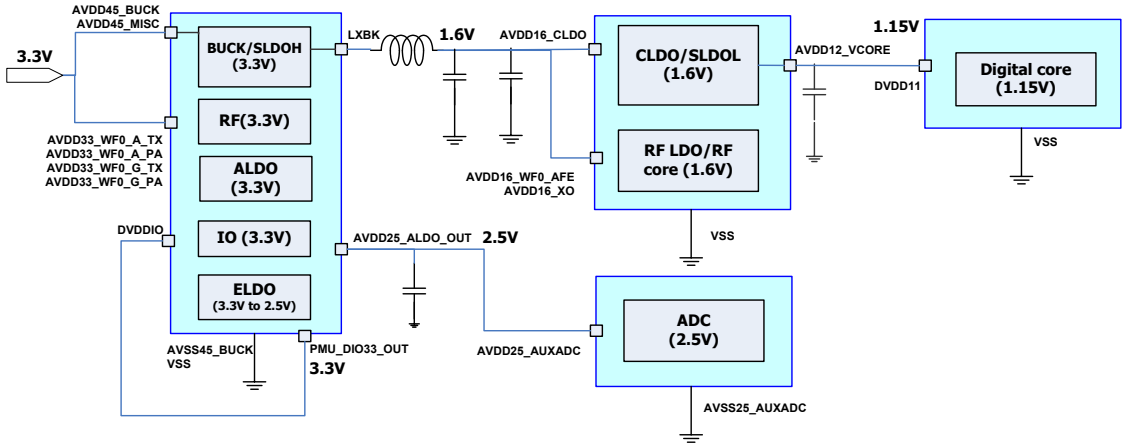



***Figure 2-1. Chip Power Block Diagram***

### 2.2.1 PMU Architecture

The PMU integrates 5 LDOs and one buck converter.

The four LDOs are CLDO, ALDO, high-voltage SLDO (SLDO-H) and low-voltage SLDO (SLDO-L). SLDO stands for sleep mode LDO, and CLDO stands for digital core LDO. The buck converter converts 1.6~1.8V output to other subsystems in MT7687F. It can be operated in PFM mode or PWM mode. Through an external on-board LC filter (2.2uH inductor and 10uF cap), it outputs a low ripple 1.6~1.8V to Wi-Fi RF system, and CLDO. CLDO is under BUCK domain, and then it outputs 1.15V for whole chip digital logics used. ALDO is also from 3.3V chip supply input and generates 2.5V for the auxiliary ADC. The two SLDOs have 1.8V and 0.85V output voltage respectively. They are used to keep BUCK and CLDO output voltage while MT7687F is in sleep mode to reduce current consumption.

Once MT7687F goes into deep sleep mode, BUCK, ALDO, and CLDO can be shut down. BUCK output voltage will be kept by SLDO-H, and CLDO output will be kept by SLDO-L.

PMU also integrated the ELDO (Efuse LDO). It provides 2.5V output voltage to the internal Efuse macro in programming mode.

### 2.2.2 Chip Power Plan

The 3.3V power source is directly supplied to the switching regulator, digital I/Os, and RF-related circuit. It is converted to 2.5V by the LDO for ADC analog circuit. It is converted to 1.6V by the buck converter for low voltage circuits. The built-in digital LDOs and RF LDOs converts 1.6V to 1.15V for digital, RF, and BBPLL core circuits.

### 2.2.3 Digital Power Domain and Power States

The digital circuit is separated into five power domains. They are TOP_AON, TOP_OFF(N9), WF_OFF and CM4_SYS. Except TOP_AON, each power domain can be turned on and off individually.

***Table 2-1. MTCMOS Power Domain***

| Domain | Description | Circuit Included | OFF Condition |
|---|---|---|---|
| TOP_AON | Always-on power domain, which keeps the minimum circuit powered to wake up from the sleep mode upon receiving a wake-up event. | It includes:<br>Chip level configuration register.<br>Sleep mode controller;<br>External interrupt controller;<br>Part of the Wi-Fi MAC that handles the beacon filtering.<br>Sustain and backup memory that stores the RAM code and the register values that need to be kept during sleep mode. | N/A |
| TOP_OFF(N9) | The power domain can be power gated in Wi-Fi power save mode. | The whole N9 subsystem, N9 peripherals, and part of the Wi-Fi MAC circuit are included. | N9 is in sleep mode and no DMA functions are enabled. |

| Domain | Description | Circuit Included | OFF Condition |
|---|---|---|---|
| WF_OFF | The power domain can be power gated when Wi-Fi is not used and in Wi-Fi power save mode. | The whole Wi-Fi baseband and part of the MAC subsystem are included. | Wi-Fi is disabled. N9 is in standby mode or in sleep mode. |
| CM4_OFF | The power domain is not powered gated when Cortex-M4 is used. | The whole Cortex-M4 subsystem and Cortex-M4 peripherals are included. | N/A |

The MT7687F power state diagram is illustrated below. There are two sleep mode controllers, controlled by N9 and CM4, respectively.

The N9 power state and CM4 power state operates independently. When both enter the sleep mode, the XTAL and PMU can be changed to the low power mode to further lower the current consumption.

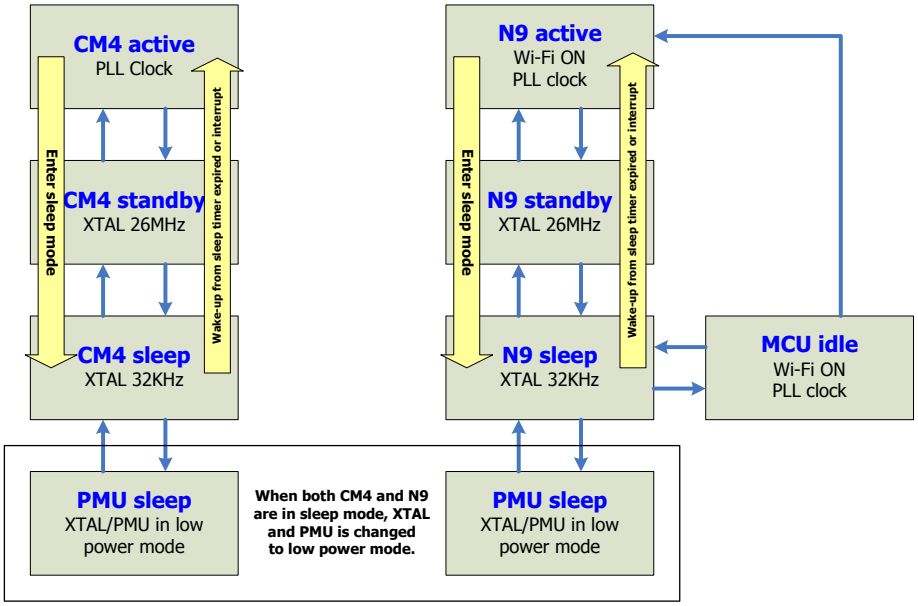



***Figure 2-2. MT7687F Power State***

***Table 2-2. Power States for CM4 Subsystem***

| MCU mode | Description | Wake-up time | Power |
|---|---|---|---|
| CM4 active | MCU executing code at PLL clock | n/a | |
| CM4 | MCU subsystem clocks are gated off and the state of the entire | 100 ns | |

| MCU mode | Description | Wake-up time | Power |
|---|---|---|---|
| standby | subsystem is retained. PLL is off. | (HCLK comes from XTAL) | |
| CM4 sleep | MCU subsystem clocks are gated off and the state of the entire subsystem is retained. Only 32KHz clock from XTAL is active. MCU is configured to wake up on the expiry of the internal timer and external wake-up events. | 850 us | 1mA |
| PMU sleep | CM4_OFF is power gated. XTAL and PMU operate in low power mode. MCU is configured to wake up on the expiry of the internal timer and external wake-up events. | 5.2 ms | 0.3mA |

***Table 2-3. Power States for N9 Subsystem***

| MCU mode | Description | Wake-up time | Power |
|---|---|---|---|
| N9 active | MCU executing code at PLL clock. | n/a | |
| MCU idle | MCU clock is gated off, while MCU subsystem clocks are on to maintain the operation of Wi-Fi function, like listening to beacon. PLL is on. | 800 ns | |
| N9 standby | MCU subsystem clocks are gated off and the state of the entire subsystem is retained. PLL is off. | 100 ns (HCLK comes from XTAL) | |
| N9 sleep | MCU subsystem clocks are gated off and the state of the entire subsystem is retained. Only 32KHz clock from XTAL is active. MCU is configured to wake up on the expiry of the internal timer, external wake-up events, or the wake-up events from Wi-Fi radio or Bluetooth ratio. | 1.2 ms | 1mA |
| PMU sleep | TOP_OFF (N9) and WF_OFF are power gated. XTAL and PMU operate in low power mode. The state information is retained in back-up buffer (sleep-mode memory) and can be restored when | 5.2 ms | 0.3mA |

| MCU mode | Description | Wake-up time | Power |
|---|---|---|---|
| | wake-up. MCU is configured to wake up on the expiry of the internal timer, external wake-up events, or the wake-up events from Wi-Fi radio or Bluetooth ratio. | | |

*XTAL: 40 MHz

The typical scenarios which N9 operates in and the power state transition are summarized in the following table.

***Table 2-4. Power State Transition Scenarios for N9***

| Scenario | Description | State transition |
|---|---|---|
| 1 | All functions are idle and the N9 firmware triggers to enter the sleep mode. | Active → Standby → Sleep |
| 2 | Wi-Fi DTIM timer is expired and the hardware wakes up to listen to beacon and then goes to sleep again when It is not necessary to wake up N9 to process the data. | Sleep → MCU idle (Wi-Fi ON) → sleep |
| 3 | Wi-Fi DTIM timer is expired and the hardware wakes up to listen to beacon and then wake up N9 to process the data. | Sleep → MCU idle (Wi-Fi ON) → Active |

The typical scenarios which CM4 operates in and the power state transition are summarized in the following table.

***Table 2-5. Power State Transition Scenarios for CM4***

| Scenario | Description | State transition |
|---|---|---|
| 1 | All functions are idle and the CM4 firmware triggers to enter the sleep mode. | Active → Standby → Sleep |
| 2 | The wake-up event (wake-up event from N9 or other sources) triggers CM4 to wake up. | Sleep → Standby → Active |

## 2.3 Clock and Reset Generation

### 2.3.1 Clock

MT7687F connects to the XTAL or external clock source as the single clock source of the whole system. The XTAL oscillator can support the XTAL frequencies from among 40, 26, and 52MHz.

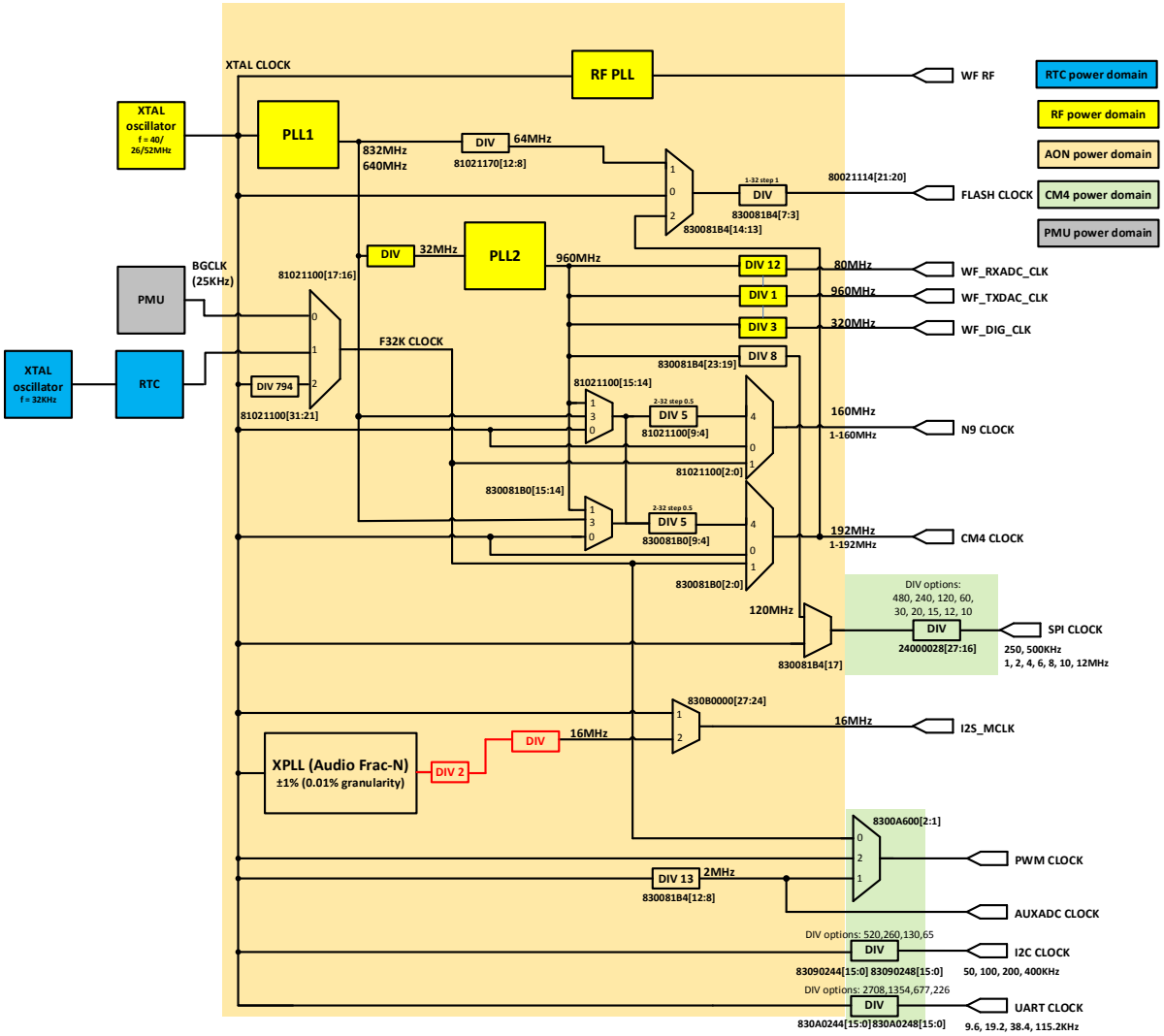



***Figure 2-3. Clock Generation Block Diagram***

- PLL1 is used to generate the clock sources for PLL2.
- PLL2 is used to generate the clock sources for Wi-Fi, N9 core, Cortex-M4 core, and bus fabric.
- XPLL is used to generate the clock sources for I2S (for external audio CODEC).

The options of clock rate for MCU are listed below.

***Table 2-6. Cortex-M4 Clock Rate***

| Reference Clock (MHz) | MCU Clock (MHz, XTAL mode) | MCU Clock (MHz, PLL mode) |
|---|---|---|
| 40 | 40 | 30, 32, 40, 48, 60, 80, 96, 120, 160, 192. |
| 26 | 26 | |
| 52 | 52 | |

***Table 2-7. N9 Clock Rate***

| Reference Clock (MHz) | MCU Clock (MHz, XTAL mode) | MCU Clock (MHz, PLL mode) |
|---|---|---|
| 40 | 40 | 30, 32, 40, 48, 60, 80, 96, 120, 160, 192. |
| 26 | 26 | |
| 52 | 52 | |

***Table 2-8. Peripheral Clock Rate***

| | Peripheral Clock Rate | Support SPEC |
|---|---|---|
| PWM | XTAL clock with DIV13 (Default) | 200Hz at minimum. |
| | XTAL clock | |
| | F32K clock | |
| UART | XTAL clock with DIV | 9.6, 19.2, 38.4, 115.2K |
| I2C | XTAL clock with DIV | 50, 100, 200, 400KHz |
| SPI | XTAL clock with DIV (Default) | 4, 6, 8, 10, 12MHz |
| Flash | XTAL clock with DIV (Default) | 64MHz. |
| | CM4 clock with DIV | |

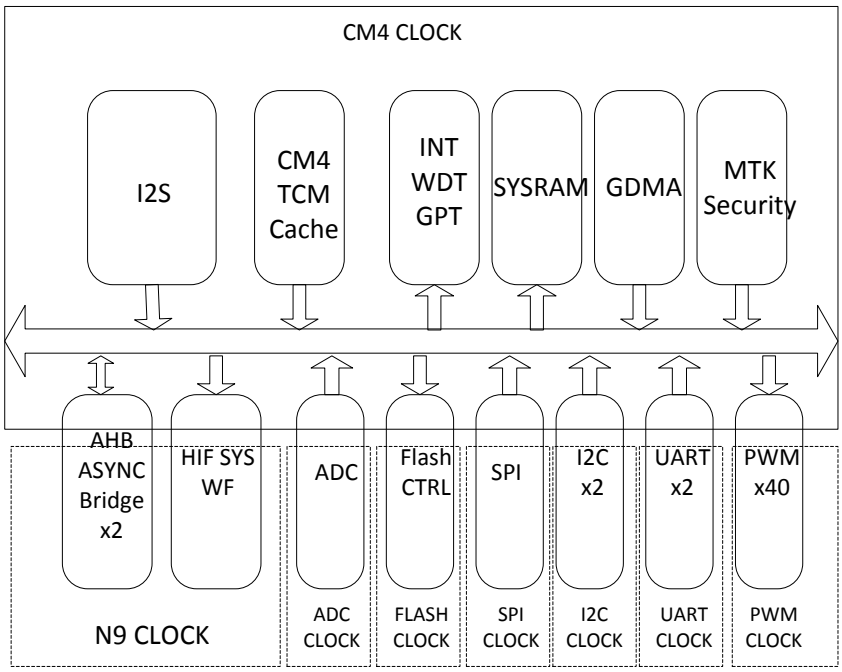



***Figure 2-4. Clock Domains in N9 and CM4 Peripherals***

### 2.3.2 Reset

MT7687F has three global resets: XRESETN, CM4_RESETN, and N9_RESETN. The figure below shows the module that the reset signals are applied to.

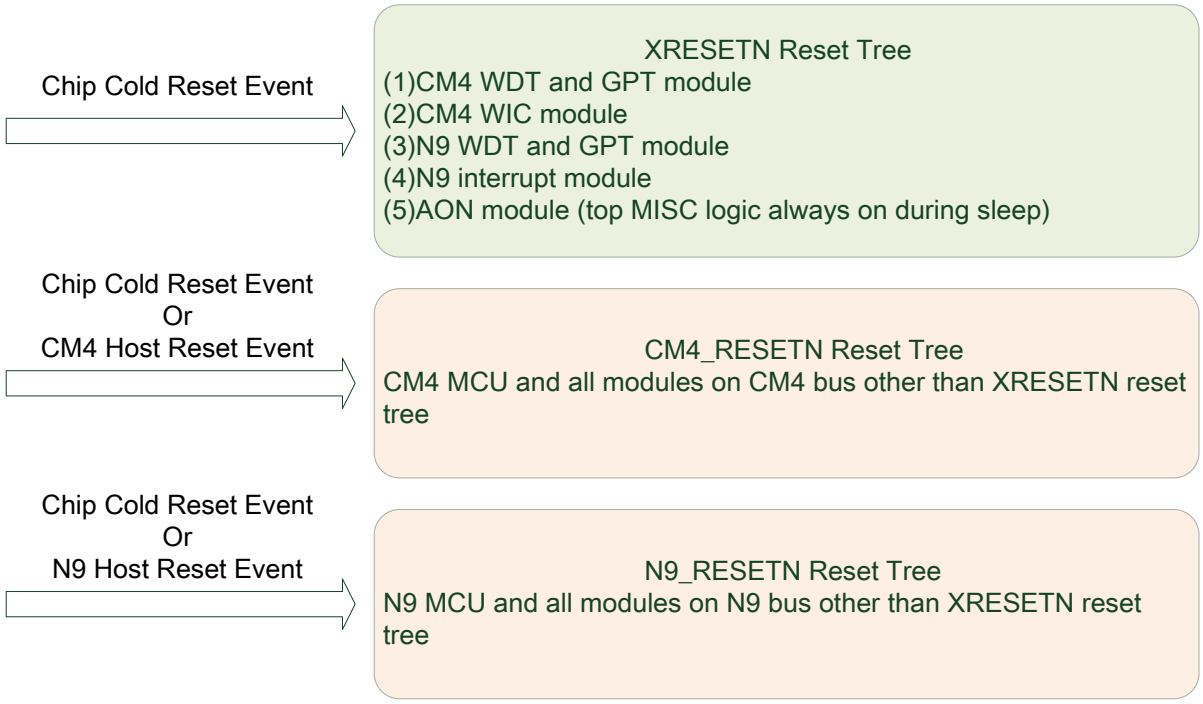



***Figure 2-5. Reset Structure***

## 2.4 Application Processor Subsystem

The MCU subsystem consists of a 32-bit MCU, the AHB/APB bus matrix, internal RAM/ROM with ROM patch function, the flash controller, and the system peripherals including Direct Memory Access (DMA) engine and the General Purpose Timer (GPT).

### 2.4.1 CPU

MT7687F features an ARM Cortex-M4 processor, which is the most energy efficient ARM processor available. It supports the clock rates from 1MHz up to 192MHz.

The MCU executes the Thump-2 instruction set for optimal performance and code size, including hardware division, single cycle multiplication, and bit-field manipulation.

MT7687F includes the memory protection unit (MPU) in Cortex-M4 MCU that provides memory protection features. It can be used to detect unexpected memory access.

MT7687F also includes floating point unit (FPU) in Corxex-M4 process to support DSP related function.

### 2.4.2 Cache and Tightly Coupled Memory

MT7687F has a cache for Cortex-M4 to improve the efficiency of the code and data fetch from the external flash. The only cacheable memory region is the external flash.

MT7687F also has a Tightly-Coupled-Memory (TCM), a zero-wait-state memory which is dedicated for Cortex-M4 and can be accessed by Cortex-M4 exclusively. It is a memory space for the critical code such as interrupt service routines which needs to be executed with minimum latency. The DMA engines on AHB bus can't access TCM.

The total size of memory of the cache and the TCM is 96KB. Four software-configurable options differ in the size of cache, the size of TCM, and the cache associativity. The user can select the option which maximizes the performance.

The cache system has the following features:

- Configurable 1/2/4-way set associative (8KB/16KB/32KB)
- Each way has 256 cache lines with 8-word link size
- 20-bit tag memory: 19-bit high address and 1-bit valid bit
- 2-bit dirty memory: each dirty bit identifies the dirtiness of half cache line

The size of SRAM is 96KB. It can be configured to the following configuration

- 96KB TCM, no cache
- 88KB TCM, 8KB cache (1 way, direct mapped)
- 80KB TCM, 16KB cache (2 way set-associative)
- 64KB TCM, 32KB cache (4 way set-associative)

The configuration setting and the memory configuration are shown in the following table.

***Table 2-9. TCM and Cache Configuration***

| 0x0153_0000[9:8] | Functional Description | Start Address | End Address |
|---|---|---|---|
| 00b | 96KB TCM, no cache | 0x0010_0000 | 0x0011_7FFF |
| 01b | 88KB TCM, 8KB cache, direct mapped | 0x0010_0000 | 0x0011_5FFF |
| 10b | 80KB TCM, 16KB cache, 2-way set-associative | 0x0010_0000 | 0x0011_3FFF |
| 11b | 64KB TCM, 32KB cache, 4-way set associative | 0x0010_0000 | 0x0010_FFFF |

The cache controller provides the user ways to perform cache operations including invalidate single/all cache lines as well as flush one/all cache lines.

To facilitate tuning the system performance, the cache controller can record the statistics of the cache hit count and the number of cacheable memory access. Cache hit rate can be obtained by dividing the cache hit count by the number of memory access.

### 2.4.3 Bus Fabric

MT7687F implements AHB/APB bus fabric to connect the MCU, memory, IO peripherals, and the radio subsystem.

- ILM/DLM: Instruction Local Memory / Data Local Memory, the zero-wait-state local memory for Radio MCU.
- Wi-Fi HIF: The data interface to Wi-Fi Packet switch engine.

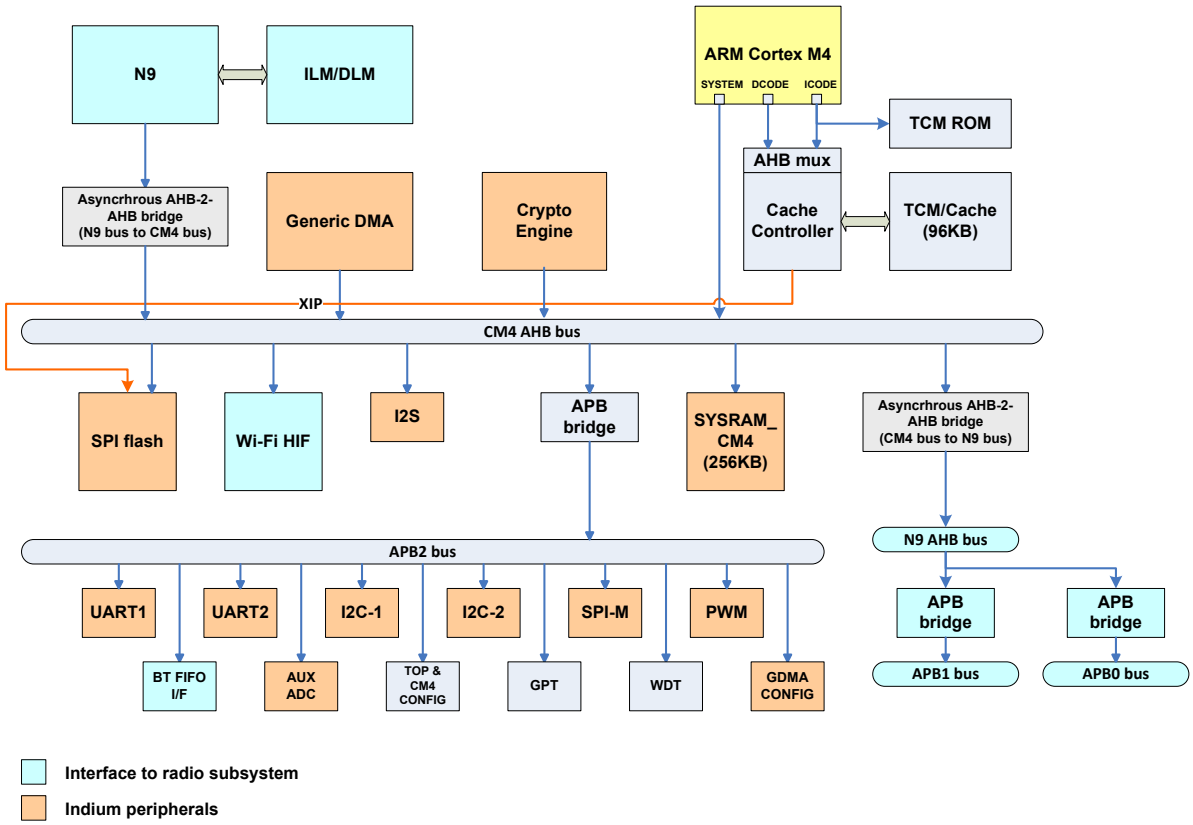



***Figure 2-6. CM4 Subsystem – Bus Fabric***

The AHB bus arbitration adopts round-robin scheme.

The N9 subsystem and Cortex-M4 subsystem are in different clock domains, so the asynchronous bridges are inserted in the bus fabric. N9 has the ability to (but would be rarely used) all the M4 peripherals.

### 2.4.4 Serial Flash Controller

MT7687F features a serial flash controller that can support the serial flash with the read mode of (JEDEC) standard SPI mode, SPI-Quad mode, QPI (Quad Peripheral Interface) mode, Dual IO mode, and Dual-Output mode.

The frequency of the serial clock rate is up to 64MHz. That provides 256Mbps equivalent throughput on flash when SPI-quad mode or QPI mode is used.

***Table 2-10. Flash Controller Support Read Mode***

| Read Mode | Description |
|---|---|
| SPI | 1xIO for receiving command and address, 1xIO for output data |
| SPI-Quad | 1xIO for receiving command, 4xIO for address, 4xIO for output data |
| QPI | 4xIO for receiving command/address and output data |
| Dual-IO | 1xIO for command, 2xIO for address and output data |
| Dual-Output | 1xIO for receiving command, 2xIO for address and output data |

The Serial Flash Controller Supports Two Operation Modes:

- Direct read mode, which supports a high-throughput direct-access through AHB bus
- Macro access mode, which supports flash access with arbitrary command and is through APB bus.

### 2.4.5 DMA

Direct memory access (DMA) is used to transfer data between memory ↔ memory as well as memory ↔ peripherals without MCU intervention.

#### 2.4.5.1 DMA Functional Description

There are three types of DMA channels supported in MT7687F.

- Full-size DMA: Both the source address and the destination address are programmable. It is normally used for memory copy.
- Half-size DMA: Either the source address or the destination address is programmable. It is normally used for data movement between memory and peripherals.
- Virtual FIFO DMA (VFF DMA): It is a half-size DMA with an additional FIFO control engine. It is used to provide the buffering capacity for peripherals including UART.

#### 2.4.5.1.1 Virtual FIFO

Virtual FIFO DMA is designed to offload the control of the serial interface. The difference between the virtual FIFO DMA and the full-size/half-size DMA is that the virtual DMA contains an additional FIFO controller.

The figure below illustrates the operations of virtual FIFO DMA used for UART RX.

- READ: DMA controller reads data from UART and increments the WRITE pointer of the FIFO controller.
- WRITE; DMA controller writes data that was area from UART to SRAM in the area defined before enabling the virtual FIFO.
- READ: MCU reads data when FIFO is not empty and the amount of data is over a pre-defined threshold. The read transaction will be finished only when DMA controller reads back the data from SRAM.
- READ: DMA controller reads data from SRAM and increments the READ pointer of the FIFO controller.

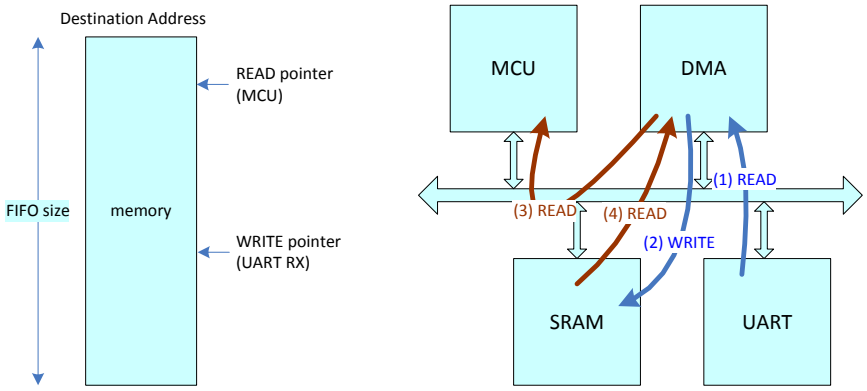



***Figure 2-7. Virtual FIFO Concept***

### 2.4.5.2 DMA Channels and Priority Control

There are two full-size DMA channels, 10 half- size DMA channels, and 13 virtual FIFO DMA channels in MT7687F.

***Table 2-11. DMA Use for Hardware Functions***

| Hardware Function | DMA Type |
|---|---|
| Radio (Wi-Fi) | Half size DMA x 1 |

| Hardware Function | DMA Type |
|---|---|
| UART (x2) | Virtual FIFO DMA x 4 |
| I2S | Virtual FIFO DMA x 2 |
| ADC | Virtual FIFO DMA x 1 |
| I2C (x2) | Half size DMA x 4 |
| Secure boot | Full size DMA x 1 |
| Reserved | Full size DMA x 1, half size DMA x 5 and virtual FIFO DMA x 4. |

The DMA provides two levels of scheduling scheme among all channels.

The 1st level scheduling follows the strict-priority scheme. All channels can be grouped into four priority groups. Group one gets the highest priority, then group two, and so on.

The 2nd level scheduling follows the round-robin scheme. Every channel in the same priority group has equal opportunity to use the bandwidth and was served sequentially.

The arbitration is done per AHB transaction. When one AHB transaction is finished, the scheduler will follow the above mechanism to select the next DMA channel to serve.

### 2.4.6 General Purpose Timer

MT7687F includes the General Purpose Timer (GPT).

Five independent timers are included. Timer 0, 1, and 3 are interrupt-based timers, while timer 2 and timer 4 are free-run timers.

Two modes are defined in interrupt-based timers:

- One-shot mode—the timer stops when the timer counts down to 0.
- Auto-repeat mode—the timer re-starts when the timer counts down to 0.

*Table 2-12. General Purpose Timer Types*

| | Mode | Clock speed | Interrupt Source |
|---|---|---|---|
| GPT0 | Interrupt-based | 1KHz or 32KHz | GPT |
| GPT1 | Interrupt-based | 1KHz or 32KHz | |
| GPT2 | Free-run | 1KHz or 32KHz | n/a |
| GPT3 | Interrupt based | 26MHz (oscillator clock) | GPT3 |
| GPT4 | Free-run | Bus clock or bus clock / 2 | n/a |

### 2.4.7 Watchdog Timer

MT7687F features the watchdog timer for CM4, which is used to recover the system to the initial status when the system hangs due to some malfunction.

WDT provides two ways to generate the WDT event:

- Triggered by the time-out event (by configuring WDT_MODE:0x83080030 and WDT_LENGTH:0x83080034). The WDT has an 11-bit counter and it uses the 32 KHz clock. The software regularly restarts the timer to prevent it from expiring. If it fails to restart the WDT, the timer would expire and generate a WDT event.
- Triggered by software programming (WDT_SWRST:0x83080044).

WDT provides the following options when a WDT event is generated:

- 0x83080030[3]=0: Reset mode

  - 0x8300917C[16] = 1: WDT whole chip mode. Reset the whole chip including CM4 and N9 subsystems.

  - 0x8300917C[16] = 0: WDT MCU mode. Reset CM4 subsystem only.

- 0x83080030[3]=1: Interrupt mode

  -Issue an interrupt to CM4 instead of resetting whole chip or CM4 subsystem.

The WDT module can only be reset by the external reset (SYS_RST_N) and the PMU reset. Some WDT control registers feature a key protection mechanism such that an unintentional access would be prevented.

WDT also provides the capability for CM4 software to interrupt N9 or reset N9 (by configuring WDT_DUAL_CORE:0x83080080).

### 2.4.8 Efuse

MT7687F uses embedded Efuse to store device specific configuration information such as MAC addresses, and power control settings.

The major fields defined in the Efuse:

- Wi-Fi MAC addresses
- Wi-Fi country code
- Wi-Fi TSSI parameters, TX power level
- Wi-Fi NIC configuration: RF front-end configuration, LED mode, baseband configuration

### 2.4.9 Interrupt Controller

MT7687F integrates the Nested Vectored Interrupt Controller (NVIC) for Cortex-M4. The NVIC supports

- Level and pulse detection of interrupt signals
- Configurable priority
- Wake-up interrupt controller (WIC) providing ultra-low power sleep mode support

#### 2.4.9.1 Interrupt Sources

The table below listed the NVIC and WIC interrupt sources. In total, there are 49 NVICs, while 23 of them are external interrupts multiplexed with GPIO functions.

The power domain/subsystem lists the power domain and the subsystem from which the interrupt is generated.

***Table 2-13. CM4 NVIC Interrupt Source***

| NVIC No. | Interrupt source | Power domain / subsystem | External interrupt | Wake-up capability (1) | De-bounce | Description |
|---|---|---|---|---|---|---|
| INT0 | UART1 | CM4_OFF/MCUSYS_CM4 | | | | UART 1 |
| INT1 | DMA_CM4 | CM4_OFF/MCUSYS_CM4 | | | | Generic DMA in CM4 subsystem |
| INT2 | HIF_CM4 | TOP_AON/HIFSYS | | V | | Wi-Fi host interface for CM4 |
| INT3 | I2C1 | CM4_OFF/MCUSYS_CM4 | | | | I2C 1 |
| INT4 | I2C2 | CM4_OFF/MCUSYS_CM4 | | | | I2C 2 |
| INT5 | UART2 | CM4_OFF/MCUSYS_CM4 | | | | UART 2 |
| INT6 | CRYPTO | CM4_OFF/MCUSYS_CM4 | | | | Crypto engine |
| INT7 | SF | CM4_OFF/MCUSYS_CM4 | | | | Serial flash controller, for debug |
| INT8 | (Reserved) | | | | | |
| INT9 | (Reserved) | | | | | |
| INT10 | WDT_CM4 | TOP_AON/MCUSYS_CM4 | | V | | Watchdog timer in CM4 subsystem |
| INT11 | N9_TO_CM4 | TOP_AON/MCUSYS_N9 | | V | | N9 software interrupt to CM4 |

| NVIC No. | Interrupt source | Power domain / subsystem | External interrupt | Wake-up capability (1) | De-bounce | Description |
|---|---|---|---|---|---|---|
| | _SW1 | | | | | |
| INT12 | SPI_S | CM4_OFF/MCUSYS_CM4 | | | | SPI slave |
| INT13 | WDT_N9 | TOP_AON/MCUSYS_N9 | | V | | Watchdog timer in N9 subsystem |
| INT14 | ADC | CM4_OFF/MCUSYS_CM4 | | | | Auxiliary ADC FIFO |
| INT15 | IRTX | CM4_OFF/MCUSYS_CM4 | | | | IrDA TX |
| INT16 | IRRX | CM4_OFF/MCUSYS_CM4 | | | | IrDA RX |
| INT17 | (Reserved) | | | | | |
| INT18 | (Reserved) | | | | | |
| INT19 | RTC_TIMER | RTC | | V | | RTC timer interrupt |
| INT20 | GPT3 | CM4_OFF/MCUSYS_CM4 | | V | | GPT3 time-out |
| INT21 | RTC_ALARM | RTC | | V | | RTC alarm interrupt |
| INT22 | (Reserved) | | | | | |
| INT23 | N9_TO_CM4 _SW2 | TOP_AON/MCUSYS_N9 | | V | | N9 software interrupt to CM4 |
| INT24 | GPT | TOP_CON/MCUSYS_CM4 | | V | | GPT0 or GPT1 time-out |
| INT25 | ADC_COMP | TOP_AON | | V | | ADC comparison mode |
| INT26 | (Reserved) | | | | | |
| INT27 | SPI | CM4_OFF/MCUSYS_CM4 | | | | SPI transaction |
| INT28 | (Reserved) | | | | | |
| INT29 | (Reserved) | | | | | |
| INT30 | (Reserved) | | | | | |
| INT31 | WIC | TOP_AON/MCUSYS_CM4 | | V (2) | | WIC WAKEUP interrupt CM4 |
| INT32 | SWD_CLK | TOP_AON | WIC[0] | V | Available | GPIO[2] |
| INT33 | I2C1_DATA | TOP_AON | WIC[1] | V | Available | GPIO[25] |
| INT34 | I2C0_CLK | TOP_AON | WIC[2] | V | Available | GPIO[27] |
| INT35 | I2S_MCLK_S PI_MOSI | TOP_AON | WIC[3] | V | Available | GPIO[29] |
| INT36 | I2S_BCLK_S PI_CS | TOP_AON | WIC[4] | V | Available | GPIO[32] |
| INT37 | ANT_SEL0 | TOP_AON | WIC[5] | V | Available | GPIO[33] |
| INT38 | ANT_SEL1 | TOP_AON | WIC[6] | V | Available | GPIO[34] |
| INT39 | GPIO17 | TOP_AON | WIC[7] | V | Available | GPIO[36] |
| INT40 | ADC0 | TOP_AON | WIC[8] | V | Available | GPIO[57] |
| INT41 | ADC1 | TOP_AON | WIC[9] | V | Available | GPIO[58] |
| INT42 | ADC2 | TOP_AON | WIC[10] | V | Available | GPIO[59] |

| NVIC No. | Interrupt source | Power domain / subsystem | External interrupt | Wake-up capability (1) | De-bounce | Description |
|---|---|---|---|---|---|---|
| INT43 | ADC3 | TOP_AON | WIC[11] | V | Available | GPIO[60] |
| INT56 | PWM0 | TOP_AON | EINT[0] | V | Available | GPIO[0] |
| INT57 | PWM1 | TOP_AON | EINT[1] | V | Available | GPIO[1] |
| INT58 | SWD_DIO | TOP_AON | EINT[2] | V | Available | GPIO[3] |
| INT59 | GPIO0 | TOP_AON | EINT[3] | V | Available | GPIO[4] |
| INT60 | GPIO1 | TOP_AON | EINT[4] | V | Available | GPIO[5] |
| INT61 | GPIO2 | TOP_AON | EINT[5] | V | Available | GPIO[6] |
| INT62 | GPIO3 | TOP_AON | EINT[6] | V | Available | GPIO[7] |
| INT75 | GPIO16 | TOP_AON | EINT[19] | V | Available | GPIO[35] |
| INT76 | GPIO18 | TOP_AON | EINT[20] | V | Available | GPIO[37] |
| INT77 | GPIO19 | TOP_AON | EINT[21] | V | Available | GPIO[38] |
| INT78 | GPIO20 | TOP_AON | EINT[22] | V | Available | GPIO[39] |

*Note 1; Capable to wake up CM4 when CM4 is in sleep mode*.

*Note 2: This interrupt is associated with other wake-up interrupts for CM4 to differentiate wake-up interrupts from non wake-up interrupts.*

#### 2.4.9.2 External Interrupt

MT7687F has the optionally enabled hardware de-bouncing circuit for each interrupt source.

***Table 2-14. CM4 External Interrupt De-Bounce Period***

| 3-bit prescaler | Reference clock rate for de-bounce counter (KHz) | Minimum de-bounce period (ms) | Maximum de-bounce period (ms) |
|---|---|---|---|
| 000 | 8 | 0.13 | 2 |
| 001 | 4 | 0.25 | 4 |
| 010 | 2 | 0.5 | 8 |
| 011 | 1 | 1 | 16 |

| 3-bit prescaler | Reference clock rate for de-bounce counter (KHz) | Minimum de-bounce period (ms) | Maximum de-bounce period (ms) |
|---|---|---|---|
| 100 | 0.5 | 2 | 32 |
| 101 | 0.25 | 4 | 64 |
| 110 | 0.125 | 8 | 128 |
| 111 | 0.0625 | 16 | 256 |

### 2.4.10 Power-on Sequence

The power-on control sequence diagram shows how the code reset (PMU_RESET_N) is generated on chip.

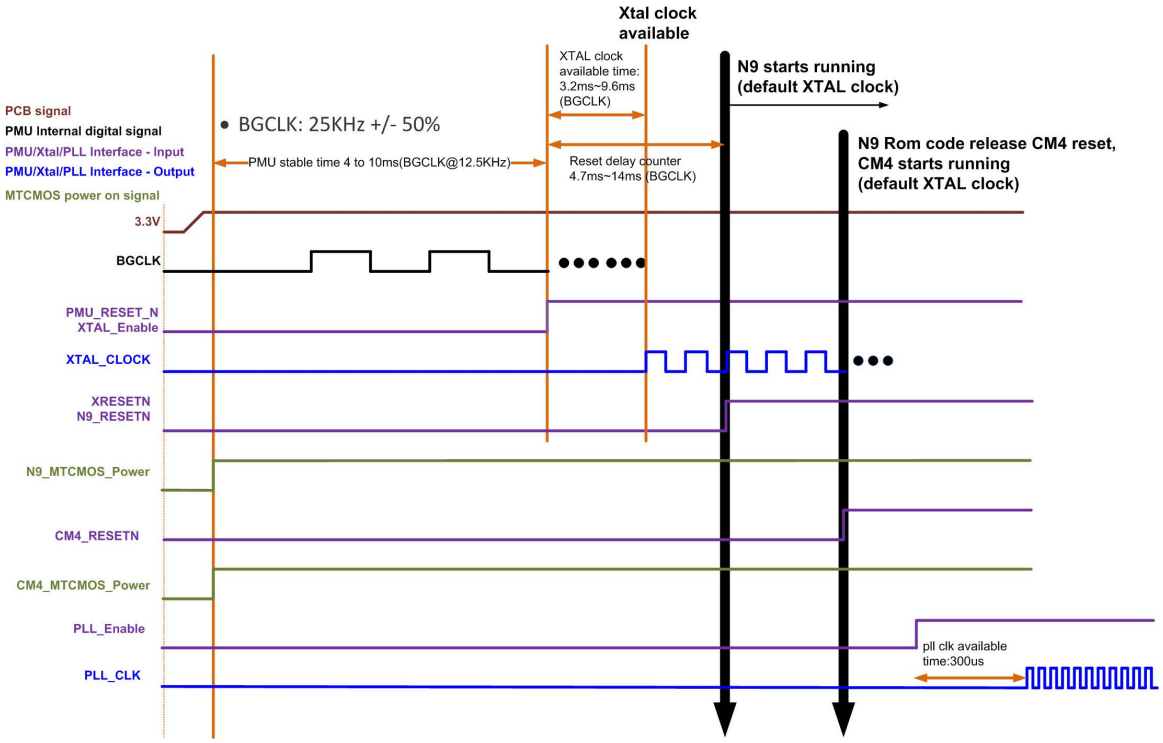



***Figure 2-8. PMU Power-on Sequence***

#### 2.4.10.1 Power-on Reset (Cold Reset)

The power on reset sequence after chip power on is shown below.

Step 1: N9 reset is de-asserted and boot from ROM (CM4 reset state is still asserted)

Step 2: N9 sets up top configuration registers (such as PLL) and then de-asserts CM4 reset

Step 3: CM4 boots from ROM while N9 polls the PDA (Patch Decryption Accelerator) status

Step 4: CM4 fetch flash header (N9 FW download length information)

Step 5: CM4 setup PDA and PDA address generator

Step 6: PDA loads firmware from the flash to N9 IDLM

Step 7: N9 executes from IDLM after PDA completes and CM4 executes from Cache/Flash or TCM.

### 2.4.10.2 Watchdog Reset

Watchdog reset WDT_N9 is the watchdog timer for N9, and WDT_CM4 is the watchdog timer for CM4.

When the WDT event of WDT_N9 occurs, WDT_N9 has the capability to

- Reset N9 or issue an interrupt to N9.
- Issue an interrupt to CM4 (can be masked by CM4 if it is not required to be received).

When the WDT event of WDT_CM4 occurs, WDT_CM4 has the capability to

- Reset whole chip or reset CM4 only or issue an interrupt to CM4.
- Issue an interrupt to N9 (can be masked by N9 if it's not required to be received).

For both WDT_N9 and WDT_CM4, the WDT events can be triggered by time-out and software programming.

For both WDT_N9 and WDT_CM4, the WDT has the capability to reset the other CPU or issue an interrupt to the other CPU.

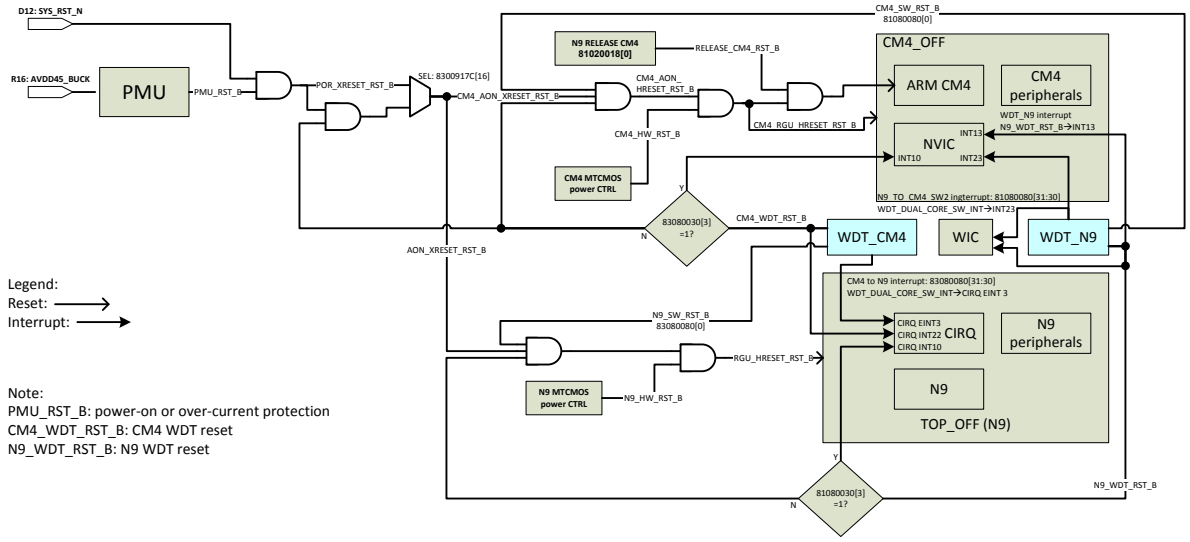


*Figure 2-9. WDT Structure*

### 2.4.10.3 Reset Scenarios

The definitions of the cold reset and the warm reset are shown below:

- Cold Reset: Power on reset and both RAM or peripheral devices will be initialized by firmware.
- Warm Reset: CPU is reset but RAM content is still retained (without firmware re-download). It's triggered by
  - Software reset: Software set WDT reset control register to reset CPU.
  - WDT reset: WDT expiration cause CPU to reset if enabled, otherwise interrupt.
  - Core reset: Reset by the other CPU (e.g. N9 to reset CM4 or CM4 to reset N9).
  - Wake-up from deep sleep mode: Reset by the MTCMOS power control.

### 2.4.10.4 Sleep/Wakeup sequence

The sleep/wakeup control sequence is shown in the diagram below.

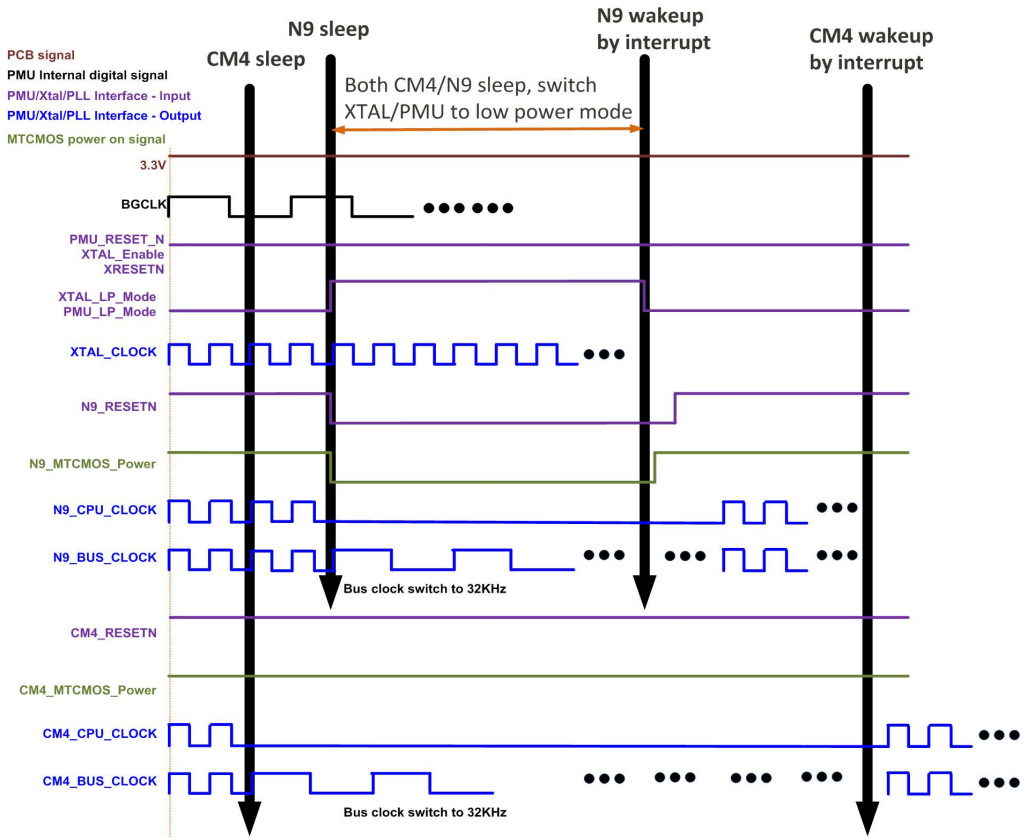



*Figure 2-10. Sleep/Wakeup Sequence*

### 2.4.11 Memory Map

The table below describes how the peripherals are mapped to the CM4 memory.

When the MCU performs a read transaction to an undefined address, the bus returns 0. When the MCU performs a write transaction to an undefined address, the bus regards it as an invalid transaction and does nothing. The memory space of 0x5040_0000 to 0x5FFF_FFFF is an undefined region and shall not be accessed.

The power domain is identified in the table. The hardware clock gating is associated with the power control. When the CPU power domain is in power-off mode, it implies that the clock is also gated.

The software clock gating control, identified in the table below, provides the way to disable the function and lower its power consumption when the function is not used.

*Table 2-15. CM4 Memory Map*

| Start address | End address | Function | Power Domain | Software Clock gating control | Description |
|---|---|---|---|---|---|
| 0x0000_0000 | 0x0000_FFFF | TCM ROM | CM4_OFF | | Tightly Coupled ROM for CM4 |
| 0x0010_0000 | 0x0010_FFFF | TCM RAM0 | CM4_OFF | | Tightly Coupled RAM for CM4 (64KB) |
| 0x0011_0000 | 0x0011_1FFF | TCM RAM1 | CM4_OFF | | Tightly Coupled RAM for CM4 (8KB) |
| 0x0011_2000 | 0x0011_3FFF | TCM RAM2 | CM4_OFF | | Tightly Coupled RAM for CM4 (8KB) |
| 0x0011_4000 | 0x0011_5FFF | TCM RAM3 | CM4_OFF | | Tightly Coupled RAM for CM4 (8KB) |
| 0x0011_6000 | 0x0011_7FFF | TCM RAM4 | CM4_OFF | | Tightly Coupled RAM for CM4 (8KB) |
| 0x1000_0000 | 0x1FFF_FFFF | Serial Flash CM4 | CM4_OFF | | Serial flash of CM4 |
| 0x2000_0000 | 0x2003_FFFF | SYSRAM_CM4 | CM4_OFF | | System RAM for CM4, 256Kbytes |
| 0x2100_0000 | 0x2100_FFFF | SPI-S | CM4_OFF | 0x8300_0200[21] | SPI slave |
| 0x2200_0000 | 0x2200_FFFF | I2S/Audio | CM4_OFF | 0x8300_0200[14] | I2S |
| 0x2400_0000 | 0x2400_FFFF | SPI-M | CM4_OFF | 0x8300_0200[22] | SPI master |
| 0x2500_0000 | 0x2500_CFFF | SYSRAM_N9 | TOP_OFF(N9) | | System RAM for N9, 52Kbytes |
| 0x3000_0000 | 0x3FFF_FFFF | Serial Flash CM4 | CM4_OFF | | Serial flash of CM4 through system bus |
| 0x5000_0000 | 0x501F_FFFF | HIF_device | TOP_OFF(N9) | | Host interface device controller |
| 0x5020_0000 | 0x502F_FFFF | HIF_host_CM4 | TOP_AON | | Host interface host controller of Wi-Fi radio |
| 0x5040_0000 | 0x5FFF_FFFF | (Undefined) | | | |
| 0x6000_0000 | 0x6FFF_FFFF | WIFISYS | TOP_OFF(N9) | 0x8000_0100[5] | Wi-Fi subsystem |
| 0x7000_0000 | 0x70FF_FFFF | PDA DMA port | | | Patch Decryption Accelerator DMA slave |
| 0x7800_0000 | 0x7800_FFFF | VFF access port | TOP_OFF(N9) | | Virtual FIFO access ports of N9 DMA |

| Start address | End address | Function | Power Domain | Software Clock gating control | Description |
|---|---|---|---|---|---|
| 0x7900_0000 | 0x7900_FFFF | VFF_CM4 access port | CM4_OFF | 0x8300_0200[3] | Virtual FIFO access ports of CM4 DMA |
| 0x8000_0000 | 0x800C_FFFF | APB0 | TOP_OFF(N9) | | APB bridge 0 (synchronous to N9) |
| 0x8000_0000 | 0x8000_FFFF | CONFG | TOP_OFF(N9) | | N9 subsystem configuration |
| 0x8001_0000 | 0x8001_FFFF | DMA | TOP_OFF(N9) | | Generic DMA engine for N9 |
| 0x8002_0000 | 0x8002_FFFF | TOP_CFG_OFF | TOP_OFF(N9) | | TOP_OFF(N9) power domain chip level configuration (GPIO, PINMUX, RF, CLK control) |
| 0x8003_0000 | 0x8003_FFFF | UART | TOP_OFF(N9) | 0x8000_0100[6] | UART host interface for N9 |
| 0x8005_0000 | 0x8005_FFFF | UART_PTA | TOP_OFF(N9) | 0x8000_0100[11] | Inter-chip communication for PTA |
| 0x8008_0000 | 0x8008_FFFF | AHB_MON | TOP_OFF(N9) | 0x8000_0100[10] | AHB bus monitor |
| 0x800A_0000 | 0x800A_FFFF | UART_DSN | TOP_OFF(N9) | 0x8000_0100[7] | UART for N9 debug |
| 0x800B_0000 | 0x800B_FFFF | SEC | TOP_OFF(N9) | | Secure boot configuration |
| 0x800C_0000 | 0x800C_FFFF | HIF | TOP_OFF(N9) | | Host interface configuration |
| 0x8100_0000 | 0x810C_FFFF | APB1 | TOP_OFF(N9) | | APB bridge 1 (synchronous to N9) |
| 0x8102_0000 | 0x8102_FFFF | TOP_CFG_AON | TOP_AON | | TOP_AON power domain chip level configuration (RGU, PINMUX, PLL, PMU, XTAL, CLK control) |
| 0x8103_0000 | 0x8103_FFFF | DBG_CIRQ | TOP_AON | | Debug interrupt controller for N9 |
| 0x8104_0000 | 0x8104_FFFF | CIRQ | TOP_AON | | Interrupt controller for N9 |
| 0x8105_8000 | 0x8105_FFFF | GPT | TOP_AON | | General Purpose Timer for N9 |

| Start address | End address | Function | Power Domain | Software Clock gating control | Description |
|---|---|---|---|---|---|
| 0x8106_0000 | 0x8106_FFFF | PTA | TOP_OFF(N9) | 0x8000_0100[14] | Packet Traffic Arbitrator for Wi-Fi |
| 0x8107_0000 | 0x8107_FFFF | EFUSE_MAC | TOP_OFF(N9) | 0x8000_0100[12] | Efuse controller |
| 0x8108_0000 | 0x8108_FFFF | WDT | TOP_AON | | Watchdog Timer for N9 |
| 0x8109_0000 | 0x8109_FFFF | PDA | TOP_OFF(N9) | | Patch Decryption Accelerator |
| 0x810A_0000 | 0x810A_FFFF | RDD | TOP_OFF(N9) | 0x8000_0100[23] | Wi-Fi debug |
| 0x810C_0000 | 0x810C_FFFF | RBIST | TOP_OFF(N9) | | RF BIST configuration |
| 0x8300_0000 | 0x810C_FFFF | APB2 | CM4_OFF | | APB bridge 1 (synchronous to CM4) |
| 0x8300_0000 | 0x8300_7FFF | CONFG_CM4 | CM4_OFF | | System configuration for CM4 |
| 0x8300_8000 | 0x8300_BFFF | TOP_CFG_AON_CM4 | TOP_AON | | TOP_AON configuration |
| 0x8300_C000 | 0x8300_EFFF | CONFG_CM4_AON | TOP_AON | | System configuration for CM4 in TOP_AON domain |
| 0x8300_F000 | 0x8300_FFFF | SEC_TOP_CM4 | CM4_OFF | 0x8300_0200[0] | JTAG security for CM4 |
| 0x8301_0000 | 0x8301_FFFF | DMA_CM4 | CM4_OFF | 0x8300_0200[3] | Generic DMA engine for CM4 |
| 0x8302_0000 | 0x8302_FFFF | UART_DSN | CM4_OFF | 0x8300_0200[4] | UART for CM4 debug |
| 0x8303_0000 | 0x8303_FFFF | UART1 | CM4_OFF | 0x8300_0200[5] | UART 1 for CM4 |
| 0x8304_0000 | 0x8304_FFFF | UART2 | CM4_OFF | 0x8300_0200[6] | UART 2 for CM4 |
| 0x8305_0000 | 0x8305_FFFF | GPT_CM4 | TOP_AON | | General Purpose Timer for CM4 |
| 0x8306_0000 | 0x8306_FFFF | IrDA | CM4_OFF | 0x8300_0200[8]<br>0x8300_0200[9] | IrDA |
| 0x8307_0000 | 0x8307_FFFF | Serial flash | CM4_OFF | 0x8300_0200[10] | Serial flash macro access |
| 0x8308_0000 | 0x8308_FFFF | WDT_CM4 | TOP_AON | | Watchdog Timer for CM4 |

| Start address | End address | Function | Power Domain | Software Clock gating control | Description |
|---|---|---|---|---|---|
| 0x8309_0000 | 0x8309_FFFF | I2C_1 | CM4_OFF | 0x8300_0200[12]<br>0x8300_0200[23] | I2C 1 |
| 0x830A_0000 | 0x830A_FFFF | I2C_2 | CM4_OFF | 0x8300_0200[13]<br>0x8300_0200[24] | I2C 2 |
| 0x830B_0000 | 0x830B_0FFF | I2S | CM4_OFF | 0x8300_0200[14] | I2S configuration |
| 0x830C_0000 | 0x830C_FFFF | RTC | RTC | | Real time clock |
| 0x830D_0000 | 0x830D_FFFF | AUXADC | CM4_OFF | 0x8300_0200[16] | Auxiliary ADC configuration |
| 0x830F_0000 | 0x830F_FFFF | Crypto | CM4_OFF | 0x8300_0200[18] | Crypto engine |
| 0xA000_0000 | 0xAFFF_FFFF | PSE | CM4_OFF | | Packet switch engine memory |
| 0xE000_E000 | 0xE000_EFFF | NVIC, SYSTICK, FPU | CM4_OFF | | Nested vectored interrupt controller<br>System Control Space (SYSTICK)<br>Floating-point unit |

### 2.4.12 SYSRAM_CM4

SYSRAM, the internal SRAM, is mapped on the system bus interface of Cortex-M4. M4 can carry out instruction fetches and data accesses to the SYSRAM.

SYSRAM is the internal SRAM that the DMA engine can access. It can be used as a GDMA or VFIFO buffer, the source and the destination of GDMA controller, for memory-to-memory transfer as well the transfer between memory and peripherals.

### 2.4.13 Crypto engine

The crypto engine supports

- AES, DES, and 3DES encryption and decryption engine.
- SHA256, SHA512 and MD5 hash engines.

## 2.5 Peripherals

Several peripheral are multiplexed GPIOs. MT7687F has two dedicated UART interfaces with flow control, one dedicated I2C interface, and one dedicated IrDA interface.

MT7687F also has the 2nd I2C interface, the SPI slave interface, the I2S interface, and the SPI master interface, but only 2 of the above interfaces can be effective at a time.

The section describes the function of all the peripherals.

### 2.5.1 GPIO Interface

#### 2.5.1.1 GPIO Function

There are two types of GPIO (General purpose IO) designs in MT7687F: GPIO and AGPIO.

Floating-well design is used in GPIO and AGPIO. It prevents potential leakage problem when the DVDD33 power supply is not enabled but the pin input is pulled up to 3.3V source.

MT7687F offers GPIO, each with the following configuration options:

- Input / Output mode
- Slew rate control
- Schmitt trigger hysteresis control
- Input mode: Floating (Hi-Z), pull-up, or pull-down
- Output mode: Active driving
- Pull up/down control. The pull-up and pull-down resistance is 75KΩ with ±20% variation over PVT condition
- Driving strength: 4mA, 8mA, 12mA, 16mA
- Input and output duty cycle tuning

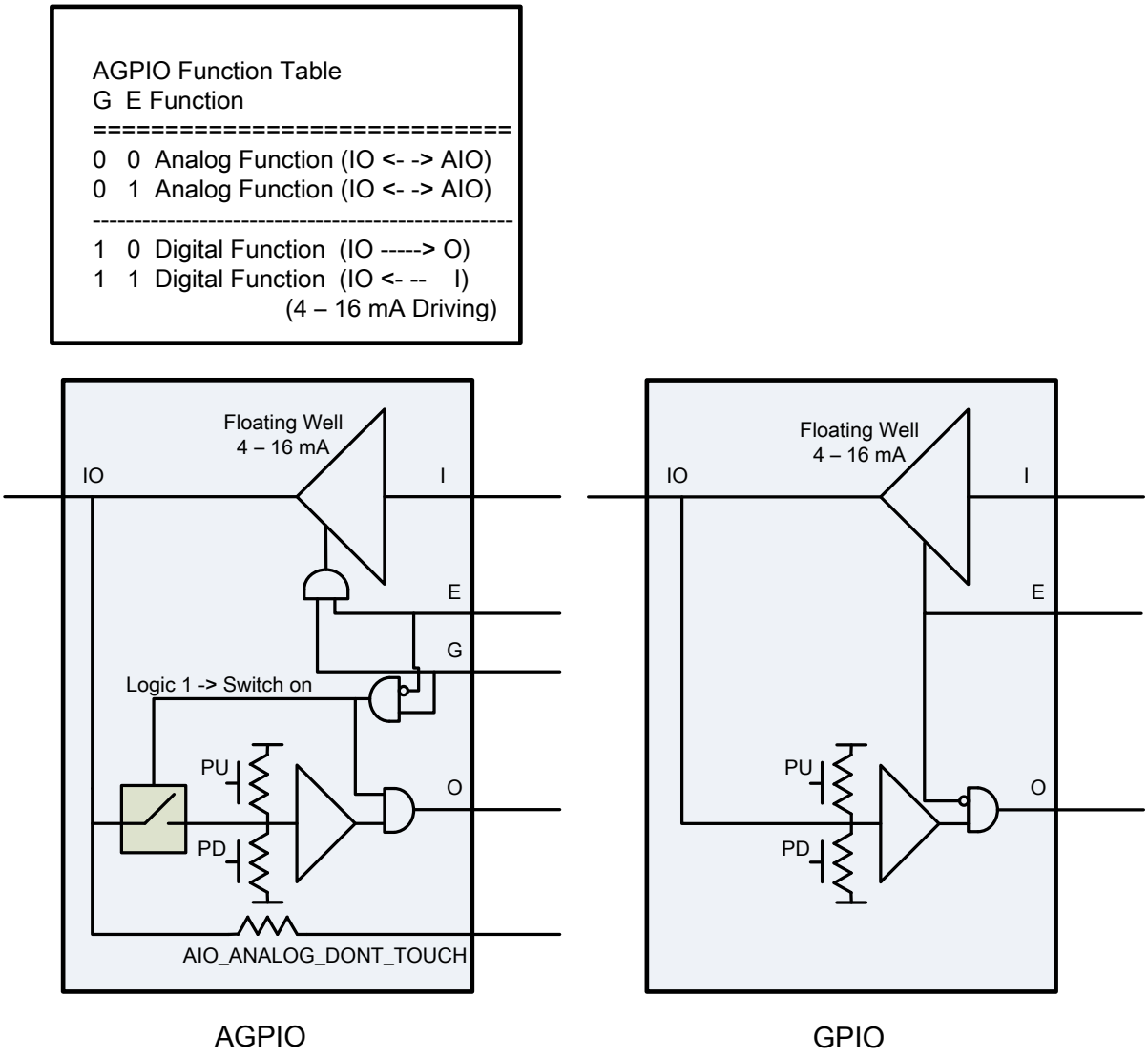



***Figure 2-11. AGPIO/GPIO Block Diagram (Left: AGPIO; Right: GPIO)***

The digital IO AGPIO function is equivalent to GPIO as shown above. A dedicated internal control signal is used to select between the digital and analog functions. The IOs are multiplexed with 16 channels ADC.

**Output Signal Multiplexing**

Function-[9:1]-AON and Function-[9:0] can all be output to PINX by setting pinx_pinmux_aon_sel and pinx_pinmux_off_sel, as shown in Figure 2-12 below. Function-[9:1]-AON signals are part of TOP_AON domain and Function-[9:0] signals are part of TOP_OFF (N9) domain. The output of the pad is enabled through E and G pad controls which require 2'b11 for digital output mode.

For a specific pin there could be only a limited number of functions available, these functions are mapped anywhere to the different inputs of the muxes (not always in an incremental scheme).

TOP_AON domain means the circuit is always powered on when PMU supplies the power. TOP_OFF (N9) domain means the N9 related circuit is powered off in some scenarios when PMU supplies the power.

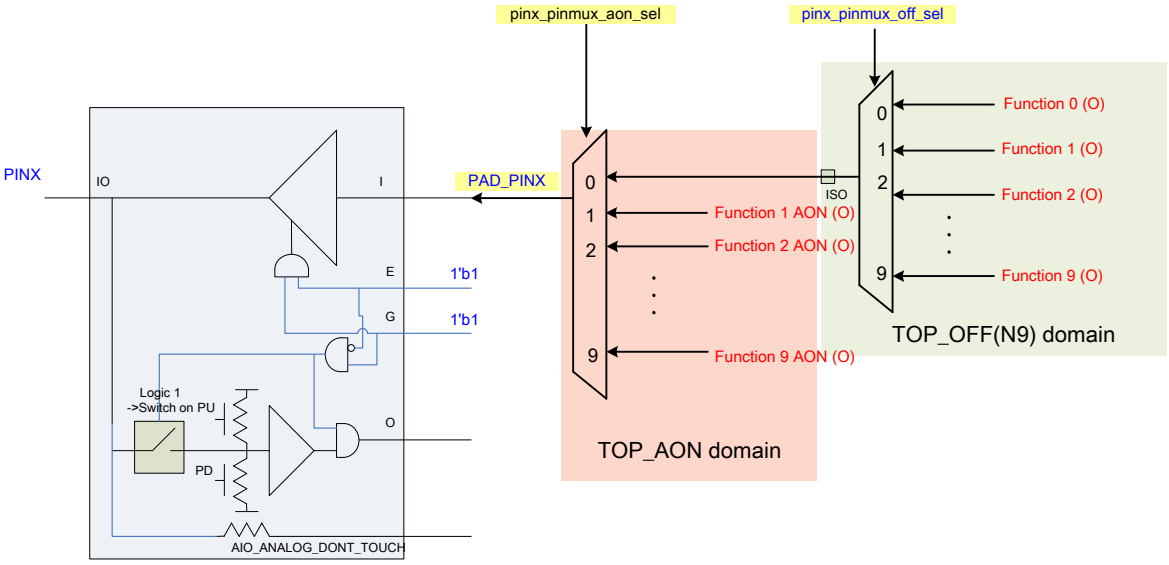



***Figure 2-12. AGPIO Configured as Output Multiplexing***

### Input Signal Multiplexing

Figure 2-13 below shows that PINX is the source of Function-AON-0, while PINX and PINY can both be the input source for Function-1. The (E, G) setting for both IO is 2'b01 for digital input mode.

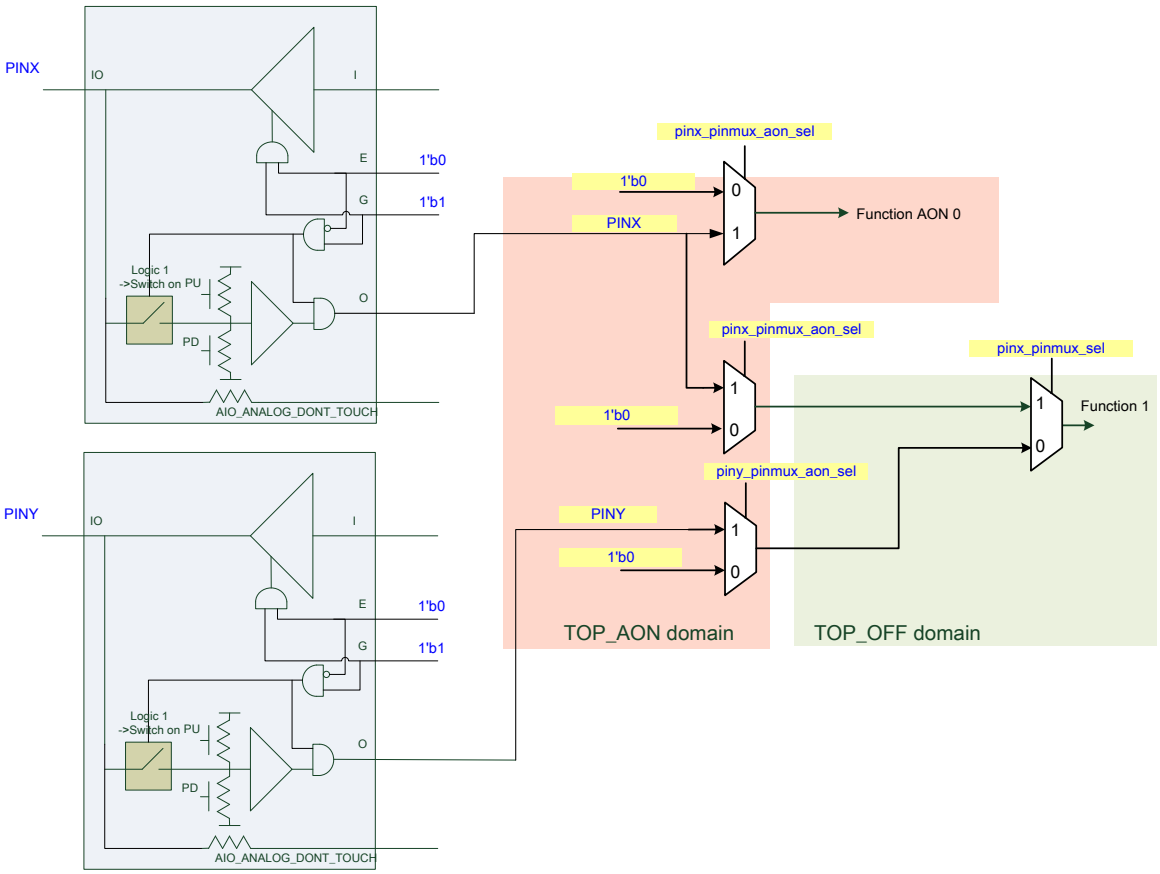



***Figure 2-13. AGPIO Configured as Input Multiplexing***

### Input / Output / Analog Signal Multiplexing

This figure below shows how function-0, function-1 and Analog-function share the same IO (PINX) by configuring (E, G) pair internally. G is controlled in off domain.

***Table 2-16. Functional Description of AGPIO***

| (G,E) value | 2'b11 | 2'b10 | 2'b0x |
|---|---|---|---|
| Function | PINX=Function-0<br>(output mode) | Function-1=PINX<br>(input mode) | Analog-function=PINX<br>(analog mode) |

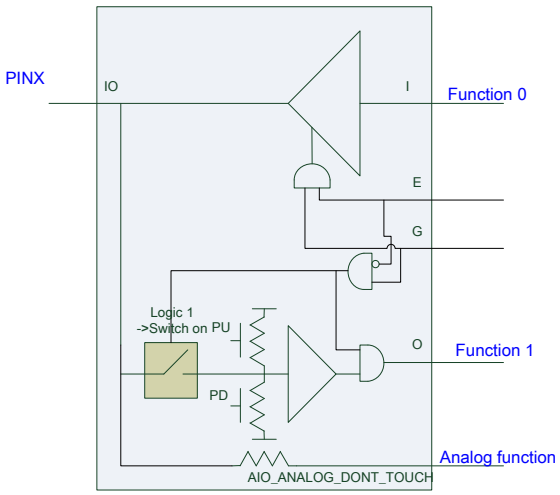



***Figure 2-14. AGPIO Configured as Input, Output, or Analog Mode***

### 2.5.2 UART Interface

MT7687F has two UART interfaces. The UART has M16C450 and M16550A modes of operation, which are compatible with a range of standard software drivers.MT7687F supports UART with configurable BAUD rates from 9.6Kbps, 19.2Kbps, 38.4Kbps, 115.2Kbps, and 921.6Kbps.

### 2.5.3 I2C Serial Interface

MT7687F features two I2C serial interface master controllers. The two signals of I2C channel 0 are I2C0_CLK and I2C0_DATA.

- I2C0_CLK is a clock signal that is driven by the master.
- I2C0_DATA is a bi-directional data signal that can be driven by either the master or the slave. It supports the clock rate of 50, 100, 200, and 400 KHz.
- I2C channel 1 supports the same feature as channel 0.

### 2.5.4 Auxiliary ADC function

MT7687F features one auxiliary ADC function. The ADC function contains a 4-channel analog switch, a single-end input asynchronous 12-bit SAR (Successive Approximation Register) ADC, and a digital averaging function. The digital averaging function can perform on-the-fly averaging function of 1/2/4/8/16/32/64 points. The ADC features the dithering function to enhance the DNL performance. The ADC uses an external VREF20 as a reference voltage.

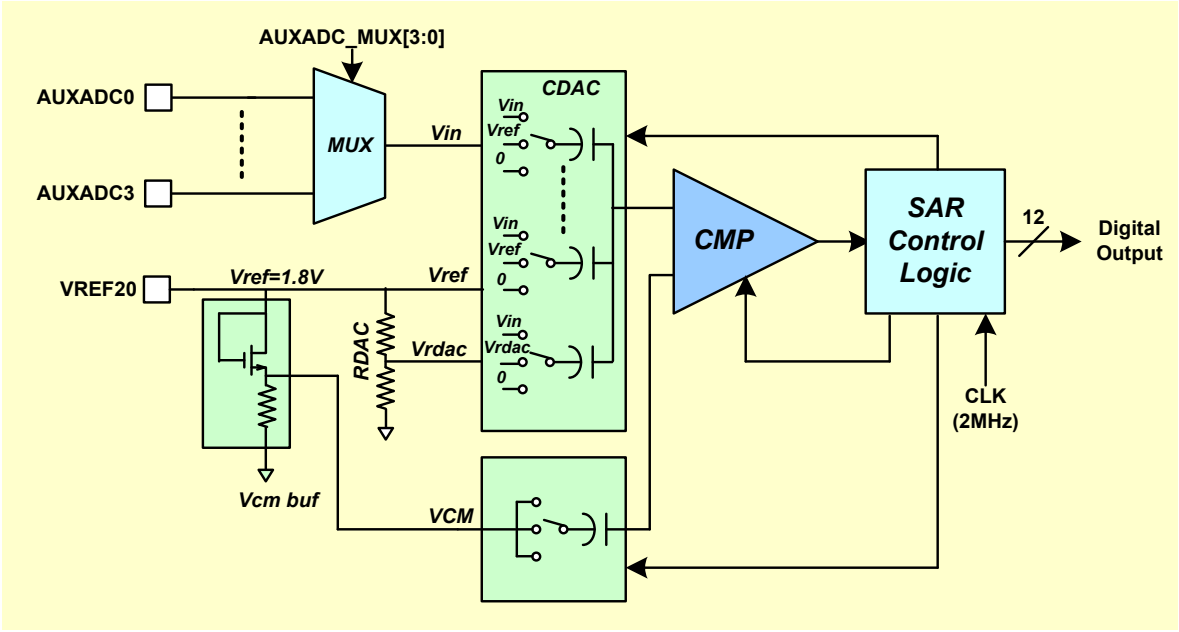



*Figure 2-15. Auxiliary ADC Block Diagram (Analog Part)*

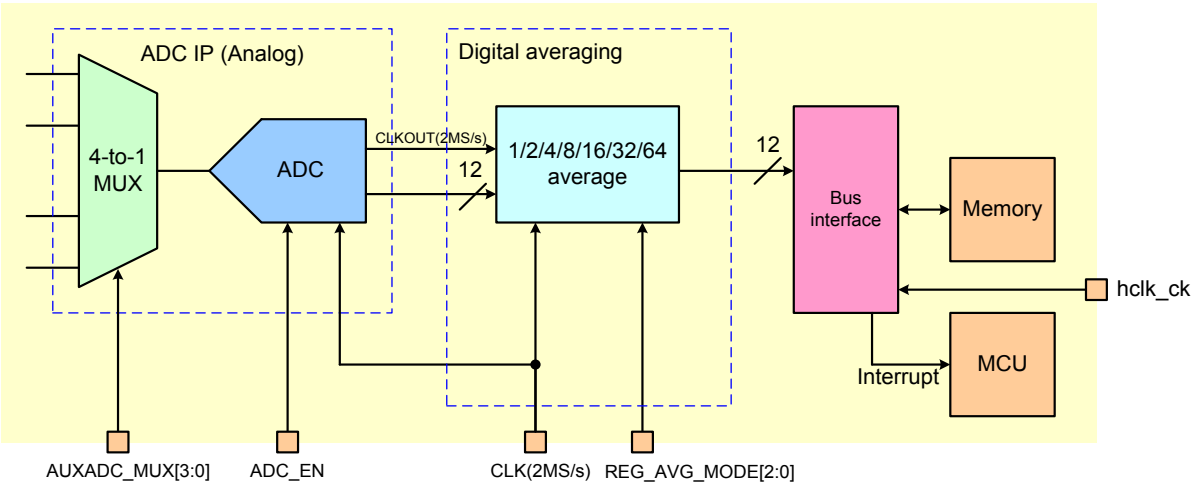



*Figure 2-16. Auxiliary ADC Block Diagram*

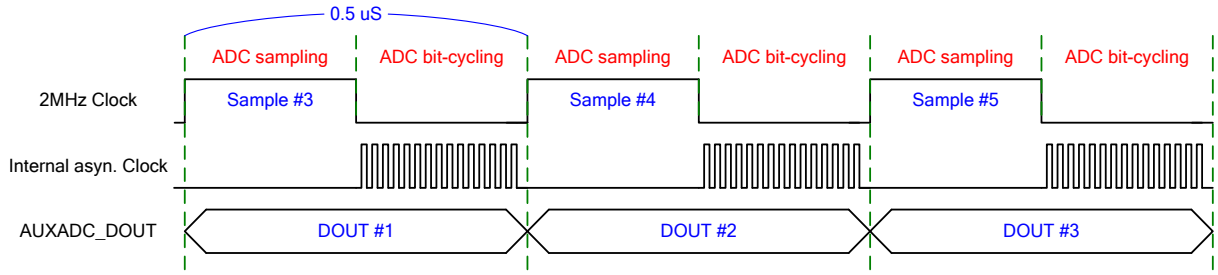



***Figure 2-17. Auxiliary ADC Clock Timing Diagram***

**Auxiliary ADC Features:**

- Input channel number: 4 channels
- Sampling and output data rate: 2MS/s
- DNL without dithering and averaging: <±2LSB
- DNL with dithering and averaging: <±1LSB
- Dithering function: 16 levels with step size of 4LSB.

### 2.5.5 SPI Master Interface

MT7687F features one SPI master controller. It is used as an extension interface to control the peripheral device on expansion port. The SPI master controller supports the clock rates of 0.25, 0.5, 1, 2, 4, 6, 8, 10, and 12MHz. It supports two options of clock polarity (CPOL) and two options of initial clock phase (CPHA). SPI pins are multiplexed with I2S pins.

***Table 2-17. SPI Pin Description***

| Signal Name | Signal Description | Direction |
|---|---|---|
| CS | Chip select | Output |
| SCK | Serial clock | Output |
| MISO | Master in, Slave out | Input |
| MOSI | Master out, Slave in | Output |

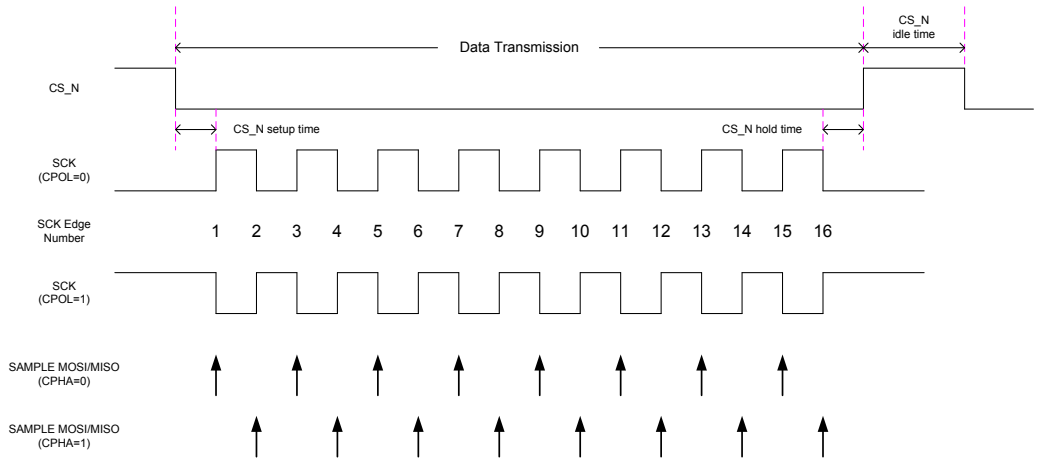



***Figure 2-18. SPI Timing Diagram***

### 2.5.6 SPI Slave Interface

The simple SPI slave module translates 16bits SPI serial protocol to create AHB master transaction for accessing SYSRAM or configuration registers.

The block diagram shows SPI slave controller, spis_top, was integrated in the CM4 system. SPI Host can write data into CM4 SYSRAM by controlling slave controller.

SPI slave controller supports interrupt to CM4 system. SPI host can configure register in slave controller to interrupt CM4 MCU. When CM4 MCU gets the interrupt, it can read status from SPI slave controller and clear the interrupt. Also, it can read data from SYSRAM.

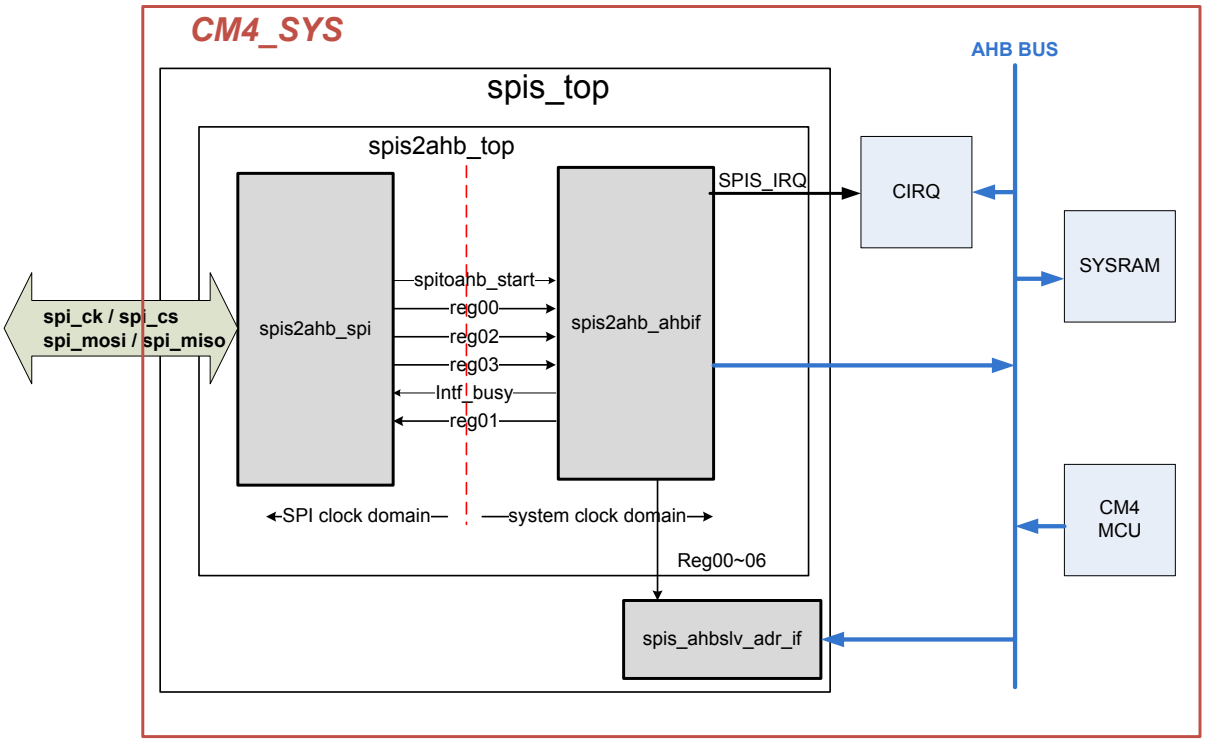



***Figure 2-19. SPI Slave Block Diagram***

SPI slave uses SPI2AHB protocol. In AHB write transaction, it should write AHB 32bits data and 32bits address into spi controller register first, and then kick the AHB_cmd to start AHB write transaction. After start AHB_cmd, 32bits data will be written into specified 32bits address. In AHB read transaction, it should write 32bits address into spi controller register first, and then kick the AHB_cmd to start AHB read transaction. After start AHB_cmd, 32 bits data will be read from specified 32bits address and stored in spi slave controller.

### 2.5.7 I2S Interface

MT7687F features one I2S interface, which is used to connect to an external audio codec. The I2S interface can support the I2S slave mode only. The five I2S signals are shown below. The I2S_MLK clock frequency is 16MHz.

*Table 2-18. I2S Pin Description*

| Signal Name | Signal Description | Direction (Slave Mode) |
|---|---|---|
| I2S_MCLK | The base clock of the function. | Output |
| I2S_BCLK | The bit clock of the interface | Input |
| I2S_FS (LRCLK) | The left/right word select line of the interface | Input |
| I2S_TX | Digital audio output | Output |
| I2S_RX | Digital audio input | Input |

MT7687F supplies the MCLK of 16MHz. The external CODEC generates BCLK and LRCLK from MCLK. When configured as the I2S slave mode, the I2S interface can support two modes.

*Table 2-19. I2S Slave Mode*

| Slave Mode | Bit Width | Input Sample (Uplink) | Output Sample (Downlink) | BCLK (Input) | FS (Input) |
|---|---|---|---|---|---|
| Mode 1 | 16b | 16KHz, mono/stereo | 16KHz, mono/stereo | 512KHz | 16KHz |
| Mode 2 | 16b | 24KHz, mono/stereo | 24KHz, mono/stereo | 768KHz | 24KHz |
| Mode 3 | 16b | 44.1KHz, mono/stereo | 44.1KHz, mono/stereo | 1.4112MHz | 44.1KHz |
| Mode 4 | 16b | 48KHz, mono/stereo | 48KHz, mono/stereo | 1.536MHz | 48KHz |

*Table 2-20. I2S Data Format*

| | Byte 3 | Byte 2 | Byte 1 | Byte 0 |
|---|---|---|---|---|
| Stereo(2 CH) | R[15:8] | R[7:0] | L[15:8] | L[7:0] |
| Mono(1 CH) | 8'b0 | 8'b0 | L[15:8] | L[7:0] |

The mono data is transferred across the I2S bus as left channel information.

In all of the modes above, when the input data is mono, the data of interest is transferred across the I2S bus on the left channel.

The I2S pins are multiplexed with SPI pins.

The signal waveform of I2S is shown below.

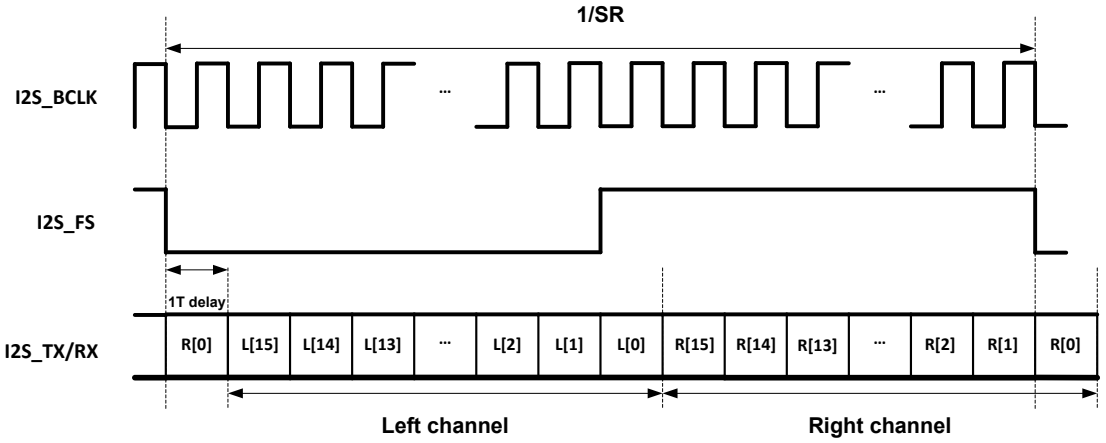
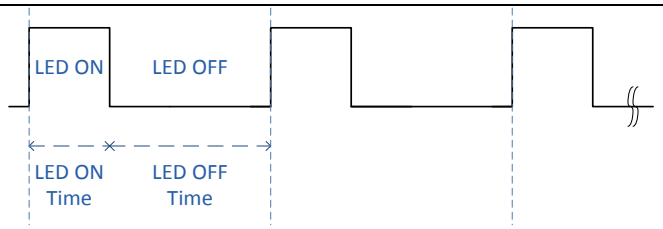
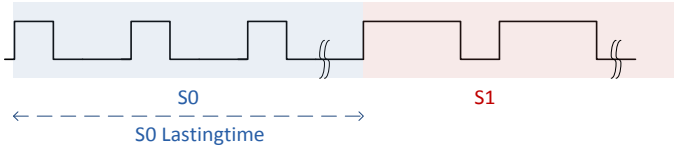
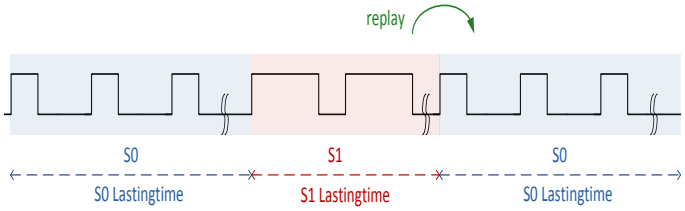



*Figure 2-20. I2S Signal Waveform*

### 2.5.8 Pulse Width Modulation (PWM)

MT7687F features 28 generic PWMs to generate pulse sequences with programmable frequency and duration for LCD, vibrators, and other devices. The PMU features three configurable pattern options.

*Table 2-21. PWM Modes*

| Mode | Description | Waveform |
|---|---|---|
| 1 | Basic PWM:<br>LED ON time (duration) and LED OFF time (duration) are configurable. |  |
| 2 | Two-State PWM:<br>There are two configurable states (S0 and S1) for PWM LED. |  |
| 3 | Two-State replay mode:<br>User can set replay mode with specified S1_Lasting_Time. PWM LED would act as [S0→S1→S0→S1→S0…] with |  |

| Mode | Description | Waveform |
|---|---|---|
| | period time of (S0_Lasting_Time + S1_Lasting_Time) | |

### 2.5.9 IrDA

IrDA TX module supports consumer IR protocols including NEC, RC-5, RC-6, and the software-based pulse-width mode. IrDA RX module supports protocols including RC-5 and pulse-width detection mode.

## 2.6 Radio MCU Subsystem

### 2.6.1 CPU

MT7687F features 32-bit CPU N9, with the following features:

- 5-stage pipeline with extensive clock-gating
- Dynamic branch prediction with BTB
- 16/32-bit mixed instruction format
- Multiply-accumulate and multiply-subtract instructions
- Instructions optimized for audio applications
- Instruction and data local memory
- JTAG based debug interface
- Programmable data endian control

### 2.6.2 RAM/ROM

The Radio MCU subsystem features ILM (Instruction Local Memory), DLM (Data Local Memory), and the SYSRAM. The ROM code is in ILM.

### 2.6.3 Memory map

The table below describes how the peripherals are mapped to the memory space in Radio MCU subsystem.

When the MCU performs a read transaction to an undefined address, the bus returns 0. When the MCU performs a write transaction to an undefined address, the bus regards it as an invalid transaction and does nothing.

***Table 2-22. N9 Memory Map***

| Start address | End address | Function | Description |
|---|---|---|---|
| 0x0000_0000 | 0x000C_FFFF | ILM ROM | Instruction local memory ROM for N9 |

| Start address | End address | Function | Description |
|---|---|---|---|
| 0x000D_0000 | 0x0011_FFFF | ILM RAM | Instruction local memory RAM for N9 |
| 0x0200_0000 | 0x0200_021C | Patch & CR | N9 ROM patch engine |
| 0x0209_0000 | 0x020C_1FFF | DLM RAM | Data local memory for N9 |
| 0x0040_0000 | 0x0040_CFFF | SYSRAM N9 | System RAM for N9 |
| 0x2000_0000 | 0x2003_FFFF | SYSRAM CM4 | System RAM for CM4 (256KB) |
| 0x2100_0000 | 0x2100_FFFF | SPI-S | SPI slave |
| 0x2200_0000 | 0x2200_FFFF | I2S/Audio | I2S |
| 0x2400_0000 | 0x2400_FFFF | (Reserved) | |
| 0x3000_0000 | 0x3FFF_FFFF | Serial Flash CM4 | Serial flash controller of CM4 |
| 0x5000_0000 | 0x501F_FFFF | HIF_device | Host interface device controller |
| 0x5020_0000 | 0x502F_FFFF | HIF_host_CM4 | Host interface host controller of Wi-Fi radio |
| 0x6000_0000 | 0x6FFF_FFFF | WIFISYS | Wi-Fi subsystem |
| 0x7000_0000 | 0x70FF_FFFF | PDA DMA port | Patch Decryption Accelerator DMA slave |
| 0x7800_0000 | 0x7800_0000 | VFF access port0 | Virtual FIFO access port 0 of N9 DMA |
| 0x7800_0100 | 0x7800_0100 | VFF access port1 | Virtual FIFO access port 1 of N9 DMA |
| 0x7900_0000 | 0x7900_FFFF | VFF_CM4 access port | Virtual FIFO access ports of CM4 DMA |
| 0x8000_0000 | 0x800C_FFFF | APB0 | APB bridge 0 (synchronous to N9) |
| 0x8000_0000 | 0x8000_FFFF | CONFG | N9 subsystem configuration |
| 0x8001_0000 | 0x8001_FFFF | DMA | Generic DMA engine for N9 |
| 0x8002_0000 | 0x8002_FFFF | TOP_CFG_OFF | TOP_OFF(N9) power domain chip level configuration (GPIO, PINMUX, RF, PLL, CLK control) |
| 0x8003_0000 | 0x8003_FFFF | UART | UART host interface for N9 |
| 0x8005_0000 | 0x8005_FFFF | UART_PTA | Inter-chip communication for PTA |
| 0x8008_0000 | 0x8008_FFFF | AHB_MON | AHB bus monitor |
| 0x800A_0000 | 0x800A_FFFF | UART_DSN | UART for N9 debug |
| 0x800B_0000 | 0x800B_FFFF | SEC | Secure boot configuration |
| 0x800C_0000 | 0x800C_FFFF | HIF | Host interface configuration |
| 0x8100_0000 | 0x810C_FFFF | APB1 | APB bridge 1 (synchronous to N9) |
| 0x8102_0000 | 0x8102_FFFF | TOP_CFG_AON | TOP_AON power domain chip level configuration (RGU, PINMUX, PMU, XTAL, CLK control) |

| Start address | End address | Function | Description |
|---|---|---|---|
| 0x8103_0000 | 0x8103_FFFF | DBG_CIRQ | Debug interrupt controller for N9 |
| 0x8104_0000 | 0x8104_FFFF | CIRQ | Interrupt controller for N9 |
| 0x8105_8000 | 0x8105_FFFF | GPT | General Purpose Timer for N9 |
| 0x8106_0000 | 0x8106_FFFF | PTA | Packet Traffic Arbitrator for Wi-Fi coexistence |
| 0x8107_0000 | 0x8107_FFFF | EFUSE | Efuse controller |
| 0x8108_0000 | 0x8108_FFFF | WDT | Watchdog Timer for N9 |
| 0x8109_0000 | 0x8109_FFFF | PDA | Patch Decryption Accelerator |
| 0x810A_0000 | 0x810A_FFFF | RDD | Wi-Fi debug |
| 0x810C_0000 | 0x810C_FFFF | RBIST | RF BIST configuration |
| 0x8300_0000 | 0x810C_FFFF | APB2 | APB bridge 1 (synchronous to CM4) |
| 0x8300_0000 | 0x8300_FFFF | CONFG_CM4 | System configuration for CM4 |
| 0x8301_0000 | 0x8301_FFFF | DMA_CM4 | Generic DMA engine for CM4 |
| 0x8302_0000 | 0x8302_FFFF | UART_DSN | UART for CM4 debug |
| 0x8303_0000 | 0x8303_FFFF | UART1 | UART 1 for CM4 |
| 0x8304_0000 | 0x8304_FFFF | UART2 | UART 2 for CM4 |
| 0x8305_0000 | 0x8305_FFFF | GPT_CM4 | General Purpose Timer for CM4 |
| 0x8306_0000 | 0x8306_FFFF | IrDA | IrDA |
| 0x8307_0000 | 0x8307_FFFF | Serial flash | Serial flash macro access |
| 0x8308_0000 | 0x8308_FFFF | WDT_CM4 | Watchdog Timer for CM4 |
| 0x8309_0000 | 0x8309_FFFF | I2C_1 | I2C 1 |
| 0x830A_0000 | 0x830A_FFFF | I2C_2 | I2C 2 |
| 0x830B_0000 | 0x830B_FFFF | I2S | I2S configuration |
| 0x830D_0000 | 0x830D_FFFF | AUXADC | Auxiliary ADC configuration |
| 0x830F_0000 | 0x830F_FFFF | Crypto | Crypto engine |
| 0xA000_0000 | 0xAFFF_FFFF | PSE | Packet switch engine memory |

### 2.6.4 N9 Bus Fabric

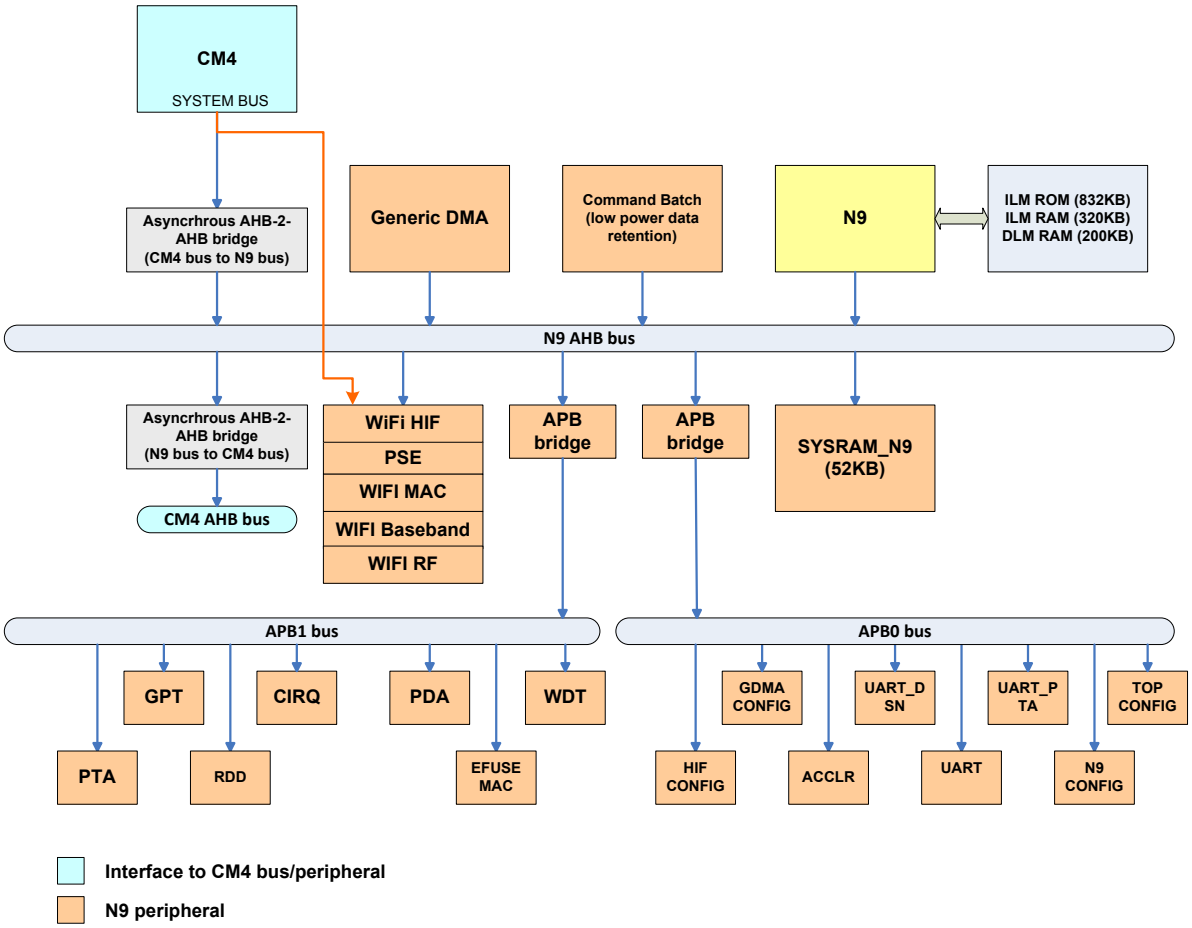



***Figure 2-21. N9 Bus Fabric***

**Functional description**:

- Command batch: Used to save/restore the critical CR and memory data when entering and leaving the low power mode.
- Wi-Fi HIF: The host control and data interface from N9 to Wi-Fi subsystem.
- Wi-Fi PSE: The Packet switch engine used to transfer packet from N9 to Wi-Fi MAC/Radio or from CM4 to Wi-Fi MAC/Radio, and vice versa.
- PDA: Packet Decryption Agent, used to download firmware and decipher the firmware which is encrypted to avoid eavesdrop.
- PTA: Packet Traffic Arbitration, used to do the traffic arbitration of Wi-Fi when the two radios are transmitting and receiving at the same time.
- RDD: The Wi-Fi debug function.
- EFUSE: The Efuse macro used for the configuration of Wi-Fi MAC and Radio.

### 2.6.5 CIRQ

N9 subsystem uses the interrupt controller CIRQ to control the source selection, mask, edge/level sensitivity, and software enabling for internal interrupts, as well as the mask and the edge/level sensitivity for external interrupts.

CIRQ also integrates the de-bounce circuit for external interrupts.

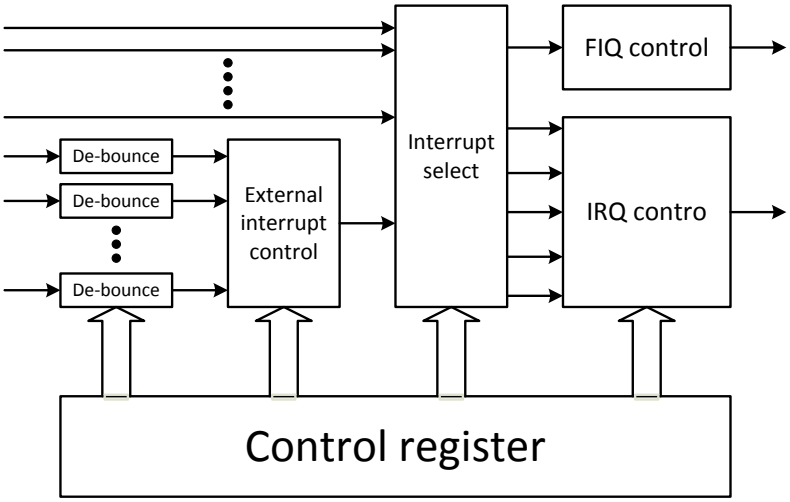



***Figure 2-22. N9 interrupt controller***

#### 2.6.5.1 Interrupt sources

The tables below lists the interrupt sources of internal and external interrupts.

There are totally 23 interrupts and 14 external interrupts.

The power domain/subsystem lists the power domain and the subsystem from which the interrupt is generated.

| IRQ No. | Interrupt source | Power domain /subsystem | External interrupt | Wake-up capability (1) | De-bounce | Description |
|---|---|---|---|---|---|---|
| INT0 | UART | TOP_OFF(N9)/MCUSYS | | | | UART module |
| INT1 | DMA | TOP_OFF(N9)/MCUSYS | | | | Generic DMA in N9 subsystem |
| INT2 | HIFSYS | TOP_AON/HIF | | | | WIFI_HIF(SDIO) |
| INT3 | (Reserved) | | | | | |
| INT4 | THERM | TOP_OFF(N9) | | | | Thermometer |
| INT5 | (Reserved) | | | | | |
| INT6 | WIFI | WF_OFF | | | | Wi-Fi subsystem |
| INT7 | ICAP | TOP_OFF(N9)/MCUSYS | | | | Internal capture in RBIST module |

| IRQ No. | Interrupt source | Power domain /subsystem | External interrupt | Wake-up capability (1) | De-bounce | Description |
|---|---|---|---|---|---|---|
| INT8 | EINT | TOP_AON/MCUSYS | | | | External interrupt |
| INT9 | (Reserved) | | | | | |
| INT10 | WDT_N9 | TOP_AON/MCUSYS | | | | Watch dog timer in N9 subsystem |
| INT11 | AHB_MONITOR | TOP_OFF(N9)/MCUSYS | | | | AHB monitor |
| INT12 | (Reserved) | | | | | |
| INT13 | PLC_ACCLR | TOP_OFF(N9)/MCUSYS | | | | Packet Loss Concealment accelerator |
| INT14 | (Reserved) | | | | | |
| INT15 | PSE | WF_OFF/PSE | | | | Packet switch engine |
| INT16 | (Reserved) | | | | | |
| INT17 | HIFSYS | TOP_OFF(N9)/HIFSYS | | | | HIF subsystem |
| INT18 | UART_PTA * | TOP_OFF(N9)/MCUSYS | | | | UART_PTA module |
| INT19 | PTA * | TOP_OFF(N9)/MCUSYS | | | | PTA module |
| INT20 | CMBT | TOP_OFF(N9) | | | | Command batch module |
| INT21 | GPT3 | TOP_AON/MCUSYS | | | | General purpose timer module |
| INT22 | WDT_CM4 | TOP_AON/MCUSYS_CM4 | | | | CM4 WDT interrupt N9 |
| EINT0 | UART_RX | TOP_AON | V | V | Available | Wake up from UART |
| EINT1 | (Reserved) | | V | V | Available | |
| EINT2 | HIFSYS | TOP_AON/HIF | V | V | Available | WIFI_HIF (SDIO) |
| EINT3 | CM4_TO_N9_SW | TOP_AON/MCUSYS_CM4 | V | V | Available | CM4 SW interrupt N9<br>83080080[31:30] SW_INT |
| EINT4 | (Reserved) | | V | V | Available | |
| EINT5 | PCIE * | TOP_OFF(N9)/HIFSYS | V | V | Available | Wake up from PCIe |
| EINT6 | GPT | TOP_AON/MCUSYS | V | V | Available | General purpose timer module (GPT0 timer and GPT1 timer) |
| EINT7 | External interrupt | TOP_AON | V | V | Available | External interrupt<br>Pin: GPIO58 |
| EINT8 | External interrupt | TOP_AON | V | V | Available | External interrupt<br>Pin: GPIO57 |
| EINT9 | External interrupt | TOP_AON | V | V | Available | External interrupt<br>Pin: GPIO30 |
| EINT10 | (Reserved) | | V | V | Available | |
| EINT11 | External interrupt | TOP_AON | V | V | Available | External interrupt<br>Pin: GPIO38 |
| EINT12 | External interrupt | TOP_AON | V | V | Available | External interrupt<br>Pin: GPIO39 |
| EINT13 | (Reserved) | | V | V | Available | |

*: Not used for MT7687F

Note 1; Capable to wake up N9 when N9 is in sleep mode.

## 2.7 Wi-Fi Subsystem

### 2.7.1 Wi-Fi MAC

MT7687F MAC supports the following features:

- Supports all data rates of 802.11g including 6, 9, 12, 18, 24, 36, 48, and 54Mbps
- Supports short GI and all data rates of 802.11n including MCS0 to MCS7
- 802.11 to 802.3 header translation offload
- RX TCP/UDP/IP checksum offload
- Supports multiple concurrent clients as an access point
- Supports multiple concurrent clients as a repeater
- Aggregate MPDU RX (de-aggregation) and TX (aggregation) support
- Transmits beamforming as a beamformee
- Transmits rate adaptation
- Transmits power control
- Security
- 64-bit WEP (WEP-40) and 128-bit WEP (WEP-104) encryption with hardware TKIP and CKIP processing
- AES-CCMP hardware processing
- SMS4-WPI (WAPI) hardware processing

### 2.7.2 WLAN Baseband

MT7687F baseband supports the following features:

- 20 and 40MHz channels
- MCS0-7 (BPSK, r=1/2 through 64QAM, r=5/6)
- Short Guard Interval
- STBC support
- Low Density Parity check (LDPC) coding
- Support digital pre-distortion to enhance PA performance
- Smoothing (channel estimation) extension to MIMO case

### 2.7.3 WLAN RF

MT7687F RF supports the following features:

- Integrated 2.4GHzPA and LNA, and T/R switch
- Support frequency band
- 2400-2497MHz
- Support RX antenna diversity for both 2.4GHz band to eliminate the requirement of an external SPDT

## 2.8 RTC

MT7687F features one RTC (Real Time Clock) module. The clock source is the 32.768 KHz Crystal or an external clock source. RTC has built in an accurate timer to wake up the system when it expires.

RTC uses a different power rail from PMU. In the hibernate mode, the PMU is turned off while the RTC module is remained powered on. The RTC module only consumes 3uA in hibernate mode.

RTC has a dedicated PMU control pin PMU_EN_RTC (pin 23) used to turn on the power to the chip when the RTC timer expires and turn off the power to the chip when it intends to enter the hibernate mode.

# 3 Radio Characteristics

## 3.1 Wi-Fi Radio Characteristics

### 3.1.1 Wi-Fi RF Block Diagram

Front-end loss with external Balun (2.4GHz band): 2.4GHz band insertion loss is 2dB.

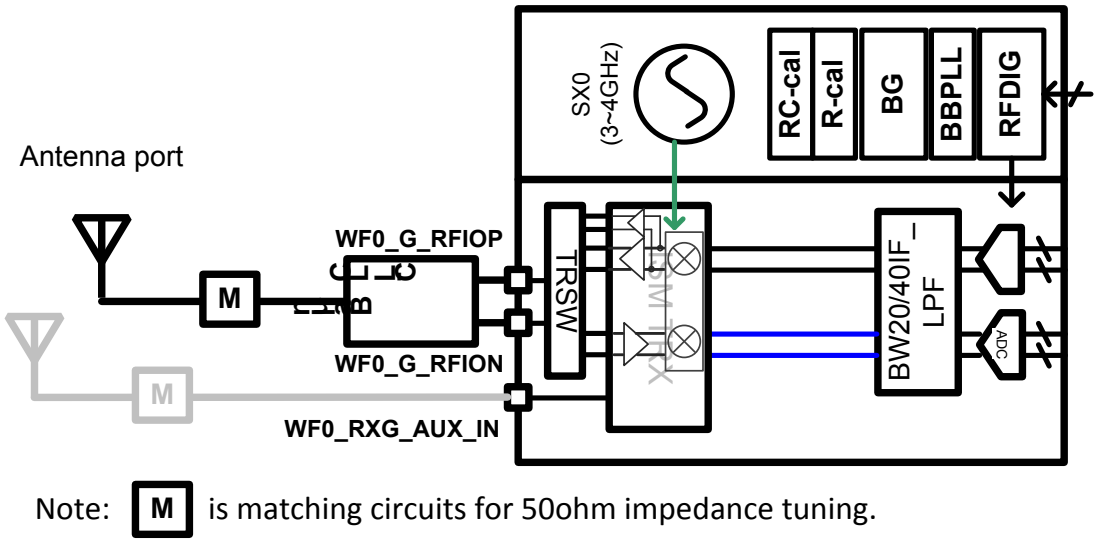



***Figure 3-1*. 2.4GHz RF Block Diagram**

### 3.1.2 Wi-Fi 2.4GHz Band RF Receiver Specifications

The specifications noted in the table below is measured at the antenna port, which includes the front-end loss.

***Table 3-1. 2.4GHz RF Receiver Specification***

| Parameter | Description | Performance | | | |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | Unit |
| Frequency range | Center channel frequency | 2412 | | 2484 | MHz |
| RX sensitivity | 1 Mbps CCK | - | -96.4 | - | dBm |
| | 2 Mbps CCK | - | -93.4 | - | dBm |
| | 5.5 Mbps CCK | - | -91.4 | - | dBm |

| Parameter | Description | Performance | | | |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | Unit |
| | 11 Mbps CCK | - | -88.4 | - | dBm |
| RX sensitivity | BPSK rate 1/2, 6 Mbps OFDM | - | -93.4 | - | dBm |
| | BPSK rate 3/4, 9 Mbps OFDM | - | -91.1 | - | dBm |
| | QPSK rate 1/2, 12 Mbps OFDM | - | -90.3 | - | dBm |
| | QPSK rate 3/4, 18 Mbps OFDM | - | -87.9 | - | dBm |
| | 16QAM rate 1/2, 24 Mbps OFDM | - | -84.6 | - | dBm |
| | 16QAM rate 3/4, 36 Mbps OFDM | - | -81.2 | - | dBm |
| | 64QAM rate 1/2, 48 Mbps OFDM | - | -77.0 | - | dBm |
| | 64QAM rate 3/4, 54 Mbps OFDM | - | -75.7 | - | dBm |
| RX Sensitivity<br>BW=20MHz<br>Mixed mode<br>800ns Guard Interval<br>Non-STBC | MCS 0, BPSK rate 1/2 | - | -92.7 | - | dBm |
| | MCS 1, QPSK rate 1/2 | - | -89.5 | - | dBm |
| | MCS 2, QPSK rate 3/4 | - | -87.1 | - | dBm |
| | MCS 3, 16QAM rate 1/2 | - | -84.1 | - | dBm |
| | MCS 4, 16QAM rate 3/4 | - | -80.6 | - | dBm |
| | MCS 5, 64QAM rate 2/3 | - | -76.2 | - | dBm |
| | MCS 6, 64QAM rate 3/4 | - | -74.8 | - | dBm |
| | MCS 7, 64QAM rate 5/6 | - | -73.6 | - | dBm |
| RX Sensitivity<br>BW=40MHz<br>Mixed mode<br>800ns Guard Interval<br>Non-STBC | MCS 0, BPSK rate 1/2 | - | -89.6 | - | dBm |
| | MCS 1, QPSK rate 1/2 | - | -86.8 | - | dBm |
| | MCS 2, QPSK rate 3/4 | - | -84.3 | - | dBm |
| | MCS 3, 16QAM rate 1/2 | - | -80.8 | - | dBm |
| | MCS 4, 16QAM rate 3/4 | - | -77.7 | - | dBm |
| | MCS 5, 64QAM rate 2/3 | - | -73.1 | - | dBm |
| | MCS 6, 64QAM rate 3/4 | - | -71.8 | - | dBm |
| | MCS 7, 64QAM rate 5/6 | - | -70.6 | - | dBm |
| Maximum Receive Level | 6 Mbps OFDM | - | -10 | - | dBm |
| | 54 Mbps OFDM | - | -10 | - | dBm |
| | MCS0 | - | -10 | - | dBm |
| | MCS7 | - | -20 | - | dBm |
| Receive Adjacent | 1 Mbps CCK | - | 40 | - | dBm |

| Parameter | Description | Performance | | | |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | Unit |
| Channel Rejection | 11 Mbps CCK | - | 40 | - | dBm |
| | BPSK rate 1/2, 6 Mbps OFDM | - | 34 | - | dBm |
| | 64QAM rate 3/4, 54 Mbps OFDM | - | 22 | - | dBm |
| | HT20, MCS 0, BPSK rate 1/2 | - | 33 | - | dBm |
| | HT20, MCS 7, 64QAM rate 5/6 | - | 15 | - | dBm |
| | HT40, MCS 0, BPSK rate 1/2 | - | 29 | - | dBm |
| | HT40, MCS 7, 64QAM rate 5/6 | - | 9 | - | dBm |

### 3.1.3 Wi-Fi 2.4GHz Band RF Transmitter Specifications

The specifications in table are measured at the antenna port, which includes the front-end loss.

***Table 3-2. 2.4GHz RF Transmitter Specifications***

| Parameter | Description | Performance | | | |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | Unit |
| Frequency range | | 2412 | - | 2484 | MHz |
| Output power with spectral mask and EVM compliance | 1 Mbps CCK | - | 21 | - | dBm |
| | 11 Mbps CCK | - | 21 | - | dBm |
| | 6 Mbps OFDM | - | 19 | - | dBm |
| | 54 Mbps OFDM | - | 18 | - | dBm |
| | HT20, MCS 0 | - | 18 | - | dBm |
| | HT20, MCS 7 | - | 17.5 | - | dBm |
| | HT40, MCS 0 | - | 17 | - | dBm |
| | HT40, MCS 7 | - | 16.5 | - | dBm |
| TX EVM | 6 Mbps OFDM | - | - | -5 | dB |
| | 54 Mbps OFDM | - | - | -25 | dB |
| | HT20, MCS 0 | - | - | -5 | dB |
| | HT20, MCS 7 | - | - | -28 | dB |
| | HT40, MCS 0 | - | - | -5 | dB |
| | HT40, MCS 7 | - | - | -28 | dB |
| Output power variation(1) | TSSI closed-loop control across all temperature range and channels and VSWR $\leqq$ 1.5:1. | -1.5 | - | 1.5 | dB |

| Parameter | Description | Performance | | | |
|---|---|---|---|---|---|
| | | MIN | TYP | MAX | Unit |
| Carrier suppression | | - | - | -30 | dBc |
| Harmonic Output Power | 2nd Harmonic | - | -45 | -43 | dBm/MHz |
| | 3nd Harmonic | - | -45 | -43 | dBm/MHz |

*Note 1: VDD33 voltage is within ±5% of typical value.*

# 4 Electrical Characteristics

## 4.1 Absolute Maximum Rating

***Table 4-1 Absolute Maximum Rating***

| Symbol | Parameters | Maximum rating | Unit |
|---|---|---|---|
| VDD33 | 3.3V Supply Voltage | -0.3 to 3.63 | V |
| $T_{STG}$ | Storage Temperature | -40 to +125 | °C |
| VESD | ESD protection (HBM) | 2000 | V |

## 4.2 Recommended Operating Range

***Table 4-2. Recommended Operating Range***

| Symbol | Supply Voltage | Source | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| AVDD45 | AVDD45_BUCK, AVDD45_MISC | To be connected to external 3.3V supply | 2.97 | 3.3 | 3.63 | V |
| RTC_3V3 | RTC_3V3 | To be connected to external supply | 1.6 | | 3.63 | V |
| AVDD33 | AVDD33_WF0_G_PA, AVDD33_WF0_G_TX, AVDD33 | To be connected to external 3.3V supply | 2.97 | 3.3 | 3.63 | V |
| DVDDIO | DVDDIO_D, DVDDIO_L, DVDDIO_R | To be connected to PMU_DIO33_OUT | 2.97 | 3.3 | 3.63 | |
| AVDD25 | AVDD25_AUXADC | To be connected to PMU ALDO output | 2.3 | 2.5 | 2.7 | V |
| AVDD16 | AVDD16_CLDO, AVDD16, AVDD16_XO, AVDD16_WF0_AFE | To be connected to PMU BUCK output | 1.6 | 1.7 | 1.8 | V |
| DVDD11 | DVDD11 | To be connected to PMU CLDO output | 0.86 | 1.15 | 1.3 | V |
| Ta | Operating Ambient Temperature | MT7687FN | -30 | | 85 | C |
| | | MT7687FIN | -40 | | 85 | C |
| Tj | Operating Junction Temperature | MT7687FN | -30 | | 125 | C |
| | | MT7687FIN | -40 | | 125 | C |

## 4.3 DC Characteristics

***Table 4-3. DC Characteristics***

| Symbol | Parameter | Conditions | MIN | MAX | Unit |
|---|---|---|---|---|---|
| $V_{IL}$ | Input Low Voltage | LVTTL | -0.28 | 0.8 | V |

| Symbol | Parameter | Conditions | MIN | MAX | Unit |
|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | | 2 | 3.63 | V |
| $V_{OL}$ | Output Low Voltage | $\|I_{OL}\|$ = 4~16 mA | -0.28 | 0.4 | V |
| $V_{OH}$ | Output High Voltage | $\|I_{OH}\|$ = 4~16 mA | 2.4 | VDD33+0.33 | V |
| $R_{PU}$ | Input Pull-Up Resistance | PU=high, PD=low | 40 | 190 | KΩ |
| $R_{PD}$ | Input Pull-Down Resistance | PU=low, PD=high | 40 | 190 | KΩ |

## 4.4 XTAL Oscillator

The table below lists the XTAL requirements for the XTAL.

***Table 4-4. XTAL Oscillator Requirements***

| Parameter | Value |
|---|---|
| Frequency | 26, 40, 52MHz. |
| Frequency stability | ±10 ppm @ 25℃ |
| Aging | ±3 ppm/year |

## 4.5 PMU Characteristics

***Table 4-5. PMU Electrical Characteristics***

| Parameter | | Reference | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **Switching regulator (BUCK)** | | | | | | | |
| Vin | Input Voltage | AVDD45_BUCK | | 2.97 | 3.3 | 3.63 | V |
| Vout | Output Voltage | LXBK | Switching operation | 1.6 | 1.7 | 1.8 | V |
| | | | Deep Sleep mode, SLDO-H enabled | | 1.8 | | V |
| Iout | Output Current | | Switching operation | | | 800 | mA |
| | | | Deep Sleep mode, SLDO-H enabled | | | 10 | mA |
| | | | Over-current shutdown | 960 | 1600 | 4000 | mA |
| Iq | Quiescent Current | | Iload < 1mA | | 150 | | uA |
| DC/DC | Line Regulation | | Iload = 0mA | | | 1 | % |
| | Load regulation | | Iload = 200-400mA | | | 0.05 | mV/mA |
| | Efficiency | | Vin = 3.3V, Iload = 400mA | 80 | 85 | | % |
| **Core LDO (CLDO)** | | | | | | | |
| Vin | Input | AVDD16_CLDO | | 1.6 | 1.7 | 1.8 | V |

| Parameter | | Reference | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Vout | Output Voltage | AVDD12_VCORE | Normal operation | 0.86 | 1.15 | 1.3 | V |
| | | | Deep Sleep mode, SLDO-L enabled | | 0.85 | | V |
| Iout | Output Current | | Normal operation | | | 420 | mA |
| | | | Deep Sleep mode, SLDO-L enabled | | | 10 | mA |
| Iq | Quiescent Current | | | | 40 | 50 | uA |
| **Analog LDO (ALDO)** | | | | | | | |
| Vin | Input Voltage | | | 2.97 | 3.3 | 3.63 | V |
| Vout | Output Voltage | AVDD25_ALDO | Normal operation | 2.3 | 2.5 | 2.7 | V |
| | | | Deep Sleep mode, OFF | | 0 | | V |
| Iout | Output Current | | Normal operation | | | 50 | mA |
| Iq | Quiescent Current | | | | 25 | 50 | uA |
| **PMU** | | | | | | | |
| Vin | Input Voltage | AVDD45, AVDD33 and DVDDIO | | 2.97 | 3.3 | 3.63 | V |
| Iq | Quiescent Current | | In Deep Sleep State | | | 50 | uA |

## 4.6 Auxiliary ADC Characteristics

This section specifies the electrical characteristics of the auxiliary ADC.

***Table 4-6. Auxiliary ADC Specifications***

| Symbol | Parameter | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| N | Resolution | - | 12 | - | Bit |
| FS | Sampling Rate @ N-Bit[1] | - | 2 | - | MSPS |
| VPP | Input Swing[2] | - | - | AVDD25 (2.45~2.55V) | V |
| VIN | Input voltage[3] | 0 | - | AVDD25 (2.45~2.55V) | V |
| RIN | Input Impedance:<br>Unselected channel<br>Selected channel | <br>400M<br>- | <br>-<br>10K | <br>-<br>- | Ohm |
| DNL | Differential Nonlinearity without dithering and averaging | - | ± 1 | ± 2 | LSB |

| Symbol | Parameter | Min | Typical | Max | Unit |
|---|---|---|---|---|---|
| INL | Integral Nonlinearity without dithering and averaging | - | ± 2 | ± 4 | LSB |
| $DNL_{dither+average}$ | Differential Nonlinearity with dithering and averaging | - | ± 0.5 | ± 1 | LSB |
| $INL_{dither+average}$ | Integral Nonlinearity with dithering and averaging | - | - | ± 2 | LSB |
| OE | Offset Error | - | - | ± 10 | mV |
| FSE | Full Swing Error | - | - | ± 50 | mV |
| SNR | Signal to Noise Ratio(2) | 60 | 63 | 66 | dB |
| | Current Consumption | - | - | 400 | µA |
| | Power-Down Current | - | - | 1 | µA |

*Note 1: Given that FS=2MHz*

*Note 2: At 1K Hz Input Frequency*

*Note 3: The voltage level is lowered by 0.04V when dithering is on.*

## 4.7 Thermal Characteristics

$\Theta_{JC}$ assumes that all the heat is dissipated through the top of the package, while $\Psi_{Jt}$ assumes that the heat is dissipated through the top, sides, and the bottom of the package. Thus it is suggested to use $\Psi_{Jt}$ to estimate the junction temperature.

***Table 4-7. Thermal Characteristics***

| Symbol | Description | Performance | |
|---|---|---|---|
| | | Typical | Unit |
| $T_J$ | Maximum Junction Temperature (Plastic Package) | 125 | °C |
| $\Theta_{JA}$ | Junction to ambient temperature thermal resistance[1] | 19.21 | °C/W |
| $\Theta_{JC}$ | Junction to case temperature thermal resistance | 7.33 | °C/W |
| $\Psi_{Jt}$ | Junction to the package thermal resistance[2] | 1.65 | °C/W |

*Note 1: JEDEC 51-7 system FR4 PCB size: 76.2mm x 114.3mm*

*Note 2: 8mm x 8mm QFN-68 package*

## 4.8 Power Performance Summary

Table 4-8 lists the current consumptions in VBAT domain. Note that the measurement conditions are typical conditions for process, voltage (3.3v) and temperature (25°C).

***Table 4-8. Current consumption in different scenarios***

| Scenario | Test Conditions | Typical | Unit |
|---|---|---|---|
| Legacy Sleep | • MCU subsystem clocks are gated off<br>• The entire subsystem is retained<br>• Only 32KHz clock from XTAL is active | 0.667 | mA |
| RTC mode[1] | • System Off<br>• No SRAM retained<br>• Only RTC is alive | 0.0031 | mA |
| WIFI Radio Off | • WFI Sleep mode[1]<br>• Tickless feature enabled | 10.79 | mA |
| | • Legacy Sleep mode[1]<br>• Tickless feature enabled | 0.97 | mA |
| WIFI Connected | • WFI Sleep mode<br>• Tickless feature enabled | 14.18 | mA |

| Scenario | Test Conditions | Typical | Unit |
|---|---|---|---|
| | • DTIM1[2] | | |
| | • Legacy Sleep mode<br>• Tickless feature enabled<br>• DTIM1[2] | 4.64 | mA |
| | • Legacy Sleep mode<br>• Tickless feature enabled<br>• DTIM10[2] | 2.07 | mA |

*Note 1: Please refer to LinkIt_for_RTOS_Power_Mode_Developers_Guide.pdf chapter 3.1 for power modes*

*Note 2:* DTIM, A **delivery traffic indication map** is a kind of traffic indication map (TIM) which informs the clients about the presence of buffered multicast/broadcast data on the access point. It is generated within the periodic beacon at a frequency specified by the DTIM Interval

DTIM 1: DTIM interval = 1, WIFI wake up each beacon period (default 100 ms)

DTIM 10: DTIM interval = 10, WIFI wake up every 10 beacon period (1000ms)

# 5 Package Specifications

## 5.1 Pin Layout

MT7687F uses 8mm x 8mm QFN package of 68-pin with 0.4mm pitch.

***Table 5-1. Pin Map***

| | | 68 | 67 | 66 | 65 | 64 | 63 | 62 | 61 | 60 | 59 | 58 | 57 | 56 | 55 | 54 | 53 | 52 | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | NC | AVDD33 | NC | AVDD33_WF0_G_TX | WF0_G_RFIOP | WF0_G_RFION | AVDD33_WF0_G_PA | WF0_RXG_AUX_IN | AVDD16 | AVDD33 | NC | GPIO33 | GPIO34 | GPIO35 | GPIO36 | GPIO37 | GPIO38 | | |
| 1 | AVDD33 | | | | | | | | | | | | | | | | | | SYSRST_B | 51 |
| 2 | AVDD16_WF0_AFE | | | | | | | | | | | | | | | | | | GPIO39 | 50 |
| 3 | AVDD16_XO | | | | | | | | | | | | | | | | | | DVDD11 | 49 |
| 4 | XO | | | | | | | | | | | | | | | | | | DVDDIO_L | 48 |
| 5 | GPIO0 | | | | | | | | | | | | | | | | | | GPIO57 | 47 |
| 6 | GPIO1 | | | | | | | | | | | | | | | | | | GPIO58 | 46 |
| 7 | GPIO2 | | | | | | | | | | | | | | | | | | GPIO59 | 45 |
| 8 | GPIO3 | | | | | | | | | | | | | | | | | | GPIO60 | 44 |
| 9 | GPIO4 | | | | | | | | | VSS | | | | | | | | | AVDD25_AUXADC | 43 |
| 10 | GPIO5 | | | | | | | | | | | | | | | | | | AVSS25_AUXADC | 42 |
| 11 | GPIO6 | | | | | | | | | | | | | | | | | | AVSS45_BUCK | 41 |
| 12 | GPIO7 | | | | | | | | | | | | | | | | | | LXBK | 40 |
| 13 | DVDDIO_R | | | | | | | | | | | | | | | | | | AVDD45_BUCK | 39 |
| 14 | DVDD11 | | | | | | | | | | | | | | | | | | AVDD15_V2P5NA | 38 |
| 15 | GPIO24 | | | | | | | | | | | | | | | | | | AVDD16_CLDO | 37 |
| 16 | DVDDIO_D | | | | | | | | | | | | | | | | | | AVDD12_VCORE | 36 |
| 17 | DVDD11 | | | | | | | | | | | | | | | | | | PMU_TEST | 35 |
| | | GPIO25 | GPIO26 | RTC_3V3 | RTC_32K_XO | RTC_32K_XI | PMU_EN_RTC | GPIO32 | GPIO31 | GPIO27 | GPIO30 | GPIO28 | GPIO29 | PMU_DIO33_OUT | AVDD25_ALDO_OUT | PMU_EN_WF | ISO_INT_PMU_EN | AVDD45_MISC | | |
| | | 18 | 19 | 20 | 21 | 22 | 23 | 24 | 25 | 26 | 27 | 28 | 29 | 30 | 31 | 32 | 33 | 34 | | |

## 5.2 Pin Description

The section describes the pin functionality of MT7687F chip.

***Table 5-2. Pin Descriptions***

| QFN | Pin Name | Pin description | PU/PD | I/O | Supply domain |
|---|---|---|---|---|---|
| **Reset and Clocks** | | | | | |
| 51 | SYSRST_B | External system reset active low | PU | Input | DVDDIO |
| 4 | XO | Crystal input or external clock input | N/A | Input | AVDD16_XO |
| 3 | AVDD16_XO | RF 1.6V power supply | N/A | Power | |
| **Programmable I/O** | | | | | |
| 5 | GPIO0 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 6 | GPIO1 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 7 | GPIO2 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 8 | GPIO3 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 9 | GPIO4 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 10 | GPIO5 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 11 | GPIO6 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 12 | GPIO7 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 15 | GPIO24 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 18 | GPIO25 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 19 | GPIO26 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 26 | GPIO27 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 28 | GPIO28 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 29 | GPIO29 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 27 | GPIO30 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 25 | GPIO31 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 24 | GPIO32 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 57 | GPIO33 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 56 | GPIO34 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 55 | GPIO35 | Programmable input/output | PU/PD | In/out | DVDDIO |

| QFN | Pin Name | Pin description | PU/PD | I/O | Supply domain |
|---|---|---|---|---|---|
| 54 | GPIO36 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 53 | GPIO37 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 52 | GPIO38 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 50 | GPIO39 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 47 | GPIO57 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 46 | GPIO58 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 45 | GPIO59 | Programmable input/output | PU/PD | In/out | DVDDIO |
| 44 | GPIO60 | Programmable input/output | PU/PD | In/out | DVDDIO |
| **RTC** | | | | | |
| 20 | VRTC | RTC domain power supply | N/A | Power | |
| 21 | RTC_32K_XO | 32KHz crystal | N/A | Analog | VRTC |
| 22 | RTC_32K_XI | 32KHz crystal | N/A | Analog | VRTC |
| 23 | PMU_EN_RTC | PMU enable | N/A | Output | VRTC |
| **WIFI Radio Interface** | | | | | |
| 1,59, 67 | AVDD33 | RF 3.3v power supply | N/A | Power | |
| 62 | AVDD33_WF0_G_PA | RF 3.3v power supply | N/A | Power | |
| 65 | AVDD33_WF0_G_TX | RF 3.3v power supply | N/A | Power | |
| 2 | AVDD16_WF0_AFE | RF 1.6v power supply | N/A | Power | |
| 58, 66,68 | NC | No Connected | N/A | Input | |
| 61 | WF0_RXG_AUX_IN | RF g-band auxiliary RF LNA port | N/A | Input | AVDD33_WF0_G |
| 64 | WF0_G_RFIOP | RF g-band RF port | N/A | In/out | AVDD33_WF0_G |
| 63 | WF0_G_RFION | RF g-band RF port | N/A | In/out | AVDD33_WF0_G |
| 60 | AVDD16 | RF 1.6v power supply | N/A | Power | |
| **PMU/BUCK** | | | | | |
| 41 | AVSS45_BUCK | BUCK ground | N/A | Ground | |
| 40 | LXBK | BUCK output | N/A | Output | |
| 39 | AVDD45_BUCK | BUCK power supply | N/A | Input | |
| 38 | AVDD15_V2P5NA | BUCK internal circuit output cap | N/A | Output | |
| 37 | AVDD16_CLDO | CLDO supply | N/A | Input | |
| 36 | AVDD12_VCORE | CLDO output | N/A | Output | |

| QFN | Pin Name | Pin description | PU/PD | I/O | Supply domain |
|---|---|---|---|---|---|
| 34 | AVDD45_MISC | PMU supply | N/A | Input | |
| 31 | AVDD25_ALDO_OUT | 2.5V ALDO output with external cap. | N/A | Output | |
| 30 | PMU_DIO33_OUT | This pin output is to provide 3.3V for all DVDDIO.<br><br>And in OFF mode, this pin is 0V. | N/A | Output | |
| 35 | PMU_TEST | PMU test pin | N/A | Output | |
| 33 | ISO_INT_PMU_EN | Input 0V for non-RTC platform.<br>Input 3.3V for RTC platform. | N/A | Input | |
| 32 | PMU_EN_WF | External PMU enable | N/A | Input | |
| **Power Supplies** | | | | | |
| 43 | AVDD25_AUXADC | Auxiliary ADC 2.5v power supply | N/A | Power | |
| 42 | AVSS25_AUXADC | Auxiliary ADC ground | N/A | Ground | |
| 13 | DVDDIO_R | Digital 3.3V input | N/A | Power | |
| 16 | DVDDIO_D | Digital 3.3V input | N/A | Power | |
| 48 | DVDDIO_L | Digital 3.3V input | N/A | Power | |
| 14, 17, 30, 49 | DVDD11 | Digital 1.15V input | N/A | Power | |
| E-PAD | VSS | Common Ground | N/A | Ground | |

## 5.3 Pin Multiplexing

The pin multiplexing could be controlled via the configuration register A (in TOP_AON domain) and the configuration register B (in TOP_OFF/N9 domain). When configuration register A is set to 0, the configuration register B determines the pin function. When configuration register A is not set to 0, the configuration register A determines the pin function.

The default function of each pin is highlighted with blue background.

The driving strength of all pins is programmable: 4mA, 8mA, 12mA, and 16mA. The default setting for all pins are 4mA.

***Table 5-3. Pin Multiplexing***

| Pin | Pin alias | APGIO/ GPIO | Name | Dir | Default dir | Default PU/PD | Description | Pinx_pinmux_aon_sel | | Pinx_pinmux_off_sel | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | | | | | Address | Value | | Value |
| 5 | GPIO0 | AGPIO | **MCU_JTCK** | **I** | **I** | **PD** | N9 JTAG debug port | 0x8102_3020[3:0] | 0 | 0x8002_5100[3:0] (0x8102_3020[3:0]=0) | **0** |
| | | | ANTSEL[0] | O | | | RF control | | - | | 1 |
| | | | UART0_RTS_CM4 | O | | | UART0 RTS (CM4) | | 7 | | 3 |
| | | | GPIO_TOPOFF[0] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[0] | O | | | General purpose input output | | 8 | | - |
| | | | PWM[0] | I/O | | | Pulse-width-modulated output | | 9 | | - |
| | | | EINT[0] | I | | | External interrupt | | 3 | | - |
| 6 | GPIO1 | AGPIO | **MCU_JTMS** | **I** | **I** | **PD** | N9 JTAG debug port | 0x8102_3020[7:4] | 0 | 0x8002_5100[7:4] (0x8102_3020[7:4]=0) | **0** |
| | | | ANTSEL[1] | O | | | RF control | | - | | 1 |
| | | | UART0_CTS_CM4 | I | | | UART0 CTS (CM4) | | 7 | | 3 |
| | | | GPIO_TOPOFF[1] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[1] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[1] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | EINT[1] | I | | | External interrupt | | 3 | | - |
| 7 | GPIO2 | AGPIO | **MCU_JTDI** | **I** | **I** | **PD** | N9 JTAG debug port | 0x8102_3020[11:8] | 0 | 0x8002_5100[11:8] (0x8102_3020[11:8]=0) | **0** |
| | | | ANTSEL[2] | O | | | RF control | | - | | 1 |
| | | | MCU_AICE_TMSC | I/O | | | N9 debug | | - | | 2 |
| | | | UART0_RX_CM4 | I | | | UART0 RX (CM4) | | 7 | | 3 |
| | | | SWD_CLK | O | | | CM4 SWD debug port | | 4 | | 4 |
| | | | GPIO_TOPOFF[2] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[2] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[23] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | WIC[0] | I | | | External interrupt | | 3 | | - |
| 8 | GPIO3 | AGPIO | **MCU_JTRST_B** | **I** | **I** | **PD** | N9 JTAG debug port | 0x8102_3020[15:12] | 0 | 0x8002_5100[15:12] (0x8102_3020[15:12]=0) | **0** |
| | | | ANTSEL[3] | O | | | RF control | | - | | 1 |
| | | | [Reserved] | I | | | [Reserved] | | - | | 2 |
| | | | UART0_TX_CM4 | O | | | UART0 TX (CM4) | | 7 | | 3 |
| | | | SWD_DIO | I/O | | | CM4 SWD debug port | | 4 | | 4 |
| | | | GPIO_TOPOFF[3] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[3] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[24] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | EINT[2] | I | | | External interrupt | | 3 | | - |
| | | | PULSE_CNT | I | | | Pulse counter | | 2 | | - |
| 9 | GPIO4 | GPIO | **MCU_DBGIN** | **I** | **I** | **PD** | N9 JTAG debug port | 0x8102_3020[19:16] | 0 | 0x8002_5100[19:16] (0x8102_3020[19:16]=0) | **0** |
| | | | ANTSEL[4] | O | | | RF control | | - | | 1 |
| | | | MCU_AICE_TCKC | I | | | N9 debug | | - | | - |
| | | | SPI_DATA0_EXT * | I/O | | | External flash interface | | 7 | | 3 |
| | | | GPIO_TOPOFF[4] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[4] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[2] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | EINT[3] | I | | | External interrupt | | 3 | | - |
| 10 | GPIO5 | GPIO | **[Debug flag]** | **O** | **O(Low)** | | Debug monitor pin | 0x8102_3020[23:20] | 0 | 0x8002_5100[23:20] (0x8102_3020[23:20]=0) | **0** |
| | | | ANTSEL[5] | O | | | RF control | | - | | 1 |
| | | | SPI_DATA1_EXT * | O | | | External flash interface | | 7 | | 3 |
| | | | GPIO_TOPOFF[5] | I/O | I | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[5] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[3] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | EINT[4] | I | | | External interrupt | | 3 | | - |
| 11 | GPIO6 | GPIO | **MCU_DBGACKN** | **O** | **O** | | N9 JTAG debug port | 0x8102_3020[27:24] | 0 | 0x8002_5100[27:24] | **0** |

| Pin | Pin alias | APGIO/ GPIO | Name | Dir | Default dir | Default PU/PD | Description | Pinx_pinmux_aon_sel | | Pinx_pinmux_off_sel | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | ANTSEL[6] | O | | | RF control | | - | (0x8102_3020[27:24]=0) | 1 |
| | | | SPI_CS_1_M_CM4 | O | | | SPI master chip select 1 | | 7 | | 3 |
| | | | GPIO_TOPOFF[6] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[6] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[4] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | EINT[5] | I | | | External interrupt | | 3 | | - |
| 12 | GPIO7 | GPIO | **MCU_JTDO** | **O** | **O(Low)** | | N9 JTAG debug port | 0x8102_3020[31:28] | 0 | 0x8002_5100[31:28] (0x8102_3020[31:28]=0) | **0** |
| | | | ANTSEL[7] | O | | | RF control | | - | | 1 |
| | | | SPI_CS_0_M_CM4 | O | | | SPI master chip select 0 | | 6 | | 2 |
| | | | SPI_CS_EXT * | O | | | External flash interface | | 7 | | 3 |
| | | | GPIO_TOPOFF[7] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[7] | | | | General purpose input output | | 8 | | - |
| | | | PWM[5] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | EINT[6] | I | | | External interrupt | | 3 | | - |
| | | | [Reserved] | | | | [Reserved] | | - | | 0 |
| | | | UART_DSN_TXD_N9 | O | | | UART_DSN TX (N9) | | - | | 1 |
| | | | SPI_MOSI_M_CM4 | O | | | SPI master MOSI | | 6 | | 2 |
| | | | SPI_DATA2_EXT * | I/O | | | External flash interface | | 7 | | 3 |
| 15 | GPIO24 | GPIO | I2C1_CLK | I/O | | | I2C1 CLK | 0x8102_302C[3:0] | 4 | 0x8002_510C[3:0] (0x8102_302C[2:0]=0) | 4 |
| | | | GPIO_TOPOFF[24] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[24] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[25] | O | | | Pulse width modulation | | 9 | | - |
| | | | **[Reserved]** | **I** | **I** | **PU** | [Reserved] | | **1** | | - |
| | | | [Reserved] | O | | | [Reserved] | | 2 | | - |
| | | | [Reserved] | | | | [Reserved] | | - | | 0 |
| | | | SPI_MISO_M_CM4 | I | | | SPI master MISO | | - | | 2 |
| | | | SPI_DATA3_EXT * | I/O | | | External flash interface | | 7 | | 3 |
| | | | I2C1_DATA | I/O | | | I2C1 DATA | | 4 | | 4 |
| 18 | GPIO25 | GPIO | GPIO_TOPOFF[25] | I/O | | | General purpose input output | 0x8102_302C[7:4] | - | 0x8002_510C[7:4] (0x8102_302C[7:4]=0) | 5 |
| | | | GPIO_TOPAON[25] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[26] | O | | | Pulse width modulation | | 9 | | - |
| | | | **[Reserved]** | **I/O** | **O** | **PU** | Default: Low. | | **1** | | **-** |
| | | | FRAME_SYNC * | I | | | 3DD synchronization | | 2 | | - |
| | | | WIC[1] | I | | | External interrupt | | 3 | | - |
| | | | [Reserved] | | | | [Reserved] | | - | | 0 |
| | | | SPI_SCK_M_CM4 | O | | | SPI master SCK | | 6 | | 2 |
| | | | SPI_CLK_EXT * | O | | | External flash interface | | 7 | | 3 |
| 19 | GPIO26 | GPIO | I2S_TX | O | | | I2S TX | 0x8102_302C[11:8] | 4 | 0x8002_510C[11:8] (0x8102_302C[11:8]=0) | 4 |
| | | | GPIO_TOPOFF[26] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[26] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[27] | O | | | Pulse width modulation | | 9 | | - |
| | | | **[Reserved]** | **I/O** | **O** | **PU** | Default: Low. | | **1** | | **-** |
| | | | SWD_DIO | I/O | | | CM4 SWD debug port | | 5 | | 1 |
| | | | I2C0_CLK | O | | | I2C0 CLK | | 4 | | 3 |
| | | | GPIO_TOPOFF[27] | I/O | | | General purpose input output | | - | | 5 |
| 26 | GPIO27 | GPIO | GPIO_TOPAON[27] | I/O | | | General purpose input output | 0x8102_302C[15:12] | 8 | 0x8002_510C[15:12] (0x8102_302C[15:12]=0) | - |
| | | | PWM[28] | O | | | Pulse width modulation | | 9 | | - |
| | | | **[Reserved]** | **I** | **I** | | [Reserved] | | **1** | | - |
| | | | PULSE_CNT | I | | | Pulse counter input | | 2 | | - |
| | | | WIC[2] | I | | | External interrupt | | 3 | | - |
| | | | SWD_CLK | I | | | CM4 SWD debug port | | 5 | | 1 |
| 28 | GPIO28 | GPIO | SPI_INT_S_N9 | O | | | SPI | 0x8102_302C[19:16] | - | 0x8002_510C[19:16] (0x8102_302C[19:16]=0) | 2 |
| | | | I2C0_DATA | O | | | I2C0 DATA | | 4 | | 3 |

| Pin | Pin alias | APGIO/ GPIO | Name | Dir | Default dir | Default PU/PD | Description | Pinx_pinmux_aon_sel | | Pinx_pinmux_off_sel | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | GPIO_TOPOFF[28] | I/O | | | General purpose input output | | 0 | | 5 |
| | | | GPIO_TOPAON[28] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[29] | O | | | Pulse width modulation | | 9 | | - |
| | | | **[Reserved]** | **I/O** | **I** | | [Reserved] | | **1** | | **-** |
| 29 | GPIO29 | GPIO | I2S_MCLK_S | O | | | I2S MCLK slave | 0x8102_302C[23:20] | - | 0x8002_510C[23:20] (0x8102_302C[23:20]=0) | 0 |
| | | | SPI_MOSI_S_CM4 | I | | | SPI slave MOSI (CM4) | | 6 | | 1 |
| | | | SPI_MOSI_S_N9 | I | | | SPI slave MOSI (N9) | | - | | 2 |
| | | | SPI_MOSI_M_CM4 | O | | | SPI master MOSI | | 7 | | 3 |
| | | | **[Reserved]** | O | | | **[Reserved]** | | 4 | | 4 |
| | | | GPIO_TOPOFF[29] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[29] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[30] | O | | | Pulse width modulation | | 9 | | - |
| | | | **[Reserved]** | **I/O** | **I** | | [Reserved] | | **1** | | **-** |
| | | | HOST_ACK | O | | | | | 2 | | - |
| | | | WIC[3] | I | | | External interrupt | | 3 | | - |
| 27 | GPIO30 | GPIO | **[Reserved]** | O | | | **[Reserved]** | 0x8102_302C[27:24] | 5 | 0x8002_5108[27:24] (0x8102_302C[27:24]=0) | 0 |
| | | | SPI_MISO_S_CM4 | O | | | SPI slave MISO (CM4) | | 6 | | 1 |
| | | | SPI_MISO_S_N9 | O | | | SPI slave MISO (N9) | | 0 | | 2 |
| | | | SPI_MISO_M_CM4 | I | | | SPI master MISO | | 7 | | 3 |
| | | | I2S_FS | I | | | I2S slave FS | | 4 | | 4 |
| | | | GPIO_TOPOFF[30] | I/O | | | General purpose input output | | 0 | | 5 |
| | | | GPIO_TOPAON[30] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[31] | O | | | Pulse width modulation | | 9 | | - |
| | | | **[Reserved]** | **I/O** | **I** | | [Reserved] | | 1 | | - |
| | | | HOST_EINT_B | I | | | | | 2 | | - |
| 25 | GPIO31 | GPIO | I2S_TX | O | | | I2S TX | 0x8102_302C[31:28] | 5 | 0x8002_510C[31:28] (0x8102_302C[31:28]=0) | 0 |
| | | | SPI_SCK_S_CM4 | I | | | SPI slave SCK (CM4) | | 6 | | 1 |
| | | | SPI_SCK_S_N9 | I | | | SPI slave SCK (N9) | | - | | 2 |
| | | | SPI_SCK_M | O | | | SPI master SCK | | 7 | | 3 |
| | | | I2S_RX | I | | | I2S slave RX | | 4 | | 4 |
| | | | GPIO_TOPOFF[31] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[31] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[32] | O | | | Pulse width modulation | | 9 | | - |
| | | | **[Reserved]** | **I/O** | **I** | | [Reserved] | | 1 | | - |
| 24 | GPIO32 | GPIO | **[Reserved]** | O | | | **[Reserved]** | 0x8102_3030[3:0] | 5 | 0x8002_5110 [3:0] (0x8102_3030[3:0]=0) | 0 |
| | | | SPI_CS_0_S_CM4 | I | | | SPI slave CS (CM4) | | 6 | | 1 |
| | | | SPI_CS_0_S_N9 | I | | | SPI slave CS (N9) | | - | | 2 |
| | | | SPI_CS_0_M | O | | | SPI master CS | | 7 | | 3 |
| | | | I2S_BCLK | I | | | I2S BCLK slave | | 4 | | 4 |
| | | | GPIO_TOPOFF[32] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[32] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[33] | O | | | Pulse width modulation | | 9 | | - |
| | | | **[Reserved]** | **I/O** | **I** | | [Reserved] | | 1 | | - |
| | | | WIC[4] | I | | | External interrupt | | 3 | | - |
| 57 | GPIO33 | AGPIO | **WIFI_INT_B** | **I/O** | **O** | **PU** | External interrupt | 0x8102_3030 [7:4] | 0 | 0x8002_5110 [7:4] (0x8102_3030 [7:4]=0) | **0** |
| | | | ALL_INT_B | I/O | | | External interrupt | | - | | 1 |
| | | | SWD_DIO | I/O | | | CM4 SWD debug port | | 6 | | 2 |
| | | | IR_TX | O | | | IrDA TX | | 7 | | 3 |
| | | | ANTSEL[5] | O | | | RF control | | 4 | | 4 |
| | | | GPIO_TOPOFF[33] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[33] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[34] | O | | | Pulse width modulation | | 9 | | - |
| | | | PULSE_CNT | I | | | Pulse counter | | 1 | | - |

| Pin | Pin alias | APGIO/ GPIO | Name | Dir | Default dir | Default PU/PD | Description | Pinx_pinmux_aon_sel | | Pinx_pinmux_off_sel | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | WF_LED_B | O | | | LED output | | 2 | | - |
| | | | WIC[5] | I | | | External interrupt | | 3 | | - |
| 56 | GPIO34 | AGPIO | **MISC_INT_B** | **I/O** | **O** | **PU** | External interrupt | 0x8102_3030 [11:8] | 0 | 0x8002_5110 [11:8] (0x8102_3030 [11:8]=0) | **0** |
| | | | ALL_INT_B | I/O | | | | | - | | 1 |
| | | | SWD_CLK | I | | | CM4 SWD debug port | | 6 | | 2 |
| | | | IR_RX | I | | | IrDA RX | | 7 | | 3 |
| | | | ANTSEL[6] | O | | | RF control | | 4 | | 4 |
| | | | GPIO_TOPOFF[34] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[34] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[35] | O | | | Pulse width modulation | | 9 | | - |
| | | | FRAME_SYNC * | I | | | 3DD synchronization | | 1 | | - |
| | | | MISC_LED_B | I/O | | | LED output | | 2 | | - |
| | | | WIC[6] | I | | | External interrupt | | 3 | | - |
| 55 | GPIO35 | GPIO | **UART_DSN_TXD_N9** | **O** | **O** | **PD** | UART DSN TX (N9) | 0x8102_3030 [15:12] | 0 | 0x8002_5110 [15:12] (0x8102_3030 [15:12]=0) | **0** |
| | | | UART_DBG_CM4 | O | | | UART DBG TX (CM4) | | 7 | | 3 |
| | | | GPIO_TOPOFF[35] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[35] | I/O | | | General purpose input output | | 8 | | - |
| | | | I2S_TX | O | | | I2S TX | | 5 | | - |
| | | | PWM[18] | O | | | Pulse-width-modulated output | | 9 | | - |
| 54 | GPIO36 | GPIO | [Reserved] | | | | [Reserved] | 0x8102_3030 [19:16] | - | 0x8002_5110 [19:16] (0x8102_3030 [19:16]=0) | 0 |
| | | | S2A_SPI_IN | I | | | SPI input | | - | | 1 |
| | | | UART1_RX_CM4 | I | | | UART1 RX (CM4) | | 7 | | 3 |
| | | | GPIO_TOPOFF[36] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[36] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[19] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | **UART_RXD_N9** | **I** | **I** | **PU** | UART RX (N9) | | **1** | | - |
| | | | WIC[7] | I | | | External interrupt | | 3 | | - |
| 53 | GPIO37 | GPIO | **UART_TXD_N9** | **O** | **O** | **PD** | UART TX (N9) | 0x8102_3030 [23:20] | 0 | 0x8002_5110 [23:20] (0x8102_3030 [23:20]=0) | **0** |
| | | | UART1_TX_CM4 | O | | | UART1 TX (CM4) | | 7 | | 3 |
| | | | GPIO_TOPOFF[37] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[37] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[20] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | EINT[20] | I | | | External interrupt | | 3 | | - |
| 52 | GPIO38 | GPIO | **UART_RTS_N9** | **O** | **O** | **PD** | UART RTS (N9) | 0x8102_3030 [27:24] | 0 | 0x8002_5110 [27:24] (0x8102_3030 [26:24]=0) | **0** |
| | | | PTA_EINT_B | I | | | Packet traffic arbitration | | - | | 1 |
| | | | IDC_DATA_OUT | O | | | UART IDC TX (N9) | | - | | 2 |
| | | | UART1_RTS_CM4 | O | | | UART1 RTS (CM4) | | 7 | | 3 |
| | | | GPIO_TOPOFF[38] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[38] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[21] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | WF_LED_B | I/O | | | LED output | | 2 | | - |
| | | | EINT[21] | I | | | External interrupt | | 3 | | - |
| | | | SWD_DIO | I/O | | | CM4 SWD debug port | | 6 | | - |
| 50 | GPIO39 | GPIO | **UART_CTS_N9** | **I** | **I** | **PU** | UART CTS (N9) | 0x8102_3030 [31:28] | 0 | 0x8002_5110[31:28] (0x8102_3030 [31:28]=0) | **0** |
| | | | PTA_EINT_B | I | | | Packet traffic arbitration | | - | | 1 |
| | | | IDC_DATA_IN | I | | | UART IDC RX (N9) | | - | | 2 |
| | | | UART1_CTS_CM4 | O | | | UART1 CTS (CM4) | | 7 | | 3 |
| | | | [Reserved] | | | | [Reserved] | | - | | 4 |
| | | | GPIO_TOPOFF[39] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[39] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[22] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | PULSE_COUNT * | I | | | Pulse counter | | 1 | | - |

| Pin | Pin alias | APGIO/ GPIO | Name | Dir | Default dir | Default PU/PD | Description | Pinx_pinmux_aon_sel | | Pinx_pinmux_off_sel | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | MISC_LED_B | I/O | | | LED output | | 2 | | - |
| | | | EINT[22] | I | | | External interrupt | | 3 | | - |
| | | | SWD_CLK | I | | | CM4 SWD debug port | | 6 | | - |
| 47 | GPIO57 | AGPIO | [Reserved] | I/O | | | [Reserved] | 0x8102_303C [7:4] (0x8102_300C[6]=0) | - | 0x8002_511C [7:4] (0x8102_303C [7:4]=0, 0x8102_300C[6]=0) | 0 |
| | | | S2A_SPI_CK | I | | | | | - | | 1 |
| | | | MCU_AICE_TCKC | I | | | N9 debug | | - | | 2 |
| | | | GPIO_TOPOFF[57] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[57] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[36] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | **[Reserved]** | **I** | **I** | **PU** | [Reserved] | | **1** | | - |
| | | | WIC[8] | I | | | External interrupt | | 3 | | - |
| | | | ADC_IN0 | I | | | Auxiliary ADC input | 0x8102_300C[6] | 1 | | - |
| 46 | GPIO58 | AGPIO | [Reserved] | I/O | | | [Reserved] | 0x8102_303C[11:8]=0 (0x8102_300C[7]=0) | - | 0x8002_511C [11:8] (0x8102_303C[11:8]=0, 0x8102_300C[7]=0) | 0 |
| | | | S2A_SPI_OUT | O | | | | | - | | 1 |
| | | | MCU_AICE_TMSC | I/O | | | N9 debug | | - | | 2 |
| | | | GPIO_TOPOFF[58] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[58] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[37] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | **[Reserved]** | **I** | **I** | **PU** | [Reserved] | | **1** | | - |
| | | | WIC[9] | I | | | External interrupt | | 3 | | - |
| | | | ADC_IN1 | I | | | Auxiliary ADC input | 0x8102_300C[7] | 1 | | - |
| 45 | GPIO59 | AGPIO | [Reserved] | O | | | [Reserved] | 0x8102_303C [15:12] (0x8102_300C[8]=0) | - | 0x8002_511C [15:12] (0x8102_303C [15:12]=0, 0x8102_300C[8]=0) | 0 |
| | | | UART_DSN_TXD_N9 | O | | | UART DSN TX (N9) | | - | | 1 |
| | | | **SWD_DIO** | **I/O** | **I** | | CM4 debug port | | **6** | | 2 |
| | | | GPIO_TOPOFF[59] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[59] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[38] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | WF_LED_B | I/O | | | LED output | | 1 | | - |
| | | | WIC[10] | I | | | External interrupt | | 3 | | - |
| | | | ADC_IN2 | I | | | Auxiliary ADC input | 0x8102_300C[8] | 1 | | - |
| 44 | GPIO60 | AGPIO | [Reserved] | I | | | [Reserved] | 0x8102_303C [19:16]=0 (0x8102_300C[9]=0) | - | 0x8002_511C [19:16] (0x8102_303C [19:16]=0, 0x8102_300C[9]=0) | 0 |
| | | | **SWD_CLK** | **I** | **I** | | CM4 SWD debug port | | **6** | | 2 |
| | | | GPIO_TOPOFF[60] | I/O | | | General purpose input output | | - | | 5 |
| | | | GPIO_TOPAON[[60] | I/O | | | General purpose input output | | 8 | | - |
| | | | PWM[39] | O | | | Pulse-width-modulated output | | 9 | | - |
| | | | MISC_LED_B | I/O | | | LED output | | 1 | | - |
| | | | PULSE_CNT | I | | | Pulse counter input | | 2 | | - |
| | | | WIC[11] | I | | | External interrupt | | 3 | | - |
| | | | ADC_IN3 | I | | | Auxiliary ADC input | 0x8102_300C[9] | 1 | | - |

*Note: * not used in MT7687F*

## 5.4 Bootstrap

The section describes the bootstrap function.

The chip modes are sensed from the device pin during power up. After chip reset, the pull configuration are stored in a register and determine the device operation mode.

***Table 5-4. Bootstrap Option– Flash Access Mode***

| Flash Access Mode | PIN53 (GPIO37) | Description |
|---|---|---|
| Normal mode | Pull-down(1) | Firmware jumps to flash. |
| Recovery mode | Pull-up | Firmware does not jump to flash and wait for UART command. |
| | | This mode is used for the firmware to jump to SYSRAM after downloading code from UART. |

Note 1: No external pull-down resistor is required because internal pull-down is active during power up.

***Table 5-5. Bootstrap Option – XTAL Clock Mode***

| XTAL Clock Mode | PIN12 (GPIO7) | PIN52 (GPIO38) | Description |
|---|---|---|---|
| 40MHz | Pull-down | Pull-up | Uses 40MHz XTAL. |
| 26MHz | Pull-up | Pull-down(1) | Uses 26MHz XTAL. |
| 52MHz | Pull-up | Pull-up | Uses 52MHz XTAL. |

*Note 1: No external pull-down resistor is required because internal pull-down is active during power up.*

***Table 5-6. Bootstrap Option – 32KHz Clock Mode***

| 32KHz clock mode | PIN11 (GPIO6) | Description |
|---|---|---|
| Internal 32KHz clock | Pull-down | 32KHz clock sources from 40/26/52MHz clock. |
| External 32KHz clock | Pull-up | 32KHz clock sources from external pin. |

***Table 5-7. Bootstrap Option — Chip Mode***

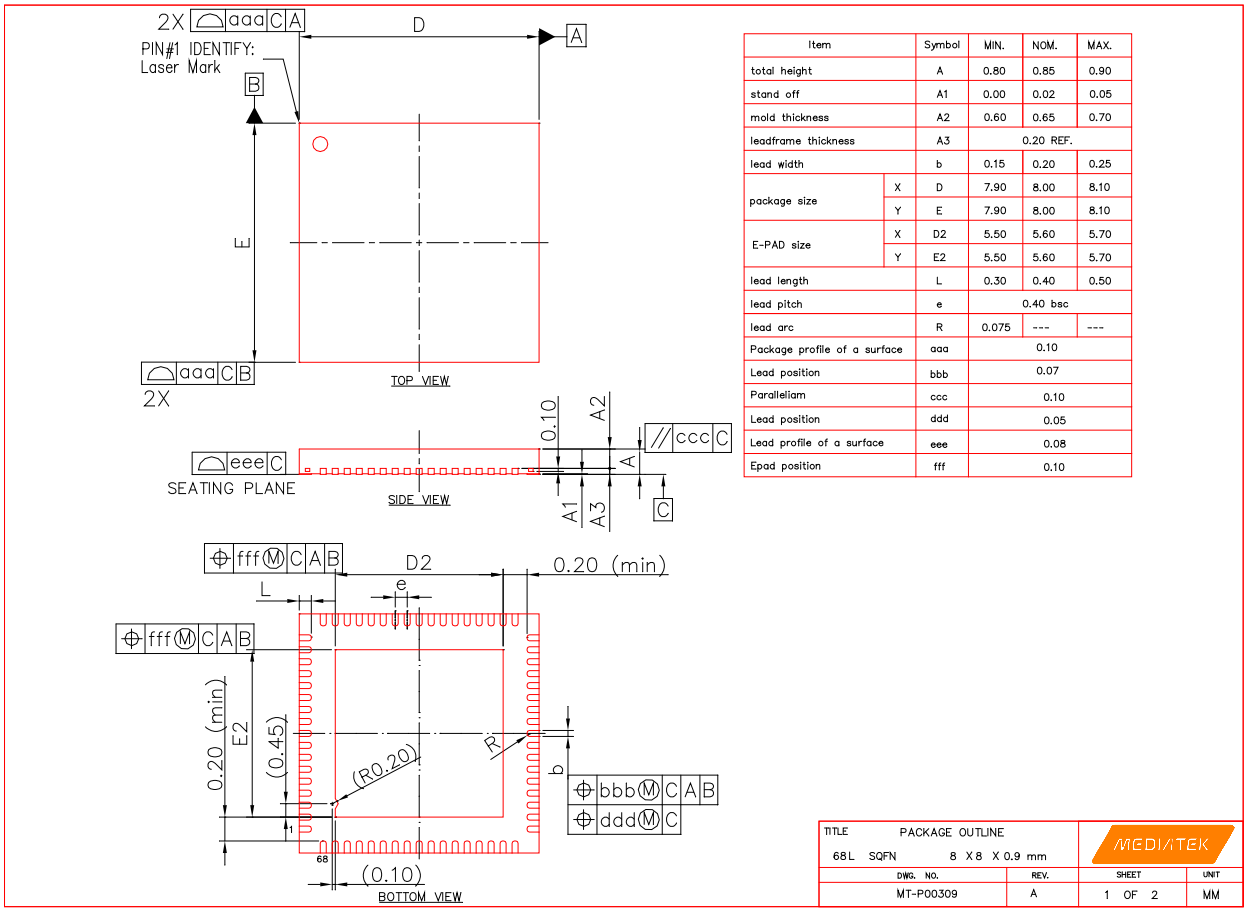
| Chip mode | PIN55 (GPIO35) | PIN10 (GPIO5) | PIN11 (GPIO6) | PIN12 (GPIO7) | PIN52 (GPIO38) | Description |
|---|---|---|---|---|---|---|
| Normal mode | Pull-down(1) | Don't care | 32KHz clock mode control | XTAL clock mode control | | Chip operates in normal mode. |
| Test mode | Pull-up | | | | | Chip operates in test mode. |

*Note 1: No external pull-down resistor is required because internal pull-down is active during power up.*

Pins 10, 11, 12, 52, 53, and 55 are is used for bootstrap. The system design should follow the following guideline:

- Those pins shall not be used as input functions because the signals from another device might affect the values sensed.

## 5.5 Package information




| Item | | Symbol | MIN. | NOM. | MAX. |
|---|---|---|---|---|---|
| total height | | A | 0.80 | 0.85 | 0.90 |
| stand off | | A1 | 0.00 | 0.02 | 0.05 |
| mold thickness | | A2 | 0.60 | 0.65 | 0.70 |
| leadframe thickness | | A3 | | 0.20 REF. | |
| lead width | | b | 0.15 | 0.20 | 0.25 |
| package size | X | D | 7.90 | 8.00 | 8.10 |
| | Y | E | 7.90 | 8.00 | 8.10 |
| E-PAD size | X | D2 | 5.50 | 5.60 | 5.70 |
| | Y | E2 | 5.50 | 5.60 | 5.70 |
| lead length | | L | 0.30 | 0.40 | 0.50 |
| lead pitch | | e | | 0.40 bsc | |
| lead arc | | R | 0.075 | --- | --- |
| Package profile of a surface | | aaa | | 0.10 | |
| Lead position | | bbb | | 0.07 | |
| Paralleliam | | ccc | | 0.10 | |
| Lead position | | ddd | | 0.05 | |
| Lead profile of a surface | | eee | | 0.08 | |
| Epad position | | fff | | 0.10 | |

| TITLE | PACKAGE OUTLINE | | |
|---|---|---|---|
| 68L SQFN 8 X 8 X 0.9 mm | | | |
| DWG. NO. | REV. | SHEET | UNIT |
| MT-P00309 | A | 1 OF 2 | MM |

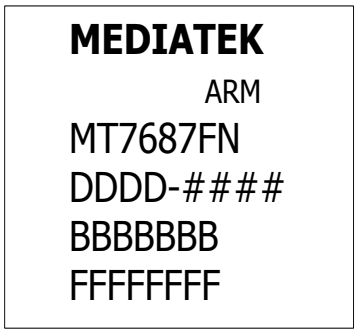
***Figure 5-1.* Package Outline Drawing**

## 5.6 Ordering information

***Table 5-8. Ordering Information***

| Part number | Package | Operational temperature range |
|---|---|---|
| MT7687FN | 8mm x 8mm x 0.8 mm QFN68 | -30~85°C |
| MT7687FIN | 8mm x 8mm x 0.8 mm QFN68 | -40~85°C |

## 5.7 Top Marking




```
MT7687FN: Part number
DDDD      : Date code
####      : Internal control code
BBBBBBB   : Main die lot number
FFFFFFF   : Flash die lot number
```

***Figure 5-2. Top Marking***