MT2511 Datasheet

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Release date: 5 May 2017

Document Revision History

Revision	Date	Description
0.1	06 October 2015	Initial draft
0.2	24 November 2015	Update ball diagram and detailed pin description
0.3	05 February 2016	Document format update
0.31	16 February 2016	Document format update
0.32	18 February 2016	Marking update
0.33	24 March 2016	TMODE is tied to ground. Correct package size. Figure refine. Remove duplicated chapter. Update Boost spec
0.34	31 March 2016	Rename package ball TXP-> TX1, TXN->TX2
0.45	29 August 2016	Remove Boost support Current consumption update.
0.46	11 January 2017	List MCU interface operation condition for low power simulation. Top marking description update.
1.0	5 May 2017	Official version.

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1. System Overview

MT2511 is a 2-in-1 bio-sensing analog front-end (AFE) to facilitate bio-signal acquisition. The AFE consists of low noise voltage and current sensing channels, and is capable of sensing EKG (Electrocardiography) and PPG (Photoplethysmography) simultaneously.

The two AFE channels in MT2511 have >100dB dynamic range and can sense pulses accurately by detecting the heart's electric signals with the presence of environment interferences and motion artifacts, and complements this method optically by illuminating the skin and measuring changes in light absorption.

MT2511 contains built-in heartbeat interval estimation for PPG signals and SRAM to optimize power consumption for sleep heart rate monitoring. This feature allows the external MCU to stay in idle mode up to four minutes when motion artifact cancellation is not required.

The sampling rates of the high-precision voltage and current sensing channels in MT2511 are configurable between 64-4kHz to support applications with other bio-signals, such as Electromyography (EMG), Electroencephalography (EEG), and Pulse oximetry (SpO2), and high-precision data acquisitions for different kinds of sensors, such as pressure and impedance sensors. With multiple MT2511s, a higher degree of sensor fusion can be achieved with synchronized data acquisition by triggering each MT2511 with the same external clock input. In addition, MT2511 integrates an oscillator to offer high-precision clock with external crystal.

With its tiny package (3.1mm x 3.4mm) and limited energy needs, MT2511 is suitable for various types of wearable devices, particularly fitness trackers, active lifestyle smart watches and sports bands. It is also suitable for next-generation health and wellness devices such as a smart medical patch and smart clothing for the emerging eldercare segment.

MT2511 is optimized for bio-sensing products with the following strengths:

- 2-in-1 bio-sensing AFE (Voltage/Current)
- Built-in beat interval detection circuit with SRAM can optimize power consumption for sleep heart rate monitoring
- Integrates an oscillator to offer high-precision clock with external crystal.
- Flexible timing control for dynamic power down for power saving.
- Two-electrode (2E) mode and right leg drive (RLD) mode for EKG monitoring.
- Ultra-low power consumption

EKG Channel

MT2511 integrates a high-resolution dc-coupled front end. It can endure wide input offset, large interference, and different electrode impedance. MT2511 is the first AFE supporting 2-electrode EKG monitoring with 500-MΩ input impedance. This facilitates the use of two dry electrodes to optimize product form factor, reduce electrode cost, and maintain good signal quality. MT2511 also supports conventional right-leg drive (RLD)

mode to reach medical-grade EKG acquisition. Note that there is larger interference at two-electrode (2E) mode.

PPG Channel

MT2511 comprises of LED drivers, a high-end dc-coupled current-mode front end, and a flexible timing control for PPG channel. The flexible timing control enable the users to control the device timing for different application and to power down the device for power saving. And the PPG front end can sense up to four channels (two for signal and two for ambient) by time multiplexing.

Heartbeat Interval Estimation

MT2511 contains built-in heartbeat interval estimation for PPG signals and SRAM to optimize power consumption for sleep heart rate monitoring. This feature allows the external MCU to stay in idle mode up to four minutes when motion artifact cancellation is not required.

Memory

MT2511 supports on-chip SRAM for data buffering. There are 1KB SRAM for EKG channel, 2KB SRAM for 2PPG channels, and 1KB SRAM for heartbeat internal detection channel. The SRAM buffering allows the MCU to stay in idle mode for power saving.

Connectivity

MT2511 supports I2C/SPI dual interface.

Package

The MT2511 device is offered in a 3.1mm×3.4mm, 41-ball, 0.4mm pitch, and WLCSP package.

1.1. MT2511 System Block Diagram

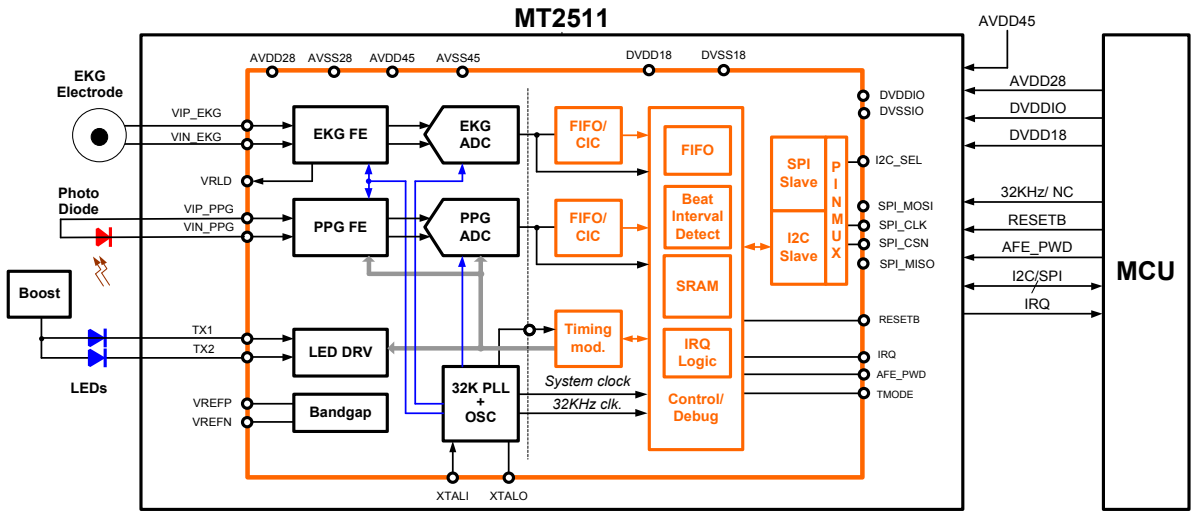


Figure 1. MT2511 System Block Diagram

1.2. EKG Channel Features

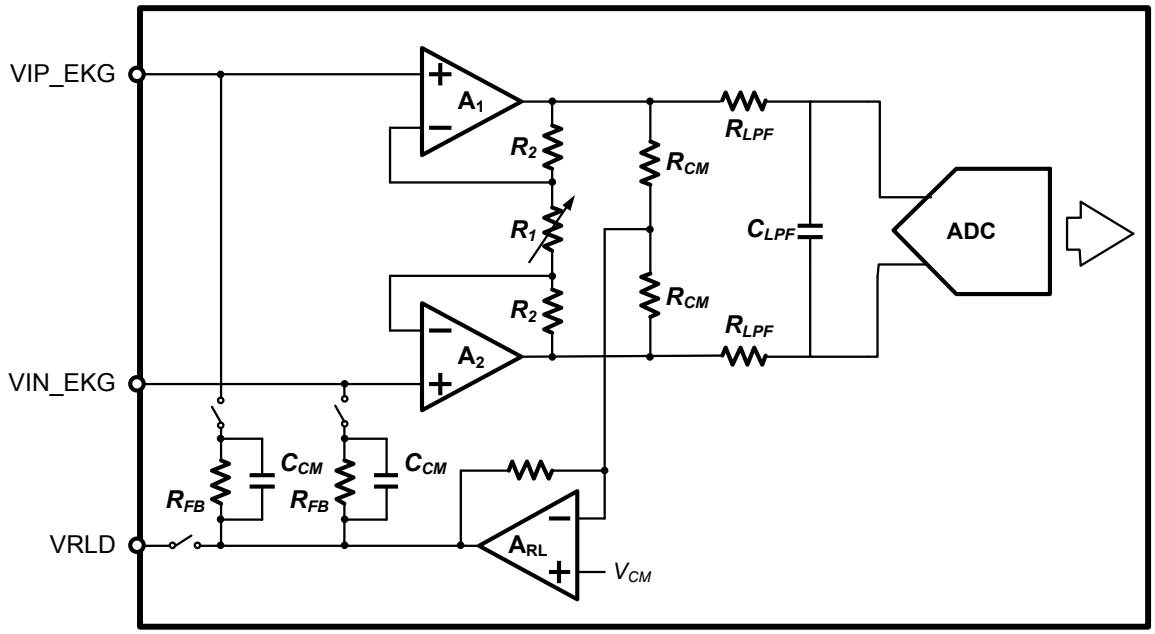


Figure 2. EKG Channel Block Diagram

Figure 2 above shows a DC-coupled EKG system. The EKG channel supports two-electrode (2E) mode and right leg drive (RLD) mode, and acts as a buffer between human and circuit. It integrates a programmable gain amplifier (PGA), a right leg drive amplifier, and a 24-bit sigma-delta analog-to-digital converter (ADC) to sense and digitize the EKG signal.

1.2.1. General Specifications

- Programmable gain from 1 to 12
- Low input-referred noise: 0.83uV$_{rms}$ at G=6 and BW=150Hz
- Dynamic range: 110 dB at G=6
- CMRR>85dB at 60Hz
- Data rate: 64SPS to 4096SPS
- Supports two-electrode and right leg drive mode
- Input impedance: 125M~500MΩ at two-electrode mode and >1GΩ at right leg drive mode

1.3. PPG Channel Features

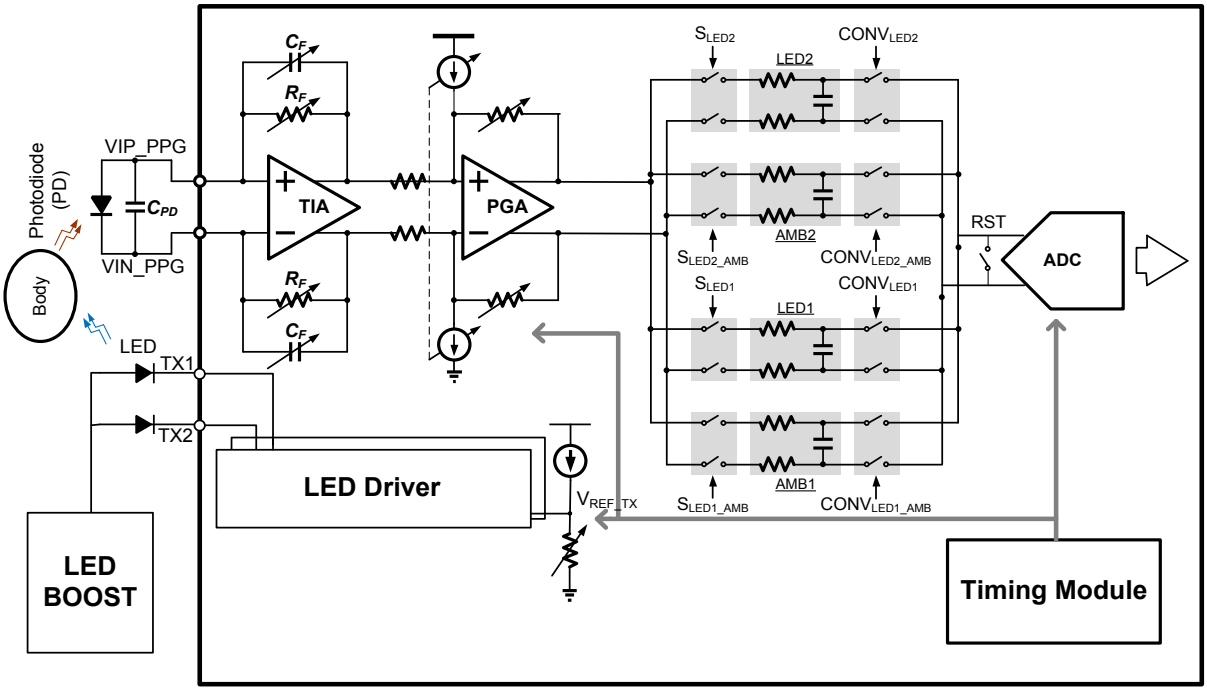


Figure 3. PPG Channel Block Diagram

The PPG channel is separated into two parts: Receiver (RX) and Transmitter (TX). The TX part consist of LED driver. The LED driver and the voltage boost are used to light up external LED and to provide the voltage drop of LED. The light emitted by LED is penetrated/reflected by the skin, and received by photodiode and the RX. The RX consists of a trans-impedance amplifier (TIA), a programmable gain amplifier (PGA), an ambient digital-to-analog converter (DAC), and a 24-bit incremental ADC. It amplifies and digitizes the received current.

1.3.1. General Specification

- Input maximum current range: 0.5-50 (μA)
- Input maximum capacitance: 1nF
- Input-referred noise: 52pA_{rms} at 5μA input current
- CMRR>80dB at 60Hz
- PGA gain: 1~6 V/V
- Ambient DAC1/2 range: 1~6 μA
- TX LED current range: 9.5/22.9/36.3/49.7/63.1/76.5/79.9/103.3mA, each with 8-bit current resolution
- TX supports H-bridge and push/ pull mode
- Loop back dynamic range: 100 dB at 5μA input current
- Flexible timing control and Support dynamic power down

1.4. Heartbeat Interval Estimation Feature

MT2511 has a built-in heartbeat interval (BI) detector to enhance heart rate monitoring application. When the signal quality of PPG is good enough, the BI detector is able to approximate wavelength of major tone. Instead of complete PPG signals, only beat time intervals are recorded in SRAM. The MCU is freed from estimating heart rate; as a result the amount of data read from MT2511 SRAM via I2C/SPI is reduced significantly.

2. Pin Description

2.1. Ball Diagram

For MT2511, a WLCSP 3.1mm*3.4mm, 41-ball, 0.4mm pitch package is offered. Pin-outs are illustrated in Figure 4 for this package.

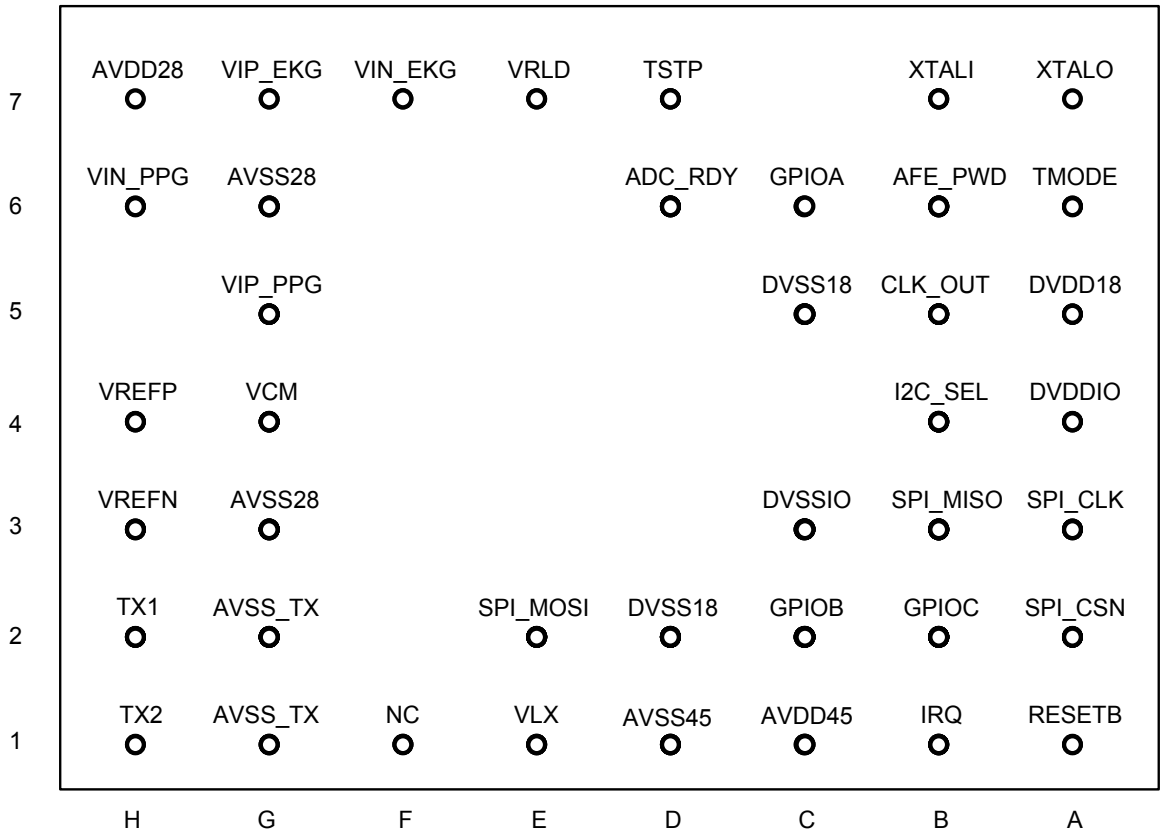


Figure 4. Ball Diagram and Top View

2.2. Pin Coordination

Table 1. Pin Coordinates

Pin#	Net name	Pin#	Net name	Pin#	Net name
A1	RESETB	C1	AVDD45	G1	AVSS_TX
A2	SPI_CSN=SDA	C2	GPIOB	G2	AVSS_TX
A3	SPI_CLK=SCL	C3	DVSSIO	G3	AVSS28
A4	DVDDIO	C5	DVSS18	G4	VCM
A5	DVDD18	C6	GPIOA	G5	VIP_PPG
A6	TMODE	D1	AVSS45	G6	AVSS28
A7	XTALO	D2	DVSS18	G7	VIP_EKG
B1	IRQ	D6	ADC_RDY	H1	TX2
B2	GPIOC	D7	TSTP	H2	TX1
B3	SPI_MISO	E1	VLX	H3	VREFN
B4	I2C_SEL	E2	SPI_MOSI	H4	VREFP
B5	CLK_OUT	E7	VRLD	H6	VIN_PPG
B6	AFE_PWD	F1	NC	H7	AVDD28
B7	XTALI	F7	VIN_EKG		

2.3. Detailed Pin Description

Table 2. Pin Type Acronyms

Abbreviation	Description
AI	Analog input
AO	Analog output
AIO	Analog bi-direction
DI	Digital input
DO	Digital output
DIO	Digital bi-direction
P	Power
G	Ground

Table 3. PIN Function Description and Power Domain

Pin Name	Type	Description	Power Domain
VIP_EKG	AI	EKG IA positive input	AVDD28
VIN_EKG	AI	EKG IA negative input	AVDD28
VRLD	AO	RLD output. (leave floating at 2E mode)	AVDD28
VIP_PPG	AI	PPG receiver input pin. Connected to photodiode anode.	AVDD28
VIN_PPG	AI	PPG receiver input pin. Connected to photodiode cathode.	AVDD28
VCM	AI	PPG input common mode voltage. (leave floating)	AVDD28
TX1	AO	LED driver output. Connected to LED.	AVDD45
TX2	AO	LED driver output. Connected to LED.	AVDD45
AVDD45	P	PPG LED driver power. 2.2uF decoupling capacitor to ground.	AVDD45
AVSS_TX	G	PPG LED driver ground. Connected to common board ground.	AVDD45
VLX	AI	PPG circuit bias	AVDD45
AVSS45	G	PPG LED driver ground. Connected to common board ground.	AVDD45
VREFP	AIO	Bandgap output voltage. 1uF decoupling capacitor to ground.	AVDD28
VREFN	AIO	Bandgap negative reference voltage. Connected to common board ground.	AVDD28
TSTP	AIO	For testing. (leave floating)	AVDD28
AVSS28	G	Analog ground. Connected to common board ground.	AVDD28
AVDD28	P	Analog supply. 2.2uF decoupling capacitor to ground.	AVDD28
DVSS18	G	Digital ground. Connected to common board ground.	DVDD18
DVDD18	P	Digital supply. 2.2uF decoupling capacitor to ground.	DVDD18

Pin Name	Type	Description	Power Domain
DVSSIO	G	Digital IO ground. Connected to common board ground.	DVDDIO
DVDDIO	P	Digital IO supply. 2.2uF decoupling capacitor to ground.	DVDDIO
XTALI	AIO	Crystal oscillator pins. Connect an external 32kHz crystal with 22pF decoupling capacitor. It can be connected to an external 32kHz clock source.	AVDD28
XTALO	AIO	Crystal oscillator pins. Connect an external 32kHz crystal with 22pF decoupling capacitor. If with external clock source, leave floating.	AVDD28
ADC_RDY	DIO	For testing. (leave floating)	DVDDIO
GPIO	DIO	For testing. (leave floating)	DVDDIO
AFE_PWD	DIO	Power down pin. Can be connected to an external MCU	DVDDIO
TMODE	DIO	Tied to ground.	DVDDIO
CLK_OUT	DIO	For testing. (leave floating)	DVDDIO
IRQ	DO	Interrupt pin. Can be connected to an external MCU.	DVDDIO
RESETB	DIO	Reset pin. Can be connected to an external MCU.	DVDDIO
I2C_SEL	DIO	(1)SPI mode -> please keep I2C_SEL Low (2)I2C mode -> please keep I2C_SEL High	DVDDIO
SPI_CLK	DIO	(1)SPI mode: SPI clock pin (SPI_CLK) (2)I2C mode: I2C clock pin (I2C_SCL)	DVDDIO
SPI_CSN	DIO	(1)SPI mode: SPI data pin (SPI_CSN) (2)I2C mode: I2C data pin (I2C_SDA)	DVDDIO
SPI_MISO	DIO	SPI serial out master in.	DVDDIO
SPI_MOSI	DIO	(1)SPI mode: SPI serial in master out. (2)I2C mode: I2C slave address (7-bit mode) (a)H=7-bit slave address (hex))=37 & 27 (b)L=7-bit slave address (hex))=33 & 23	DVDDIO
NC		Leave floating	

3. Electrical Characteristics

3.1. Absolute Maximum Ratings

Table 4. Power Supply Absolute Maximum Ratings

Symbol or Pin Name	Description	Min.	Max.	Unit
DVDDIO	Digital IO voltage input	-0.3	+4	V
DVDD18	Digital core circuit voltage input	-0.3	+4	V
AVDD28	Analog main voltage input	-0.3	+4	V
AVDD45	Analog secondary voltage input	-0.3	+4.5	V

Table 5. Voltage Input Absolute Maximum Ratings

Symbol or Pin Name	Description	Min.	Max.	Unit
V_{IN}	Input voltage	-0.3	+4	V
I_{IN}	DC input current at V_{IN} < 0V or V_{IN} > VDD	-20	+20	mA
I_{OUT}	DC output current at V_{OUT} < 0V or V_{OUT} > VDD	-20	+20	mA

Table 6. Storage Temperature Absolute Maximum Ratings

Symbol or Pin Name	Description	Min.	Max.	Unit
Tstg	Storage temperature range	-40	125	°C

3.2. Recommended Operating Conditions

Table 7. Recommended Operating Conditions for Power Supply

Symbol or Pin Name	Description	Min.	Typ.	Max.	Unit
DVDDIO	Digital IO voltage input	1.62	2.8	3.3	V
DVDD18	Digital core circuit voltage input	1.62	1.8	1.98	V
AVDD28 *(1)	Analog main voltage input	2.66	2.8	2.94	V
AVDD45	Analog secondary voltage input	3.4	4	4.5	V

*(1) Please refer to Table 14 for AVDD28 power noise requirement.

Table 8. Recommended Operating Conditions for Operating Temperature

Symbol or Pin Name	Description	Min.	Typ.	Max.	Unit
Tc	Operating temperature range	-20	-	65	°C

3.3. EKG Electrical Characteristics

Table 9. EKG Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
EKG ANALOG INPUTS						
	Full-scale differential input voltage			±1.9/GAIN		V
	Input capacitance	RLD mode		30		pF
		Two-electrode mode		190		pF
	DC input impedance	RLD mode	1000			MΩ
		Two-electrode mode		500		MΩ
EKG IA PERFORMANCE						
	Gain settings		1, 2, 3, 4, 6, 8, 12			V/V
	Bandwidth		See Table 10			
EKG LOW-PASS FILTER						
	Low-pass corner frequency	3-dB attenuation	28, 112			kHz
EKG ADC PERFORMANCE						
	Resolution				23	Bits
	Data rate		64		4096	SPS
EKG CHANNEL PERFORMANCE						
	Input-referred noise	Gain=6, 10 seconds of data		5.25		μV_{PP}
		Gain settings other than 6, data rates other than 500SPS	See Table 11			
	Common-mode rejection	f_{CM}=50Hz, 60Hz		85		dB
	Power-supply rejection	f_{PS}=50Hz, 60Hz	100			dB
THD	Total harmonic distortion	100Hz, -0.5dBFs		78		dB
		100Hz, -20dBFs		105		dB

Table 10. IA Gain versus Bandwidth

GAIN	Bandwidth of IA(kHz)

GAIN	Bandwidth of IA(kHz)
1	680
2	250
3	135
4	100
6	65
8	50
12	34

Table 11. Input-Referred Noise (uVrms/uVpp) vs Data Rate and PGA Gain

Output data rate (SPS)	BW (Hz)	PGA G=1	PGA G=2	PGA G=3	PGA G=4	PGA G=6	PGA G=8	PGA G=12
4096	2048	15.2/91.55	6.34/30.52	3.51/20.35	3.13/15.26	2.64/15.26	2.05/11.44	1.69/10.17
2048	1024	7.24/45.78	3.35/19.07	2.4/15.25	1.8/11.44	1.49/8.9	1.3/8.58	1.15/9.63
1024	512	4.61/28.6	2.44/15.26	1.74/11.44	1.4/9.54	1.14/8.27	0.96/7.15	0.93/6.2
512	256	3.49/21.45	1.69/11.2	1.12/7.31	0.98/7.39	0.81/5.96	0.78/5.66	0.71/4.61
256	128	3.66/23.37	1.91/11.92	1.37/8.9	1.05/7.39	0.83/5.25	0.69/4.53	0.73/4.85
128	64	3.5/22.89	1.83/11.68	1.32/8.11	0.99/6.32	0.83/5.16	0.82/4.83	0.6/3.93
64	32	3.47/20.03	1.85/11.92	1.27/7.47	1.02/6.44	0.82/5.25	0.7/4.53	0.67/4.45

3.4. PPG Electrical Characteristics

Table 12. PPG Electrical Characteristics

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PPG Full-Signal Chain						
I_{IN_FS}	Full-scale input current	R_F=10KΩ		50		µA
		R_F=25KΩ		20		µA
		R_F=50KΩ		10		µA
		R_F=100KΩ		5		µA
		R_F=250KΩ		2		µA
		R_F=500KΩ		1		µA
		R_F=1MΩ		0.5		µA
PRF	Pulse repetition frequency		64		4096	SPS
DC_{PRF}	PRF duty cycle				25%	
CMRR	Common-mode rejection ratio	f_{CM}=50Hz and 60Hz, R_{SERIES}=100KΩ, R_F=100KΩ		80		dB
PSRR	Power-supply rejection ratio	f_{CM} =50Hz,60Hz at PRF=125Hz	80			dB
	Total integrated noise current, input referred (receiver with transmitter loop back, 0.1Hz to 20Hz bandwidth)	R_F=100KΩ with stage2 gain=1.5, PRF=1300Hz, duty cycle=5%		52		pA_{RMS}
		R_F=500KΩ with ambient cancellation enabled and stage2 gain=6, PRF=1300Hz, duty cycle=25%		7.2		pA_{RMS}
PPG RECEIVER FUNCTIONAL BLOCK LEVEL SPECIFICATION						
	Total integrated noise current, input referred (receiver alone) over 0.1Hz to 5Hz bandwidth	R_F=500KΩ, ambient cancellation enabled, stage2 gain=6, PRF=1300Hz, LED duty cycle=25%		1.25		pA_{RMS}
		R_F=500KΩ, ambient cancellation enabled, stage2 gain=6, PRF=1300Hz, LED duty cycle=5%		3.85		pA_{RMS}

Table 13. PPG Electrical Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
PPG I-V TRANSIMPEDANCE AMPLIFIER						
G	Gain	R_F=10KΩ to 1MΩ				
	Feedback resistance	R_F	10k, 25k, 50k, 100k, 250k, 500k, and 1M			Ω
	Feedback capacitance	C_F	5, 10, 25, 50, 100, and 250			pF
	Common-mode voltage on input pins	Set internally		1.25		V
	External differential input capacitance	Include equivalent capacitance of photodiode, cables, EMI filter, and so forth			1000	pF
PPG AMBIENT CANCELLATION STAGE						
G	Gain		1, 1.5, 2, 3, 4, 6			V/V
	Current range		1		6	µA
	Current DAC step size			1		µA
PPG LOW-PASS FILTER						
	Low-pass corner frequency	3-dB attenuation	0.5, 1, 2, and 4			kHz
PPG ANALOG-TO-DIGITAL CONVERTER						
	Resolution		16			Bits
	Sample rate			4xPRF		SPS
	ADC full-scale voltage			±1.6		V
	ADC conversion time		60			µs
	ADC reset time		0.95			µs
PPG TRANSMITTER						
	Output current range		9.5, 22.9, 36.3, 49.7, 63.1, 76.5, 89.9, and 103.3			mA
	Output current accuracy		±10%			
	Output current resolution			8		Bits
	Minimum sample time of LED1 and LED2 pulses			50		µs

3.5. System Electrical Characteristics

Table 14. System Electrical Characteristics

PARAMETER	MIN	TYP	MAX	UNIT

PARAMETER		MIN	TYP	MAX	UNIT
AVDD28	noise requirement, BW = 10 Hz to 100 kHz			90	μV_{RMS}
Clock					
	External clock DC range	0		2.8	V
	External clock voltage	400			mVpp
	External clock frequency		32k		Hz
	Frequency shift		±100		ppm
	Phase noise		-100		dBc/Hz
VIH	Input logic low voltage	0.65*VDD		VDD+0.3	V
VIL	Input logic high voltage	-0.3		0.35*VDD	V
VOH(DC)	DC Output logic low voltage	0.75*VDD			V
VOL(DC)	DC Output logic high voltage			0.25*VDD	V

4. Low Power Performance

4.1. Operating Scenarios and Current Consumption

Table 15 below summarizes the operating scenarios and gives the current consumption. Note the current measurement condition is under the typical condition of process, voltage, and temperature. The MCU interface used in measurement is 200 KHz I2C.

Table 15. Operating Scenarios and Current Consumption

	AVDD28	DVDD18	DVDDIO	AVDD45
Mode	2.8	1.8	2.8	4
IDLE	3.5	< 1	< 1	1.5
EKG	367	200	7.5	1.5
PPG *(1)	225	200	4	5
PPG1+BI	225	240	5	5
PPG1+PPG2	225	225	6	5
EKG+PPG1 *(2)	545	230	6	5
	uA	uA	uA	uA

*(1) When MCU read PPG 125Hz sampling rate data.
*(2) When MCU read PPG 512Hz and EKG 512Hz sampling rate data.
DVDDIO consumption depends on different I2C/SPI speed and data sample rates.

5. Functional Overview

5.1. SPI/I2C Specification

5.1.1. SPI/I2C Supply Voltage

Table 16. SPI/I2C Specification

I2C interface			
Pin name	**Type**	**Description**	**Power domain**
I2C_SEL	DIO	(1)SPI mode -> please keep I2C_SEL Low (2)I2C mode -> please keep I2C_SEL High	DVDDIO
SPI_CLK	DIO	(1)SPI mode: SPI clock pin (SPI_CLK) (2)I2C mode: I2C clock pin (I2C_SCL)	DVDDIO
SPI_CSN	DIO	(1)SPI mode: SPI data pin (SPI_CSN) (2)I2C mode: I2C data pin (I2C_SDA)	DVDDIO
SPI_MISO	DIO	SPI serial out master in.	DVDDIO
SPI_MOSI	DIO	(1)SPI mode: SPI serial in master out. (2)I2C mode: I2C slave address (a)H=7-bit slave address (hex))=37 & 27 (b)L=7-bit slave address (hex))=33 & 23	DVDDIO

Digital Input/ Output						
PARAMETER	**DESCRIPTION**	**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
VIH	Input logic low voltage		0.65*VDD		VDD+0.3	V
VIL	Input logic high voltage		-0.3		0.35*VDD	V
VOH(DC)	DC Output logic low voltage		0.75*VDD			V
VOL(DC)	DC Output logic high voltage				0.25*VDD	V

5.2. Access Speed of SPI/I2C

The maximum SPI Clock is designed to operate at a frequency of 2MHz.

The maximum I2C Clock depends on board-level parameters such as trace latency. Typically, the maximum speed is 400K Hz.

Actual operating clock frequency may depending on board level condition, like trace length and total loading,

Either MT2511 I2C or MT2511 SPI does not support burst access.

5.3. Power Sequence

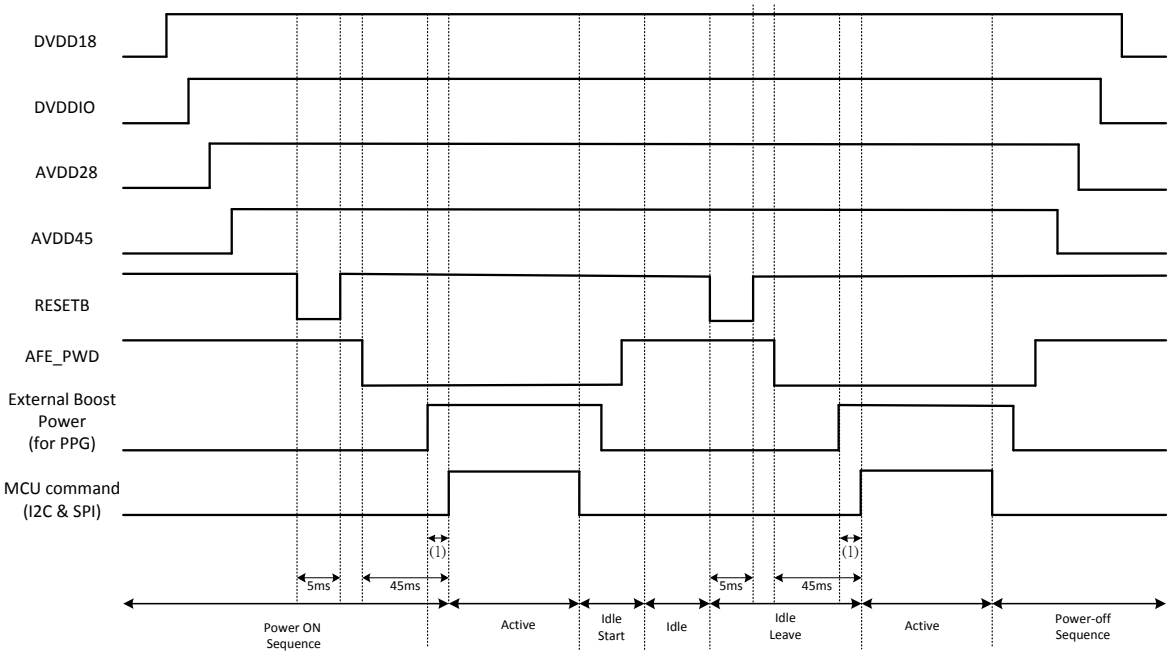


Figure 5. MT2511 Power-on, Idle and Power-off Sequence.

(1) Depend on external boost settling time

5.4. Timing Module Operation

5.4.1. General Operation

- The data of LED and ambient (AMB) are stored at the low pass filter (LPF) separately and then digitized by 24-bit incremental ADC
- Flexible timing module: PRF: 64~4096 SPS, duty: 1~25%

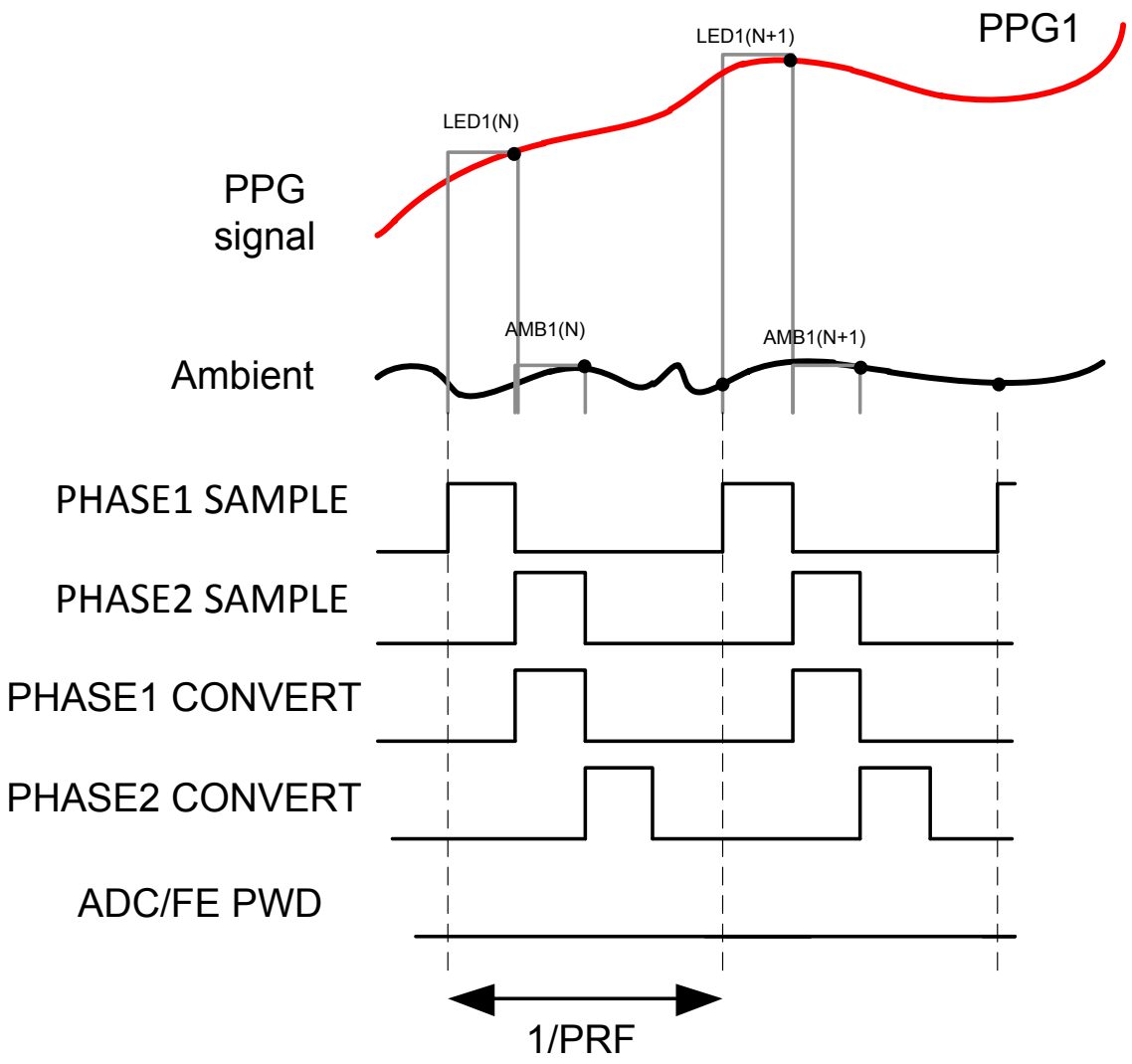


Figure 6. Timing Module General Operation

5.4.2. Dynamic Power Down Mode

- The flexible timing control enables the users to control the device timing for different applications and to power down the device for power saving.

- I_{RX+TX}=480µA → 100µA at PRF=125 and duty=1.5%

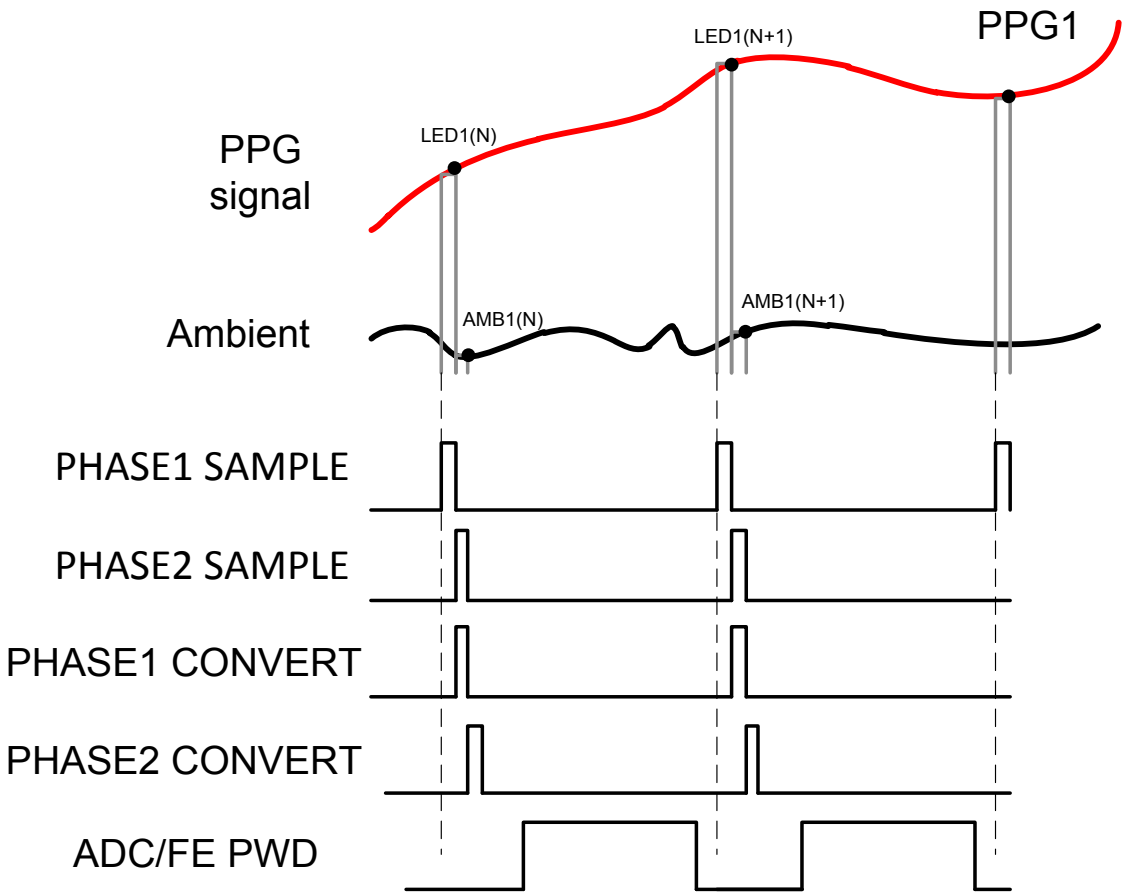


Figure 7. Dynamic Power Down Mode

5.4.3. Timing Module Operation

The rising and falling edge position of below 14 signals can be set separately. The graphic below provides some timing examples.

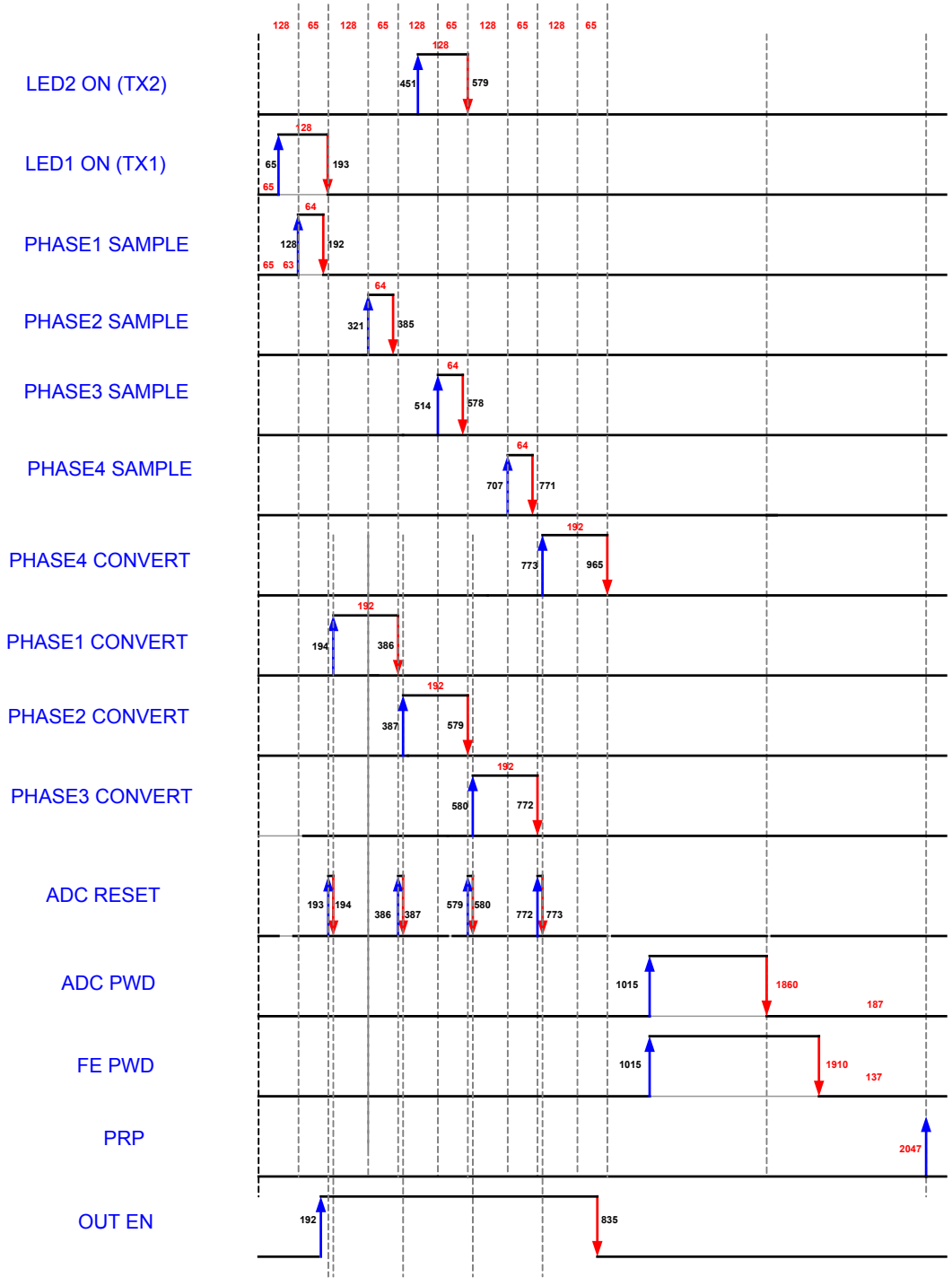
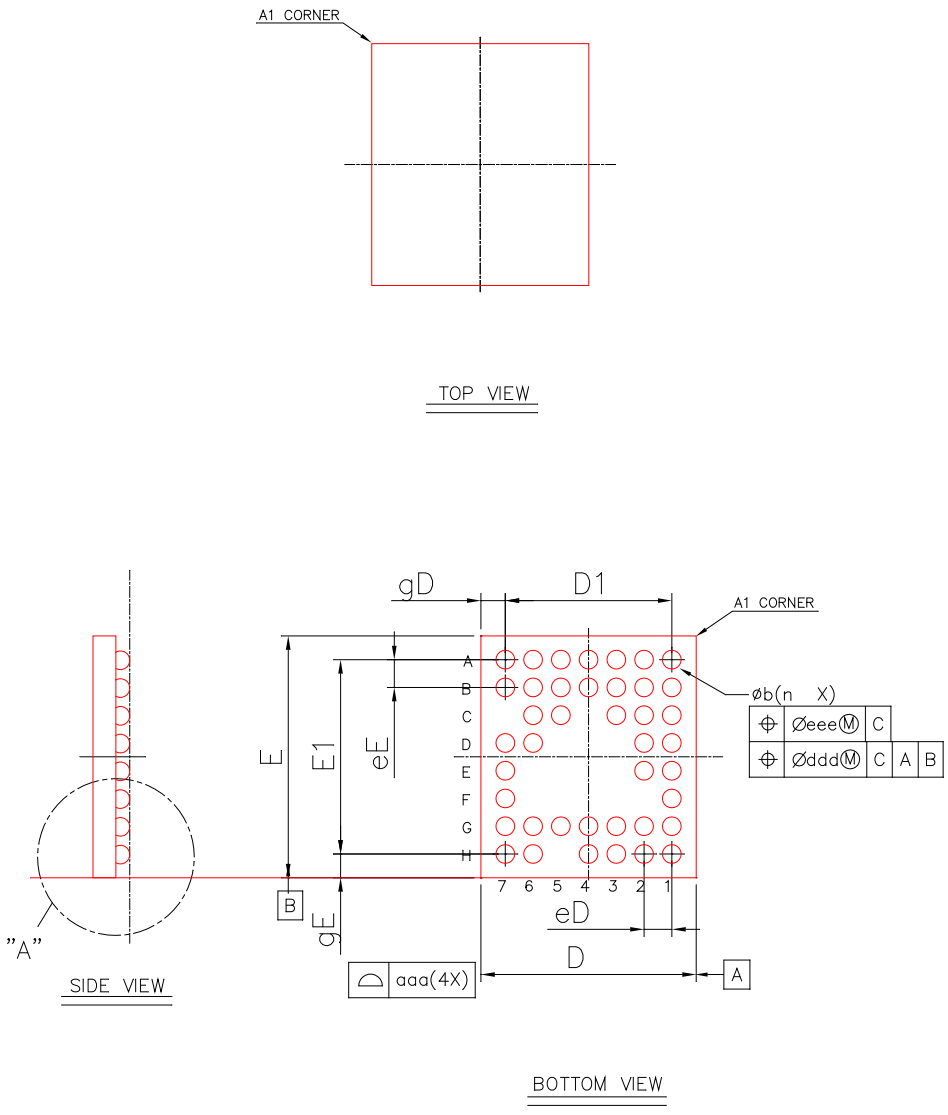
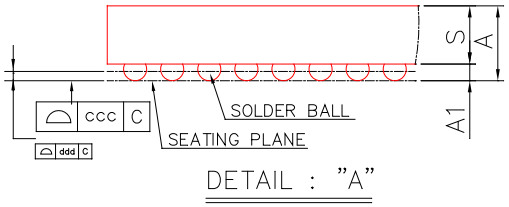


Figure 8. Timing Module Operation Example

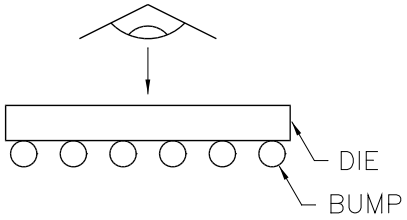
6. Package Information

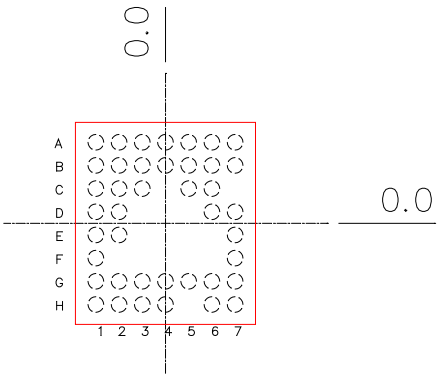
6.1. Package Mechanical Data





DETAIL : "A"





TOP VIEW

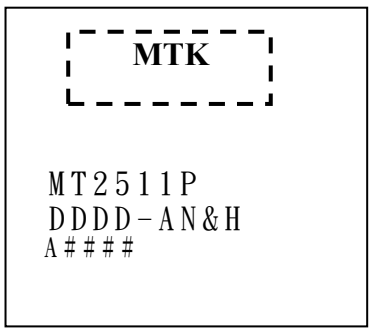
Ball	Location X(mm)	Location Y(mm)	Ball	Location X(mm)	Location Y(mm)	Ball	Location X(mm)	Location Y(mm)
A1	-1.200	1.400	H2	-0.800	-1.400	A6	0.800	1.400
B1	-1.200	1.000	A3	-0.400	1.400	B6	0.800	1.000
C1	-1.200	0.600	B3	-0.400	1.000	C6	0.800	0.600
D1	-1.200	0.200	C3	-0.400	0.600	D6	0.800	0.200
E1	-1.200	-0.200	G3	-0.400	-1.000	G6	0.800	-1.000
F1	-1.200	-0.600	H3	-0.400	-1.400	H6	0.800	-1.400
G1	-1.200	-1.000	A4	0.000	1.400	A7	1.200	1.400
H1	-1.200	-1.400	B4	0.000	1.000	B7	1.200	1.000
A2	-0.800	1.400	G4	0.000	-1.000	D7	1.200	0.200
B2	-0.800	1.000	H4	0.000	-1.400	E7	1.200	-0.200
C2	-0.800	0.600	A5	0.400	1.400	F7	1.200	-0.600
D2	-0.800	0.200	B5	0.400	1.000	G7	1.200	-1.000
E2	-0.800	-0.200	C5	0.400	0.600	H7	1.200	-1.400
G2	-0.800	-1.000	G5	0.400	-1.000			

Item		Symbol	Common Dimensions		
			MIN.	NOM.	MAX
Package Type			WLCSP		
Body Size	X	D	3.048	3.103	3.128
	Y	E	3.431	3.486	3.511
Ball Pitch	X	eD		0.400	
	Y	eE		0.400	
Total Thickness		A	0.49	0.53	0.57
Back Side Coating		A2		---	
Wafer Thickness		S	0.305	0.330	0.355
Ball Diameter				0.250	
Stand Off		A1	0.17	0.20	0.23
Ball Width		b	0.24	0.27	0.30
Package Edge Tolerance		aaa		+0.025 -0.055	
Coplanarity		ccc		0.030	
Ball Offset (Package)		ddd		0.050	
Ball Offset (Ball)		eee		0.015	
Ball Count		n		41	
Edge Ball Center to Center	X	D1		2.400	
	Y	E1		2.800	
Edge Ball Center to Package Edge	X	gD		0.344	
	Y	gE		0.335	

Figure 9. Outlines and Dimension of MT2511 WLCSP 3.1 mm * 3.4 mm, 41-ball, 0.4 mm Pitch Package

7. Ordering Information

7.1. MT2511 Top Marking Definition



Logo format: Refer 11.
PART NO.
&: Subcontractor code
DDDD: DATE CODE
####: U1 LOT NO.

Figure 10.MT2511 Mass Production Top Marking

Table 17. Ordering information

Product number	Package	Description
MT2511	WLCSP	3.1mm*3.4mm, 41-ball, 0.4mm pitch WLCSP Package