Course No.: CS224
Lab No.: 6
Section No.: 3
Ghulam Ahmed
22101001

Bilkent University
Computer Engineering
CS 224

Design Report

Lab # 6

Section # 3

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Question 1)

No.	Cache Size KB	N way cache	Word Size	Block size (no. of words)	No. of Sets	Tag Size in bits	Index Size (Set No.) in bits	Word Block Offset Size in bits	Byte Offset Size in bits	Block Replacement Policy Needed (Yes/No)
1	64	1	32 bits	4	2^{12}	16	12	2	2	No
2	64	2	32 bits	4	2^{11}	17	11	2	2	Yes
3	64	4	32 bits	8	2^{9}	18	9	3	2	Yes
4	64	Full	32 bits	8	2^{0}	27	0	3	2	Yes
9	128	1	16 bits	4	2^{13}	16	13	2	1	No
10	128	2	16 bits	4	2^{12}	17	12	2	1	Yes
11	128	4	16 bits	16	2^{11}	18	11	4	1	Yes
12	128	Full	16 bits	16	2^{0}	27	0	4	1	Yes

Question 2)

a)

Instruction	Iteration No.				
	1	2	3	4	5
lw $t1, 0x4($0)	Compulsory				
lw $t2, 0xC($0)	Compulsory				
lw $t3, 0x8($0)					

b)

- 1 block has 2 * 32 data segments
- 1 block has 27 tag segments
- 1 valid bit
- 4 blocks
- Total cache memory size = (32 * 2 * 4) + (27 * 4) + (1 * 4) = 368 bits

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c)

- 1 x AND gate
- 0 x OR gate
- 1 x Equality comparator
- 1 x 2-1 MUX

Question 3)

a)

Instruction	Iteration No.				
	1	2	3	4	5
lw $t1, 0x4($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t2, 0xC($0)	Compulsory	Capacity	Capacity	Capacity	Capacity
lw $t3, 0x8($0)	Capacity	Capacity	Capacity	Capacity	Capacity

b)

- 1 block has 32 data segments
- 1 block has 30 tag segments
- 1 valid bit
- 1 LRU bit
- 2 blocks
- Total cache memory size = (32 * 2) + (30 * 2) + (2 * 2) = 128 bits

c)

- 2 x AND gate
- 1 x OR gate
- 2 x Equality comparator
- 1 x 2-1 MUX

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4)

Access times:

- L1: 1 clock cycle
- L2: 4 clock cycles
- Main memory: 40 clock cycles

AMAT = 1 + 0.2(4 + 0.05(40)) = 2.2 clock cycles

Clock rate = 4 GHz

Total execution time = $4 * 2.2 * 10^{12} * 10^{-9} = 8.8 * 10^{3}$ seconds