Ryerson University

Department of Electrical & Computer Engineering
Faculty of Engineering & Architectural Science

Course Title:	Electronic Circuit I
Course Number:	ELE404
Semester/Year (e.g. F2017)	W2024

Instructor	Dr. Fei Yuan

Assignment/Lab Number:	
Assignment/Lab Title:	Design Project

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*By signing above you attest that you have contributed to this written lab report and confirm that all work you have contributed to this lab report is your own work. Any suspicion of copying or plagiarism in this work will result in an investigation of Academic Misconduct and may result in a "0" on the work, an "F" in the course, or possibly more severe penalties, as well as a Disciplinary Notice on your academic record under the Student Code of Academic Conduct, which can be found online at: http://www.ryerson.ca/senate/current/pol60.pdf

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I: Introduction

II: Objective

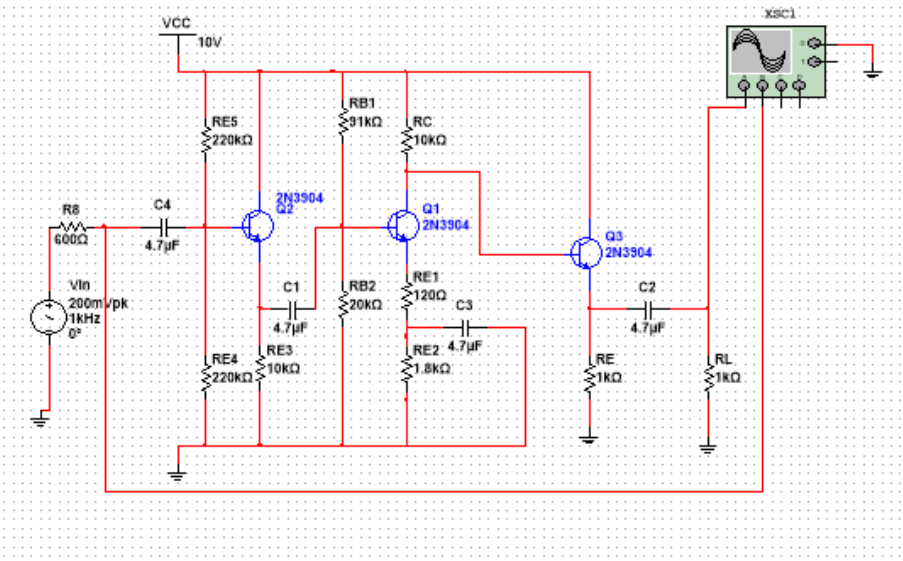
Specifications

- Power supply: $+\mathbf{10}\boldsymbol{V}$ relative to the ground;
- Quiescent current drawn from the power supply: ***no larger than*** $\mathbf{10}\ \boldsymbol{mA}$***;***
- No-load voltage gain (at 1 kHz): $|\boldsymbol{A_{vo}}| = \mathbf{50}\ (\pm\ \mathbf{10}\%)$**;**
- Maximum no-load output voltage swing (at 1 kHz): ***no smaller than 8 V peak to peak;***
- Loaded voltage gain (at 1 kHz and with $R_L = 1\ k\Omega$): ***no smaller than*** $\mathbf{90}\%$ ***of the no-load voltage gain;***
- Maximum loaded output voltage swing (at 1 kHz and $R_L = 1\ k\Omega$): ***no smaller than 4 V peak to peak;***
- Input resistance (at 1 kHz): ***no smaller than*** $\mathbf{20}\ \boldsymbol{k\Omega}$;
- Amplifier type: ***inverting or non-inverting;***
- Frequency response: ***20 Hz to 50 kHz (*** $-3dB$ ***response);***
- Type of transistors: ***BJT;***
- Number of transistors (stages): ***no more than 3***;
- Resistances permitted: ***values smaller than*** $\mathbf{220}\ \boldsymbol{k\Omega}$ ***from the E24 series***;
- Capacitors permitted: $\mathbf{0.1}\ \boldsymbol{\mu F}$, $\mathbf{1.0}\ \boldsymbol{\mu F}$, $\mathbf{2.2}\ \boldsymbol{\mu F}$, $\mathbf{4.7}\ \boldsymbol{\mu F}$, $\mathbf{10}\ \boldsymbol{\mu F}$, $\mathbf{47}\ \boldsymbol{\mu F}$, $\mathbf{100}\ \boldsymbol{\mu F}$, $\mathbf{220}\ \boldsymbol{\mu F}$***;***
- Other components (BJTs, diodes, Zener diodes, etc.): ***only from your ELE404 lab kit.***

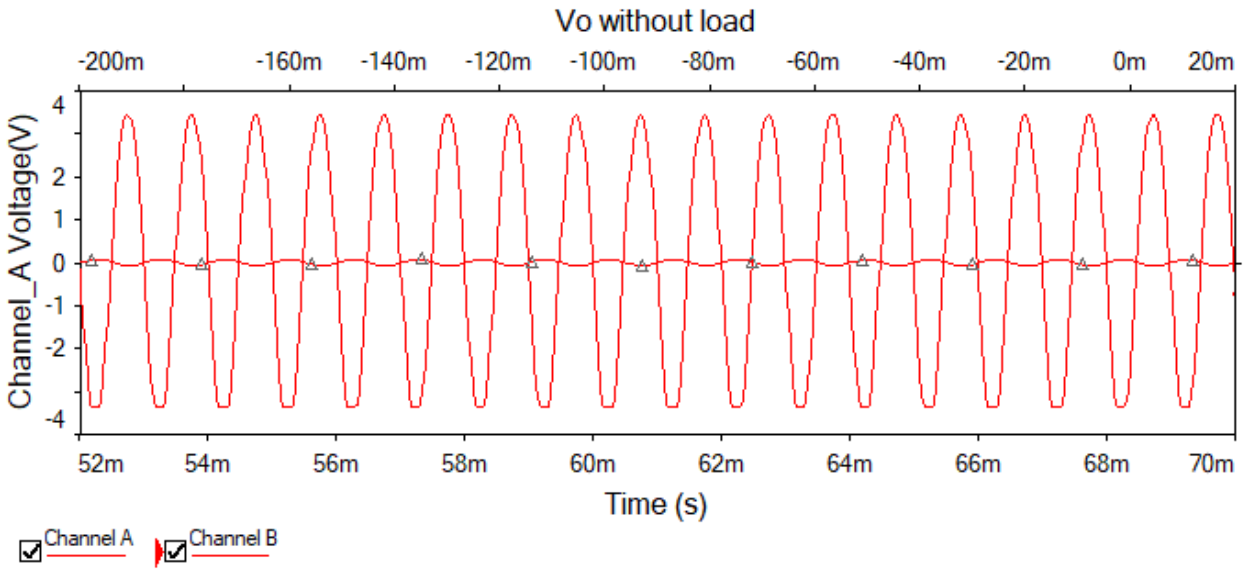
III: Circuit

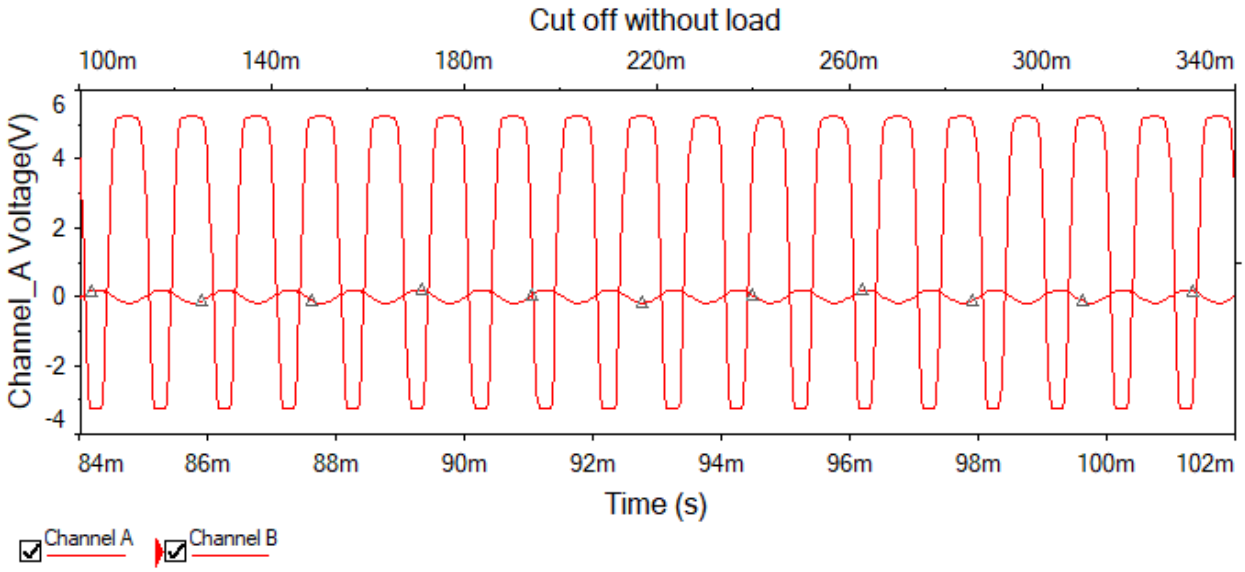
According to the specifications, I have made a circuit with approximately 50 volts again. I utilized the CC-CE-CC configuration to design the circuit.

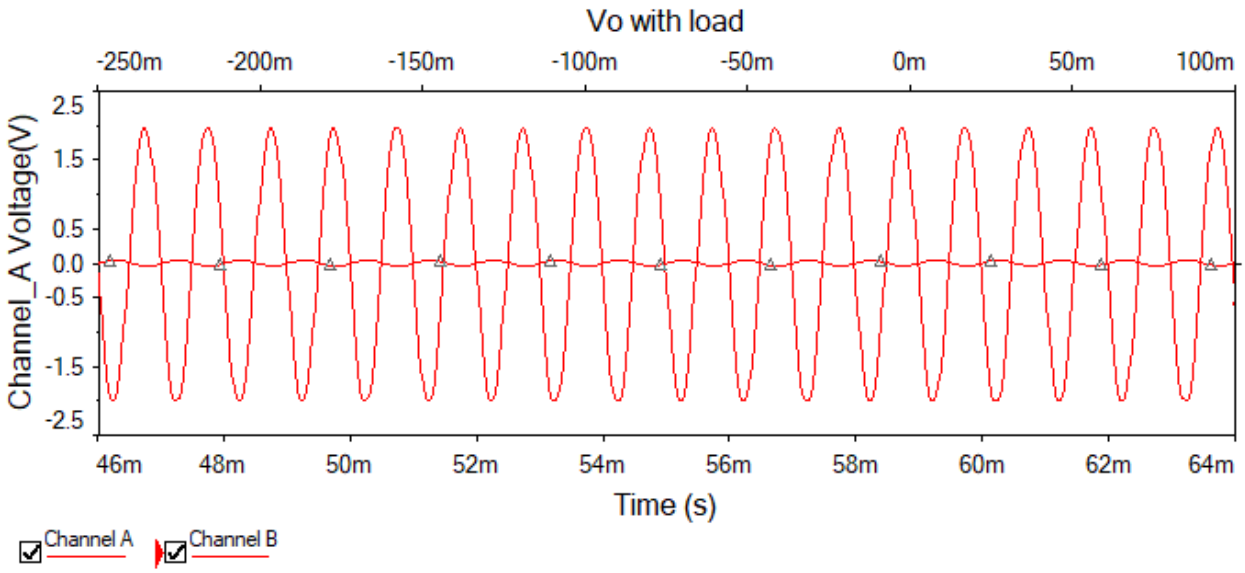
1. The first stage employs a CC amplifier configuration to increase the input resistance to above 20k ohms.
2. The second stage utilizes a CE amplifier configuration to amplify the input signal by 50 times (Av no load = 50).
3. The third stage adopts a CC configuration to stabilize the load at 1K, ensuring that the voltage gain does not drop below 90% of the no-load voltage gain (~45).

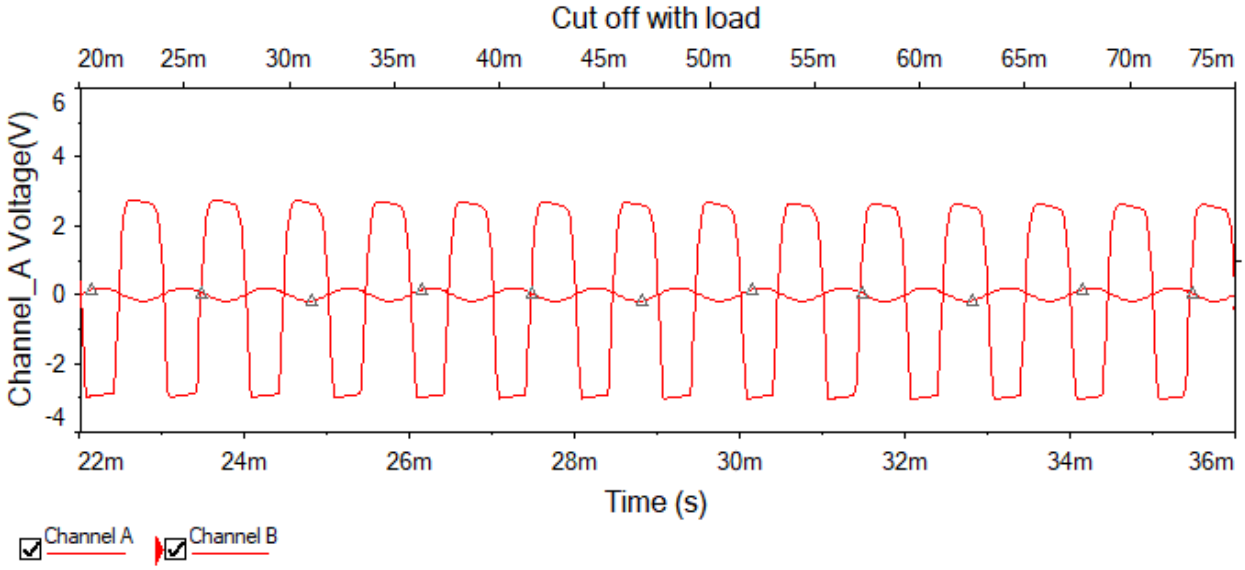


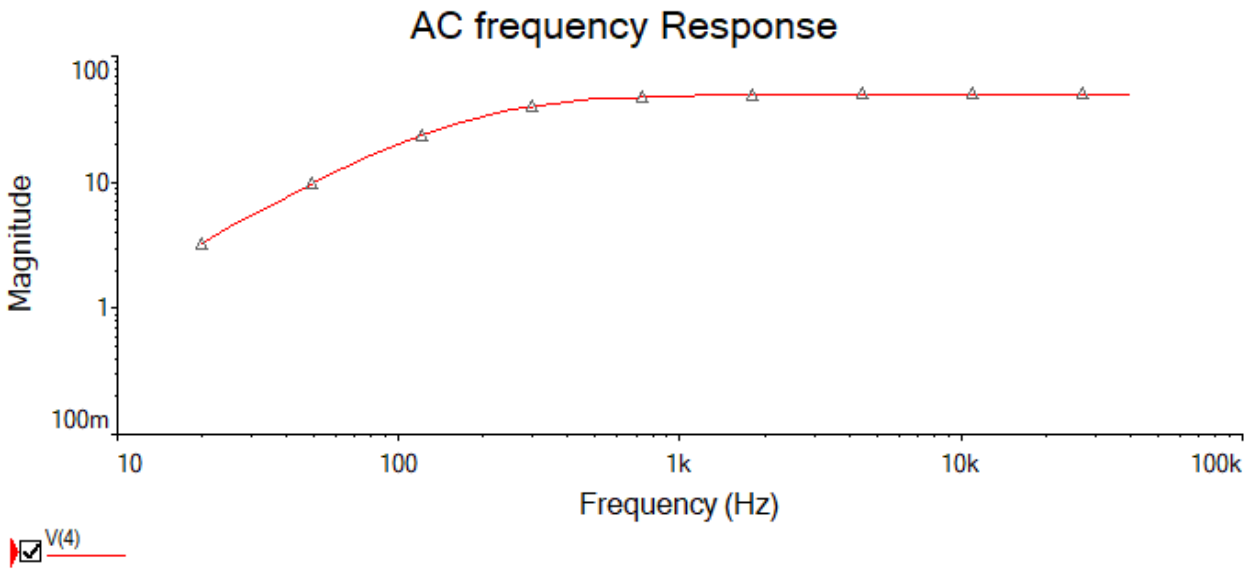
IV: Experimental Results


Vo without load
-200m
-160m
-140m
-120m
-100m
-80m
-60m
-40m
-20m
0m
20m
Channel_A Voltage(V)
4
2
1
0
-1
-2
-4
52m
54m
56m
58m
60m
62m
64m
66m
68m
70m
Time (s)
Channel A
Channel B


Cut off without load
100m
140m
180m
220m
260m
300m
340m
Channel_A Voltage(V)
6
4
2
0
-2
-4
84m
86m
88m
90m
92m
94m
96m
98m
100m
102m
Time (s)
Channel A
Channel B


Vo with load
-250m
-200m
-150m
-100m
-50m
0m
50m
100m
2.5
1.5
0.5
0.0
-0.5
-1.5
-2.5
Channel_A Voltage(V)
46m
48m
50m
52m
54m
56m
58m
60m
62m
64m
Time (s)
Channel A
Channel B


Cut off with load
20m
25m
30m
35m
40m
45m
50m
55m
60m
65m
70m
75m
6
4
2
0
-2
-4
Channel_A Voltage(V)
22m
24m
26m
28m
30m
32m
34m
36m
Time (s)
Channel A
Channel B



V: Explanation

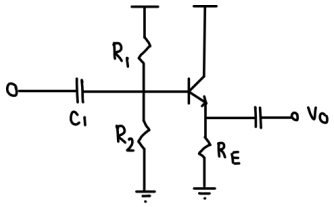
When testing the circuit without any load, I applied an 80mV input signal and observed a voltage gain of approximately 50. However, when a load was introduced, the voltage gain dropped to around 40 under the same conditions.

Considering the operational limits, the circuit has a maximum swing of 10 volts peak-to-peak (Vpp) without load, restricting it to a range between +5V and -5V. With a load, the maximum swing reduces to 6 volts peak-to-peak, limiting it between +3V and -3V.

Examining its frequency response, the circuit achieves its maximum gain starting from 1k ohms onwards up to 50kHz. Additionally, the lower cutoff frequency is approximately 100Hz, indicating its operational range in terms of frequency. These observations provide insights into the performance and limitations of the circuit across different conditions and frequencies.

VI: Manual Calculation

First stage: CC amplifier



CC theovitically has $A_V = 1$ => Can be used to increase input impendence

1. Choose $I_C = 0.5\,mA$
2. Choose R_E to centre V_o @ $\frac{V_{cc}}{2}$

$$I_E R_E = V_E = \frac{V_{cc}}{2}$$

$$R_E = \frac{V_{cc}}{2I_E} = 10K\Omega$$

R_E can be any value as long as $\leq 10K$

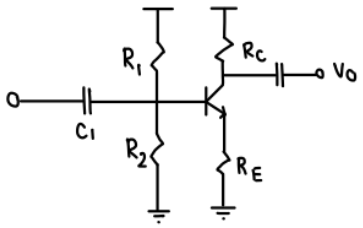
R_{b1} and R_{b2} can be any value $\leq 100k$ as

$$R_{b2} \leq \frac{\beta R_e}{10} \leq 100K$$

Choose $R_{b1} = R_{b2} = 30K\Omega$

$$R_{in} = R_{b1} // R_{b2} // R_{be} \approx 24.691k\Omega$$

2nd stage: CE amplifier



Choose operating point

$I_C = 0.5mA$ ($< 10mA$)

$\Rightarrow I_E \approx 0.5mA$

1. V_E should be ~10% of power supply or 1^V for DC stability

$V_E = 1^V$

$I_E R_E = 1^V$

$R_E = \frac{1}{0.5mA} = 2K\Omega$

2. V_C should be in the middle of transistor's operating point

$\Rightarrow V_C = 1/2 V_{CC}$

$I_C R_C = 5$

$R_C = 5 / 0.5mA = 10K\Omega$

3. Calculate the voltage divider resistors' value.

$V_B - V_E = 0.7^V$

$V_B = 1.7^V$

$\Rightarrow V_{B2} = 1.7^V$

$\frac{V_{B1}}{V_{B2}} = \frac{10^V - 1.7^V}{1.7^V} = 4.88$

For stable $V_B \Rightarrow R_{B2} \lessapprox \beta \frac{R_E}{10}$ $\qquad r_e = \frac{V_t}{I_C} \approx \frac{26\,mV}{0.5mA} \approx 50\Omega$

$R_{B2} \lessapprox 20K \Rightarrow R_{B2} = 20K\Omega$

$\Rightarrow R_{B1} \lessapprox 97.647K \Rightarrow R_{B1} = 91K\Omega$

linear amplification : $A_V = \frac{R_C}{R_E} = \frac{10K}{2K} = 5$

we want the amplification ~ 50

$A_V = \frac{R_C}{r_e' + R_{E_1}}$

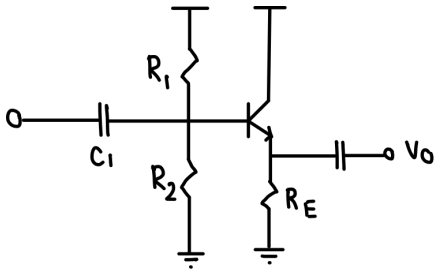
$r_e + R_{E_1} = \frac{R_C}{A_C} = \frac{10K}{50} = 200$

$r_e' = 50\Omega \Rightarrow R_{E_1} = 150\Omega$

$R_{E_1} + R_{E_2} = 2K \Rightarrow R_{E_2} = 1.2K\Omega$

Choose R_{E_2} as it produces a better looking graph.

3rd stage: CC amplifier



1. Choose $I_C = 0.5\,mA$
2. Choose R_E to centre V_o @ $\frac{V_{cc}}{2}$

$$I_E R_E = V_E = \frac{V_{cc}}{2}$$

$$R_E = \frac{V_{cc}}{2I_E} = 10K\Omega$$

But the V_o, max voltage swing $5^V \Rightarrow V_E \leq 4.3^V$ for $V_{BE} \geq 0.7^V$

$$R_E \leq 10K\Omega$$

Choose $R_E = 1K\Omega$

Multistage voltage gain amplification

CC	CE	CC
$Zin_1 \approx 25K$	$Zin_2 = 8K$	$Zin_3 = 0$
$Z_{out_1} = 50$	$Z_{out_2} = 9.1K$	$Z_{out_3} = 1K$
$A_{V_1} = 1$	$A_{V_2} = 50$	$A_{V_3} = 1$

$$A_{V_1} = A_{V_1} \cdot \frac{Zin_2}{Zin_2 + Z_{out_1}} = \frac{8K}{8.05K} \cdot 1 \approx 0.9937$$

$$A_{V_2} = A_{V_2} \frac{Zin_3}{Zin_3 + Z_{out_2}} = \frac{9.1K}{9.1K} \cdot 50 = 50$$

$$A_V = A_{V_1} \times A_{V_2} \times A_{V_3} \approx 50$$

Conclusion and remarks

Following a comprehensive investigation and testing, it is certified that the circuit fulfills the stipulated specifications. However, small differences were discovered during the study, notably in the waveform display. The final output waveform had a minor distortion, as seen by a small cut-off at the bottom. This distortion, while present, is controllable and may be mitigated by making changes such as raising the emitter current.

Despite the observed distortion, the circuit's overall performance is outstanding, with all important requirements satisfied. The circuit's ability to sustain the necessary voltage increases with and without load, which is consistent with the anticipated objectives.

Furthermore, the frequency response analysis demonstrates strong performance, with the circuit achieving maximum gain within the given frequency range. The circuit's lower cutoff frequency of about 100Hz suggests its ability to tolerate a wide range of frequencies well.

In conclusion, although noting the modest waveform distortion, the circuit's compliance with the needed requirements emphasizes its overall functioning and appropriateness for the intended applications. Moving ahead, improvements may be made to rectify the detected differences, resulting in even better accuracy and dependability in performance.