Department of Electrical
& Computer Engineering
Faculty of Engineering & Architectural Science

Ryerson University

Course Title:	Electronic Circuit I
Course Number:	ELE404
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Instructor	Dr. Fei Yuan

Assignment/Lab Number:	
Assignment/Lab Title:	Design Project

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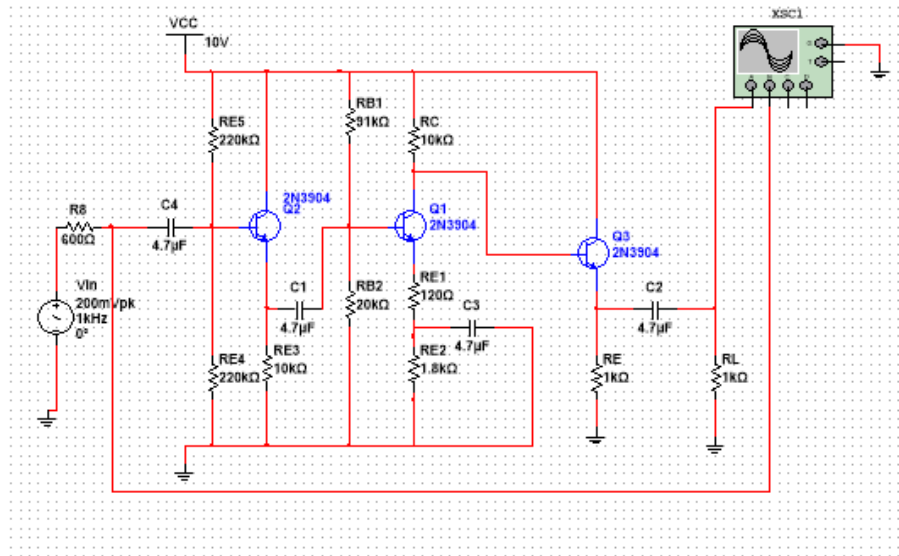| Student LAST Name	Student FIRST Name	Student Number	Section	Signature*
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I: Introduction

II: Objective

Specifications

- Power supply: **+10V** relative to the ground;
- Quiescent current drawn from the power supply: **no larger than 10 mA**;
- No-load voltage gain (at $1\ kHz$): $|A_{vo}| = 50\ (\pm\ 10\%)$;
- Maximum no-load output voltage swing (at $1\ kHz$): **no smaller than 8 V peak to peak**;
- Loaded voltage gain (at $1\ kHz$ and with $R_L = 1\ k\Omega$): **no smaller than 90% of the no-load voltage gain;**
- Maximum loaded output voltage swing (at $1\ kHz$ and $R_L = 1\ k\Omega$): **no smaller than 4 V peak to peak;**
- Input resistance (at $1\ kHz$): **no smaller than 20 kΩ**;
- Amplifier type: **inverting or non-inverting;**
- Frequency response: **20 Hz to 50 kHz ($-3dB$ response);**
- Type of transistors: **BJT;**
- Number of transistors (stages): **no more than 3;**
- Resistances permitted: **values smaller than 220 kΩ from the E24 series**;
- Capacitors permitted: **0. 1 μF, 1. 0 μF, 2. 2 μF, 4. 7 μF, 10 μF, 47 μF, 100 μF, 220 μF;**
- Other components (BJTs, diodes, Zener diodes, etc.): **only from your ELE404 lab kit.**
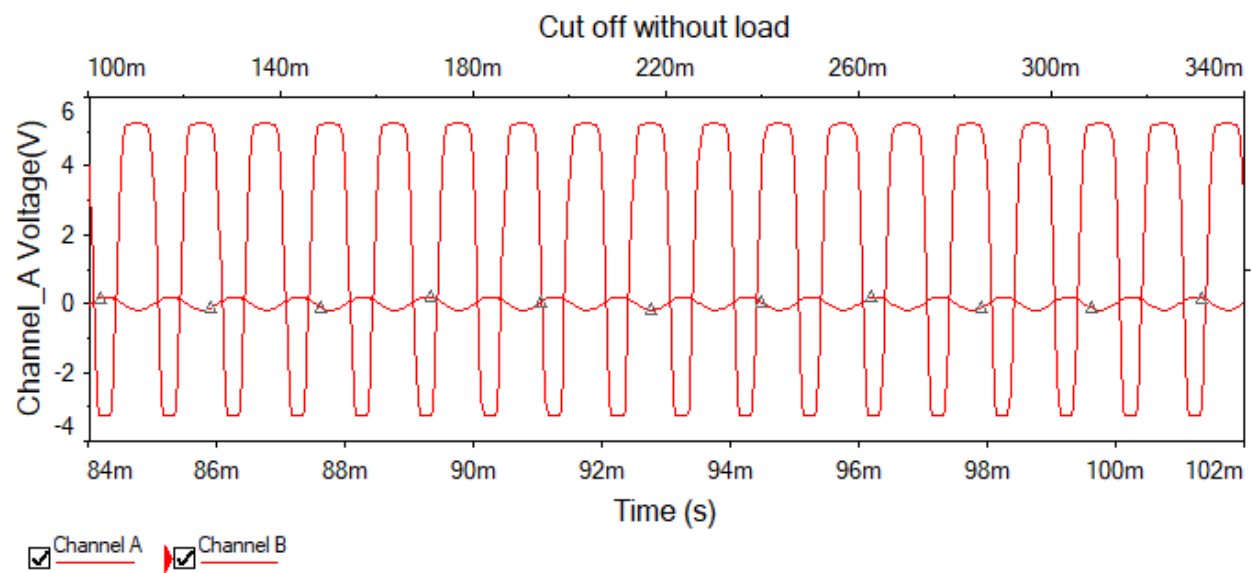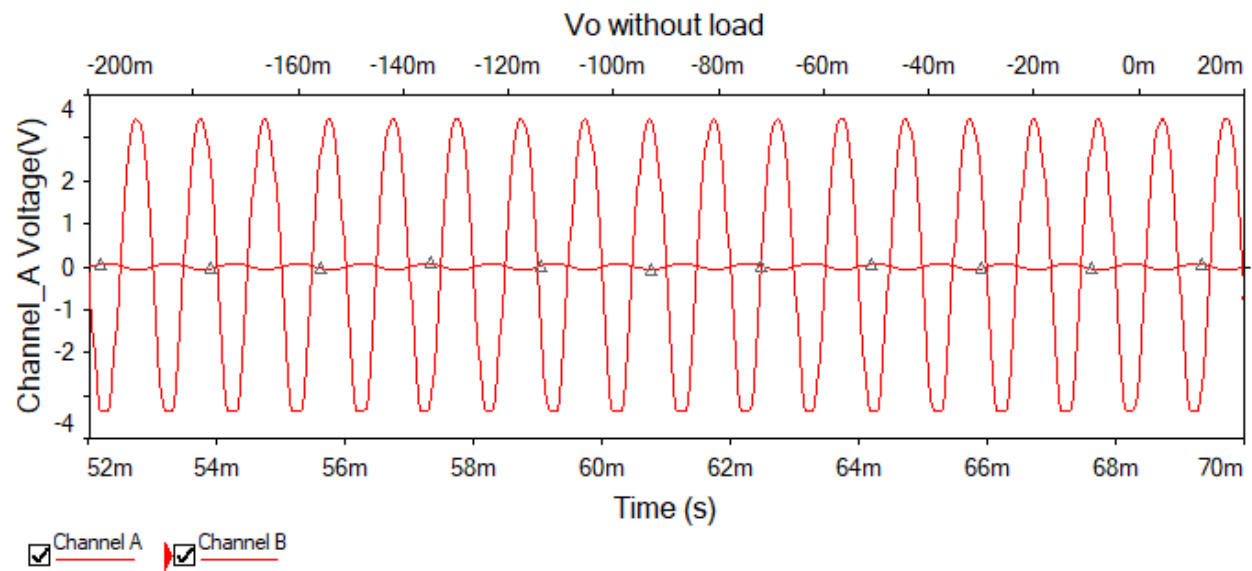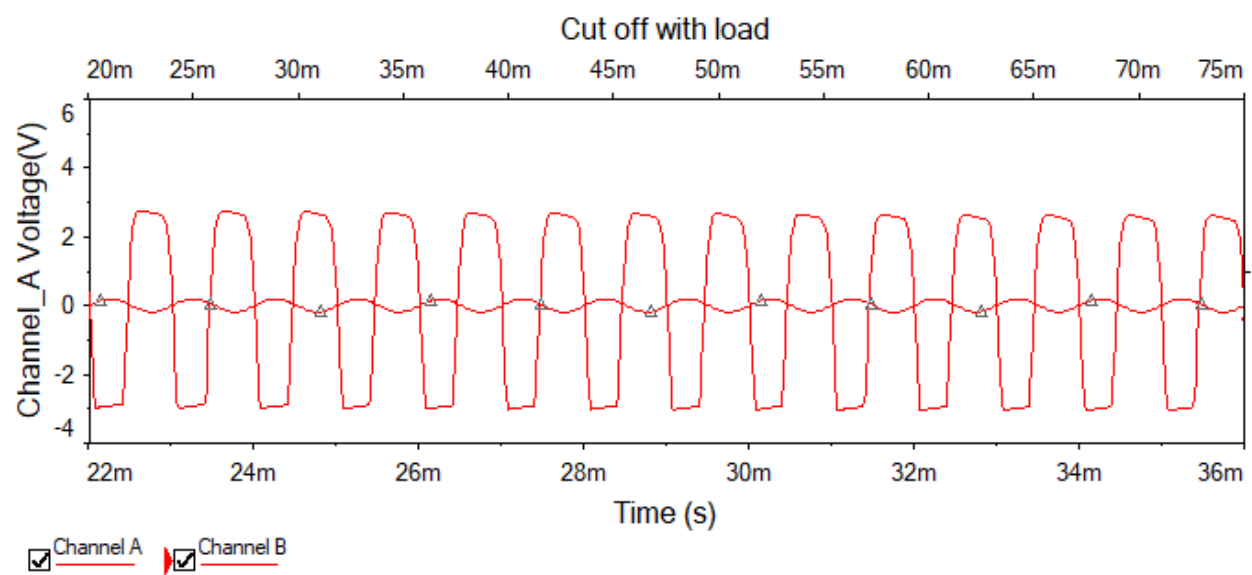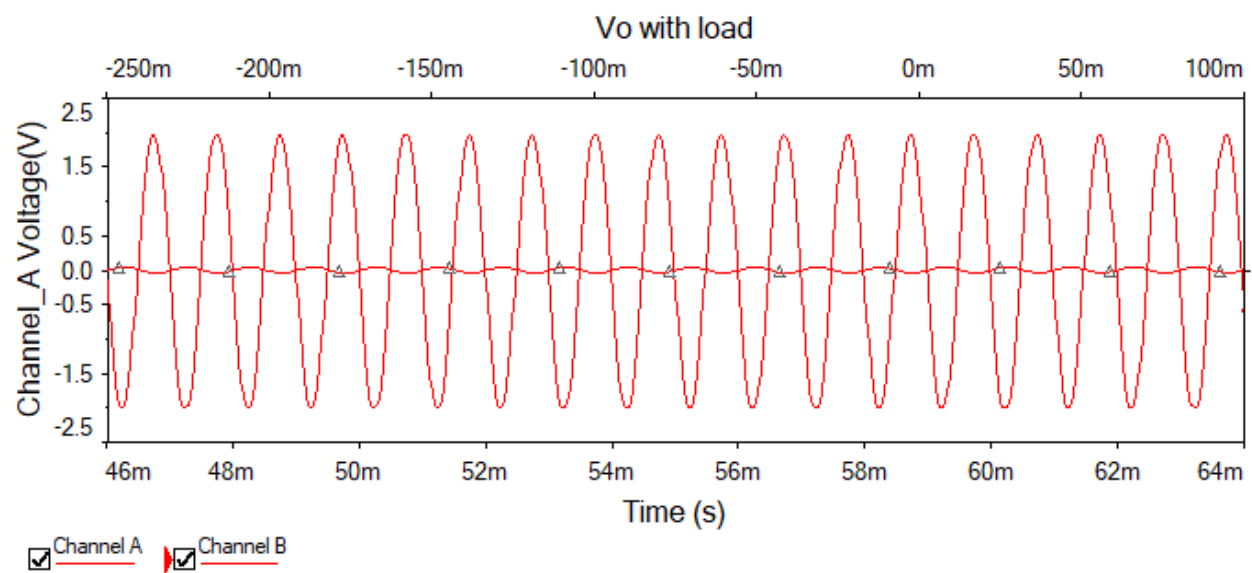
III: Circuit

According to the specifications, I have made a circuit with approximately 50 volts again. I utilized the CC-CE-CC configuration to design the circuit.

1. The first stage employs a CC amplifier configuration to increase the input resistance to above 20k ohms.

2. The second stage utilizes a CE amplifier configuration to amplify the input signal by 50 times (Av no load = 50).

3. The third stage adopts a CC configuration to stabilize the load at 1K, ensuring that the voltage gain does not drop below 90% of the no-load voltage gain (~45).

IV: Experimental Results

Vo without load

☑ Channel A   ☑ Channel B

Cut off without load

☑ Channel A   ☑ Channel B

Vo with load

Channel A   Channel B

Cut off with load

Channel A   Channel B

AC frequency Response


V(4)
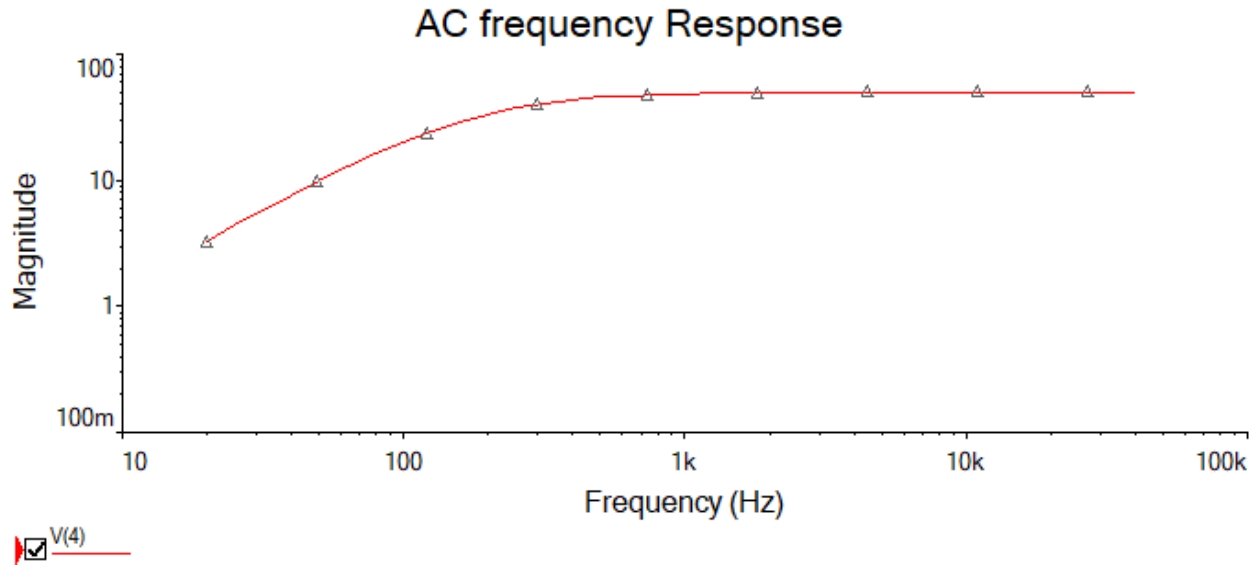
V: Explanation

When testing the circuit without any load, I applied an 80mV input signal and observed a voltage gain of approximately 50. However, when a load was introduced, the voltage gain dropped to around 40 under the same conditions.

Considering the operational limits, the circuit has a maximum swing of 10 volts peak-to-peak (Vpp) without load, restricting it to a range between +5V and -5V. With a load, the maximum swing reduces to 6 volts peak-to-peak, limiting it between +3V and -3V. The quiescent current of 3 resistors are approximately 1.5mA which is less than 10mA

Examining its frequency response, the circuit achieves its maximum gain starting from 20Hz onwards up to 50kHz. Additionally, the lower cutoff frequency is approximately 100Hz, indicating its operational range in terms of frequency. These observations provide insights into the performance and limitations of the circuit across different conditions and frequencies.

VI: Manual Calculation

First stage: CC amplifier
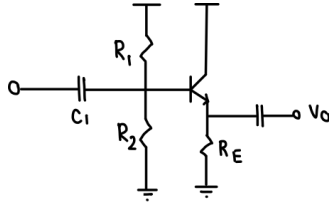
CC theoritically has $A_v = 1$ ⇒ Can be used to increase input impendence

1. Choose $I_C = 0.5 mA$

2. Choose R_E to centre V_o @ $\frac{Vcc}{2}$

$$I_E R_E = V_E = \frac{Vcc}{2}$$

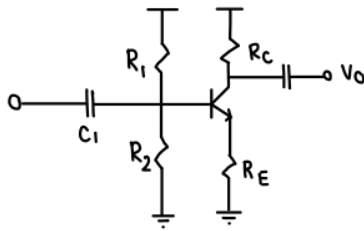$$R_E = \frac{Vcc}{2I_E} = 10K\,\Omega$$

R_E can be any value as long as $\leq 10K$

R_{b_1} and R_{b_2} can be any value $\leq 100k$ as

$$R_{b_2} \leq \frac{\beta R_e}{10} < 100K$$

Choose $R_{b_1} = R_{b_2} = 50K\,\Omega$

$$R_{in} = R_{b_1} \| R_{b_2} \| R_{be} = R_{b_1} \| R_{b_2} \| \beta(re' + Re)$$
$$= 24.39K\,\Omega$$

2nd stage: CE amplifier

Choose operating point

$$I_C = 0.5\,mA \quad (\;\; < 10\,mA)$$

$$\Rightarrow I_E \approx 0.5\,mA$$

1. V_E should be $\sim 10\%$ of power supply or 1^V for DC stability

$$V_E = 1^V$$

$$I_E R_E = 1^V$$

$$R_E = \frac{1}{0.5\,mA} = 2K\,\Omega$$

2. V_C should be in the middle of transistor's operating point

$$\Rightarrow V_C = \tfrac{1}{2} V_{CC}$$

$$I_C R_C = 5$$

$$R_C = 5 / 0.5\,mA = 10K\,\Omega$$

3. Calculate the voltage divider resistors' value.

$$V_B - V_E = 0.7^V$$

$$V_B = 1.7^V$$

$$\Rightarrow V_{B2} = 1.7^V$$

$$\frac{V_{B1}}{V_{B2}} = \frac{10^V - 1.7^V}{1.7^V} = 4.88$$

For stable $V_B \Rightarrow R_{B2} < \beta \dfrac{R_E}{10}$ 　　　 $r_e = \dfrac{V_t}{I_C} \approx \dfrac{26\,mV}{0.5\,mA} \approx 50\,\Omega$

$$R_{B2} < 20K \quad \Rightarrow R_{B2} = 20K \;\Omega$$

$$\Rightarrow R_{B1} < 97.647K \quad \Rightarrow R_{B1} = 91K \;\Omega$$

linear amplification : $A_V = \dfrac{R_C}{R_E} = \dfrac{10K}{2K} = 5$

We want the amplification ~ 50

$$A_V = \frac{R_C}{r_e' + R_{E_1}}$$

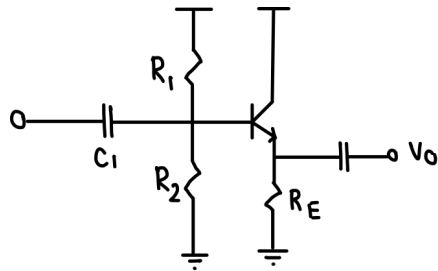$$r_e + R_{E_1} = \frac{R_C}{A_C} = \frac{10k}{50} = 200$$

$$r_e' = 50\,\Omega \quad \Rightarrow \quad R_{E_1} = 150\,\Omega$$

$$R_{E_1} + R_{E_2} = 2k \Rightarrow R_{E_2} = 1.8K\Omega$$

Choose $R_{E_2} = 2K$ as it produces a better looking graph.

3rd stage: CC amplifier

1. Choose $I_C = 0.5 \, mA$

2. Choose R_E to centre V_0 @ $\frac{Vcc}{2}$

$$I_E R_E = V_E = \frac{Vcc}{2}$$

$$R_E = \frac{Vcc}{2 I_E} = 10K \, \Omega$$

But the $V_{0,}$ max voltage swing $5^V \Rightarrow V_E \leq 4.3 \, V$ for $V_{BE} \geqslant 0.7^V$

$$R_E \leq 10K\Omega$$

Choose $R_E = 1K\Omega$ $\Rightarrow$ $I_Q = \frac{Vcc}{2R_E} = 5mA$

The higher the emitter current the better

Voltage diver is not needed in the third stage.
Multistage voltage gain amplification

CC	CE	CC
$Zin_1 \approx 25K$	$Zin_2 = 8K$	$Zin_3 = 0$
$Zout_1 = 50$	$Zout_2 = 9.1k$	$Zout_3 = 1K$
$Av_1 = 1$	$Av_2 = 50$	$Av_3 = 1$

$$Av_1 = Av_1 \cdot \frac{Zin_2}{Zin_2 + Zout_1} = \frac{8K}{8.05k} \cdot 1 \approx 0.9937$$

$$Av_2 = Av_2 \frac{Zin_3}{Zin_3 + Zout_2} = \frac{9.1k}{9.1k} \cdot 50 = 50$$

$$Av = Av_1 \times Av_2 \times Av_3 \approx 50$$

Quiescent current: Ie1 + Ic2 + Ie3 (as the operating points have been chosen above)

Quienscent current : $I_{E_1} + I_{C_2} + I_{E_2}$

$$\approx 0.5mA + 0.5mA + 6mA$$

$$\approx 7mA \quad (< 10mA)$$

Conclusion and remarks

Following a comprehensive investigation and testing, it is certified that the circuit fulfills the stipulated specifications. However, small differences were discovered during the study, notably in the waveform display. The final output waveform had a minor distortion, as seen by a small cut-off at the bottom. This distortion, while present, is controllable and may be mitigated by making changes such as raising the emitter current.

Despite the observed distortion, the circuit's overall performance is outstanding, with all important requirements satisfied. The circuit's ability to sustain the necessary voltage increases with and without load, which is consistent with the anticipated objectives.

Furthermore, the frequency response analysis demonstrates strong performance, with the circuit achieving maximum gain within the given frequency range. The circuit's lower cutoff frequency of about 100Hz suggests its ability to tolerate a wide range of frequencies well.

In conclusion, although noting the modest waveform distortion, the circuit's compliance with the needed requirements emphasizes its overall functioning and appropriateness for the intended applications. Moving ahead, improvements may be made to rectify the detected differences, resulting in even better accuracy and dependability in performance.