SLG7XL45106

GreenPAK ™

Reset Chip

General Description

Dialog SLG7XL45106 is a low power and small form device. The SoC is housed in a 4mm x 4mm STQFN package which is optimal for using with small devices.

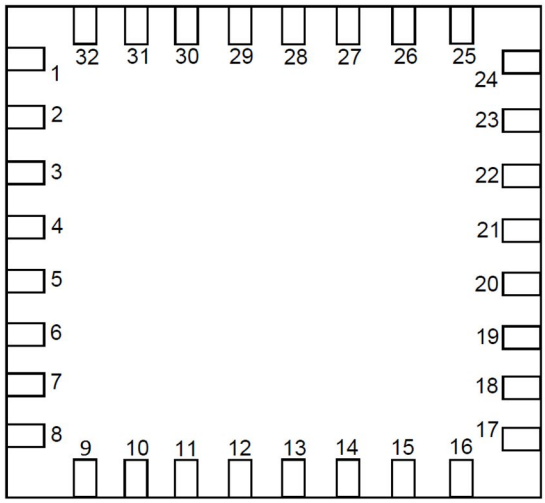
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 32 Package

Output Summary

12 Outputs - Open Drain NMOS 1X

Pin Configuration

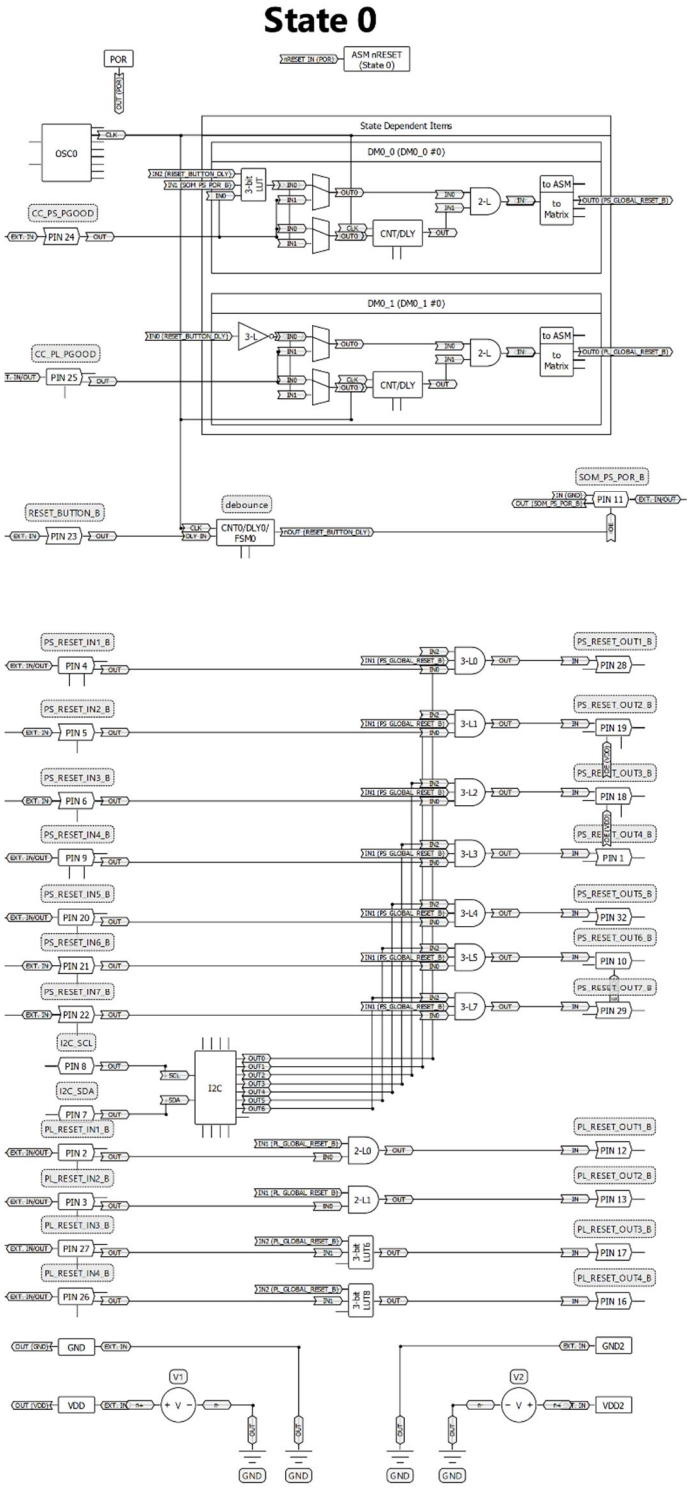


STQFN-32 (Top view)

Pin name

Pin #	Pin name	Pin #	Pin name
1	PS_RESET_OUT4_B	17	PL_RESET_OUT3_B
2	PL_RESET_IN1_B	18	PS_RESET_OUT3_B
3	PL_RESET_IN2_B	19	PS_RESET_OUT2_B
4	PS_RESET_IN1_B	20	PS_RESET_IN5_B
5	PS_RESET_IN2_B	21	PS_RESET_IN6_B
6	PS_RESET_IN3_B	22	PS_RESET_IN7_B
7	I2C_SDA	23	RESET_BUTTON_B
8	I2C_SCL	24	CC_PS_PGOOD
9	PS_RESET_IN4_B	25	CC_PL_PGOOD
10	PS_RESET_OUT6_B	26	PL_RESET_IN4_B
11	SOM_PS_POR_B	27	PL_RESET_IN3_B
12	PL_RESET_OUT1_B	28	PS_RESET_OUT1_B
13	PL_RESET_OUT2_B	29	PS_RESET_OUT7_B
14	GND	30	GND
15	VDD2	31	VDD
16	PL_RESET_OUT4_B	32	PS_RESET_OUT5_B

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	PS_RESET_OUT4_B	Digital Output	Open Drain NMOS 1X	floating
2	PL_RESET_IN1_B	Digital Input	Low Voltage Digital Input	1MΩ pulldown
3	PL_RESET_IN2_B	Digital Input	Low Voltage Digital Input	1MΩ pulldown
4	PS_RESET_IN1_B	Digital Input	Low Voltage Digital Input	1MΩ pulldown
5	PS_RESET_IN2_B	Digital Input	Low Voltage Digital Input	1MΩ pulldown
6	PS_RESET_IN3_B	Digital Input	Low Voltage Digital Input	1MΩ pulldown
7	I2C_SDA	Digital Input	Low Voltage Digital Input	floating
8	I2C_SCL	Digital Input	Low Voltage Digital Input	floating
9	PS_RESET_IN4_B	Digital Input	Low Voltage Digital Input	1MΩ pulldown
10	PS_RESET_OUT6_B	Digital Output	Open Drain NMOS 1X	floating
11	SOM_PS_POR_B	Bi-directional	Low Voltage Digital Input / Open Drain NMOS 1X	floating
12	PL_RESET_OUT1_B	Digital Output	Open Drain NMOS 1X	floating
13	PL_RESET_OUT2_B	Digital Output	Open Drain NMOS 1X	floating
14	GND	GND	Ground	--
15	VDD2	PWR	Supply Voltage	--
16	PL_RESET_OUT4_B	Digital Output	Open Drain NMOS 1X	floating
17	PL_RESET_OUT3_B	Digital Output	Open Drain NMOS 1X	floating
18	PS_RESET_OUT3_B	Digital Output	Open Drain NMOS 1X	floating
19	PS_RESET_OUT2_B	Digital Output	Open Drain NMOS 1X	floating
20	PS_RESET_IN5_B	Digital Input	Low Voltage Digital Input	1MΩ pulldown
21	PS_RESET_IN6_B	Digital Input	Low Voltage Digital Input	1MΩ pulldown
22	PS_RESET_IN7_B	Digital Input	Low Voltage Digital Input	1MΩ pulldown
23	RESET_BUTTON_B	Digital Input	Digital Input without Schmitt trigger	10kΩ pullup
24	CC_PS_PGOOD	Digital Input	Digital Input without Schmitt trigger	floating
25	CC_PL_PGOOD	Digital Input	Digital Input without Schmitt trigger	floating
26	PL_RESET_IN4_B	Digital Input	Low Voltage Digital Input	1MΩ pulldown
27	PL_RESET_IN3_B	Digital Input	Low Voltage Digital Input	1MΩ pulldown
28	PS_RESET_OUT1_B	Digital Output	Open Drain NMOS 1X	floating
29	PS_RESET_OUT7_B	Digital Output	Open Drain NMOS 1X	floating
30	GND	GND	Ground	--
31	VDD	PWR	Supply Voltage	--
32	PS_RESET_OUT5_B	Digital Output	Open Drain NMOS 1X	floating

Ordering Information

Part Number	Package Type
SLG7XL45106V	32-pin STQFN
SLG7XL45106VTR	32-pin STQFN - Tape and Reel (5k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at Input Pin	GND-0.5V	VDD+0.5V	V
Maximum Average or DC Current (Through V_{DD} or GND pin)	--	90	mA
Current at Input Pin	-1.0	1.0	mA
Input leakage Current (Absolute Value)	--	1000	nA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD} (Note 4)	Supply Voltage		2.3	5	5.5	V
V_{DD2} (Note 4)	Supply Voltage		2.3	5	5.5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3	V
V_{IH}	HIGH-Level Input Voltage	Logic Input at VDD=2.5V	0.7 x VDD	--	VDD+0.3	V
		Logic Input at VDD=3.3V	0.7 x VDD	--	VDD+0.3	V
		Logic Input at VDD=5.0V	0.7 x VDD	--	VDD+0.3	V
		Low-Level Logic Input at VDD=2.5V	1.25	--	VDD+0.3	V
		Low-Level Logic Input at VDD=3.3V	1.25	--	VDD+0.3	V
		Low-Level Logic Input at VDD=5.0V	1.25	--	VDD+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input at VDD=2.5V	GND-0.3	--	0.3xVDD	V
		Logic Input at VDD=3.3V	GND-0.3	--	0.3xVDD	V
		Logic Input at VDD=5.0V	GND-0.3	--	0.3xVDD	V
		Low-Level Logic Input at VDD=2.5V	GND-0.3	--	0.5	V
		Low-Level Logic Input at VDD=3.3V	GND-0.3	--	0.5	V
		Low-Level Logic Input at VDD=5.0V	GND-0.3	--	0.5	V

V_{OL}	LOW-Level Output Voltage	Open Drain NMOS 1X, I_{OL}=100µA, at VDD=2.5V	--	0.003	0.011	V
		Open Drain NMOS 1X, I_{OL}=3mA, at VDD=3.3V	--	0.063	0.087	V
		Open Drain NMOS 1X, I_{OL}=5mA, at VDD=5.0V	--	0.079	0.114	V
I_{OL}	LOW-Level Output Current (Note 1)	Open Drain NMOS 1X, V_{OL}=0.15V, at VDD=2.5V	4.15	5.38	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=3.3V	12.90	17.14	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=5.0V	16.98	23.70	--	mA
R_{PULL_UP}	Internal Pull Up Resistance	Pull up on PIN 23	7	--	17	kΩ
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PINs 2, 3, 4, 5, 6, 9, 20, 21, 22, 26, 27	740	--	1500	kΩ
T_{DLY0}	Delay0 Time	At temperature 25°C	40.56	41.26	42.89	ms
		At temperature -40 +85°C (Note 3)	40.22	41.62	45.53	ms
$T_{DM0\_0\ (DM0\_0\ \#0)}$	Delay Time	At temperature 25°C	25.10	25.63	27.09	ms
		At temperature -40 +85°C (Note 3)	24.90	25.86	28.73	ms
$T_{DM0\_1\ (DM0\_1\ \#0)}$	Delay Time	At temperature 25°C	25.10	25.63	27.09	ms
		At temperature -40 +85°C (Note 3)	24.90	25.86	28.73	ms
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1.13	1.72	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.64	1.84	2.11	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.98	1.25	1.49	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides.
3. Guaranteed by Design.
4. PINs 1, 2, 3, 4, 5, 6, 7, 8, 9, 20, 21, 22, 23, 24, 25, 26, 27, 28, 29, 32 are powered from VDD and PINs 10, 11, 12, 13, 16, 17, 18, 19 are powered from VDD2.

I²C Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
F_{SCL}	Clock Frequency, SCL	V_{DD} = (2.3...5.5) V	--	--	1000	kHz
t_{LOW}	Clock Pulse Width Low	V_{DD} = (2.3...5.5) V	500	--	--	ns
t_{HIGH}	Clock Pulse Width High	V_{DD} = (2.3...5.5) V	260	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = 2.5V ± 8%	--	--	168	ns
		V_{DD} = 3.3V ± 10%	--	--	157	ns
		V_{DD} = 5.0V ± 10%	--	--	156	ns
t_{AA}	Clock Low to Data Out Valid	V_{DD} = (2.3...5.5) V	--	--	450	ns
t_{BUF}	Bus Free Time between Stop and Start	V_{DD} = (2.3...5.5) V	500	--	--	ns
t_{HD_STA}	Start Hold Time	V_{DD} = (2.3...5.5) V	260	--	--	ns
t_{SU_STA}	Start Set-up Time	V_{DD} = (2.3...5.5) V	260	--	--	ns
t_{HD_DAT}	Data Hold Time	V_{DD} = (2.3...5.5) V	0	--	--	ns

t_{SU_DAT}	Data Set-up Time	V_{DD} = (2.3...5.5) V	50	--	--	ns
t_R	Inputs Rise Time	V_{DD} = (2.3...5.5) V	--	--	120	ns
t_F	Inputs Fall Time	V_{DD} = (2.3...5.5) V	--	--	120	ns
t_{SU_STO}	Stop Set-up Time	V_{DD} = (2.3...5.5) V	260	--	--	ns
t_{DH}	Data Out Hold Time	V_{DD} = (2.3...5.5) V	170.70	--	--	ns

Asynchronous State Machine (ASM) Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
$t_{st\_out\_delay}$	Asynchronous State Machine Output Delay Time	VDD = 2.5V ± 8%	133	--	277	ns
		VDD = 3.3V ± 10%	96	--	190	ns
		VDD = 5.0V ± 10%	70	--	123	ns
t_{st_out}	Asynchronous State Machine Output Transition Time	VDD = 2.5V ± 8%	--	--	165	ns
		VDD = 3.3V ± 10%	--	--	70	ns
		VDD = 5.0V ± 10%	--	--	46	ns
t_{st_pulse}	Asynchronous State Machine Input Pulse Acceptance Time	VDD = 2.5V ± 8%	28	--	--	ns
		VDD = 3.3V ± 10%	19	--	--	ns
		VDD = 5.0V ± 10%	12	--	--	ns
t_{st_comp}	Asynchronous State Machine Input Compete Time	VDD = 2.5V ± 8%	--	--	10	ns
		VDD = 3.3V ± 10%	--	--	7	ns
		VDD = 5.0V ± 10%	--	--	5	ns
$t_{st\_sequential\_delay}$	Asynchronous State Machine Sequential Output Delay Time	VDD = 2.5V ± 8%	229	--	485	ns
		VDD = 3.3V ± 10%	162	--	330	ns
		VDD = 5.0V ± 10%	119	--	208	ns
$t_{st\_dmlatch\_delay}$	Asynchronous State Machine Dynamic Memory Latch Delay	VDD = 2.5V ± 8%	229	--	485	ns
		VDD = 3.3V ± 10%	162	--	330	ns
		VDD = 5.0V ± 10%	119	--	208	ns

Chip address

HEX	BIN	DEC
0x10	0010000	16

I2C Description

1. I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<4083:4080>. The address source is selected by reg<4087>. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read (“1”) or written (“0”) by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 1 shows this basic command structure.

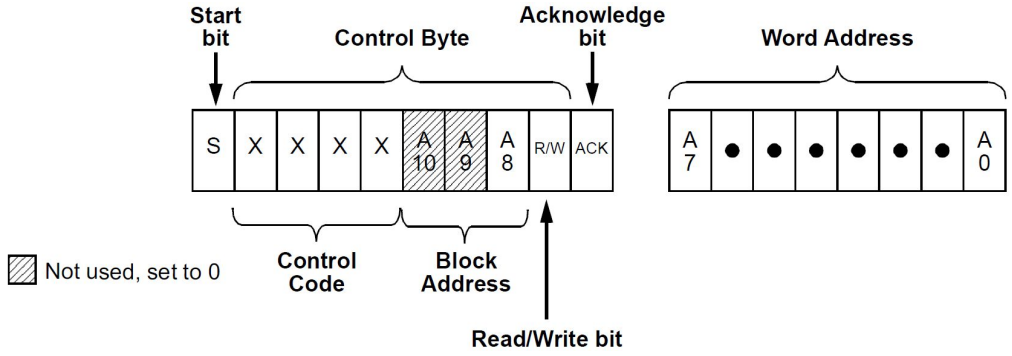


Figure1. I2C Basic Command Structure

2. I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

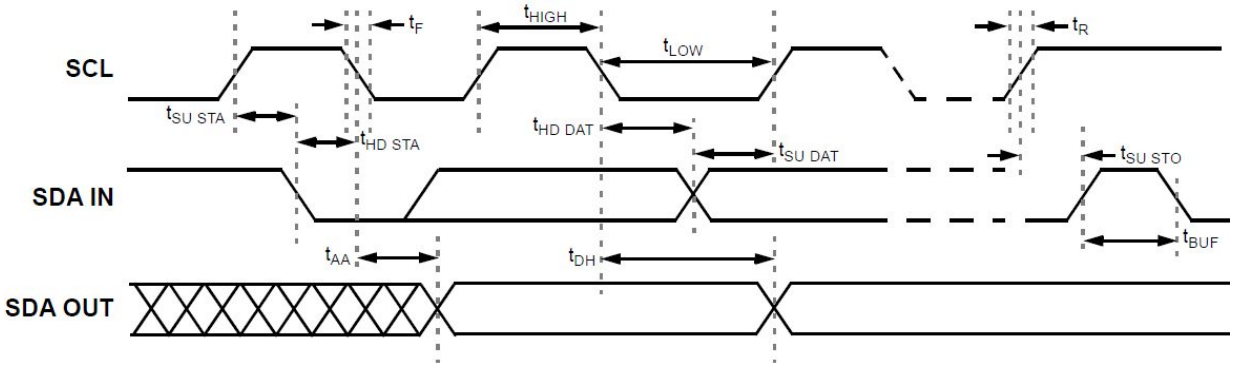


Figure2. I2C Serial General Timing

3. I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to “0”), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledge bit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG7XL45106 to the correct data byte to be written. After the SLG7XL45106 sends another Acknowledge bit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG7XL45106 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7XL45106 generates the Acknowledge bit.

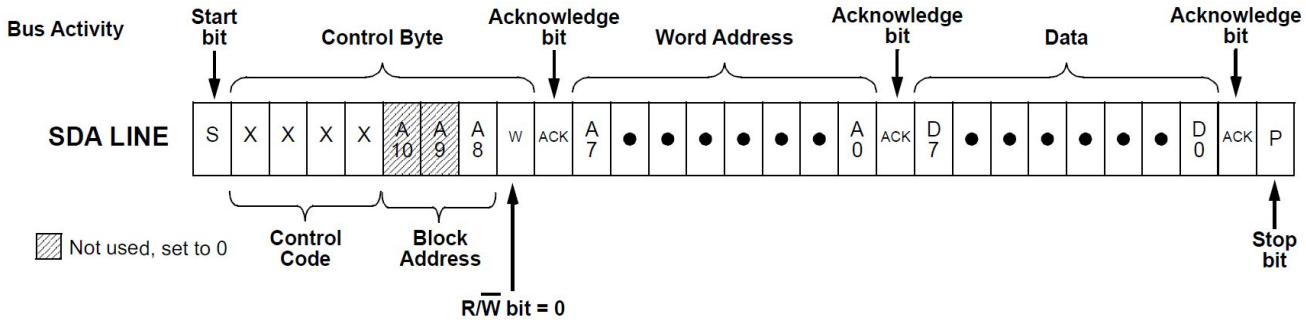


Figure3. I2C Write Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLG7XL45106 issues an Acknowledge bit, followed by the requested eight data bits.

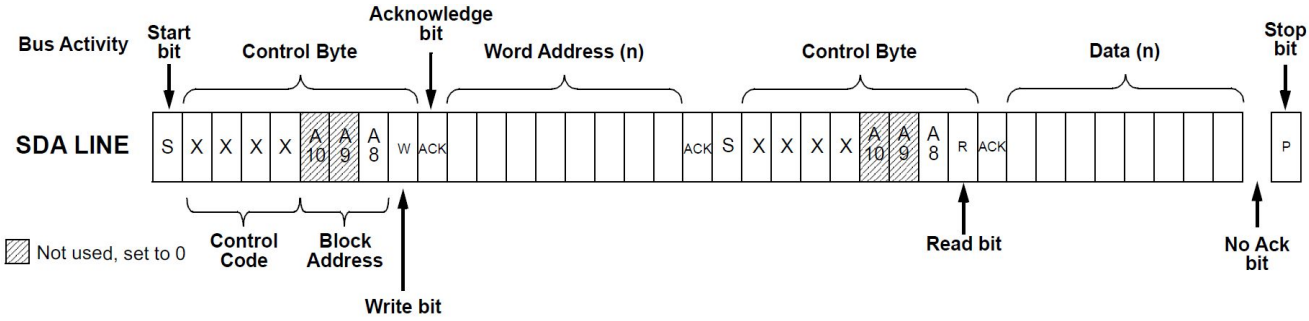


Figure4. I2C Random Read Command

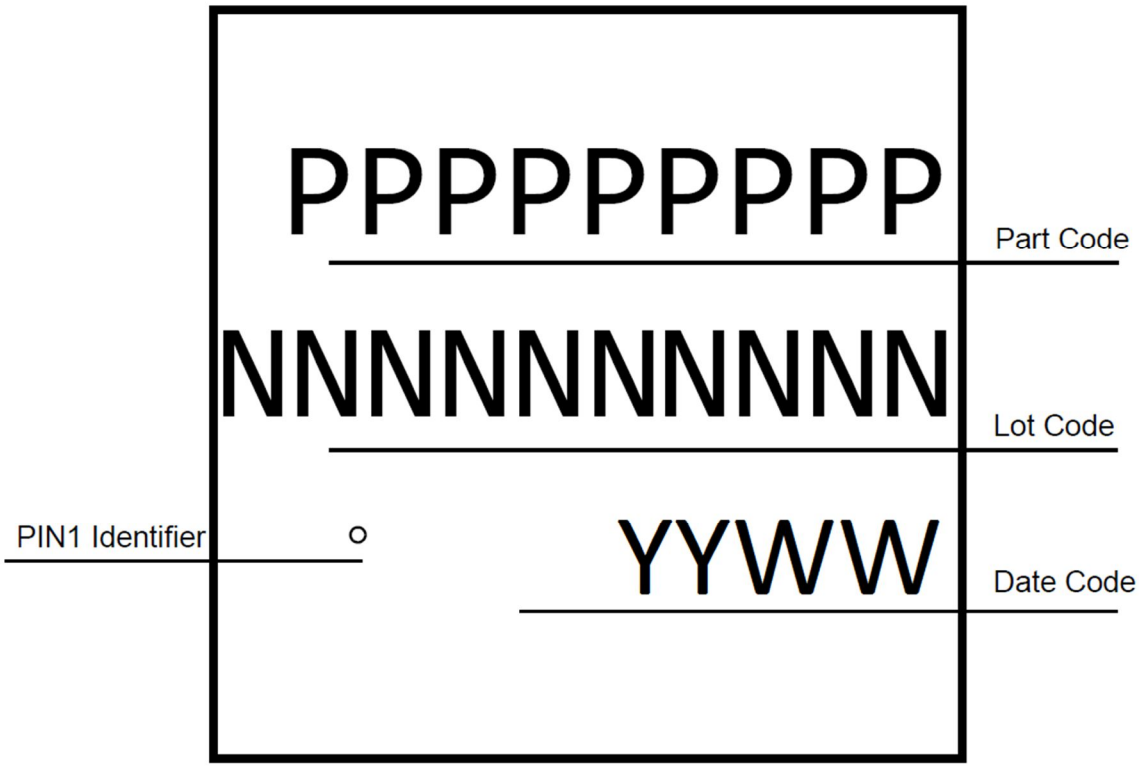
4. I2C register control data

Address Byte	Register Bit	Block	Function
0x1DB	reg<3800>	Virtual Input <0>	Enable (0) and disable (1) Virtual OUT0 Default is 1.
	reg<3801>	Virtual Input <1>	Enable (0) and disable (1) Virtual OUT1 Default is 1.
	reg<3802>	Virtual Input <2>	Enable (0) and disable (1) Virtual OUT2 Default is 1.
	reg<3803>	Virtual Input <3>	Enable (0) and disable (1) Virtual OUT3 Default is 1.
	reg<3804>	Virtual Input <4>	Enable (0) and disable (1) Virtual OUT4 Default is 1.
	reg<3805>	Virtual Input <5>	Enable (0) and disable (1) Virtual OUT5 Default is 1.
	reg<3806>	Virtual Input <6>	Enable (0) and disable (1) Virtual OUT6 Default is 1.

5. I2C Commands:

1. [start] [0x11] [w] [0xDB] [xxxxxxx(OUT0)] [stop] // *enable (OUT0 = 0) or disable (OUT0 = 1)*
2. [start] [0x11] [w] [0xDB] [xxxxxx(OUT1)x] [stop] // *enable (OUT1 = 0) or disable (OUT1 = 1)*
3. [start] [0x11] [w] [0xDB] [xxxxx(OUT2)xx] [stop] // *enable (OUT2 = 0) or disable (OUT2 = 1)*
4. [start] [0x11] [w] [0xDB] [xxxx(OUT3)xxx] [stop] // *enable (OUT3 = 0) or disable (OUT3 = 1)*
5. [start] [0x11] [w] [0xDB] [xxx(OUT4)xxxx] [stop] // *enable (OUT4 = 0) or disable (OUT4 = 1)*
6. [start] [0x11] [w] [0xDB] [xx(OUT5)xxxxx] [stop] // *enable (OUT5 = 0) or disable (OUT5 = 1)*
7. [start] [0x11] [w] [0xDB] [x(OUT6)xxxxxx] [stop] // *enable (OUT6 = 0) or disable (OUT6 = 1)*
8. [start] [0x11] [w] [0xDB] [stop] [start] [0x11] [R] [x(OUT6)(OUT5)(OUT4)(OUT3)(OUT2)(OUT1)(OUT0)][stop] // *read*

Package Top Marking



Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.00	003	L	0xDC3922AC	7XL45106V	B	02/23/2022

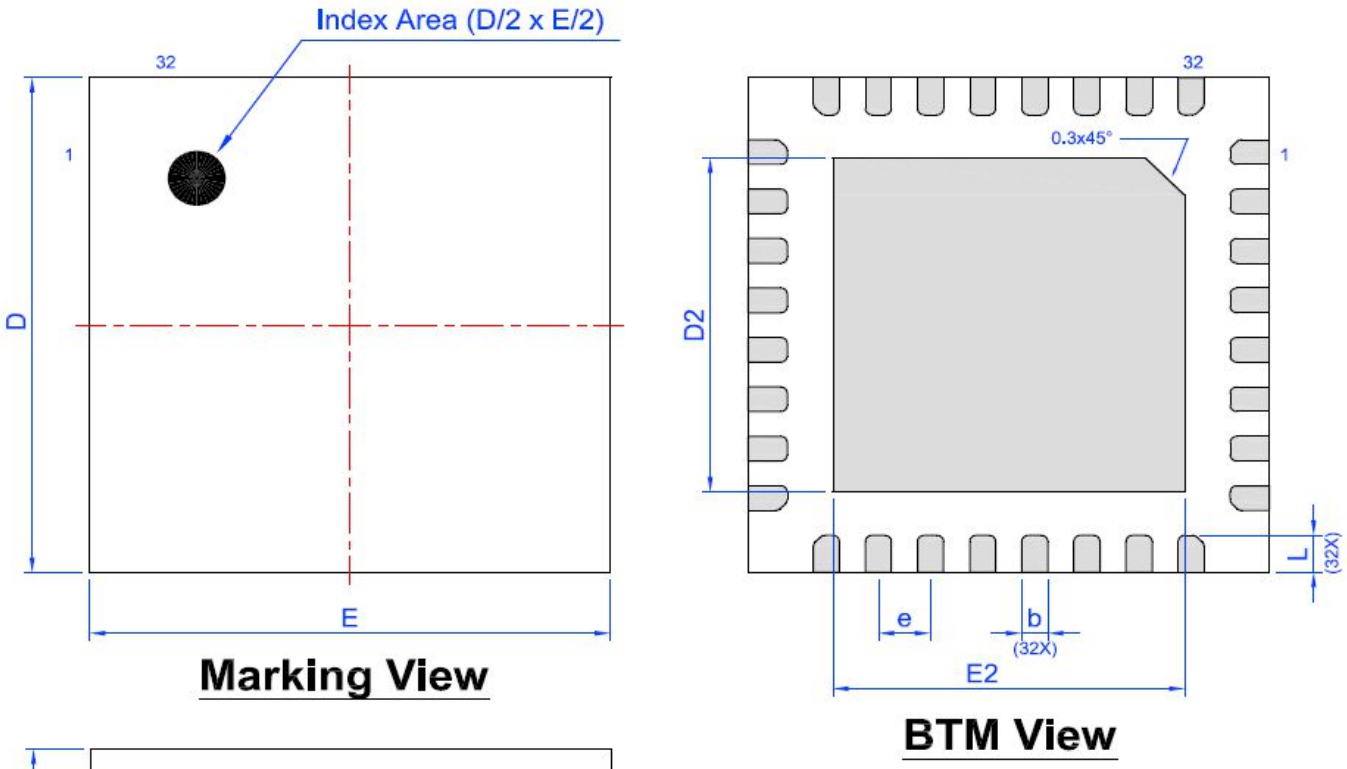
Lock coverage for this part is indicated by √, from one of the following options:

	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
√	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Outlines

STQFN 32L 4x4mm 0.4P Package
IC Net Weight: TBD g



Unit: mm

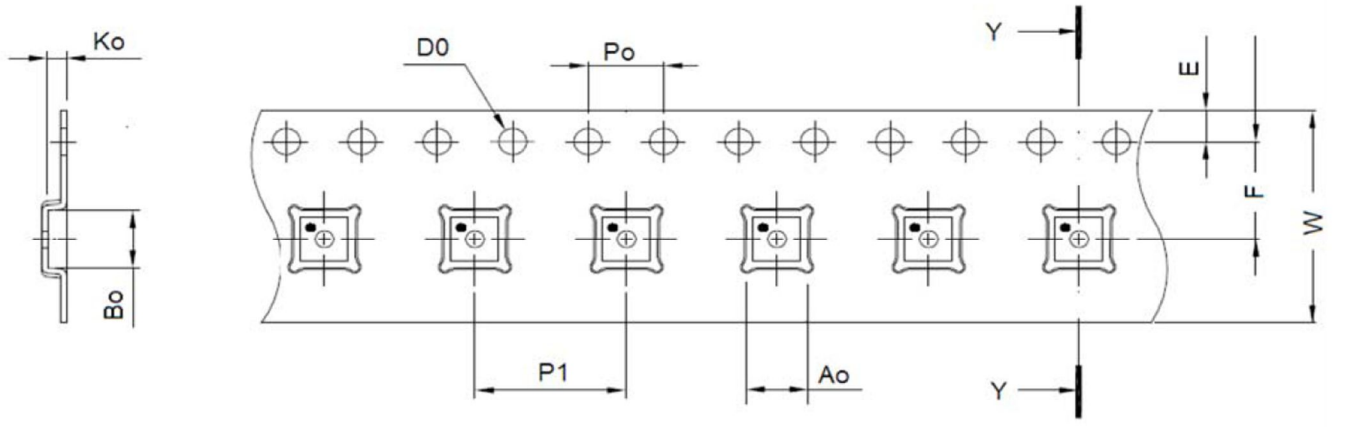
Symbol	Min.	Nom.	Max.	Symbol	Min.	Nom.	Max.
A	0.500	0.550	0.600	D	3.950	4.000	4.050
A1	0.00	-	0.050	E	3.950	4.000	4.050
A2	0.150 REF			D2	2.650	2.700	2.750
b	0.150	0.200	0.250	E2	2.650	0.270	2.750
e	0.400 BSC			L	0.250	0.300	0.350

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 32L 4x4 mm 0.4P Green	32	4 x 4 x 0.55	5000	10000	330/100	42	336	42	336	12	8

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 32L 4x4 mm 0.4P Green	4.25	4.25	0.75	4	8	1.5	1.75	5.5	12

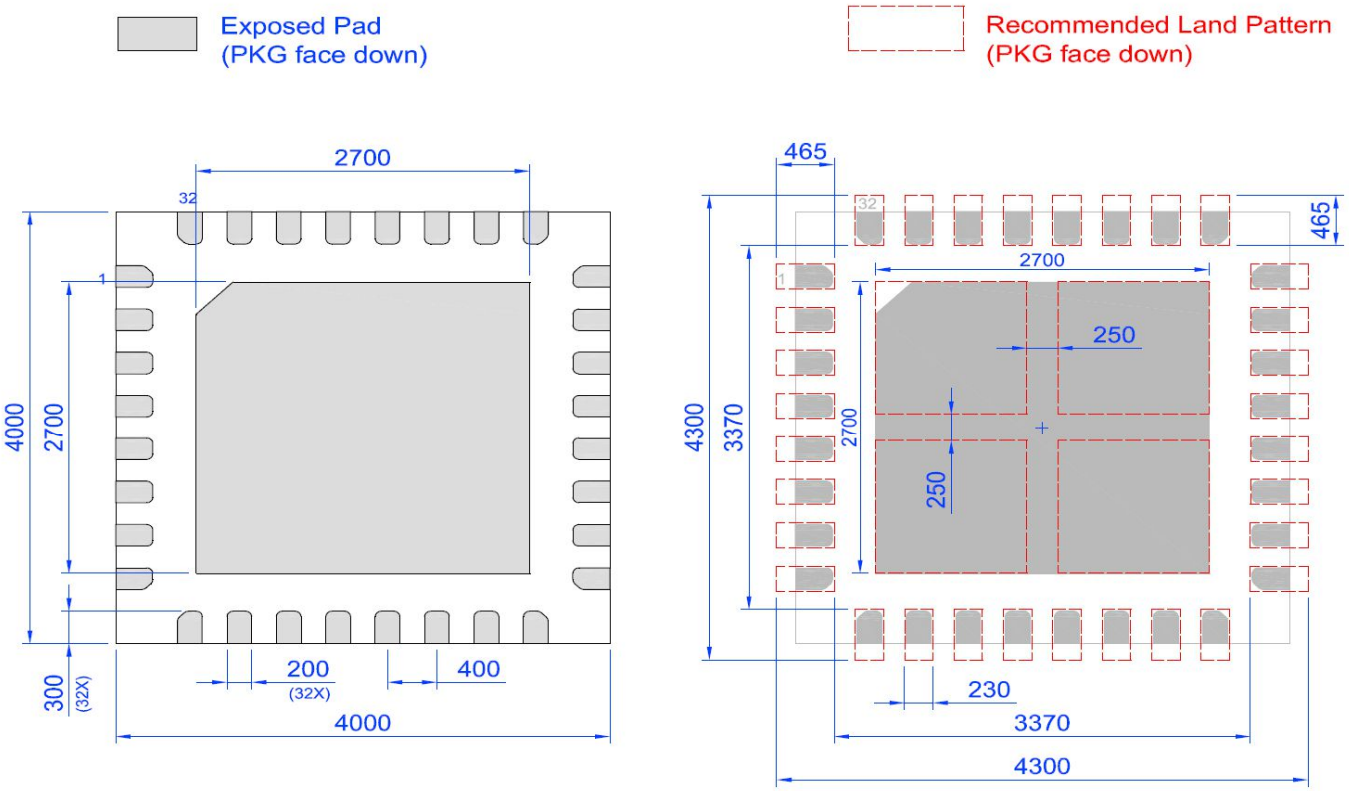


Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.85 mm^3 (nominal). More information can be found at www.jedec.org.

Layout Guidelines



Units: µm

Datasheet Revision History

Date	Version	Change
07/12/2021	0.10	The design moved to SLG46880 chip
07/21/2021	0.11	Changed Address to 0x10; Set IO expander to HIGH; Changed SDA and SCL to LVDI
07/23/2021	0.12	fixed typo in The I2C Description
07/27/2021	0.13	The Customer Edited The Design
08/13/2021	0.14	Updated DRS Table
09/23/2021	0.15	Fixed typos in pages 6, 8, 5.
02/04/2022	0.16	Updated lock status. Updated Electrical Characteristics Table.
02/23/2022	0.17	Updated Device Revision Table
02/23/2022	1.00	Production Release

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