

# ESC201A Assignment 11

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2023-2024 Semester I

## Topics

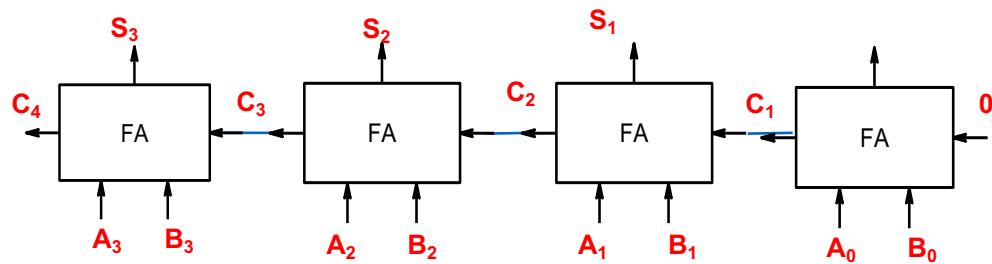
Sequential Circuits

## Questions

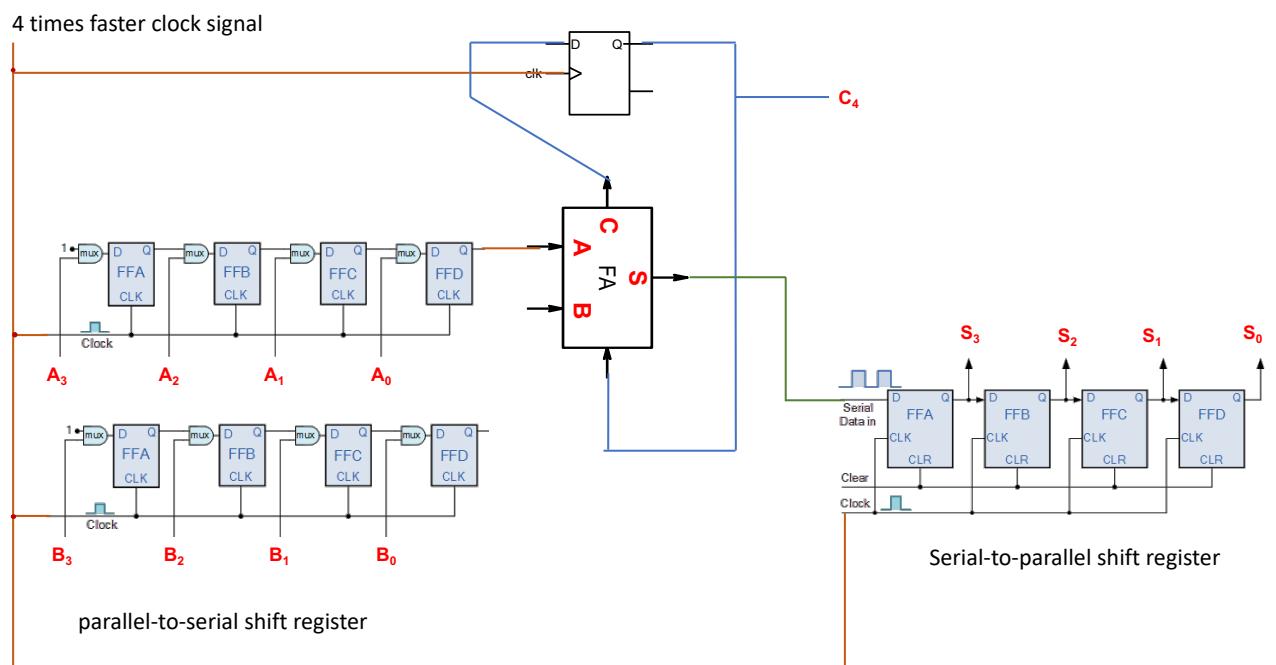
1. Consider the objective of designing a 4 bit adder. Show a combinatorics circuit which can add two 4 bit numbers with the help of multiple single bit full adders. Now, let us design a sequential circuit with the help of only one single bit adder and D FFs.

## Solution

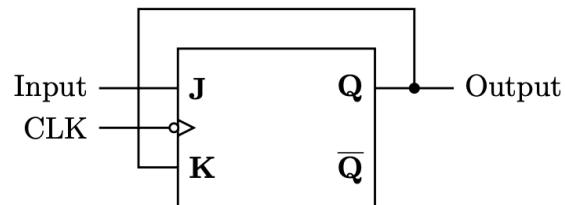
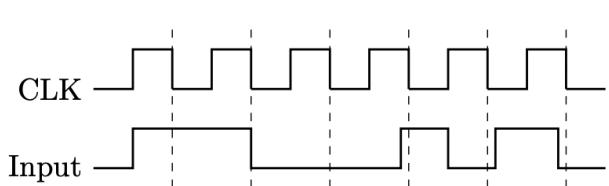
### combinatorics circuit



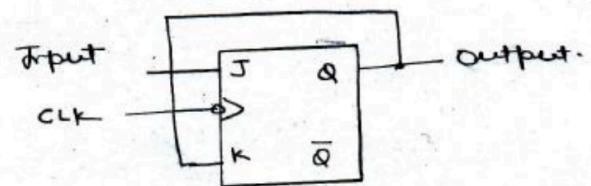
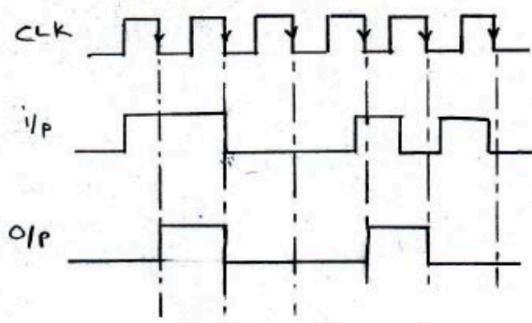
### Sequential Circuit



2. The waveform of the clock as shown below excites the circuit shown. Sketch the output waveform.



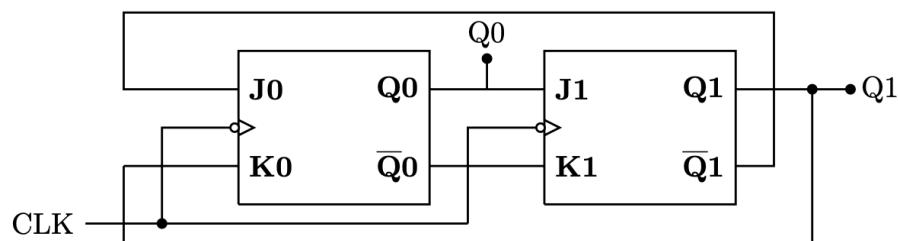
$\because$  J-K flip flop is -ve edge triggered.



$\therefore$  for J-K flip flop  
 $Q(t+1) = J\bar{Q} + \bar{K}Q$ .

$$\therefore K = Q \rightarrow \bar{Q}Q = 0 \\ \Rightarrow Q(t+1) = J\bar{Q}$$

3. If initially  $Q_0 = Q_1 = 0$ , find the logic states of  $Q_0$  and  $Q_1$  immediately after 777<sup>th</sup> clock pulse.



The logic states for successive clock pulses are shown below.

	$Q_0$	$Q_1$	$J_0$	$K_0$	$J_1$	$K_1$	$Q_0(n+1)$	$Q_1(n+1)$
After 1 <sup>st</sup> clock	0	0	1	0	0	1	1	0
After 2 <sup>nd</sup> clock	1	0	1	0	1	0	1	1
After 3 <sup>rd</sup> clock	1	1	0	1	1	0	0	1
After 4 <sup>th</sup> clock	0	1	0	1	0	1	0	1
After 5 <sup>th</sup> clock	0	0	1	0	0	1	0	0
After 6 <sup>th</sup> clock	1	0	1	0	1	0	1	1

The above logic states reveal that after every 4 clock pulses the states will repeat.

NOW,

$$777 = (194 \times 4) + 1$$

This implies after 777<sup>th</sup> clock pulse we arrive at

$$Q_0 \cdot Q_1 = 10.$$

4. A PN flip-flop has four operations, reset to 0, hold, complement and set to 1 when inputs PN are 00,01,10,11 respectively. Tabulate the characteristic table, excitation table and show how the PN FF can be converted to a D FF.

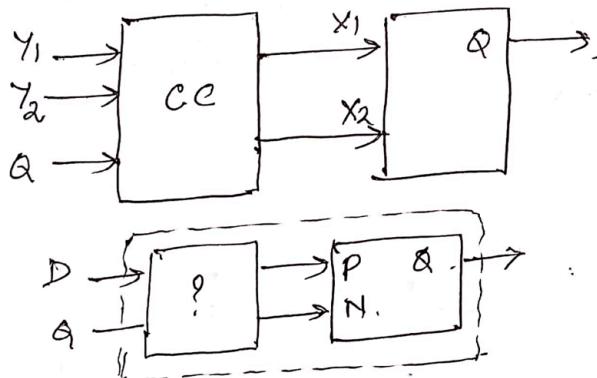
SOTW. Characteristic Table

P	N	$Q(t+1)$	State
0	0	0	Reset
0	1	$Q(t)$	Hold
1	0	$\bar{Q}(t)$	Toggle
1	1	1	Set

Excitation Table

$Q(t)$	$Q(t+1)$	P	N
0	0	0	X
0	1	1	X
1	0	X	0
1	1	X	1

General ckt for converting a FF with 2/Ps.  
 $x_1, x_2$  into a different FF with inputs  $y_1, y_2$

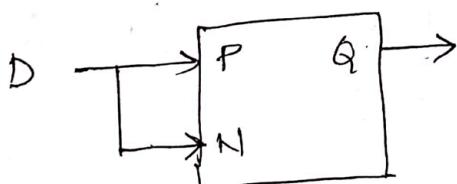


D	Q	$Q(t+1)$	P	N
0	0	0	0	X
0	1	0	X	0
1	0	1	1	X
1	1	1	1	1

$$P = D$$

$$N = \bar{D}$$

So, PN FF can be converted to a D FF by



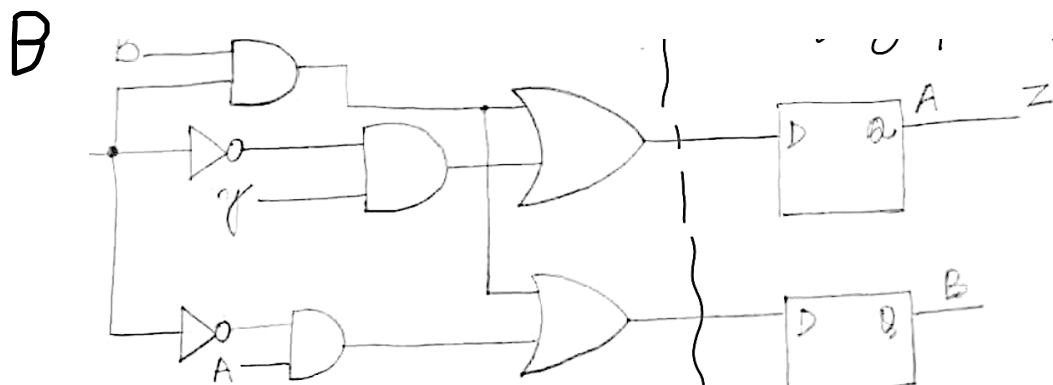
5. A sequential circuit with two flip-flops A and B, two inputs x, y and a output z has the following behavior:

$$A(t+1) = x.y + x.B;$$

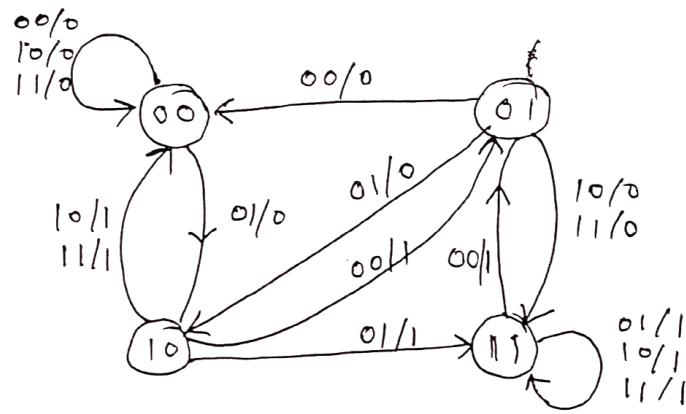
$$B(t+1) = x.A + x.B;$$

$$z = A$$

Draw the logic diagram of the circuit, list the state table and draw the state transition graph.

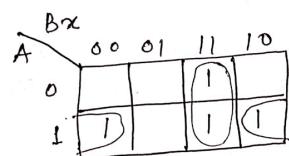


$A_t$	$B_t$	Input		Next State		$z$	
		$x$	$y$	$A_{t+1}$	$B_{t+1}$		
0	0	0	0	0	0	0	
0	0	0	1	1	0	0	
0	0	1	0	0	0	0	
0	0	1	1	0	0	0	
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0	1	0	0	0	0	0	
0	1	0	1	1	0	0	
0	1	1	0	1	1	0	
0	1	1	1	1	1	0	
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1	0	0	0	0	1	1	
1	0	0	1	1	1	1	
1	0	1	0	0	0	1	
1	0	1	1	0	0	1	
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1	1	0	0	0	1	1	
1	1	0	1	1	1	1	
1	1	1	0	1	1	1	
1	1	1	1	1	1	1	

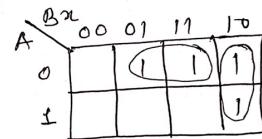


6. Design a sequential circuit with two D flip-flops A and B and one input x such that when  $x = 0$ , the state of the circuit remains the same. When  $x = 1$ , the circuit goes through the state transitions from 00 to 01, to 11, to 10 and back to 00, and repeats.

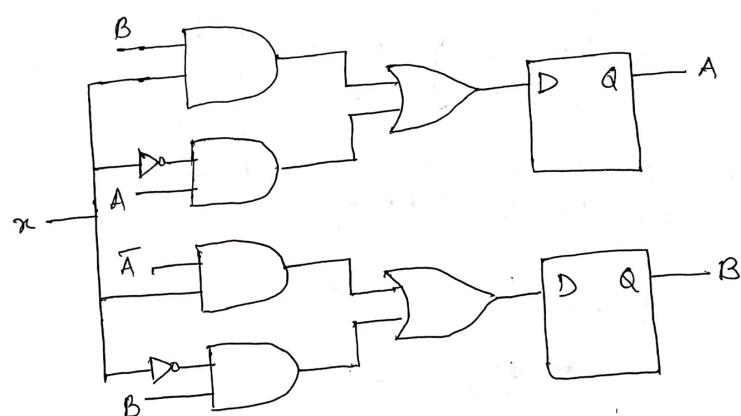
Present State		$\Delta P$	Next State		$D_A$	$D_B$
$A_t$	$B_t$	$x$	$A_{t+1}$	$B_{t+1}$		
0	0	0	0	0	0	0
0	0	1	0	1	0	1
0	1	0	0	1	0	1
0	1	1	1	1	1	1
1	0	0	1	0	1	0
1	0	1	0	0	0	0
1	1	0	1	1	1	1
1	1	1	1	0	1	0



$$D_A = \bar{A}\bar{x} + Bx$$

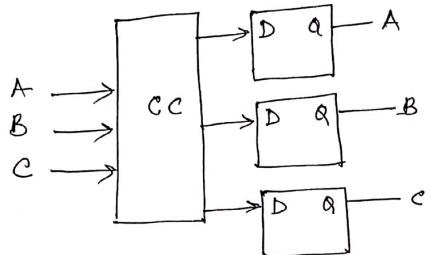


$$D_B = \bar{A}\bar{x} + B\bar{x}$$



7. Design a synchronous counter that goes through the following repeating sequence 0, 2, 1, 4, 3, 6, 5, 7.

Q4 There are 8 states, so 3 FFs are required.  
Soln. Let the FFs be D type.



State transition table.

Present State			Next State			D <sub>A</sub>	D <sub>B</sub>	D <sub>C</sub>
A	B	C	A	B	C			
0	0	0	0	1	0	0	1	0
0	1	0	0	0	1	0	0	1
0	0	1	1	0	0	1	0	0
1	0	0	0	1	1	0	1	1
0	1	1	1	1	0	1	1	0
1	1	0	1	0	1	1	0	1
1	0	1	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0

$$D_A = C \cdot (\overline{A} \cdot \overline{B}) + \overline{C} \cdot (AB)$$

$$D_B = B \cdot (A + \overline{C}) + \overline{B} \cdot (A + \overline{C})$$

$$D_C = A\overline{B} + B\overline{C}$$

