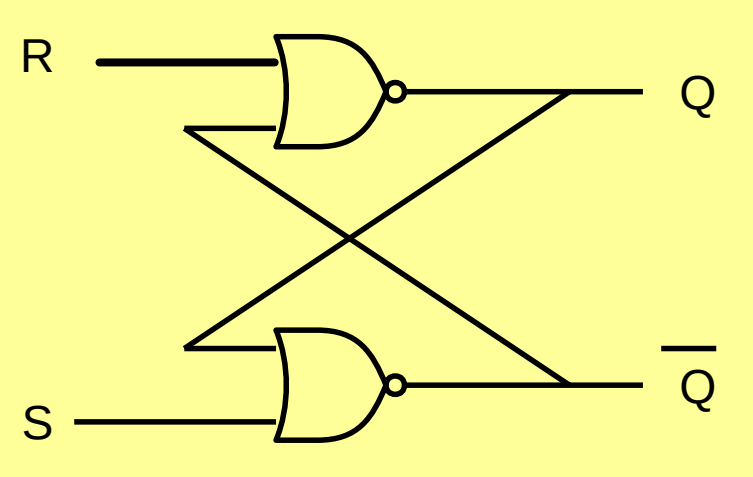
# ESc201 : Introduction to Electronics

## Sequential Circuits

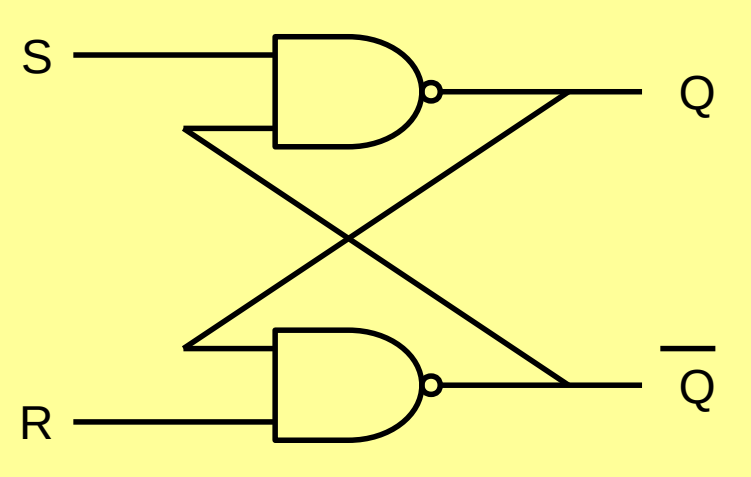
Amit Verma
Dept. of Electrical Engineering
IIT Kanpur

# SR latch (recap)



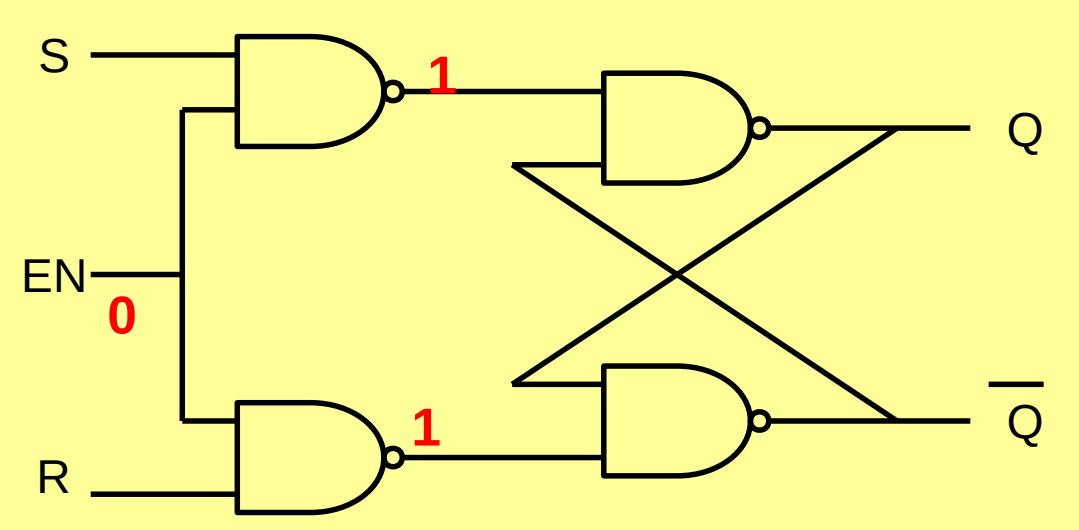

| S | R | Q | $\overline{Q}$ | State |
|---|---|---|---|---|
| 1 | 0 | 1 | 0 | SET |
| 0 | 1 | 0 | 1 | RESET |
| 0 | 0 | Q | $\overline{Q}$ | HOLD |
| 1 | 1 | 0 | 0 | INVALID |

# NAND Latch (recap)

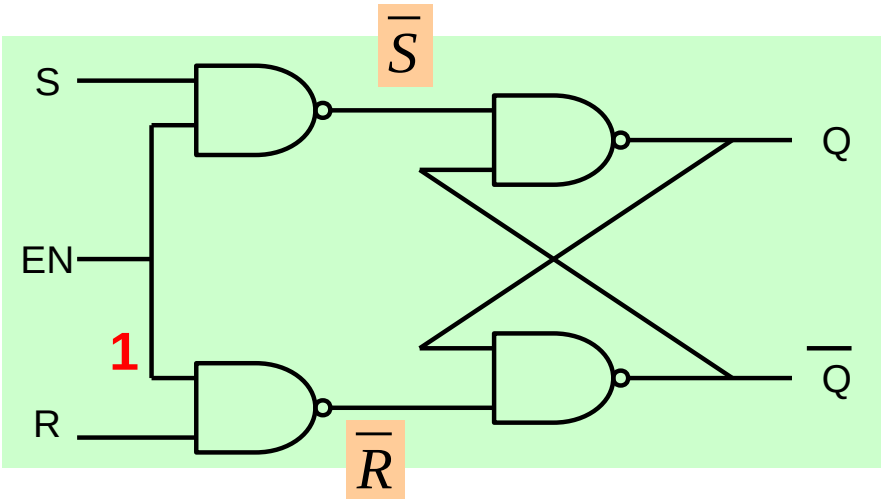



| S | R | Q | $\overline{Q}$ | State |
|---|---|---|---|---|
| 0 | 1 | 1 | 0 | SET |
| 1 | 0 | 0 | 1 | RESET |
| 1 | 1 | Q | $\overline{Q}$ | HOLD |
| 0 | 0 | 1 | 1 | INVALID |

# RS NAND Latch with Enable (recap)

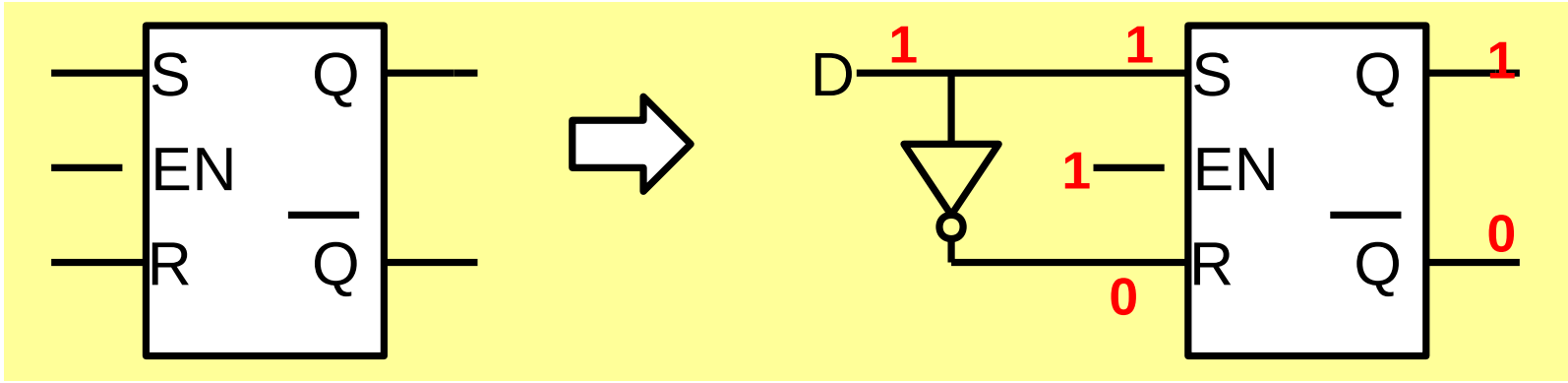



**Hold State**

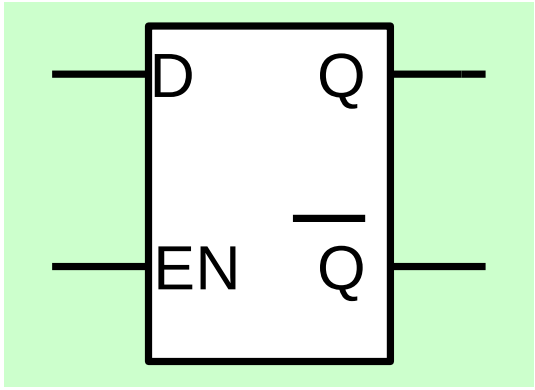



| Enable | S R | Q $\overline{Q}$ | State |
|---|---|---|---|
| 0 | x x | Q $\overline{Q}$ | Hold |
| 1 | 1 0 | 1 0 | Set |
| 1 | 0 1 | 0 1 | Reset |
| 1 | 0 0 | Q $\overline{Q}$ | Hold |
| 1 | 1 1 | 0 0 | Invalid |

# D latch (recap)

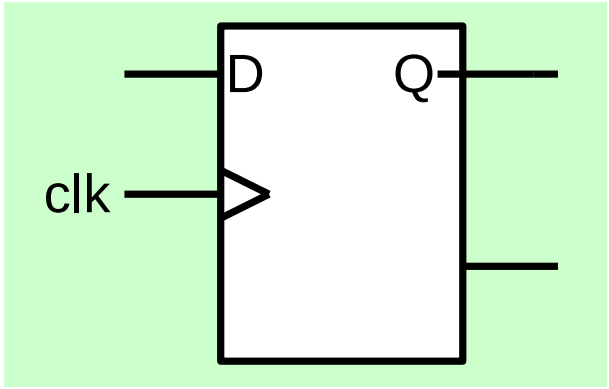


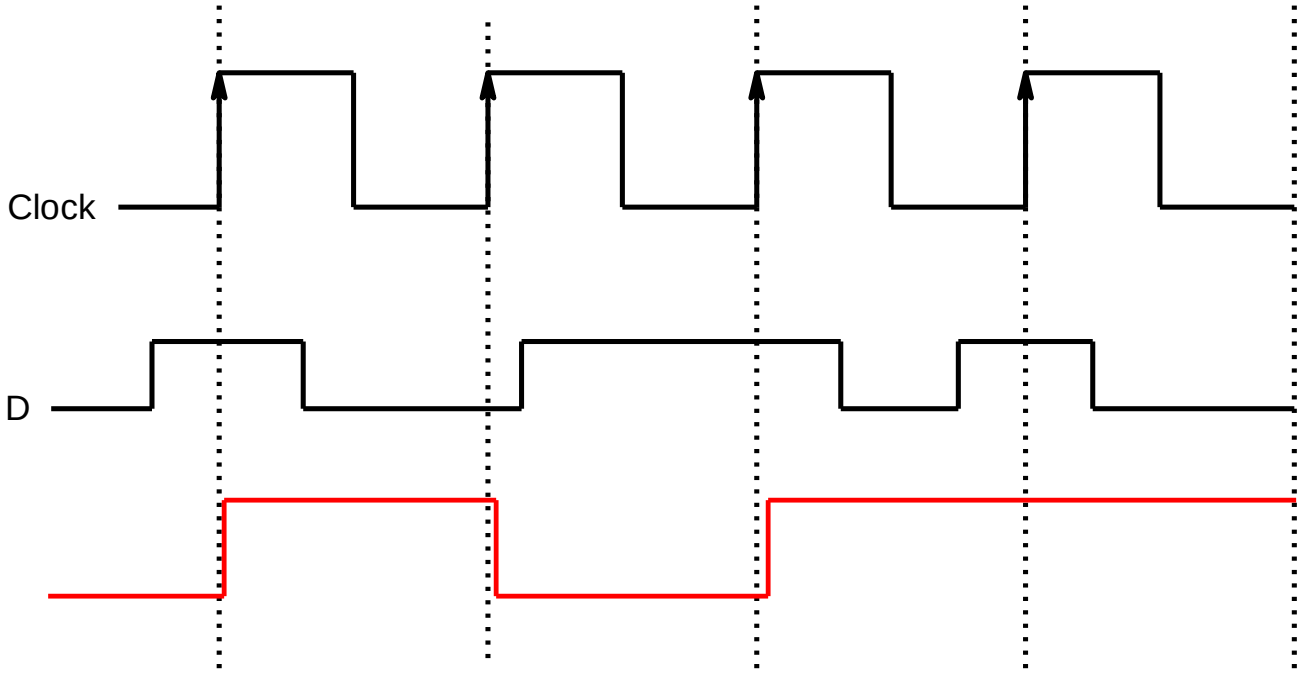

| Enable | S | R | Q | $\overline{Q}$ | State |
|---|---|---|---|---|---|
| 0 | x | x | Q | $\overline{Q}$ | Hold |
| 1 | 1 | 0 | 1 | 0 | Set |
| 1 | 0 | 1 | 0 | 1 | Reset |
| 1 | 0 | 0 | Q | $\overline{Q}$ | Hold |
| 1 | 1 | 1 | 0 | 0 | Invalid |




If EN = 1 then Q = D otherwise the latch is in Hold state

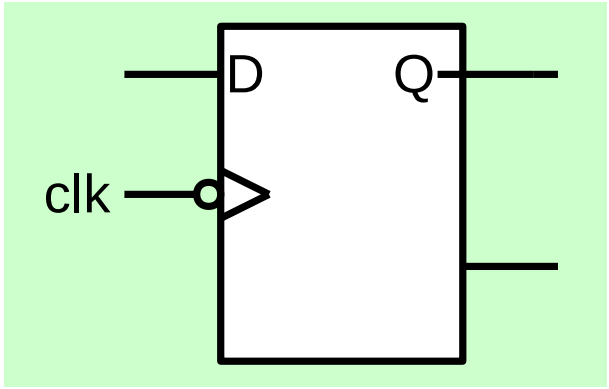
# Edge Triggered Latch or Flip-flop (recap)

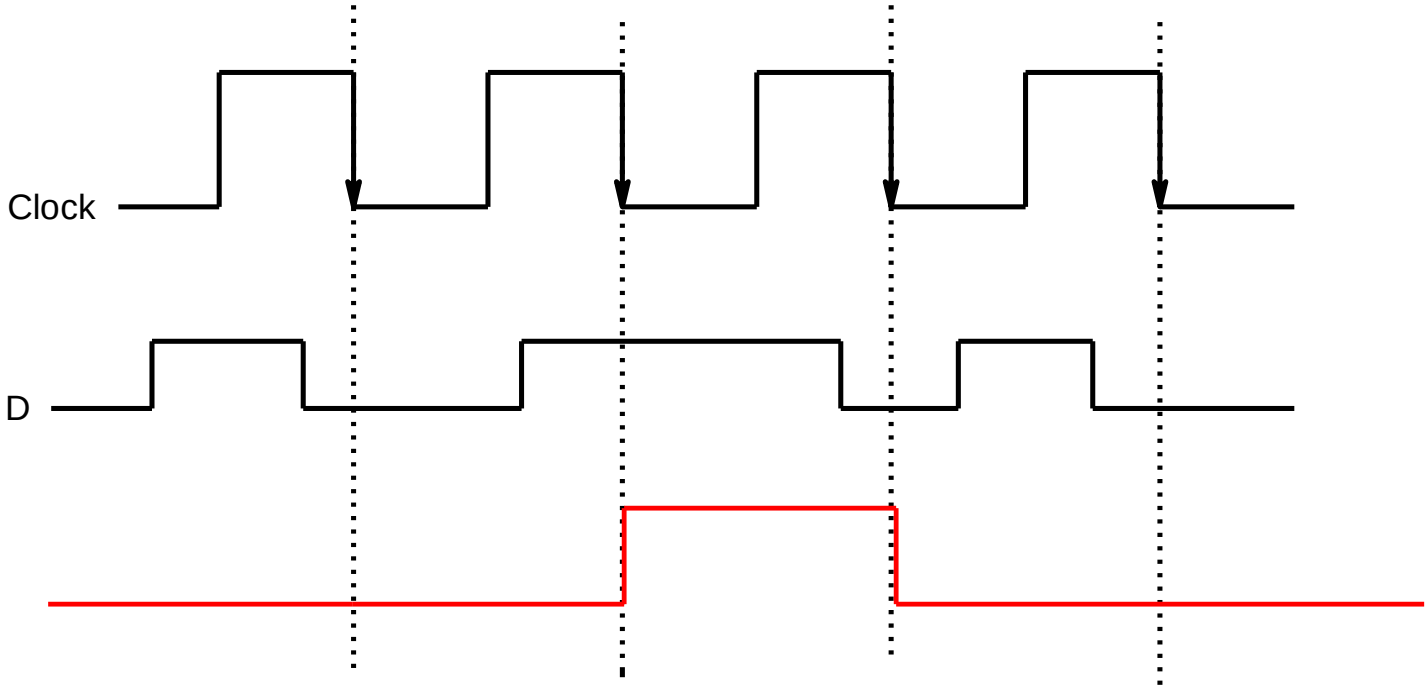



**Positive edge triggered flipflop**

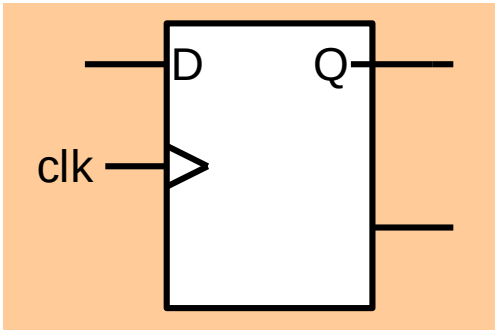
# Negative Edge Triggered Latch or Flip-flop (recap)



# Characteristic table (recap)

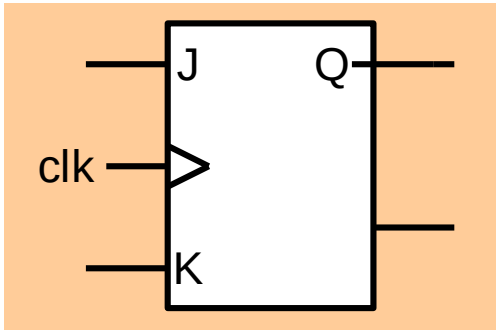
Given a input and the present state of the flip-flop, what is the next state of the flip-flop




| Inputs (D) | Q(t+1) |
|---|---|
| 0 | 0 |
| 1 | 1 |

**Characteristic equation:** $Q(t+1) = D$

## JK Flip-flop



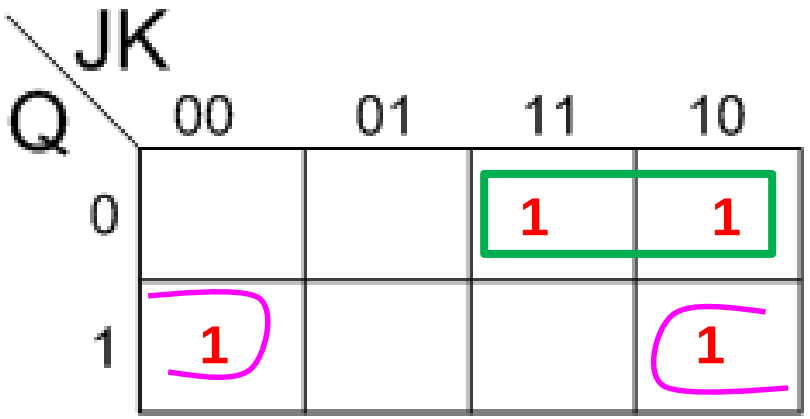

| Inputs J | K | Q(t+1) |
|---|---|---|
| 0 | 0 | Q(t) |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | $\overline{Q(t)}$ |

**Characteristic equation:** $Q(t+1) = J\overline{Q}(t) + \overline{K}Q(t)$

**JK flip flop is refinement of RS flip flop where indeterminate state of RS flip flop is defined in JK Flip Flop**

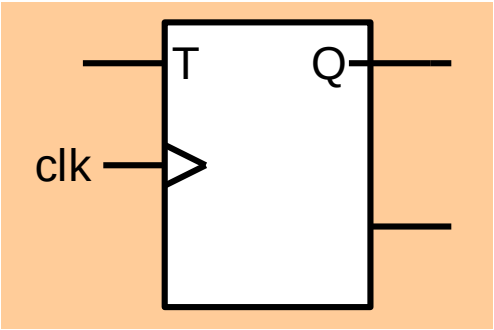
# JK Flip-flop (characteristic equation)

| Q | J | K | Q(t+1) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |




$$Q(t+1) = J\overline{Q}(t) + \overline{K}Q(t)$$

# Toggle or T Flip-flop (recap)

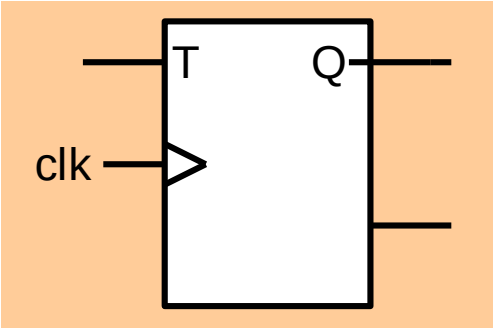



| Inputs (T) | Q(t+1) |
|---|---|
| 0 | Q(t) |
| 1 | $\overline{Q(t)}$ |

**Characteristic equation:** $Q(t+1) = T \oplus Q(t)$

| T | Q(t) | Q(t+1) |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# Toggle or T Flip-flop (recap)




| Inputs (T) | Q(t+1) |
|---|---|
| 0 | Q(t) |
| 1 | $\overline{Q(t)}$ |

**Characteristic equation:** $Q(t+1) = T \oplus Q(t)$

# Excitation Table

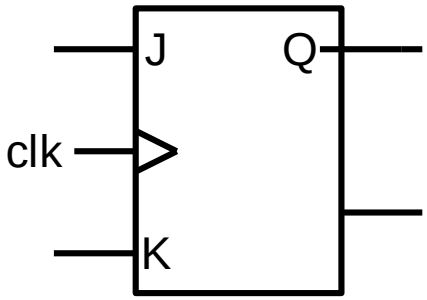
What inputs are required to effect a particular state change

| Q | T | Q(t+1) |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Excitation Table**

| Q(t) | Q(t+1) | Inputs T |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

# JK Flip-flop excitation table (recap)




| J | K | Q(t+1) |
|---|---|---|
| 0 | 0 | Q(t) |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | $\overline{Q(t)}$ |

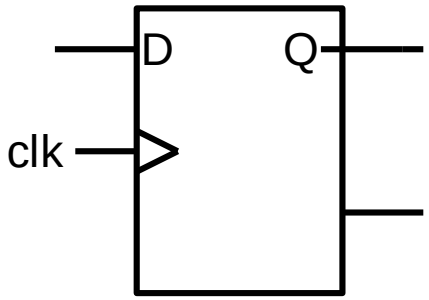
**Characteristic Table**

| Q | J | K | Q(t+1) |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 |
| 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

| Q(t) | Q(t+1) | Inputs J | K |
|---|---|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

**Excitation Table**

# D Flip flop excitation table




| D | Q(t+1) |
|---|---|
| 0 | 0 |
| 1 | 1 |

**Characteristic Table**

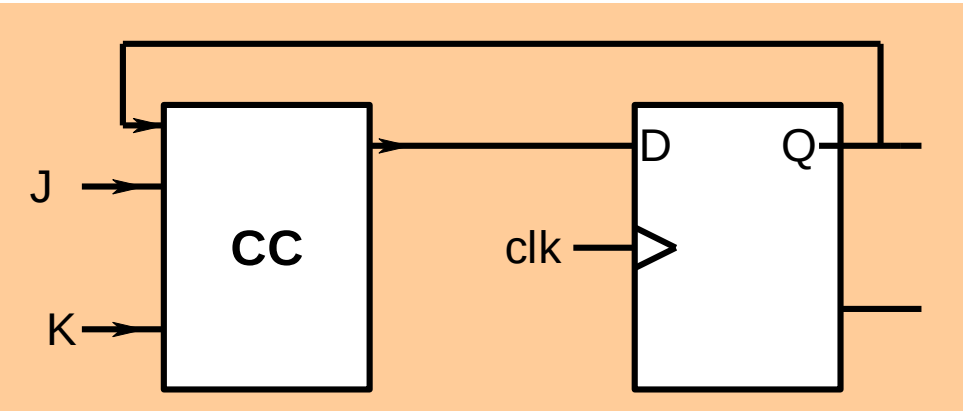
| Q | D | Q(t+1) |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

Inputs

| Q(t) | Q(t+1) | D |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Excitation Table**

# Convert a D FF to JK FF




| J | K | Q | Q(t+1) | D |
|---|---|---|---|---|
| 0 | X | 0 | 0 | 0 |
| 1 | X | 0 | 1 | 1 |
| X | 1 | 1 | 0 | 0 |
| X | 0 | 1 | 1 | 1 |

Inputs

| Q(t) | Q(t+1) | J | K |
|---|---|---|---|
| 0 | 0 | 0 | X |
| 0 | 1 | 1 | X |
| 1 | 0 | X | 1 |
| 1 | 1 | X | 0 |

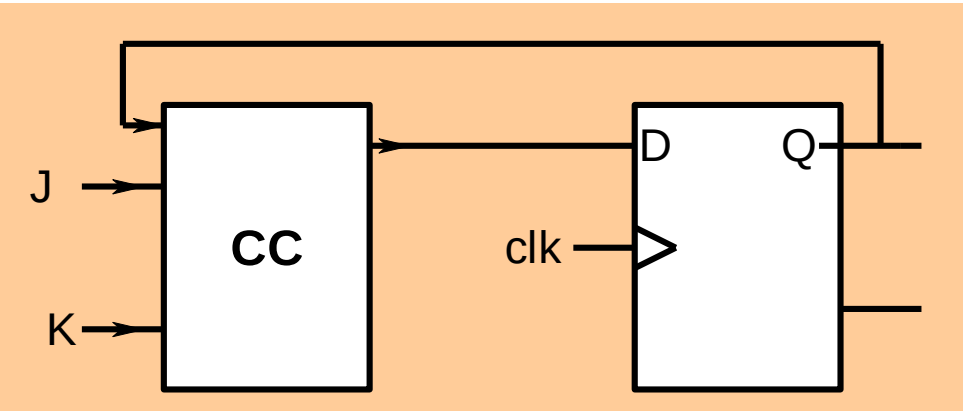
**Excitation Table**

Inputs

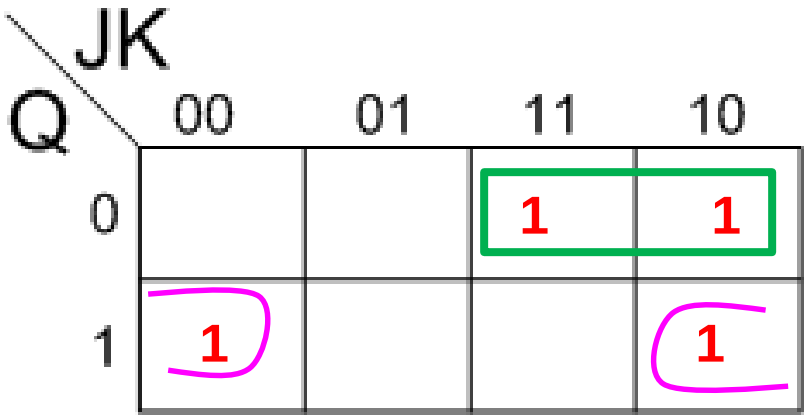
| Q(t) | Q(t+1) | D |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 0 |
| 1 | 1 | 1 |

**Excitation Table**

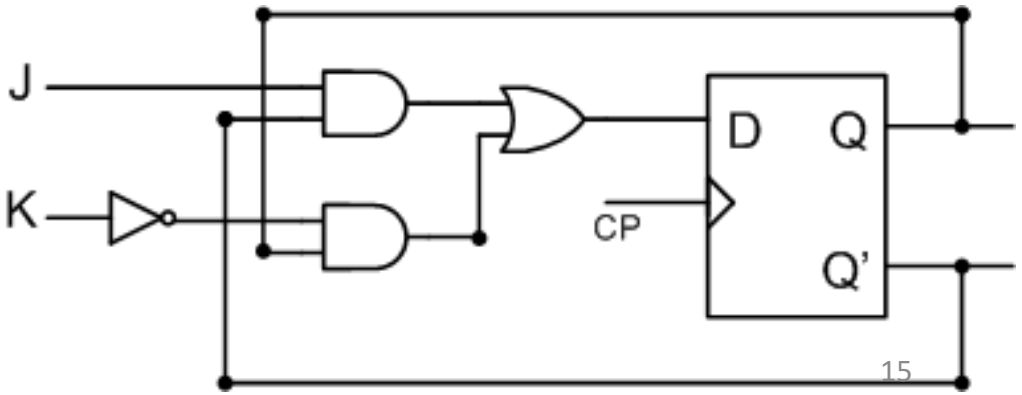
# Convert a D FF to JK FF




| J | K | Q | Q(t+1) | D |
|---|---|---|---|---|
| 0 | X | 0 | 0 | 0 |
| 1 | X | 0 | 1 | 1 |
| X | 1 | 1 | 0 | 0 |
| X | 0 | 1 | 1 | 1 |

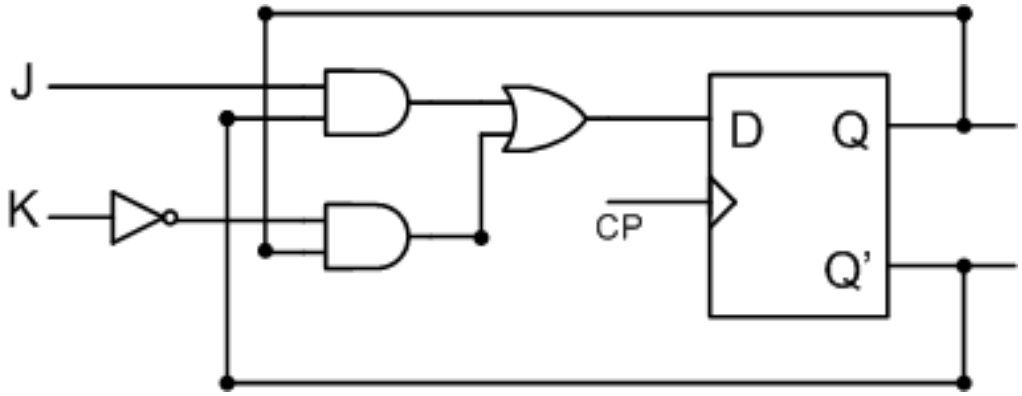



$$D = \overline{Q}.J + Q.\overline{K}$$



# Convert a D FF to JK FF

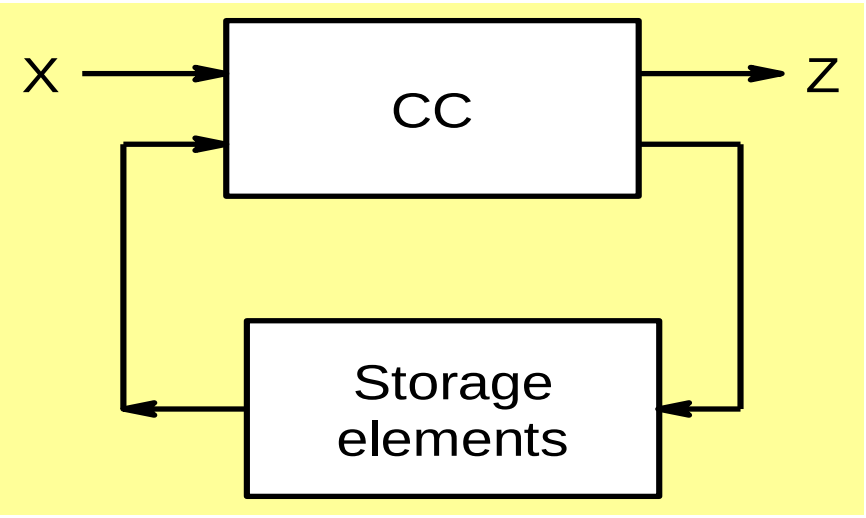
$$D = \overline{Q}.J + Q.\overline{K}$$




| Q | J | K | D | Q(t+1) |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 0 |
| 0 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | 0 |
| 1 | 1 | 0 | 1 | 1 |
| 1 | 1 | 1 | 0 | 0 |

| Inputs J | K | Q(t+1) |
|---|---|---|
| 0 | 0 | Q(t) |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | $\overline{Q(t)}$ |

# Sequential Circuits

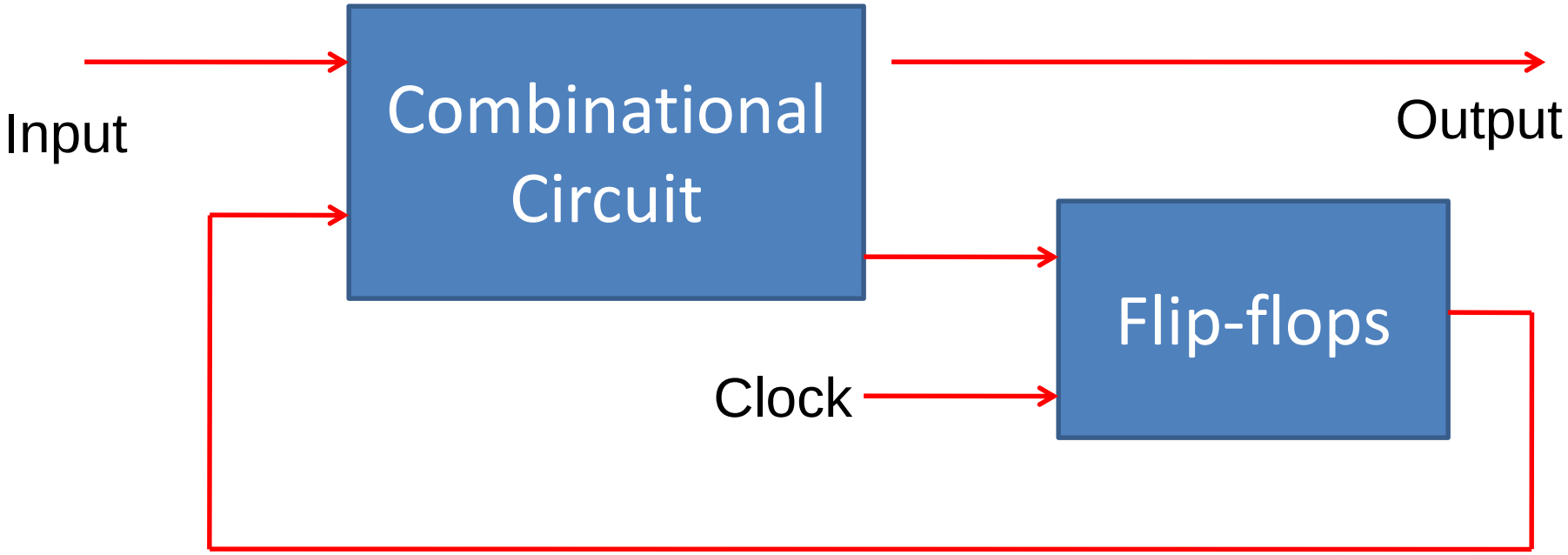



The binary information stored in the storage elements at any given time defines the ***state*** of the sequential circuit at that time

Output is a function of input as well as the present state of the storage elements.

Next state is also a function of the present state and the external inputs.

# Synchronous Sequential Circuits

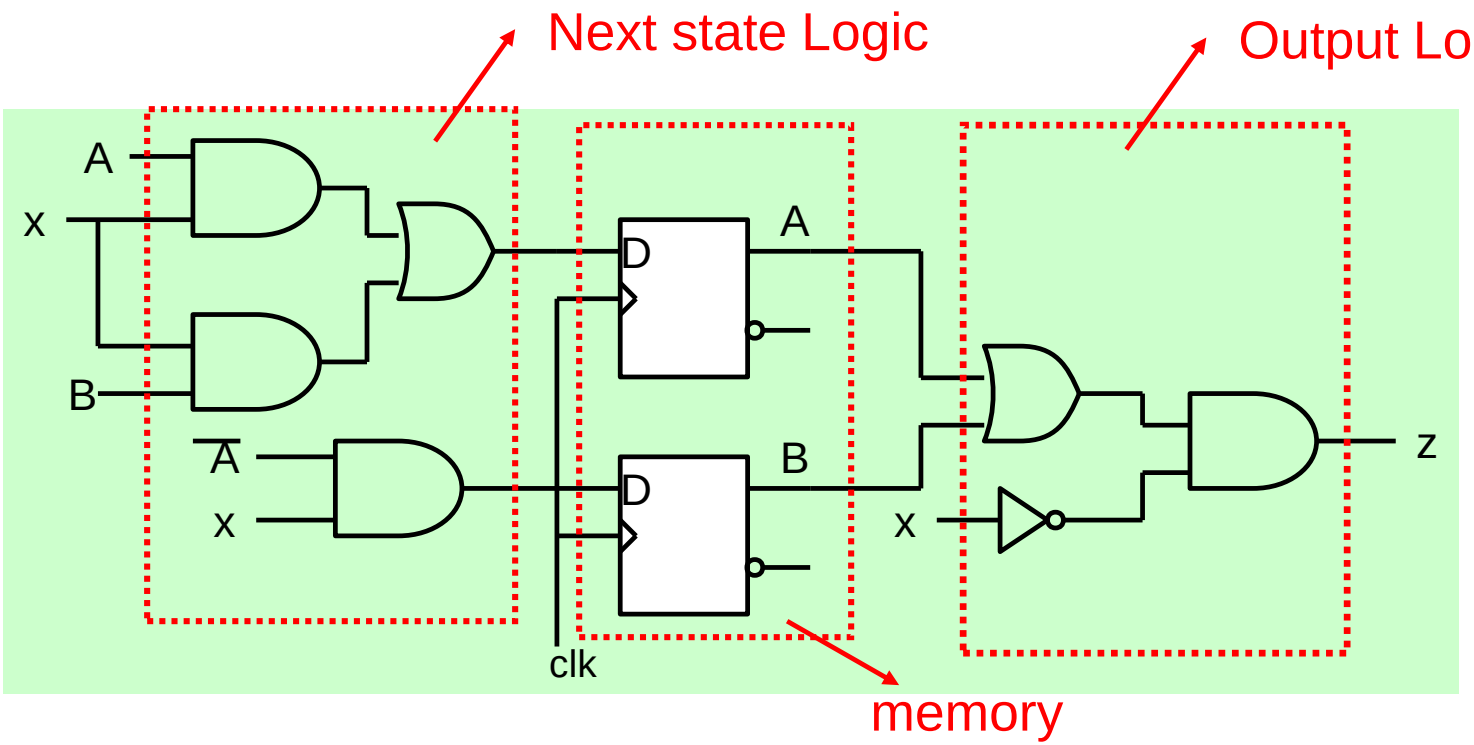



Employs signals that affect the storage elements only at discrete instants of time.

Synchronization is achieved via the ***clock pulses***.

**Synchronous Clocked Sequential Circuits**

# Analysis



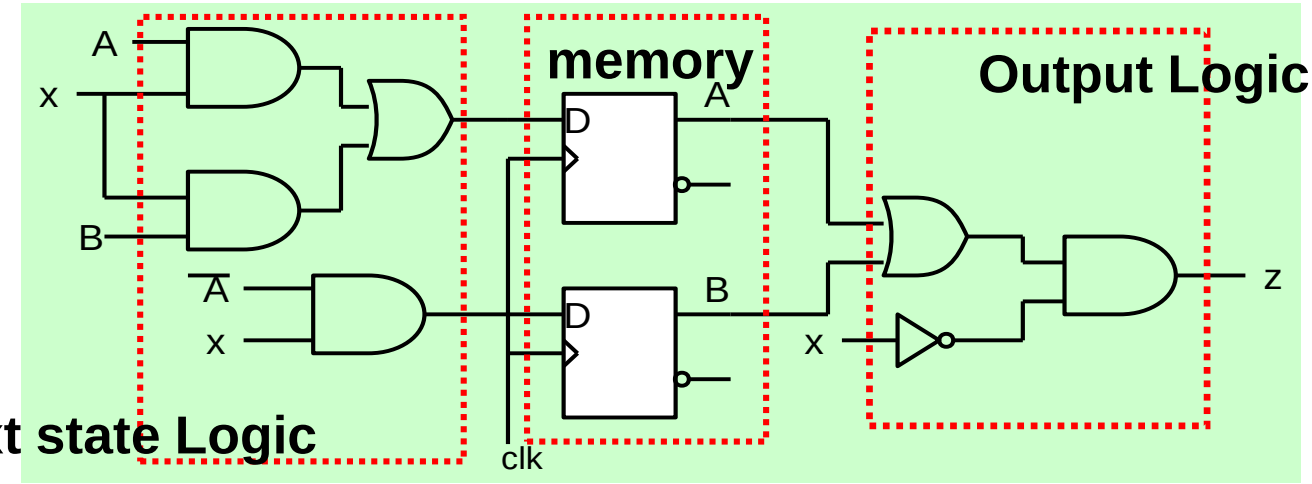

Output z depends on the input x and on the state of the memory (A,B)

The memory has 2 FFs and each FF can be in state 0 or 1. Thus there are four possible states: AB: 00,01,10,11.

To describe the behavior of a sequential circuit, we need to show

1. How the system goes from one memory state to the next as the input changes
2. How the output responds to input in each state

# Analysis of Sequential Circuits




$$D_A = A.x + B.x \;\; ; \; D_B = \overline{A}.x ; z = (A + B).\overline{x}$$

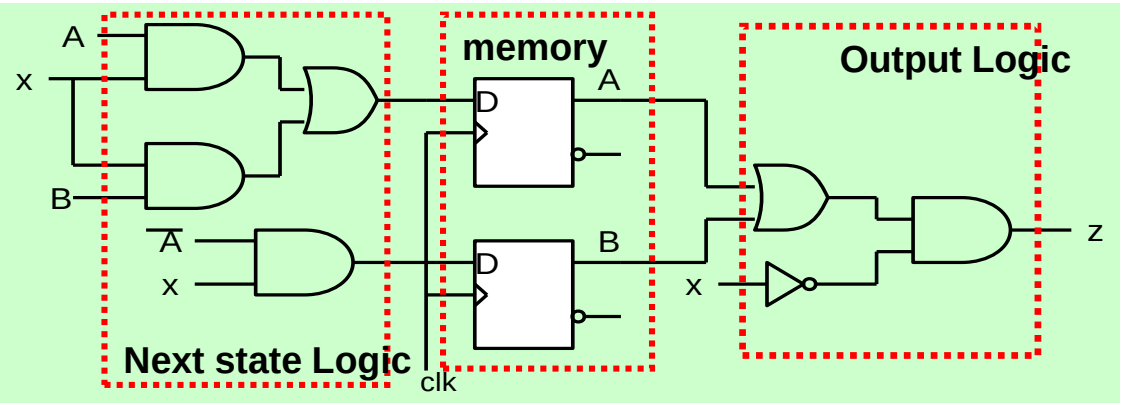
State Transition Table

| Present State A | Present State B | Input x | Next State A | Next State B | Output z |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |

$$A(t+1) = A(t).x + B(t).x$$

$$B(t+1) = \overline{A(t)}.x$$

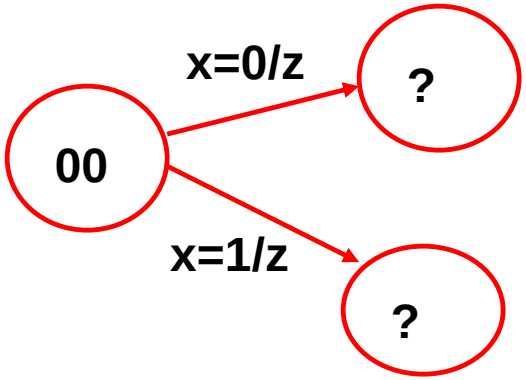
$$z = (A + B).\overline{x}$$




State Transition Table

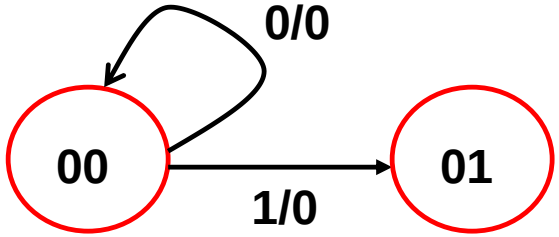
| Present State A | Present State B | Input x | Next State A | Next State B | Output z |
|---|---|---|---|---|---|
| 0 | 0 | 0 | **0** | **0** | **0** |
| 0 | 0 | 1 | **0** | **1** | **0** |
| 0 | 1 | 0 | **0** | **0** | **1** |
| 0 | 1 | 1 | **1** | **1** | **0** |
| 1 | 0 | 0 | **0** | **0** | **1** |
| 1 | 0 | 1 | **1** | **0** | **0** |
| 1 | 1 | 0 | **0** | **0** | **1** |
| 1 | 1 | 1 | **1** | **0** | **0** |


Memory state in which FF A& B have output values 00

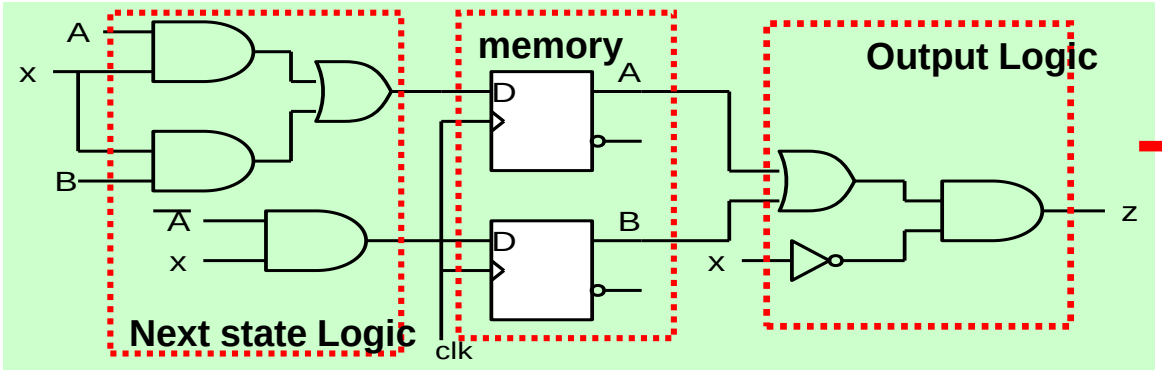



If x = 0 then z = 0, When the clock edge comes the system would stay in 00 state.

If x = 1 then z = 0. When the clock edge comes the system would go to 01 state.



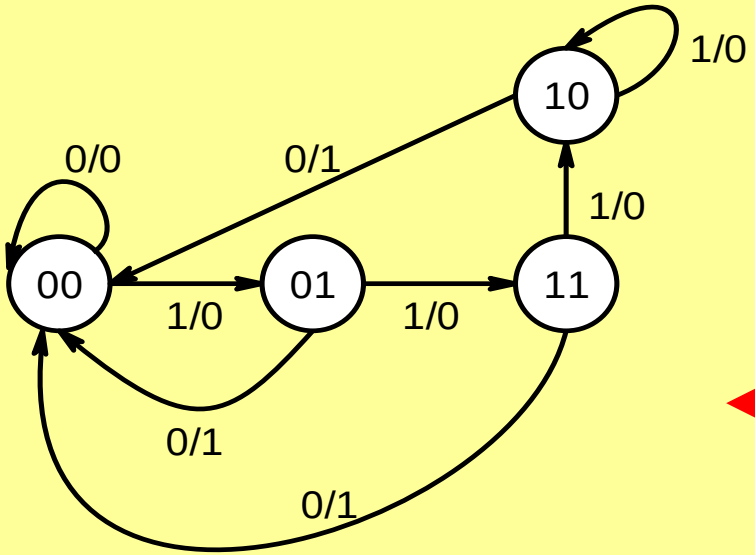
# Analysis of Sequential Circuits




$$A(t+1) = A(t).x + B(t).x$$

$$B(t+1) = \overline{A(t)}.x$$

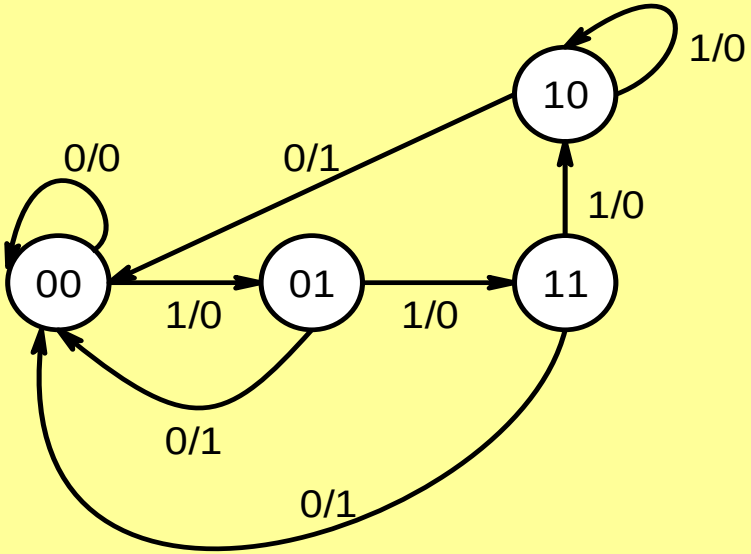
$$z = (A+B).\overline{x}$$



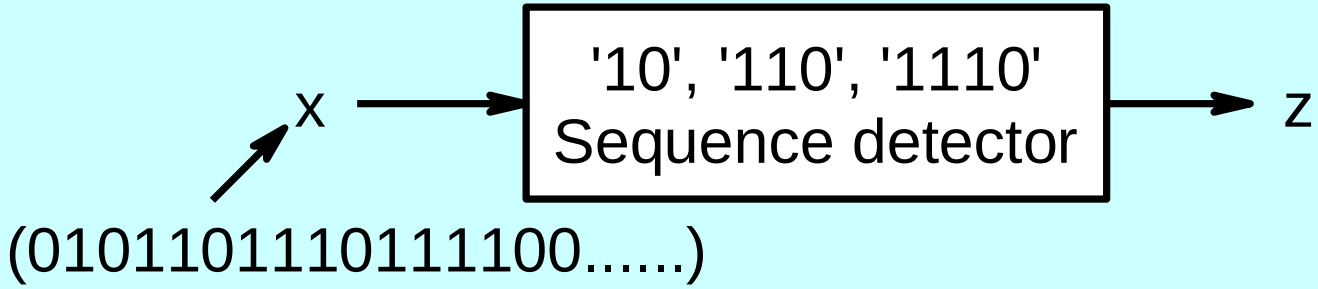

State transition Graph

State Transition Table

| Present State A | Present State B | Input x | Next State A | Next State B | Output z |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 |
| 1 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 |




**State transition Graph**



# Quiz-2 Solution Discussion