ESC201A Quiz3 Set A

SAMYAK SINGHANIA

TOTAL POINTS

8 / 10

QUESTION 1

Q1 5 pts

1.1 Q1(a) **2 / 3**

- **+ 3 pts** Completely Correct
- **+ 0 pts** Completely Incorrect
- **+ 0 pts** Not Attempted
- **+ 0 pts** Copied
- ✓ **+ 1 pts** *4-bit 2's complement representation correct for both numbers*
- **+ 0.5 pts** 4-bit addition performed correctly
- **+ 0.5 pts** Identified problem correctly
- ✓ **+ 1 pts** *5-bit representation and addition correct*

1.2 Q1(b) **2 / 2**

- ✓ **+ 2 pts** *Completely Correct*
- **+ 0 pts** Completely Incorrect
- **+ 0 pts** Not Attempted
- **+ 0 pts** Copied
- **+ 1 pts** Solution correct but not minimal

QUESTION 2

2 Q2 **4 / 5**

- **+ 5 pts** Correct
- **+ 0 pts** Completely Incorrect
- **+ 0 pts** Not Attempted
- **+ 0 pts** Copied
- ✓ **+ 2.5 pts** *Excitation table for given flip flop completely correct*
- ✓ **+ 1.5 pts** *Assignment to input terminals of flip flop correct*
- **+ 1 pts** Implementation of D flip correct with minimal gates

ESC201A: Introduction to Electronics, Quiz -3 (Set-A) **Date: 10.11.2022**

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Q.1(a) Carry out the operation -5-6 using 4-bit 2's complement representation. Do you get the right answer? If not, what is the problem ?. [3 Marks]

$(5)_{10} = (0101)_2$

↳ signed bit representing positive.

$\therefore -5 =$ 2's complement of $5 = 1010 + 1 = 1011$

$(6)_{10} = (0110)_2$

$-6 = 1001 + 1 = 1010$

$\Rightarrow -5-6 = (-5) + (-6)$

$-5-6 = (-5) + (-6)$

$1011 + 1010 = 10101$

$\Rightarrow$ Negative Number since signed bit is 1

Magnitude of 10101 = 2's complement $= 01010 + 1 = (01011)_2 = 11$

$\therefore -5-6 = -11$ The result is -11 & we got the right answer.

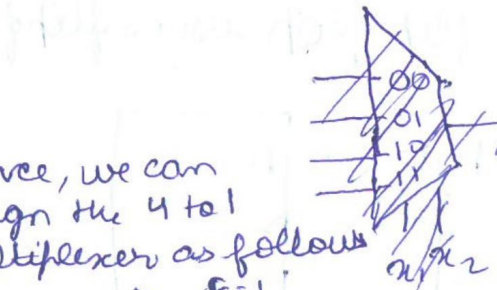
(b) Show how one can use a 4 to 1 multiplexer to implement the following 6-variable Boolean expression: $F = \overline{x_1}.\overline{x_2}.x_3 + x_1.\overline{x_2}.x_4 + \overline{x_1}.x_2.x_5 + x_1.x_2.x_6$. Use minimum number of external gates. [2 Marks]

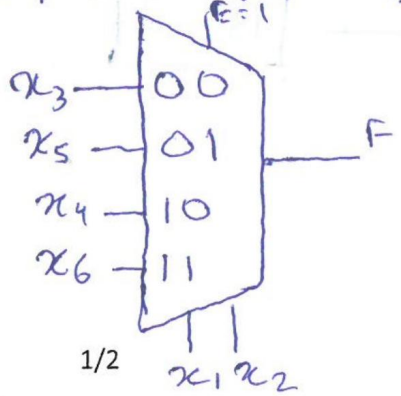
x_1	x_2	x_3	F
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	1
1	1	0	0
1	1	1	1

Design the 4 to 1 multiplexer as follows.

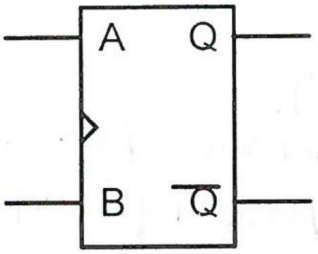
x_1	x_2	F
0	0	$F = x_3$
0	1	$F = x_5$
1	0	$F = x_4$
1	1	$F = x_6$

Hence, we can design the 4 to 1 multiplexer as follows





Q.2 The characteristic table for a flip-flop X with two inputs A and B is given below. Show how one can implement a D flip-flop using flip-flop X and basic gates. Use as few gates as possible. [5 Marks]



A	B	Q(t+1)	State
0	0	Q(t)	Hold
0	1	1	Set
1	0	0	Reset
1	1	Q(t)	Hold

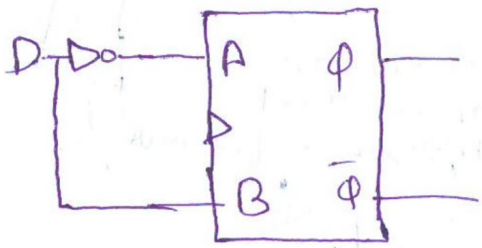
We get the following excitation table.

Q(t)	Q(t+1)	A	B	D
0	0	0 / 1	0 / 1	0
0	1	0	1	1
1	0	1	0	0
1	1	0 / 1	0 / 1	1

We know that the characteristic table for D-flip flop is

D	Q(t+1)
0	0
1	1

∴ If we choose $A = \bar{D}$ & $B = D$, we can implement D-flip flop using flipflop X.



when D = 0.
A = 1, B = 0
⇒ Q(t+1) = 0

when D = 1
A = 0, B = 1
⇒ Q(t+1) = 1