Department of Electrical Engineering, IIT Kanpur ESc 201: Introduction to Electronics

Assignment-11

1. Design a half subtractor circuit with inputs x and y and outputs Diff. and B_{out}. The circuit subtracts the bits x-y, places the result in Diff., and borrow in B_{out}.

2. Construct a 4-to-16 line decoder with five 2-to-4 line decoders with enable input.

3. (i) Implement the following function using a decoder: $F(A,B,C) = \sum(3,5,6)$

   (ii) Implement the above function using a multiplexer.

4. Construct a 16 x 1 multiplexer with two 8 to 1 and one 2 to 1 multiplexers. Use block diagrams.

5. Implement the following Boolean function using one 4 to 1 multiplexer and external gates. (Hint: Connect inputs A and B to the control or selection lines of the mux and then use basic gates to apply appropriate combinations of C & D to the input lines of the Mux.)

   $F(A,B,C,D) = \sum(1,3,4,11,12,13,14,15)$

6. (i) Implement a AND gate with a 2 to 1 MUX.

   (ii) Implement a NOT gate with a 2 to 1 MUX.

   (iii) Now implement a NAND (a universal gate) with two 2 to 1 MUX.

[So, you can actually implement any Boolean logic by combining 2 to 1 MUXs]