ESc201 : Introduction to Electronics

Counters and Registers

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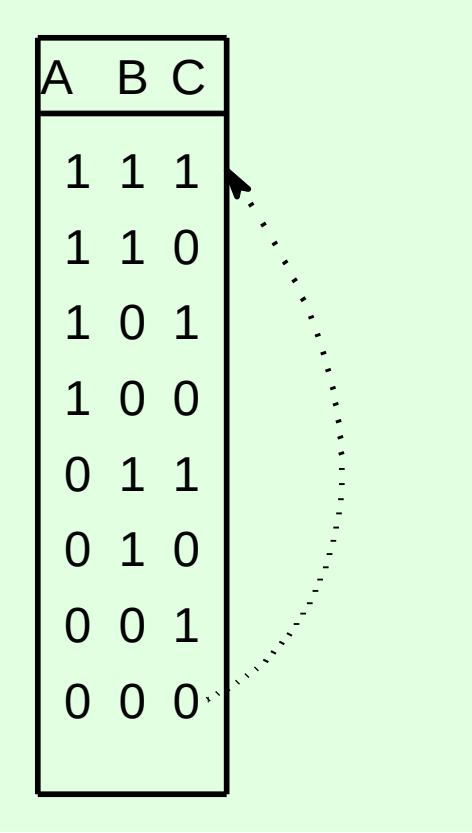
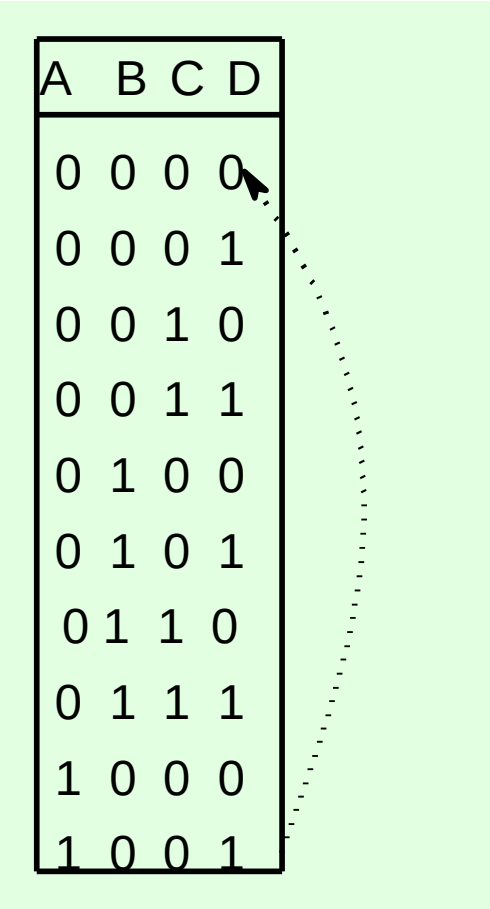
Recap: Counters

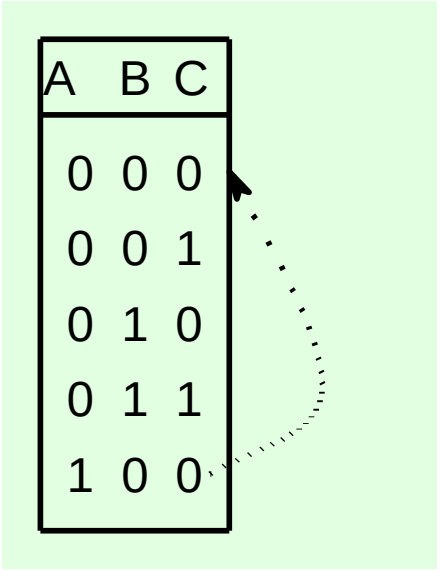


Binary down counter



Decade counter

Modulo-10 Counter



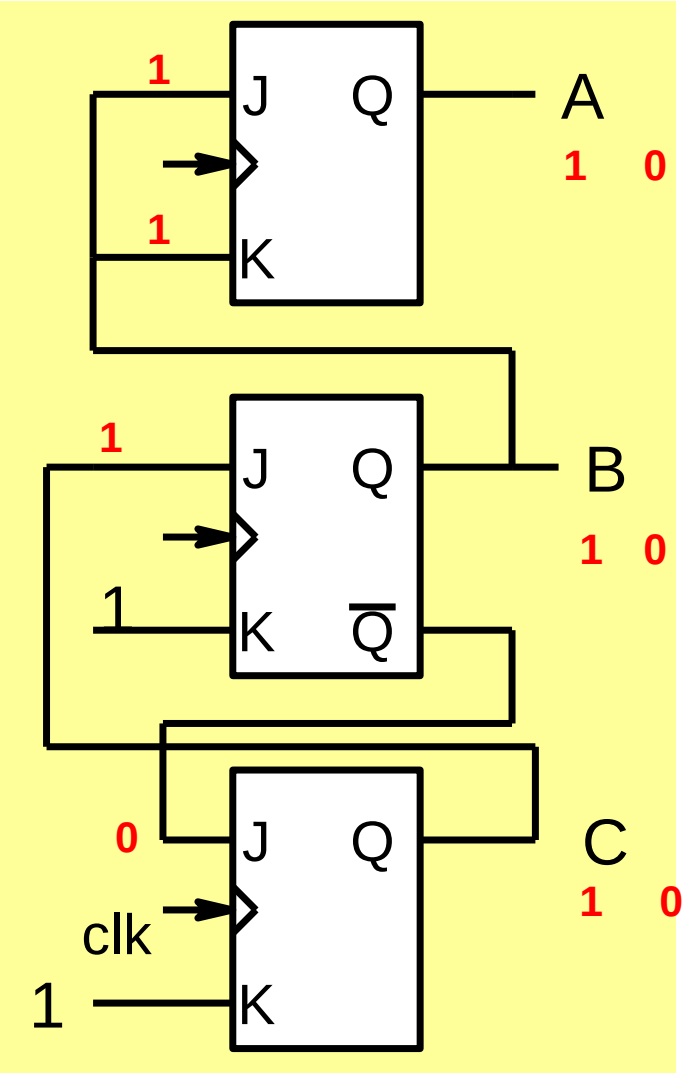
Modulo-5 Counter

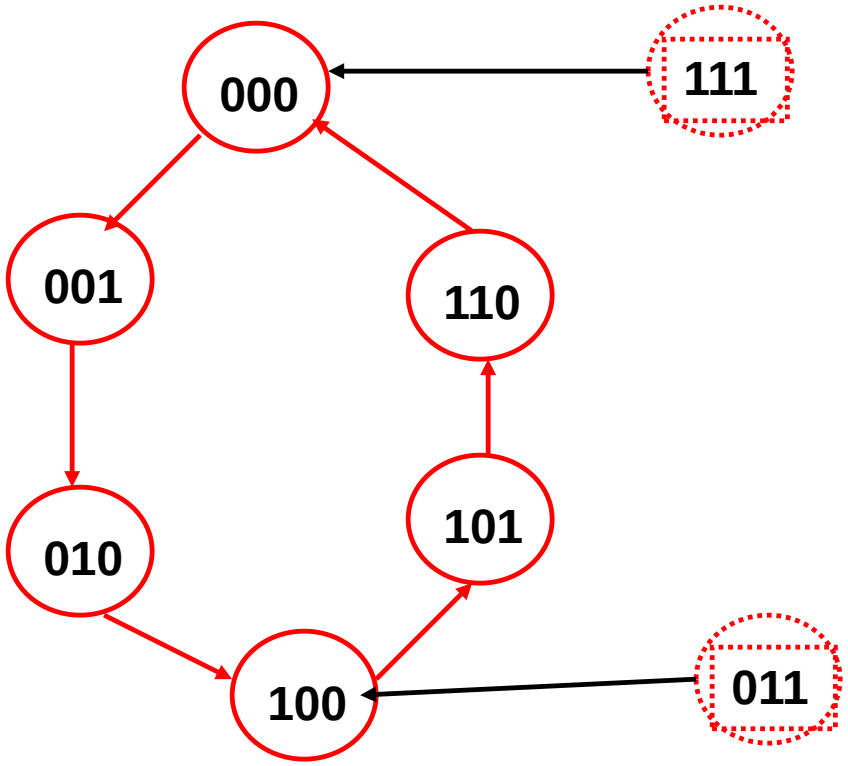
Recap: Counter with Unused States

PS			NS			J_A	K_A	J_B	K_B	J_C	K_C
A	B	C	A	B	C						
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

There are two unused states 011 and 111. one approach to handle this situation is that, while evaluating expressions for J K , we use don't care conditions corresponding to these unused states

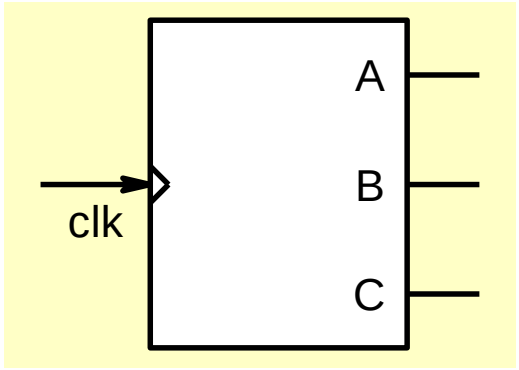
Recap:



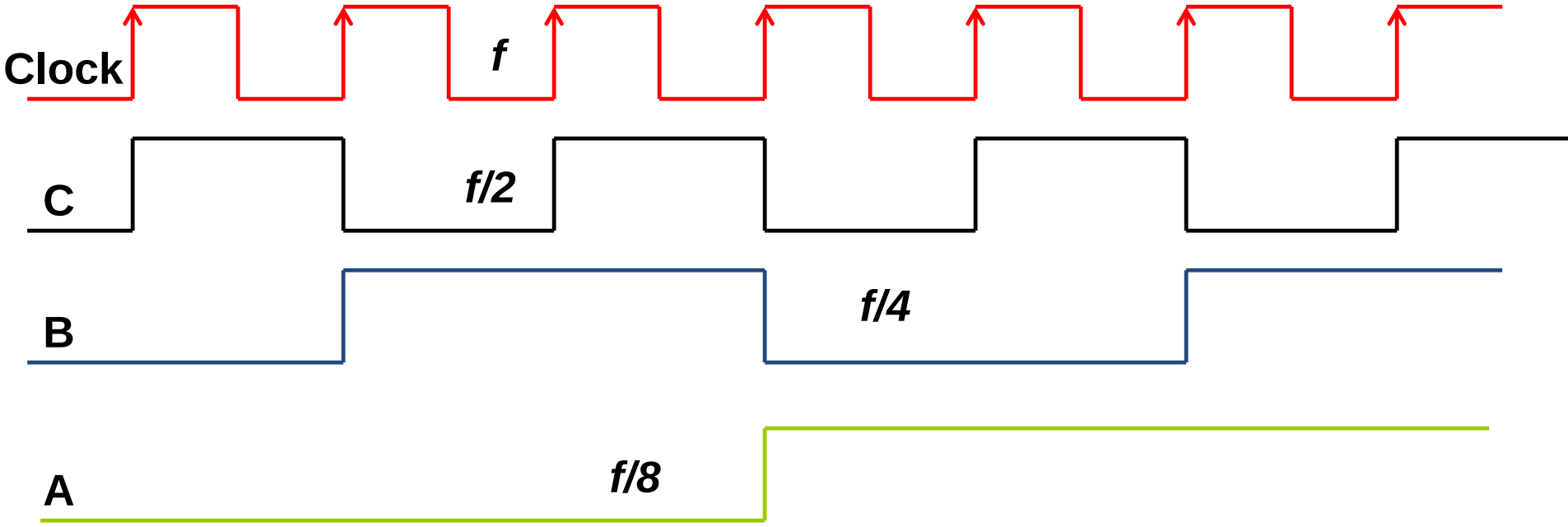


We can see that if by chance the counter goes into unused states 111 or 011, then after a clock cycle it enters one of the used states.

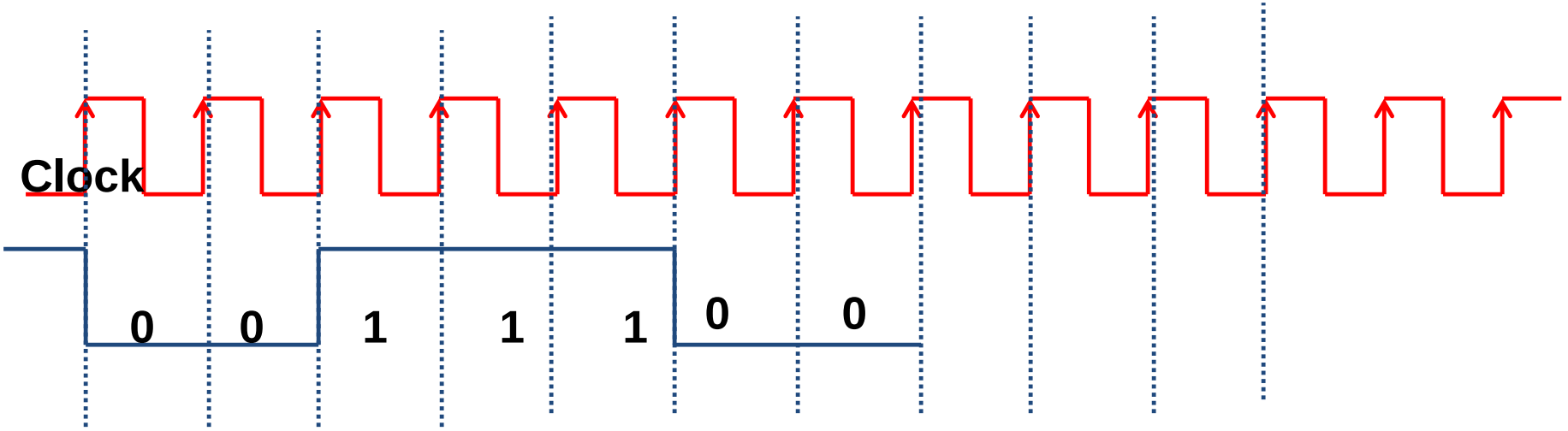
Recap: Counter as frequency divider



A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1



Example From a frequency of 10KHz, generate the following signal of frequency 2KHz



A divide by 5 counter is required that has 5 states.

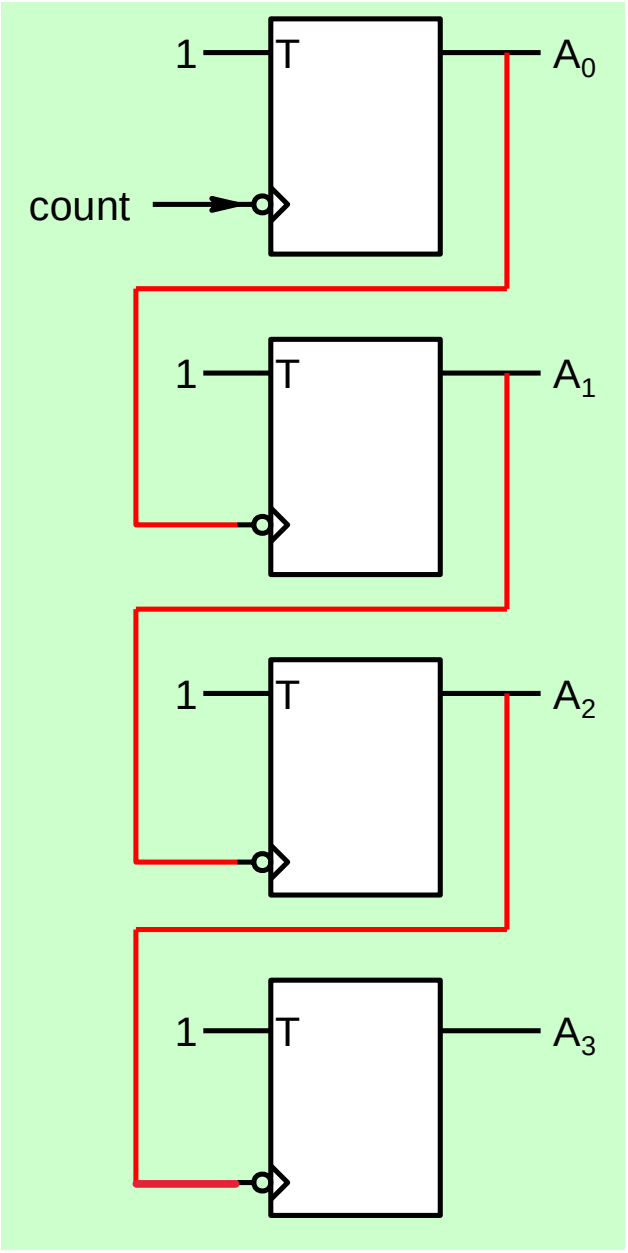
A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

Modify

A	B	C
0	0	0
0	0	1
1	1	0
1	1	1
1	0	0

A will give the required waveform.

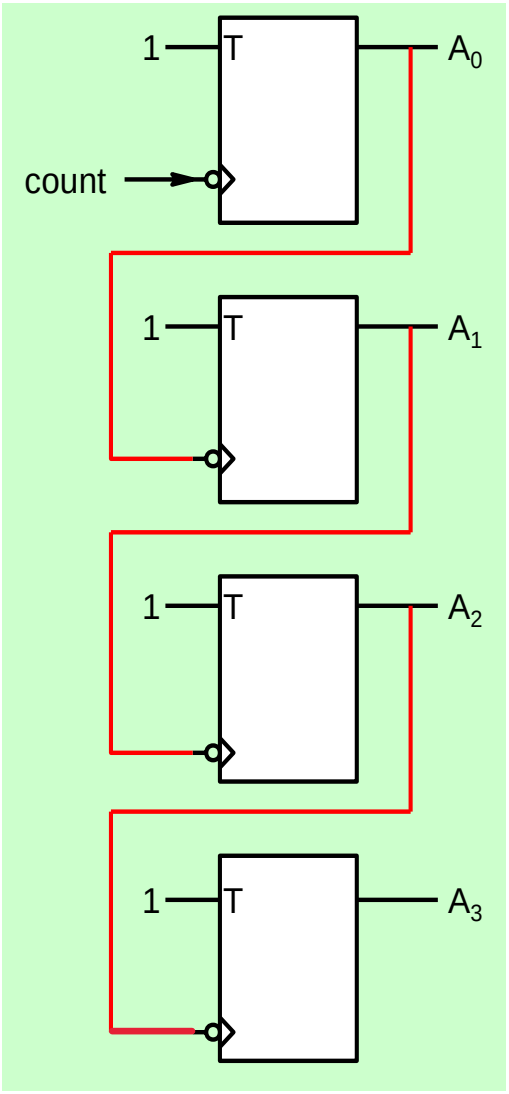
Ripple Counter



T FF toggles when T = 1; otherwise Hold state

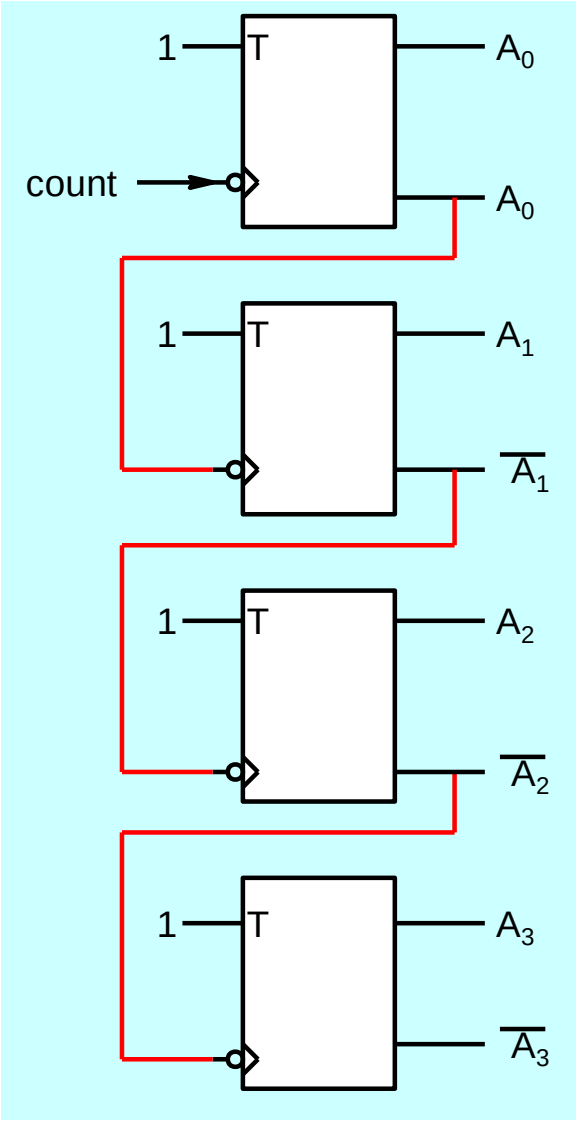
FF is negative edge Triggered

Ripple Counter



0	1	2	3	4	5	------15	
0	1	0	1	0	1	------1	0
0	0	1	1	0	0	------1	0
0	0	0	0	1	1	------1	0
0	0	0	0	0	0	------1	0

Ripple Down Counter



0 1 0

0 1 1

0 1 1

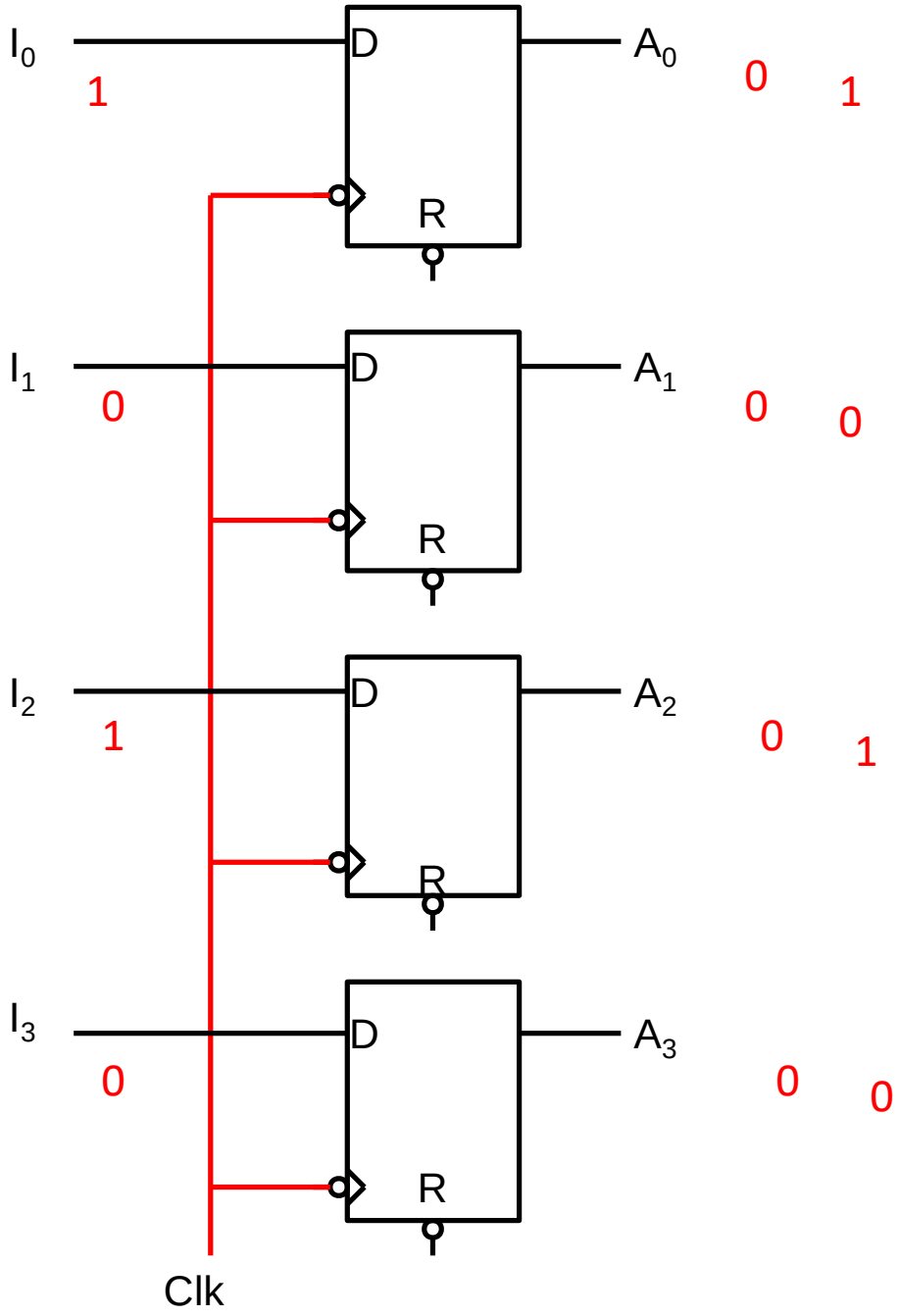
0 1 1

Example: A flip-flop has a 3ns delay from the time the clock edge occurs to the time the output is complemented. What is the maximum delay in a 10-bit counter that uses this type of flip-flop?

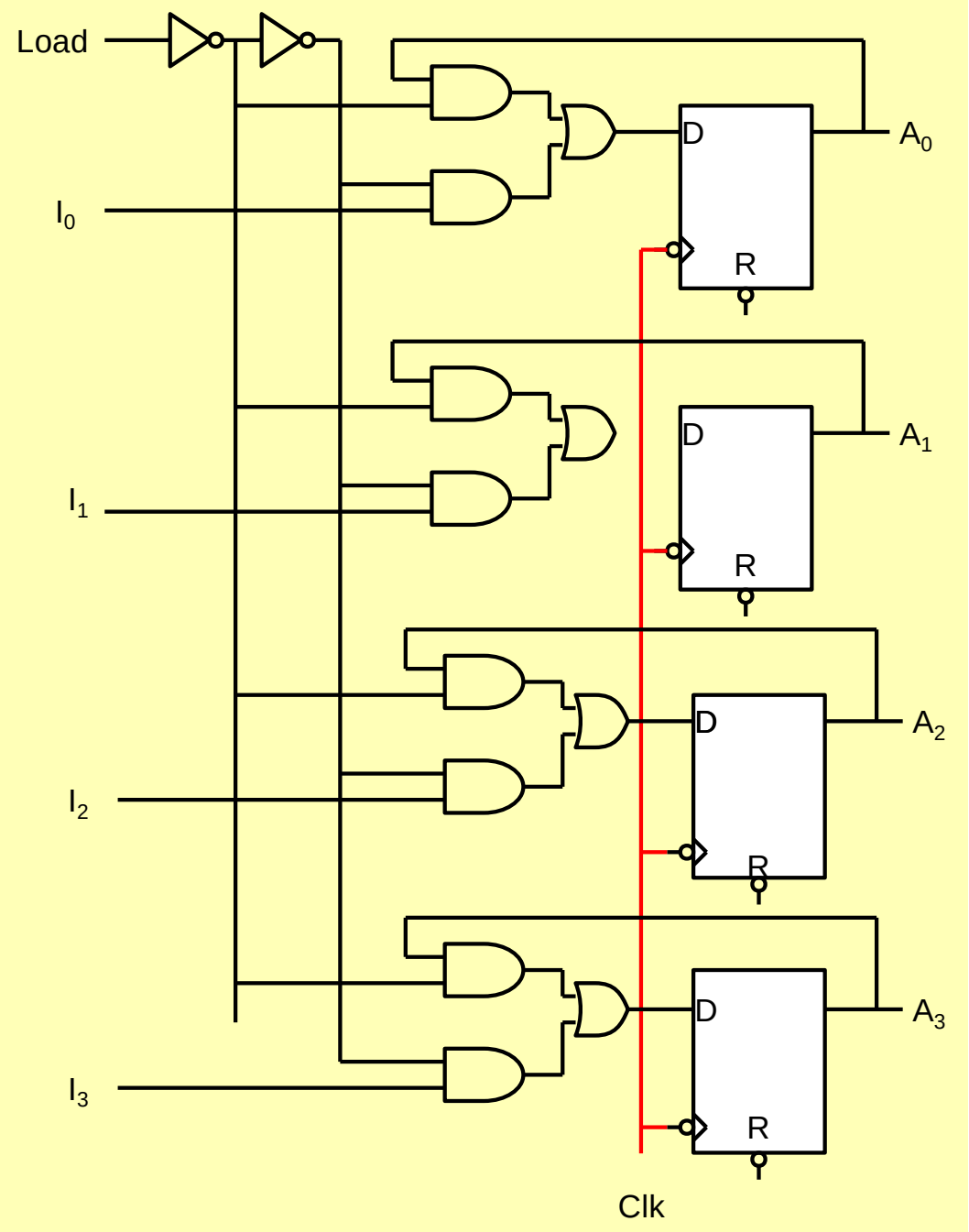
The worst case is when all 10 flip-flops are complemented. The maximum delay is 10 x 3ns = 30ns.

The maximum frequency then will be: $f = \frac{1}{30ns} = 33.3MHz$

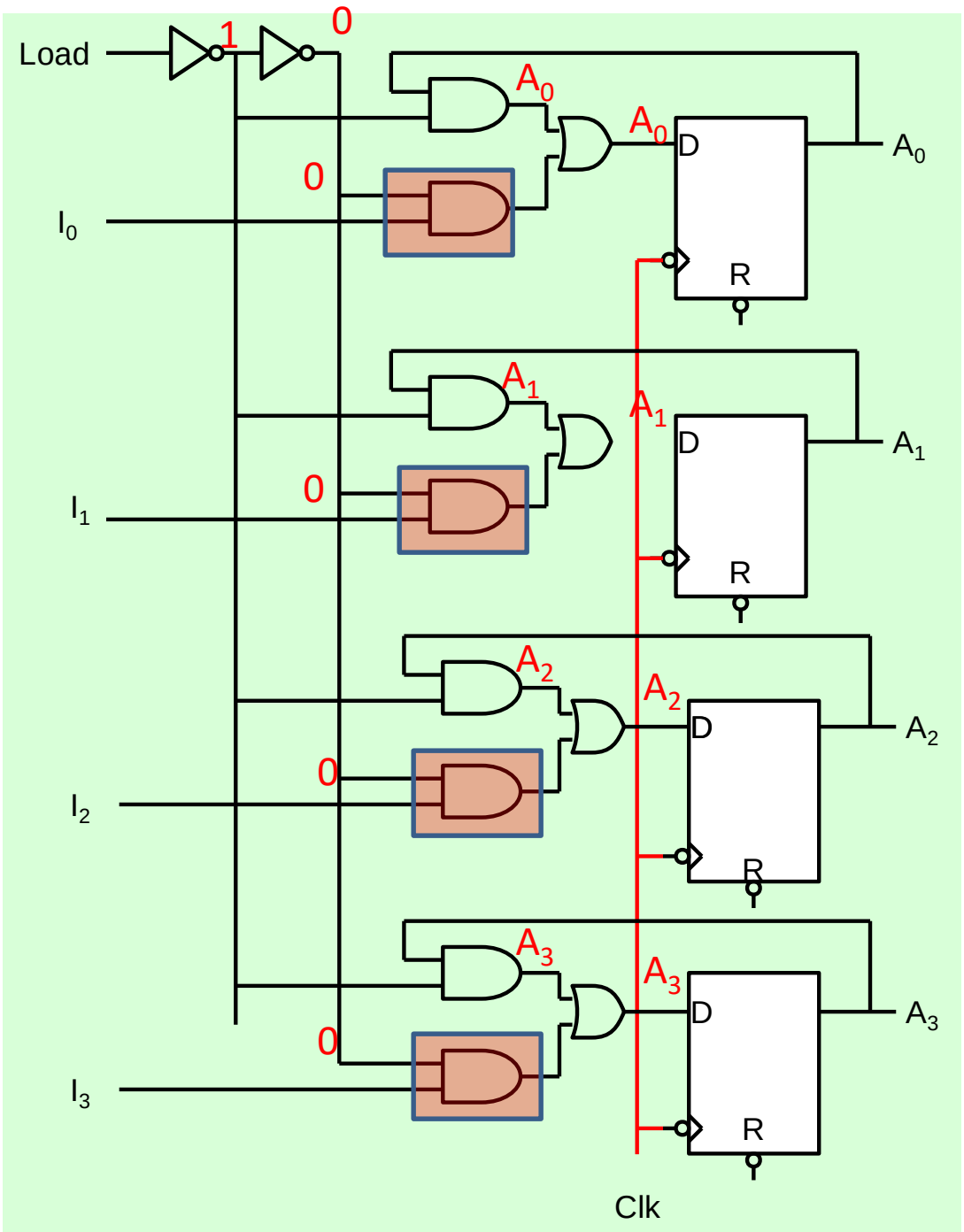
Register



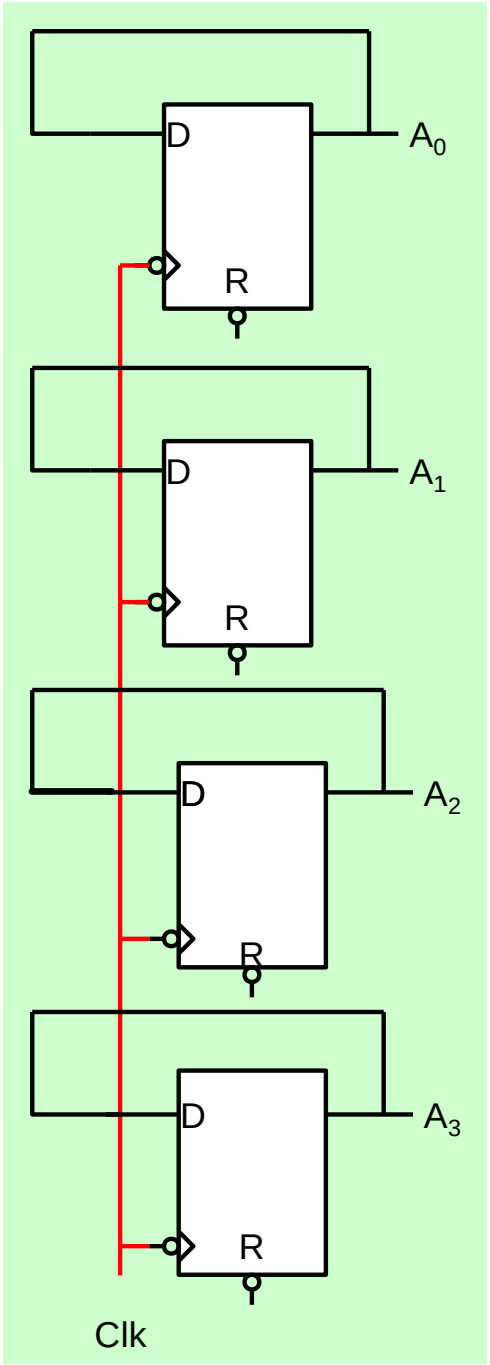
4-bit Register with parallel load



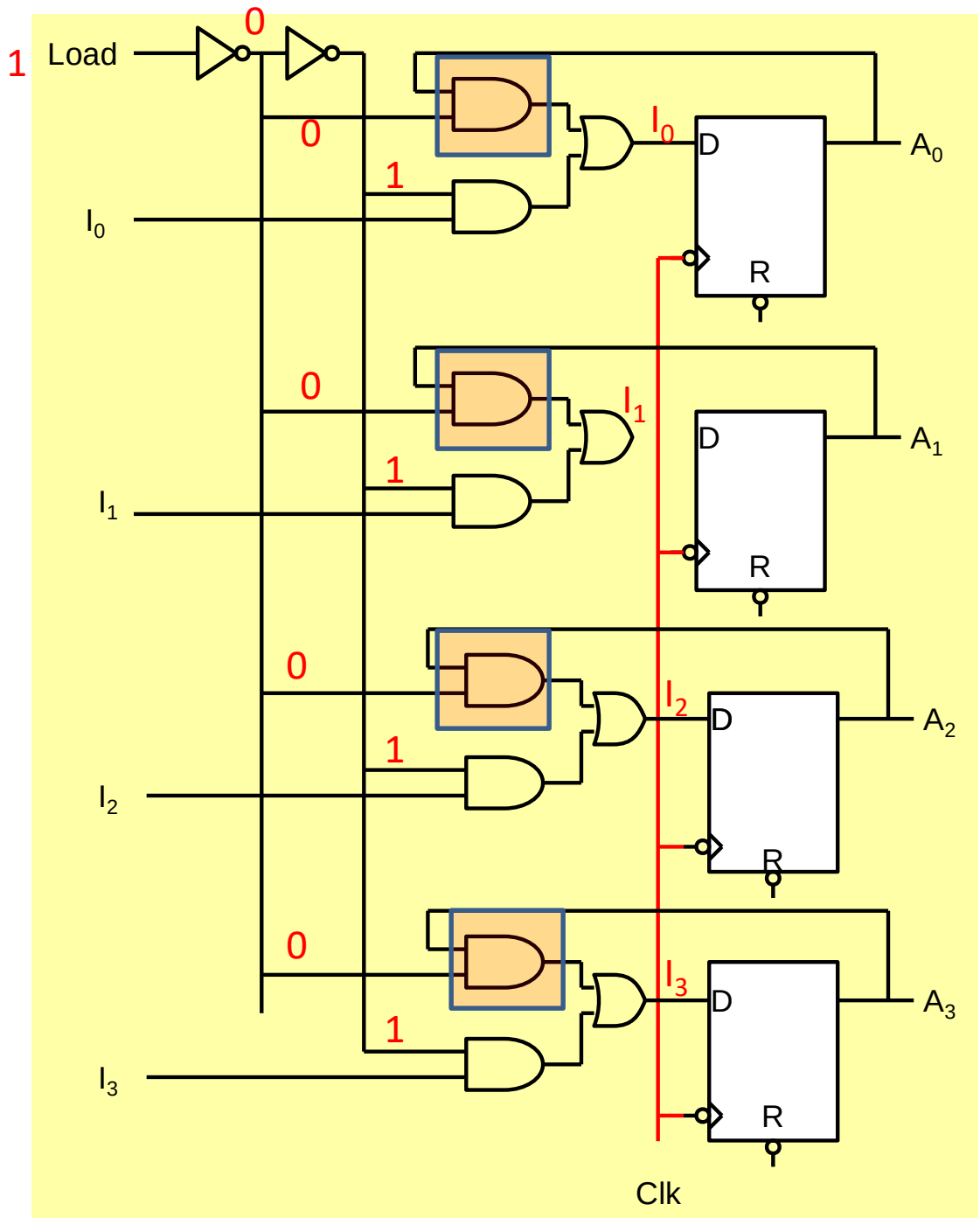
Load = 0


0
Load
1
0
A_0
A_0
0
I_0
D
R
A_0
A_1
A_1
0
I_1
D
R
A_1
A_2
A_2
0
I_2
D
R
A_2
A_3
A_3
0
I_3
D
R
A_3
Clk

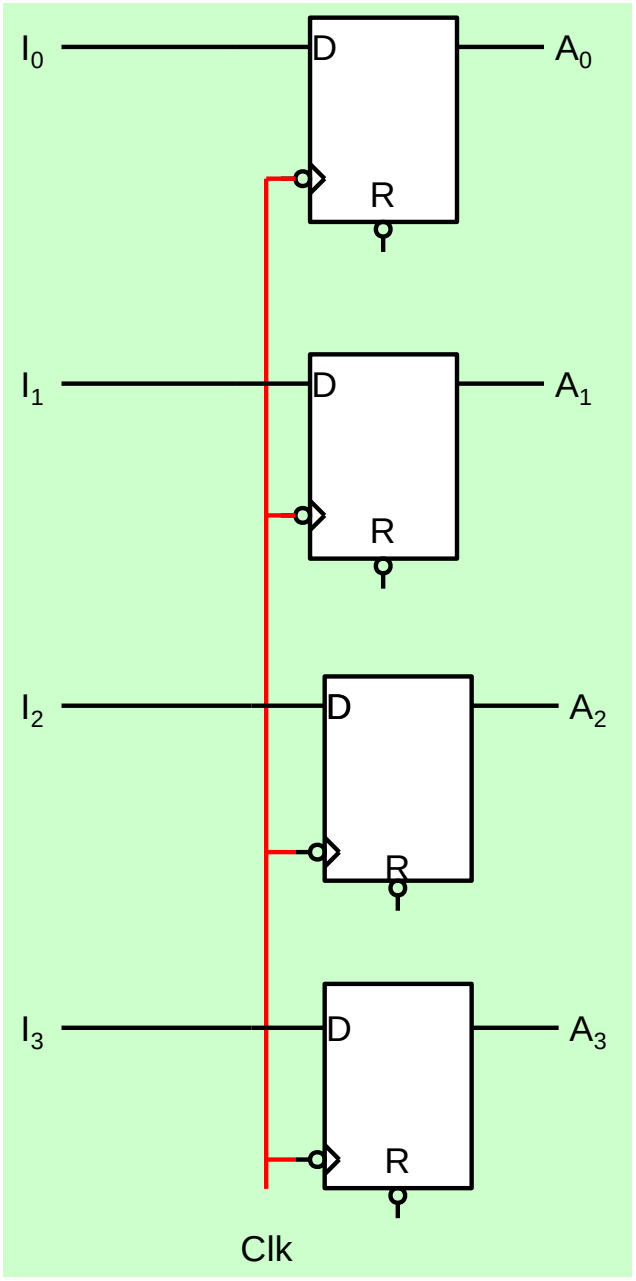
Equivalent Circuit



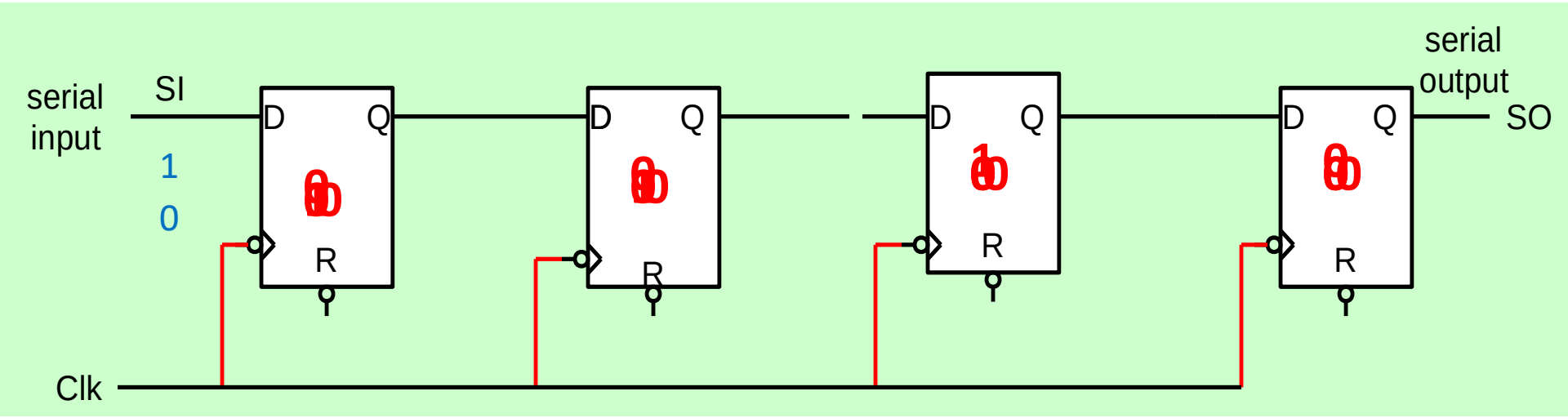
Load = 1



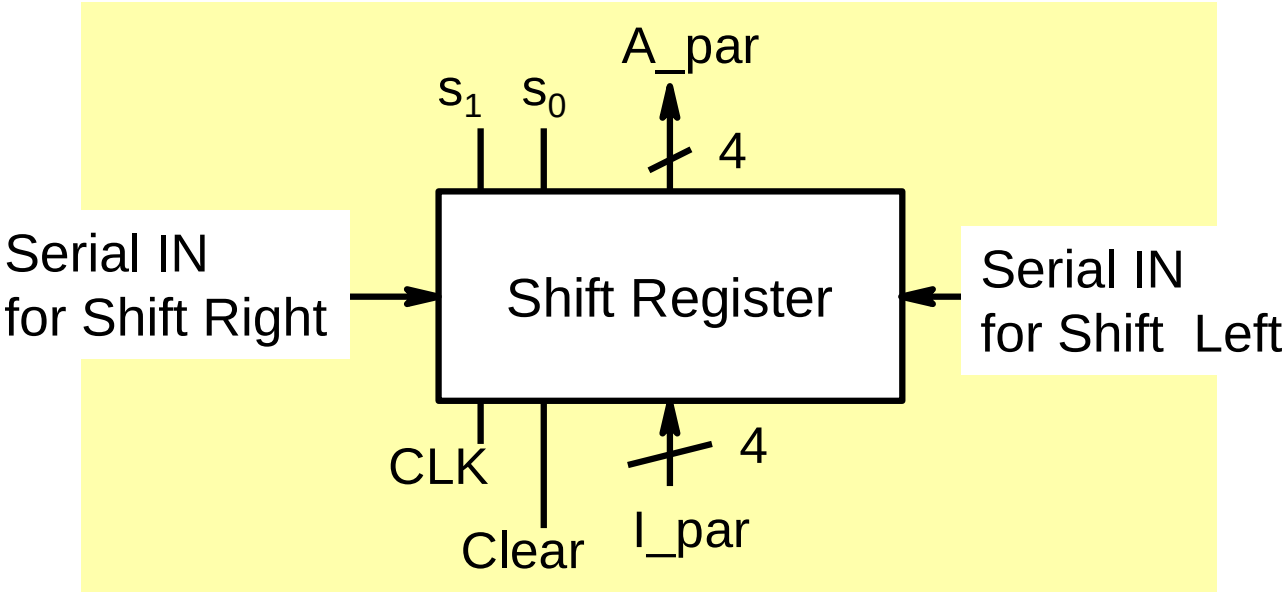
Equivalent Circuit



4-bit Shift Register

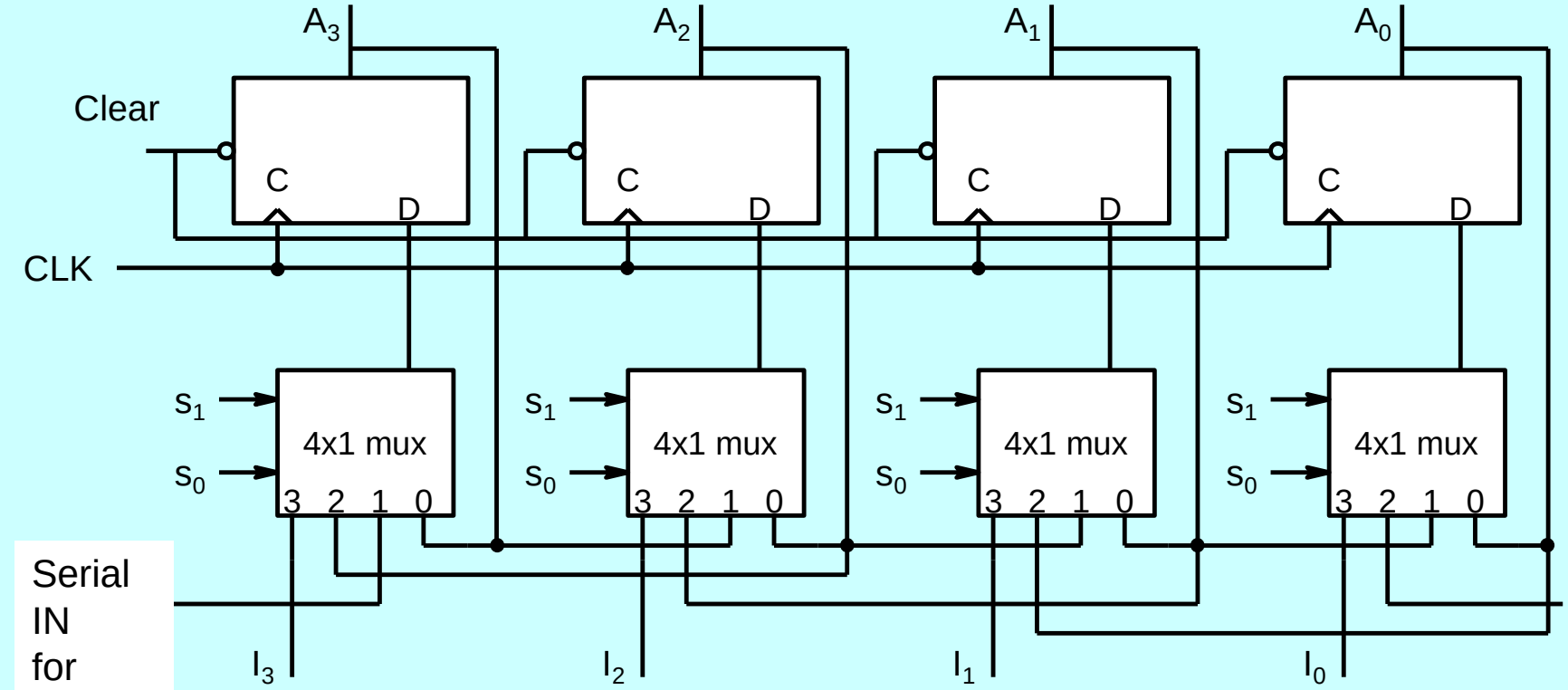


4-bit universal Register



Function

S_1	S_0	Register Operation
0	0	No change
0	1	Shift right
1	0	Shift left
1	1	Parallel Load



Function

S_1	S_0	Register Operation
0	0	No change
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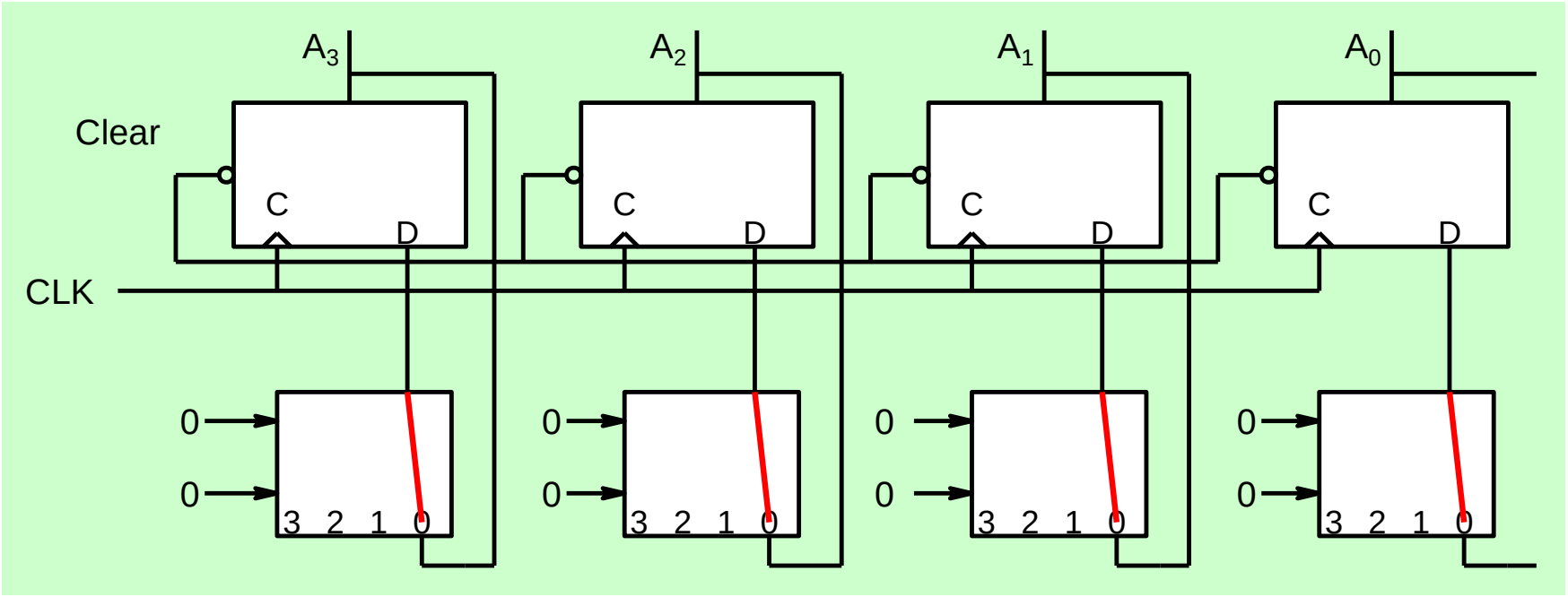
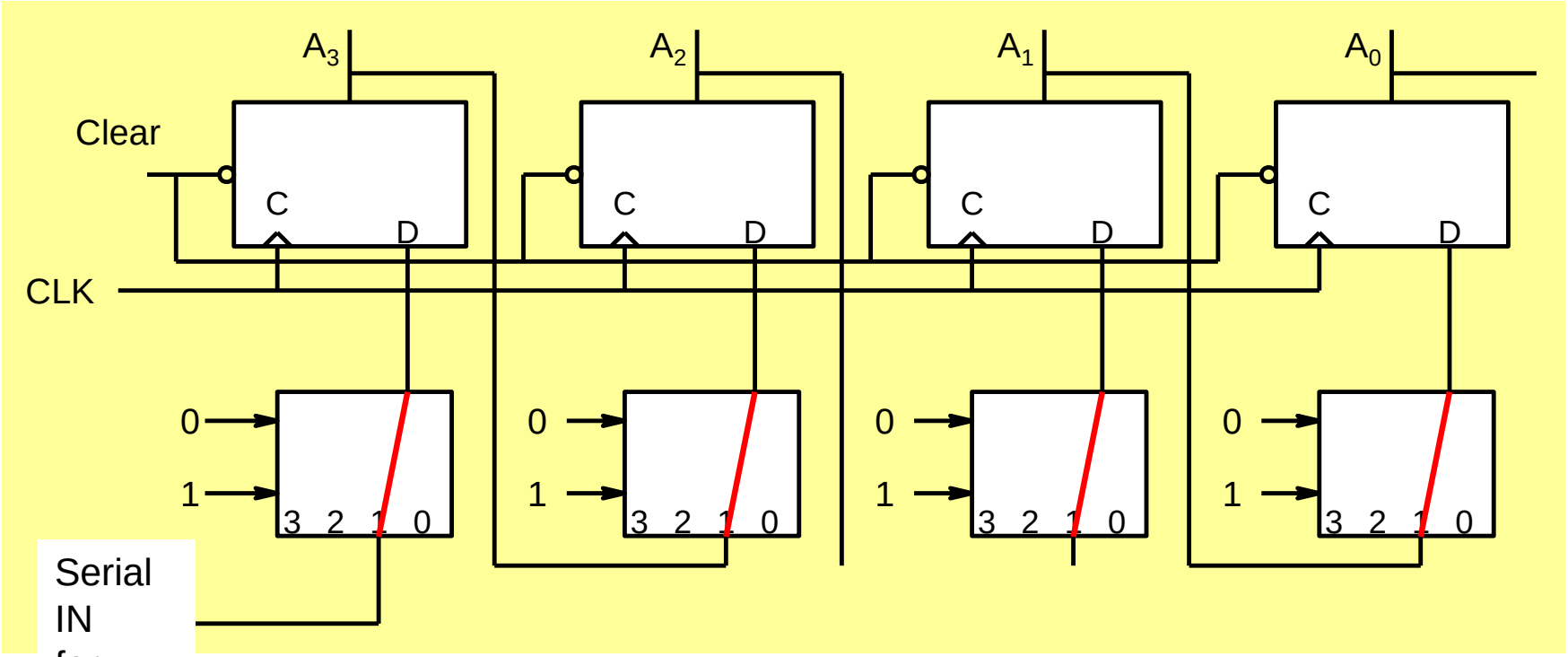
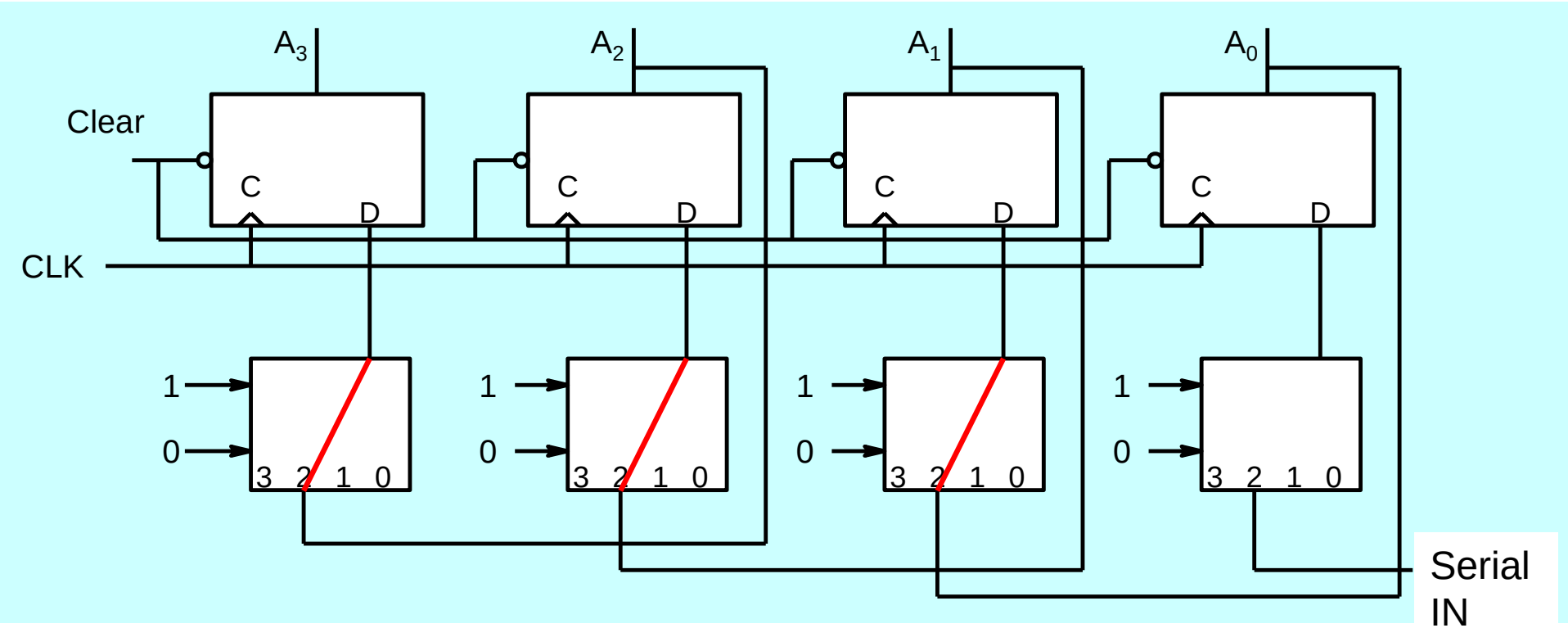


The register maintains its state

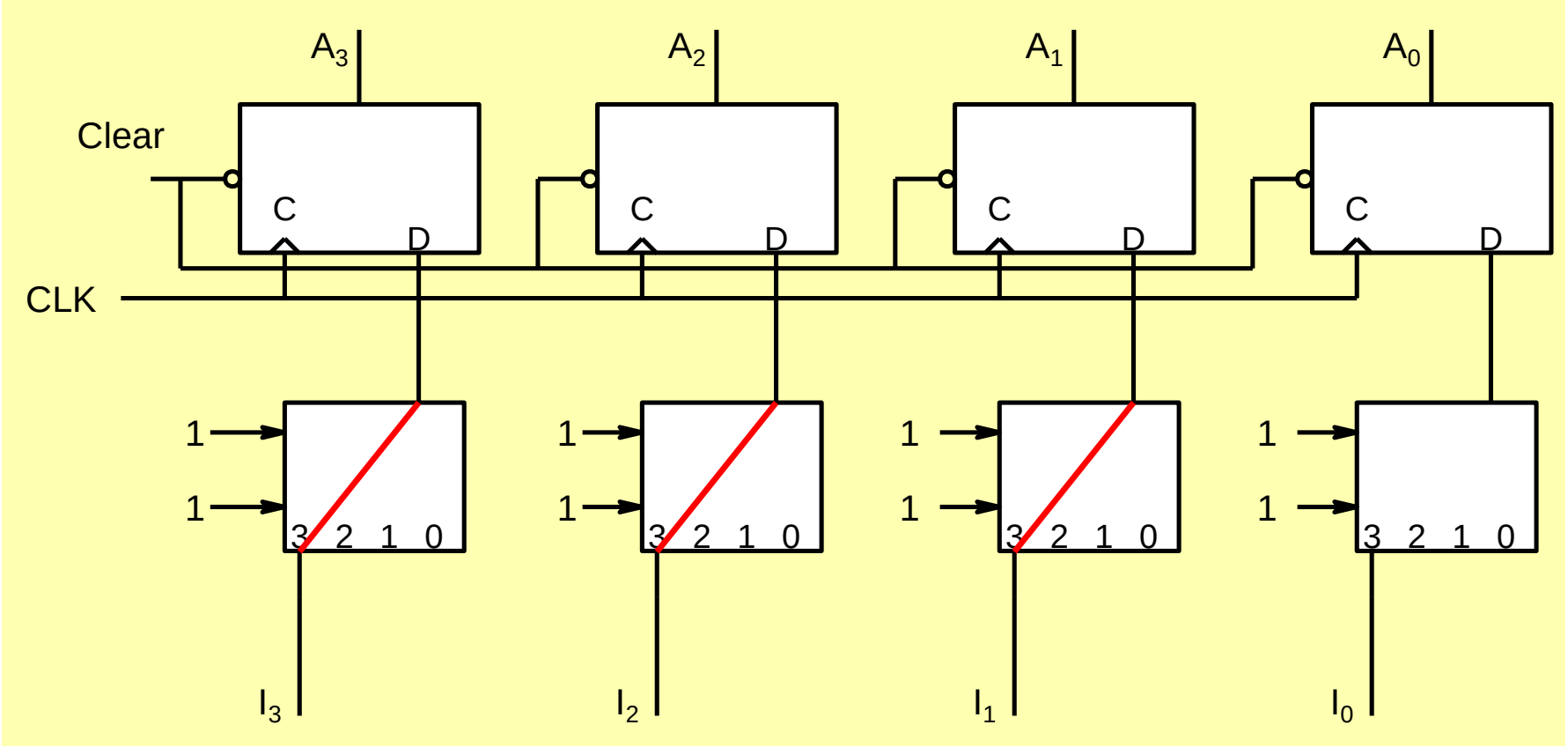
S_1 S_0 = 01: Shift right



$S_1\ S_0 = 10$: Shift left

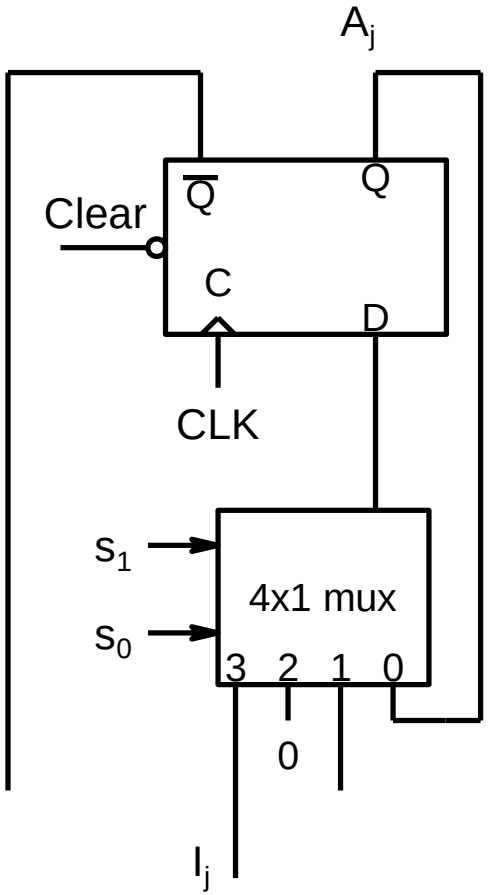


S_1 S_0 = 11: Parallel Load



Example: Design a 4-bit register with 4 D FFs and four 4-to-1 multiplexers with control inputs s1 and s2 such that when S1S2 = 00, there is no change in the register content; when 01 the outputs are complemented; when 10 the register is cleared to 0 synchronously and when 11 the parallel data is synchronously loaded

The register is made of 4 stages each of which has the structure shown below



Quiz-3 Discussion

All the best for the exams!