ESC201A Assignment 10

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2023-2024 Semester I

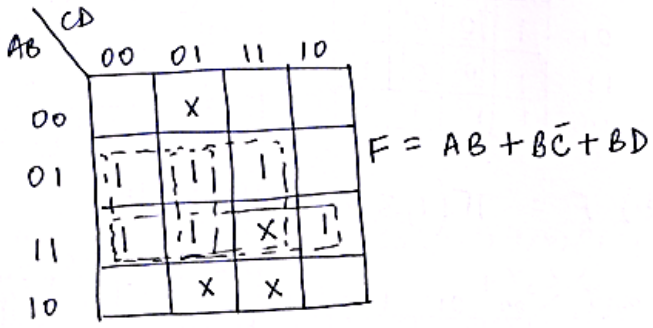
Topics

Boolean Expressions Minimization, Implementation, En/Decoder, Multiplexers/Demux, Modular Design

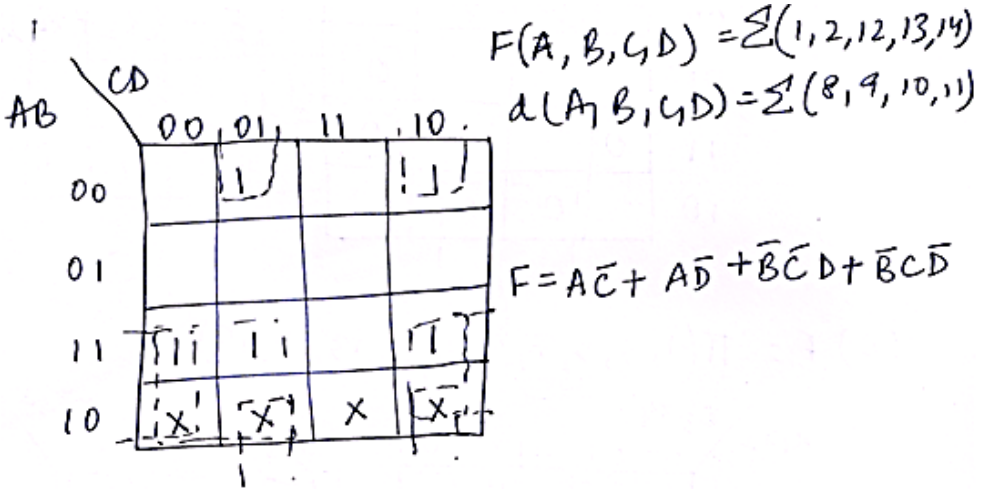
Questions

1. Simplify the following expressions into sum-of-products form using the don't care conditions (d) into account.

   a. $F(A,B,C,D) = \sum(4,5,7,12,13,14) \quad d(A,B,C,D) = \sum(1,9,11,15)$



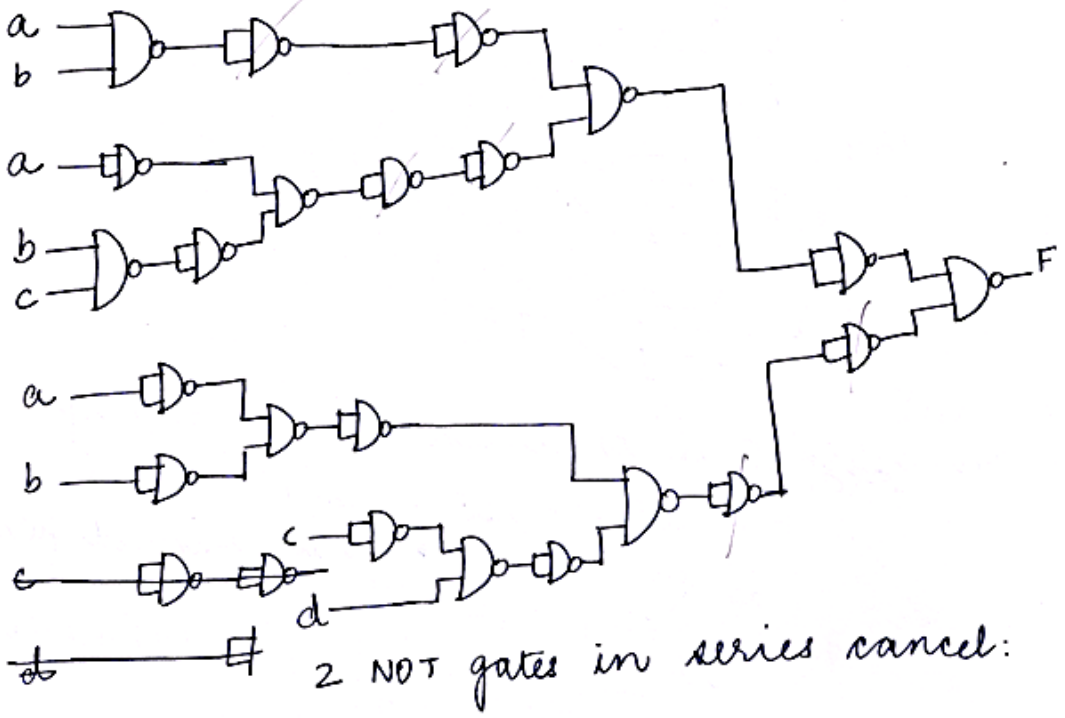
   b. $F(A,B,C,D) = \sum(1,2,12,13,14) \quad d(A,B,C,D) = \sum(8,9,10,11)$



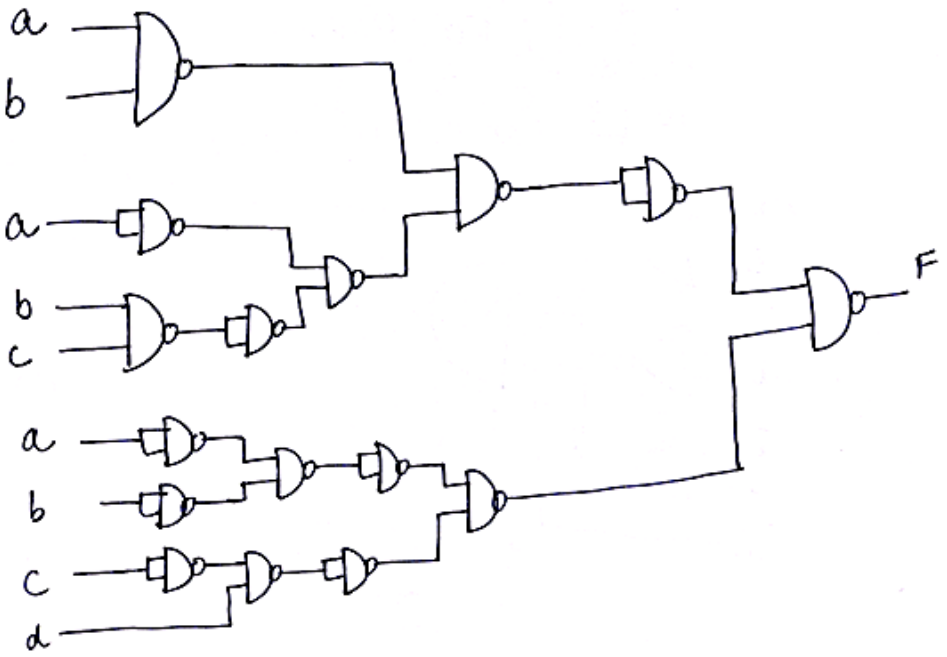
2. Implement the following expression using only 2-input NAND gates and then repeat the problem with only 2 input NOR gates.

$$F(a,b,c,d) = ab + \bar{a}bc + \bar{a}\bar{b}\bar{c}d$$

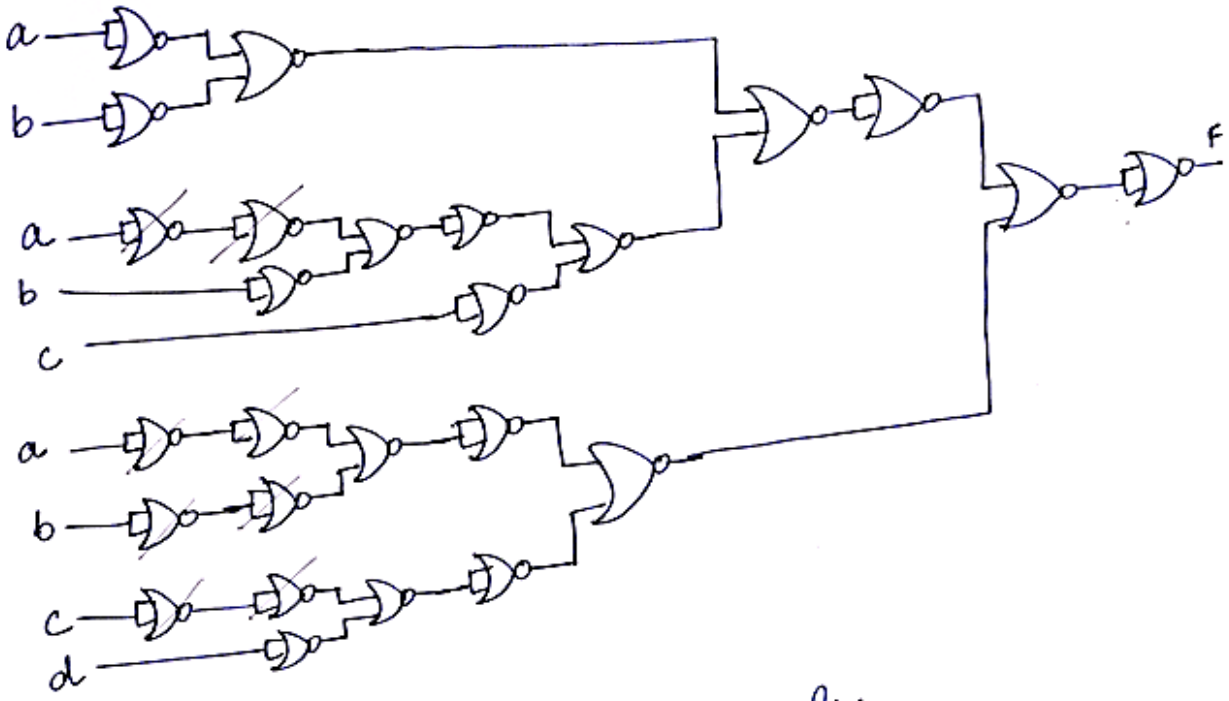
Using 2-input NAND gates:



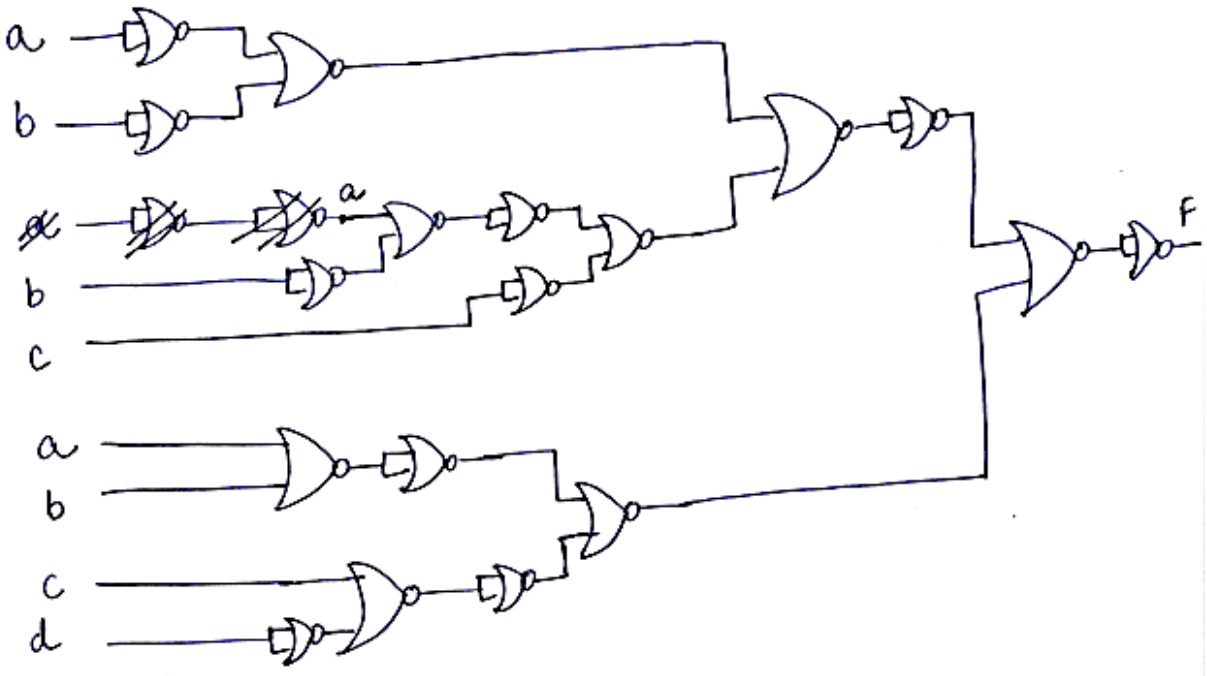
2 NOT gates in series cancel:



Using 2-input NOR gates:



2 NOT gates in series cancel:



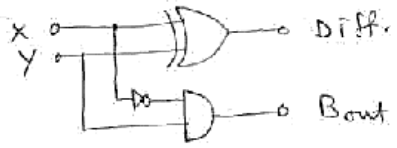
3. Design a half subtractor circuit with inputs x and y and outputs Diff. and B_{out}. The circuit subtracts the bits x-y, places the result in Diff., and borrow in B_{out}.

Half Subtractor. Truth table

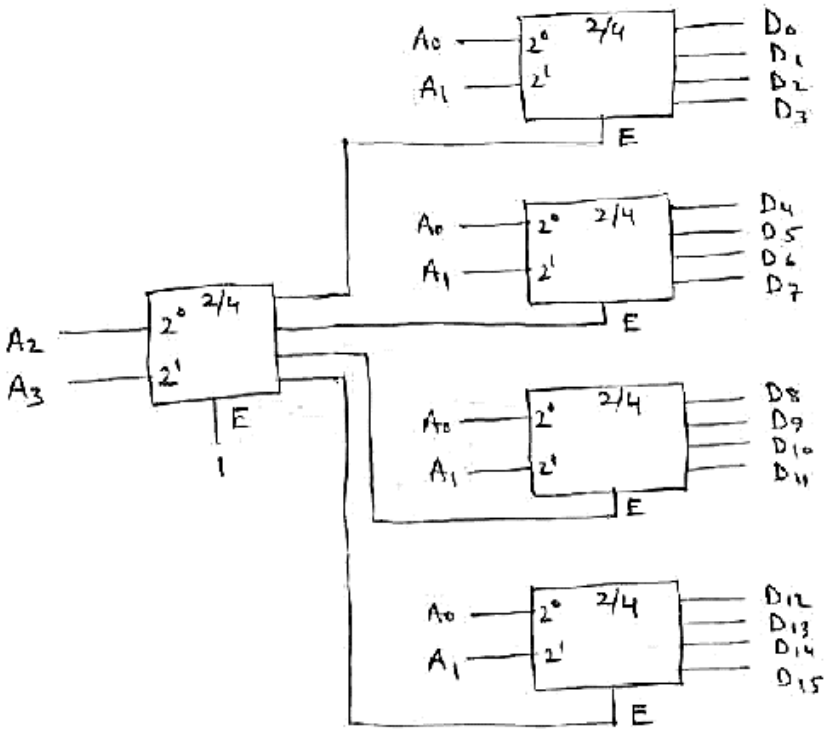
Input		Output	
X	Y	Diff.	Bout
0	0	0	0
0	1	1	1
1	0	1	0
1	1	0	0

$Diff. = x \oplus y$

$B_{out} = \bar{x} \cdot y$

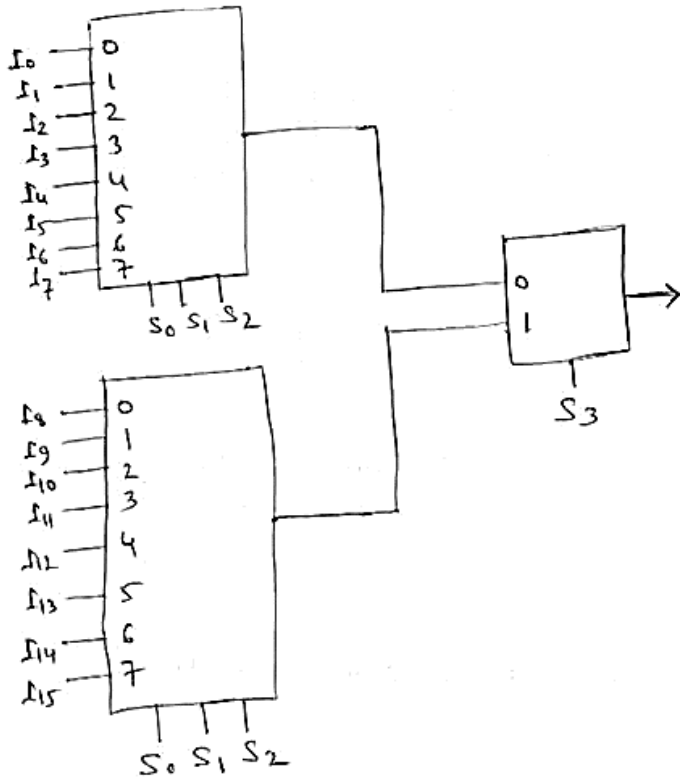


4. Construct a 4-to-16 line decoder with five 2-to-4 line decoders with enable input.



4 to 16 decoder using five 2 to 4 decoder.

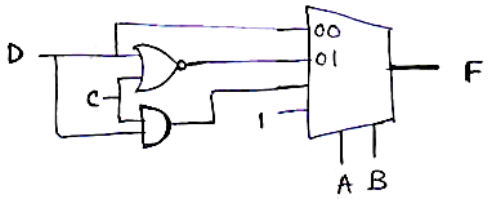
5. Construct a 16 x 1 multiplexer with two 8-to-1 and one 2-to-1 multiplexers. Use block diagrams.



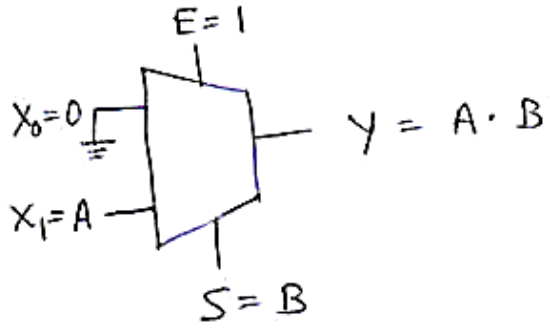
6. Implement the following Boolean function using one 4 to 1 multiplexer and external gates. (Hint: Connect inputs A and B to the control or selection lines of the mux and then use basic gates to apply appropriate combinations of C & D to the input lines of the Mux.)

$$F(A,B,C,D)=\sum(1,3,4,11,12,13,14,15)$$

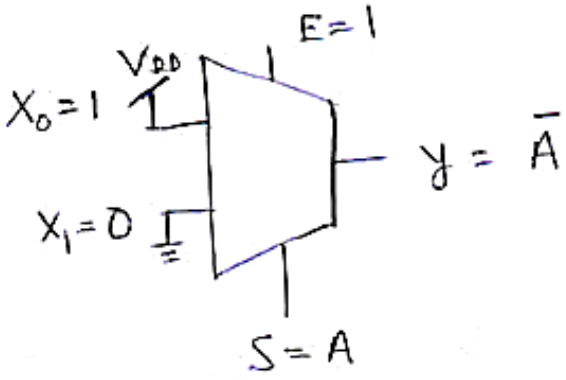
A B	C D	F	
0 0	0 0	0	
0 0	0 1	1	F = D
0 0	1 0	0	
0 0	1 1	1	
0 1	0 0	1	
0 1	0 1	0	F = $\bar{C}\bar{D}$
0 1	1 0	0	
0 1	1 1	0	
1 0	0 0	0	
1 0	0 1	0	F = C D
1 0	1 0	0	
1 0	1 1	1	
1 1	0 0	1	
1 1	0 1	1	F = 1
1 1	1 0	1	
1 1	1 1	1	



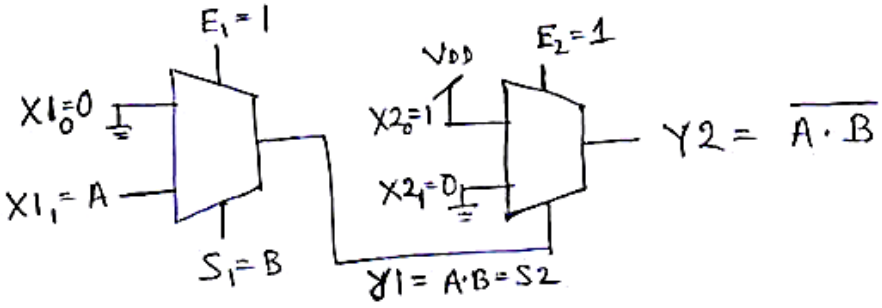
7. (i) Implement a AND gate with a 2 to 1 MUX.



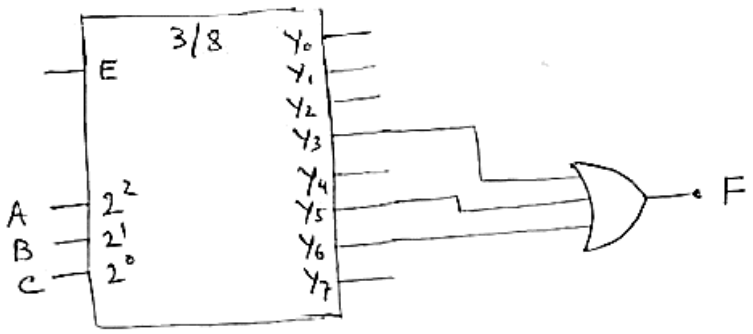
(ii) Implement a NOT gate with a 2 to 1 MUX.



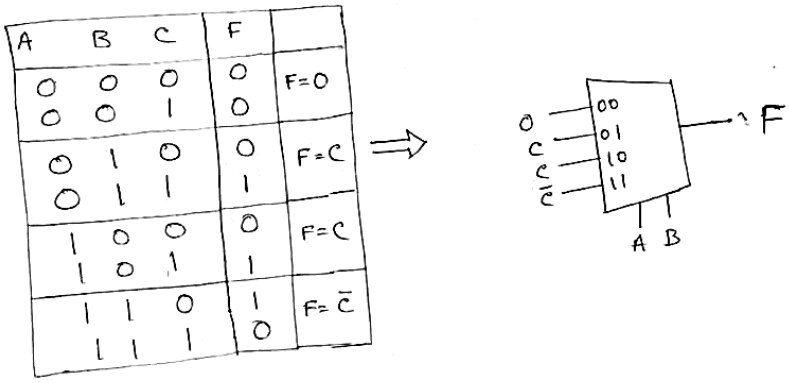
(iii) Now implement a NAND (a universal gate) with two 2 to 1 MUX.



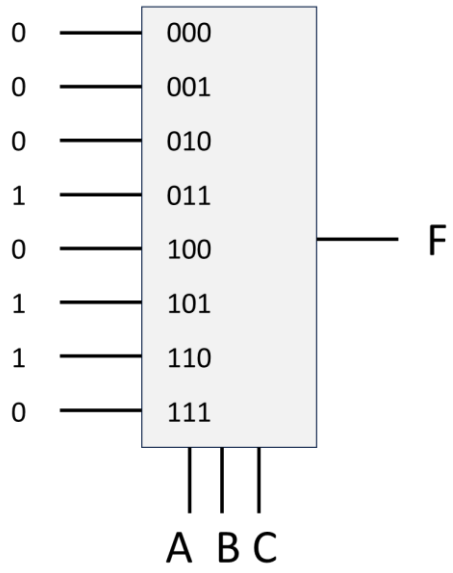
8. (i) Implement the following function using a 3-to-8-lines decoder: $F(A, B, C) = \sum(3,5,6)$



(ii) Implement the above function using a 4-to-1 line multiplexer.



(iii) Implement the above function using a 8-to-1 line multiplexer.



This shows that any truth table can be implemented with a multiplexer without any additional gates.