## **ESc201: Introduction to Electronics**

**Logic Gates and Minimization** 

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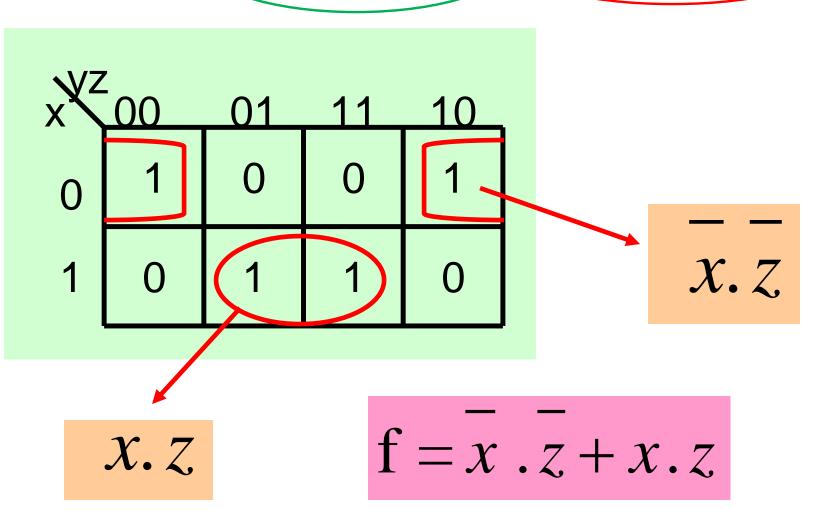
#### 3-variable minimization (recap)

$$f = x.y.z + x.y.z + x.y.z + x.y.z$$

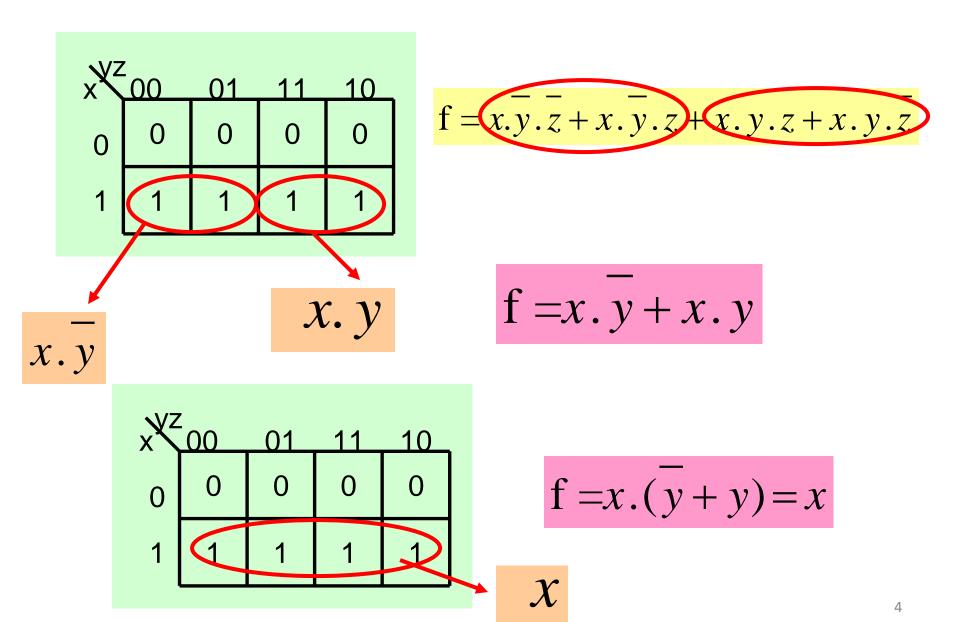
$$x = x.y.z + x.y.z + x.z$$

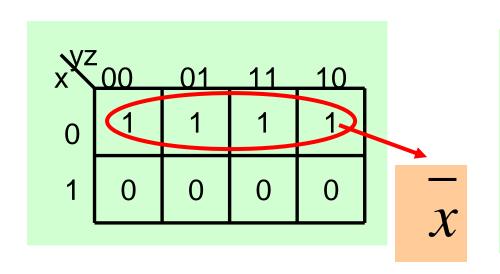
#### 3-variable minimization (recap)

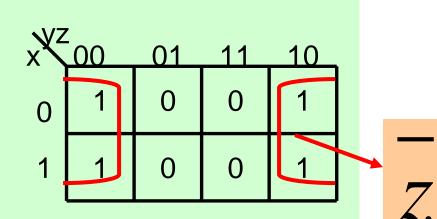
$$f = \overbrace{x.y.z + x.y.z + x.y.z}$$

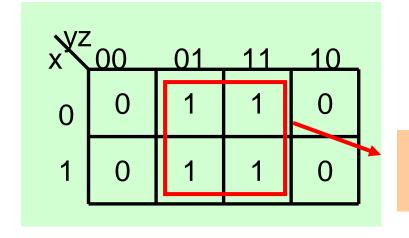


## 3-variable minimization (recap)

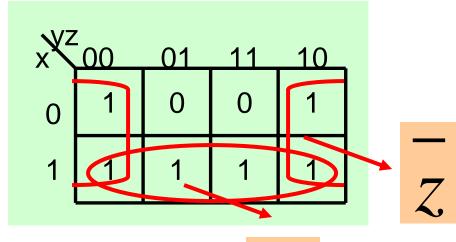








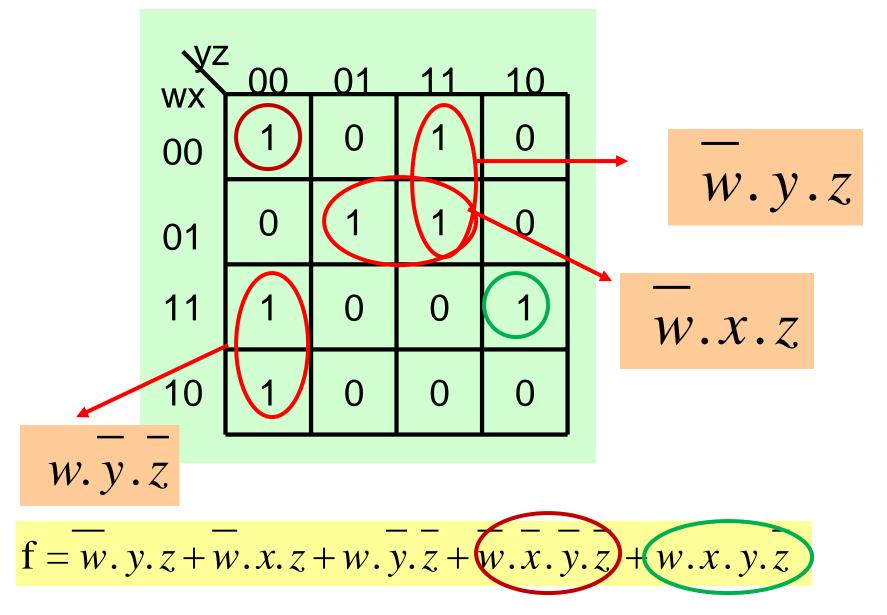
Z



$$f = x + \overline{z}$$

 $\mathcal{X}$ 

#### 4-variable minimization



Is this the simplest expression?

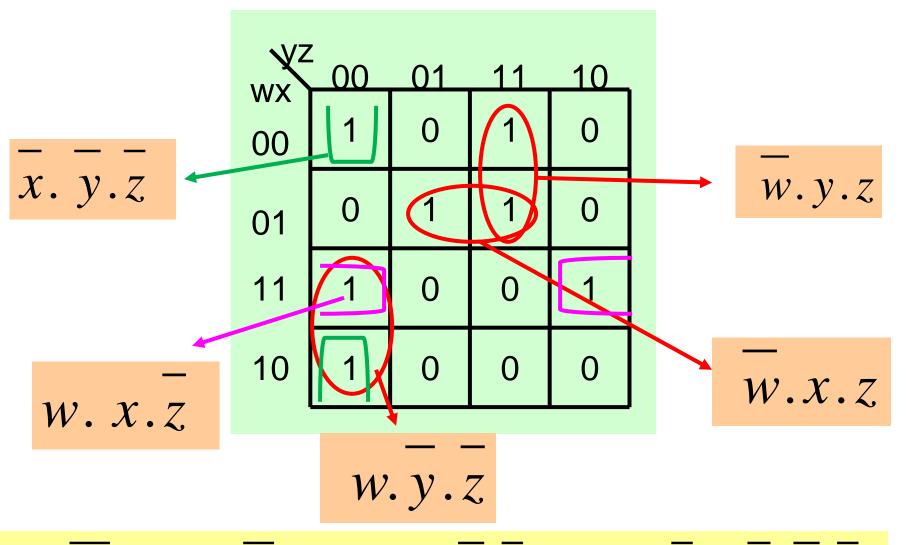
wx VZ	00_	01_	11_	10_	
00	1	0	1	0	
01	0	1	1	0	
11	1	0	0	1	
10	1	0	0	0	

VZ	00	01	11	10_	
wx 00	1	0	1	0	
01	0	1	1	0	
11	1	0	0	1	
10	1	0	0	0	

$$w. x. y. z + w. x. y. z = x. y. z$$

$$w. x. y. z + w. x. y. z = w. x. z$$

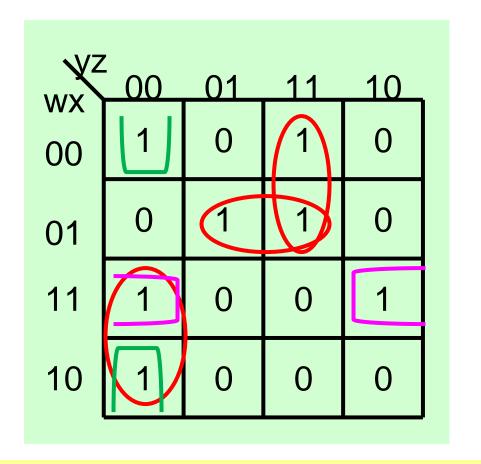
#### 4-variable minimization



$$f = w.y.z + w.x.z + w.y.z + w.x.z + x.y.z$$

Is this the best that we can do?

#### Cover the 1's with minimum number of terms

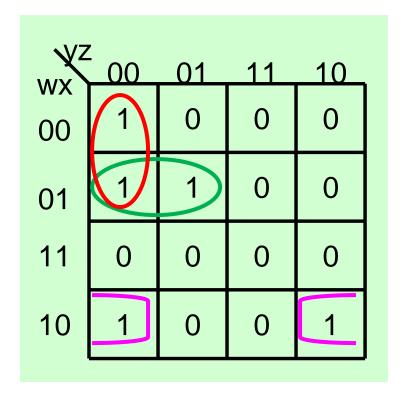


WX WX	00	01	11	10_	
00	1	0	$\bigcap$	0	
01	0		D	0	
11	1	0	0	1	
10	1	0	0	0	

$$f = w. y. z + w. x. z + w. y. z + w. x. z + w. y. z + w. x. z + x. y. z$$

$$f = w. y. z + w. x. z$$

#### 4-variable minimization

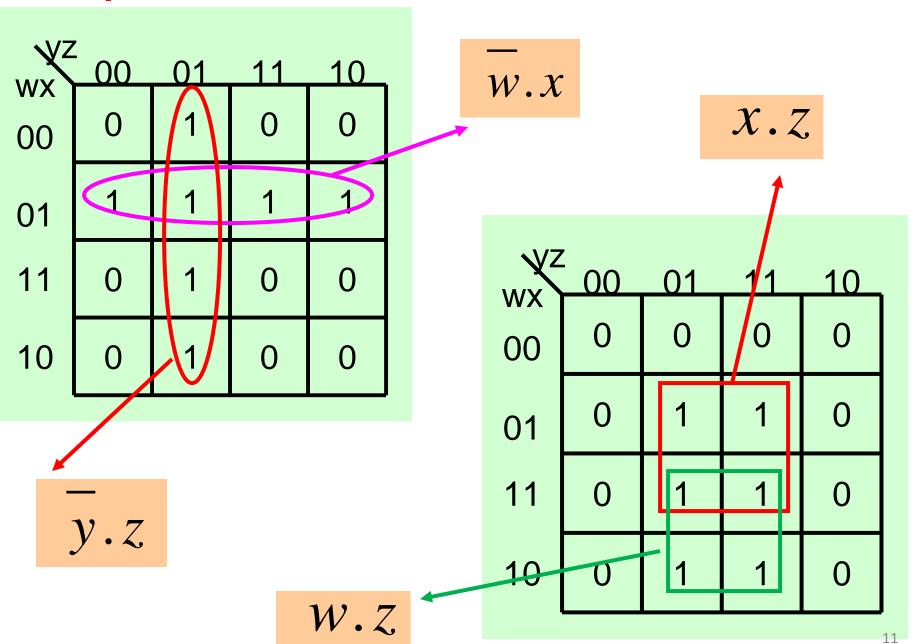


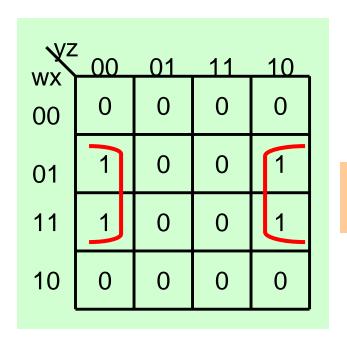
VZ WY	00	01	11	10_
wx 00	1	0	0	0
01	$\bigcirc$	(T)	0	0
11	0	0	0	0
10	1	0	0	1

$$f = \overline{w.x.y} + \overline{w.x.z} + \overline{w.y.z}$$

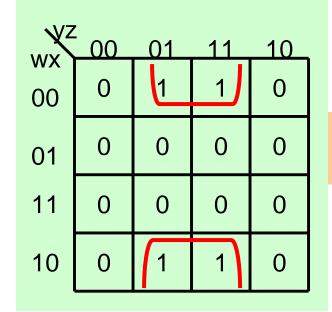
$$f = \overline{w.x.y} + \overline{w.x.z} + \overline{x.y.z}$$

# **Groups of 4**





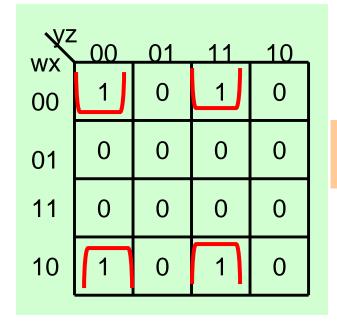
		_
$\mathcal{X}$	•	Z





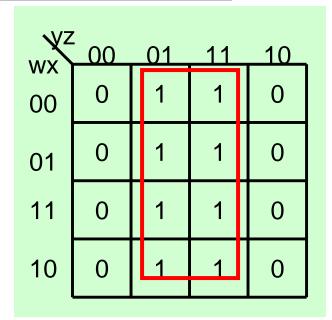
WX VZ	00	01_	11	_10_
00	1	0	0	1
01	0	0	0	0
11	0	0	0	0
10	1	0	0	1

 $\overline{x}.\overline{z}$ 

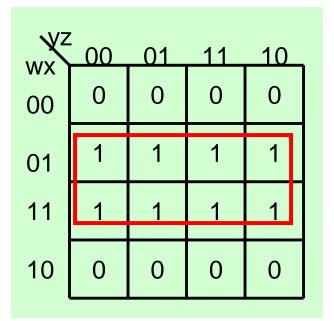


??

# **Groups of 8**



Z



 $\mathcal{X}$ 

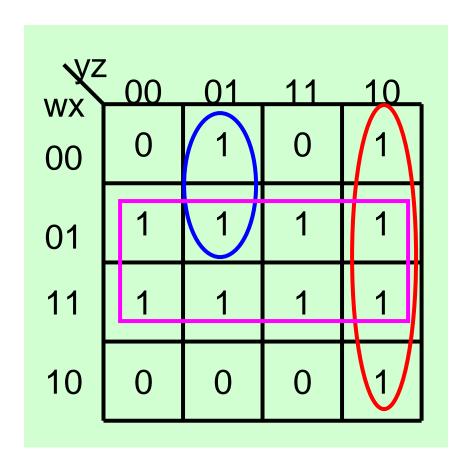
WX VZ	00	01	11	10_
00	1	0	0	1
01	1	0	0	1
11	1	0	0	1
10	1	0	0	1

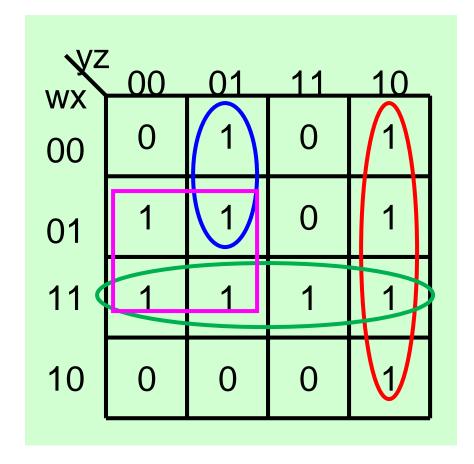
Z

WX WX	00	01_	11	10_
00	1	1	1	1
01	0	0	0	0
11	0	0	0	0
10	1	1	1	1

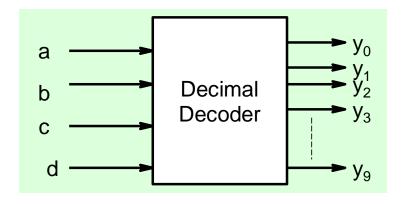
 $\mathcal{X}$ 

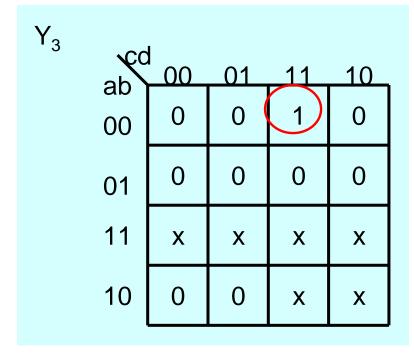
# **Examples**





#### Don't care terms





$$y_3 = \overline{a.b.c.d}$$

а	b	С	d	<b>y</b> <sub>0</sub> <b>y</b> <sub>1</sub> <b>y</b> <sub>2</sub> <b>y</b> <sub>3</sub> <b>y</b> <sub>4</sub> <b>y</b> <sub>5</sub> <b>y</b> <sub>6</sub> <b>y</b> <sub>7</sub> <b>y</b> <sub>8</sub> <b>y</b> <sub>9</sub>
0	0	0	0	1000000000
0	0	0	1	0100000000
0	0	1	0	0010000000
0	0	1	1	0001000000
0	1	0	0	0000100000
0	1	0	1	0000010000
0	1	1	0	0000001000
0	1	1	1	0000000100
1	0	0	0	0000000010
 1	0	0	1	0000000001
1	0	1	0	xxxxxxxxx
1	0	1	1	xxxxxxxxx
1	1	0	0	XXXXXXXXX
1	1	0	1	XXXXXXXXX
1	1	1	0	XXXXXXXXX
1	1	1	1	XXXXXXXXX

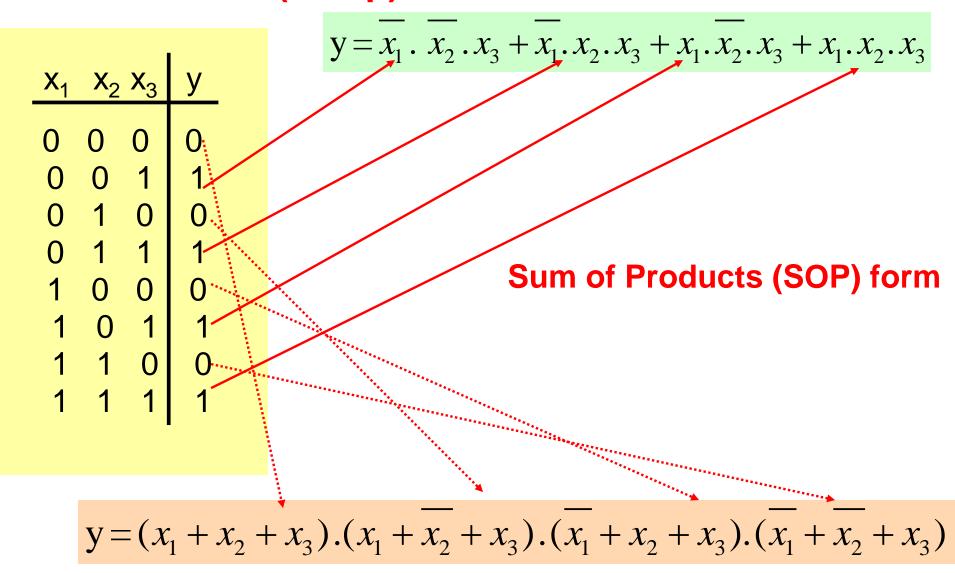
Don't care terms can be chosen as 0 or 1. Depending on the problem, we can choose the don't care term as 1 and use it to obtain a simpler Boolean expression

Y <sub>3</sub>	00	01	11	10	
ab 00	0	0	1	0	
01	0	0	0	0	
11	Х	Х	Х	Х	
10	0	0	X	Х	

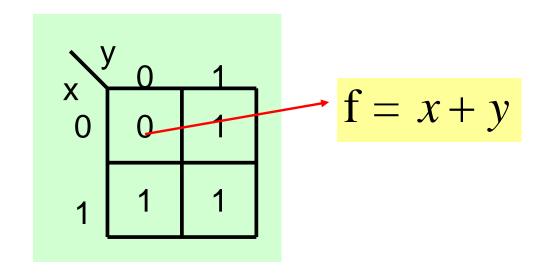
$$y_3 = \overline{b}.c.d$$

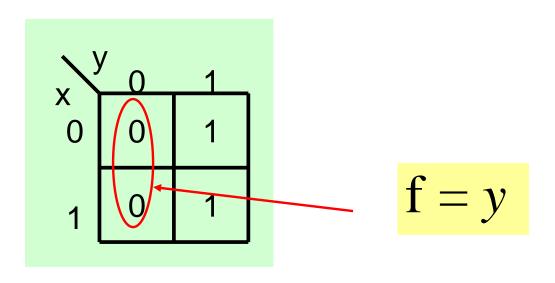
Don't care terms should only be included in encirclements if it helps in obtaining a larger grouping or smaller number of groups.

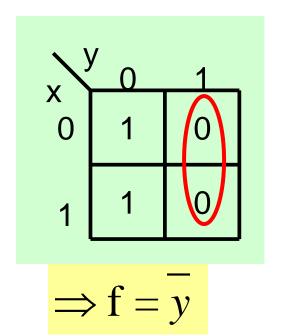
#### **SOP/POS form (recap)**

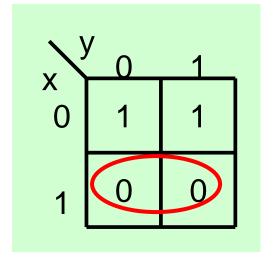


# Minimization of Product of Sum Terms using Kmap

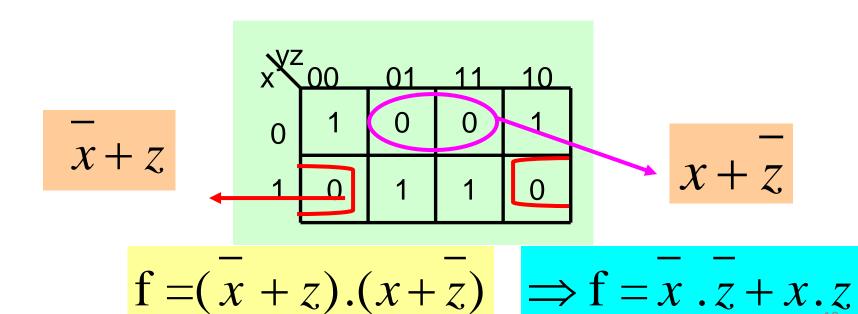








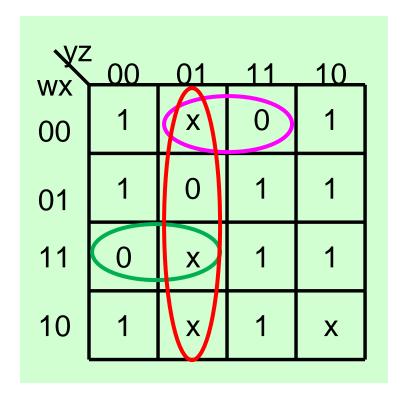
$$\Rightarrow$$
 f = x



$$f = (x + y + z).(x + y + z).(w + y + z).(w + x + z)$$

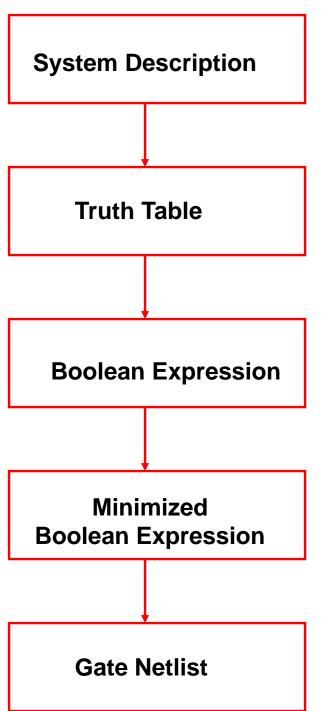
#### **Example**

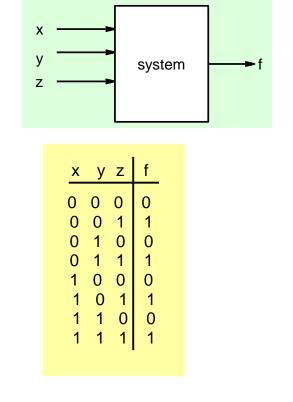
Obtain the minimized PoS by suitably using don't care terms



$$f = (w + x + z)(w + x + y)(y + z)$$

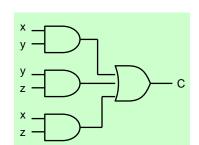
# **Design Flow**





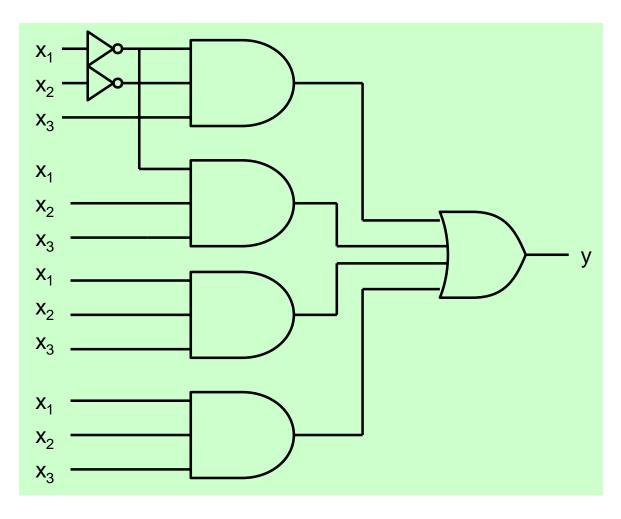
$$f = x.y.z + x.y.z + x.y.z + x.y.z$$

$$\Rightarrow$$
 f =  $\bar{x} \cdot \bar{z} + x \cdot z$ 



# Mapping of Boolean expression to a Network of gates available in the library

$$y = \overline{x_1} \cdot \overline{x_2} \cdot x_3 + \overline{x_1} \cdot x_2 \cdot x_3 + x_1 \cdot \overline{x_2} \cdot x_3 + x_1 \cdot x_2 \cdot x_3$$



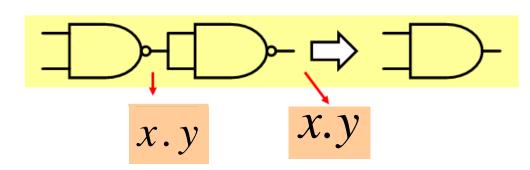
## Implementation using only NAND gates

**NAND** to Inverter

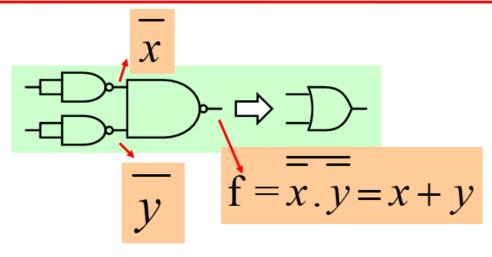


$$x.x = x$$

**NAND to AND** 

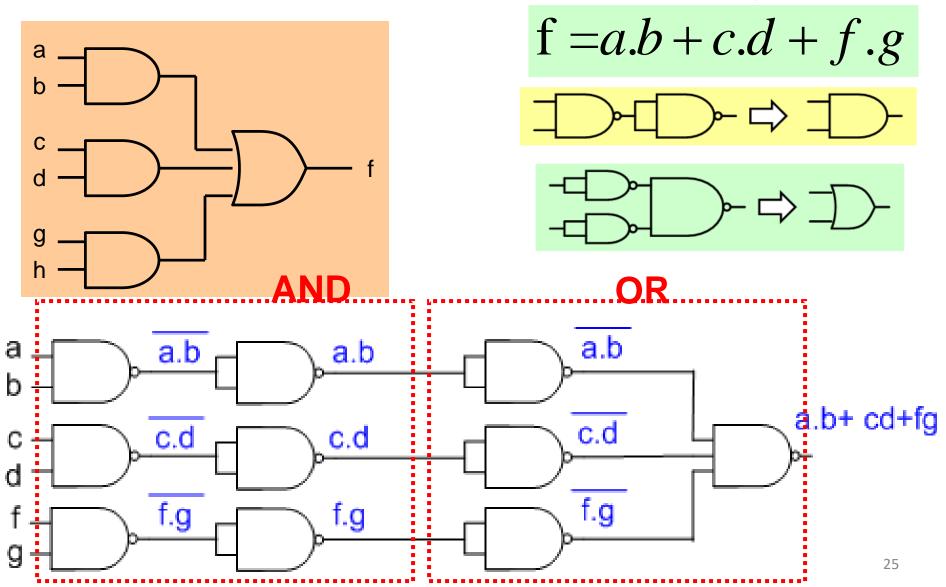


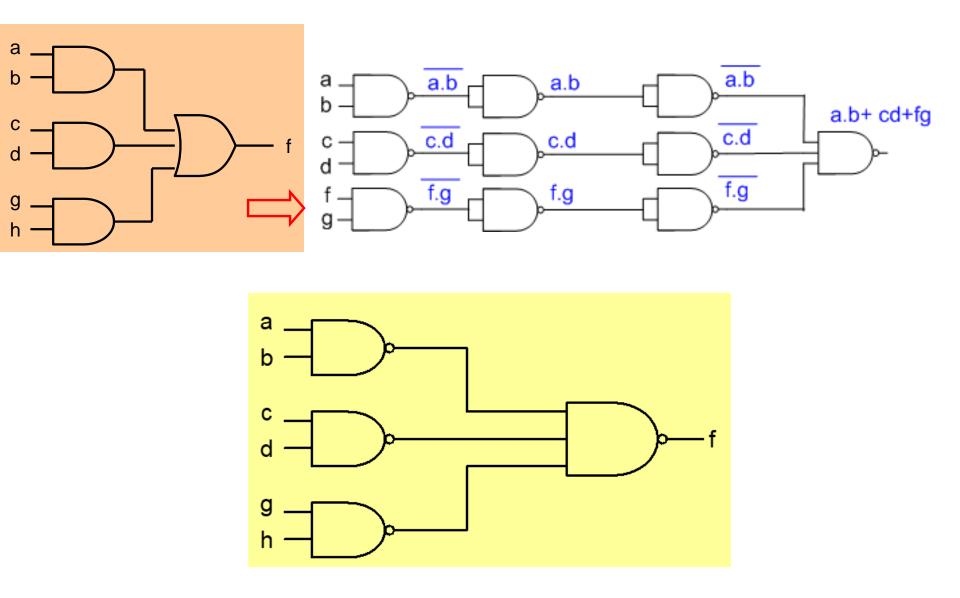
**NAND to OR** 



## Implementation using only NAND gates

A SoP expression is easily implemented with NAND gates.



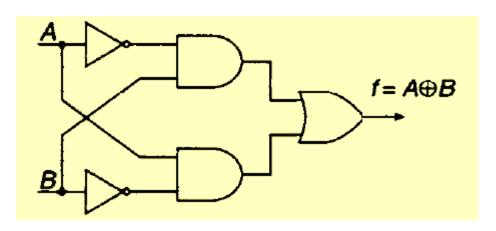


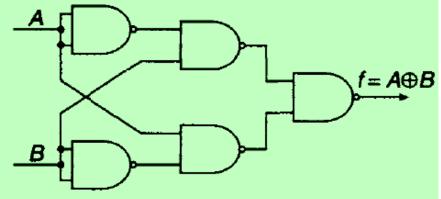
There is a one-to-one mapping between AND-OR network and NAND network

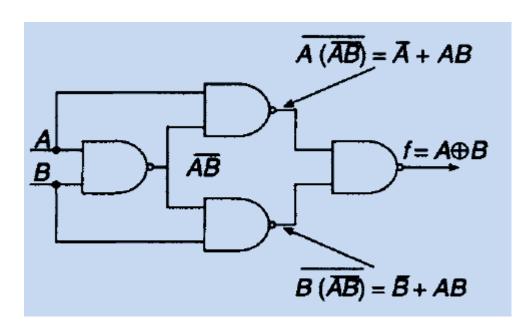
#### Often there is lot of further optimization that can be done

Consider implementation of XOR gate f = A.B + A.B

$$f = \overline{A}.B + A.\overline{B}$$

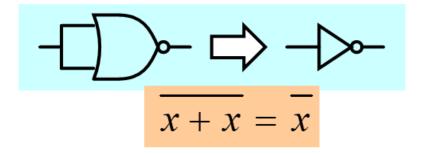




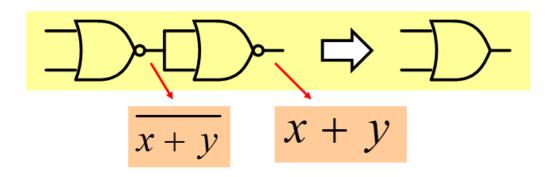


## Implementation using only NOR gates

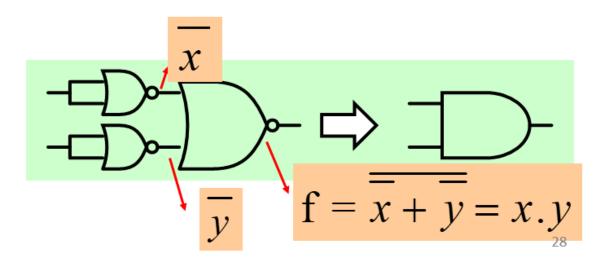
**NOR** to Inverter



**NOR** to **OR** 

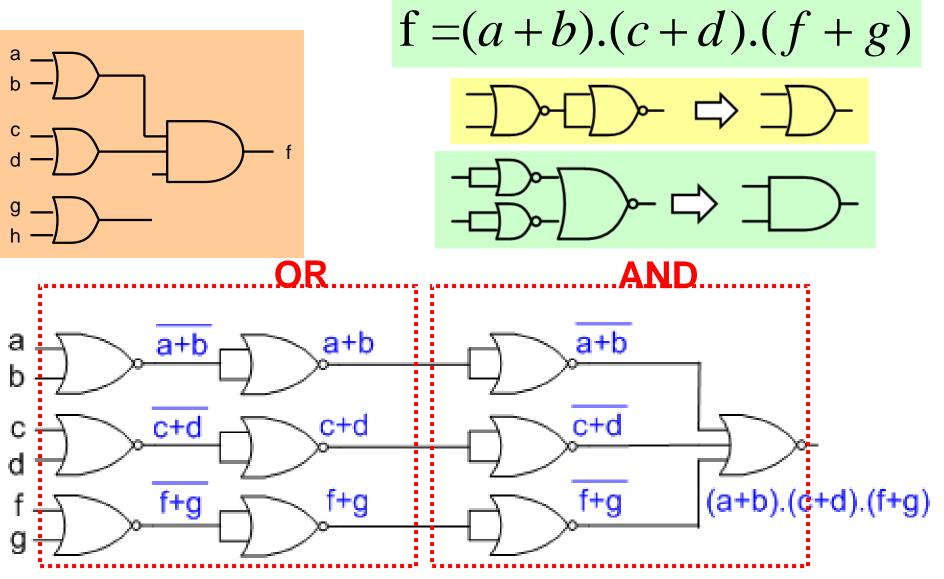


**NOR to AND** 

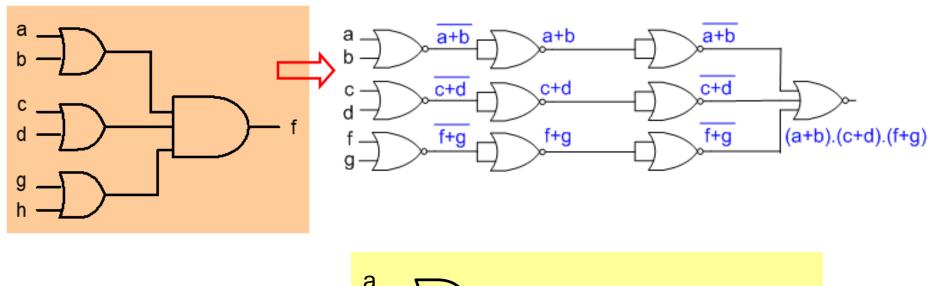


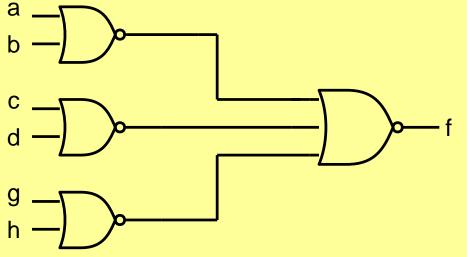
## Implementation using only NOR gates

To implement using NOR gates, it is easiest to start with minimized Boolean expression in POS form



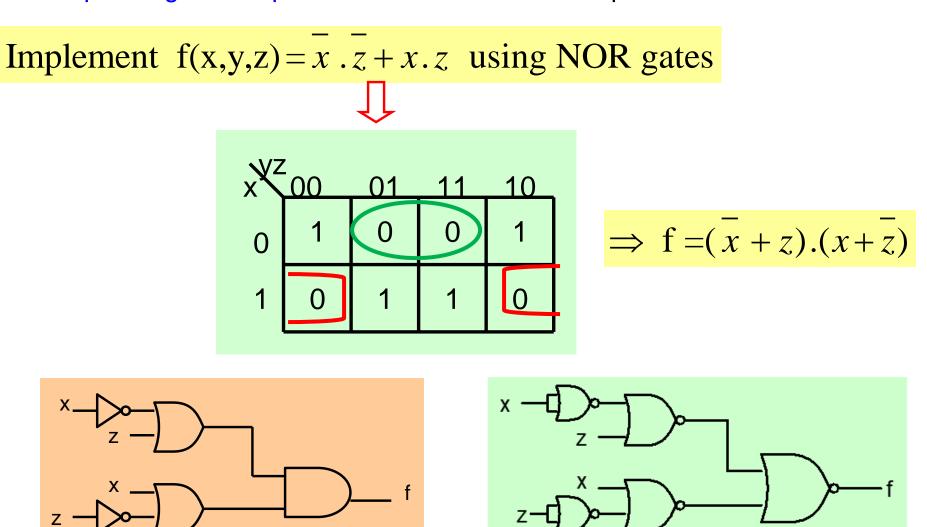
$$f = (a+b).(c+d).(f+g)$$





There is a one-to-one mapping between OR-AND network and NOR network

To implement SoP expression using NOR gates, determine first the corresponding PoS expression and then follow the procedure outlined earlier



Similarly PoS expression can be implemented as NAND network by first converting it to SoP expression and then following the procedure outlined earlier



How do we get the chocolate?