ESc201 : Introduction to Electronics

Digital Circuits

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Comparator

$$A = A_3 A_2 A_1 A_0$$

$$B = B_3 B_2 B_1 B_0$$

$$x_i = A_i.B_i + \overline{A_i}.\overline{B_i} \quad \text{for i} = 0,1,2,3$$

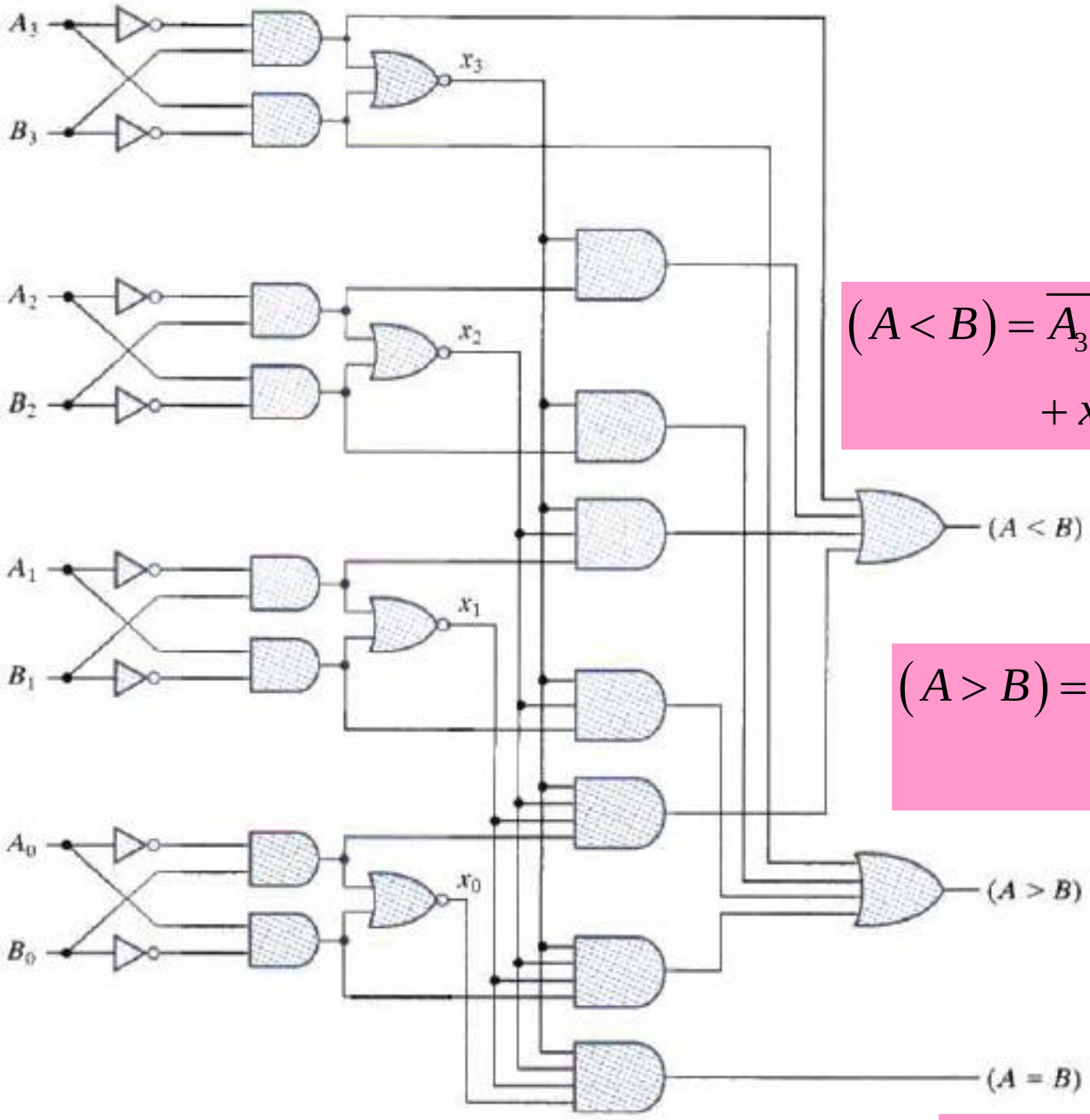
where x_i = *1 only if the pair of bits in position i are equal (i.e., if both are 1 or both are: 0).*

$$(A = B) = x_3 x_2 x_1 x_0$$

all x_i *variable must be equal to 1*

$$(A > B) = A_3 \overline{B_3} + x_3 A_2 \overline{B_2} + x_3 x_2 A_1 \overline{B_1} + x_3 x_2 x_1 A_0 \overline{B_0}$$

$$(A < B) = \overline{A_3} B_3 + x_3 \overline{A_2} B_2 + x_3 x_2 \overline{A_1} B_1 + x_3 x_2 x_1 \overline{A_0} B_0$$

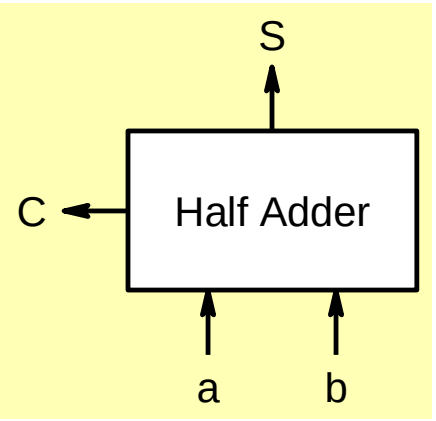


$$(A < B) = \overline{A_3} B_3 + x_3 \overline{A_2} B_2 + x_3 x_2 \overline{A_1} B_1 + x_3 x_2 x_1 \overline{A_0} B_0$$

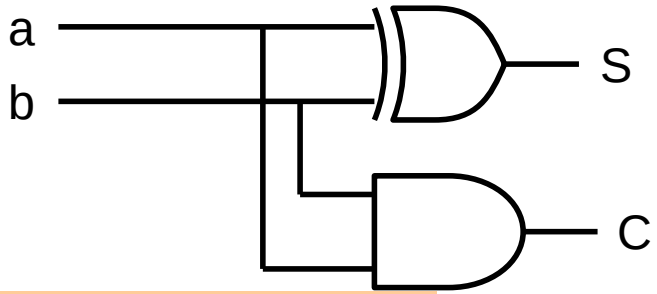
$$(A > B) = A_3 \overline{B_3} + x_3 A_2 \overline{B_2} + x_3 x_2 A_1 \overline{B_1} + x_3 x_2 x_1 A_0 \overline{B_0}$$

$$(A = B) = x_3 x_2 x_1 x_0$$

Adder



a	b	S	C
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1



$$S = \bar{a}.b + a.\bar{b}; C = a.b$$

```
   1
  1 1 1
  1 1 0
 --------
1 1 0 1
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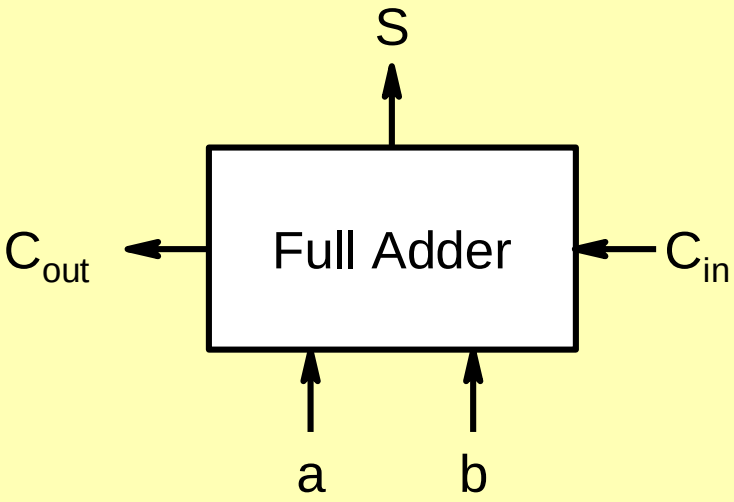


a	b	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

$$S = \bar{a}.\bar{b}.c_{in} + \bar{a}.b.\overline{c_{in}} + a.\bar{b}.\overline{c_{in}} + a.b.c_{in};$$

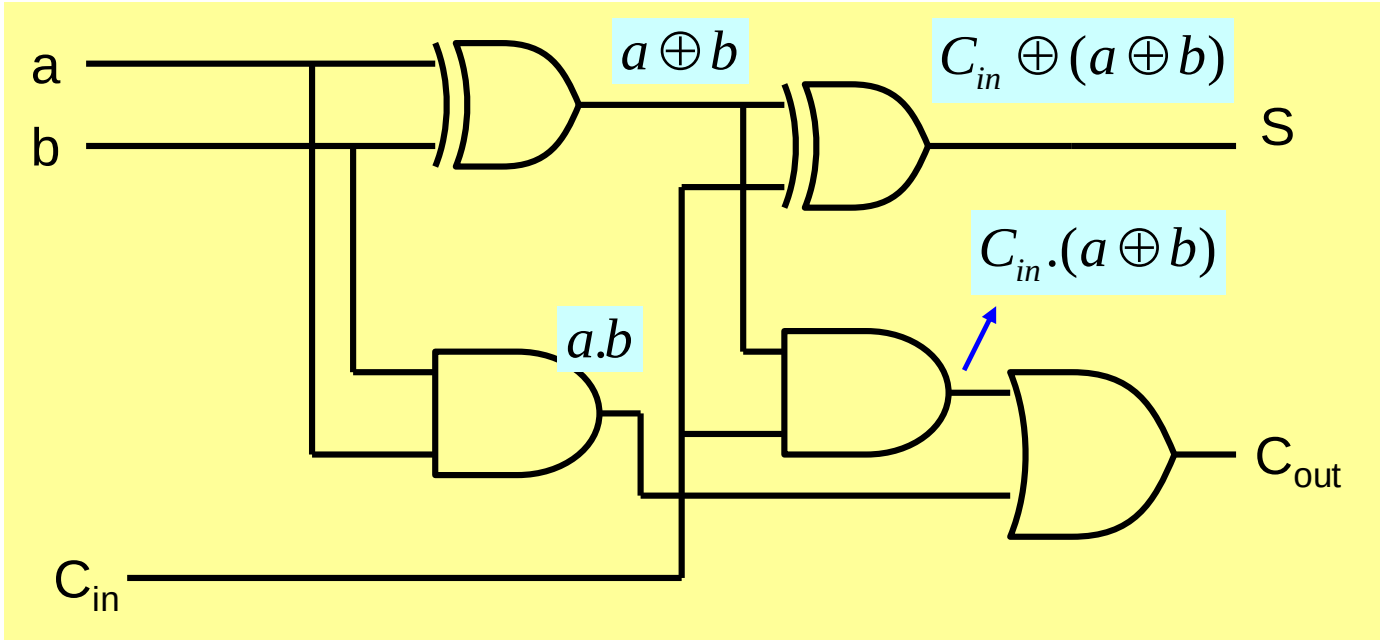
$$C_{out} = \bar{a}.b.c_{in} + a.\bar{b}.c_{in} + a.b.\overline{c_{in}} + a.b.c_{in}$$

$$S = \bar{a}.\bar{b}.c_{in} + \bar{a}.b.\overline{c_{in}} + a.\bar{b}.\overline{c_{in}} + a.b.c_{in}$$

$$S = C_{in} \oplus (a \oplus b)$$

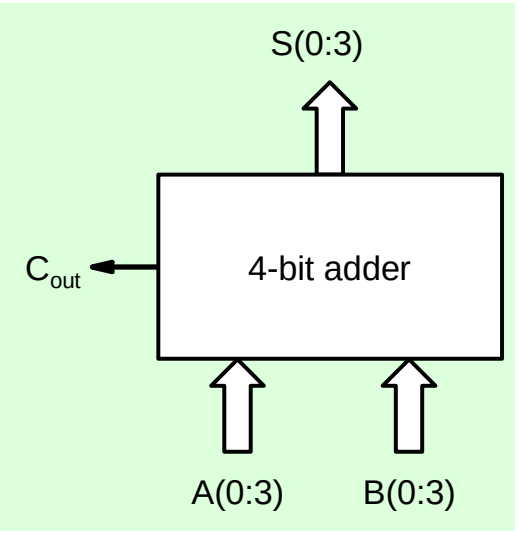
$$C_{out} = \bar{a}.b.C_{in} + a.\bar{b}.C_{in} + a.b.\overline{C_{in}} + a.b.C_{in}$$

$$C_{out} = C_{in}(a.\bar{b} + \bar{a}.b) + a.b = C_{in}.(a \oplus b) + a.b$$



a	b	C_{in}	S	C_{out}
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

4-bit Adder



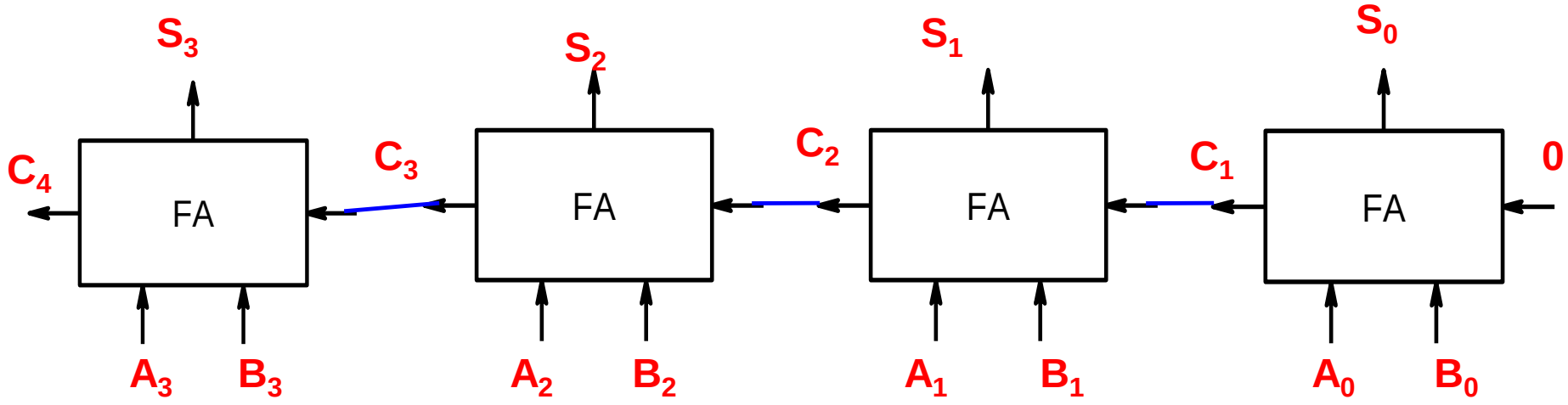
$A_3A_2A_1A_0$	$B_3B_2B_1B_0$	$S_3S_2S_1S_0$	C_{out}
0000	0000	0000	0
0000	0001	0001	0
0001	0000	0001	0
⋮	⋮	⋮	⋮

$C_3\ C_2\ C_1$

$A_3\ A_2\ A_1 A_0$

$B_3\ B_2\ B_1 B_0$

C_4 $S_3\ S_2\ S_1 S_0$



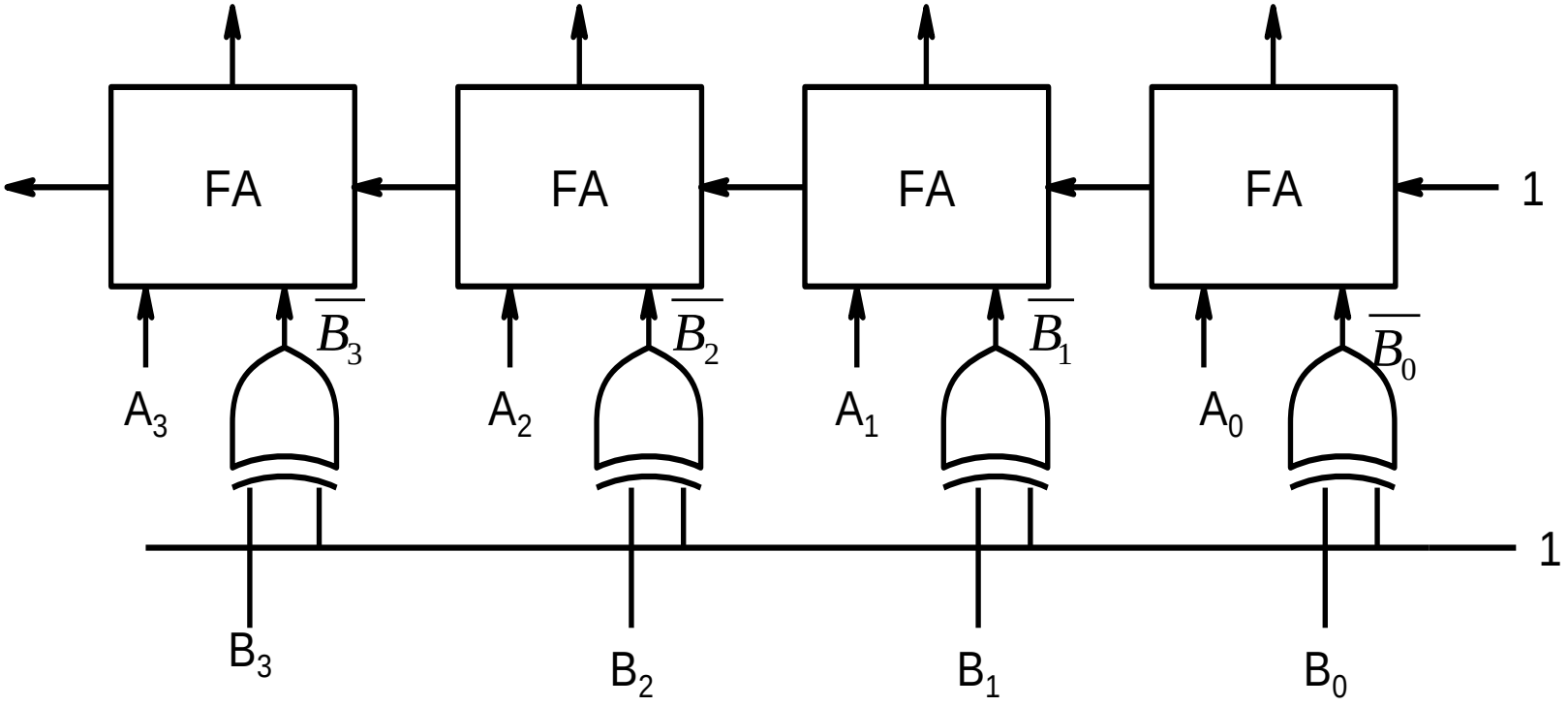
FA = Full Adder

Subtraction

A - B = A + 2's complement of B

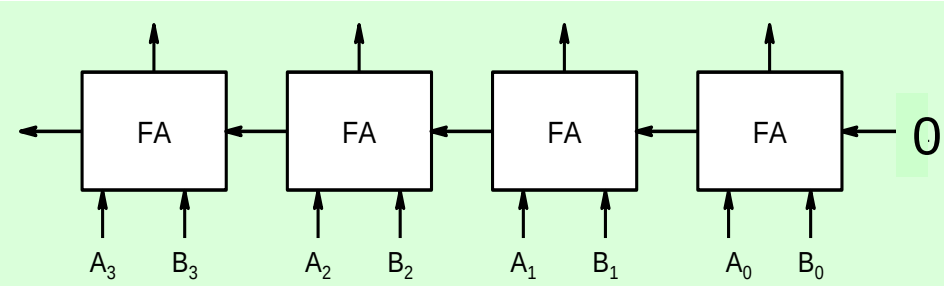
$$A - B = A + \overline{B} + 1$$

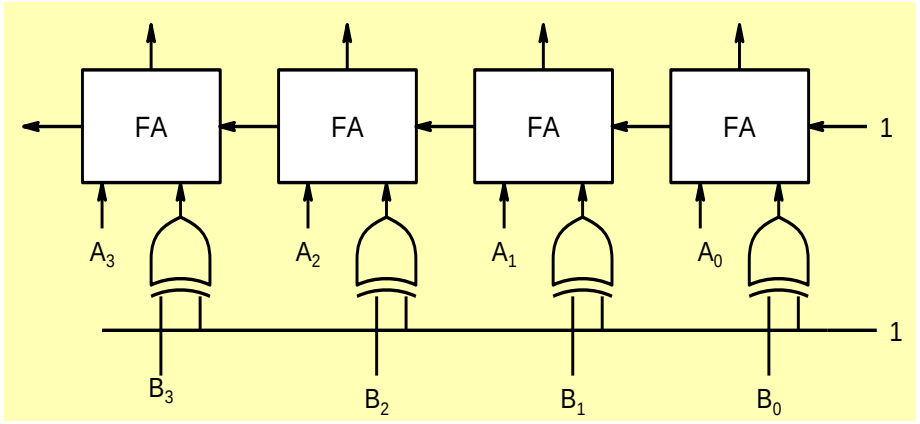
A - B = A + 1's complement of B+1

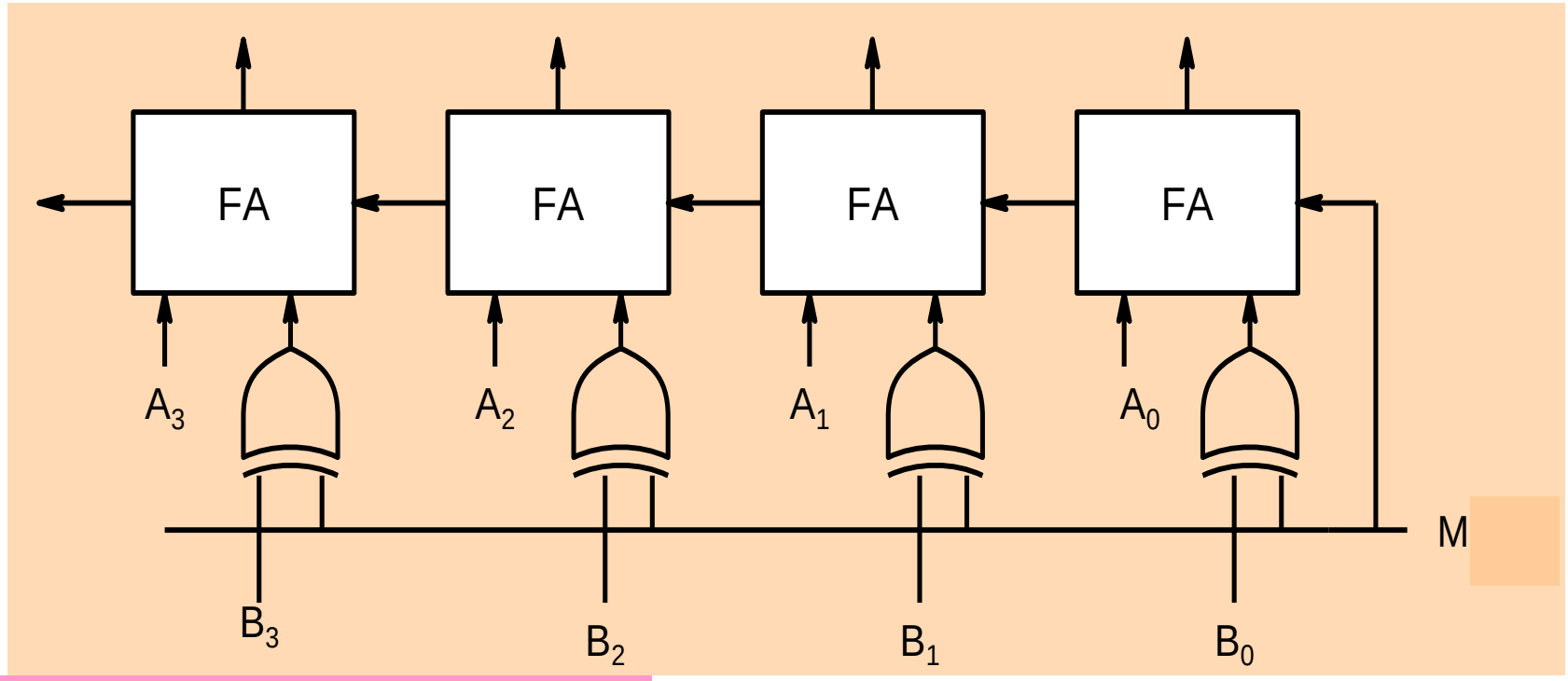


$$B_0 \oplus 1 = B_0.\bar{1} + \overline{B_0}.1 = \overline{B_0}$$

Adder/Subtractor







$$B_0 \oplus 0 = B_0.\bar{0} + \overline{B_0}.0 = B_0$$

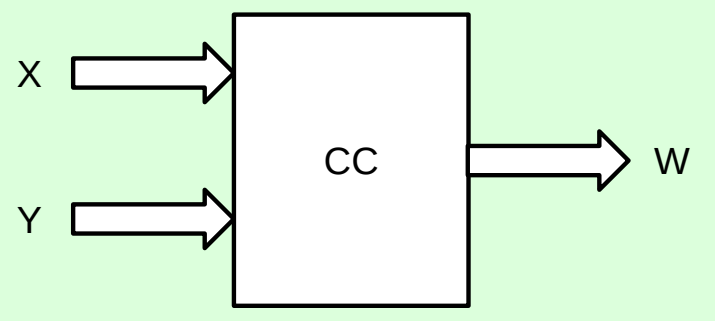
$$B_0 \oplus 1 = B_0.\bar{1} + \overline{B_0}.1 = \overline{B_0}$$

$M = 0$ for Adder

M=1 for Subtractor

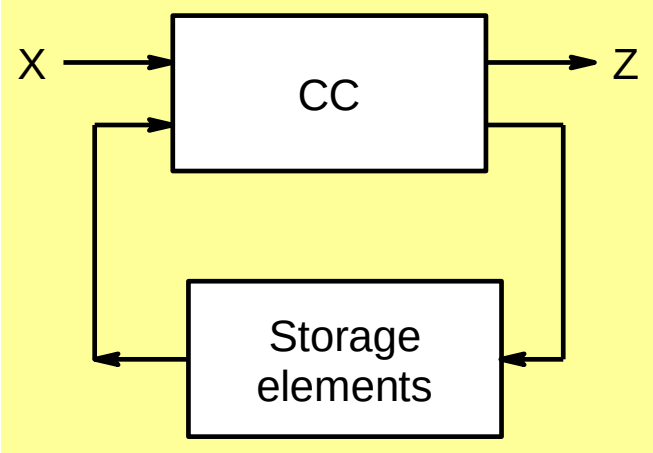
Digital Circuits

Combinational Circuits



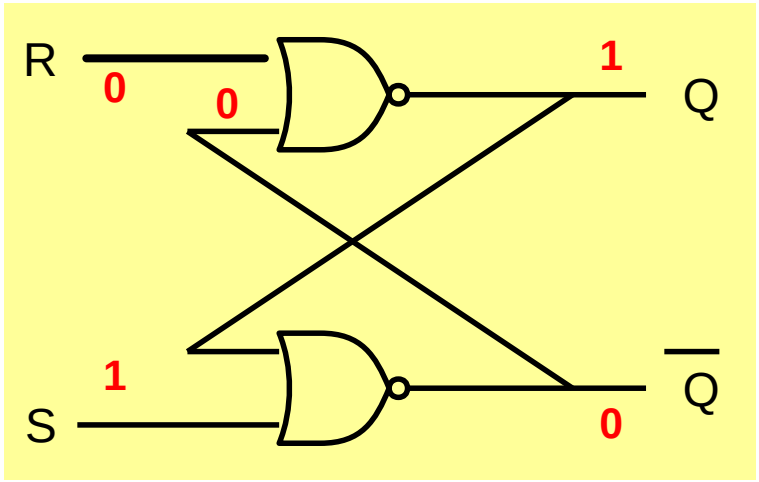
Output is determined by current values of inputs only.

Sequential Circuits



Output is determined in general by current values of inputs and past values of inputs/outputs as well.

NOR SR Latch (Set-Reset Latch)

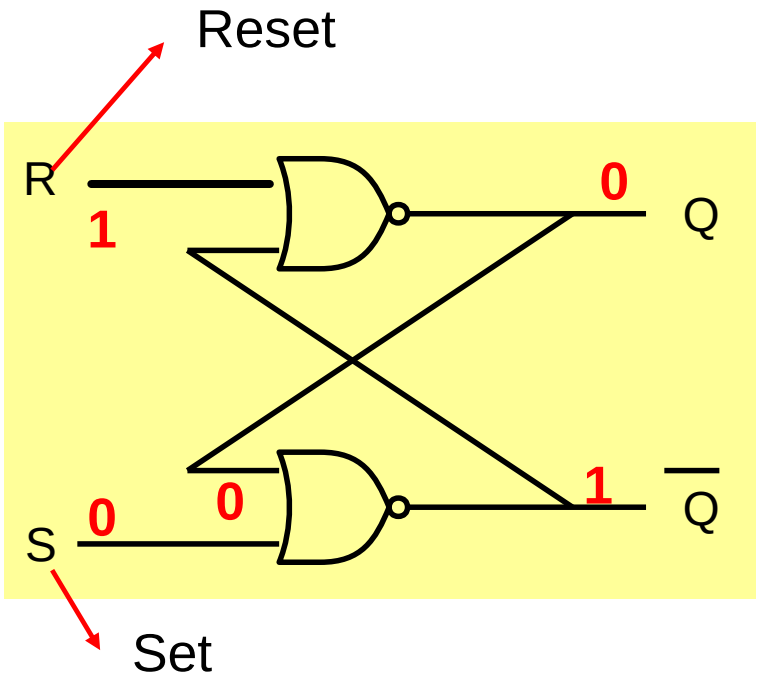


$Q = 1; \overline{Q} = 0$ Set State

$Q = 0; \overline{Q} = 1$ Re set State

S	R	Q	$\overline{Q}$	State
1	0	1	0	SET

NOR SR Latch

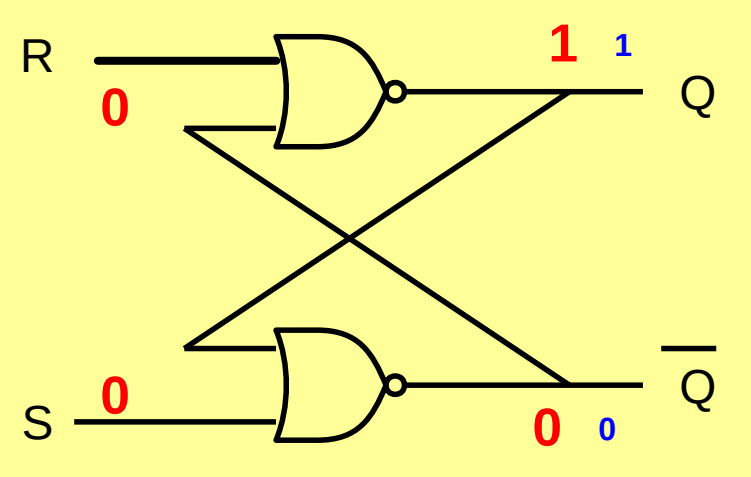


$Q = 1; \overline{Q} = 0$ Set State

$Q = 0; \overline{Q} = 1$ Re set State

S	R	Q	$\overline{Q}$	State
1	0	1	0	SET
0	1	0	1	RESET

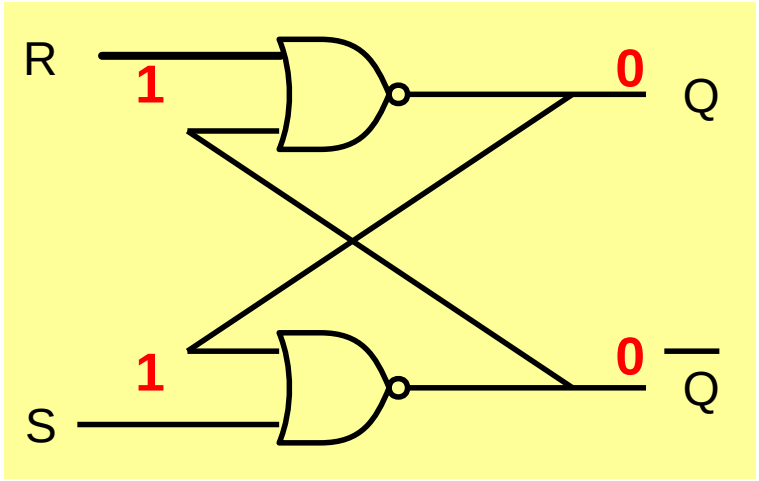
HOLD State



S	R	Q	$\overline{Q}$	State
1	0	1	0	SET
0	0	1	0	HOLD
0	1	0	1	RESET
0	0	0	1	HOLD

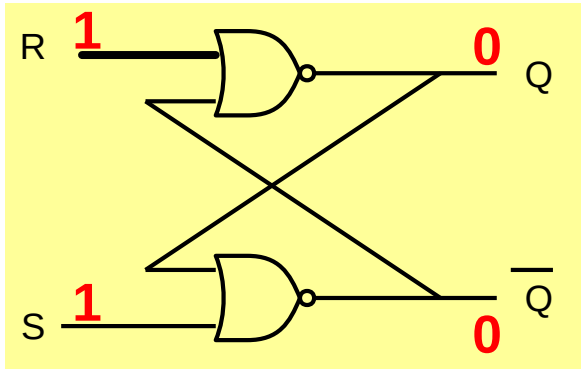
S	R	Q	$\overline{Q}$	State
1	0	1	0	SET
0	1	0	1	RESET
0	0	Q	$\overline{Q}$	HOLD
1	1	0	0	INVALID

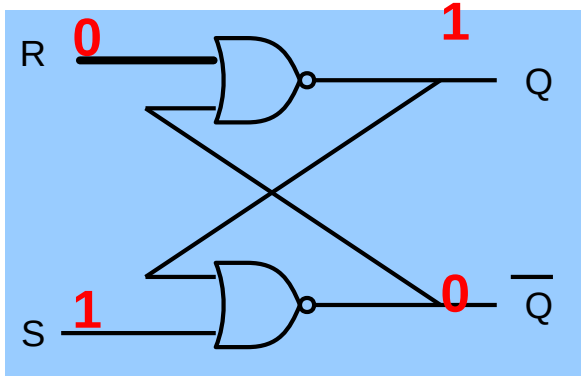
1 bit memory?

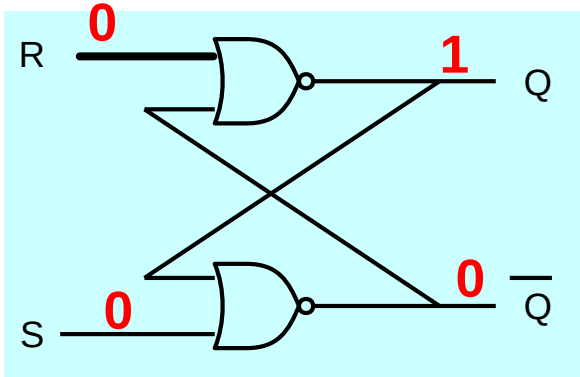


Both the outputs are well defined and 0. The first problem is that we do not get complementary output.

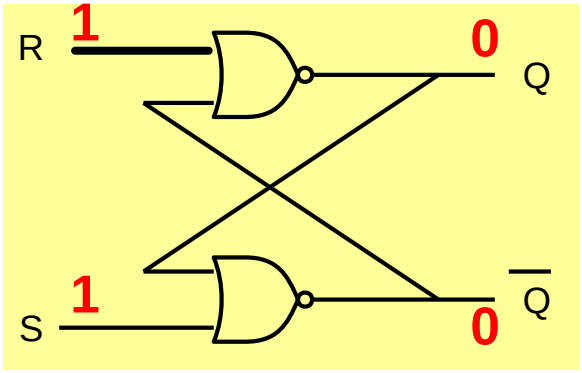
A more serious problem occurs when we switch the latch to the hold state by changing RS from 11 → 00 . Suppose the inputs do not change simultaneously and we get the situation 11 → 01* → 00

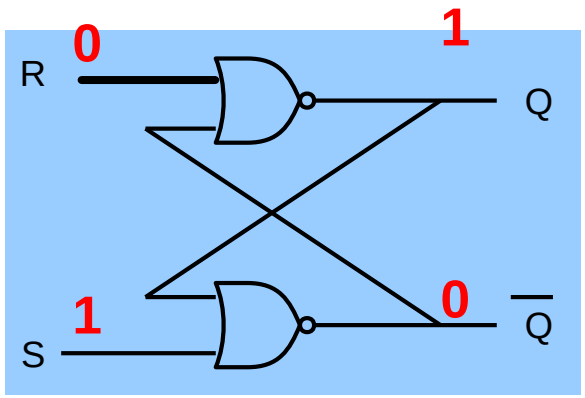


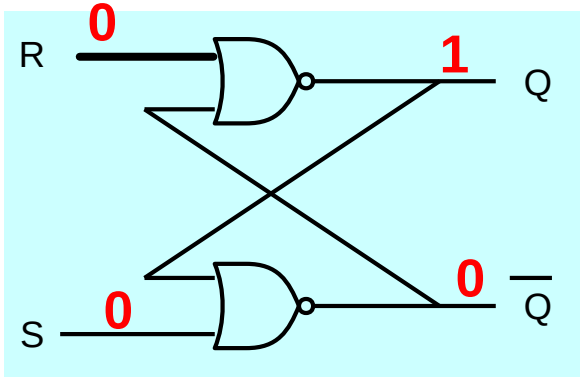




Q = 1

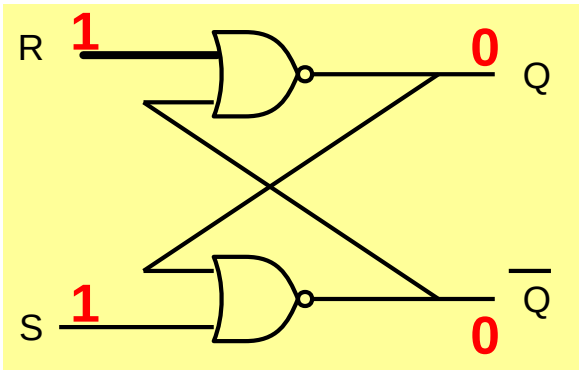


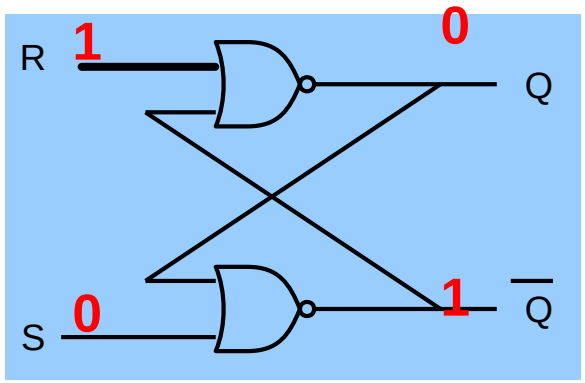


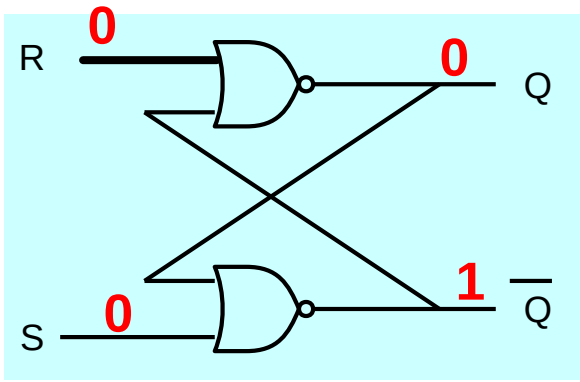


Q = 1

Suppose the inputs change as RS = 11 → 10* → 00







Q = 0

So although output is well defined when we apply RS = 11, it becomes unpredictable once we switch the latch to hold state by applying RS = 00. That is why RS = 11 is not used as an input combination.