ESC201A EndSem Part 3

SAMYAK SINGHANIA

TOTAL POINTS

16 / 20

QUESTION 1

Q1 10 pts

1.1 1(a) 2 / 2

✓ **+ 2 pts** *Completely Correct*

+ **0 pts** Completely Incorrect
+ **0 pts** Not Attempted
+ **0 pts** Copied

1.2 1(b) 3 / 3

+ **3 pts** Completely Correct
+ **0 pts** Completely Incorrect
+ **0 pts** Not Attempted
+ **0 pts** Copied

✓ **+ 1 pts** *Correct number of 1 to 2 decoders used*

✓ **+ 2 pts** *Final implementation correct*

1.3 1(c) 1 / 5

+ **5 pts** Completely Correct
+ **0 pts** Completely Incorrect
+ **0 pts** Not Attempted
+ **0 pts** Copied
+ **2 pts** Minimized PoS expression correct
+ **3 pts** Final implementation using 2-input NOR gates correct

+ 1 *Point adjustment*

QUESTION 2

Q2 10 pts

2.1 2(a) 4 / 4

✓ **+ 4 pts** *Completely Correct*

+ **0 pts** Completely Incorrect
+ **0 pts** Not Attempted
+ **0 pts** Copied
+ **2 pts** Excitation table correct
+ **2 pts** Final implementation correct

2.2 2(b) 6 / 6

✓ **+ 6 pts** *Completely Correct*

+ **0 pts** Completely Incorrect
+ **0 pts** Not Attempted
+ **0 pts** Copied
+ **1 pts** Counter states and transitions correctly identified
+ **3 pts** Assignment to D inputs of the two flip flops correct
+ **2 pts** Final implementation schematic correct

Department of Electrical Engineering, IIT Kanpur

End-Semester Exam (Part-III), Date: 19/11/2022 Duration: 55 minutes

ESc 201: Introduction to Electronics

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1 (a). Prove using basic postulates of Boolean algebra that $x+\bar{x}.y = x+y$. **[2]**

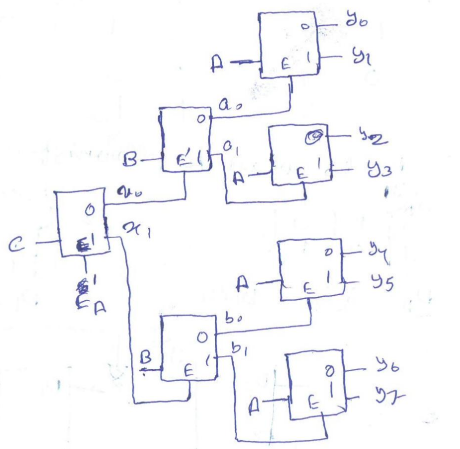
We know that $x+\bar{x}=1$

& $x+y.z=(x+y).(x+z)$

$\therefore x+\bar{x}.y=(x+\bar{x}).(x+y) = x+y$

1(b). Implement a 3 to 8 decoder using only 1 to 2 decoders. Assume that each decoder has an enable signal. Label all the input and output lines. [3]

C B A
0 0 0
0 0 1
0 1 0
0 1 1
1 0 0
1 0 1
1 1 0
1 1 1



~~When C=0~~

C	x_0	x_1
0	1	0
1	0	1

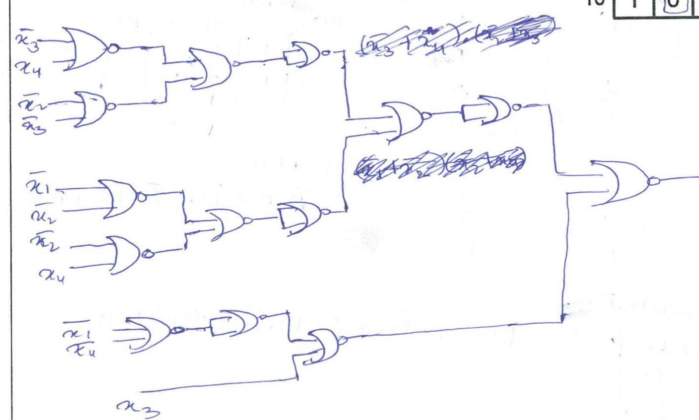
When $E_A=0$
$y_i = 0$.

E_A	C B A	y_0	y_1	y_2	y_3	y_4	y_5	y_6	y_7
1	0 0 0	1	0	0	0	0	0	0	0
1	0 0 1	0	1	0	0	0	0	0	0
1	0 1 0	0	0	1	0	0	0	0	0
1	0 1 1	0	0	0	1	0	0	0	0
1	1 0 0	0	0	0	0	1	0	0	0
1	1 0 1	0	0	0	0	0	1	0	0
1	1 1 0	0	0	0	0	0	0	1	0
1	1 1 1	0	0	0	0	0	0	0	1

1(c). Determine the minimized product of Sum (PoS) expression for the K-map shown below and implement using only 2-input NOR gates. Assume that complements of input variables are also available and need not be generated using gates. [5]

X_1X_2 \ X_3X_4	00	01	11	10
00	1	1	1	0
01	0	1	0	0
11	0	0	0	0
10	1	0	1	0

$y=(\bar{x}_3+x_4)(\bar{x}_2+\bar{x}_3).(\bar{x}_1+\bar{x}_2).(\bar{x}_2+x_4).(\bar{x}_1+x_3+\bar{x}_4)$



2(a). For the Flip-flop with two inputs A and B whose characteristic table is shown below, determine first the excitation table and then implement the flip-flop using a D flip-flop and a 4 to 1 multiplexer. [4]

A B	Q(t+1)	State
0 0	1	Set
0 1	$\overline{Q}(t)$	Toggle
1 0	0	Reset
1 1	Q(t)	Hold

Excitation table

Q(t)	Q(t+1)	A	B
0	0	1	x
0	1	0	x
1	0	1 / 0	0 / 1
1	1	0 / 1	0 / 1

Q(t)	A	B	Q(t+1)
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Using k-map, we get

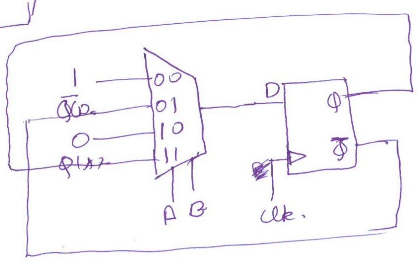
Q(t) \ AB	00	01	11	10
0	1	1	0	0
1	1	0	1	0

$\therefore Q(t+1)$
$= \bar{A}.\bar{B} + \bar{Q}(t).\bar{A} + Q(t).A.B$

We know that

D	Q(t+1)
0	0
1	1

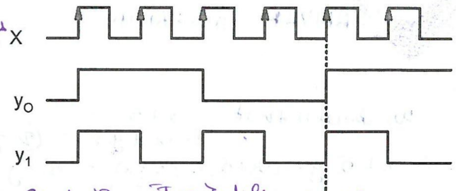
$\therefore D = \bar{A}.\bar{B} + \bar{Q}(t).\bar{A} + Q(t)\,A.B.$



A B	D
0 0	1
0 1	$\bar{Q}(t)$
1 0	0
1 1	Q(t)

2(b). Design a synchronous circuit using D flip-flops that can produce the outputs y_0 and y_1 from a clock input X as shown below. The output sequence repeats after the dotted line shown below. [6]

We use 2 D flip flops



We get the following State Transition Table

Previous State y_0	y_1	Next State y_0	y_1	D_0	D_1
0	0	1	1	1	1
1	1	1	0	1	0
1	0	0	1	0	1
0	1	0	0	0	0
0	0	1	1	1	1

For D_0, we get the following from K-map

y_0 \ y_1	0	1
0	1	0
1	0	1

$D_0 = \bar{y}_0\bar{y}_1 + y_0 y_1$

For D_1

y_0 \ y_1	0	1
0	1	0
1	1	0

$D_1 = \bar{y}_1$