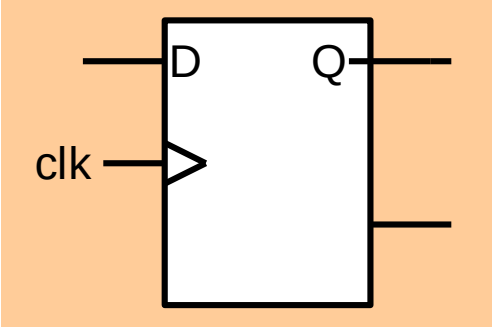
ESc201 : Introduction to Electronics

Counters

Amit Verma
Dept. of Electrical Engineering
IIT Kanpur

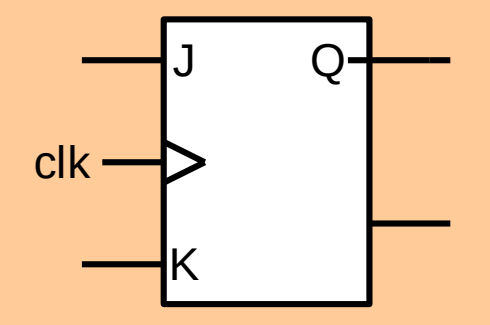
Recap

D Flip-flop



Inputs (D)	Q(t+1)
0	0
1	1

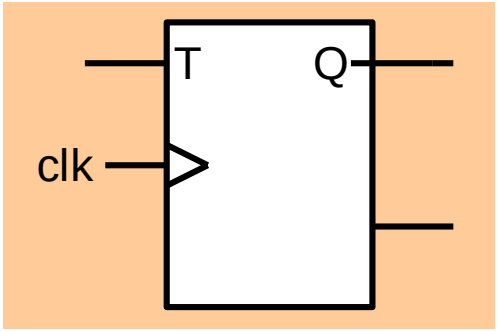
JK Flip-flop



Inputs J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q(t)}$

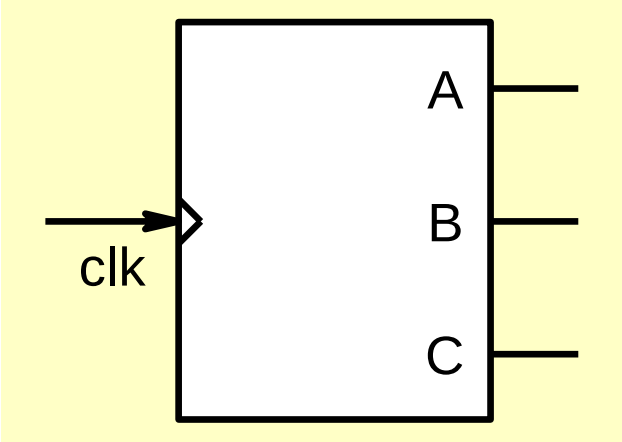
Recap

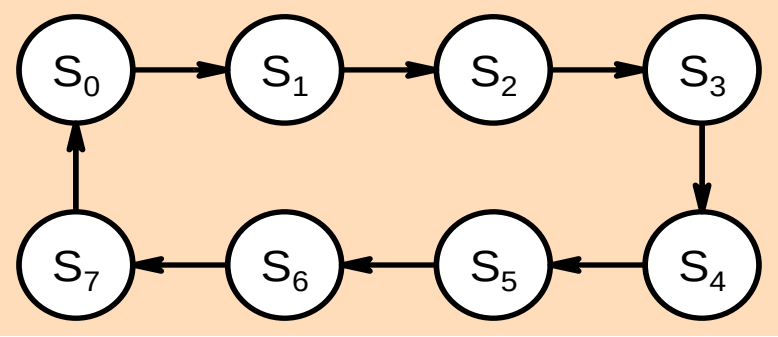
Toggle or T Flip-flop



Inputs (T)	Q(t+1)
0	Q(t)
1	$\overline{Q(t)}$

Counters

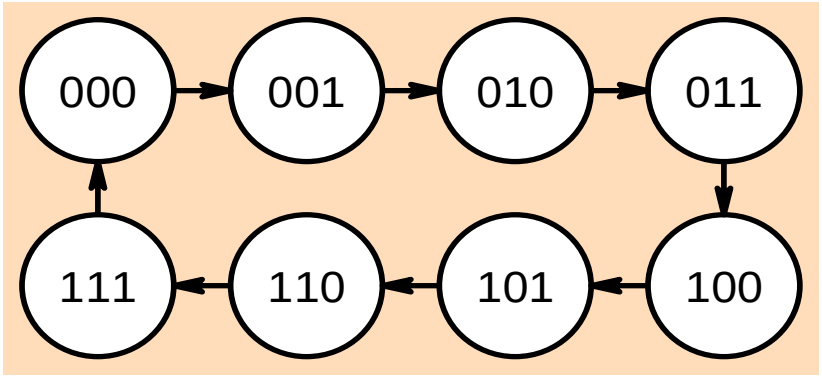




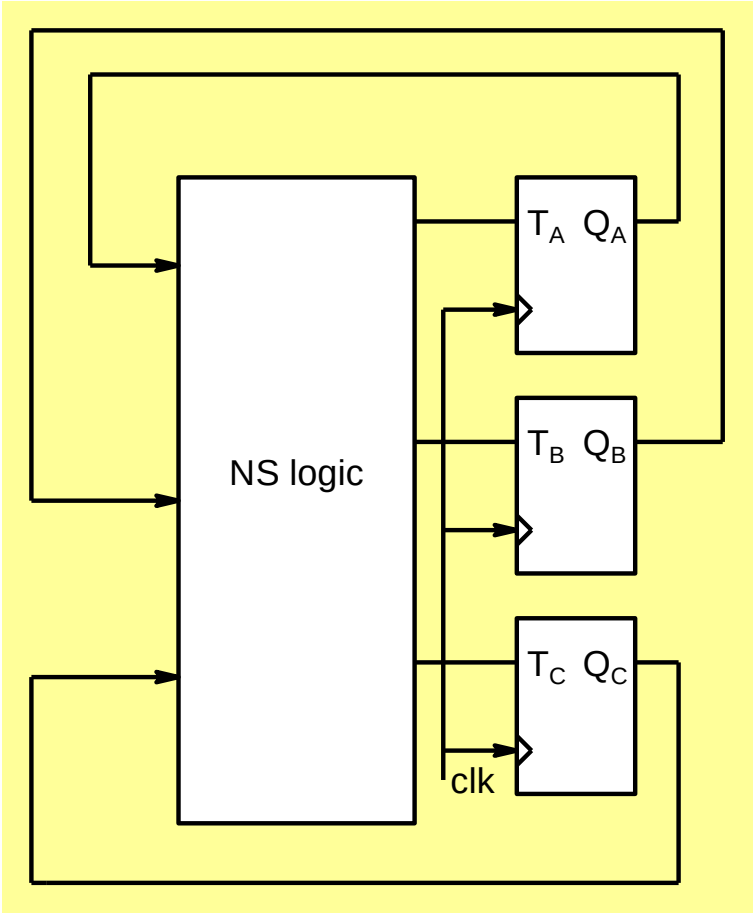
A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

In state S_0, the output ABC is 000, in S_1 001 and so on

There are 8 states so 3 FFs are at least required. Let us choose T FF.



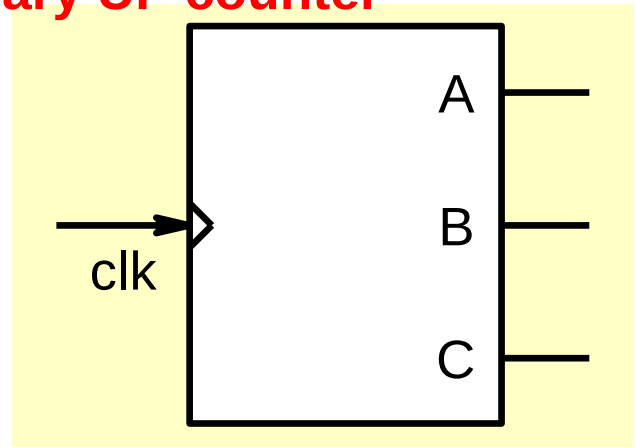
PS A B C	NS A B C	T_A T_B T_C
0 0 0	0 0 1	0 0 1
0 0 1	0 1 0	0 1 1
0 1 0	0 1 1	0 0 1
0 1 1	1 0 0	1 1 1
1 0 0	1 0 1	0 0 1
1 0 1	1 1 0	0 1 1
1 1 0	1 1 1	0 0 1
1 1 1	0 0 0	1 1 1



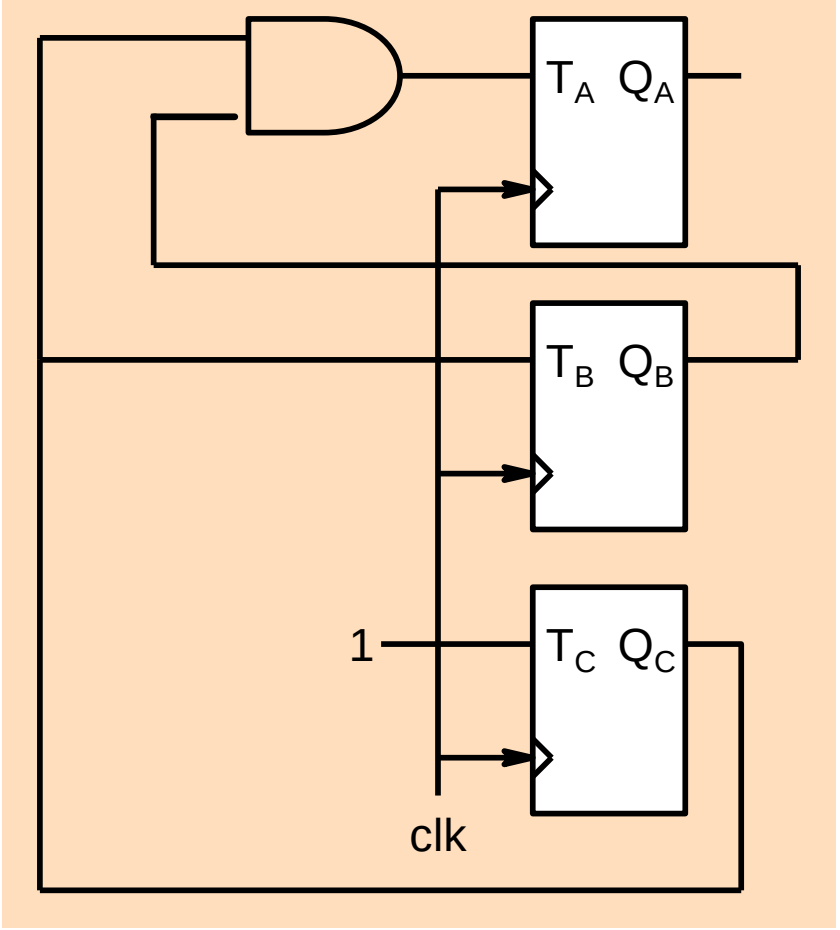
$$T_A = B.C \; ; \; T_B = C \; ; \; T_C = 1$$

Please prove this!

Binary UP counter

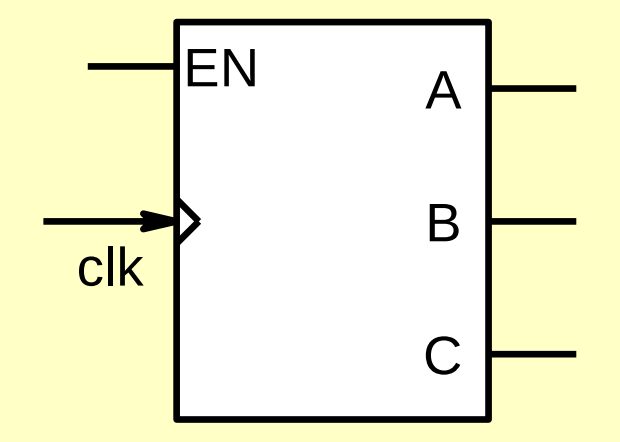


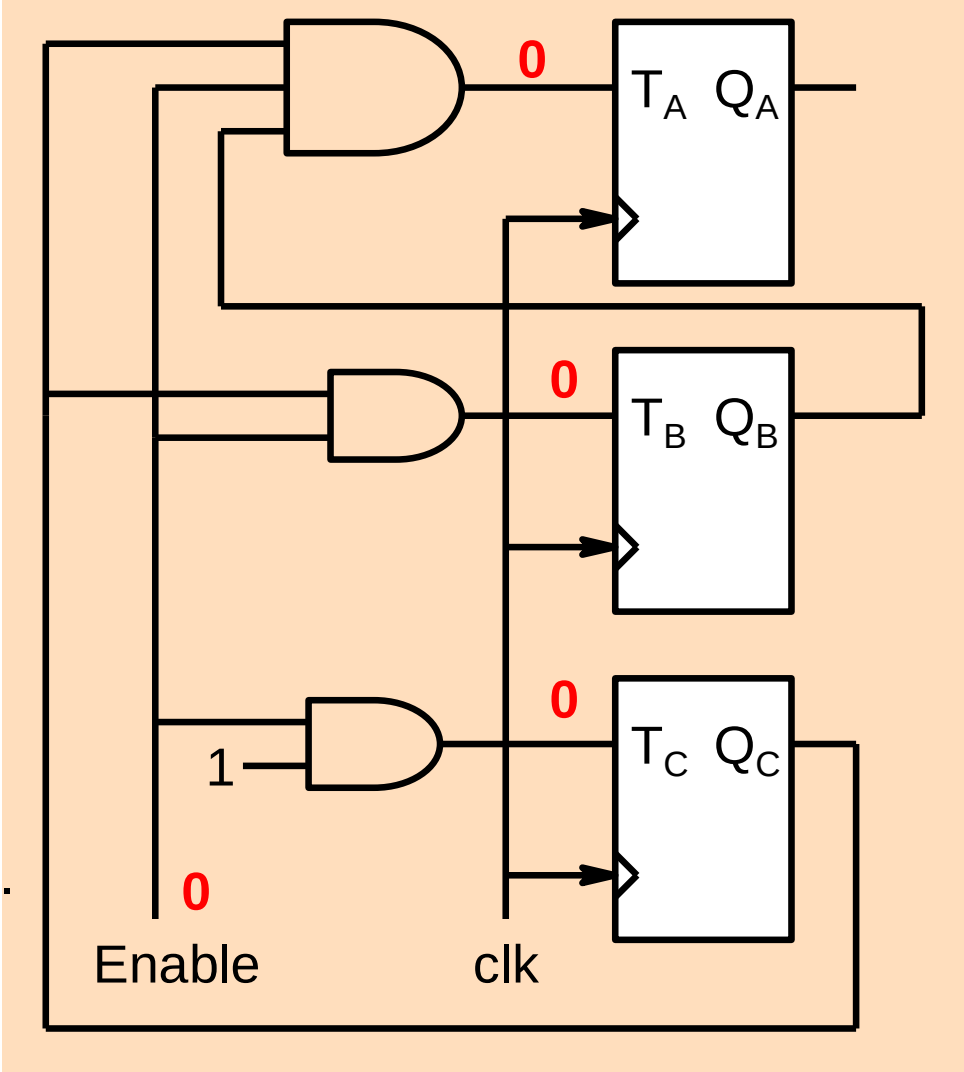
A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1



$$T_A = B.C \; ; \; T_B = C \; ; \; T_C = 1$$

Counter with Enable

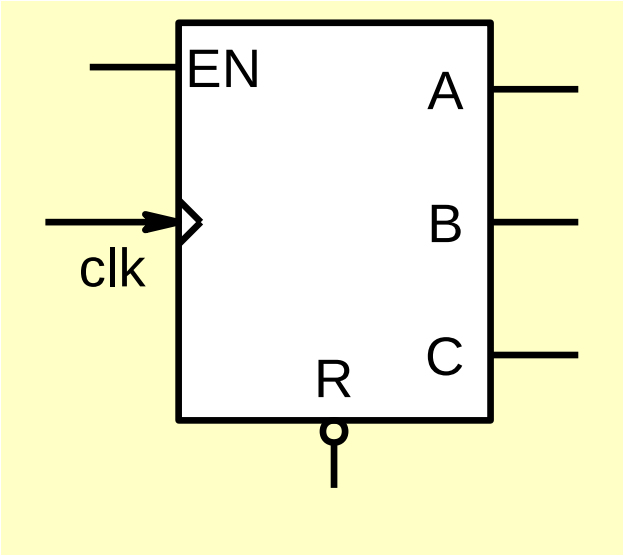


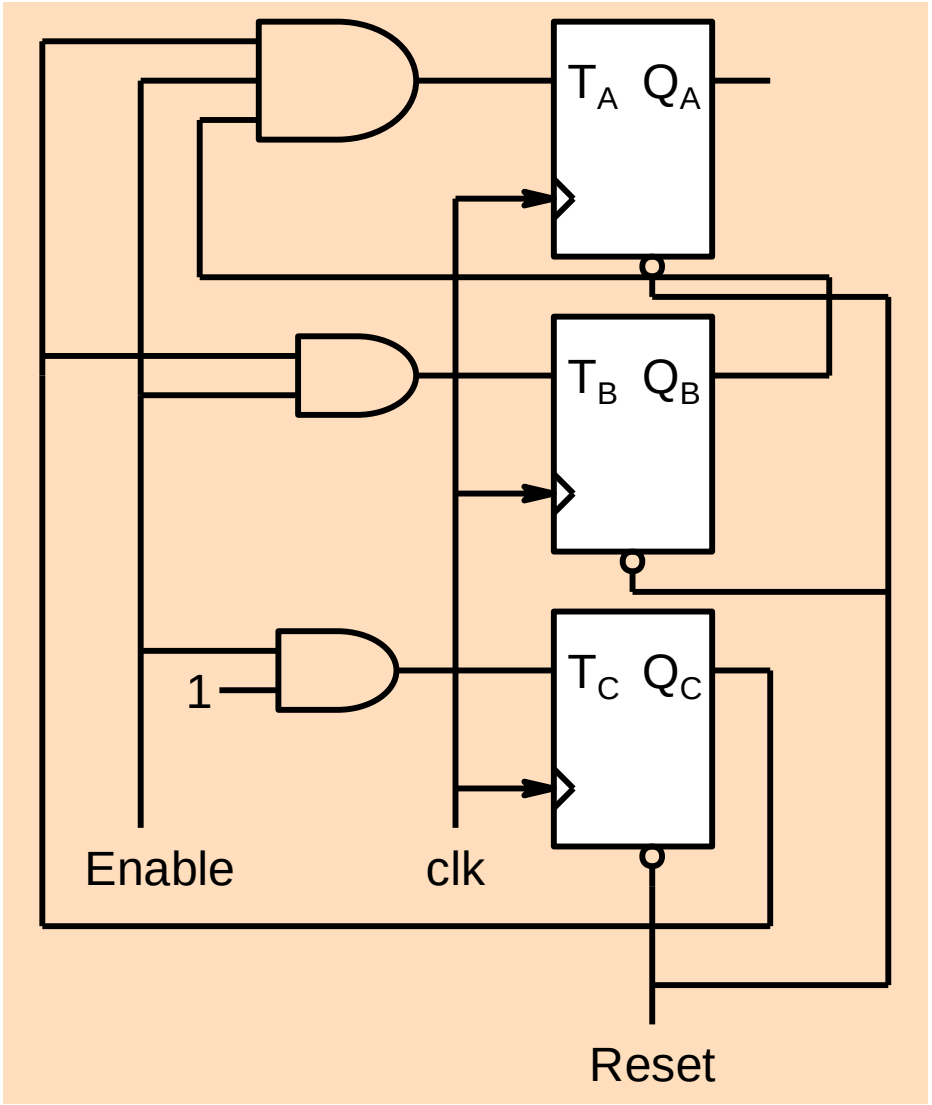


Counter is in Hold state.

When Enable = 1, the counter begins the count.

Counter with Asynchronous Reset



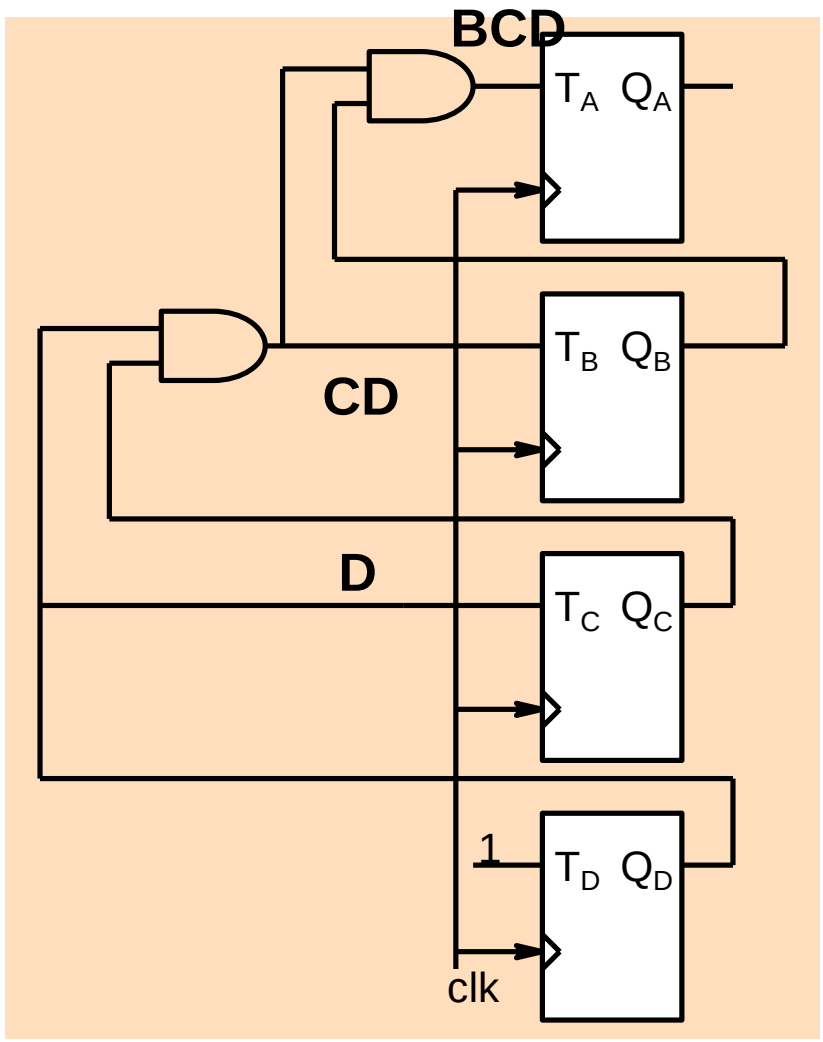


When Reset = 1, counter gets initialized to a known state.

-D toggles every clock cycle
-C toggles only when D is 1
-B toggles only when both C and D are 1
-A toggles only when B C D are 1

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	10	
0	1	1	1
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0
1	1	0	1
1	1	1	0
1	1	1	1
0	0	0	0

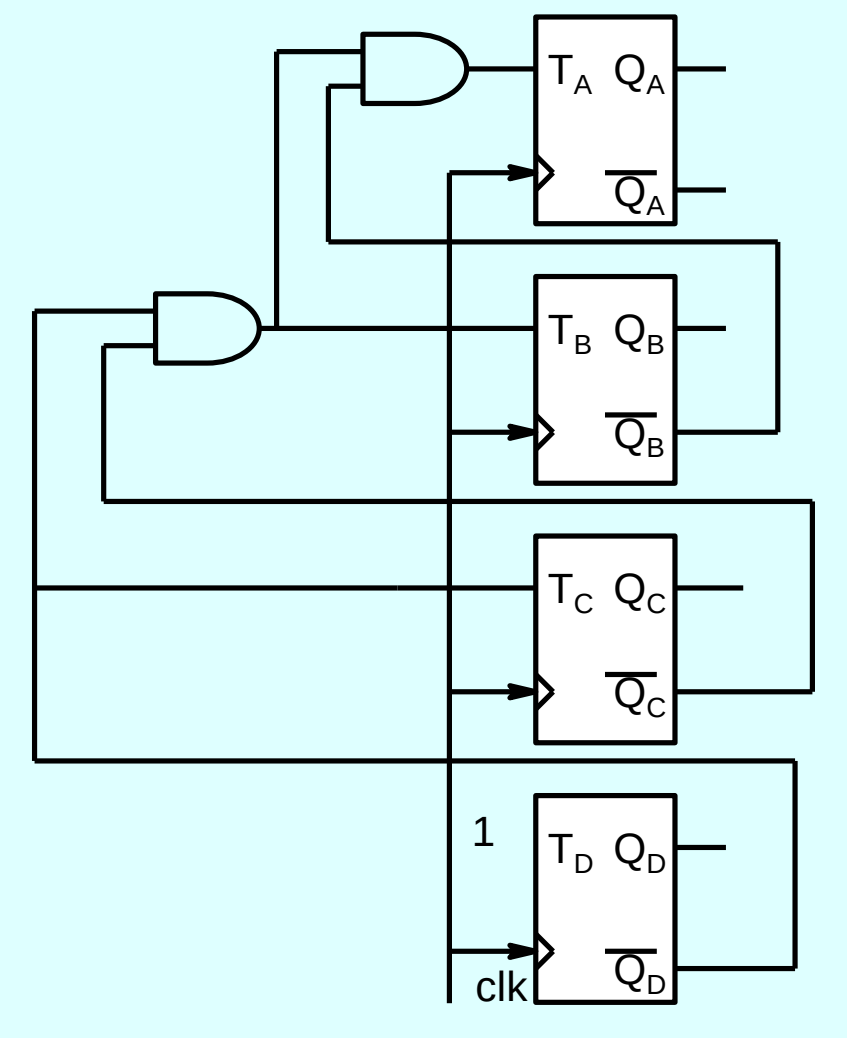
T FF toggles when T=1



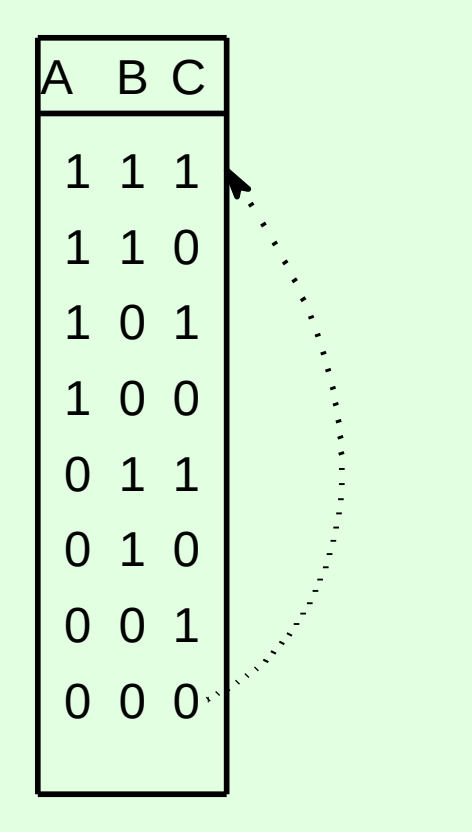
4-bit Down Counter

A	B	C	D
1	1	1	1
1	1	1	0
1	1	0	1
1	1	0	0
1	0	1	1
1	0	1	0
1	0	0	1
1	0	0	0
0	1	1	1
0	1	1	0
0	1	0	1
0	1	0	0
0	0	1	1
0	0	1	0
0	0	0	1
0	0	0	0
1	1	1	1

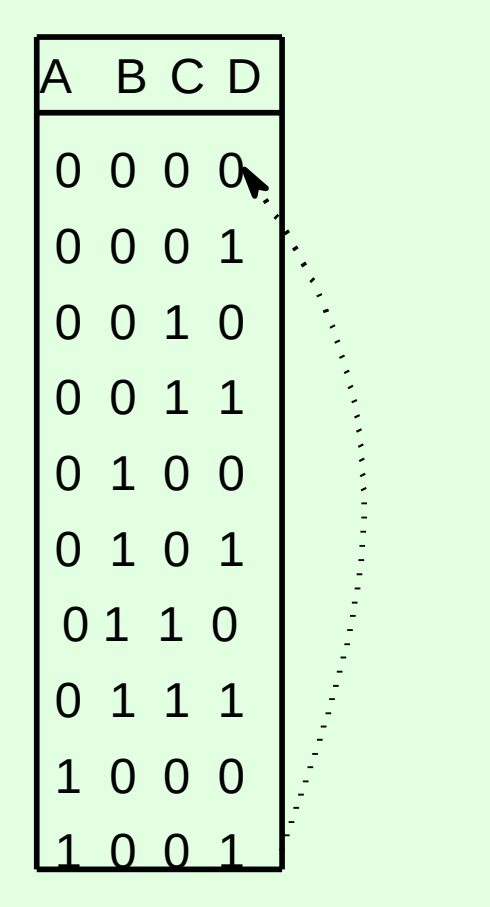
-D toggles every clock cycle
-C toggles only when D is 0
-B toggles only when both C and D are 0
-A toggles only when D C B are 0



Counters

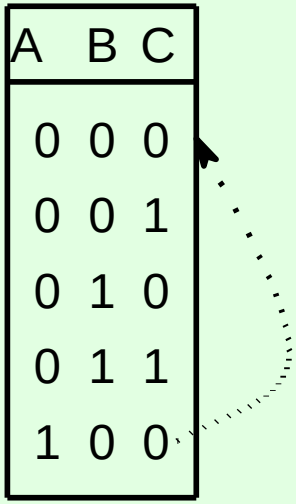


Binary down counter



Decade counter

Modulo-10 Counter



Modulo-5 Counter

Counter with Unused States

PS			NS			J_A	K_A	J_B	K_B	J_C	K_C
A	B	C	A	B	C						
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

There are two unused states 011 and 111. one approach to handle this situation is that, while evaluating expressions for J K , we use don't care conditions corresponding to these unused states

Counter with Unused States

PS			NS			J_A	K_A	J_B	K_B	J_C	K_C
A	B	C	A	B	C						
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

A \ BC	00	01	11	10
0	0	0	X	1
1	X	X	X	X

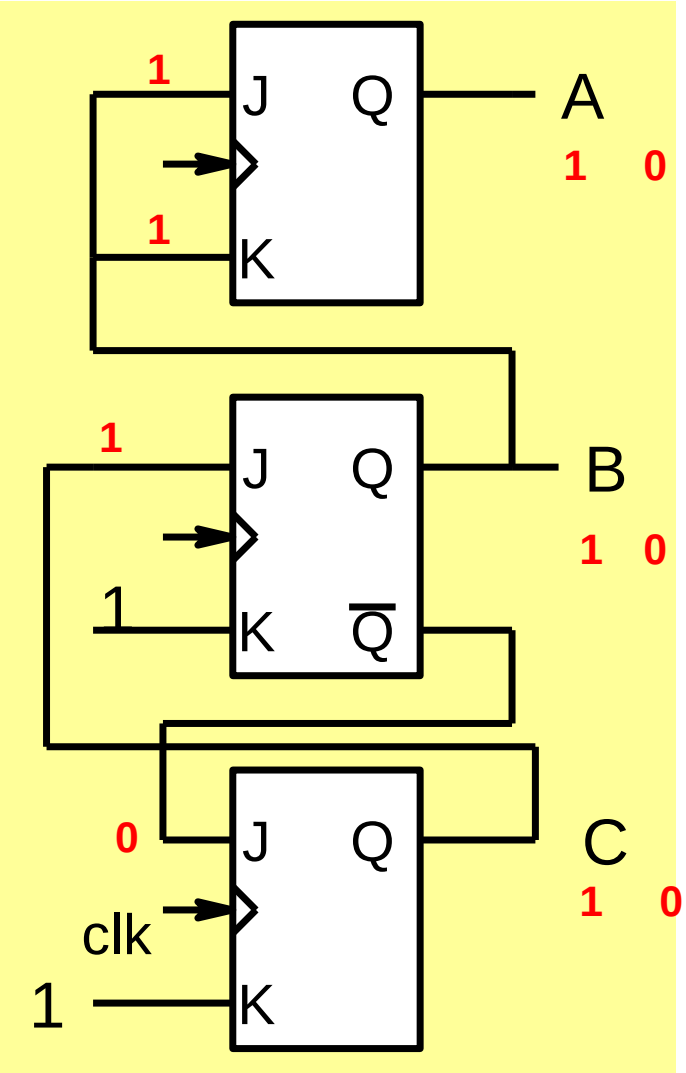
$J_A = B$

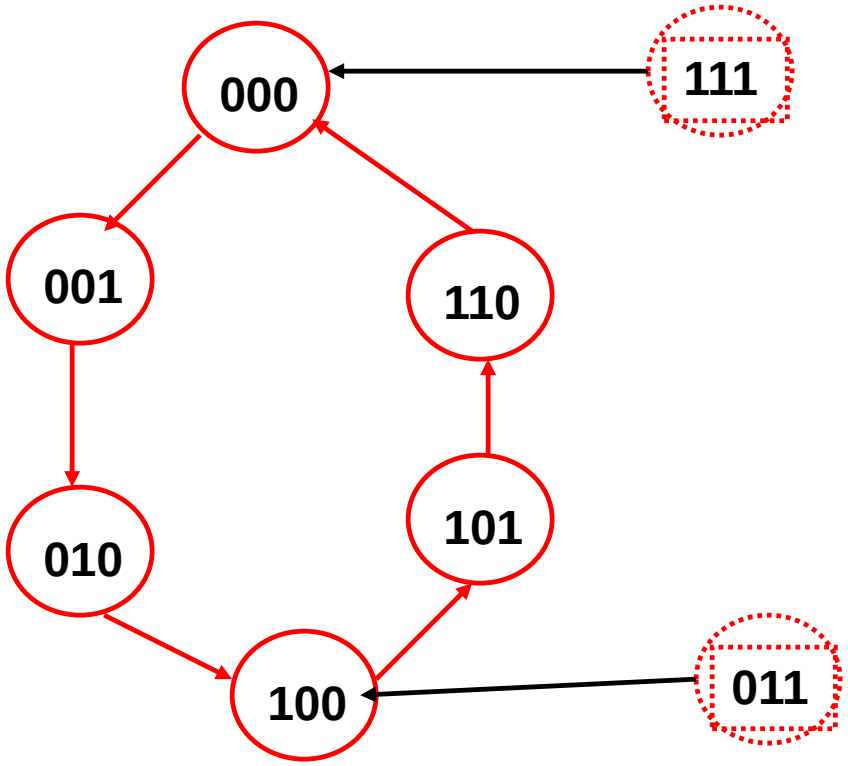
Counter with Unused States

PS			NS			J_A	K_A	J_B	K_B	J_C	K_C
A	B	C	A	B	C						
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	1	0	0	1	X	X	1	0	X
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X

$$J_A = B \qquad K_A = B$$
$$J_B = C \qquad K_B = 1$$
$$J_C = \overline{B} \qquad K_C = 1$$

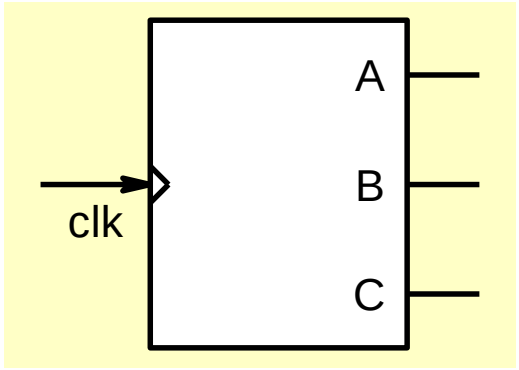
After synthesizing the circuit, one needs to check that if by chance the counter goes into one of the unused states, after one or more clock cycles, it enters a used state and then remains among the used states



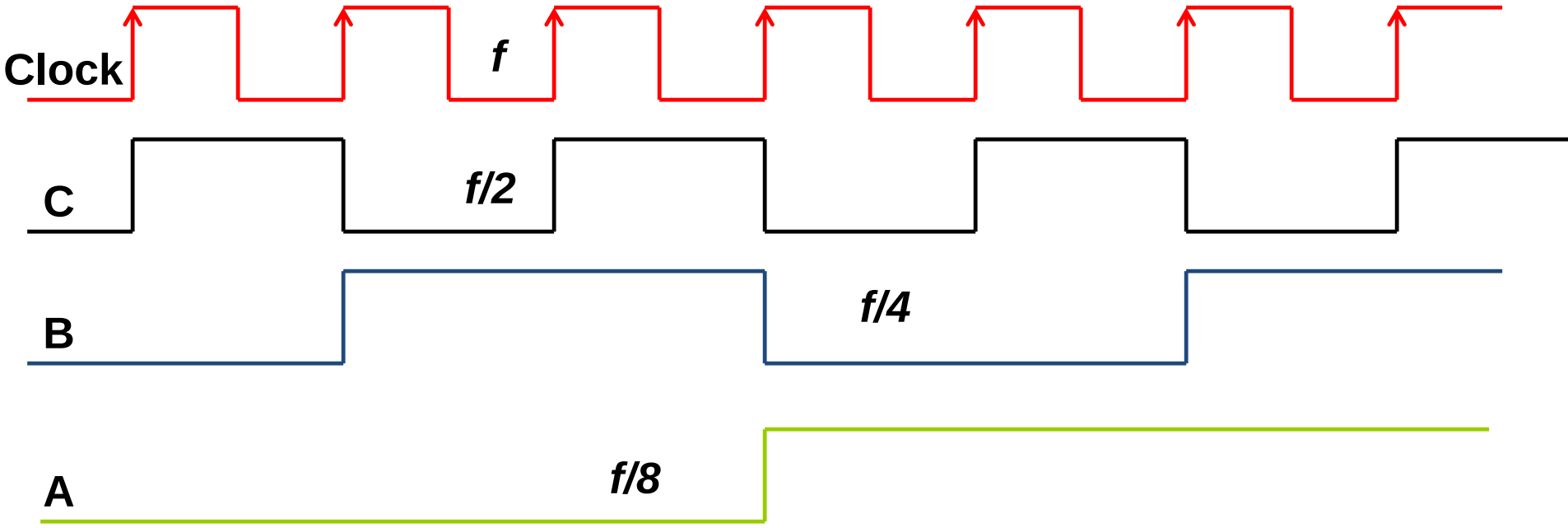


We can see that if by chance the counter goes into unused states 111 or 011, then after a clock cycle it enters one of the used states.

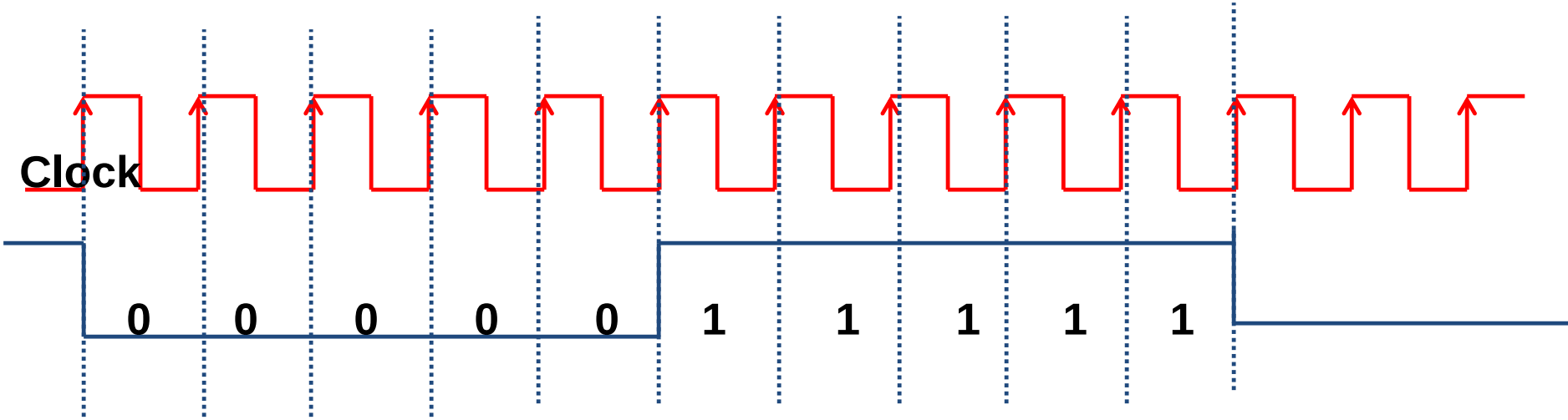
Counter as frequency divider



A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
1	0	1
1	1	0
1	1	1

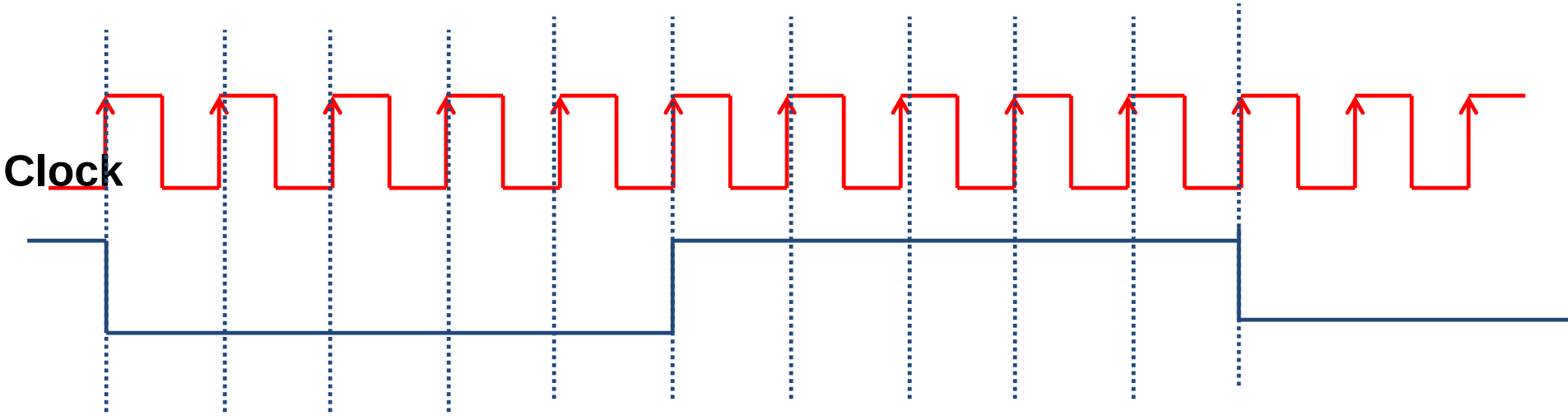


Example From a frequency of 10KHz, generate the following signal of frequency 1KHz



A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

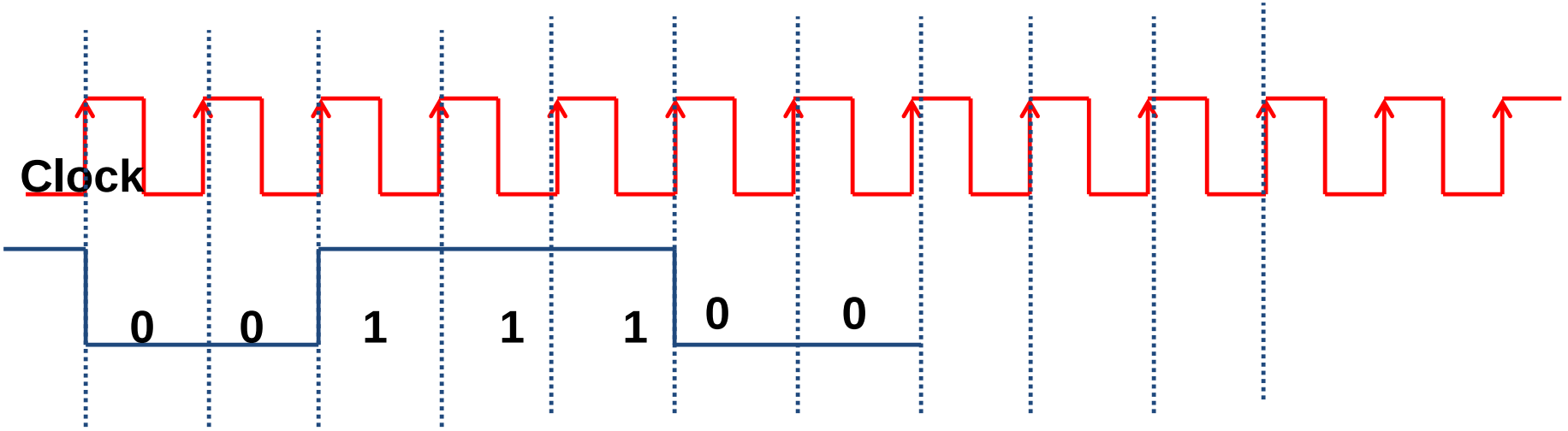
This will have a frequency of 1KHz but it will not have the same waveform



Design a divide by 10 counter with the following states

A	B	C	D
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
1	0	0	0
1	0	0	1
1	0	1	0
1	0	1	1
1	1	0	0

Example From a frequency of 10KHz, generate the following signal of frequency 2KHz



A divide by 5 counter is required that has 5 states.

A	B	C
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0

Modify

A	B	C
0	0	0
0	0	1
1	1	0
1	1	1
1	0	0

A will give the required waveform.