ESc201 : Introduction to Electronics

Digital Circuits

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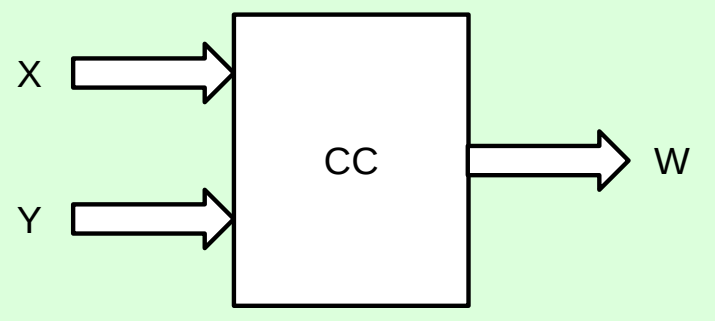
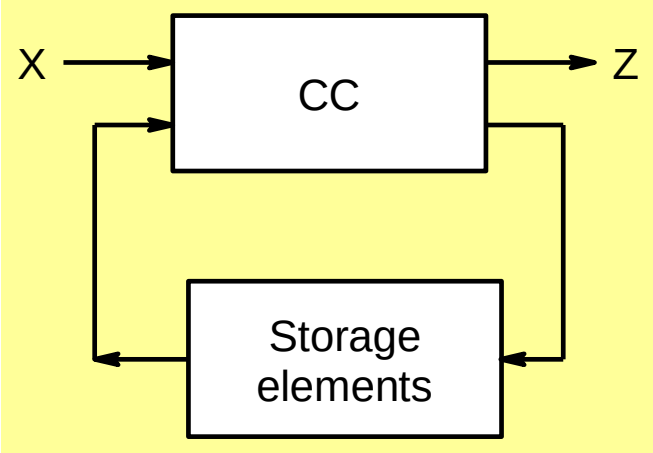
Digital Circuits

Combinational Circuits



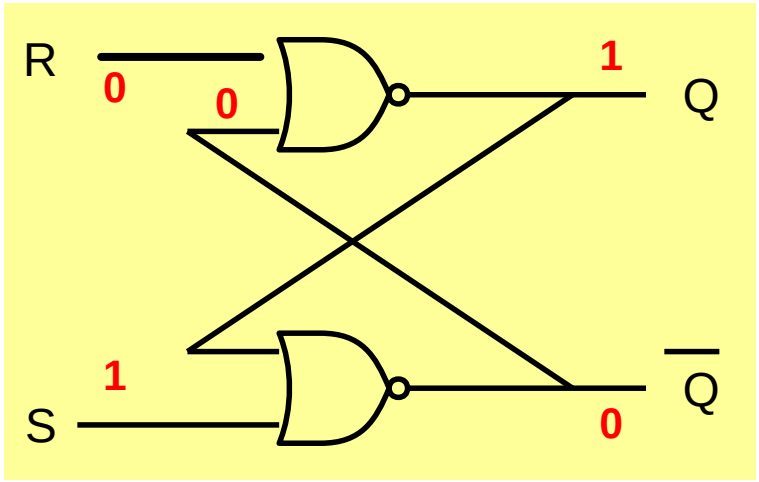
Output is determined by current values of inputs only.

Sequential Circuits



Output is determined in general by current values of inputs and past values of inputs/outputs as well.

NOR SR Latch (Set-Reset Latch) (recap)

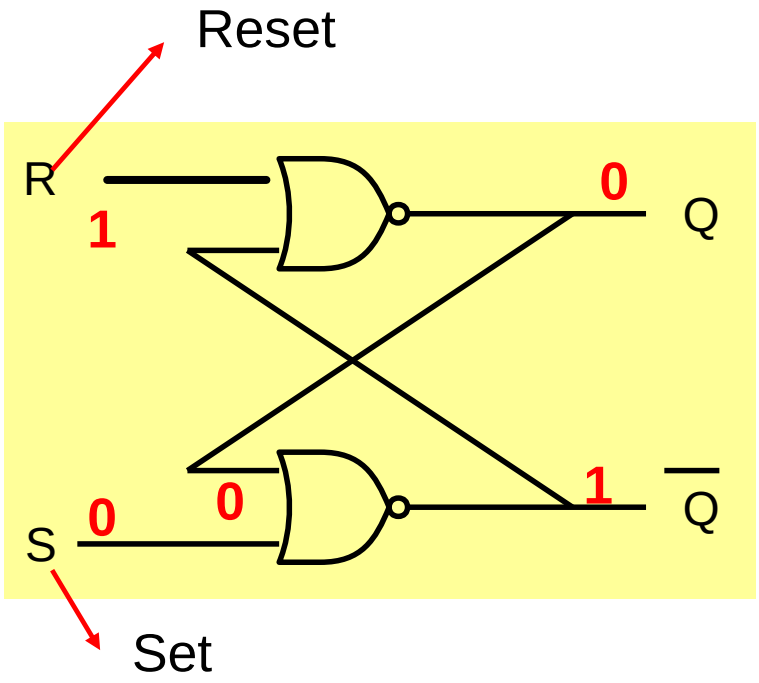


$Q = 1; \overline{Q} = 0$ Set State

$Q = 0; \overline{Q} = 1$ Re set State

S	R	Q	$\overline{Q}$	State
1	0	1	0	SET

NOR SR Latch (recap)

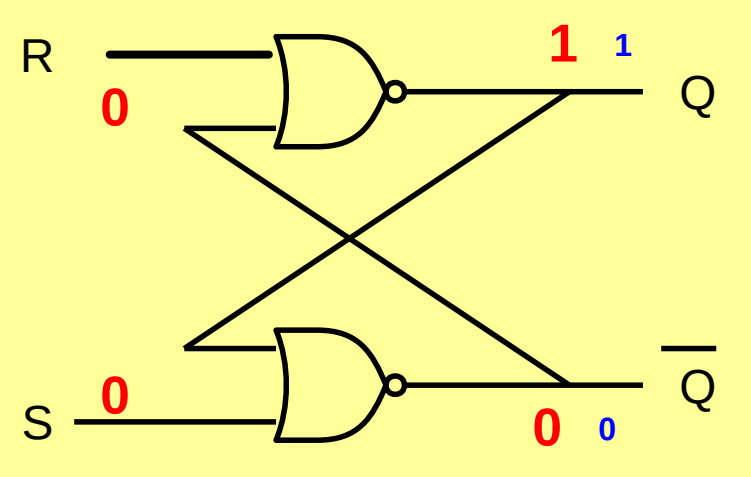


$Q = 1; \overline{Q} = 0$ Set State

$Q = 0; \overline{Q} = 1$ Re set State

S	R	Q	$\overline{Q}$	State
1	0	1	0	SET
0	1	0	1	RESET

HOLD State (recap)

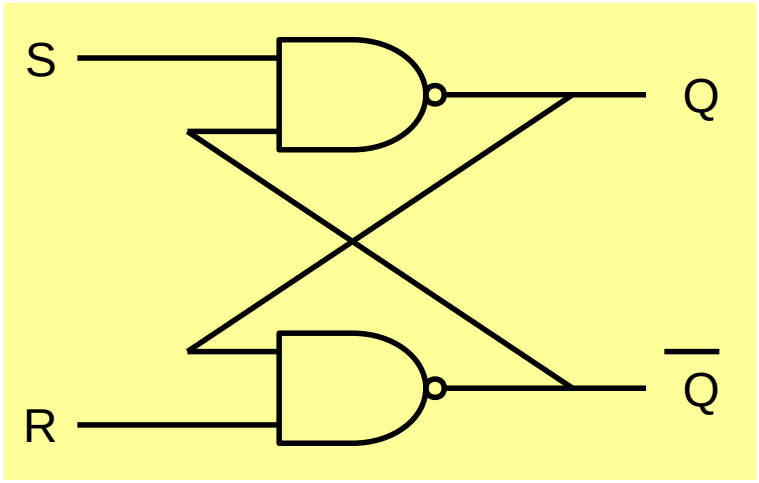


S	R	Q	$\overline{Q}$	State
1	0	1	0	SET
0	0	1	0	HOLD
0	1	0	1	RESET
0	0	0	1	HOLD

S	R	Q	$\overline{Q}$	State
1	0	1	0	SET
0	1	0	1	RESET
0	0	Q	$\overline{Q}$	HOLD
1	1	0	0	INVALID

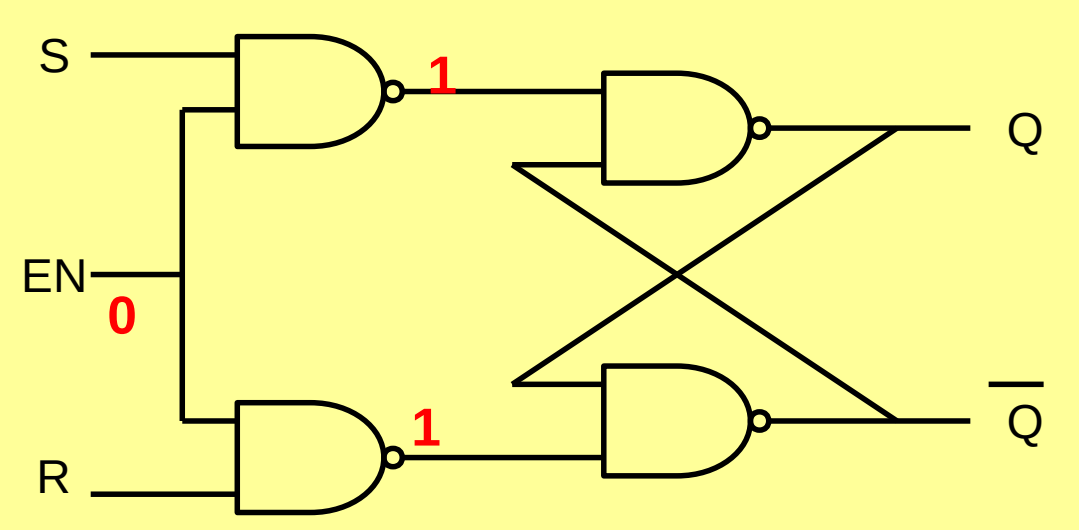
1 bit memory?

NAND Latch

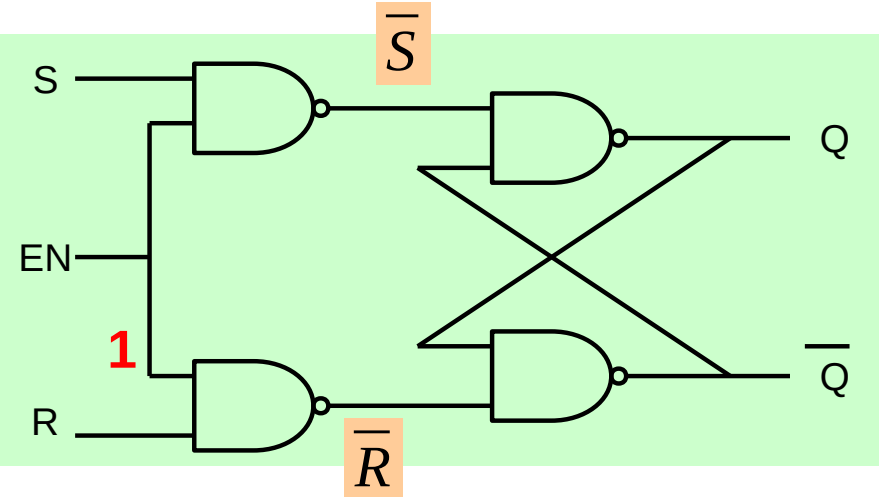


S	R	Q	$\overline{Q}$	State
0	1	1	0	SET
1	0	0	1	RESET
1	1	Q	$\overline{Q}$	HOLD
0	0	1	1	INVALID

RS NAND Latch with Enable

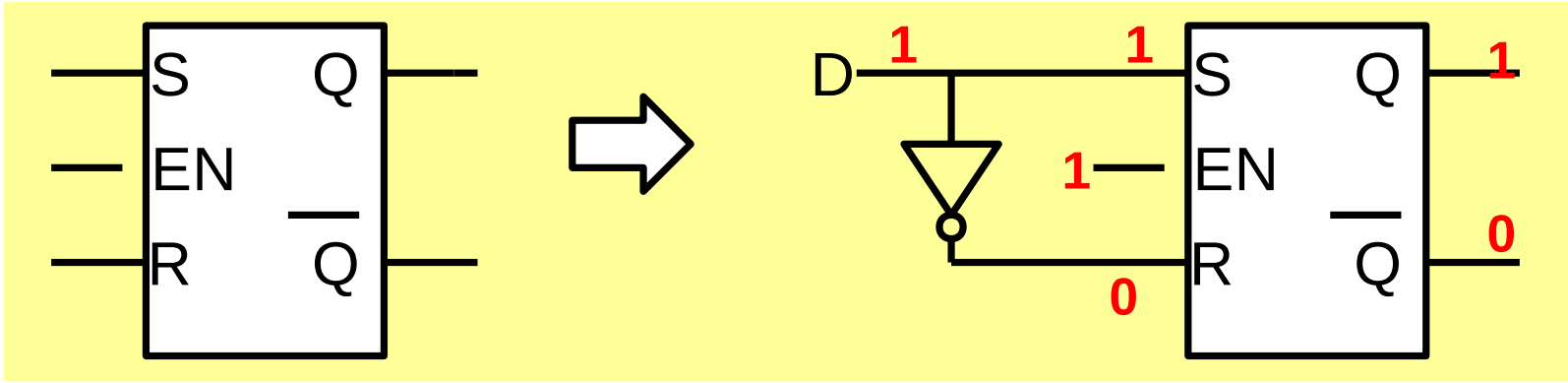


Hold State

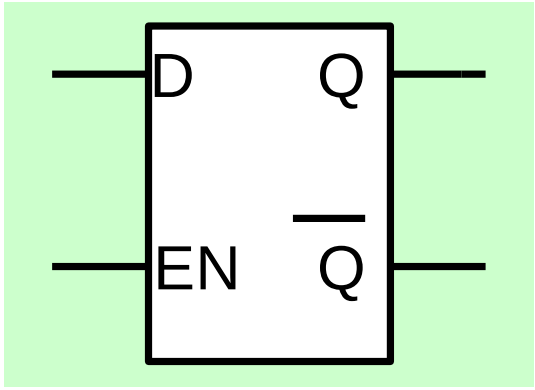


Enable	S R	Q $\overline{Q}$	State
0	x x	Q $\overline{Q}$	Hold
1	1 0	1 0	Set
1	0 1	0 1	Reset
1	0 0	Q $\overline{Q}$	Hold
1	1 1	0 0	Invalid

D latch

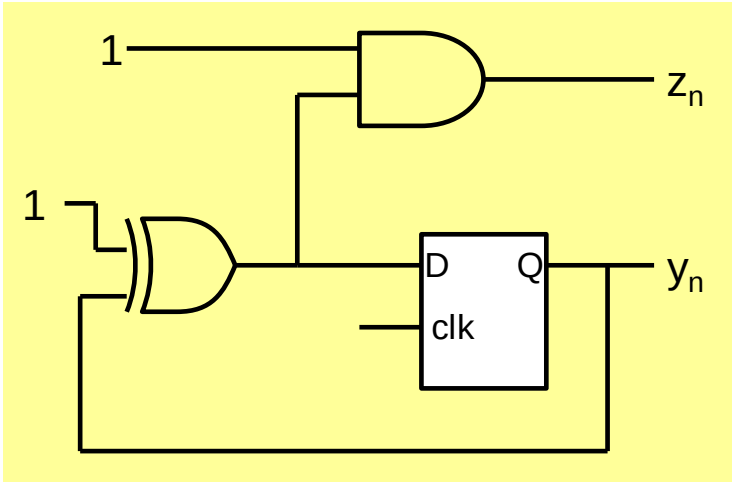


Enable	S	R	Q	$\overline{Q}$	State
0	x	x	Q	$\overline{Q}$	Hold
1	1	0	1	0	Set
1	0	1	0	1	Reset
1	0	0	Q	$\overline{Q}$	Hold
1	1	1	0	0	Invalid

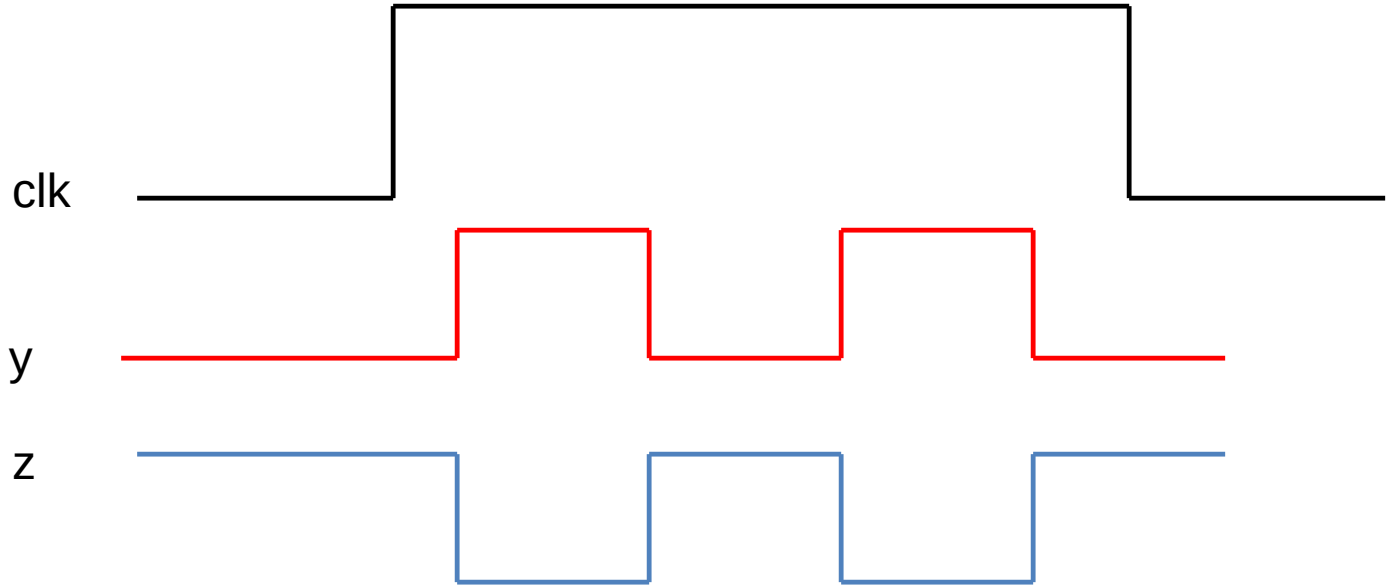


If EN = 1 then Q = D otherwise the latch is in Hold state

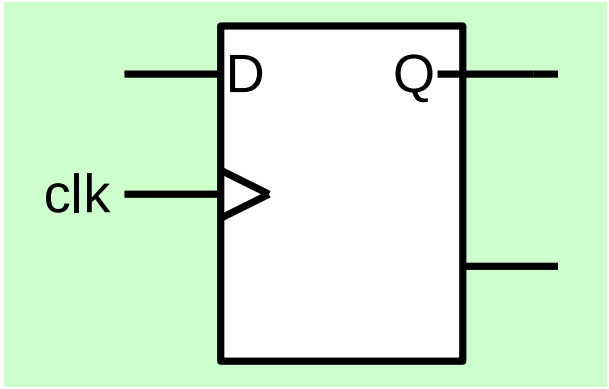
Latch with clock

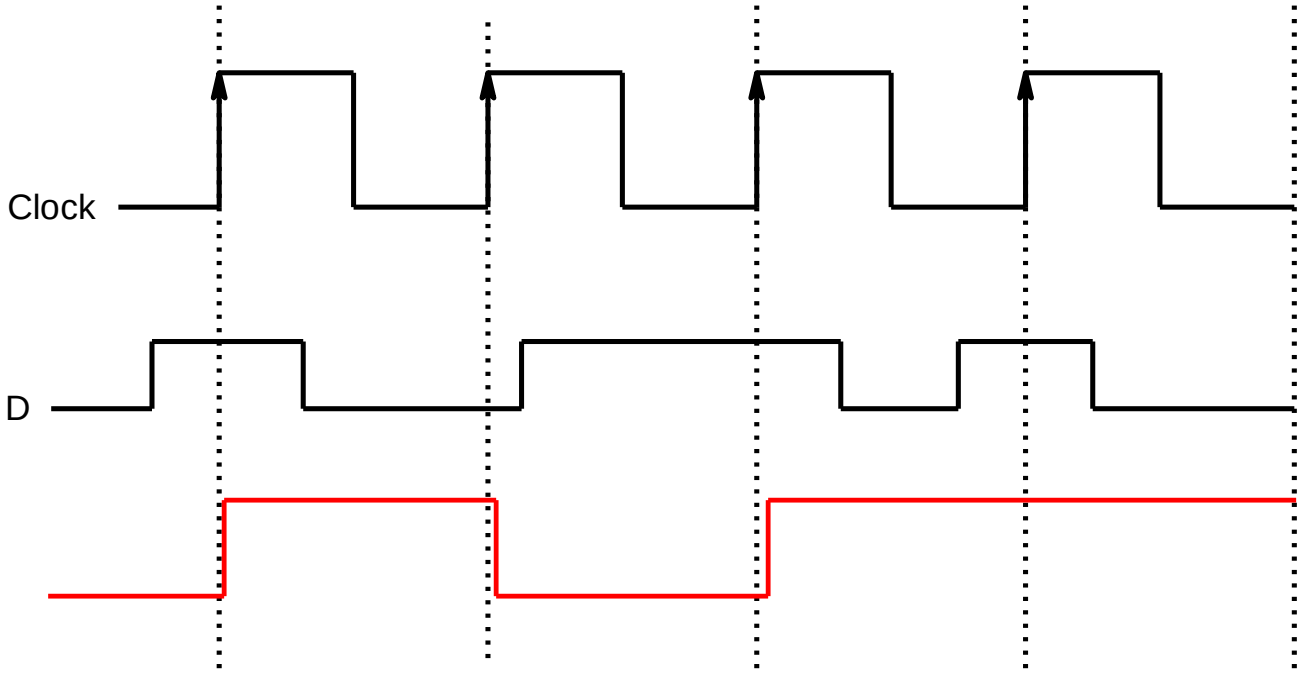


Circuits are designed with the idea there would be single change in output or memory state in single clock cycle.



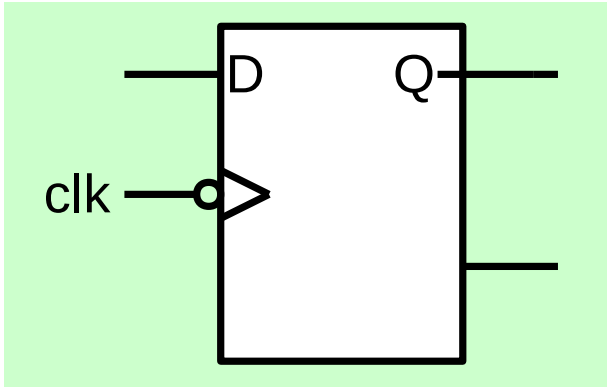
Edge Triggered Latch or Flip-flop

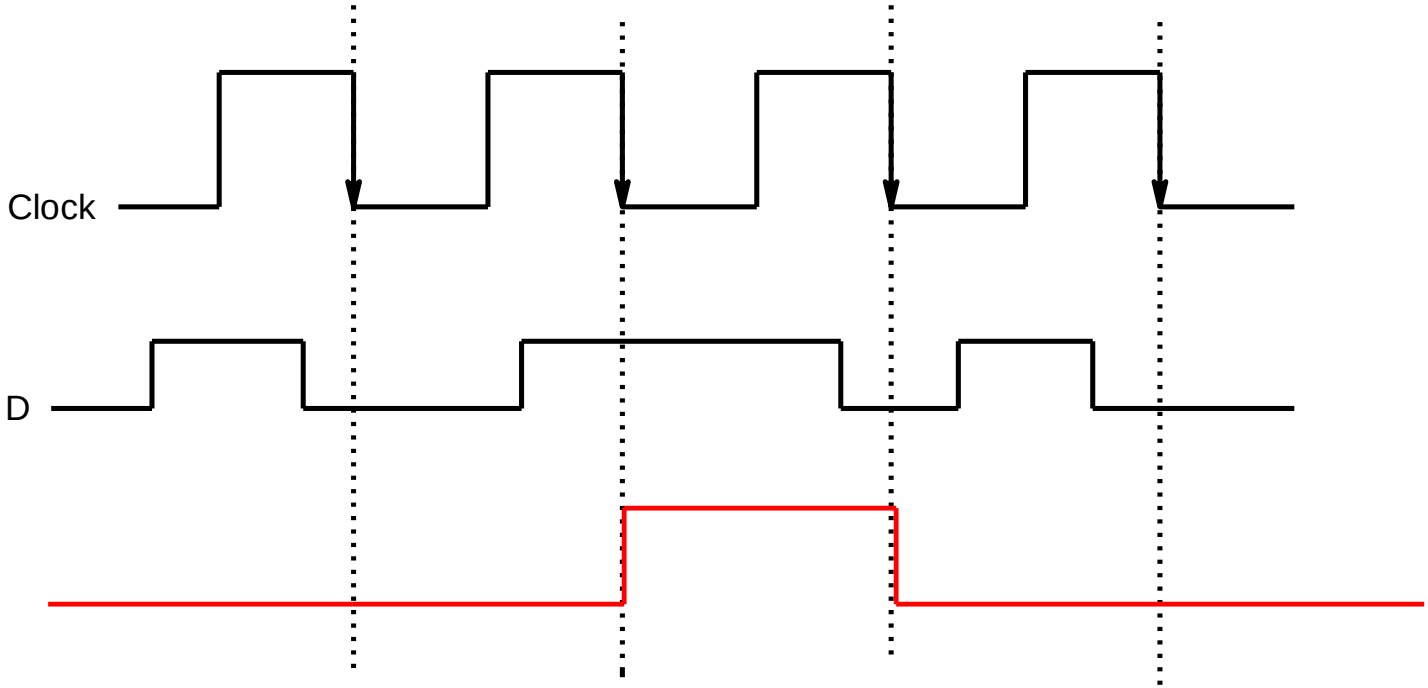




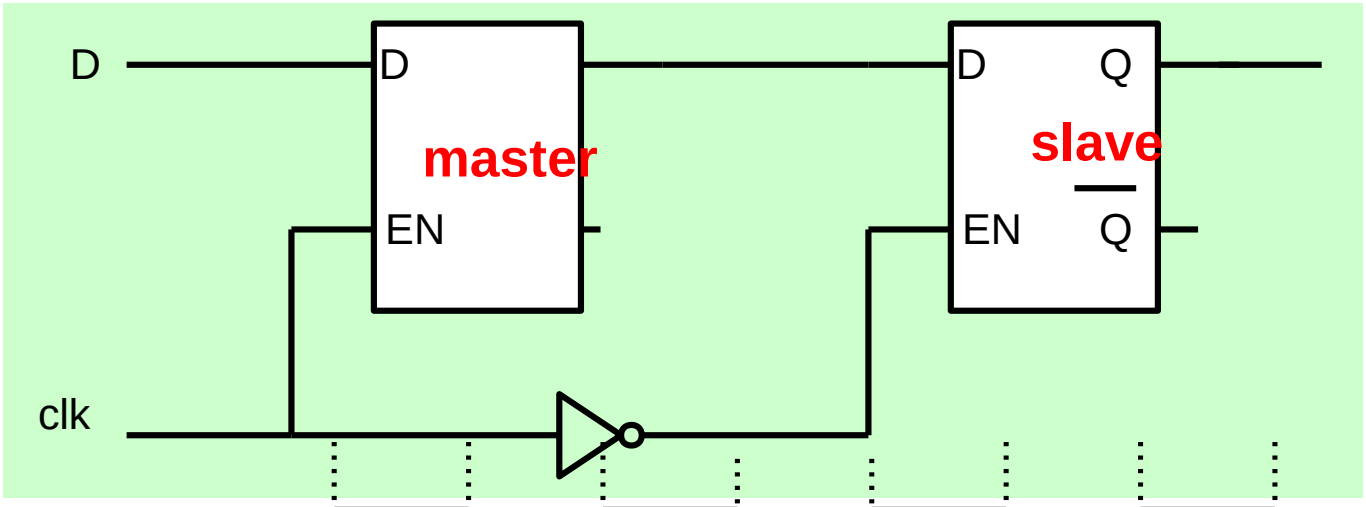
Positive edge triggered flipflop

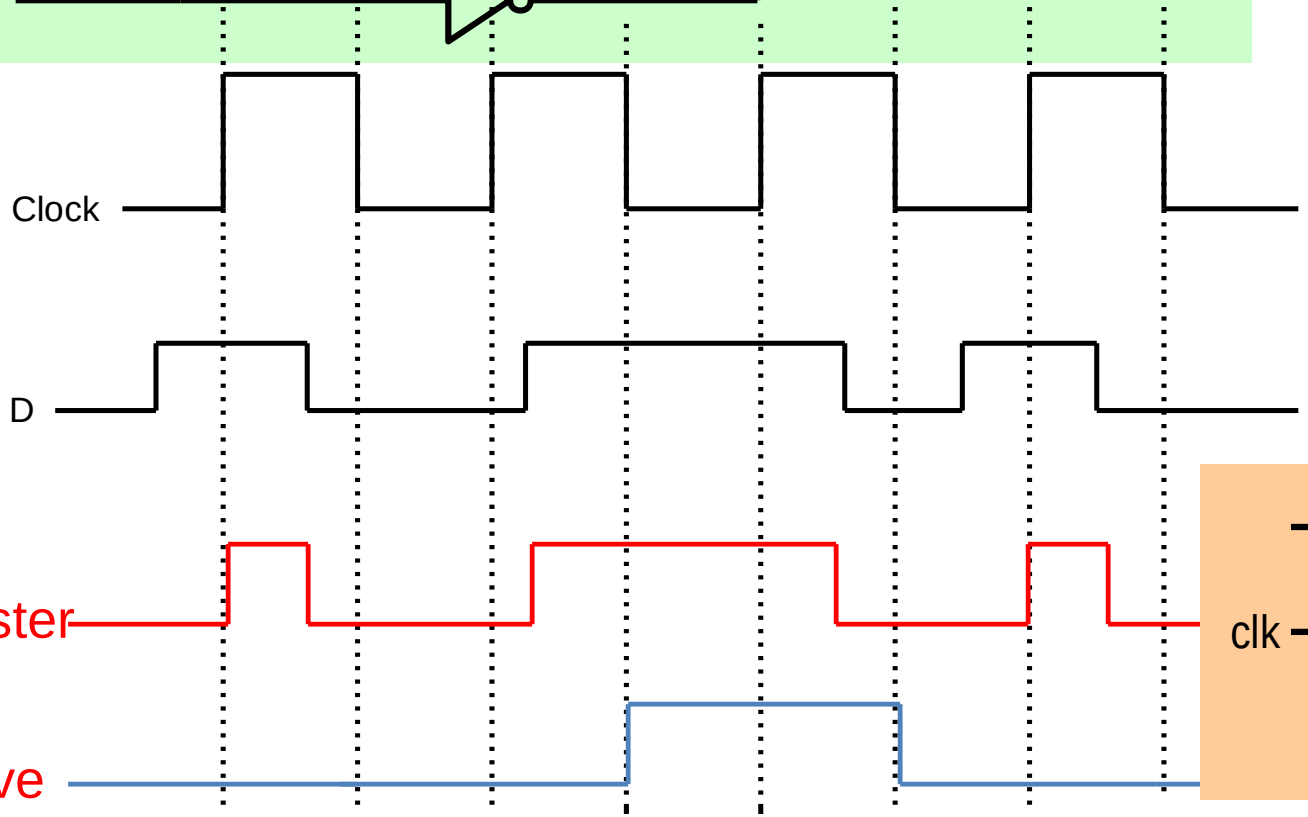
Negative Edge Triggered Latch or Flip-flop

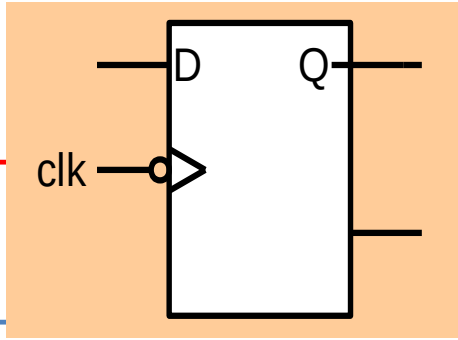




Master-Slave D Flip-flop

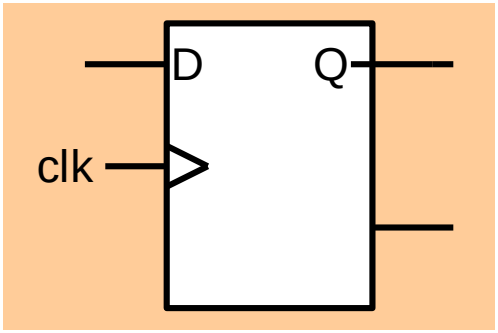






Characteristic table

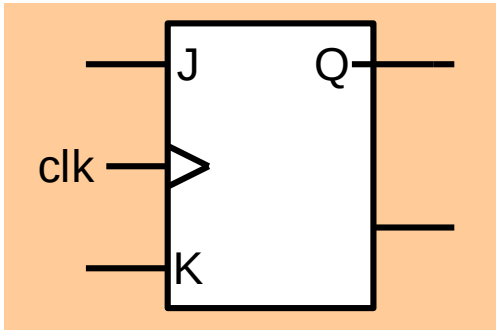
Given a input and the present state of the flip-flop, what is the next state of the flip-flop



Inputs (D)	Q(t+1)
0	0
1	1

Characteristic equation: $Q(t+1) = D$

JK Flip-flop



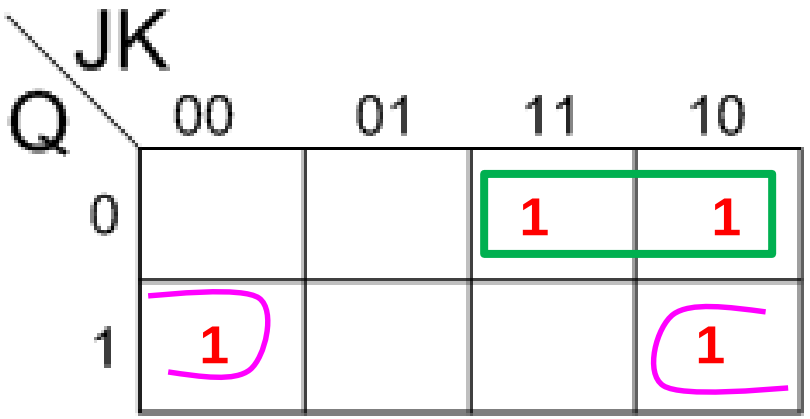
Inputs J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q(t)}$

Characteristic equation: $Q(t+1) = J\overline{Q}(t) + \overline{K}Q(t)$

JK flip flop is refinement of RS flip flop where indeterminate state of RS flip flop is defined in JK Flip Flop

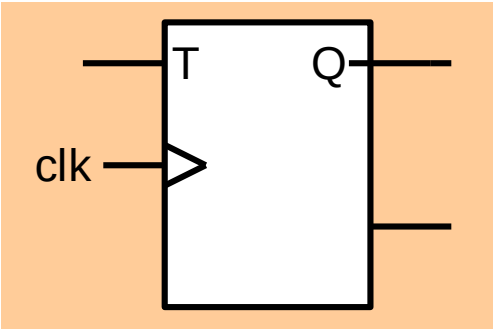
JK Flip-flop (characteristic equation)

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0



$$Q(t+1) = J\overline{Q}(t) + \overline{K}Q(t)$$

Toggle or T Flip-flop

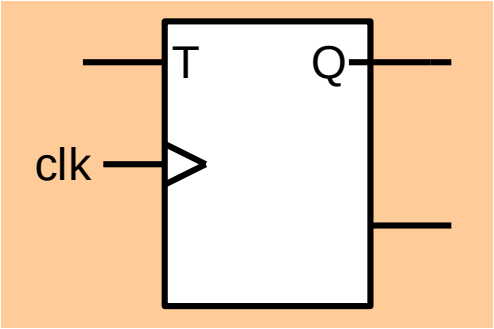


Inputs (T)	Q(t+1)
0	Q(t)
1	$\overline{Q(t)}$

Characteristic equation: $Q(t+1) = T \oplus Q(t)$

T	Q(t)	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Toggle or T Flip-flop



Inputs (T)	Q(t+1)
0	Q(t)
1	$\overline{Q(t)}$

Characteristic equation: $Q(t+1) = T \oplus Q(t)$

Excitation Table

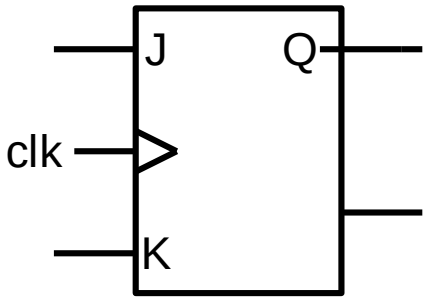
What inputs are required to effect a particular state change

Q	T	Q(t+1)
0	0	0
0	1	1
1	0	1
1	1	0

Excitation Table

Q(t)	Q(t+1)	Inputs T
0	0	0
0	1	1
1	0	1
1	1	0

JK Flip-flop excitation table



J	K	Q(t+1)
0	0	Q(t)
0	1	0
1	0	1
1	1	$\overline{Q(t)}$

Characteristic Table

Q	J	K	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	0

Q(t)	Q(t+1)	Inputs J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

Excitation Table