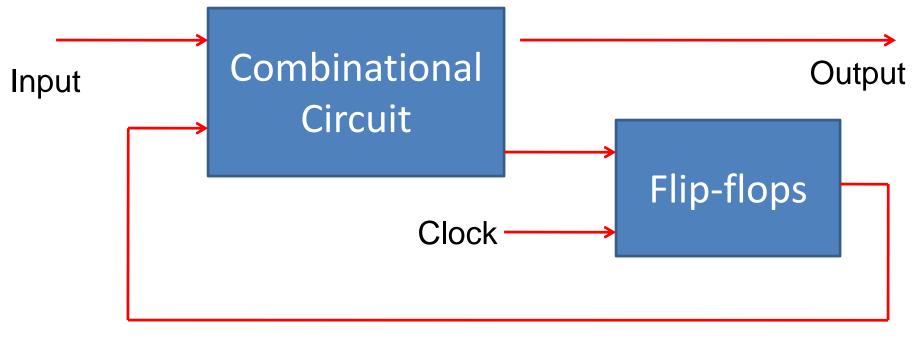
### **ESc201: Introduction to Electronics**

**Sequential Circuits** 

Amit Verma
Dept. of Electrical Engineering
IIT Kanpur

## Synchronous Sequential Circuits

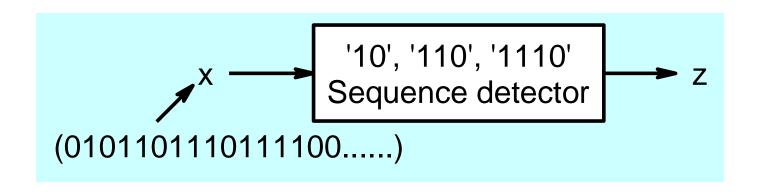


Employs signals that affect the storage elements only at discrete instants of time.

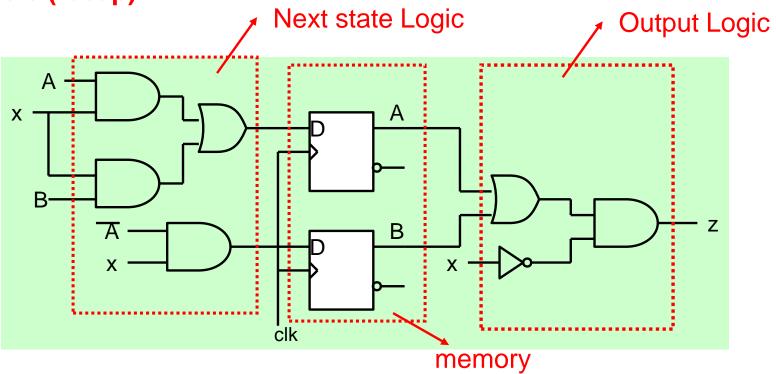
Synchronization is achieved via the *clock pulses*.

**Synchronous Clocked Sequential Circuits** 

# Synchronous Sequential Circuit Example



Analysis (recap)



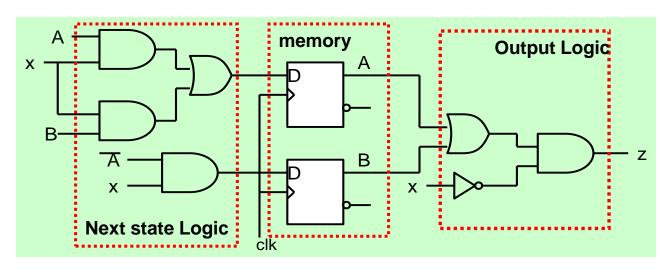
Output z depends on the input x and on the current state of the memory (A,B)

The memory has 2 FFs and each FF can be in state 0 or 1. Thus there are four possible states: AB: 00,01,10,11.

#### To describe the behavior of a sequential circuit, we need to show

- 1. How the system goes from one memory state to the next as the input changes
- 2. How the output responds to input in each state

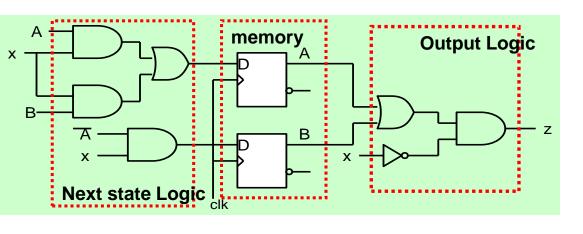
#### **Analysis of Sequential Circuits (recap)**



$$D_A = A.x + B.x$$
;  $D_B = A.x$ ;  $z = (A + B).x$ 

A(t+1) = A(t).x + B(t).x
$B(t+1) = \overline{A(t)}.x$
$z=(A+B).\overline{x}$

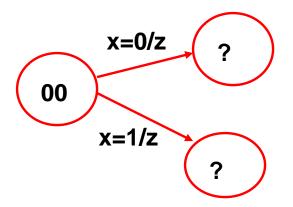
P	reser	nt State	Input	Next	State	Output
	Α	В	Х	Α	В	z
	0	0 0	0 1	0	0 1	0
ŀ	0	1	0	0	0	1 0
ŀ	1	0	0	0	0	1 0
	1 1	1 1	0 1	0	0	1 0



#### State Transition Table Present State Input **Next State** Output В Α Α В Χ Ζ 0 0 0 0 0 0 0 1 0 0 1 0 0 0 0

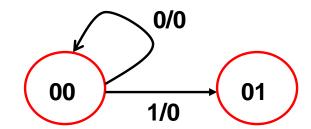
0

00 Memory state in which FF A& B have output values 00

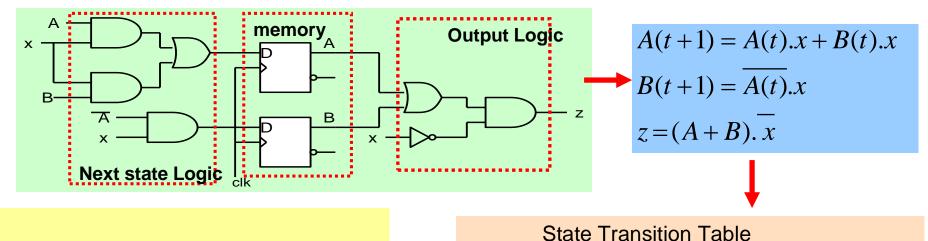


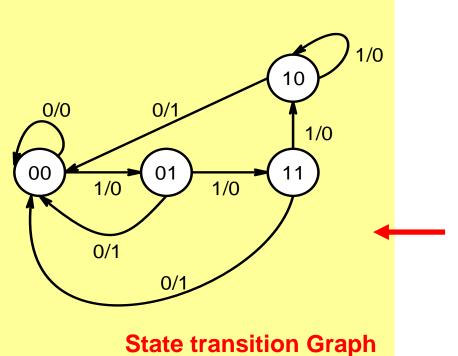
If x = 0 then z = 0, When the clock edge comes the system would stay in 00 state.

If x = 1 then z = 0. When the clock edge comes the system would go to 01 state.

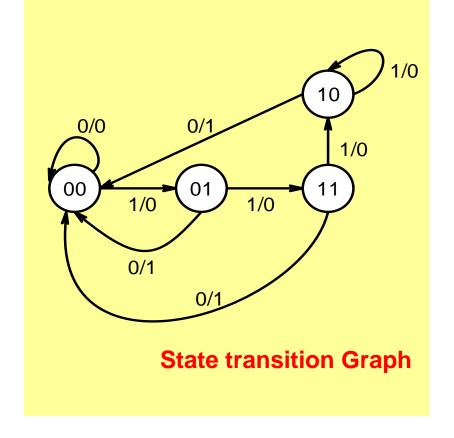


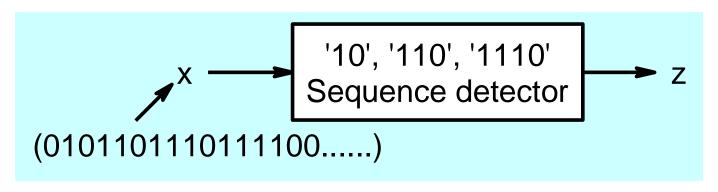
#### **Analysis of Sequential Circuits**

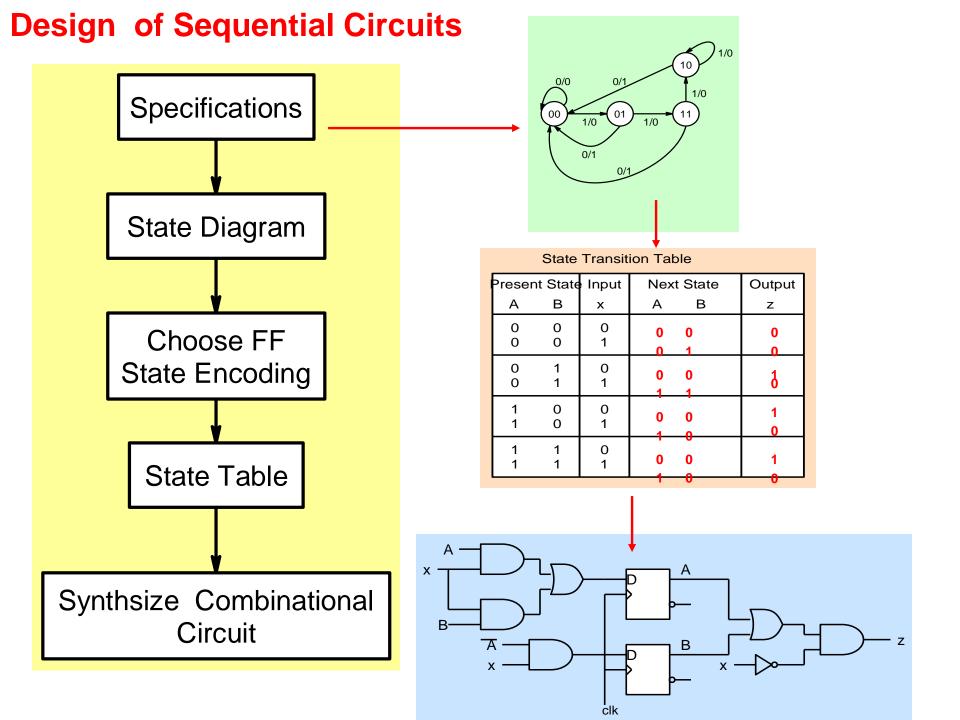




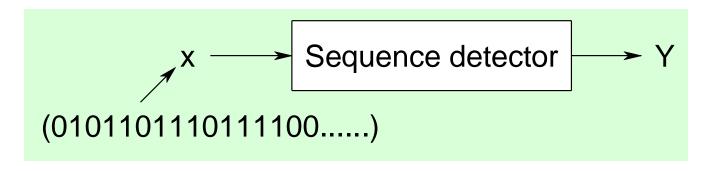
1	Present State In		Input	Nov	t State	Output
	Fresent State		input	ivex	Siale	Output
	Α	В	X	Α	В	Z
	0	0	0	0	0	0
	0	0	1	0	1	0
	0	1	0	0	0	1
	0	1	1	1	1	0
	1	0	0	0	0	1
	1	0	1	1	0	0
	1	1	0	0	0	1
	1 .	4		_	_	



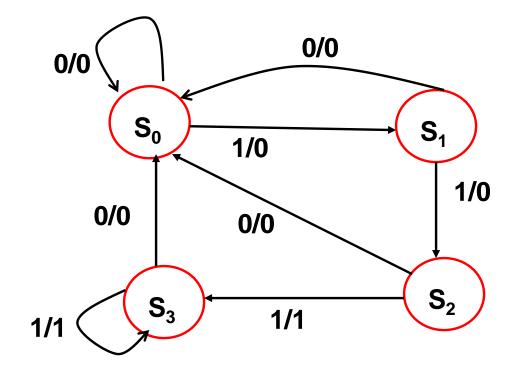




#### **System specification to State diagram**

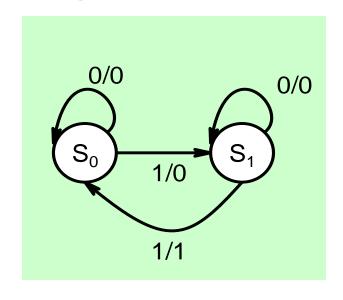


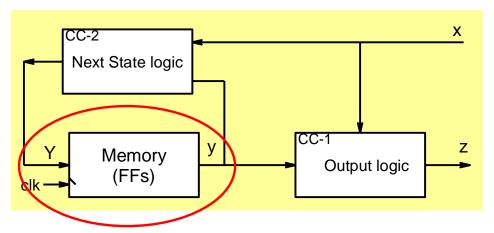
Detect 3 or more consecutive 1's in the input stream



#### Conversion of State transition graph to a circuit

#### **Example-1**



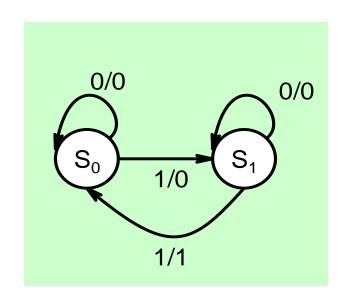


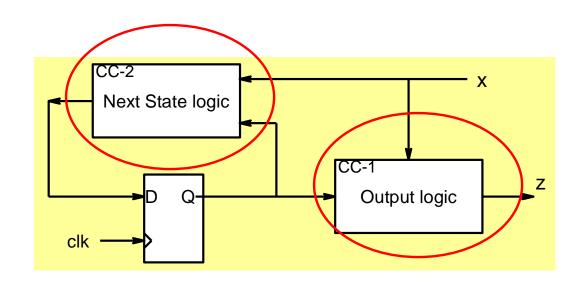
3 blocks need to be designed

- 1. How many FFs do we need?
- N FFS can represent 2<sup>N</sup> states so Minimum is 1

2. Which FF do we choose?

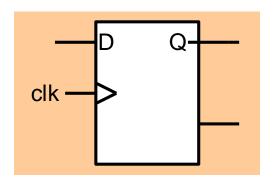
- Say D FF
- 3. How are the states encoded?
- Say FF output Q=0 represents S₀ and Q=1 represents S₁ state



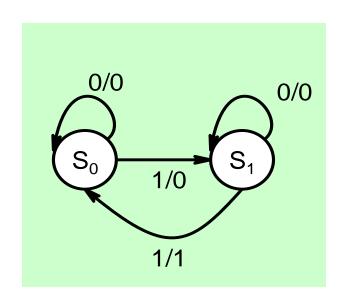


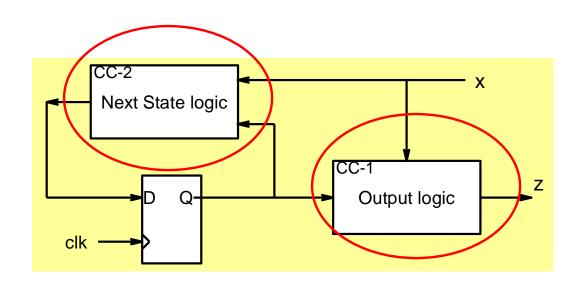
Present State In		Input	Next State	D	Output
	Q(t)	Х	Q(t+1)		Z
	0 0	0 1	0 1		0 0
	1 1	0 1	1 0		0

#### **Excitation Table**

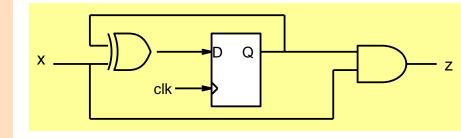


		Inputs
Q(t)	Q(t+1)	D
0	0	0
0	1	1
1	0	0
1	1	1



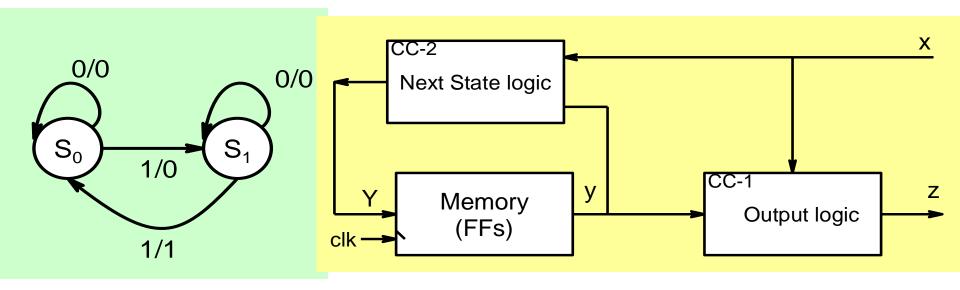


Present State	Input	Next State	D	Output
Q(t)	Х	Q(t+1)		z
0	0 1	0 1	0	0 0
1	0	1 0	1 0	0 1

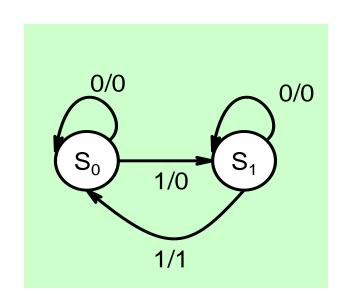


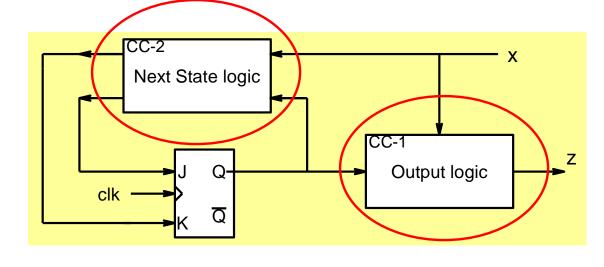
$$D = \overline{Q}.x + Q.\overline{x} \quad ; \quad z = Q.x$$

#### Example-2



- How many FFs do we need?
- 2. Which FF do we choose? Say JK FF
- 3. How are the states encoded? Say FF output Q=0 represents  $S_0$  and Q=1 represents  $S_1$  state

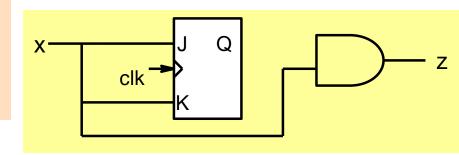




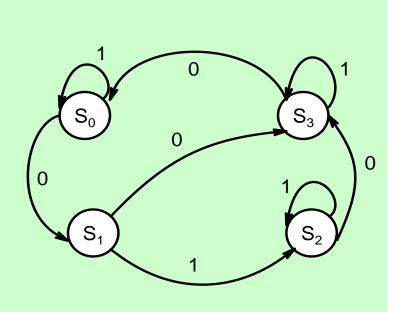
Present State	Input	Next State	J K	Output
Q(t)	Х	Q(t+1)		z
0	0 1	0 1	0 X 1 X	0 0
1 1	0	1 0	X 0 X 1	0 1

$$J = x$$
;  $K = x$ ;  $z = Q.x$ 

Q(t)	Q(t+1)	J K
0	0	0 X
0	1	1 X
1	0	X 1
1	1	X 0



#### Example-3



 State
 FF O/P A B

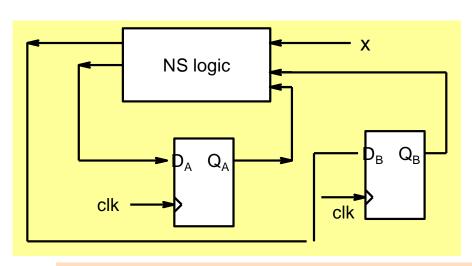
  $S_0$  0 0

  $S_1$  0 1

  $S_2$  1 0

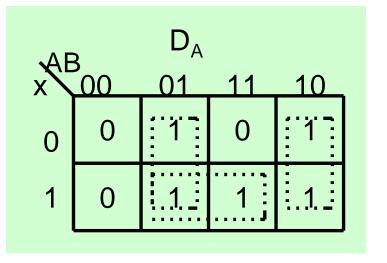
  $S_3$  1 1

For 4 states a minimum of two FFs will be required. Let us choose 2 D FFs A &B



Preser	nt State	Input	Next	State		
Α	В	Х	Α	В	$D_A$	$D_B$
0 0	0 0	0 1	0 0	1 0	0	1 0
0 0	1	0 1	1 1	1 0	1	1 0
1 1	0 0	0 1	1 1	1 0	1	1 0
1 1	1 1	0 1	0 1	0 1	0	0

Present State Input		Input	Next	State		
Α	В	Х	Α	В	$D_A$	$D_B$
0 0	0 0	0 1	0 0	1 0	0	1 0
0	1	0 1	1 1	1 0	1	1
1	0	0 1	1 1	1 0	1	1
1	1 1	0 1	0	0 1	0	0 1



$$D_A = \overline{A}B + xB + A\overline{B}$$
$$= A \oplus B + x.B$$

$$D_{B} = \overline{x}.\overline{A} + \overline{x}.\overline{B} + x.A.B$$

$$= \overline{x}.(\overline{A} + \overline{B}) + x.A.B$$

$$= \overline{x}.\overline{AB} + x.AB = \overline{x} \oplus \overline{AB}$$

$$D_A = A \oplus B + x.B$$

$$D_B = \overline{x \oplus AB}$$

