# ESc201 : Introduction to Electronics

## Amplifiers

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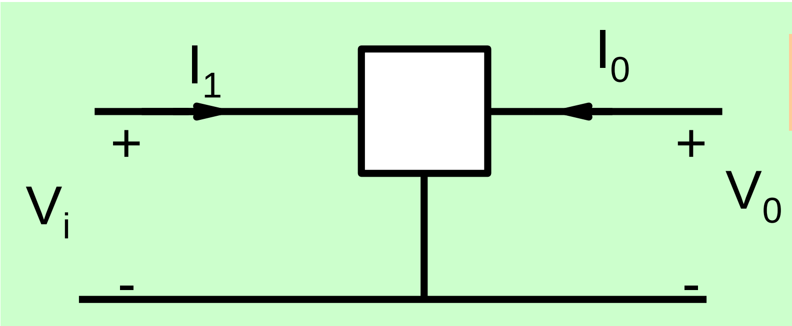
# RECAP

Input resistance $R_i = V_i / I_i$

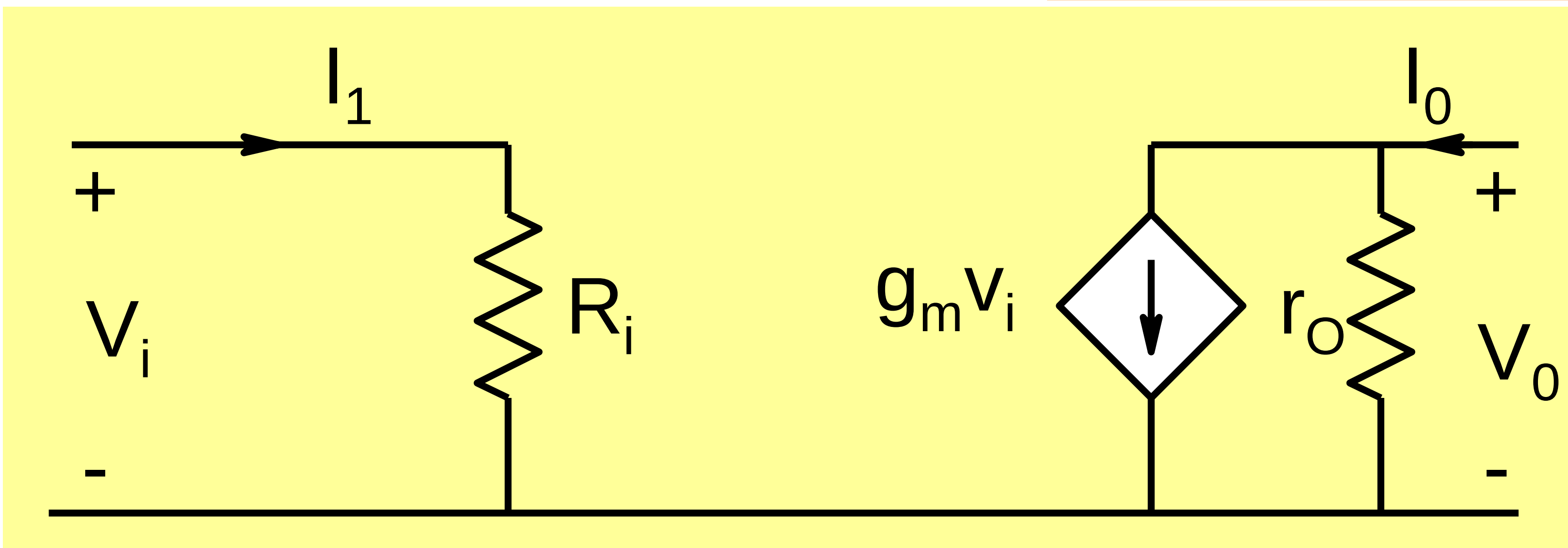
(Ideally large)




Trans conductance

$$g_m = \left.\frac{I_o}{V_i}\right|_{V_0=0}$$

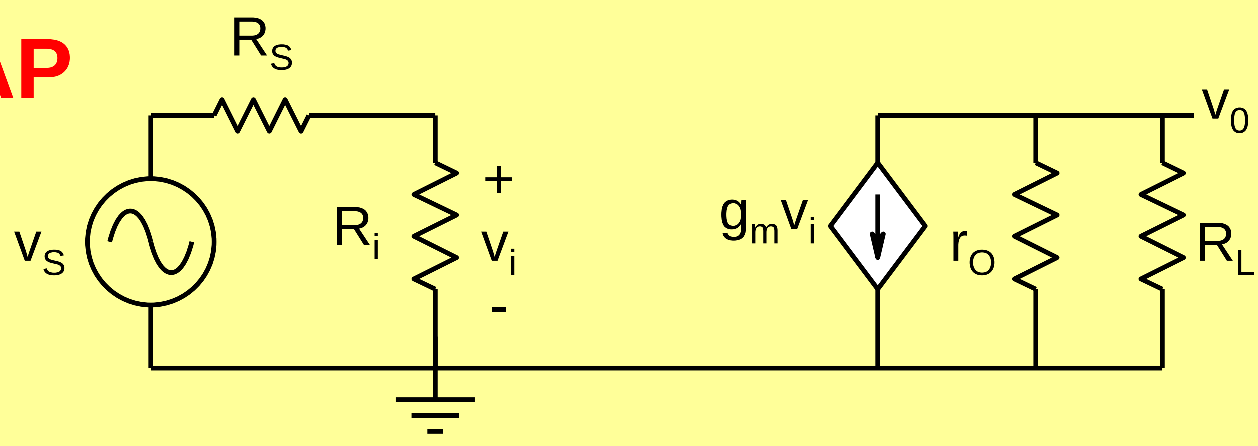
(Ideally large)




Output conductance: $g_o = 1/r_o = \left.\frac{I_o}{V_o}\right|_{V_i=0}$

(Ideally small)

# RECAP




$$A_V = \frac{V_o}{V_s} = -g_m r_o \times \frac{R_L}{r_o + R_L} \times \frac{R_i}{R_i + R_S}$$

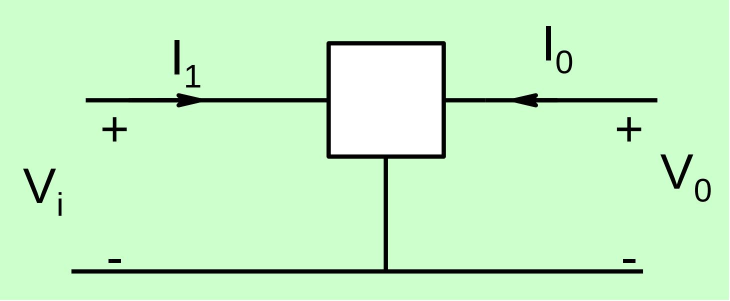
In the ideal case $r_o$ is infinite

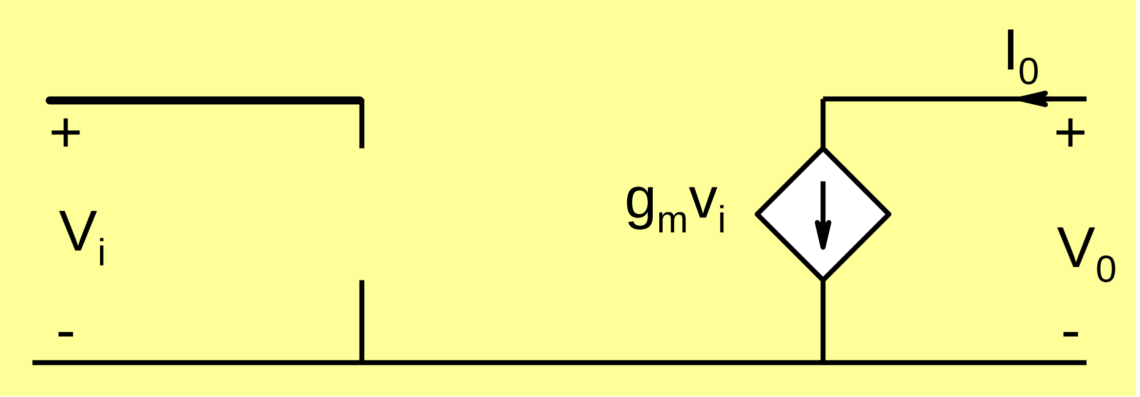
$$A_V = \frac{V_o}{V_s} = -g_m R_L \times \frac{R_i}{R_i + R_S}$$

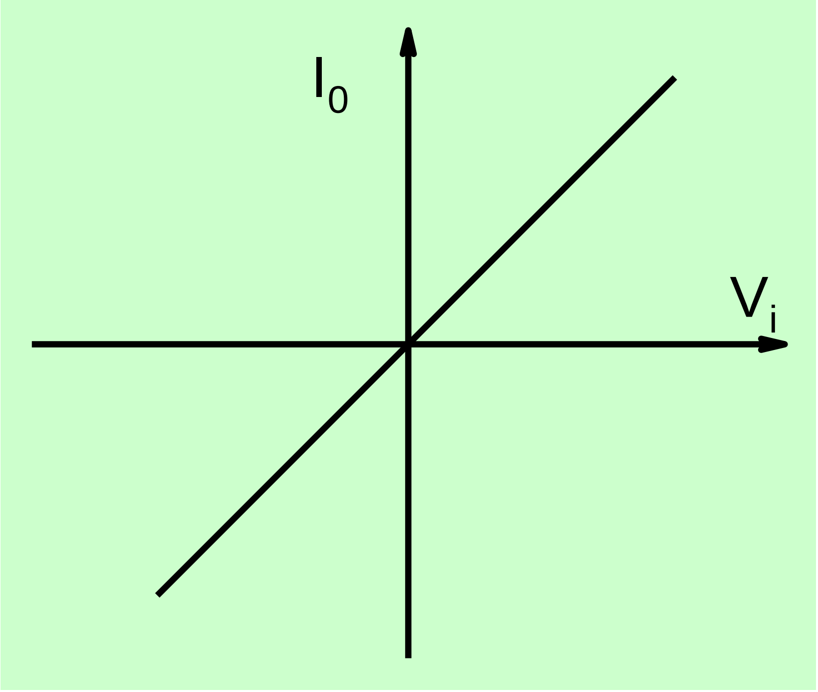
We would ideally like input resistance $R_i$ to be infinite as well !

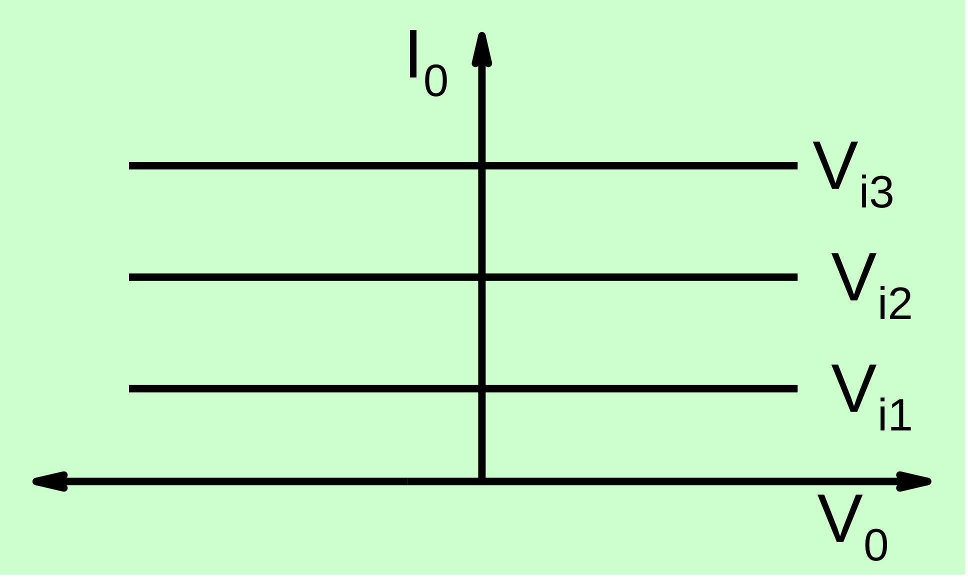
$$A_V = -g_m R_L$$

# RECAP



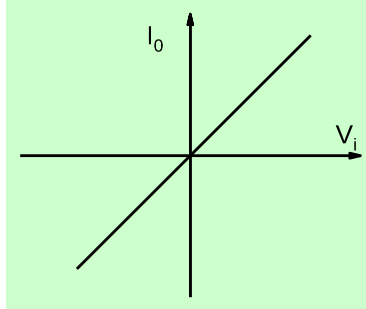



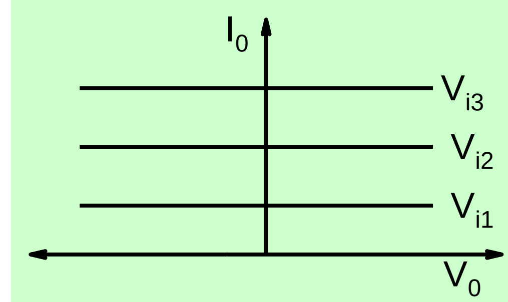




**Ideal Transistor Characteristics**

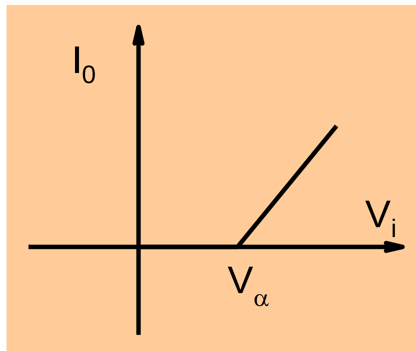
**RECAP**

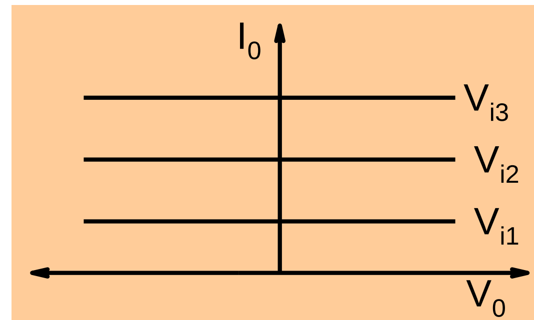
**Ideal transistor**



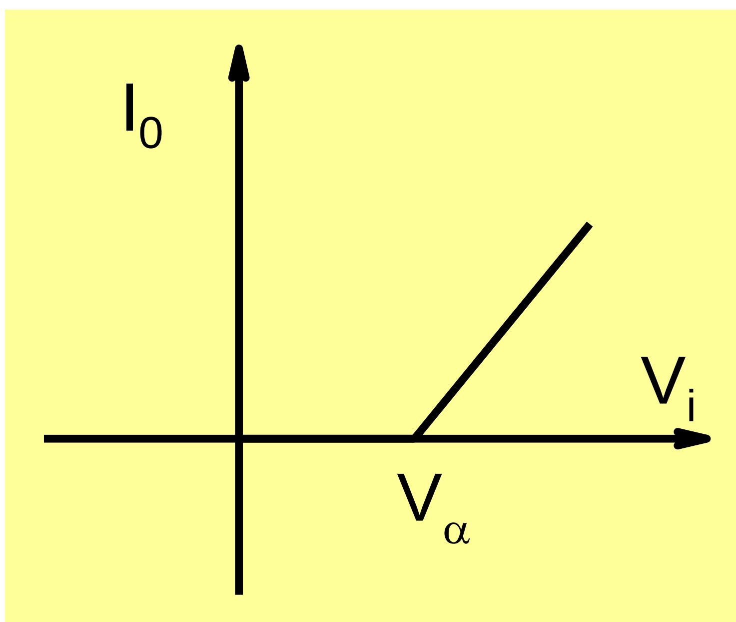



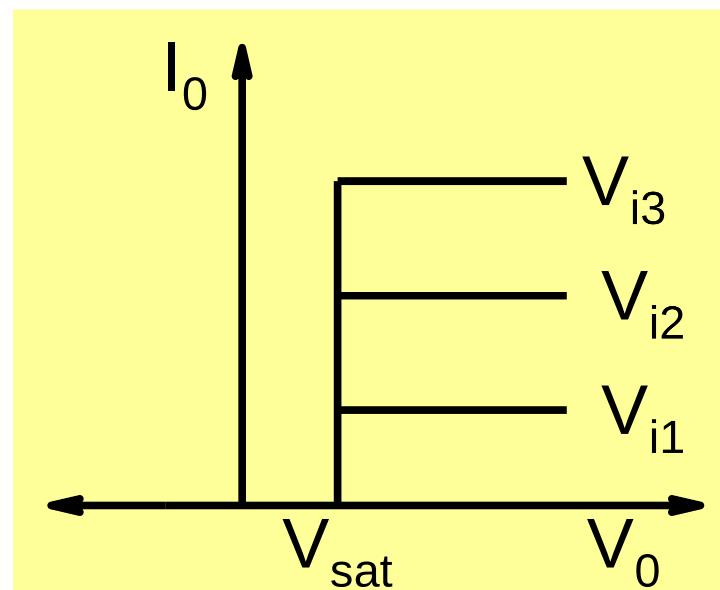

**Device X**



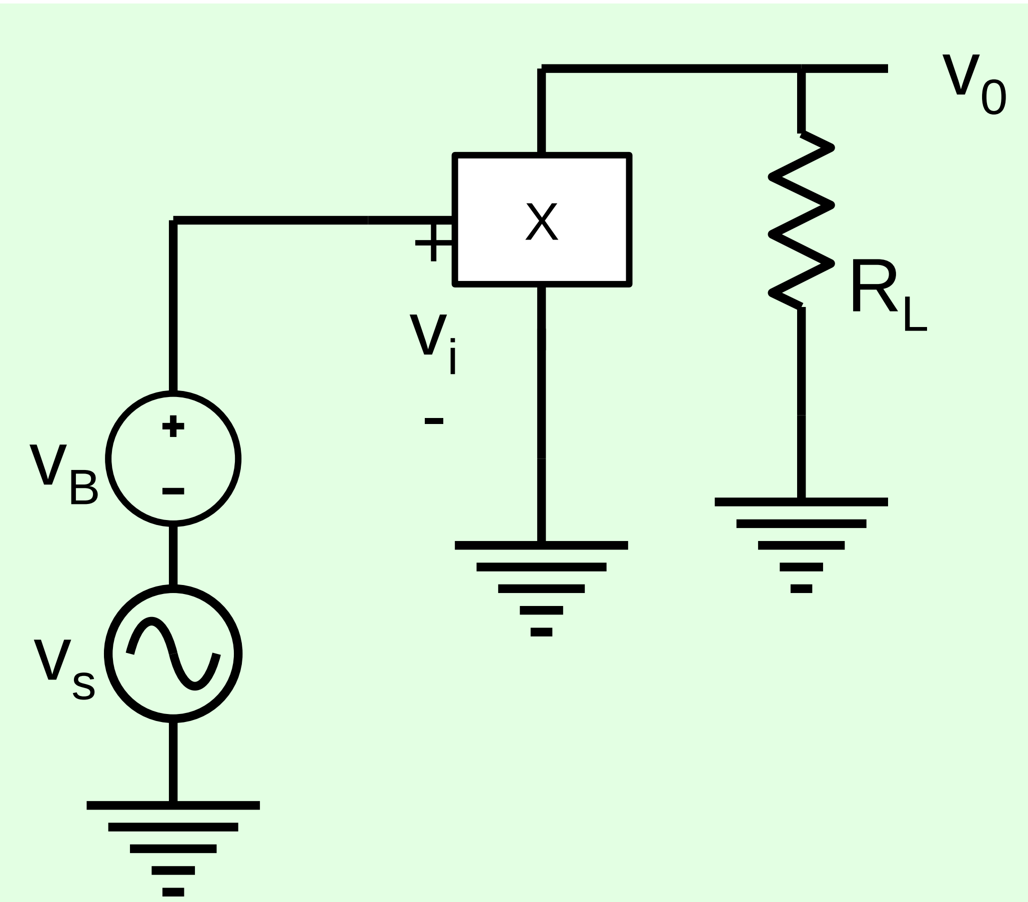

**Device Y**

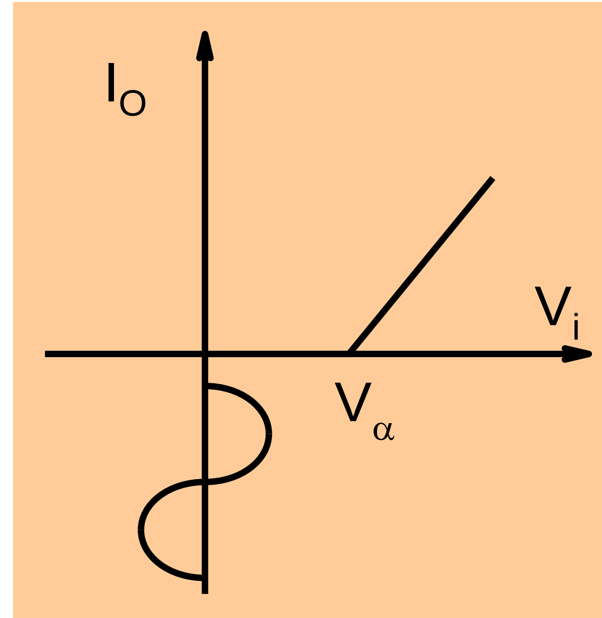


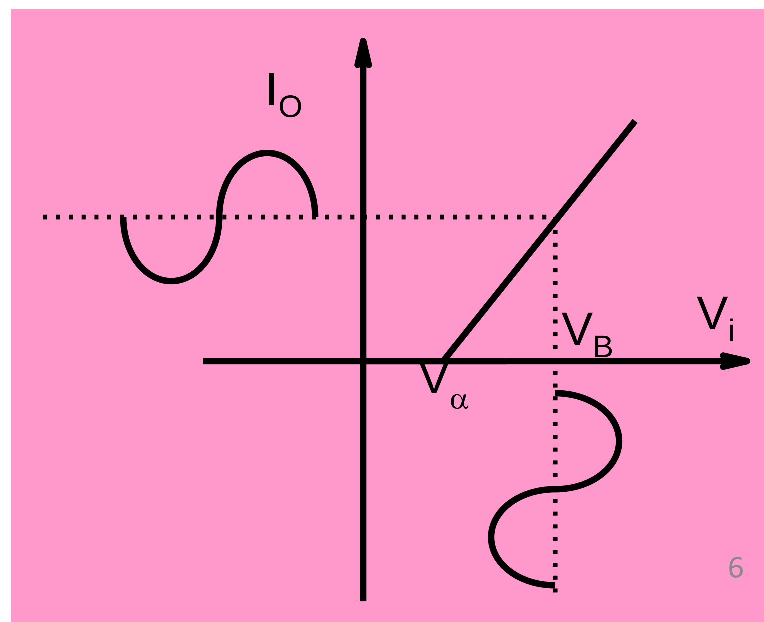

How do we use elements such as X, Y etc to make amplifiers?

When only a part of device characteristics is suitable for amplification, then we need to push the device into that region by applying suitable bias voltages. This process is called **BIASING**



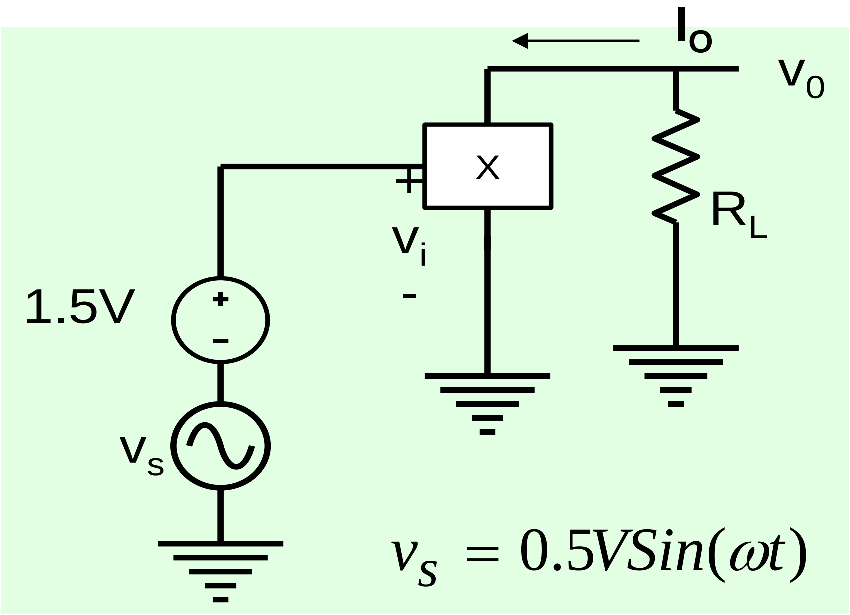



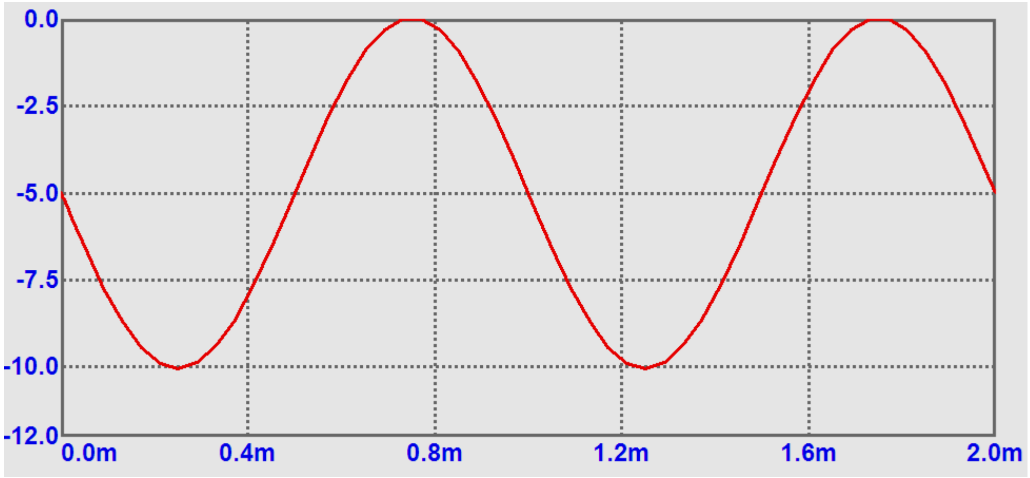

**RECAP**

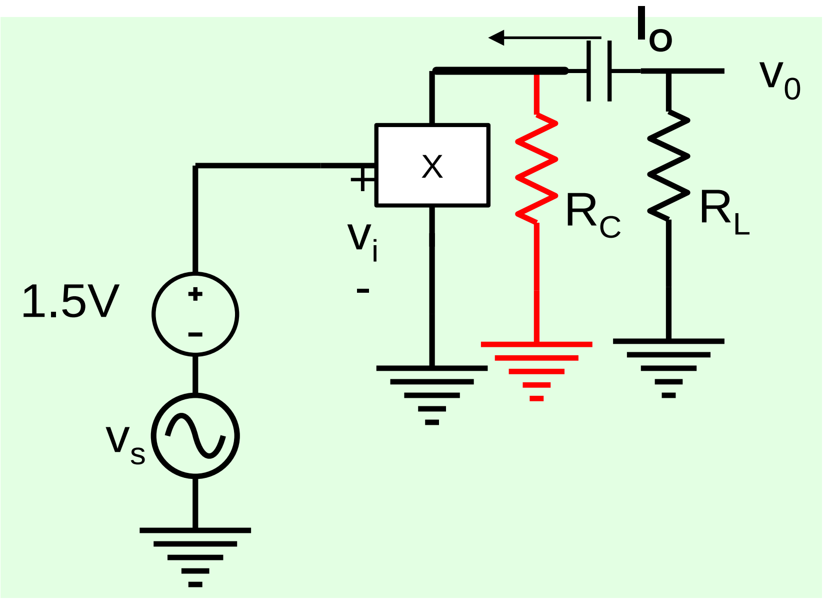


# How do we get rid of unwanted dc voltage at the output ?

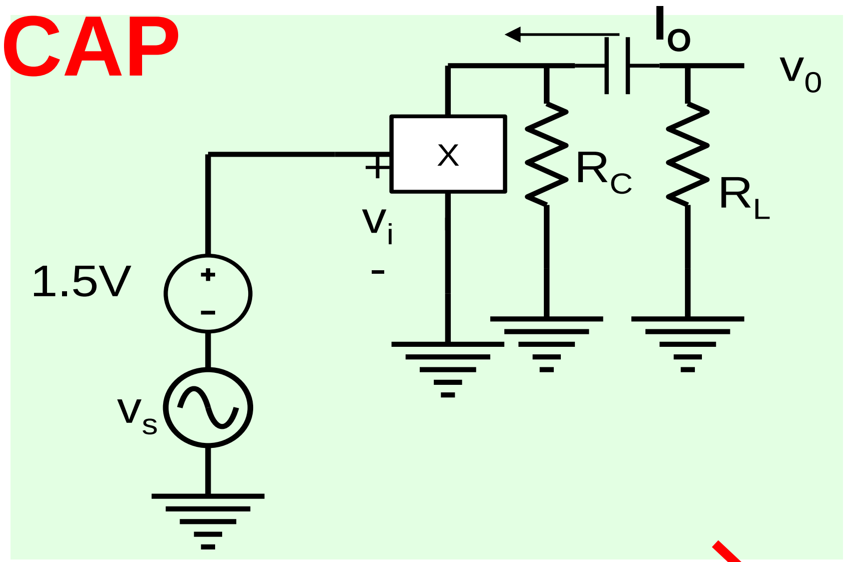
**RECAP**

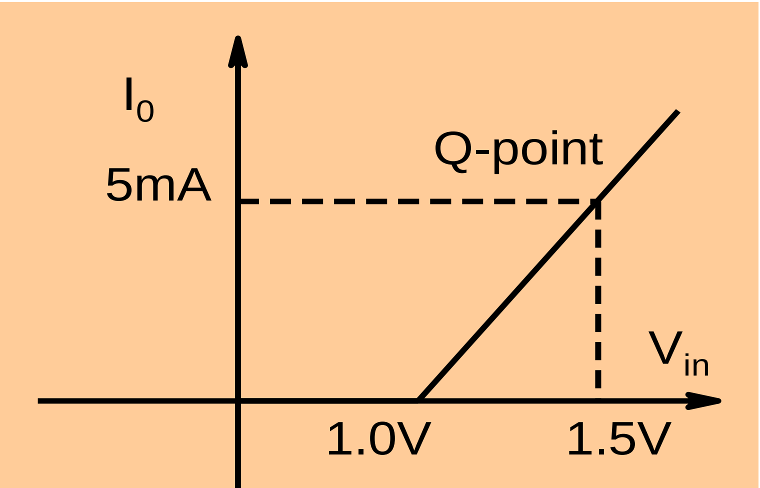


# RECAP

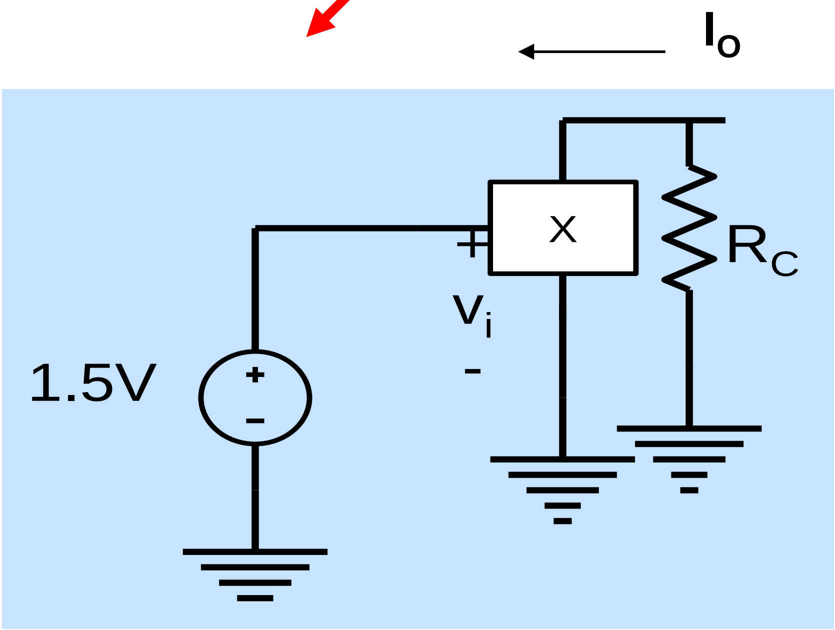


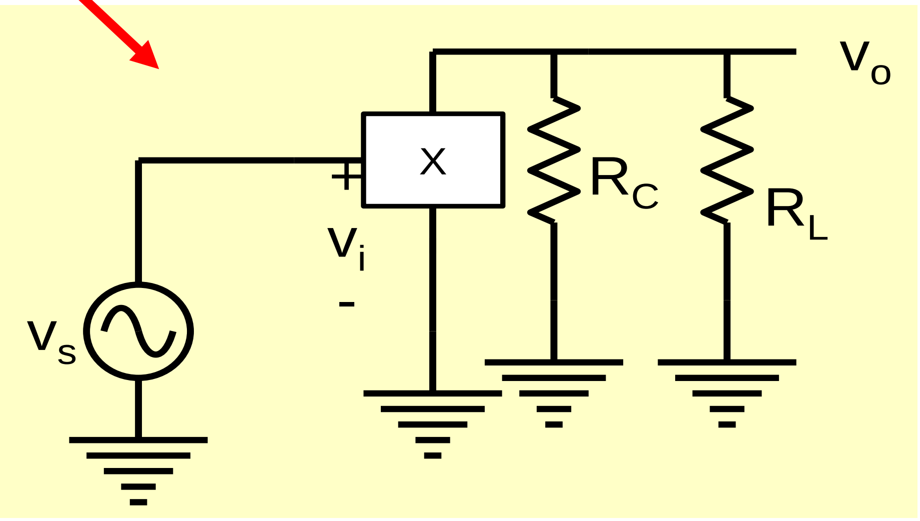




$$V_\alpha = 1V;\ g_m = 0.01\Omega^{-1}$$

dc

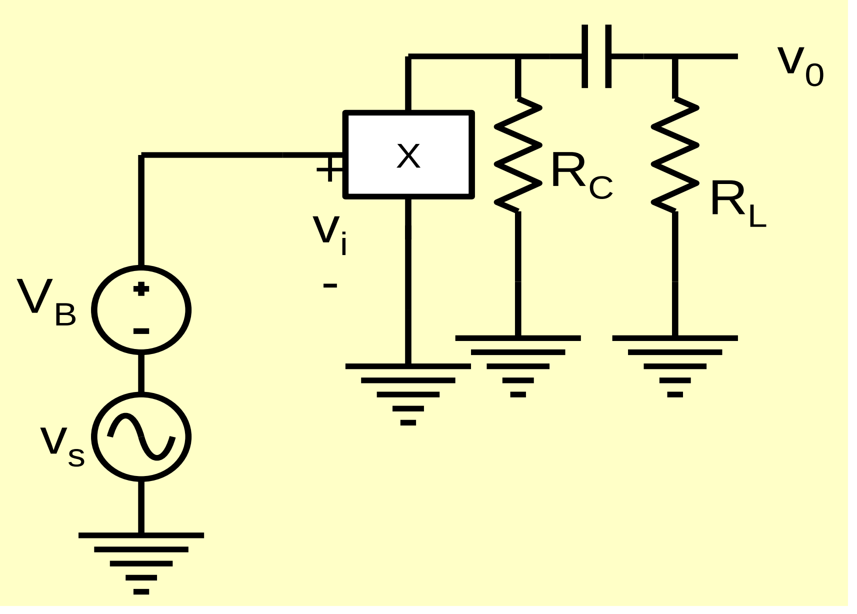
ac (signal)

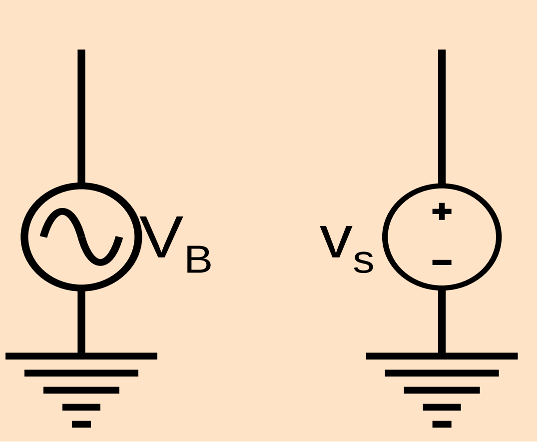


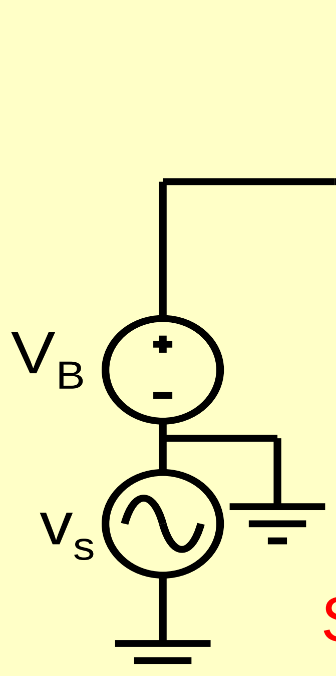




Capacitor is chosen large enough so that at the signal frequency 1/jωC ~0.

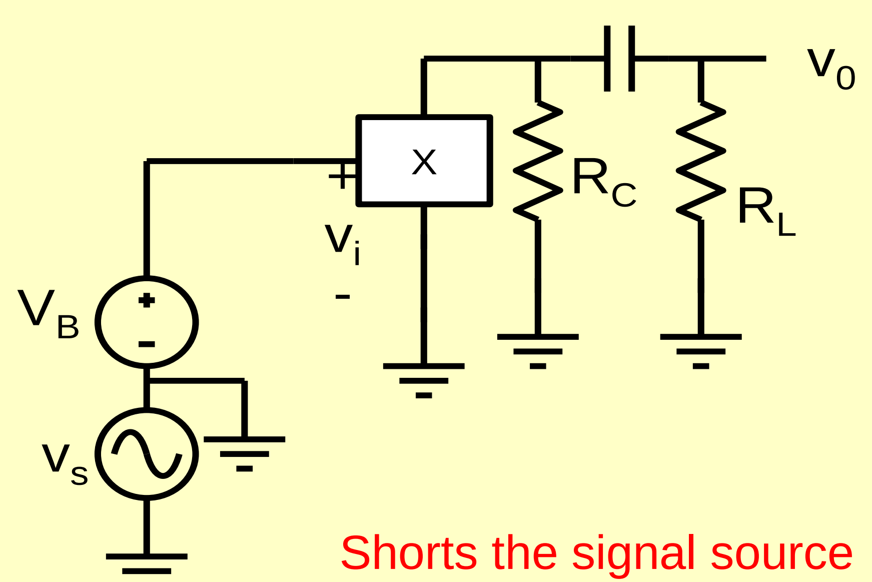
## What happens if both dc voltage source and signal source have one terminal as ground?



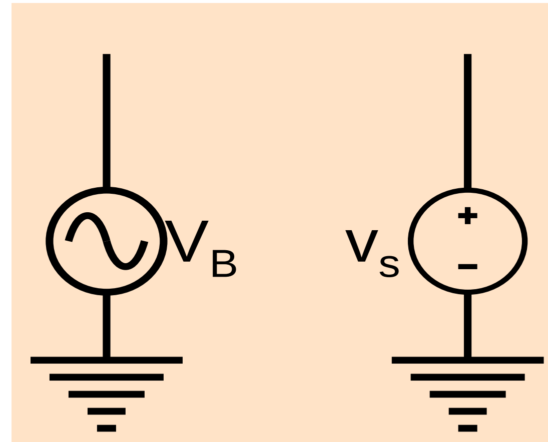




Shorts the signal source

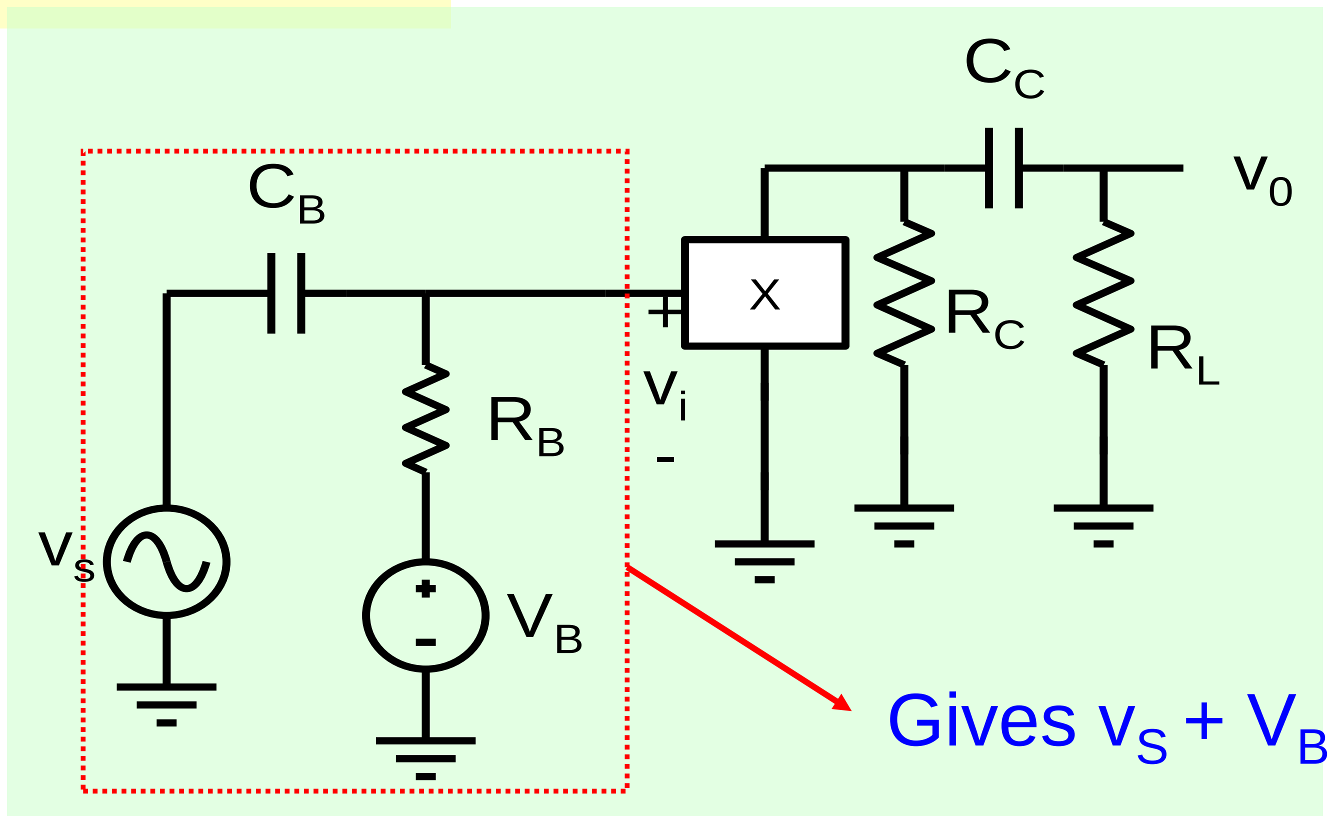


X
$R_C$
$R_L$
$v_0$
+
$v_i$
-
$V_B$
$v_s$
Shorts the signal source

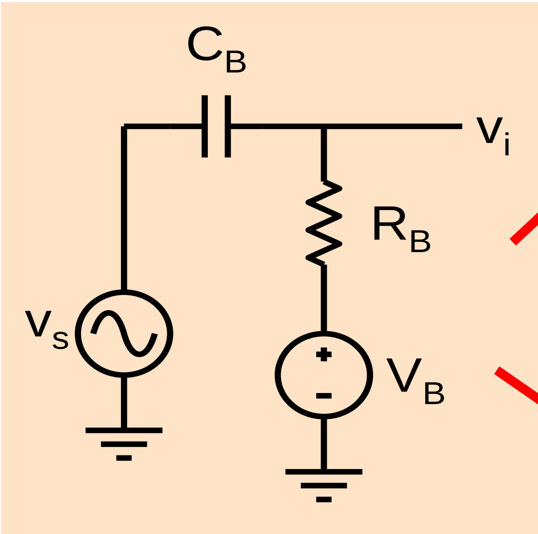



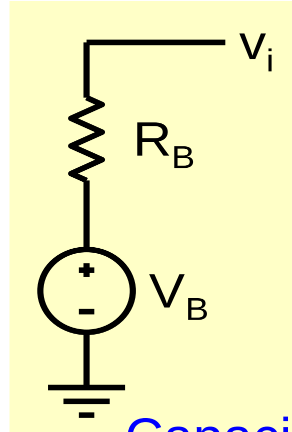
$V_B$
$v_s$


## Solution



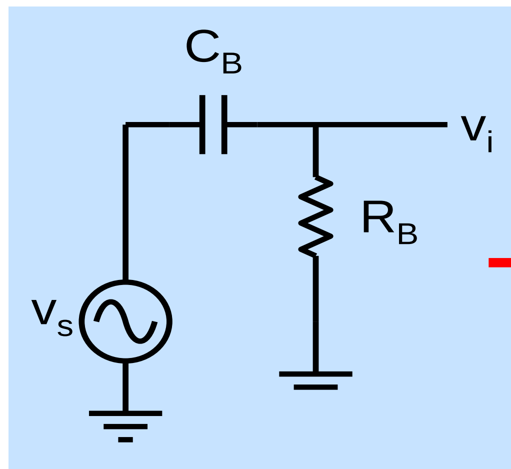
$C_C$
$v_0$
$C_B$
X
$R_C$
$R_L$
+
$v_i$
-
$R_B$
$v_s$
$V_B$
Gives $v_S + V_B$

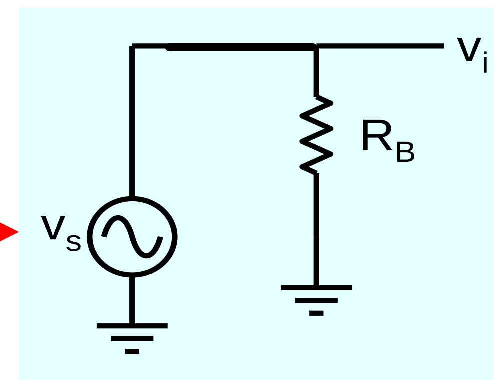



$$v_i = V_B$$

Capacitor is chosen large enough so that at the signal frequency 1/jωC ~0.



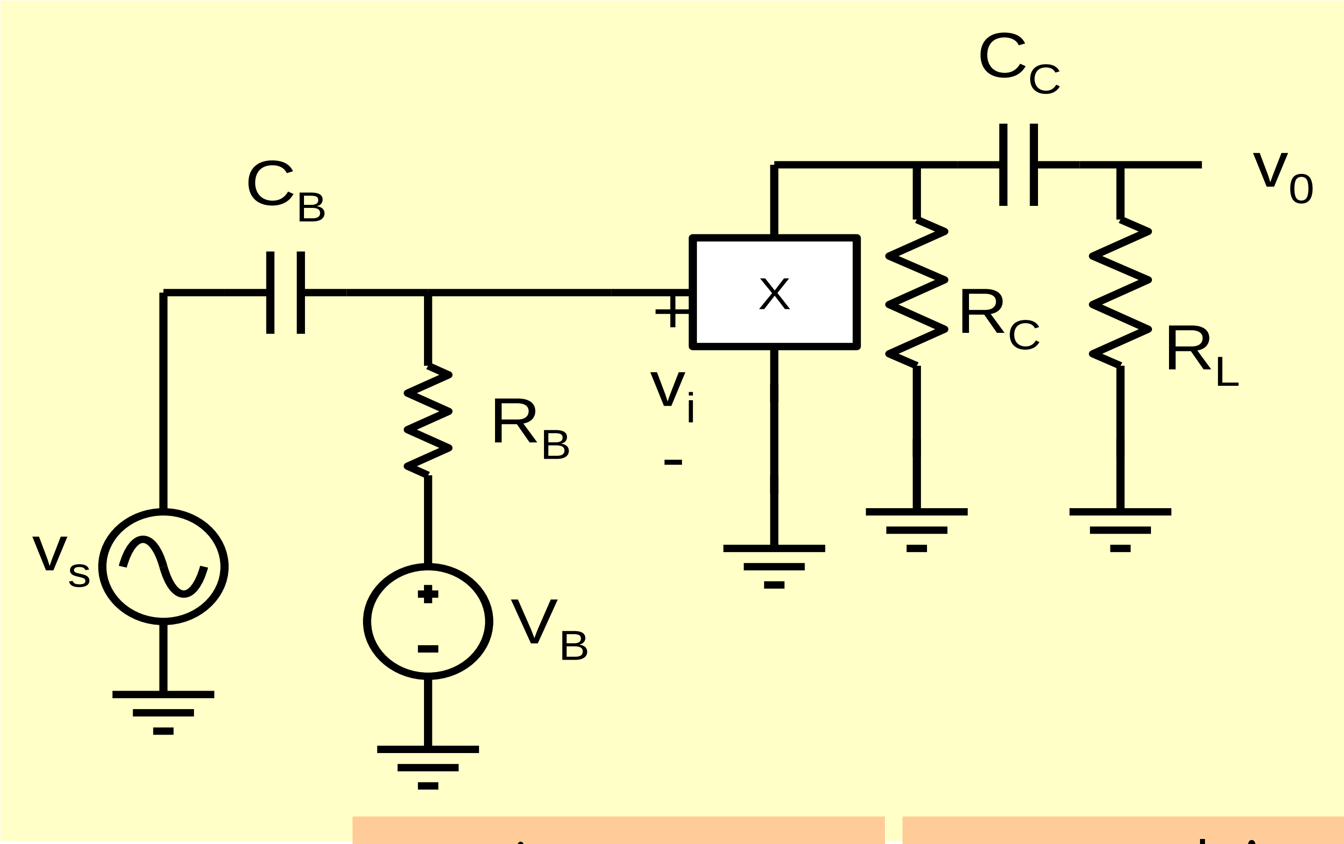



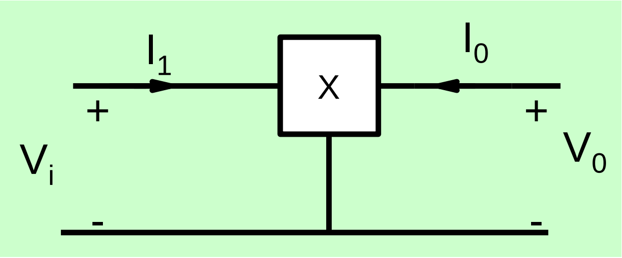

$$v_i = v_s$$

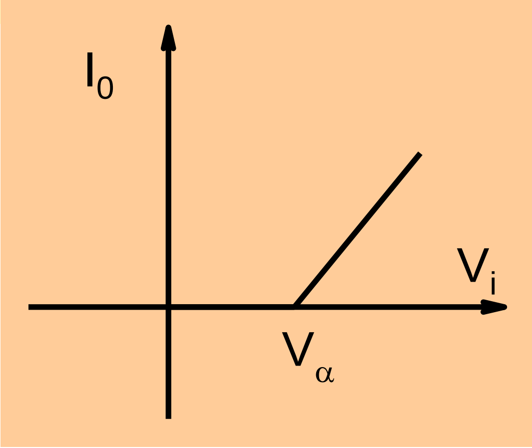
$$v_i(total) = v_s + V_B$$

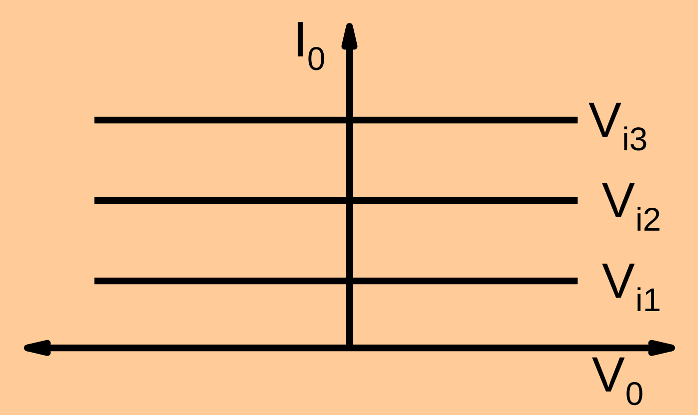
Note the role of $R_B$

# Amplifier Schematic using Device X

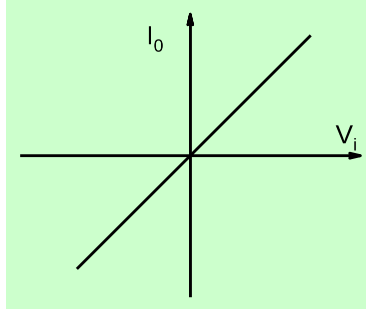


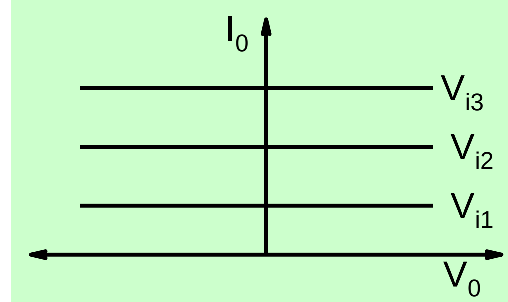



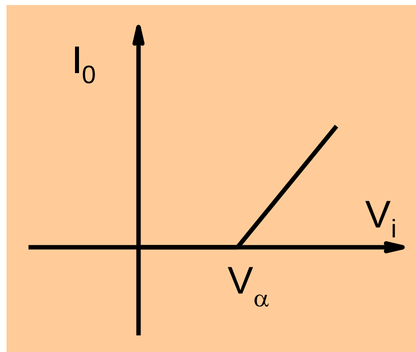



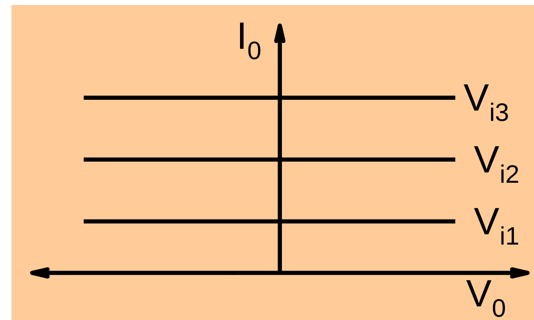
**Ideal transistor**



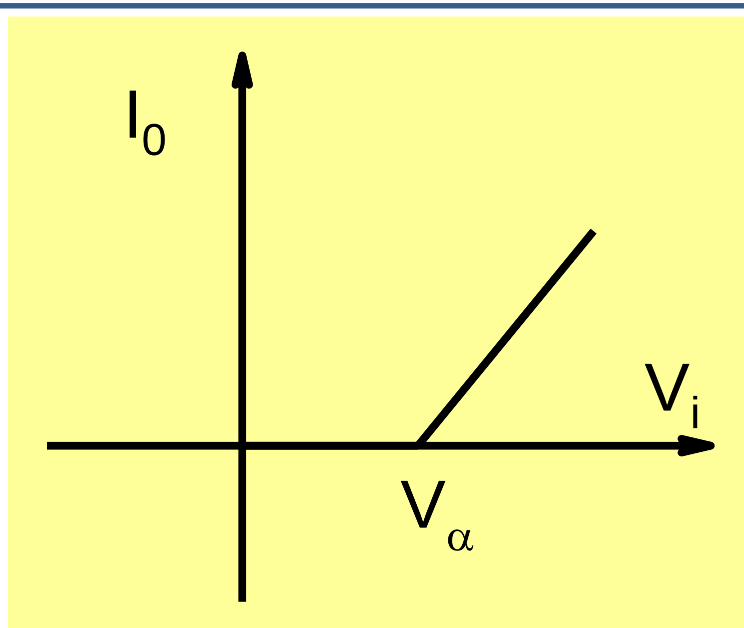



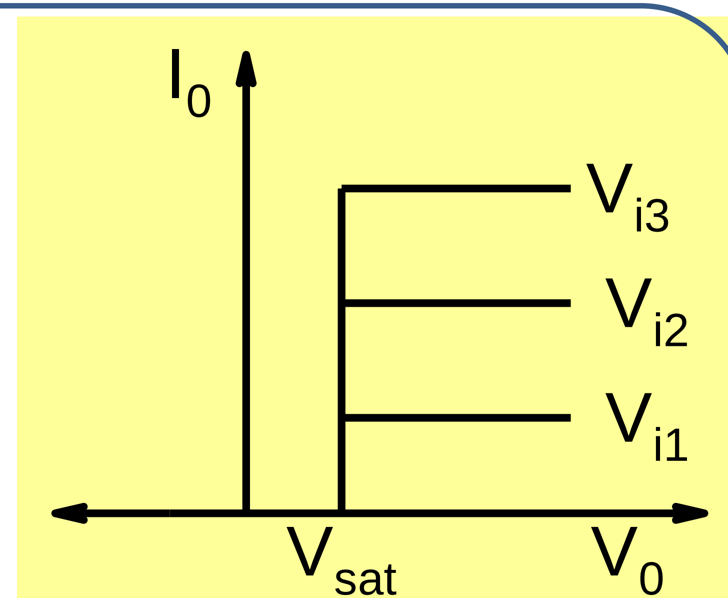

**Device X**



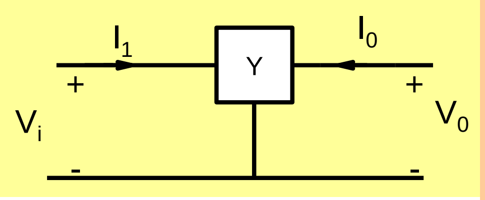

**Device Y**

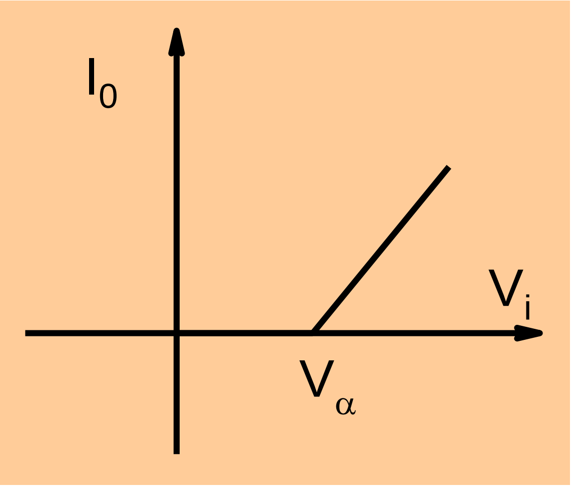


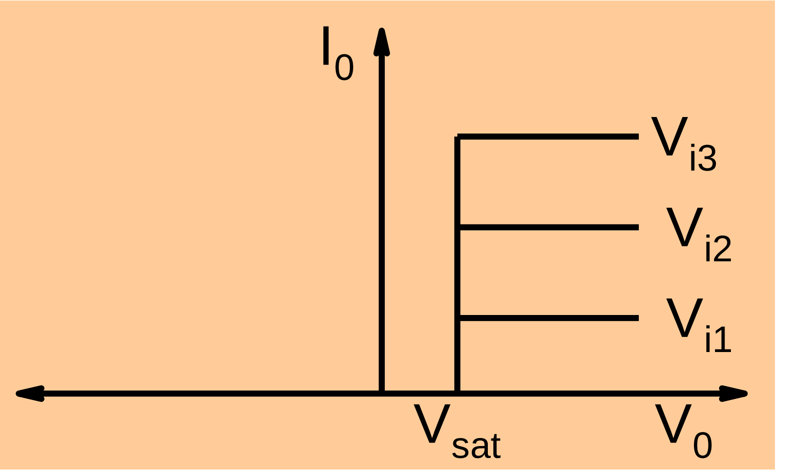




How do we use element Y to make amplifiers?

# Device Y



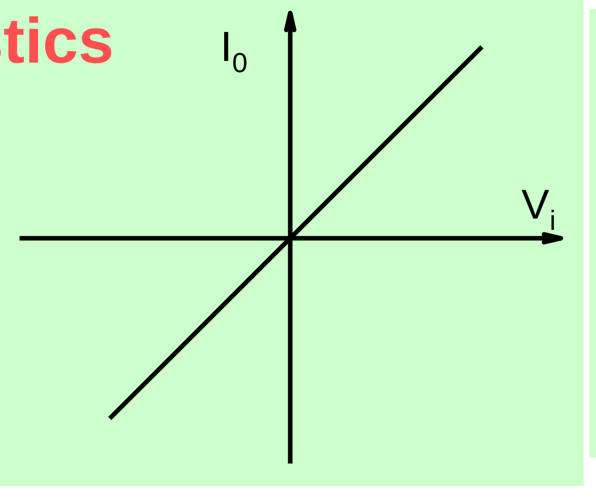



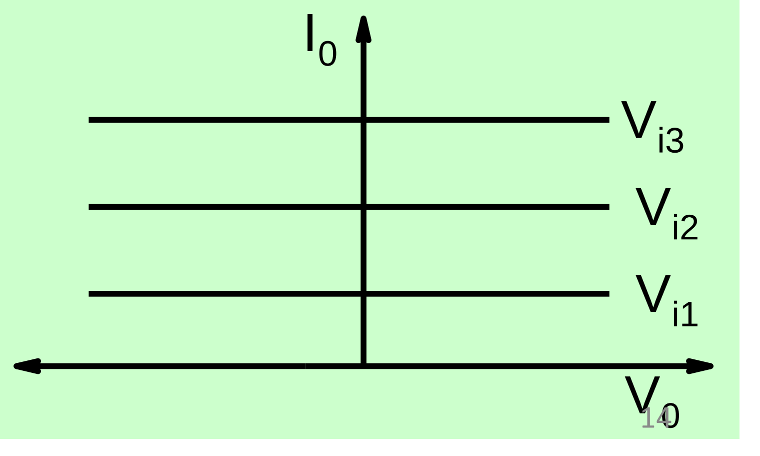




$I_o = 0$ for $V_0 < V_{sat}$

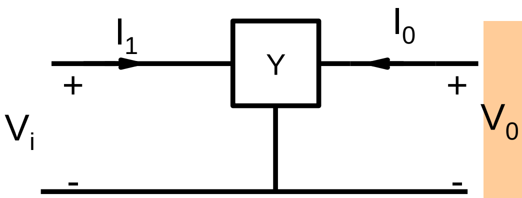
$$\begin{aligned} I_o &= 0 && \text{for } V_i \le V_\alpha \\ &= g_m \times (V_i - V_\alpha) && \text{for } V_i > V_\alpha \end{aligned}$$ for $V_0 > V_{sat}$

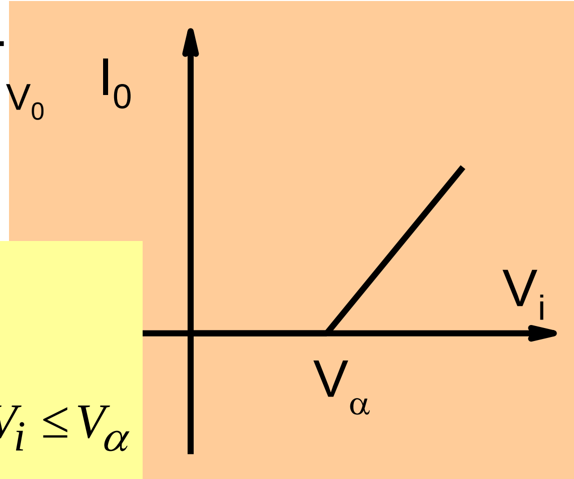
## Ideal Characteristics

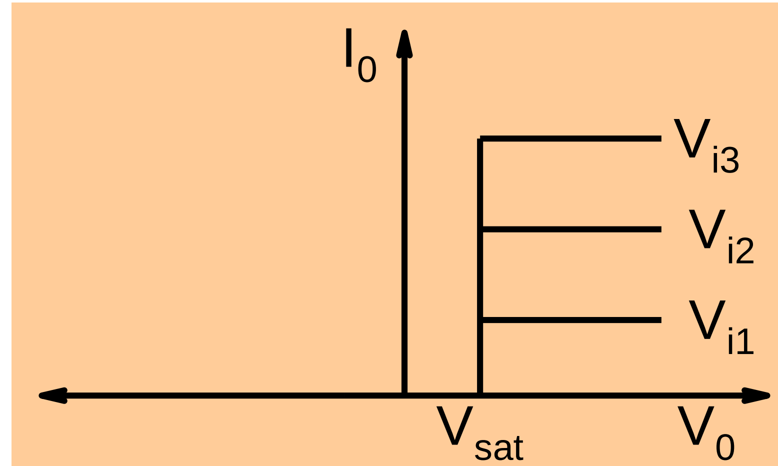


# How do we use device Y to make an amplifier?



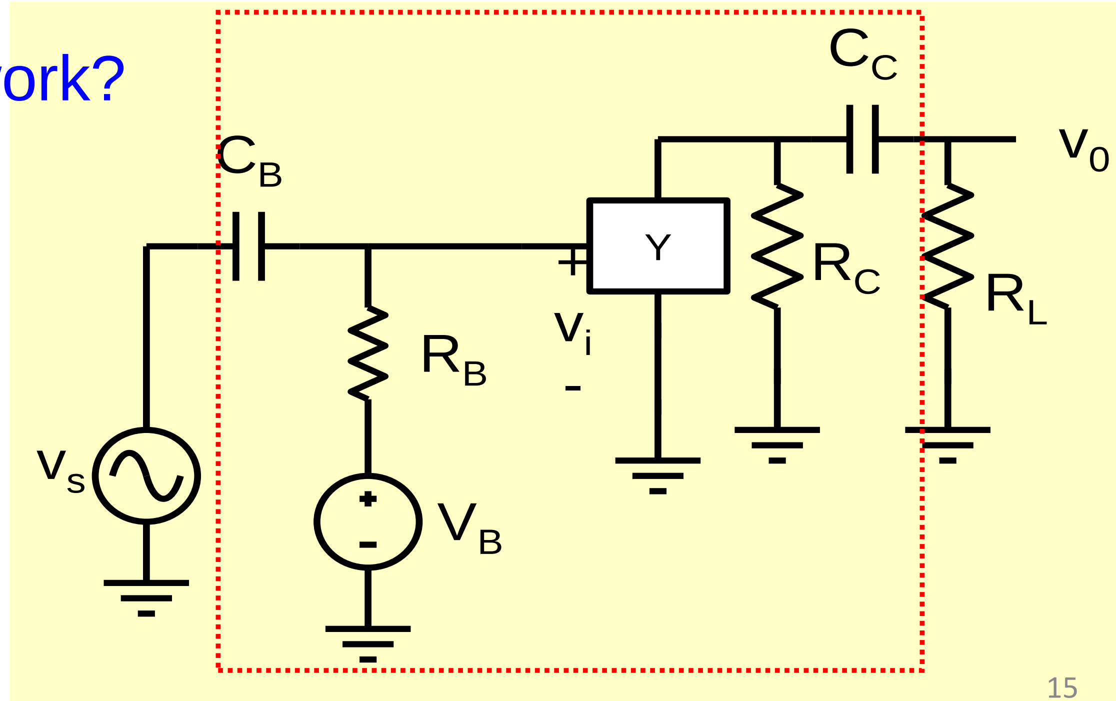

for $V_O < V_{sat} : I_o = 0$

for $V_O \geq V_{sat}$ :

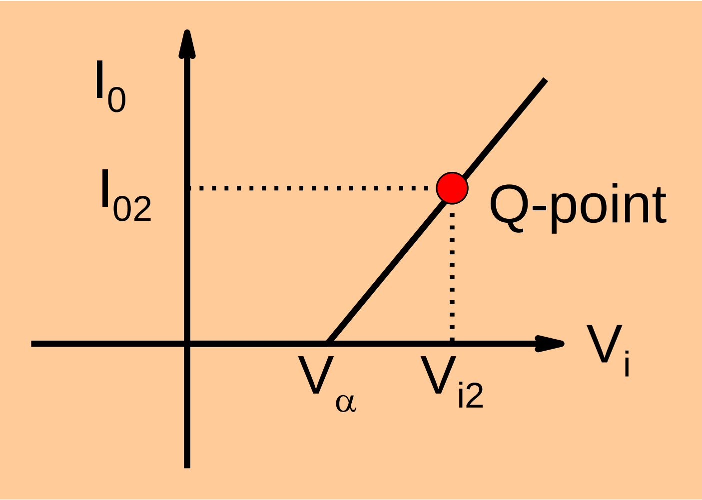
$I_o = 0 \quad$ for $V_i \leq V_\alpha$

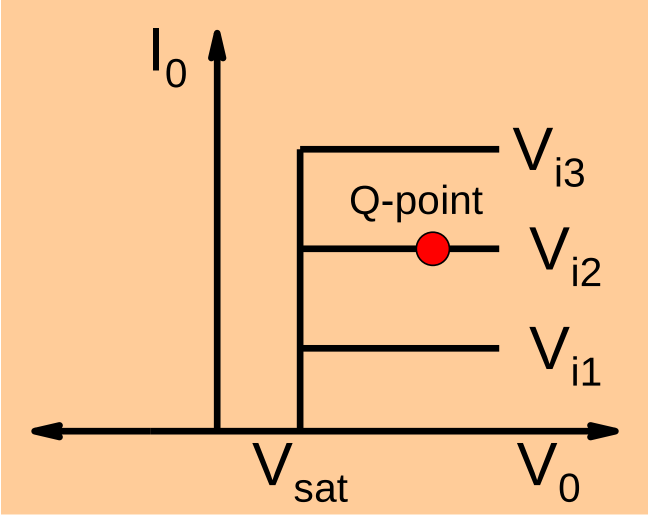
$= g_m \times (V_i - V_\alpha) \quad$ for $V_i > V_\alpha$

Will the earlier solution work?

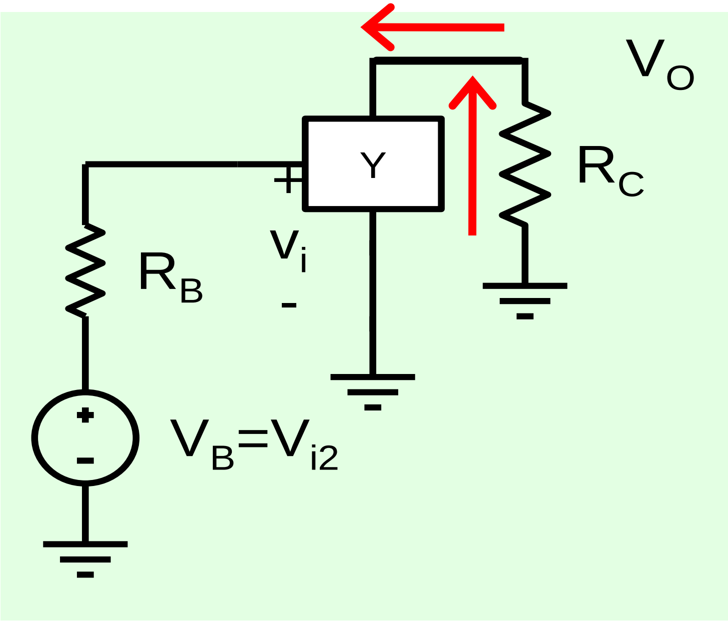


**The purpose of biasing network is to operate the device in a region which resembles ideal transistor**

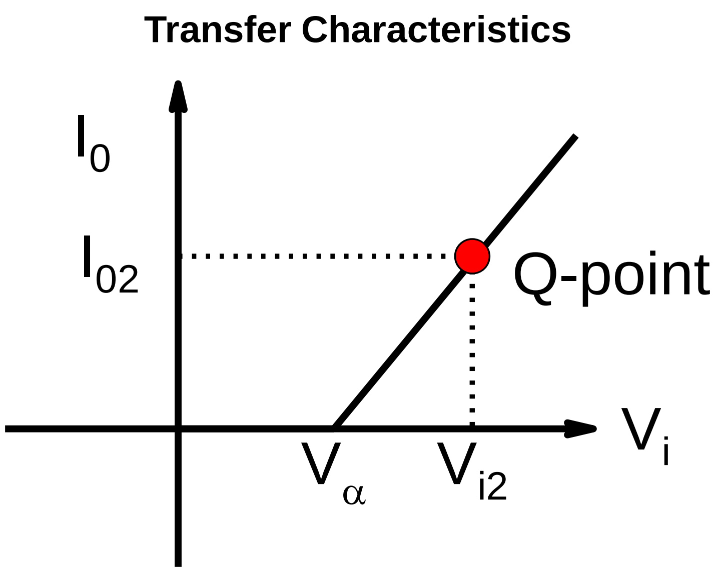


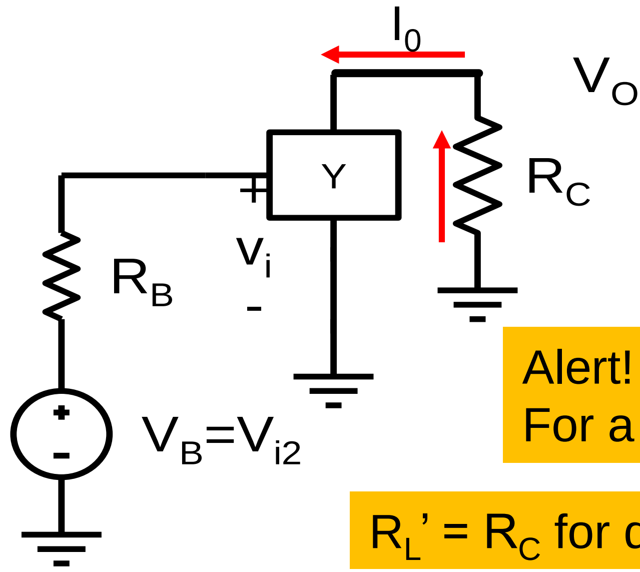




$V_O$ = -ve which is not possible for device Y



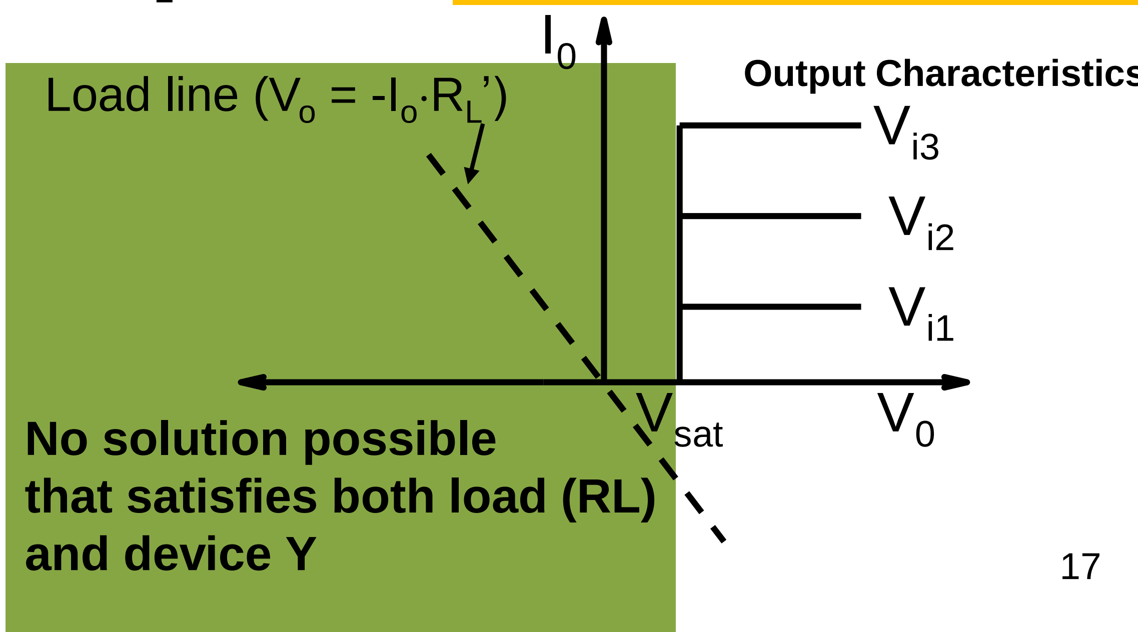
# Earlier Solution in terms of load line



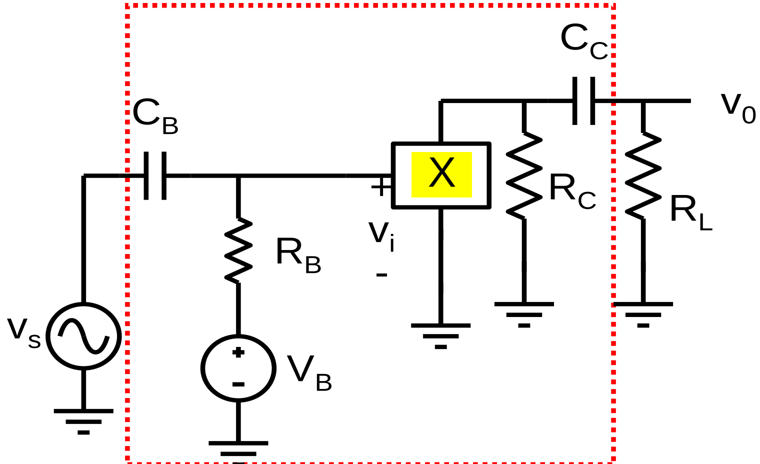

Alert!
For a positive $I_0$, $V_O$ = -ve

$R_L$' = $R_C$ for dc and $R_C||R_L$ for ac



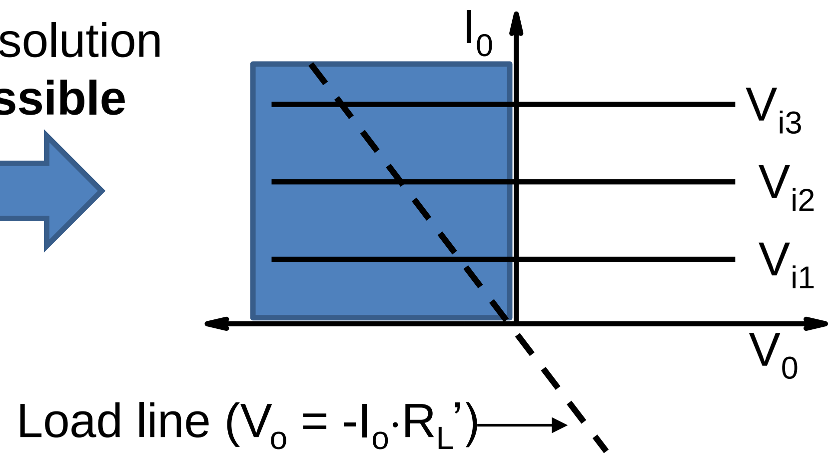
# Why is circuit working for Device X and not for Device Y?

**Device X** discussed in earlier lectures



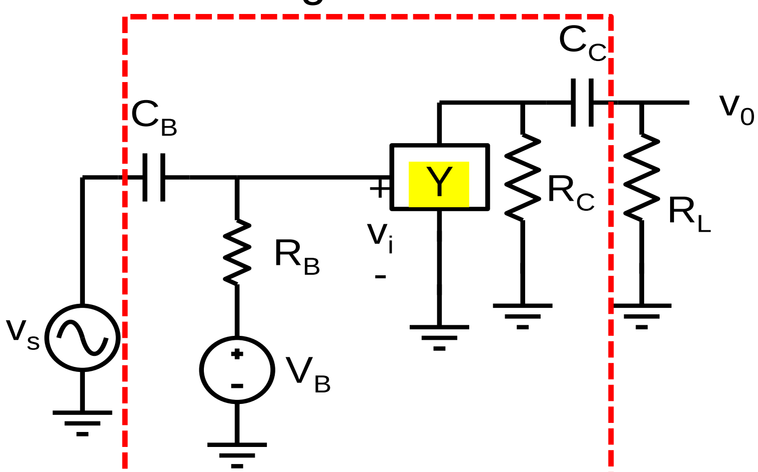

Valid solution
**possible**

**Output Characteristics**

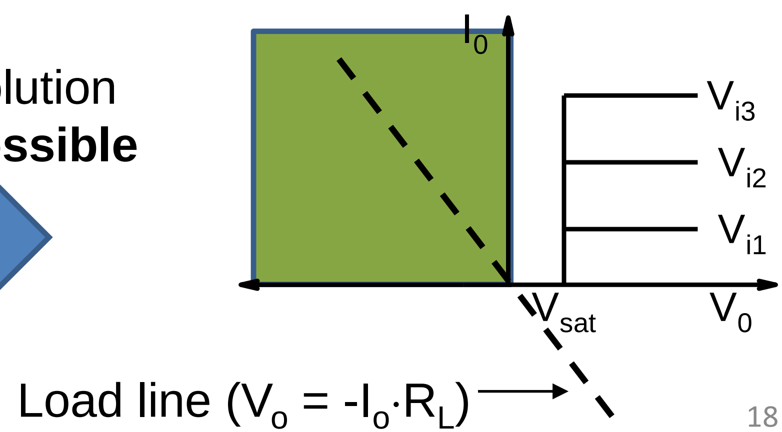



$R_L' = R_C$ for dc and $R_C||R_L$ for ac

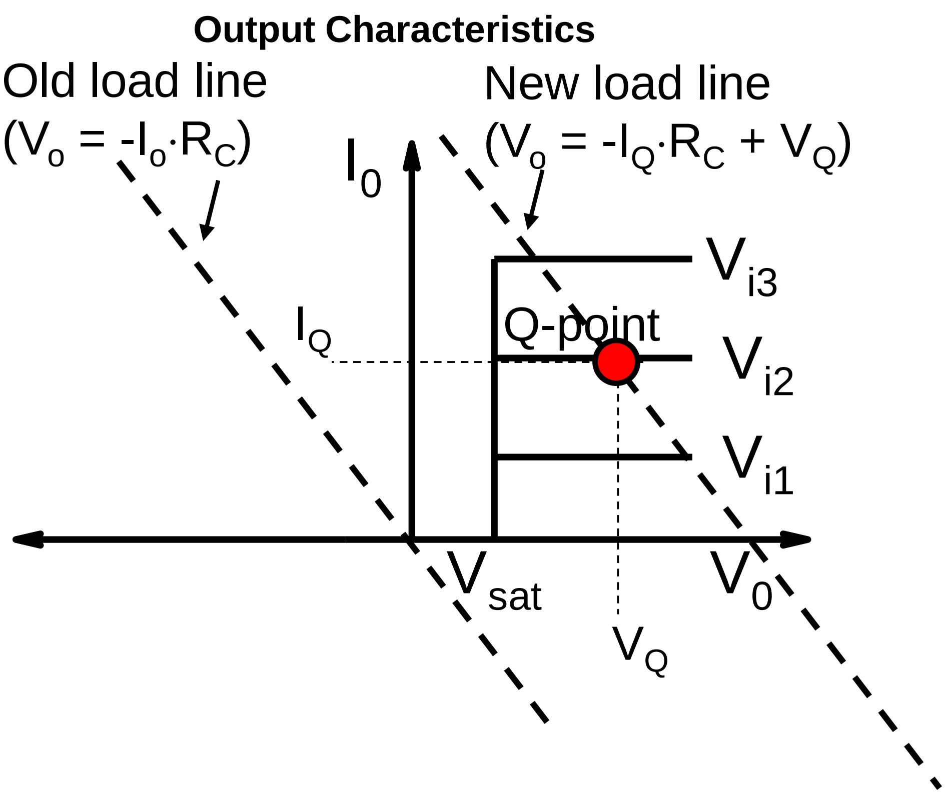
**Device Y** being discussed in current lecture

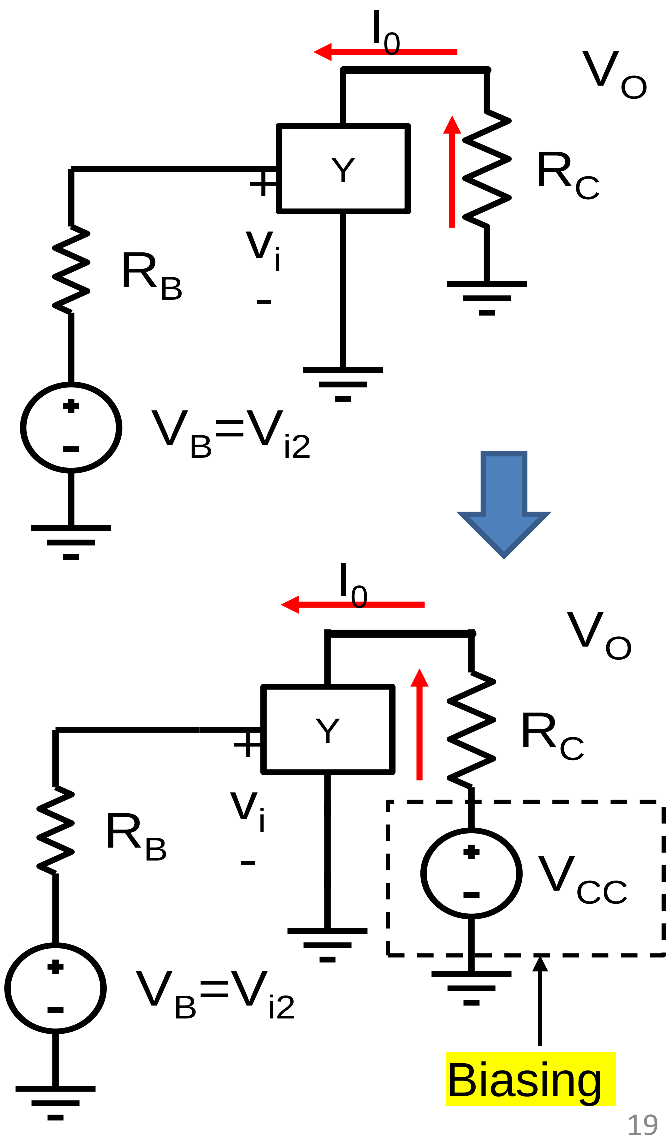



Valid solution
**NOT possible**



# Solution to get meaningful Q point

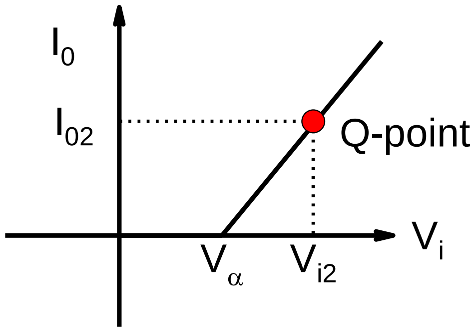


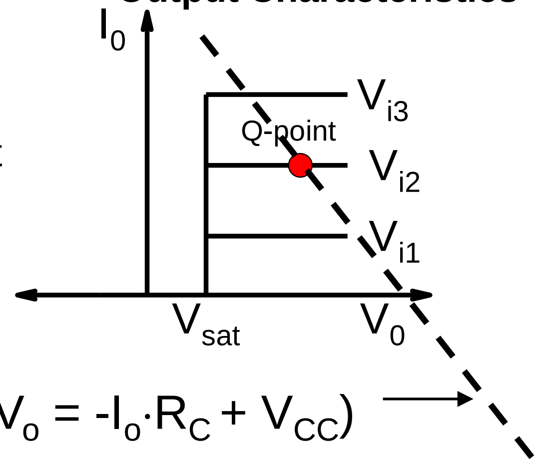

**The purpose of biasing network is to operate the device in a region which resembles ideal transistor**

# Revised Amplifier Schematic for Device Y

**Transfer Characteristics**

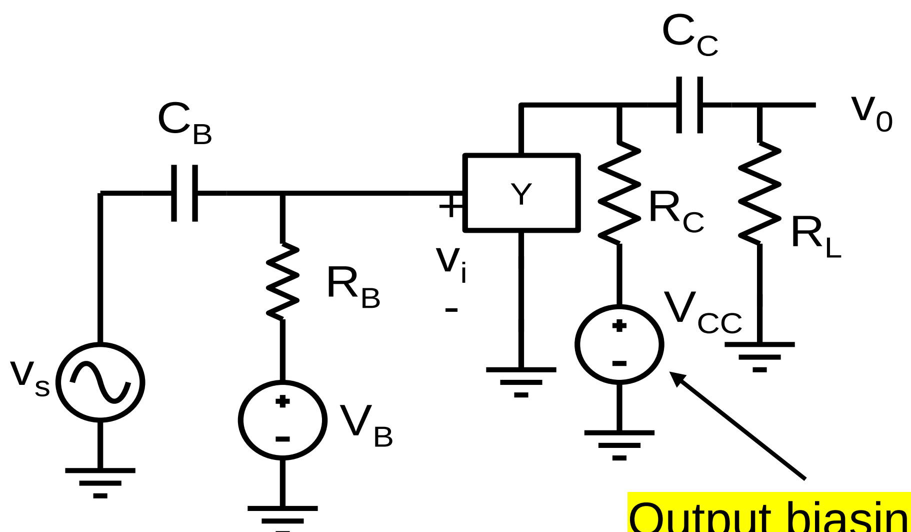



**Output Characteristics**



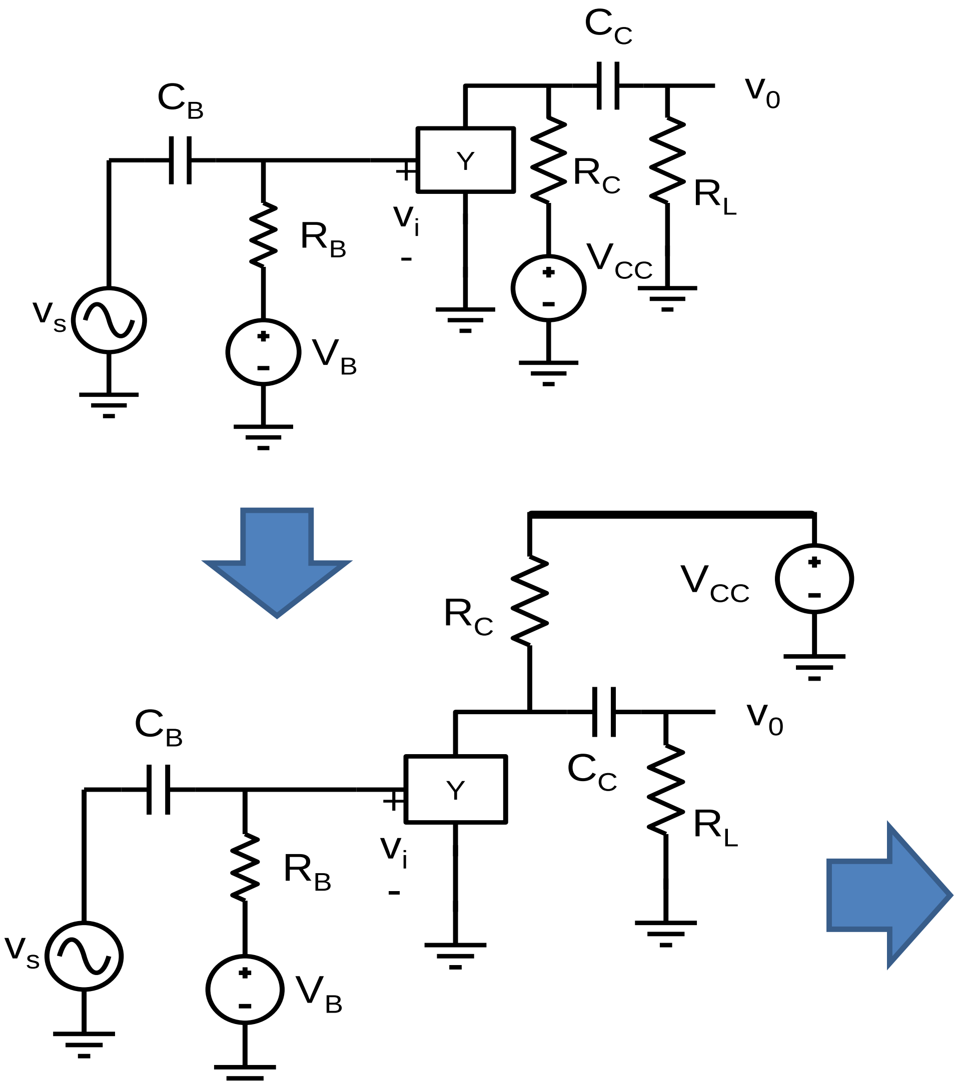

Usually $V_{CC}$ is fixed
$I_0$ and $R_C$ are varied

Load line ($V_o = -I_o \cdot R_C + V_{CC}$)

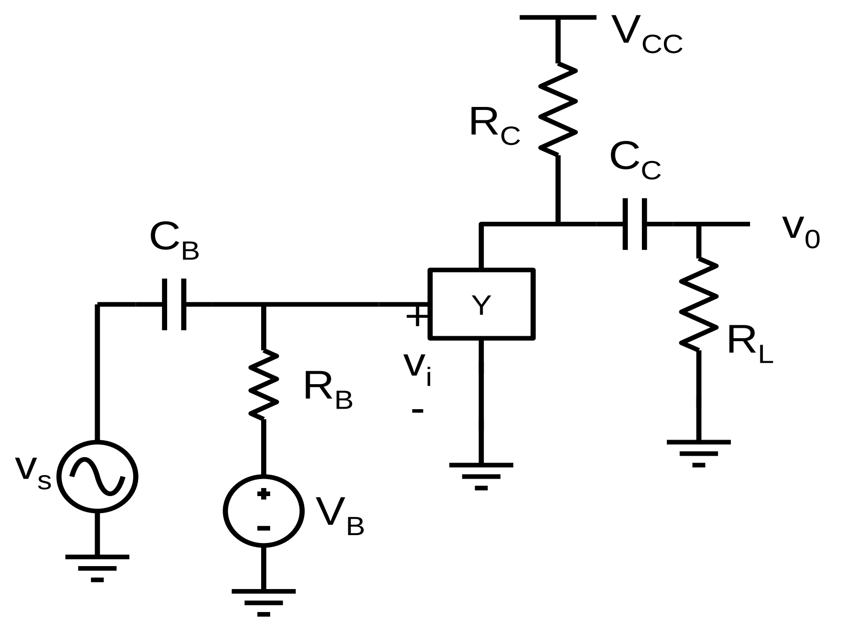



Output biasing is included

# Better representation of biasing

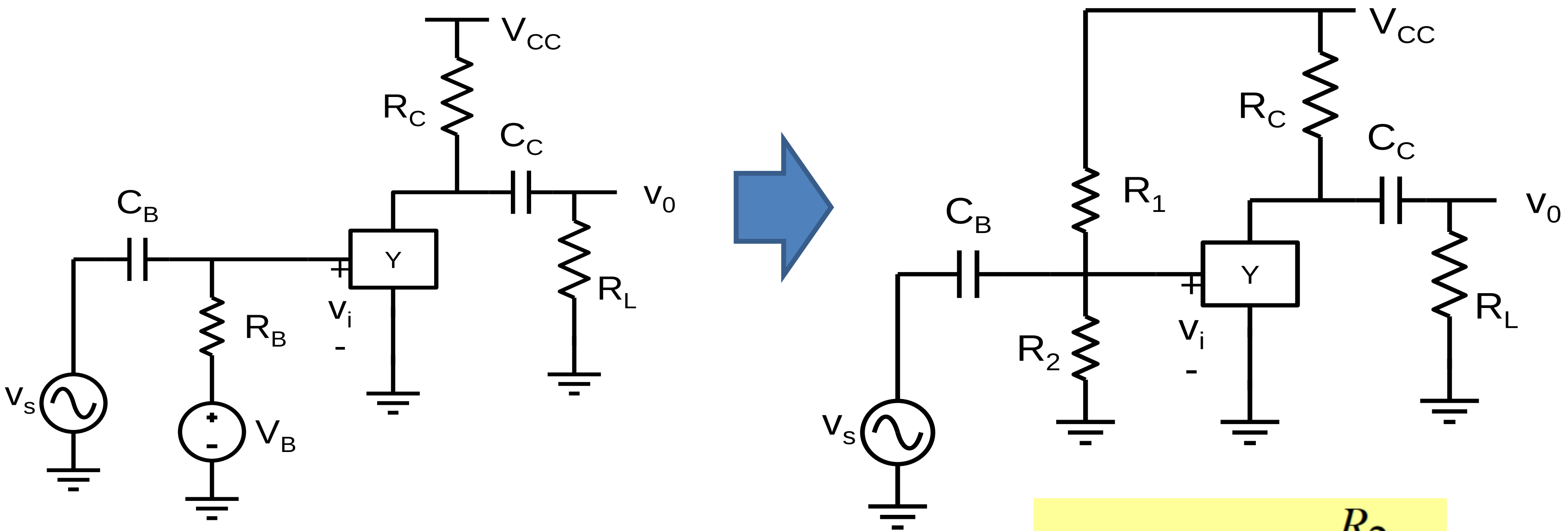



A more common representation



# Economising on power supplies

Can we implement an amplifying circuit using one dc voltage source only?



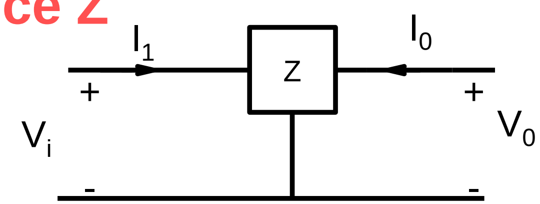

$$V_B = V_{CC} \times \frac{R_2}{R_1 + R_2}$$

and $R_B = R_1 || R_2$

A single supply $V_{CC}$ can be used to provide bias to both input and output

# High response device

**Device Z**




For $V_o < 0.2$ V ⇨ $I_o = 0$ Output characteristics

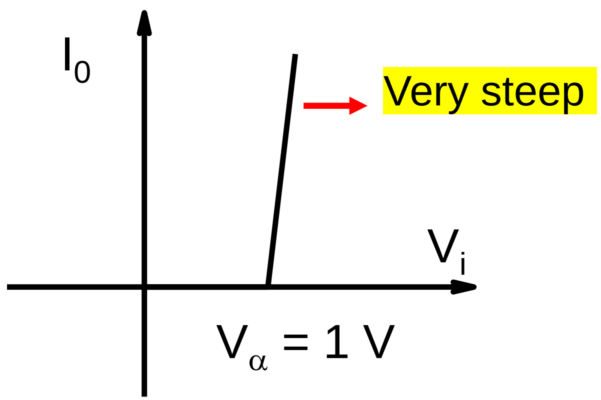
For $V_o \geq 0.2$ V

$I_o = 0$ for $V_i \leq 1$ V

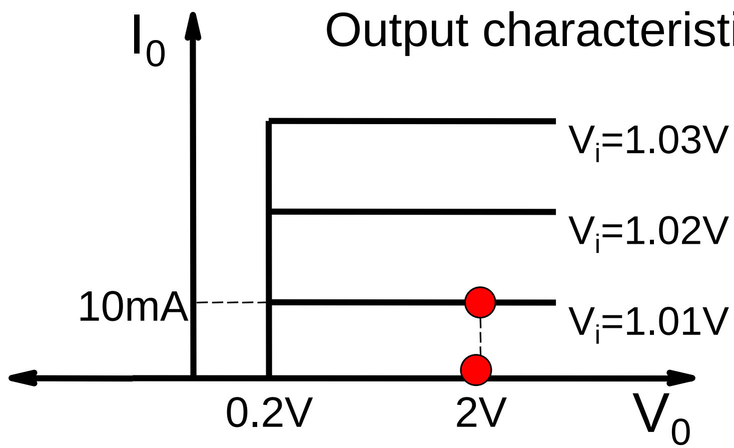
$I_o = 10^3 \cdot (V_i - 1\text{ V})$ mA for $V_i > 1$ V

Transfer characteristics

Transfer characteristics




Output characteristics



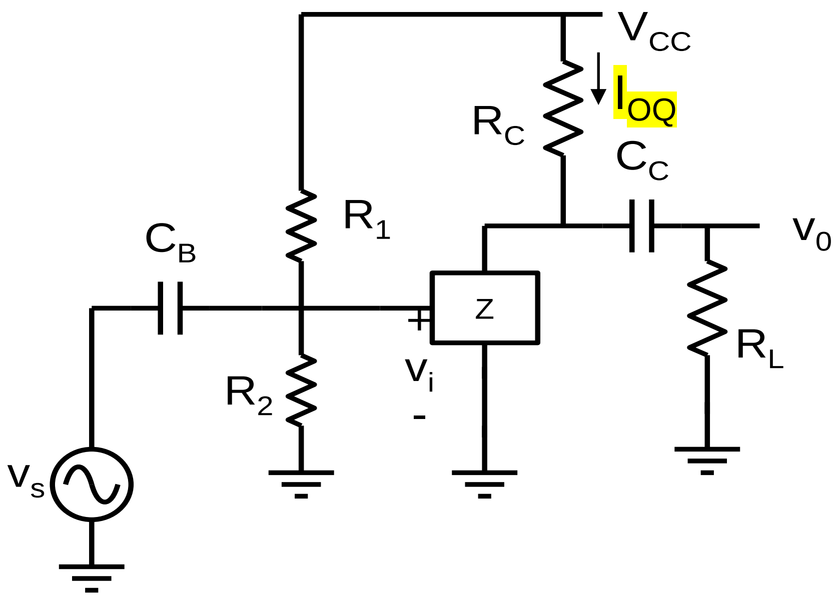

- The voltage gain circuit we designed will be **very sensitive** to:
  - variations in resistor values, power supply, device parameters such as $V_\alpha$,etc.

# Highly sensitive to resistor value

Assume $V_o \geq 0.2$ V by choosing proper bias

$I_o = 0$ for $V_i \leq 1$ V

$I_o = 10^3 \cdot (V_i - 1\ \text{V})$ mA for $V_i > 1$ V




Target Quiescent Current:

$V_{CC} = 5$ V; $R_2 = 1\ \text{k}\Omega$; $R_1 = 3.95\ \text{k}\Omega$

⇨ $V_i = 1.01$ V ⇨ $I_{OQ} = 10$ mA

What if $R_2$ varies?

$V_{CC} = 5$ V; $R_2 = 0.99\ \text{k}\Omega$; $R_1 = 3.95\ \text{k}\Omega$

⇨ $V_i = 1.002$ V ⇨ $I_{OQ} = 1.9$ mA

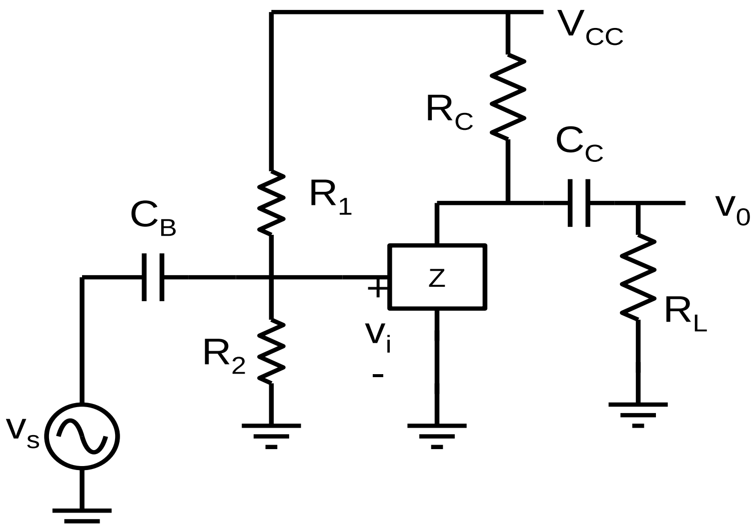
$V_{CC} = 5$ V; $R_2 = 0.98\ \text{k}\Omega$; $R_1 = 3.95\ \text{k}\Omega$

⇨ $V_i = 0.994$ V ⇨ $I_{OQ} = 0$ mA

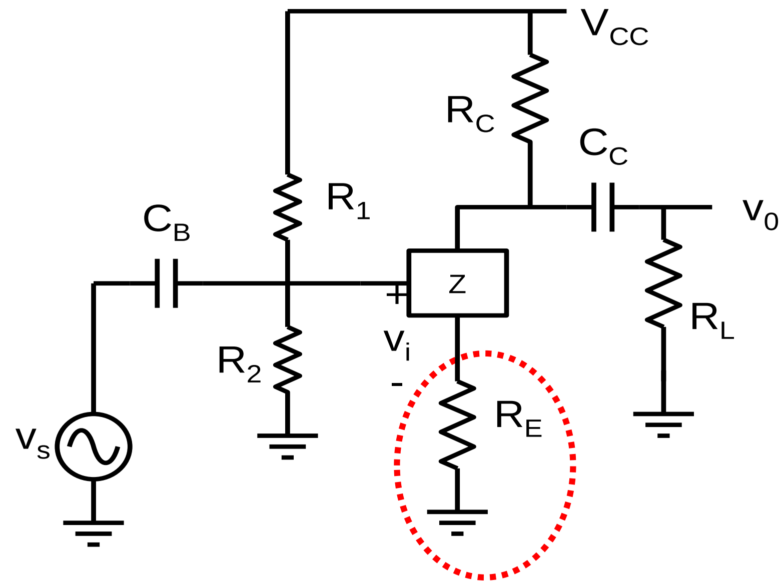
A 2% drop in $R_2$ value causes the circuit to become non-operational!

# A solution

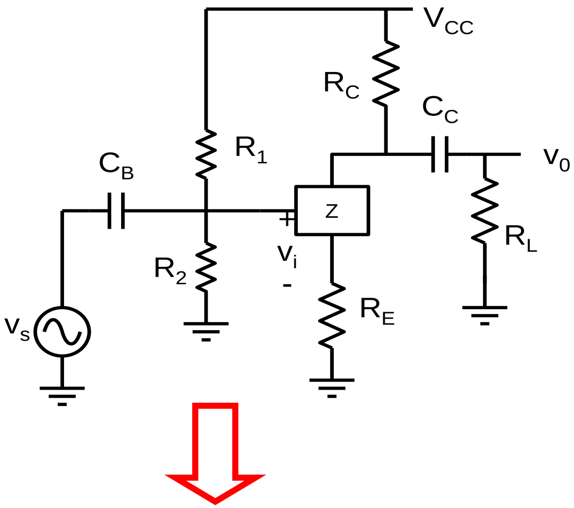
Original Circuit



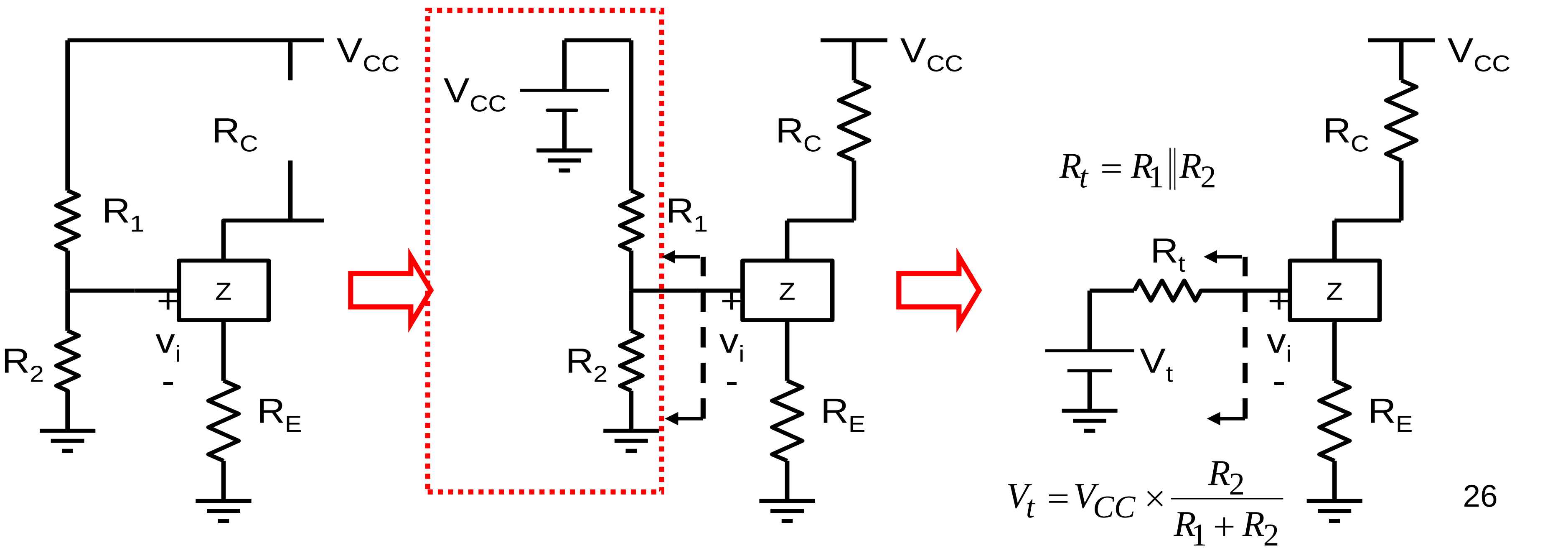

Modified Circuit



# DC analysis of modified circuit



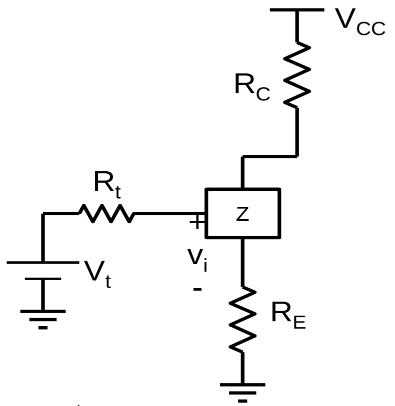

Represent the input bias as:
Thévenin equivalent as seen from input

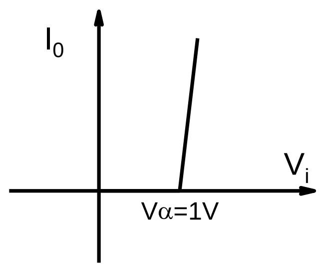


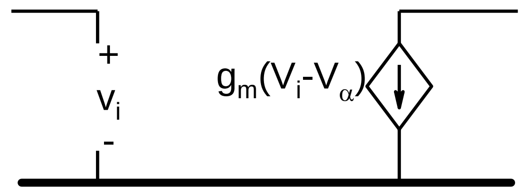

$$R_t = R_1 \| R_2$$

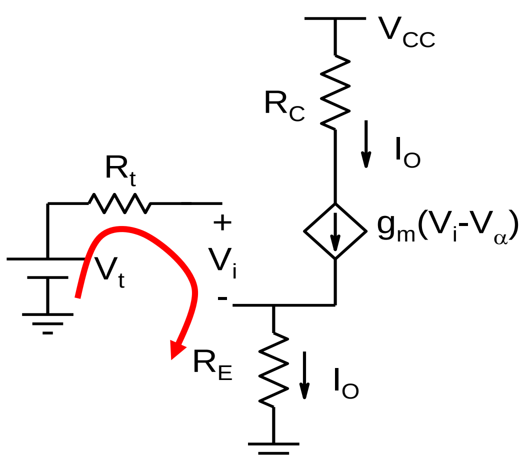
$$V_t = V_{CC} \times \frac{R_2}{R_1 + R_2}$$

# DC analysis of modified circuit




$$-V_t + 0 \times R_t + V_i + I_O R_E = 0$$

Since $I_o$ vs. $V_i$ characteristics is very sharp, $V_i \sim V_\alpha = 1\text{V}$

$$I_O \cong \frac{V_t - V_\alpha}{R_E}$$

If $V_t$ changes by 1% due to variation in resistor values then the change in output current is proportional.

Circuit much less sensitive to variations in circuit parameters