COMP551 – Interfacing

Fall 2017

Lab 7

Programming PWM with CCP Modules

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Students:		
Student ID's:		
Section:	**01** **02** **03** **04**	

NOTE: Labs are due at the start of the next lab period. Only submit one lab per group of two students.

Lab 7 – Programming PWM with CCP Modules

7. Introduction:

In previous labs you've seen how PIC18 Timers can been programmed to create square waves. Timers can also be used to create Pulse Width Modulated (PWM) wave forms, however, using Timers to program PWM waveforms can be a tedious task. The PIC18 CCP (Capture, Compare, PWM) modules, make the programming of PWM waveforms much easier and less tedious. PWM is used in industrial controls systems to control D.C. motors, by sending D.C. pulses to the motor and by varying the width of those pulses. PWM can also be used to control the intensity of a light or a LED.

In creating pulses with variable widths for PWM, two factors are important; the period of the pulse and its duty cycles. The duty cycle (DC) is the portion of the pulse that stays HIGH relative to the entire period. Duty cycle is usually stated as a percentage. For example, a pulse with a period of 8 ms, that stays HIGH for 2 ms, has a DC of 25%.

7.1.1 Review the information in the attached data sheets, as well as the information on PIC18 CCP modules in the lecture notes and then complete the exercise at the end of the lab.

13.0 TIMER2 MODULE

The Timer2 timer module incorporates the following features:

- 8-Bit Timer and Period registers (TMR2 and PR2, respectively)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4 and 1:16)
- Software programmable postscaler (1:1 through 1:16)
- Interrupt on TMR2 to PR2 match
- Optional use as the shift clock for the MSSPx modules

The module is controlled through the T2CON register (Register 13-1) which enables or disables the timer and configures the prescaler and postscaler. Timer2 can be shut off by clearing control bit, TMR2ON (T2CON<2>), to minimize power consumption.

A simplified block diagram of the module is shown in Figure 13-1.

13.1 Timer2 Operation

In normal operation, TMR2 is incremented from 00h on each clock (Fosc/4). A 4-bit counter/prescaler on the clock input gives direct input, divide-by-4 and divide-by-16 prescale options. These options are selected by the prescaler control bits, T2CKPS1:T2CKPS0 (T2CON<1:0>). The value of TMR2 is compared to that of the Period register, PR2, on each clock cycle. When the two values match, the comparator generates a match signal as the timer output. This signal also resets the value of TMR2 to 00h on the next cycle and drives the output counter/postscaler (see **Section 13.2 "Timer2 Interrupt"**).

The TMR2 and PR2 registers are both directly readable and writable. The TMR2 register is cleared on any device Reset, while the PR2 register initializes at FFh. Both the prescaler and postscaler counters are cleared on the following events:

- a write to the TMR2 register
- a write to the T2CON register
- any device Reset (Power-on Reset, $\overline{\text{MCLR}}$ Reset, Watchdog Timer Reset or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

REGISTER 13-1: T2CON: TIMER2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7 **Unimplemented:** Read as '0'

bit 6-3 **T2OUTPS3:T2OUTPS0**: Timer2 Output Postscale Select bits

0000 = 1:1 Postscale
0001 = 1:2 Postscale
•
•
•
1111 = 1:16 Postscale

bit 2 **TMR2ON**: Timer2 On bit

1 = Timer2 is on
0 = Timer2 is off

bit 1-0 **T2CKPS1:T2CKPS0**: Timer2 Clock Prescale Select bits

00 = Prescaler is 1
01 = Prescaler is 4
1x = Prescaler is 16

16.0 CAPTURE/COMPARE/PWM (CCP) MODULES

Members of the PIC18F97J60 family of devices all have a total of five CCP (Capture/Compare/PWM) modules. Two of these (CCP4 and CCP5) implement standard Capture, Compare and Pulse-Width Modulation (PWM) modes and are discussed in this section. The other three modules (ECCP1, ECCP2, ECCP3) implement standard Capture and Compare modes, as well as Enhanced PWM modes. These are discussed in **Section 17.0 "Enhanced Capture/Compare/PWM (ECCP) Modules"**.

Each CCPx/ECCPx module contains a 16-bit register which can operate as a 16-Bit Capture register, a 16-Bit Compare register or a PWM Master/Slave Duty Cycle register. For the sake of clarity, all CCPx module operation in the following sections is described with respect to CCP4, but is equally applicable to CCP5.

Capture and Compare operations described in this chapter apply to all standard and Enhanced CCPx modules. The operations of PWM mode, described in **Section 16.4 "PWM Mode"**, apply to CCP4 and CCP5 only.

Note: Throughout this section and **Section 17.0 "Enhanced Capture/Compare/PWM (ECCP) Modules"**, references to register and bit names that may be associated with a specific CCP module are referred to generically by the use of 'x' or 'y' in place of the specific module number. Thus, "CCPxCON" might refer to the control register for ECCP1, ECCP2, ECCP3, CCP4 or CCP5.

REGISTER 16-1: CCPxCON: CCPx CONTROL REGISTER (CCP4 AND CCP5)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **DCxB1:DCxB0**: CCPx Module PWM Duty Cycle bit 1 and bit 0

Capture mode:
Unused.

Compare mode:
Unused.

PWM mode:
These bits are the two Least Significant bits (bit 1 and bit 0) of the 10-bit PWM duty cycle. The eight Most Significant bits (DCxB9:DCxB2) of the duty cycle are found in CCPRxL.

bit 3-0 **CCPxM3:CCPxM0**: CCPx Module Mode Select bits

0000 = Capture/Compare/PWM disabled (resets CCPx module)
0001 = Reserved
0010 = Compare mode; toggle output on match (CCPxIF bit is set)
0011 = Reserved
0100 = Capture mode; every falling edge
0101 = Capture mode; every rising edge
0110 = Capture mode; every 4th rising edge
0111 = Capture mode; every 16th rising edge
1000 = Compare mode; initialize CCPx pin low; on compare match, force CCPx pin high (CCPxIF bit is set)
1001 = Compare mode; initialize CCPx pin high; on compare match, force CCPx pin low (CCPxIF bit is set)
1010 = Compare mode; generate software interrupt on compare match (CCPxIF bit is set, CCPx pin reflects I/O state)
1011 = Reserved
11xx = PWM mode

16.1 CCPx Module Configuration

Each Capture/Compare/PWM module is associated with a control register (generically, CCPxCON) and a data register (CCPRx). The data register, in turn, is comprised of two 8-bit registers: CCPRxL (low byte) and CCPRxH (high byte). All registers are both readable and writable.

16.1.1 CCPx/ECCPx MODULES AND TIMER RESOURCES

The CCPx/ECCPx modules utilize Timers 1, 2, 3 or 4, depending on the mode selected. Timer1 and Timer3 are available to modules in Capture or Compare modes, while Timer2 and Timer4 are available for modules in PWM mode.

TABLE 16-1: CCPx/ECCPx MODE – TIMER RESOURCE

CCPx/ECCPx Mode	Timer Resource
Capture	Timer1 or Timer3
Compare	Timer1 or Timer3
PWM	Timer2 or Timer4

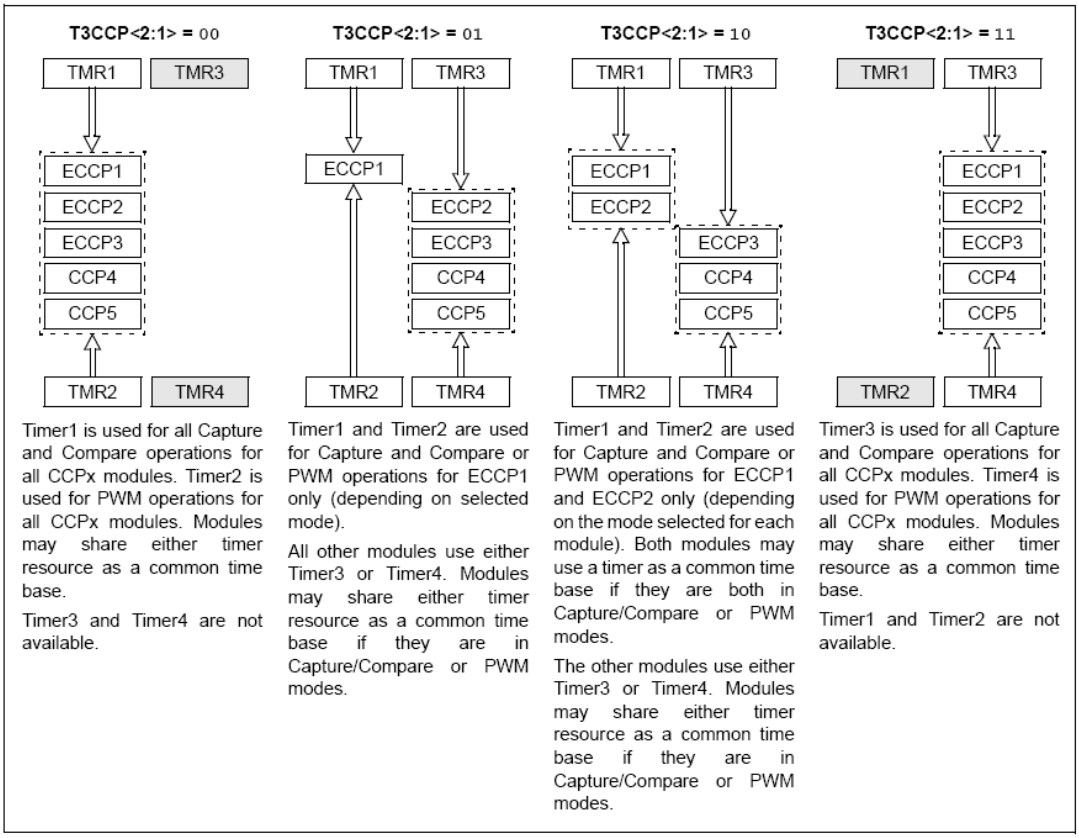
The assignment of a particular timer to a module is determined by the timer to CCPx enable bits in the T3CON register (Register 14-1, page 179). Depending on the configuration selected, up to four timers may be active at once, with modules in the same configuration (Capture/Compare or PWM) sharing timer resources. The possible configurations are shown in Figure 16-1.

16.1.2 ECCP2 PIN ASSIGNMENT

The pin assignment for ECCP2 (Capture input, Compare and PWM output) can change based on device configuration. The CCP2MX Configuration bit determines which pin ECCP2 is multiplexed to. By default, it is assigned to RC1 (CCP2MX = 1). If the Configuration bit is cleared, ECCP2 is multiplexed with RE7 on 80-pin and 100-pin devices in Microcontroller mode and RB3 on 100-pin devices in Extended Microcontroller mode.

Changing the pin assignment of ECCP2 does not automatically change any requirements for configuring the port pin. Users must always verify that the appropriate TRIS register is configured correctly for ECCP2 operation regardless of where it is located.

FIGURE 16-1: CCPx/ECCPx AND TIMER INTERCONNECT CONFIGURATIONS



Timer1 is used for all Capture and Compare operations for all CCPx modules. Timer2 is used for PWM operations for all CCPx modules. Modules may share either timer resource as a common time base.

Timer3 and Timer4 are not available.

Timer1 and Timer2 are used for Capture and Compare or PWM operations for ECCP1 only (depending on selected mode).

All other modules use either Timer3 or Timer4. Modules may share either timer resource as a common time base if they are in Capture/Compare or PWM modes.

Timer1 and Timer2 are used for Capture and Compare or PWM operations for ECCP1 and ECCP2 only (depending on the mode selected for each module). Both modules may use a timer as a common time base if they are both in Capture/Compare or PWM modes.

The other modules use either Timer3 or Timer4. Modules may share either timer resource as a common time base if they are in Capture/Compare or PWM modes.

Timer3 is used for all Capture and Compare operations for all CCPx modules. Timer4 is used for PWM operations for all CCPx modules. Modules may share either timer resource as a common time base.

Timer1 and Timer2 are not available.

16.4 PWM Mode

In Pulse-Width Modulation (PWM) mode, the CCPx pin produces up to a 10-bit resolution PWM output. Since the CCP4 and CCP5 pins are multiplexed with a PORTG data latch, the appropriate TRISG bit must be cleared to make the CCP4 or CCP5 pin an output.

Note:	Clearing the CCP4CON or CCP5CON register will force the RG3 or RG4 output latch (depending on device configuration) to the default low level. This is not the PORTG I/O data latch.

Figure 16-4 shows a simplified block diagram of the CCPx module in PWM mode.

For a step-by-step procedure on how to set up a CCPx module for PWM operation, see **Section 16.4.3 "Setup for PWM Operation"**.

16.4.1 PWM PERIOD

The PWM period is specified by writing to the PR2 (PR4) register. The PWM period can be calculated using Equation 16-1:

EQUATION 16-1:

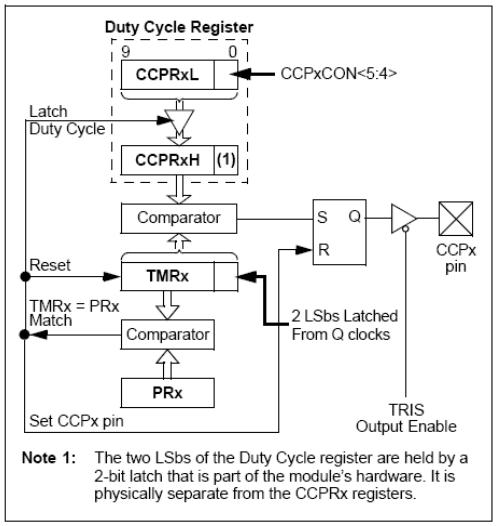
$$\text{PWM Period} = [(\text{PR2}) + 1] \cdot 4 \cdot \text{Tosc} \cdot (\text{TMR2 Prescale Value})$$

PWM frequency is defined as 1/[PWM period].

When TMR2 (TMR4) is equal to PR2 (PR4), the following three events occur on the next increment cycle:

- TMR2 (TMR4) is cleared
- The CCPx pin is set (exception: if PWM duty cycle = 0%, the CCPx pin will not be set)

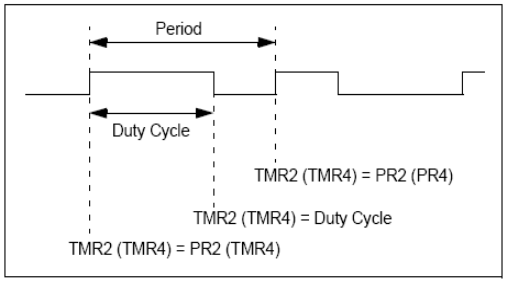
FIGURE 16-4: SIMPLIFIED PWM BLOCK DIAGRAM



Note 1: The two LSbs of the Duty Cycle register are held by a 2-bit latch that is part of the module's hardware. It is physically separate from the CCPRx registers.

A PWM output (Figure 16-5) has a time base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 16-5: PWM OUTPUT



- The PWM duty cycle is latched from CCPRxL into CCPRxH

Note: The Timer2 and Timer4 postscalers (see **Section 13.0 "Timer2 Module"** and **Section 15.0 "Timer4 Module"**) are not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

16.4.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPRxL register and to the CCPxCON<5:4> bits. Up to 10-bit resolution is available. The CCPRxL contains the eight MSbs and the CCPxCON<5:4> contains the two LSbs. This 10-bit value is represented by CCPRxL:CCPxCON<5:4>. Equation 16-2 is used to calculate the PWM duty cycle in time.

EQUATION 16-2:

$$\text{PWM Duty Cycle} = (\text{CCPRxL:CCPxCON<5:4>}) \bullet T_{OSC} \bullet (\text{TMRx Prescale Value})$$

CCPRxL and CCPxCON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPRxH until after a match between PR2 (PR4) and TMR2 (TMR4) occurs (i.e., the period is complete). In

PWM mode, CCPRxH is a read-only register.

The CCPRxH register and a 2-bit internal latch are used to double-buffer the PWM duty cycle. This double-buffering is essential for glitchless PWM operation.

When the CCPRxH and 2-bit latch match TMR2 (TMR4), concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 (TMR4) prescaler, the CCPx pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by Equation 16-3:

EQUATION 16-3:

$$\text{PWM Resolution (max)} = \frac{\log\left(\frac{FOSC}{FPWM}\right)}{\log(2)} \text{ bits}$$

Note:	If the PWM duty cycle value is longer than the PWM period, the CCPx pin will not be cleared.

16.4.3 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCPx module for PWM operation:

1. Set the PWM period by writing to the PR2 (PR4) register.
2. Set the PWM duty cycle by writing to the CCPRxL register and CCPxCON<5:4> bits.
3. Make the CCPx pin an output by clearing the appropriate TRIS bit.
4. Set the TMR2 (TMR4) prescale value, then enable Timer2 (Timer4) by writing to T2CON (T4CON).
5. Configure the CCPx module for PWM operation.

TABLE 16-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 40 MHz

PWM Frequency	2.44 kHz	9.77 kHz	39.06 kHz	156.25 kHz	312.50 kHz	416.67 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	FFh	FFh	FFh	3Fh	1Fh	17h
Maximum Resolution (bits)	10	10	10	8	7	6.58

TABLE 16-4: REGISTERS ASSOCIATED WITH PWM, TIMER2 AND TIMER4

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset Values on Page:
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	63
RCON	IPEN	—	$\overline{CM}$	$\overline{RI}$	$\overline{TO}$	$\overline{PD}$	$\overline{POR}$	$\overline{BOR}$	64
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSP1IF	CCP1IF	TMR2IF	TMR1IF	65
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSP1IE	CCP1IE	TMR2IE	TMR1IE	65
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSP1IP	CCP1IP	TMR2IP	TMR1IP	65
PIR3	SSP2IF	BCL2IF	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	65
PIE3	SSP2IE	BCL2IE	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	65
IPR3	SSP2IP	BCL2IP	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	65
TRISG	TRISG7	TRISG6	TRISG5	TRISG4	TRISG3(1)	TRISG2	TRISG1	TRISG0	65
TMR2	Timer2 Register								64
PR2	Timer2 Period Register								64
T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	64
TMR4	Timer4 Register								66
PR4	Timer4 Period Register								66
T4CON	—	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0	66
CCPR4L	Capture/Compare/PWM Register 4 Low Byte								66
CCPR4H	Capture/Compare/PWM Register 4 High Byte								66
CCPR5L	Capture/Compare/PWM Register 5 Low Byte								67
CCPR5H	Capture/Compare/PWM Register 5 High Byte								67
CCP4CON	—	—	DC4B1	DC4B0	CCP4M3	CCP4M2	CCP4M1	CCP4M0	67
CCP5CON	—	—	DC5B1	DC5B0	CCP5M3	CCP5M2	CCP5M1	CCP5M0	67

Legend: — = unimplemented, read as '0'. Shaded cells are not used by PWM, Timer2 or Timer4.

Note 1: This bit is only available in 80-pin and 100-pin devices; otherwise, it is unimplemented and reads as '0'.

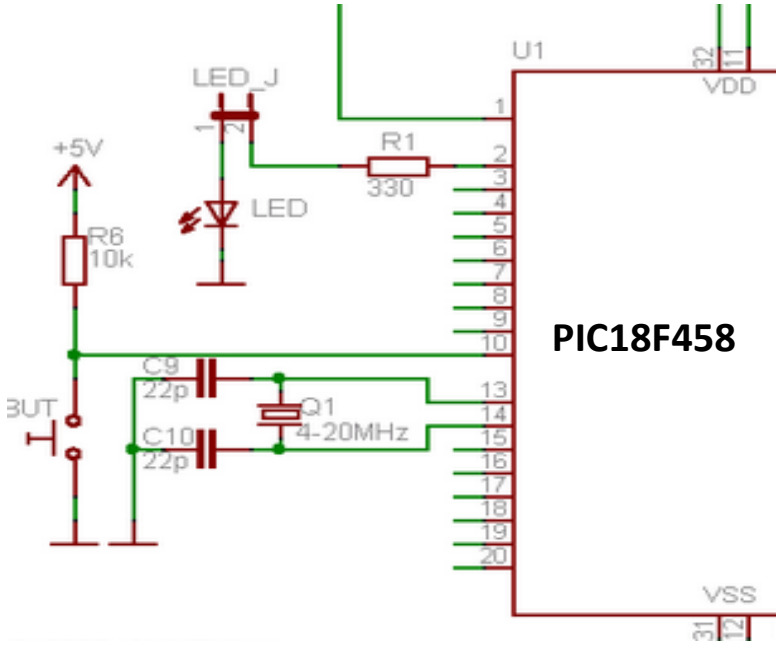
Exercise:

1. Connect an LED to the output pin of the CCP module on your PIC-P40 board. Be sure to use a current limiting resistor in series with the LED (see the PIC-P40 schematic at the end of this lab for specifications on the size of the current limiting resistor and for proper wiring of the LED). Using Timer 2 and the CCP module of the output pin you connected the LED to, write a program to monitor the status of the PIC-P40 onboard button and perform the following: if the button is pressed, the LED will be illuminated using a PWM waveform with a 5% DC. If the button is not pressed, the LED will be illuminated using a PWM waveform with a 95% DC.

   Use the MPLAB simulator to verify the proper operation of the program ***before*** programming the PIC-P40. Use the Stimulus feature of MPLAB SIM to simulate the button.

   Demonstrate the proper operation of the program to the instructor and submit a hardcopy of your program code and screen shots of the working simulation. Be sure to include the calculations you did to determine the CCP and PR register values. Use a value of 20 kHz for Fpwm.

PIC-P40 SCHEMATIC



PIN DIAGRAM – PDIP (Plastic Dual In-line Package)