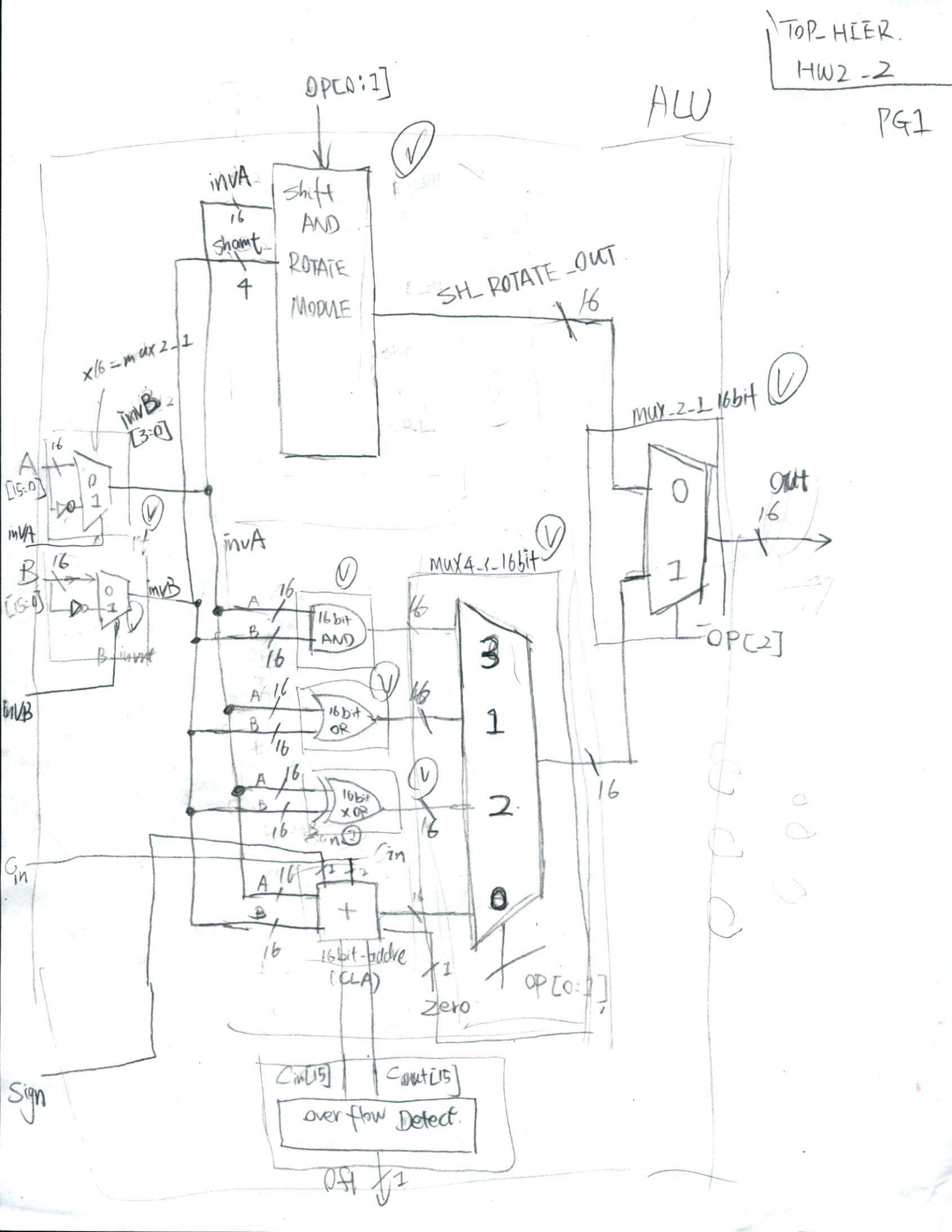
TOP_HIER.
HW2_2

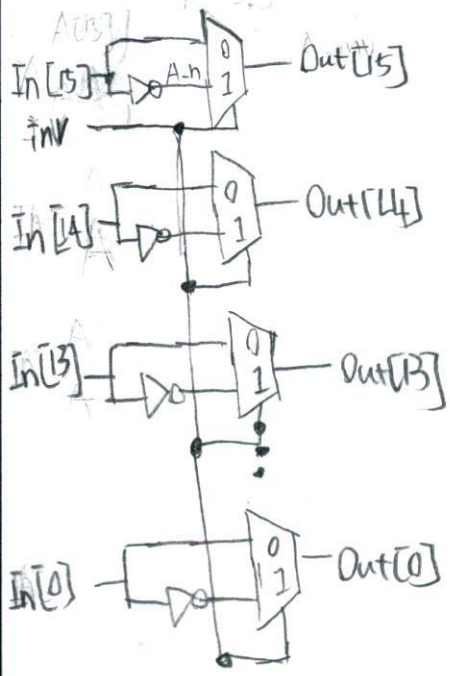
PG1



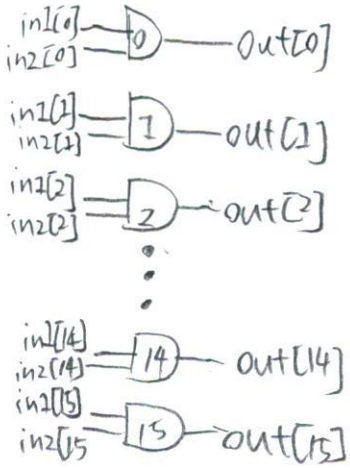
HW2_2

PG 1

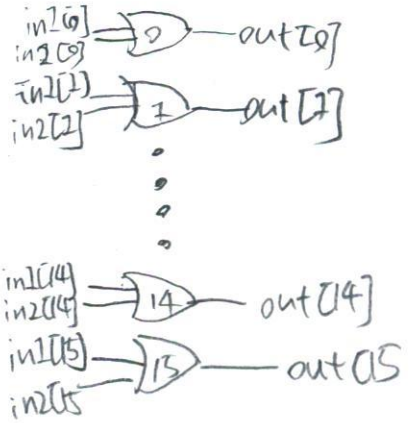
inverter_16bit.V ✓



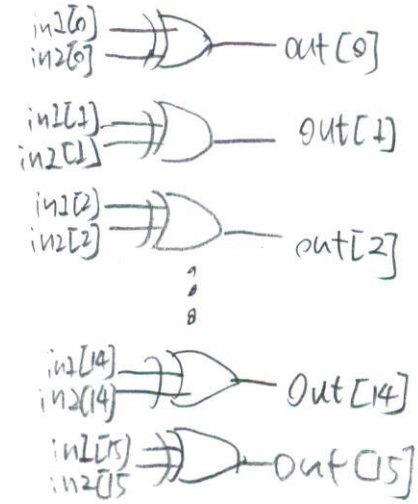
and2_16bit.V ✓



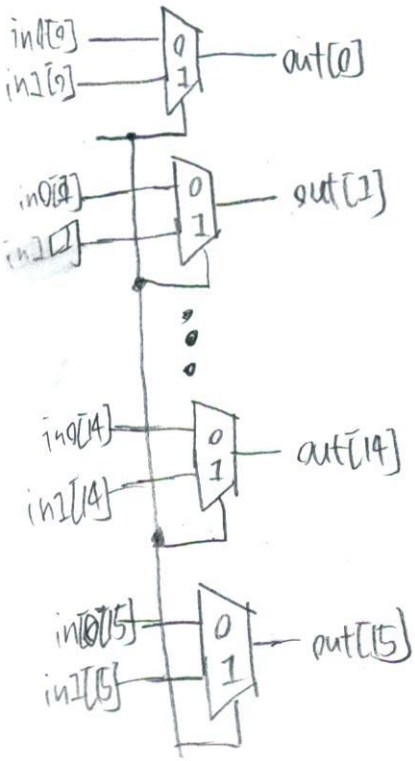
or2_16bit.V ✓



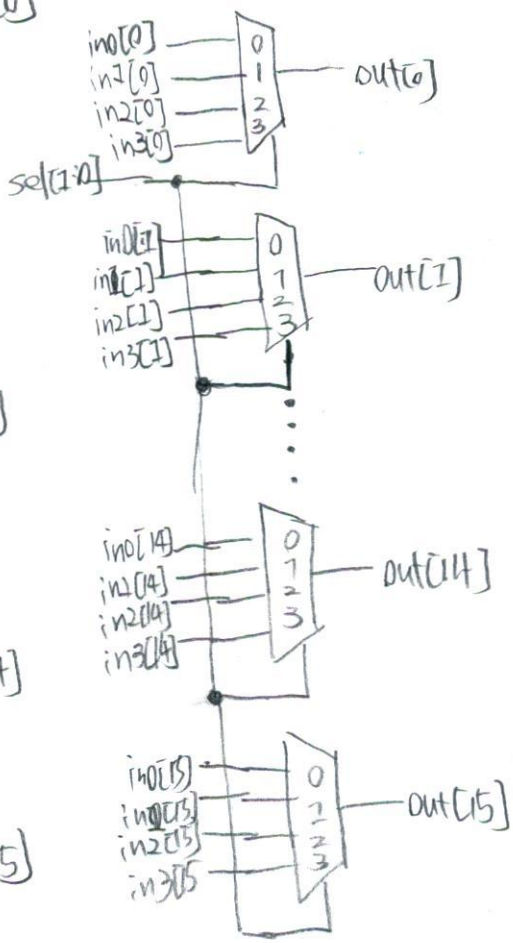
xor2_16bit.V ✓



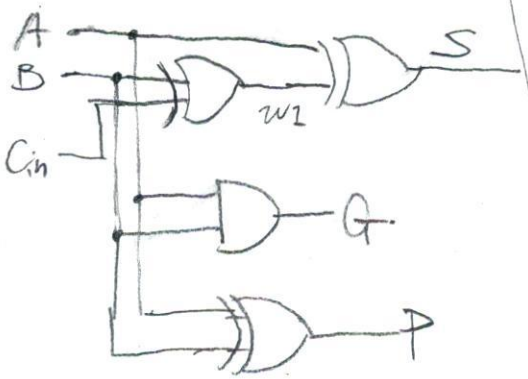
mux2_1_16bit.V



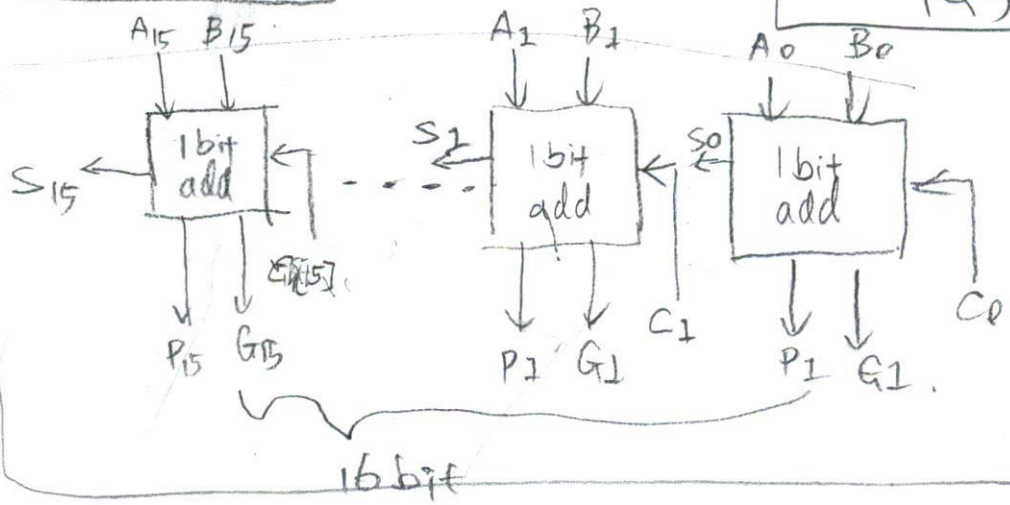
mux4_1_16bit.V



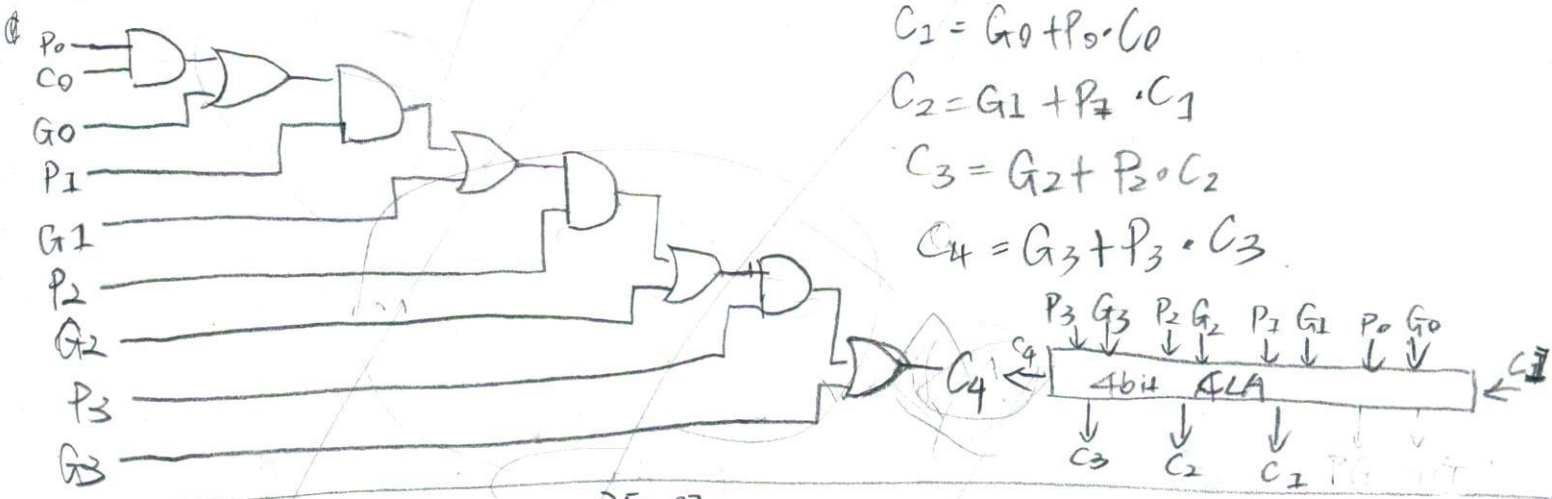
fulladder.v



16bit_fulladden.v



CLU_4bit.v



$C_1 = G_0 + P_0 \cdot C_0$

$C_2 = G_1 + P_1 \cdot C_1$

$C_3 = G_2 + P_2 \cdot C_2$

$C_4 = G_3 + P_3 \cdot C_3$

CLU_16bit.V