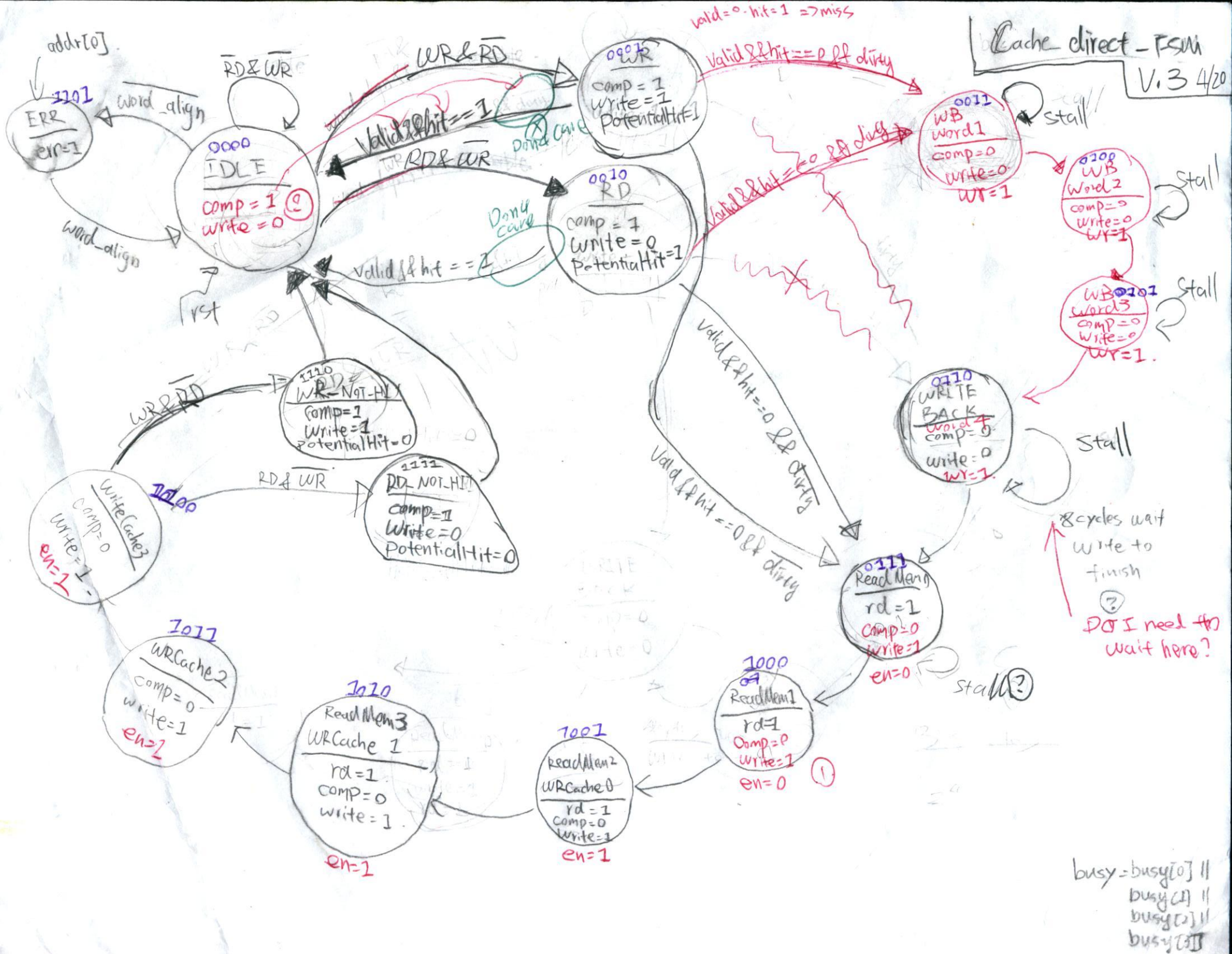
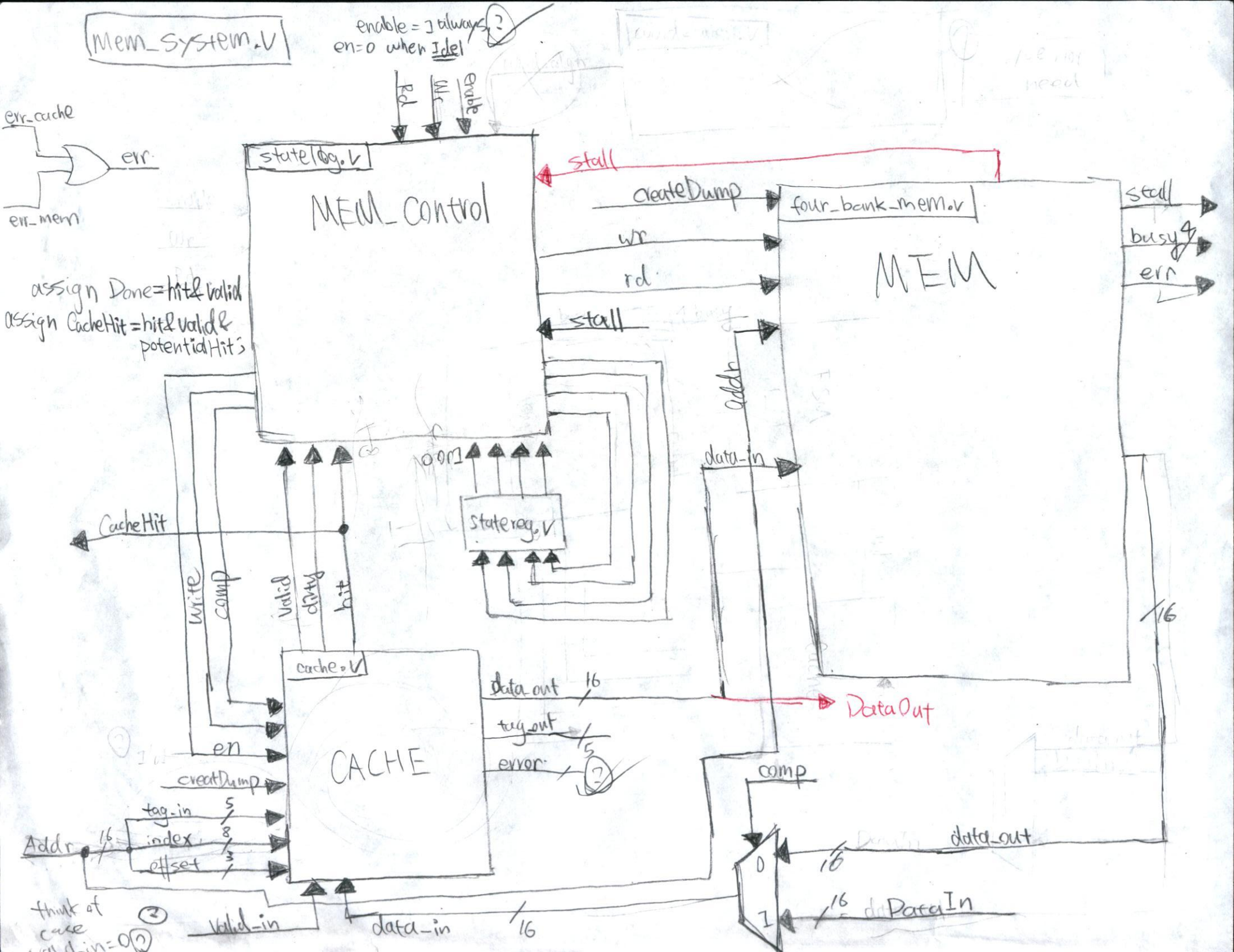

Cache direct - FSM
V.3 4/20
addr[0]
1101
ERR
err=1
word_align
RD&WR
0000
IDLE
comp=1
write=0
WR&RD
Valid&&hit==1
Dont care
0001
WR
comp=1
write=1
PotentialHit=1
Valid&&hit==0 && dirty
valid=0 hit=1 =>miss
0010
RD
comp=1
write=0
PotentialHit=1
Valid&&hit==1
rst
0011
WB
word1
comp=0
write=0
WR=1
stall
0100
WB
word2
comp=0
write=0
WR=1
0101
WB
word3
comp=0
write=0
WR=1.
0110
WRITE
BACK
comp=0
write=0
WR=1.
Valid&&hit==0 && dirty
1110
WR_NOT_HIT
comp=1
write=1
PotentialHit=0
1111
RD_NOT_HIT
comp=1
write=0
PotentialHit=0
1000
WriteCache3
comp=0
write=1
en=1
1011
WRCache2
comp=0
write=1
en=1
1010
ReadMem3
WRCache 1
rd=1
comp=0
write=1
en=1
1001
ReadMem2
WRCache0
rd=1
comp=0
write=1
en=1
0111
ReadMem
rd=1
comp=0
write=1
en=0
stall
1000
ReadMem1
rd=1
comp=0
write=1
en=0
8cycles wait write to finish
DO I need to wait here?
busy=busy[0] || busy[1] || busy[2] || busy[3]


Mem_System.v
enable = 1 always ?
en=0 when Idel
rd
wr
enable
err_cache
err
err_mem
stateReg.v
MEM_Control
stall
createDump
four_bank_mem.v
MEM
wr
rd
stall
stall
busy
err
assign Done=hit& valid
assign CacheHit=hit& valid& potentialHit;
addr
data_in
com
stateReg.v
CacheHit
write
comp
valid
dirty
hit
cache.v
CACHE
data_out 16
tag_out 5
error
DataOut
en
creatDump
tag_in 5
index 8
offset 3
Addr 16
think of case wr_in=0 ?
Valid_in
data_in 16
comp
data_out
16
DataIn
16
0
1

RD_MEM0

rd = 1

mem_offset = 00

RD_MEM1

rd = 1

mem_offset = 01

WD_cache0

RD_MEM2

rd = 1

mem_offset = 10

comp = 0

write = 1

cache_offset = 00

WD_cache1

RD_MEM3

rd = 1

mem_offset = 11

comp = 0

write = 1

cache_offset = 01

WD_cache2

comp = 0

write = 1

cache_offset = 10

WD_cache3

comp = 0

write = 1

cache_offset = 11

RD MEM mem_offset, Addr[0]

Addr[0:3]

BUG

Mem_addr

assign mem_addr = (comp == 1) ? Addr : (comp == 0 && write == 0) ? {Addr[0:3], tag_out, mem_offset, Addr[0]}

assign cache_addr = {Addr[0:3], cache_offset, Addr[0]}

tag_out

comp = 0, write = 0

WB_W1

comp = 0

write = 0

wr = 1

cache_offset = 00

mem_offset = 00

WB_W2

comp = 0

write = 0

wr = 1

cache_offset = 01

mem_offset = 01