HW3_3

State diagram (top):

- State 0: FIFO_EMPTY = 1
- State 1: FIFO NOT FULL = 1
- State 2: FIFO FULL = 1

Transitions: data_in, data_in & count==4, POP, ~POP, POP & count<4

fifo_out. V

decoder 2x4.V

data_in & count<4

R W — Push 2, Pop

read_ptr = 0
write_ptr = 0
count = 0

sel
2
64
in0
64
in1
64
in2
64
in3
64

64

mux4_1_64bit.V

data_in

data_in & valid

fifo_full

2
write_ptr

2-4 decoder

64 64 64bit
64
1
CLK

read_ptr
2

data_out
64

reg_64bit.V

data_in
64
in[0]
16
out[0]
16
data out
64

in[1]
16
out[1]

en

in[2]
16
out[2]

in[3]
16
out[3]

rst

CLK