Address (HEX)	Register Operation	
	Write	Read
$D1E0	Set address A15-A8 for $D600 RAM window. (LSB of sector number.)	Set RST- signal true (low). Resets the SCSI/SASI bus. (RST- also true during RESET)
$D1E1	Set printer data and SCSI/SASI data. True logic for printer — Inverted for SCSI/SASI bus.	Read data from SCSI/SASI bus. Data is inverted.
$D1E2	General purpose outputs. B[3..0] High RAM address, sets address A19-A16. B[4] 1 = Set SEL- true B[5] 1 = Enable RAM access B[6] 1 = Set STROBE- true B[7] 1 = Enable Parallel IRQ	General purpose inputs. B[0] = SASI C/D- B[1] = SASI MSG- B[2] = SASI I/O- B[4] = Printer FAULT- B[5] = SASI BUSY- B[6] = Printer BUSY B[7] = SASI REQ- Also clears RST- signal
$D1E3 or $D1FF	Set ROM enable and bank. Only 1 bit allowed set at a time. B[2] 1 = Disk Interface ROM B[3] 1 = Seg 2 of setup MENU B[4] 1 = R:/P: Handler ROM B[5] 1 = Seg 1 of setup MENU B[7..6] High RAM address, set address A21-A20 All bits 0 disable the ROM.	IRQ sense bits + Misc inputs. B[0] = RS-232 DCD line B[1] = RS-232 DSR line B[2] = RS-232 CTS line B[3] = Printer BUSY- IRQ B[4] = MIO IRQ (from 6551 or Printer BUSY- IRQ)
$D1C0	Write ACIA transmit register.	Read ACIA receive register.
$D1C1	Perform a programmed RESET on ACIA (data is "don't care").	Read Status register (resets IRQ). B[0] 1 = Parity error B[1] 1 = Framing error B[2] 1 = Overrun has occurred B[3] 1 = Receiver reg. full B[4] 1 = Transmitter empty B[7] 1 = IRQ occurred
$D1C2	Write ACIA command register.	Read ACIA command register.
$D1C3	Write ACIA control register.	Read ACIA control register.
$D6xx	Write RAM. High address A21-A8 selected by $D1E0/$D1E2/$D1E3	Read RAM. High address A21-A8 selected by $D1E0/D1E2/$D1E3.

Addressing the RAM

The MIO standard board can access up to 1 Megabyte of RAM which takes 20 bits to address. Address bits A19-A16 are set from writing to the latch at $D1E2, bits A15-A8 are set from writing to the latch at $D1E0, and bits A7-A0 are CPU address lines A7-A0 when reading/writing $D6xx. Thus there are up to 4096 "pages" of memory that may appear at the $D6xx window.
*The **DUO MIO** board add two extra bits for addressing up to 4 Megabyte of RAM which takes 22 bits to address (A20-A21). Those extra bits are at $D1E3 or $D1FF, bits 6/7.*
In order to access the memory, it must first be enabled by setting $D1E2 bit 5 to "1" (this also turns on the MIO's red LED and the DUO MIO's amber LED). It is generally a good idea to leave the RAM disabled while not using it in
case of a system crash (which could inadvertently write in the $D6xx window).