

Sheet: VeraModule

VERA FPGA

File: vera-fpga.sch

Sheet: BusDecoder

BUS DECODER

File: busdecoder.sch

Sheet: Vera FPGA flash

VERA SPI FLASH SD CARD INTERFACE

File: vera-fpga-flash.sch

Sheet: CartridgeInterface

CARTRIDGE INTERFACE

File: cartridgeInterface.sch

Sheet: PowerSupply

POWER SUPPLY

File: powersupply.sch

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Sheet: /
File: VERA-MODULE-RBL.sch

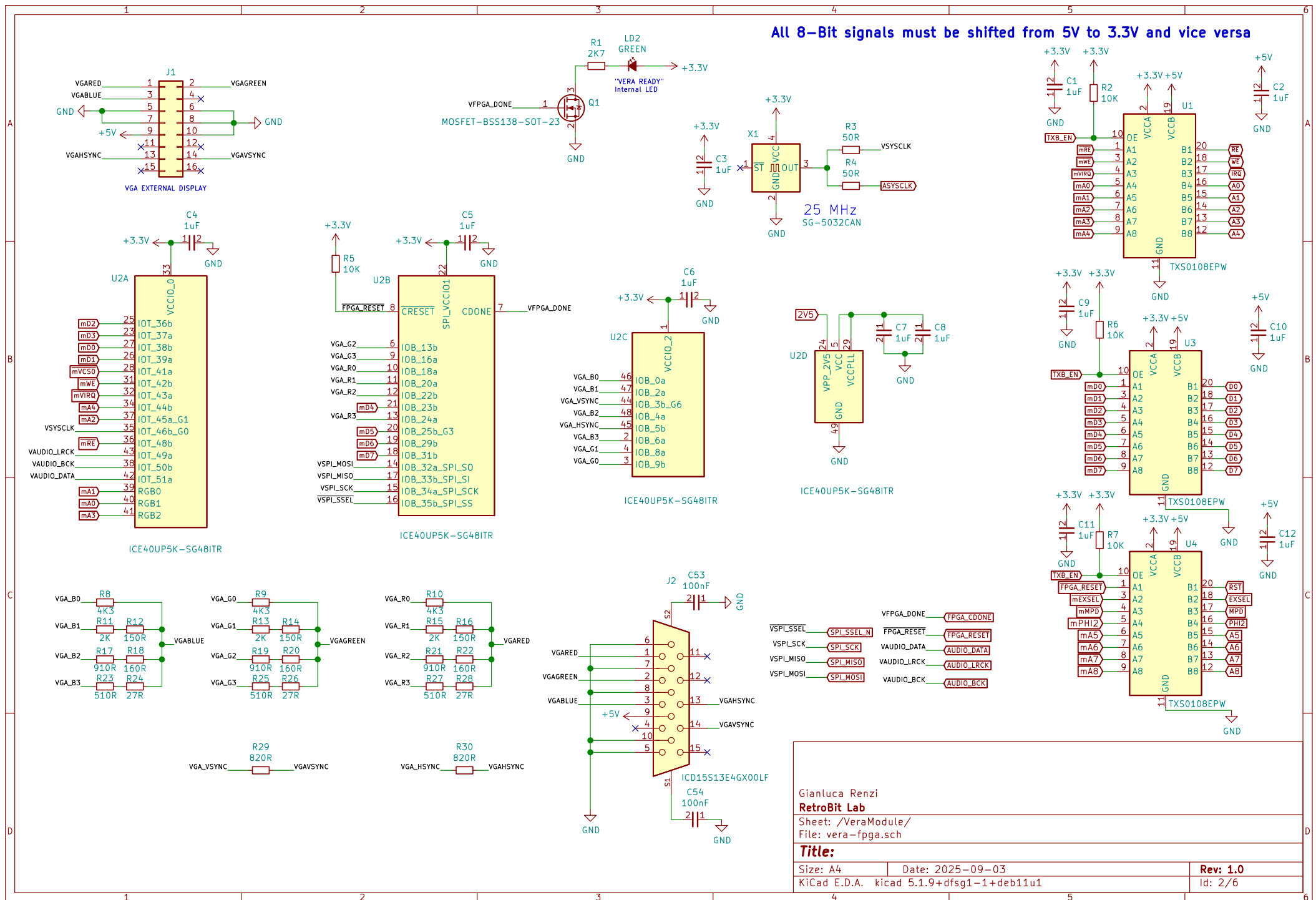
Title: VERA FPGA Audio & Video Board

Size: A4 Date: 2025-09-03

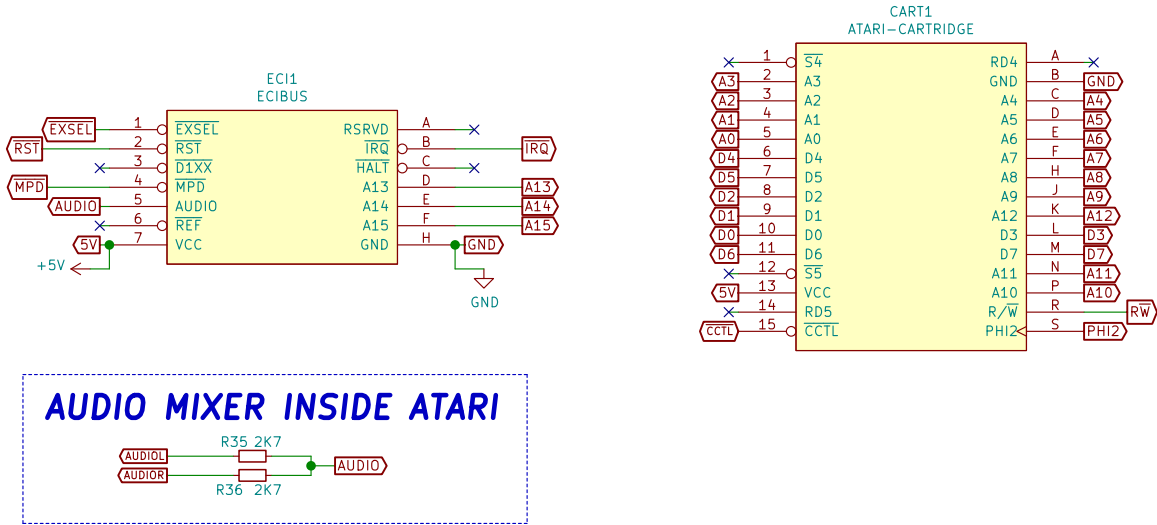
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1

Rev: 1.0

Id: 1/6



ATARI 130XE ECI & CARTRIDGE INTERFACE



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Sheet: /CartridgeInterface/
File: cartridgeInterface.sch

Title:

Size: A4

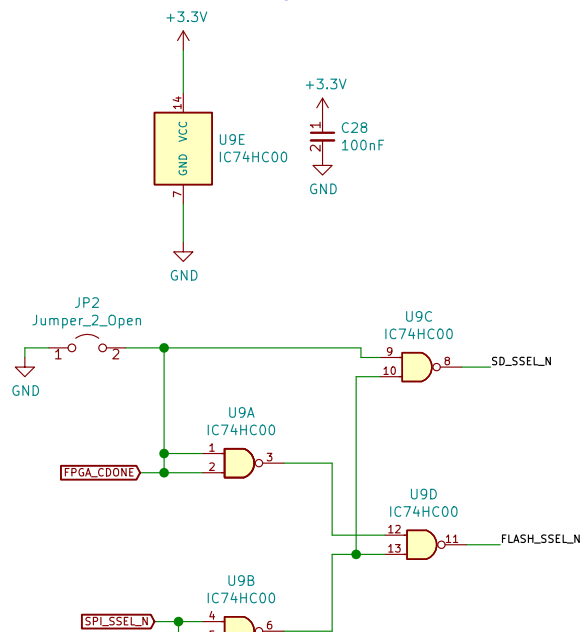
Date: 2025-09-03

Rev: 1.0

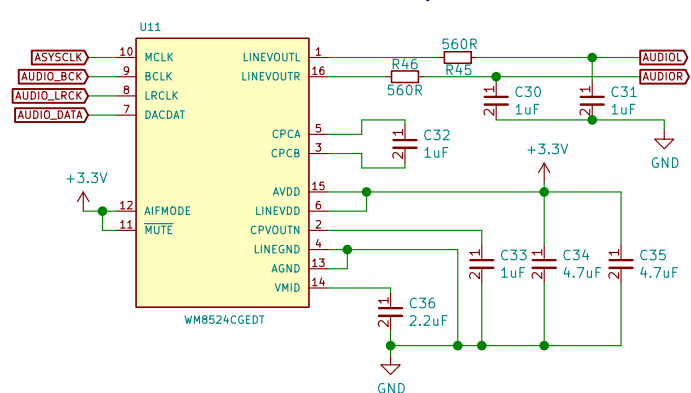
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1

Id: 4/6

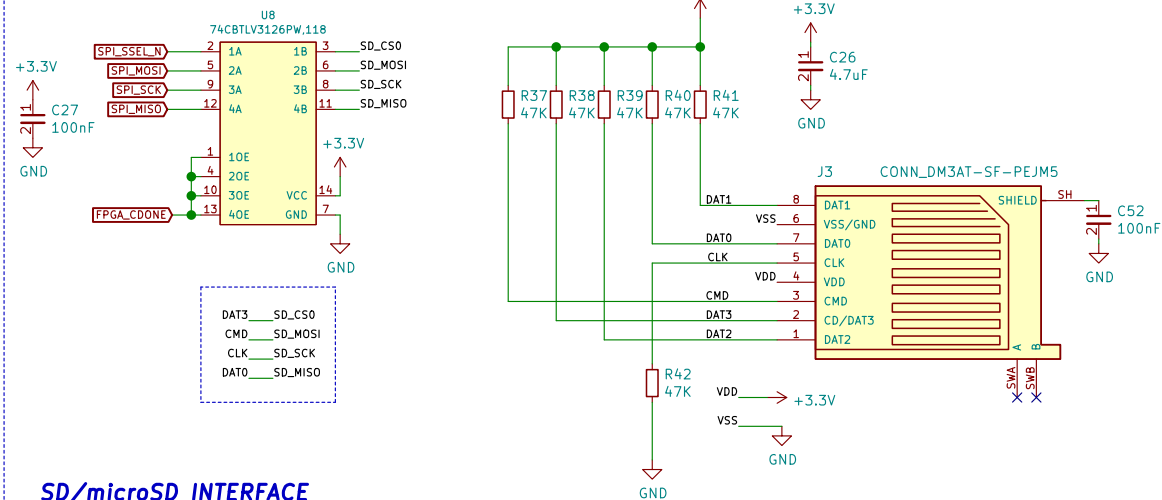
FPGA/SSD Flash Glue Logic



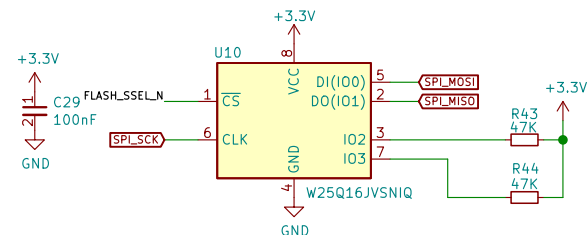
IC DAC/AUDIO 24BIT 192K 16TSSOP



SD/microSD INTERFACE



SPI 16MB FLASH



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Sheet: /Vera FPGA flash/

File: vera-fpga-flash.sch

Title:

Size: A4

Date: 2025-09-03

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Rev: 1.0

Id: 5/6

USB ESP32 PROGRAMMING

When programming ESP32, all level shifters must be DISABLED

POWER INPUT: from 5VDC...24VDC Positive CENTRAL PIN

POWER 3.3V & POWER 2.5V

POWER LED
5V: RED
3.3V: GREEN

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RetroBit Lab
Sheet: /PowerSupply/
File: powersupply.sch
Title:
Size: A4 Date: 2025-09-03
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1
Rev: 1.0
Id: 6/6

When programmig ESP32,
all level shifters must be
DISABLED

POWER INPUT: from 5VDC...24VDC
Positive CENTRAL PIN

PJ-002AH-SMT-TR

U15
L7805

CREZ12061%
R56

+5V

5V

10uF-35V
C47

10uF-20V
C48

100nF
C49

1A
J5

GND

The image shows two circuit diagrams for AMS1117 voltage regulators. The left diagram is for the AMS1117-3.3, which takes a +5V input and provides a +3.3V output. It includes a 100nF input capacitor (C44), a 10uF-20V output capacitor (C45), and a 100nF bypass capacitor (C46). The right diagram is for the AMS1117-2.5, which takes a +5V input and provides a +2.5V output. It includes a 100nF input capacitor (C50), a 10uF-20V output capacitor (C51), and a 1uF bypass capacitor (C43). Both regulators are shown in a yellow box with pins labeled VI, V0, and GND.

Sheet: /PowerSupply/
File: powersupply.sch

Size: A4	Date: 2025-09-03
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Rev: 1.0
Id: 6/6