

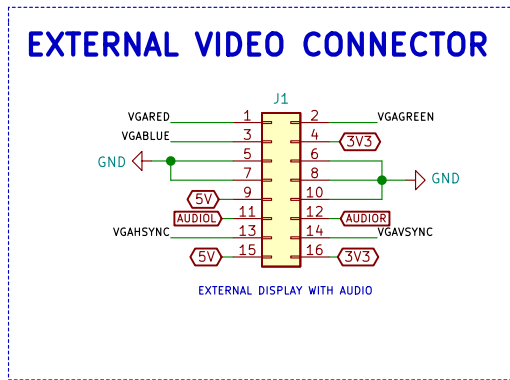
EXTERNAL VIDEO CONNECTOR

The diagram illustrates the pin configuration for an external video connector, labeled J1. The connector has 16 pins arranged in two rows of 8. The connections are as follows:

- Pin 1:** VGARED
- Pin 2:** VGAGREEN
- Pin 3:** VGBLUE
- Pin 4:** 3V3 (Power)
- Pin 5:** GND
- Pin 6:** 3V3 (Power)
- Pin 7:** GND
- Pin 8:** 3V3 (Power)
- Pin 9:** 5V (Power)
- Pin 10:** 5V (Power)
- Pin 11:** AUDIOL (Audio Left)
- Pin 12:** AUDIOR (Audio Right)
- Pin 13:** 5V (Power)
- Pin 14:** 5V (Power)
- Pin 15:** 5V (Power)
- Pin 16:** 3V3 (Power)

Additional labels include VGAREDB, VGBLUEB, and VGBLUEC, which are not connected to any pins. The diagram also shows a GND symbol on the left and a 3V3 symbol on the right, indicating the power and ground connections for the connector.

EXTERNAL DISPLAY WITH AUDIO



FPGA VERA LOGIC VIDEO & AUDIO CARD

The image displays four circuit diagrams for an FPGA VERA Logic Video & Audio Card, each featuring an ICE40UP5K-SG48ITR chip.

Diagram U2A: Shows the chip connected to a 3V3 power supply (C4, 1uF) and GND. The chip is labeled U2A. The VCCIO_0 pin is connected to the 3V3 supply. The chip is connected to various I/O pins (mB2, mB3, mB0, mB1, mVC50, mWE, mVIRQ, mA4, mA2, mA1, mA0, mA3) and a VSYCLK pin. The chip is labeled ICE40UP5K-SG48ITR.

Diagram U2B: Shows the chip connected to a 3V3 power supply (C5, 1uF) and GND. The chip is labeled U2B. The VCCIO1 pin is connected to the 3V3 supply. The chip is connected to various I/O pins (mB2, mB3, mB0, mB1, mVC50, mWE, mVIRQ, mA4, mA2, mA1, mA0, mA3) and a VSYCLK pin. The chip is labeled ICE40UP5K-SG48ITR.

Diagram U2C: Shows the chip connected to a 3V3 power supply (C6, 1uF) and GND. The chip is labeled U2C. The VCCIO_2 pin is connected to the 3V3 supply. The chip is connected to various I/O pins (mB2, mB3, mB0, mB1, mVC50, mWE, mVIRQ, mA4, mA2, mA1, mA0, mA3) and a VSYCLK pin. The chip is labeled ICE40UP5K-SG48ITR.

Diagram U2D: Shows the chip connected to a 3V3 power supply (C59, 1uF) and GND. The chip is labeled U2D. The VCCIO_2 pin is connected to the 3V3 supply. The chip is connected to various I/O pins (mB2, mB3, mB0, mB1, mVC50, mWE, mVIRQ, mA4, mA2, mA1, mA0, mA3) and a VSYCLK pin. The chip is labeled ICE40UP5K-SG48ITR.

ANALOG VGA SIGNALS

The diagram illustrates the analog VGA signal output stage. It features three resistor networks for the color channels (Red, Green, Blue) and two for the sync and blue/white signals. The color channels are connected to the DAC's outputs 11, 12, and 13. The sync and blue/white signals are connected to outputs 14 and 15. The DAC is a DS1038-15FBNSiA74-0CC. The circuit includes a 5V supply and two 100nF capacitors (C53, C54) connected to ground.

Color Channel Resistor Networks:

- Red (VGA_R0-VGA_R3):** R10 (4K3), R15 (2K), R21 (910R), R27 (510R) in series; R16 (150R), R22 (160R), R28 (27R) in parallel.
- Green (VGA_G0-VGA_G3):** R9 (4K3), R14 (2K), R19 (910R), R25 (510R) in series; R14 (150R), R20 (160R), R26 (27R) in parallel.
- Blue (VGA_B0-VGA_B3):** R8 (4K3), R11 (2K), R17 (910R), R23 (510R) in series; R12 (150R), R18 (160R), R24 (27R) in parallel.

Sync and Blue/White Resistor Networks:

- Sync (VGA_HS, VGA_VS):** R29 (820R) and R30 (820R) in series.
- Blue/White (VGA_BLUE, VGA_WHITE):** R29 (820R) and R30 (820R) in series.

Signal Connections:

- VGA_R0-VGA_R3 to DAC outputs 11, 12, 13.
- VGA_HS, VGA_VS to DAC outputs 14, 15.
- VGA_BLUE, VGA_WHITE to DAC outputs 14, 15.

Power and Timing:

- 5V supply connected to DAC output 9.
- Capacitors C53 and C54 (100nF) connected to ground.

Legend:

- VFPGA_DONE: FPGA_CDONE
- VSPIL_SSEL: SPIL_SSEL_N
- VSPIL_SCK: SPIL_SCK
- VSPIL_MISO: SPIL_MISO
- VSPIL_MOSI: SPIL_MOSI
- VFGA_RESET: FPGA_RESET
- VAUDIO_DATA: AUDIO_DATA
- VAUDIO_LRCK: AUDIO_LRCK
- VAUDIO_BCK: AUDIO_BCK

VERA FPGA PROGRAMMED OK

VERA FPGA PROGRAMMED OK

Circuit diagram showing the connection for the VERA_READY status indicator:

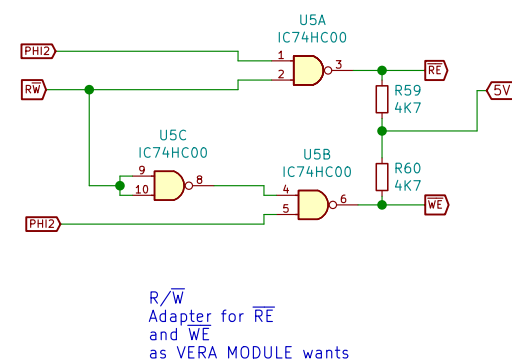
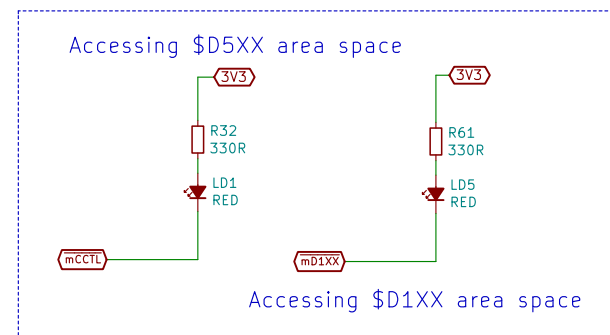
- VFGPA_DONE** (pin 1) is connected to the gate of the MOSFET **BSS138-SOT-23** (Q1).
- The MOSFET's source is connected to **GND**.
- The MOSFET's drain is connected to a resistor **R1 (2K7)** and the anode of the LED **LD2 (GREEN)**.
- The LED's cathode is connected to a **3V3** supply.
- The LED is labeled **"VERA_READY" Internal LED**.

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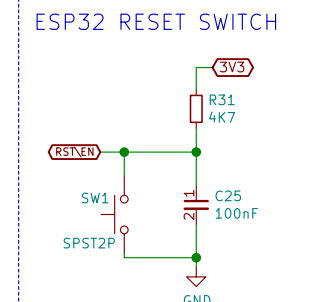
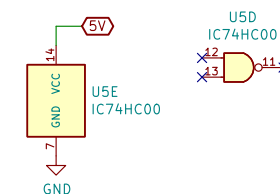
\$D1FF access & DATABUS = PBI DEVICE ID -> mVCS0 active/deactive

Those signals are valid in ATARI XE only

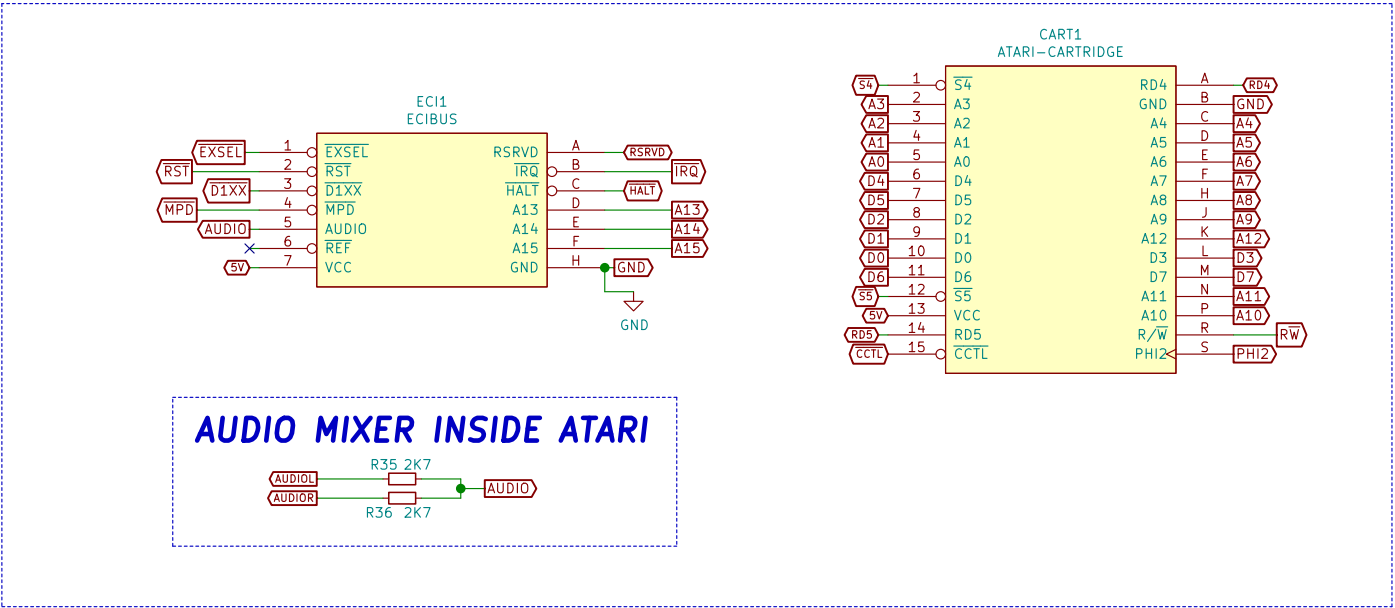


External Memory Setup:
The range must be defined in software
EXSEL

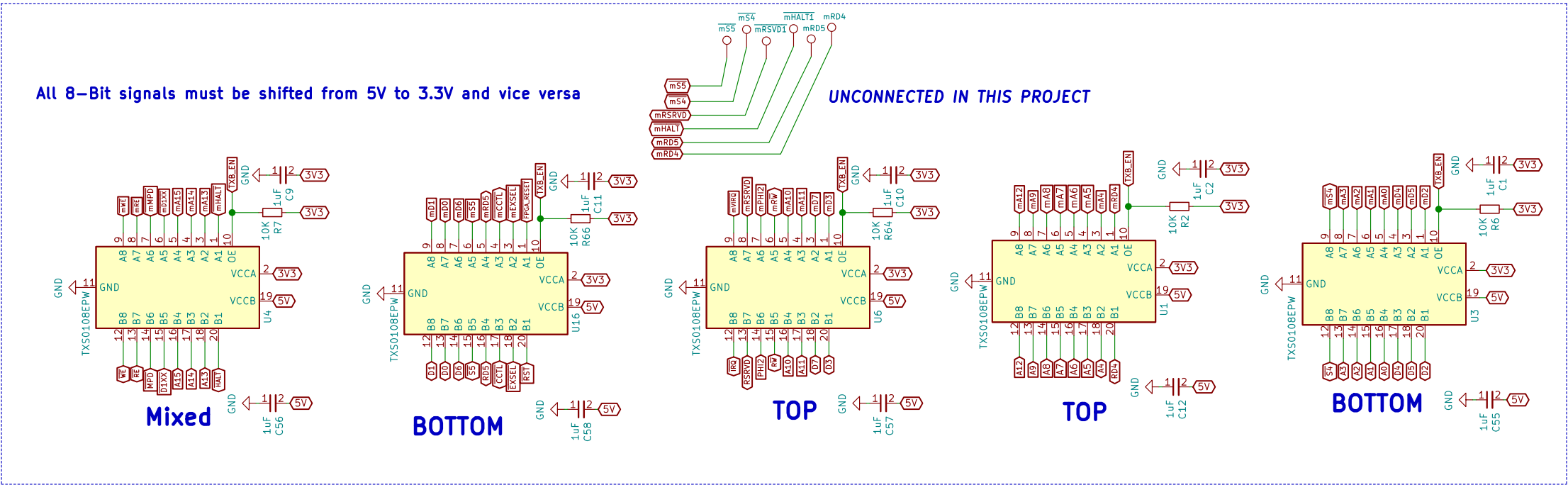
In PBI Atari XL there is EXTENB signal output and EXTSEL signal input
In PBI Atari XE there is only the EXSEL signal output



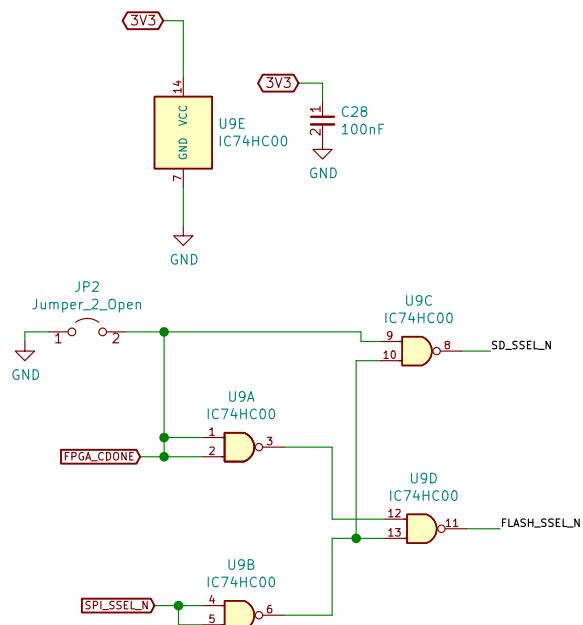
ATARI 130XE ECI & CARTRIDGE INTERFACE



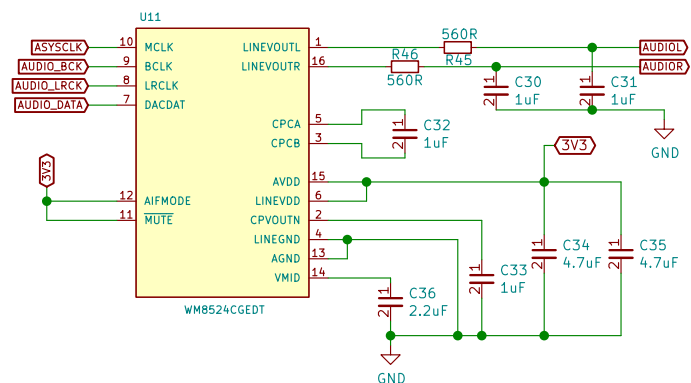
BUS LOGIC LEVEL SHIFTERS



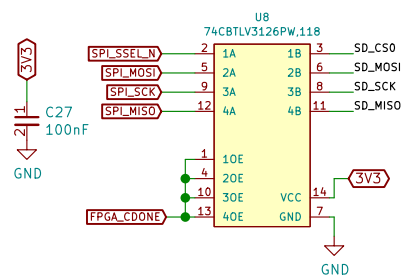
FPGA/SSD Flash Glue Logic



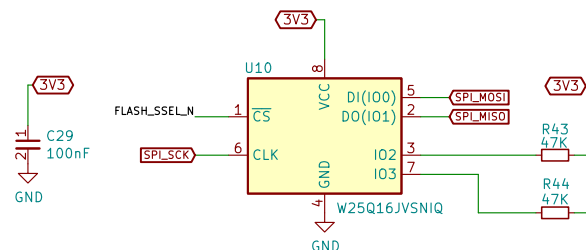
IC DAC/AUDIO 24BIT 192K 16TSSOP



SD/microSD INTERFACE



SPI 16MB FLASH



Gianluca Renzi

RetroBit Lab

Sheet: /Vera FPGA flash/

File: vera-fpga-flash.sch

Title: uSD Card and FLASH for FPGA

Size: A4 Date: 2025-09-12

KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1

Rev: 1.0

Id: 5/6

[illegible]

POWER INPUT: from 5VDC...24VDC
Positive CENTRAL PIN

PJ-002AH-SMT-TR

J5

1A

10uF-35V

C47

U15 L7805

IN OUT

10uF-20V

C48

100nF

C49

R56 0R

U17 MAX40200AUK

VDD OUT

EN

5V_USB

5V

TP5V

GND

POWER 3.3V & POWER 2.5V

The image displays two circuit diagrams for voltage regulation. The first diagram, labeled 'POWER 3.3V & POWER 2.5V', shows the 3.3V regulator (U13, AMS1117-3.3) connected to a 5V source. The input capacitor C44 (100nF) is connected to the input (VI) of the regulator. The output (VO) is connected to the output capacitor C45 (10uF-20V) and the 3V3 output. The second diagram shows the 2.5V regulator (U14, AMS1117-1.5) connected to a 5V source. The input capacitor C50 (100nF) is connected to the input (VI) of the regulator. The output (VO) is connected to the output capacitor C51 (10uF-20V) and the 1V5 output.

Rev: 1.0
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