

Sheet: VeraModule

VERA FPGA

File: vera-fpga.sch

Sheet: BusDecoder

BUS DECODER

File: busdecoder.sch

Sheet: Vera FPGA flash

VERA SPI FLASH
SD CARD INTERFACE

File: vera-fpga-flash.sch

Sheet: CartridgeInterface

CARTRIDGE INTERFACE

File: cartridgeInterface.sch

Sheet: PowerSupply

POWER SUPPLY

File: powersupply.sch

FIDUCIAL TOP

FID3
Fiducial

FID4
Fiducial

FIDUCIAL BOTTOM

FID2
Fiducial

FID1
Fiducial

LOG01
VERA X16 LOGO
LOG02
ATARI READY

LOG03
KICAD DESIGN
LOG04
ATARI DUO BUS

LOG05
ESP32_BOBOARD
LBL1

Gianluca Renzi
RetroBit Lab

Sheet: /
File: VERA-MODULE-RBL.sch

Title: VERA FPGA Audio & Video Board

Size: A3
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1

Date: 2025-09-23
Id: 1/6

Rev: 1.0

FPGA VERA LOGIC VIDEO & AUDIO CARD

The schematic diagram illustrates the internal connections of the FPGA VERA Logic Video & Audio Card. It features three primary components: two ICE40UP5K-SG48ITR FPGAs (U2A and U2B) and an ECS-2033-250-BN oscillator (X1).

U2A (ICE40UP5K-SG48ITR) Connections:

- VCCIO_0:** Connected to 3V3 via C4 (1uF) and GND.
- Inputs:** mB2, mB3, mB0, mB1, mVCS0, mWE, mA4, mA2, mRE, mA1, mA0, mA3.
- Outputs:** IOT_36b, IOT_37a, IOT_38b, IOT_39a, IOT_41a, IOT_42b, IOT_43a, IOT_44b, IOT_45a_G1, IOT_46b_G0, IOT_48b, IOT_49a, IOT_50b, IOT_51a, RGB0, RGB1, RGB2.
- Other:** VSYSCLK, VAUDIO_LRCK, VAUDIO_BCK, VAUDIO_DATA.

U2B (ICE40UP5K-SG48ITR) Connections:

- VCCIO1:** Connected to 3V3 via C5 (1uF) and GND.
- Inputs:** FPGA_RESET, VGA_G2, VGA_G3, VGA_R0, VGA_R1, VGA_R2, VGA_R3, mDB5, mDB6, mDB7.
- Outputs:** CRESET, CDONE, IOB_13b, IOB_16a, IOB_18a, IOB_20a, IOB_22b, IOB_23b, IOB_24a, IOB_25b_G3, IOB_29b, IOB_31b, IOB_32a_SPL_S0, IOB_33b_SPL_S1, IOB_34a_SPL_SCK, IOB_35b_SPL_SS.
- Other:** VSPL_MOSI, VSPL_MISO, VSPL_SCK, VSPL_SSEL.

X1 (ECS-2033-250-BN) Connections:

- VDD:** Connected to 3V3.
- GND:** Connected to GND.
- OUT:** Connected to VSYSCLK via R3 (50R) and R4 (50R).
- Frequency:** 25 MHz.

Legend:

- VFPGA_DONE → FPGA_CDONE
- VSPL_SSEL → SPL_SSEL_N
- VSPL_SCK → SPL_SCK
- VSPL_MISO → SPL_MISO
- VSPL_MOSI → SPL_MOSI
- FPGA_RESET → FPGA_RESET
- VAUDIO_DATA → AUDIO_DATA
- VAUDIO_LRCK → AUDIO_LRCK
- VAUDIO_BCK → AUDIO_BCK

ANALOG VGA SIGNALS

The diagram illustrates the analog VGA signal connections. It shows three resistor networks for the color channels (Red, Green, Blue) and two for the sync signals (Vsync and Hsync). The color channels are connected to a common bus (VGA_B0 to VGA_B3) and then to the respective color lines (VGARED, VGAGREEN, VGABLUE). The sync signals are connected to a common bus (VGA_G0 to VGA_G3) and then to the sync lines (VGA_VSYNC, VGA_HSYNC). The connector pinout for the DS1038-15FBNSIA74-0CC connector is shown, with pins 1 through 15 labeled. Pins 11, 12, 13, 14, and 15 are marked with an 'X' and are not connected. The connector is connected to a 5V supply and ground (GND) through capacitors C53 and C54 (100nF).

Color Channel Resistor Networks:

- Red Channel:** VGA_B0 (4K3, R8), VGA_B1 (2K, R11), VGA_B2 (910R, R17), VGA_B3 (510R, R23) connected to VGARED.
- Green Channel:** VGA_G0 (4K3, R9), VGA_G1 (2K, R13), VGA_G2 (910R, R19), VGA_G3 (510R, R25) connected to VGAGREEN.
- Blue Channel:** VGA_B0 (4K3, R12), VGA_B1 (150R, R14), VGA_B2 (160R, R18), VGA_B3 (27R, R24) connected to VGABLUE.

Sync Signal Resistor Networks:

- Vsync:** VGA_VSYNC (820R, R29) connected to VGAVSYNC.
- Hsync:** VGA_HSYNC (820R, R30) connected to VGAHSYNC.

Connector Pinout (DS1038-15FBNSIA74-0CC):

- Pins 1, 2, 3, 4, 5: VGARED, VGAGREEN, VGABLUE, 5V, GND.
- Pins 6, 7, 8, 9, 10: 11, 12, 13, 14, 15 (not connected).
- Pins 11, 12, 13, 14, 15: VGABLUE, VGAVSYNC, VGAHSYNC, VGARED, VGAGREEN.

VERA FPGA PROGRAMMED OK

VERA READY Internal LED

EXTERNAL VIDEO CONNECTOR

The diagram illustrates the pin configuration for the External Video Connector (J1). The connector has 16 pins, numbered 1 through 16. The connections are as follows:

- Pin 1:** VGARED
- Pin 2:** VGAGREEN
- Pin 3:** VGABLUE
- Pin 4:** 3V3
- Pin 5:** GND
- Pin 6:** 3V3
- Pin 7:** 5V
- Pin 8:** AUDIOL
- Pin 9:** 5V
- Pin 10:** AUDIOR
- Pin 11:** 5V
- Pin 12:** AUDIOL
- Pin 13:** 5V
- Pin 14:** AUDIOR
- Pin 15:** 5V
- Pin 16:** 3V3

The diagram also shows the following connections:

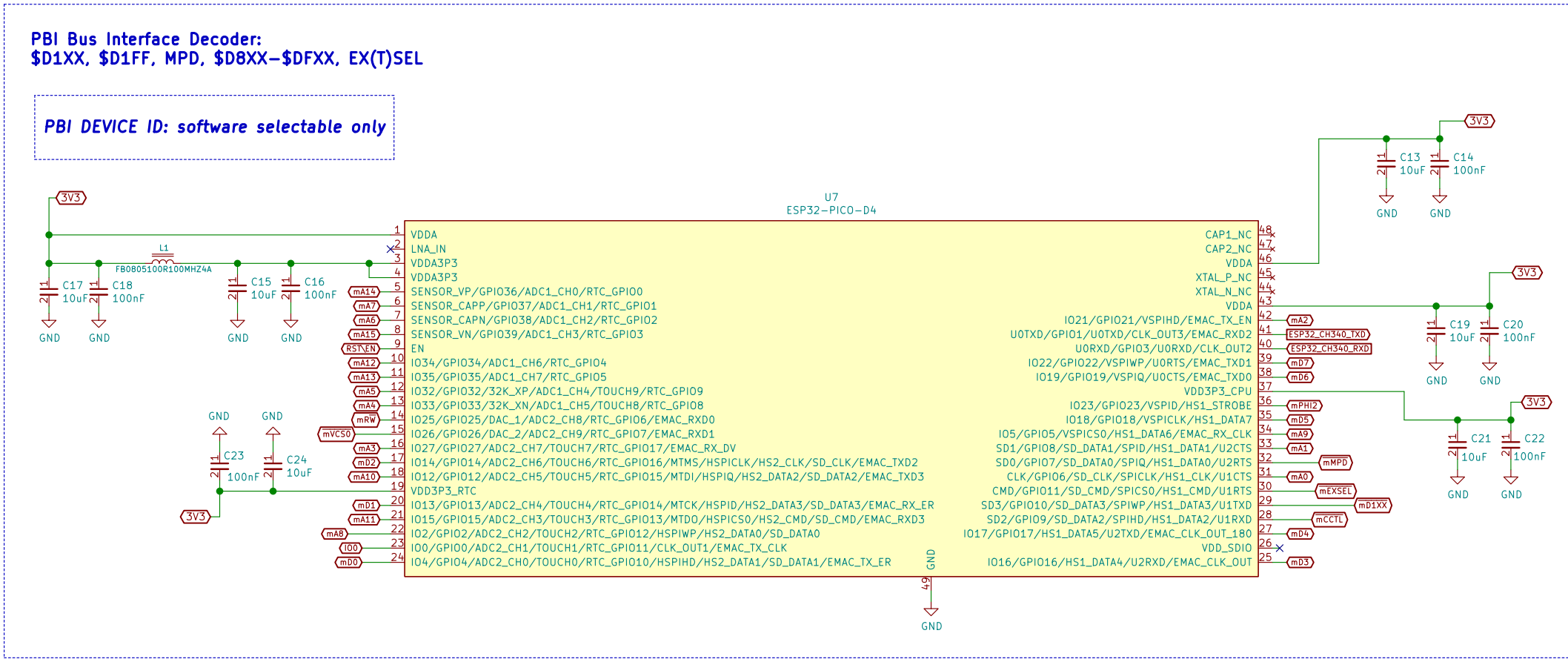
- Pin 1:** VGARED
- Pin 2:** VGAGREEN
- Pin 3:** VGABLUE
- Pin 4:** 3V3
- Pin 5:** GND
- Pin 6:** 3V3
- Pin 7:** 5V
- Pin 8:** AUDIOL
- Pin 9:** 5V
- Pin 10:** AUDIOR
- Pin 11:** 5V
- Pin 12:** AUDIOL
- Pin 13:** 5V
- Pin 14:** AUDIOR
- Pin 15:** 5V
- Pin 16:** 3V3

EXTERNAL DISPLAY WITH AUDIO

The diagram shows the connection of an Iceprog programmer to a target device via a 6-pin header (J6). The connections are as follows:

- Pin 1:** Connected to a 5V supply through a 10K resistor (R33).
- Pin 2:** Connected to the target's **FPGA_CDSN** pin through a 10K resistor (R34).
- Pin 3:** Connected to the target's **FPGA_RESET** pin.
- Pin 4:** Connected to the target's **SPL_MISO** pin.
- Pin 5:** Connected to the target's **SPL_MOSI** pin.
- Pin 6:** Connected to the target's **SPL_SCK** pin.
- Pin 7:** Connected to the target's **SPL_SS[SEL_N]** pin through a 10K resistor (R62).
- Pin 8:** Connected to GND.

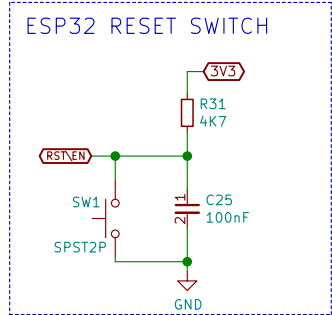
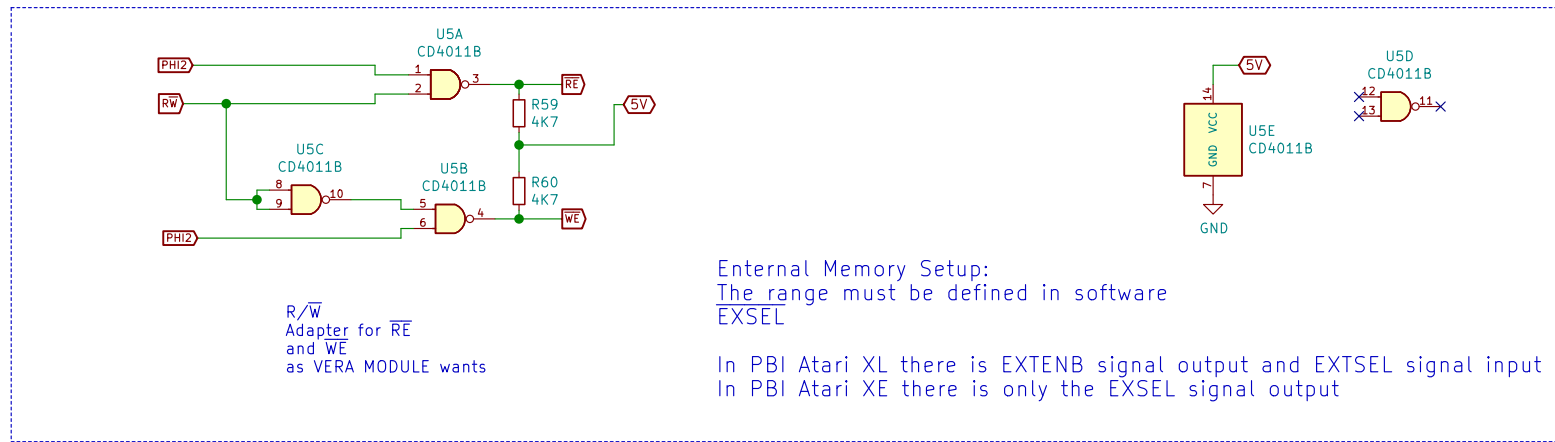
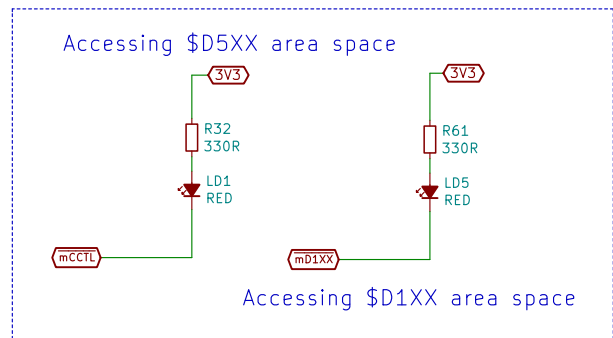
Power supplies are indicated as 3V3 and 5V. A note at the bottom states: **ALL SIGNALS MUST BE IN 3.3V RANGE**.



mVCS0 active & A15..A0 \$D8XX-\$DFXX -> MPD active (Internal 2K ROM)

\$D1FF access & DATABUS = PBI DEVICE ID -> mVCS0 active/deactive

Those signals are valid in ATARI XE only



Gianluca Renzi

RetroBit Lab

Sheet: /BusDecoder/

File: busdecoder.sch

Title: BUS DECODER

Size: A3

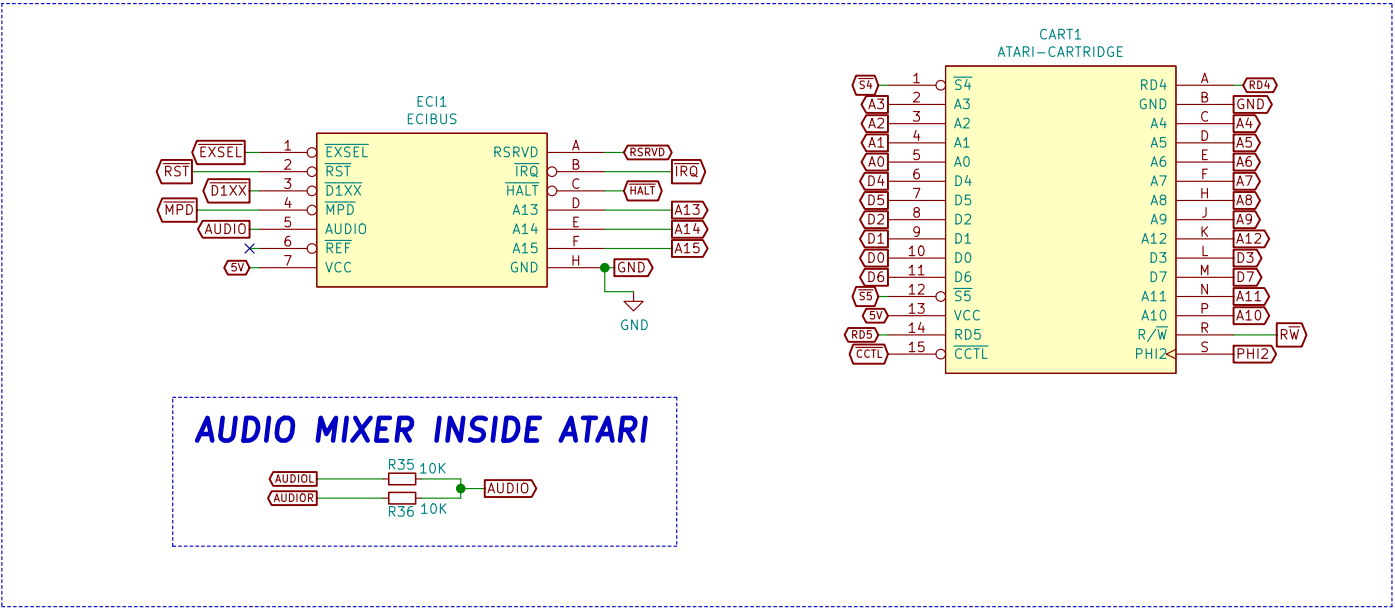
Date: 2025-09-23

Rev: 1.0

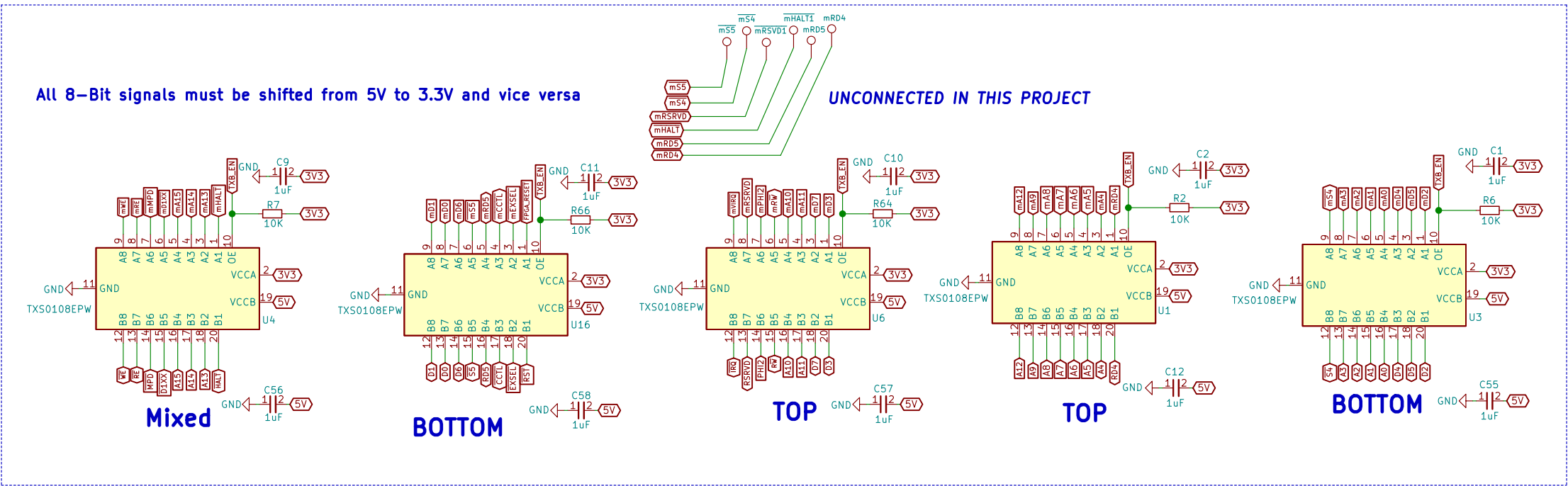
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1

Id: 3/6

ATARI 130XE ECI & CARTRIDGE INTERFACE

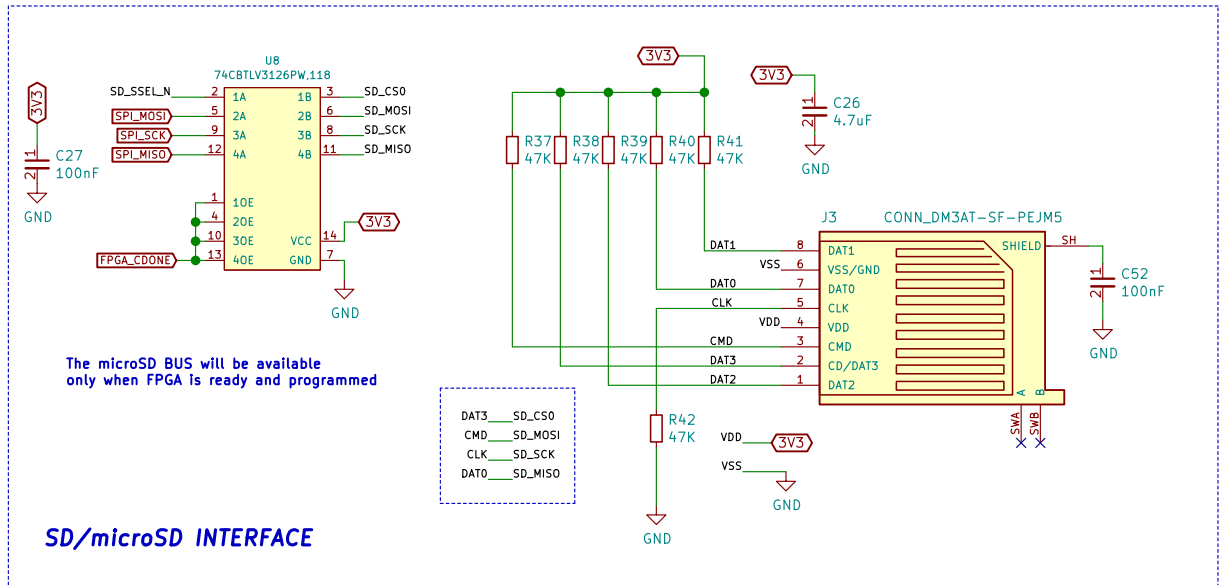


BUS LOGIC LEVEL SHIFTERS



FPGA/SSD Flash Glue Logic

When programming SPI FLASH for bitstream, the JP2 jumper must be closed. Should be open in a normal operational mode.



IC DAC/AUDIO 24BIT 192K 16TSSOP

The diagram shows the WM8524CGEDT IC with the following connections:

- Pin 10 (MCLK):** Connected to ASYSEL.
- Pin 9 (BCLK):** Connected to AUDIO_BCK.
- Pin 8 (LRCLK):** Connected to AUDIO_LRCK.
- Pin 7 (DACDAT):** Connected to AUDIO_DATA.
- Pin 12 (AIFMODE):** Connected to 3V3.
- Pin 11 (MUTE):** Connected to 3V3.
- Pin 1 (LINEOUTL):** Connected to R46 (560R) and then to R45 (560R) and C30 (1uF).
- Pin 16 (LINEOUTR):** Connected to R46 (560R) and then to R45 (560R) and C30 (1uF).
- Pin 5 (CPCA):** Connected to C32 (1uF).
- Pin 3 (CPCB):** Connected to C32 (1uF).
- Pin 15 (AVDD):** Connected to 3V3.
- Pin 6 (LINEVDD):** Connected to 3V3.
- Pin 2 (CPVOUTN):** Connected to C33 (1uF).
- Pin 4 (LINEGND):** Connected to C33 (1uF).
- Pin 13 (AGND):** Connected to C36 (2.2uF).
- Pin 14 (VMID):** Connected to C36 (2.2uF).
- Pin 13 (AGND):** Also connected to C34 (4.7uF) and C35 (4.7uF).
- Pin 14 (VMID):** Also connected to C34 (4.7uF) and C35 (4.7uF).
- Output of C34 and C35:** Connected to 3V3.
- Output of C30 and C31:** Connected to AUDIOIOL and AUDIOIOR.
- Output of C32 and C33:** Connected to GND.
- Output of C36:** Connected to GND.

AUDIO 3.5mm OUTPUT

AUDIO 3.5mm OUTPUT

560R R67 2 TP

560R R68 3 RMC

1 SLEEVE

GND

SJ-3523-SMT-TR

J7

