Sheet: VeraModule

VERA FPGA

File: vera-fpga.sch

Sheet: BusDecoder

BUS DECODER

File: busdecoder.sch

Sheet: Vera FPGA flash

VERA SPI FLASH
SD CARD INTERFACE

File: vera-fpga-flash.sch

Sheet: CartridgeInterface

CARTRIDGE INTERFACE

File: cartridgeInterface.sch

Sheet: PowerSupply

POWER SUPPLY

File: powersupply.sch

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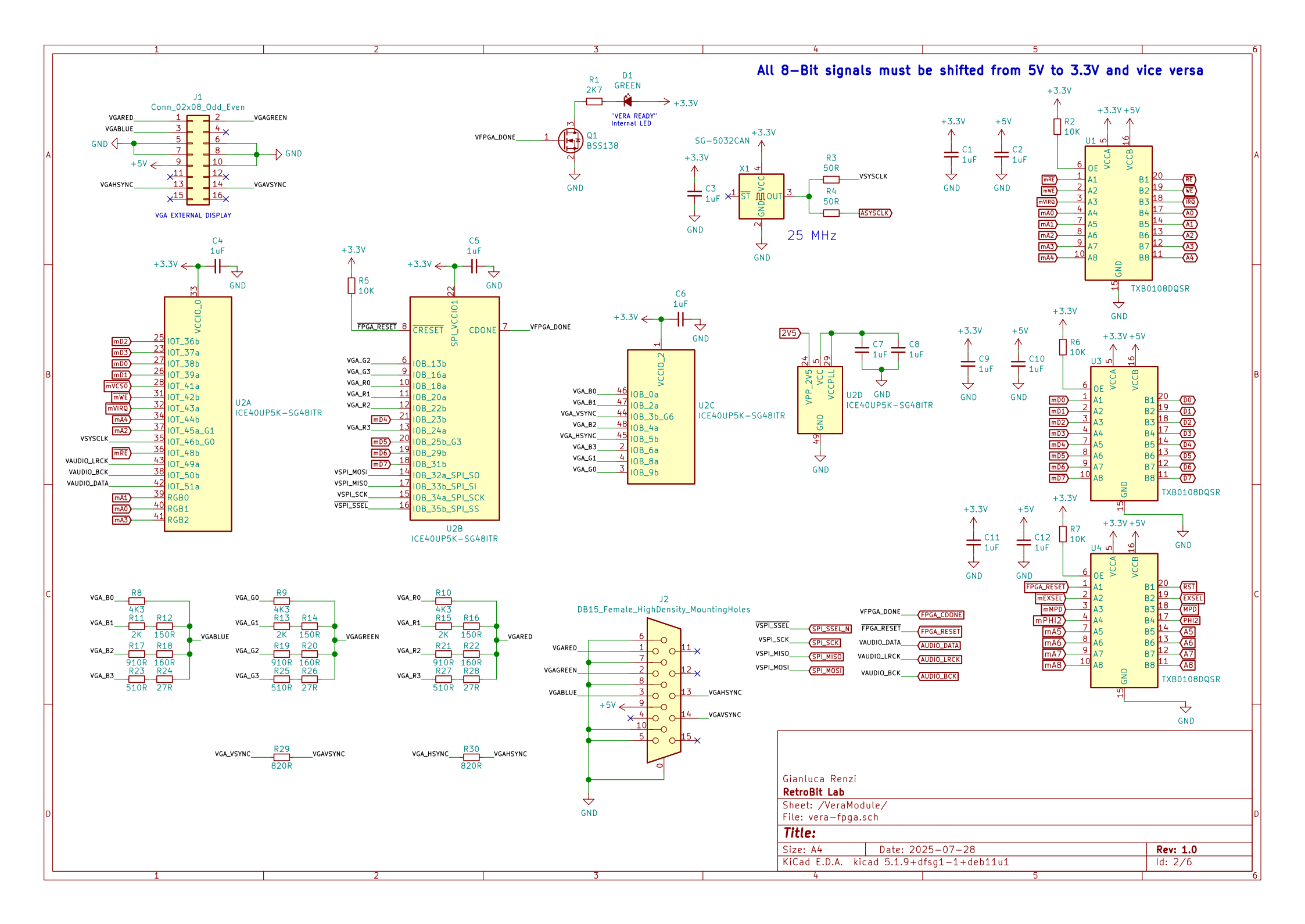
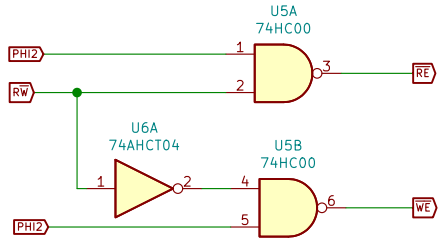
Sheet: /
File: VERA-MODULE-RBL.sch

***Title: VERA FPGA Audio & Video Board***

| Size: A4 | Date: 2025-07-28 | **Rev: 1.0** |
|---|---|---|
| KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1 | | Id: 1/6 |


All 8-Bit signals must be shifted from 5V to 3.3V and vice versa
J1
Conn_02x08_Odd_Even
VGARED
VGABLUE
VGAHSYNC
VGAGREEN
VGAVSYNC
GND
+5V
VGA EXTERNAL DISPLAY
R1
2K7
D1
GREEN
"VERA READY"
Internal LED
+3.3V
VFPGA_DONE
Q1
BSS138
SG-5032CAN
X1
C3
1uF
R3
50R
R4
50R
VSYSCLK
ASYSCLK
25 MHz
C1
1uF
C2
1uF
R2
10K
U1
TXB0108DQSR
C4
1uF
R5
10K
C5
1uF
FPGA_RESET
CRESET
SPI_VCCIO1
CDONE
VFPGA_DONE
U2B
ICE40UP5K-SG48ITR
C6
1uF
VCCIO_2
U2C
ICE40UP5K-SG48ITR
2V5
VPP_2V5
VCC
VCCPLL
C7
1uF
C8
1uF
U2D
ICE40UP5K-SG48ITR
C9
1uF
C10
1uF
R6
10K
U3
TXB0108DQSR
C11
1uF
C12
1uF
R7
10K
U4
TXB0108DQSR
VCCIO_0
U2A
ICE40UP5K-SG48ITR
mD2
mD3
mD0
mD1
mVCS0
mWE
mVIRQ
mA4
mA2
VSYSCLK
mRE
VAUDIO_LRCK
VAUDIO_BCK
VAUDIO_DATA
mA1
mA0
mA3
RGB0
RGB1
RGB2
R8
R11
R12
R17
R18
R23
R24
VGABLUE
R9
R13
R14
R19
R20
R25
R26
VGAGREEN
R10
R15
R16
R21
R22
R27
R28
VGARED
R29
820R
VGAVSYNC
R30
820R
VGAHSYNC
J2
DB15_Female_HighDensity_MountingHoles
VSPI_SSEL
VSPI_SCK
VSPI_MISO
VSPI_MOSI
SPI_SSEL_N
SPI_SCK
SPI_MISO
SPI_MOSI
FPGA_CDONE
FPGA_RESET
VAUDIO_DATA
VAUDIO_LRCK
VAUDIO_BCK
AUDIO_DATA
AUDIO_LRCK
AUDIO_BCK
Gianluca Renzi
RetroBit Lab
Sheet: /VeraModule/
File: vera-fpga.sch
Title:
Size: A4
Date: 2025-07-28
Rev: 1.0
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1
Id: 2/6



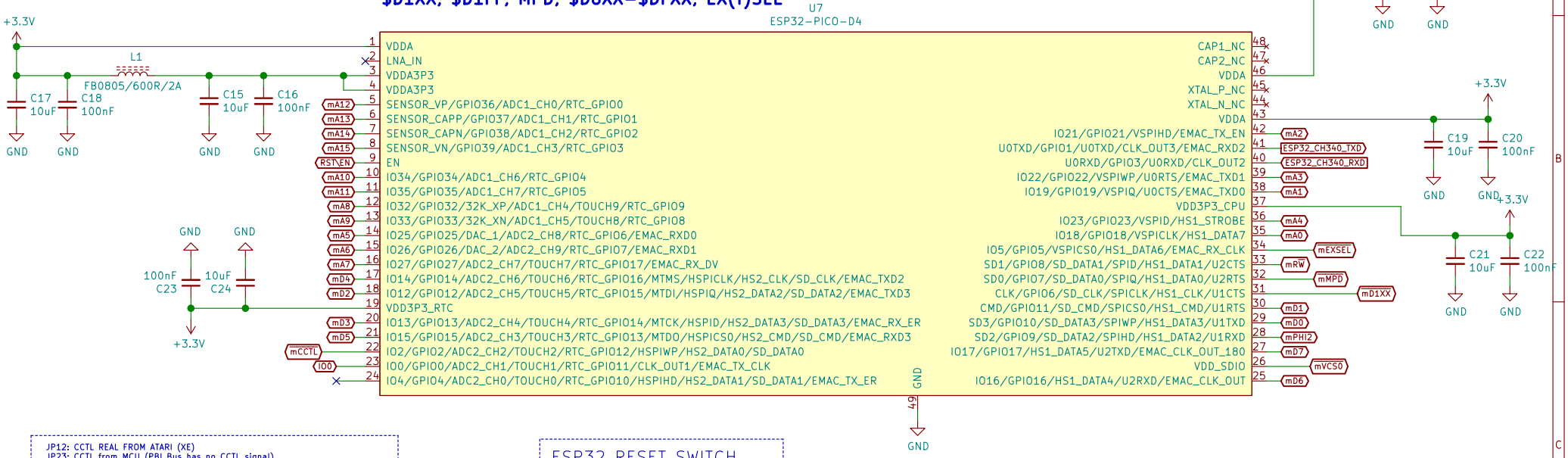

R/$\overline{W}$
Adapter for $\overline{RE}$
and $\overline{WE}$
as VERA MODULE wants

Enternal Memory Setup:
The range must be defined in software
EXSEL

In PBI Atari XL there is EXTENB signal output and EXTSEL signal input
In PBI Atari XE there is only the EXSEL signal output

**PBI DEVICE ID: software selectable only**

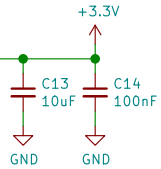
**PBI Bus Interface Decoder:**
**$D1XX, $D1FF, MPD, $D8XX–$DFXX, EX(T)SEL**





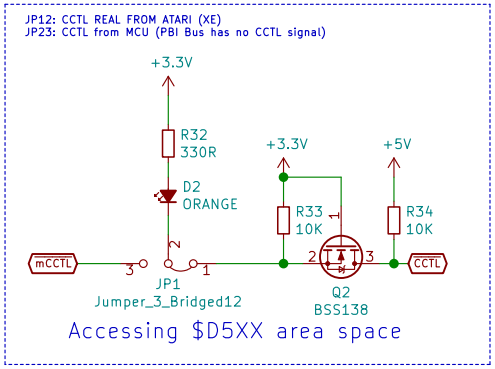


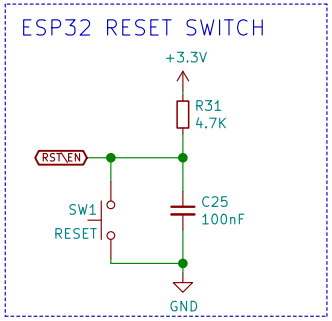









mVCS0 active & A15..A0 $D8XX–$DFXX –> MPD active (Internal 2K ROM)

$D1FF access & DATABUS = PBI DEVICE ID –> mVCS0 active/deactive

| | | |
|---|---|---|
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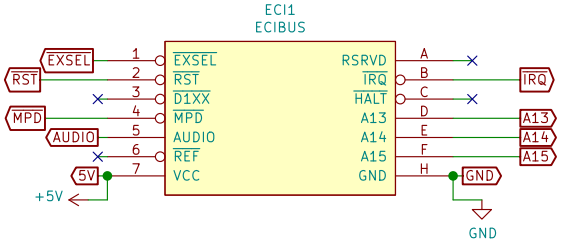
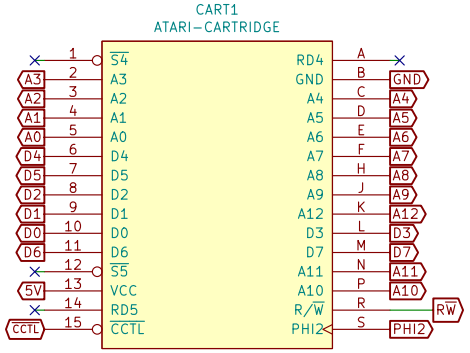
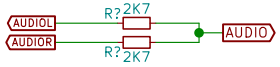
| Sheet: /BusDecoder/<br>File: busdecoder.sch | | |
| ***Title:*** | | |
| Size: A4 | Date: 2025-07-28 | **Rev: 1.0** |
| KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1 | | Id: 3/6 |

# ATARI 130XE ECI & CARTRIDGE INTERFACE




## AUDIO MIXER INSIDE ATARI





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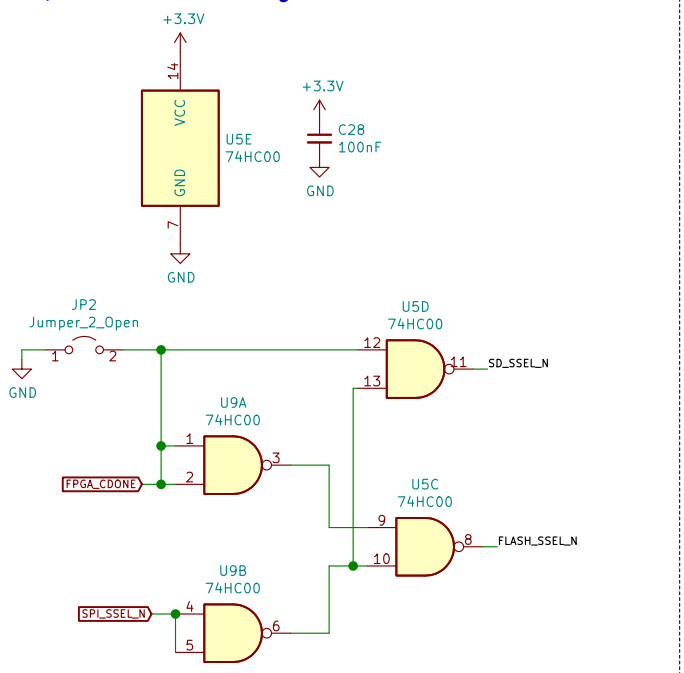
Sheet: /CartridgeInterface/
File: cartridgeInterface.sch

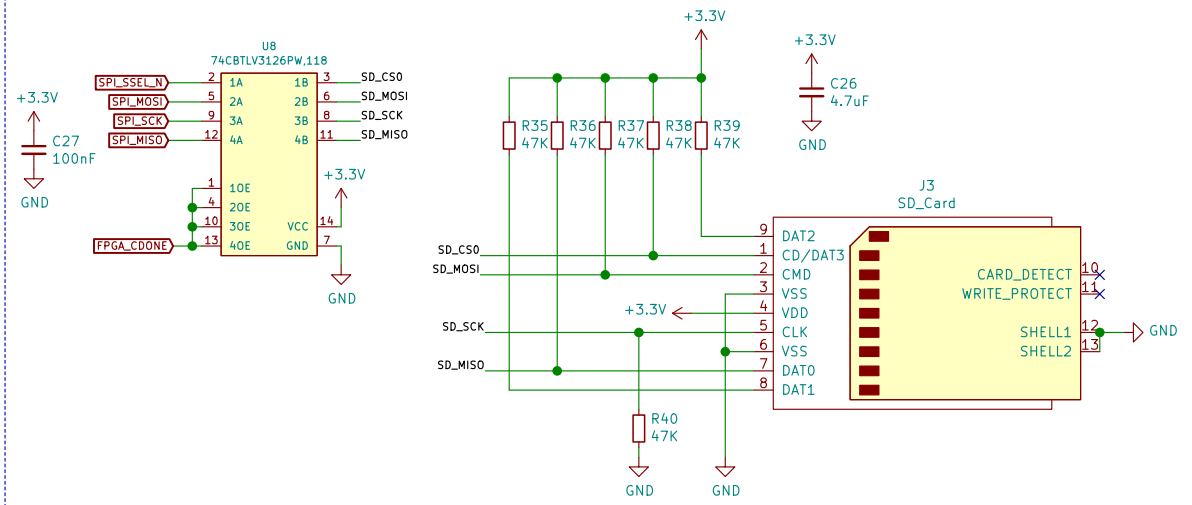
***Title:***

| | | |
|---|---|---|
| Size: A4 | Date: 2025-07-28 | **Rev: 1.0** |
| KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1 | | Id: 4/6 |

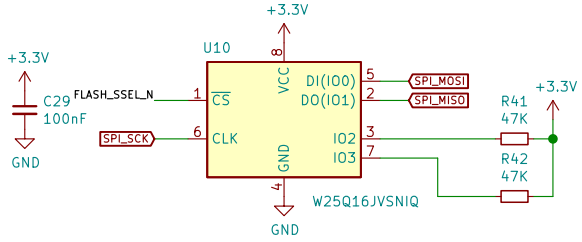
## FPGA/SSD Flash Glue Logic



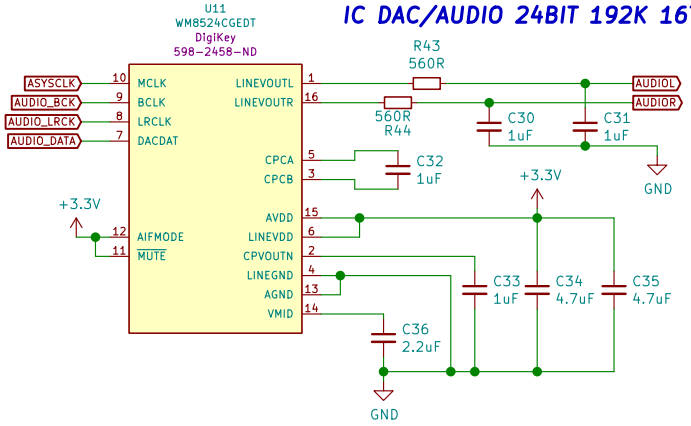

## SD/microSD INTERFACE




## SPI 16MB FLASH




## IC DAC/AUDIO 24BIT 192K 16TSSOP

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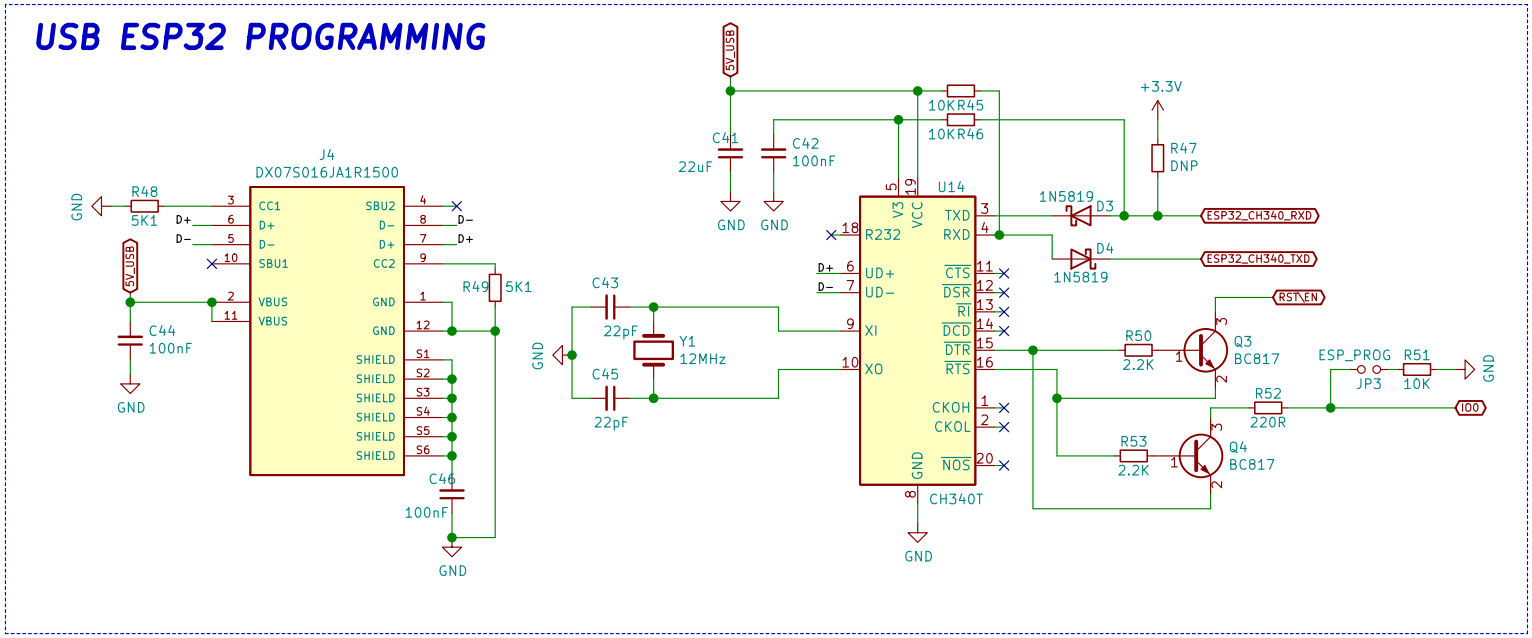
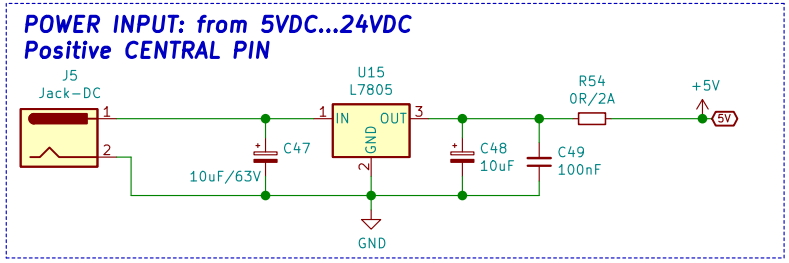
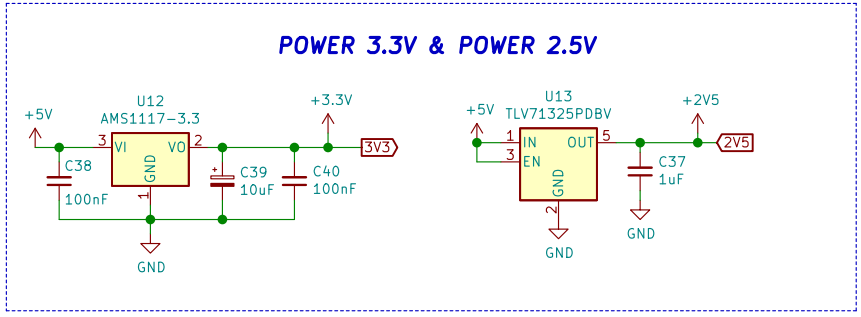
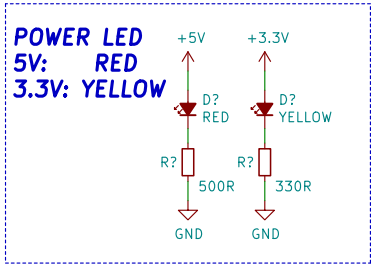
| | | |
|---|---|---|
| Sheet: /Vera FPGA flash/ | | |
| File: vera-fpga-flash.sch | | |
| ***Title:*** | | |
| Size: A4 | Date: 2025-07-28 | **Rev: 1.0** |
| KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1 | | Id: 5/6 |

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Sheet: /PowerSupply/
File: powersupply.sch

***Title:***

| | | |
|---|---|---|
| Size: A4 | Date: 2025-07-28 | **Rev: 1.0** |
| KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1 | | Id: 6/6 |