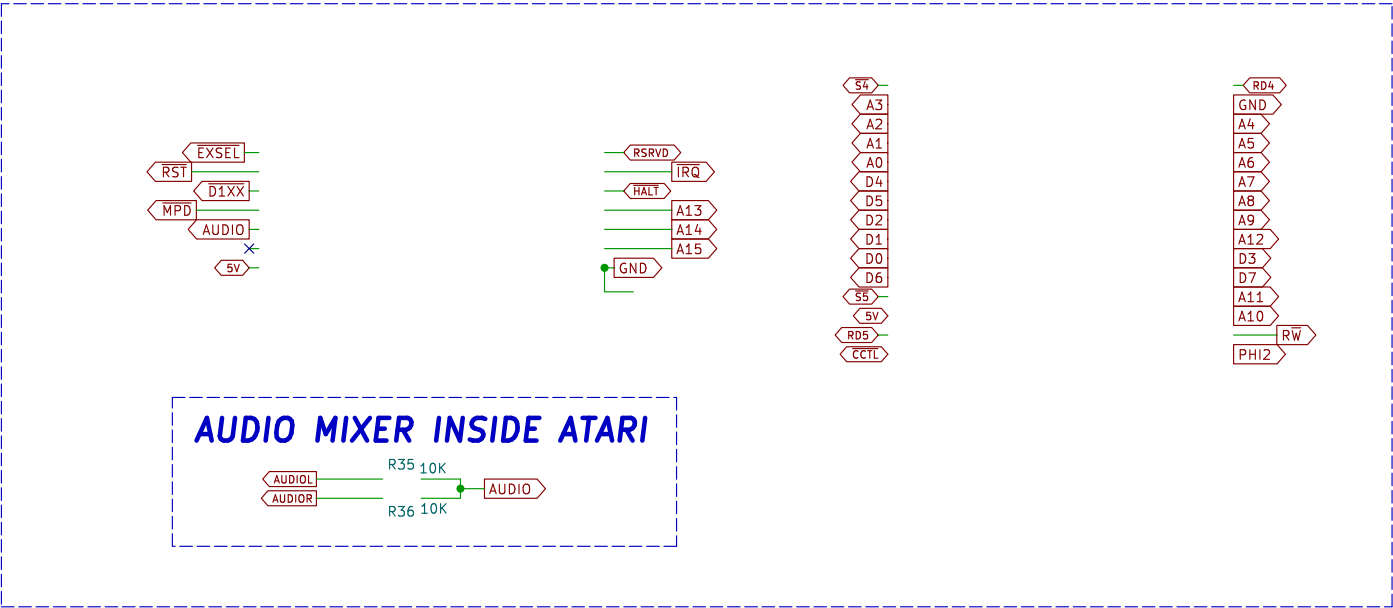
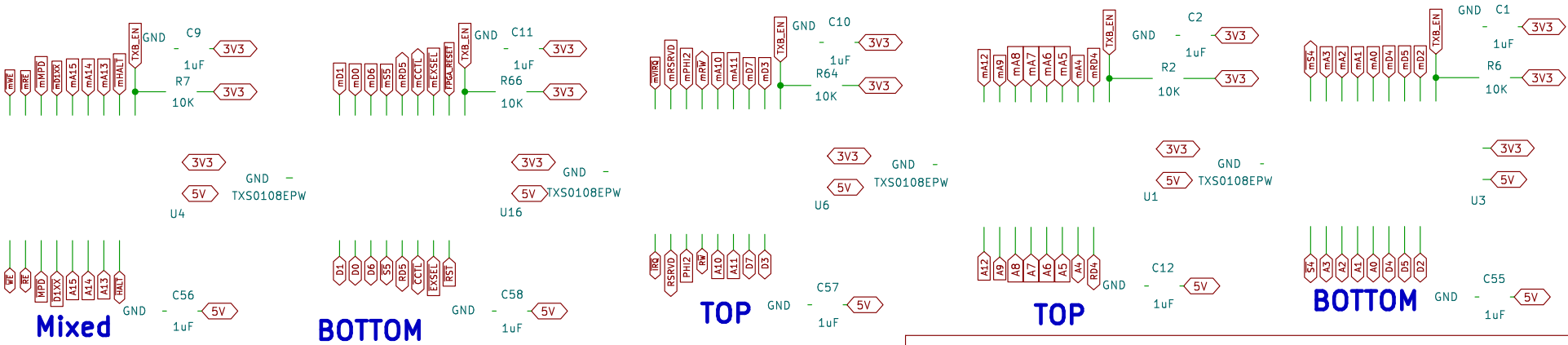


# ATARI 130XE ECI & CARTRIDGE INTERFACE

All 8-Bit signals must be shifted from 5V to 3.3V and vice versa

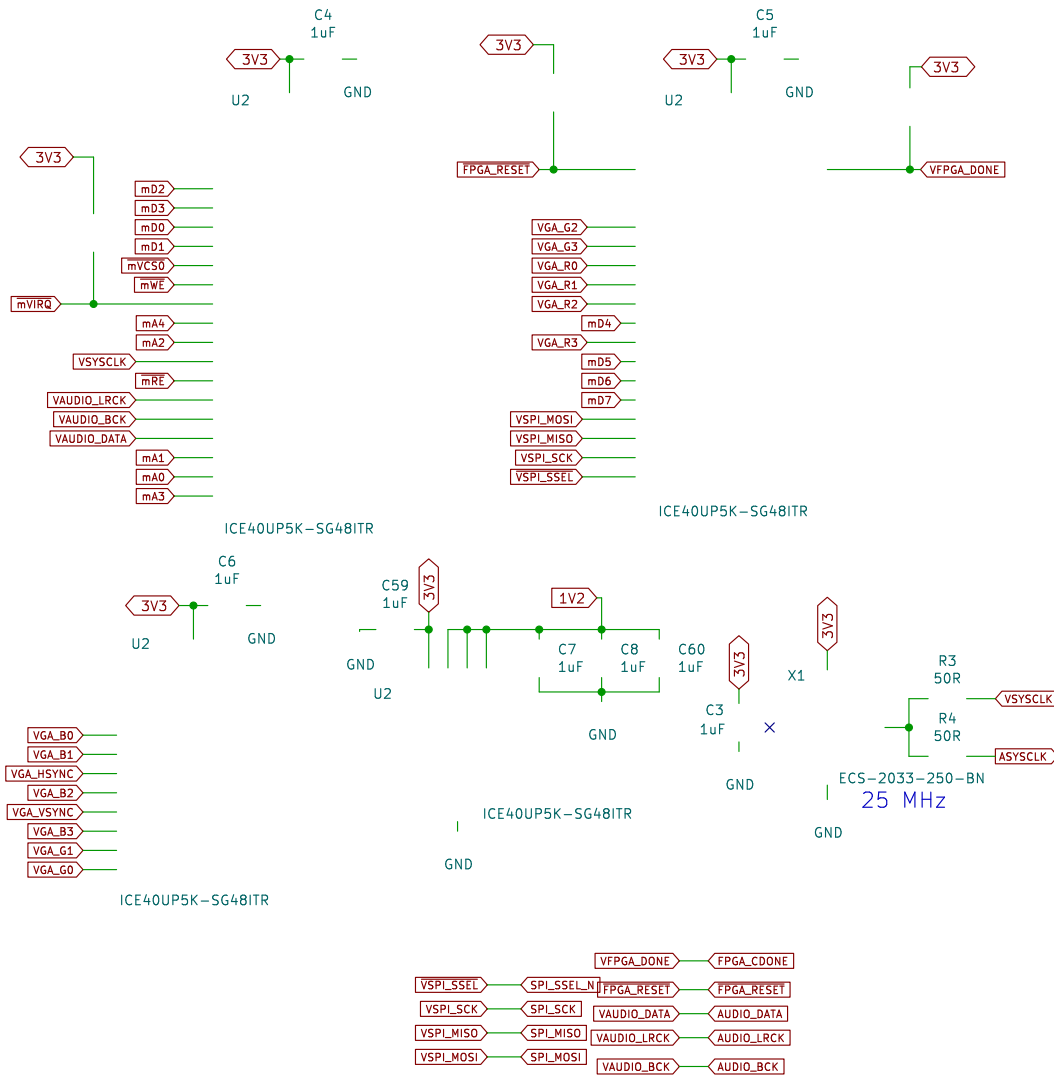


UNCONNECTED IN THIS PROJECT

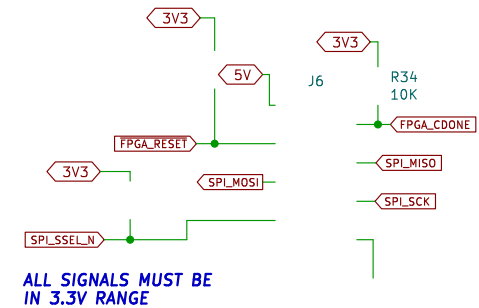


## BUS LOGIC LEVEL SHIFTERS

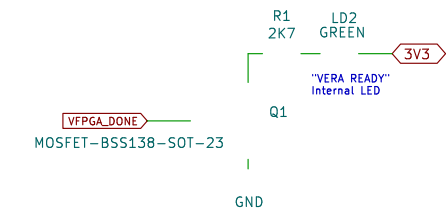
## FPGA VERA LOGIC VIDEO & AUDIO CARD



### iceprog programmer USB FTDI / SPI



### VERA FPGA PROGRAMMED OK



Gianluca Renzi

**RetroBit Lab**

Sheet: /VeraModule/

File: vera-fpga.sch

**Title: VERA MODULE AND PROGRAMMING CONNECTOR**

Size: A4

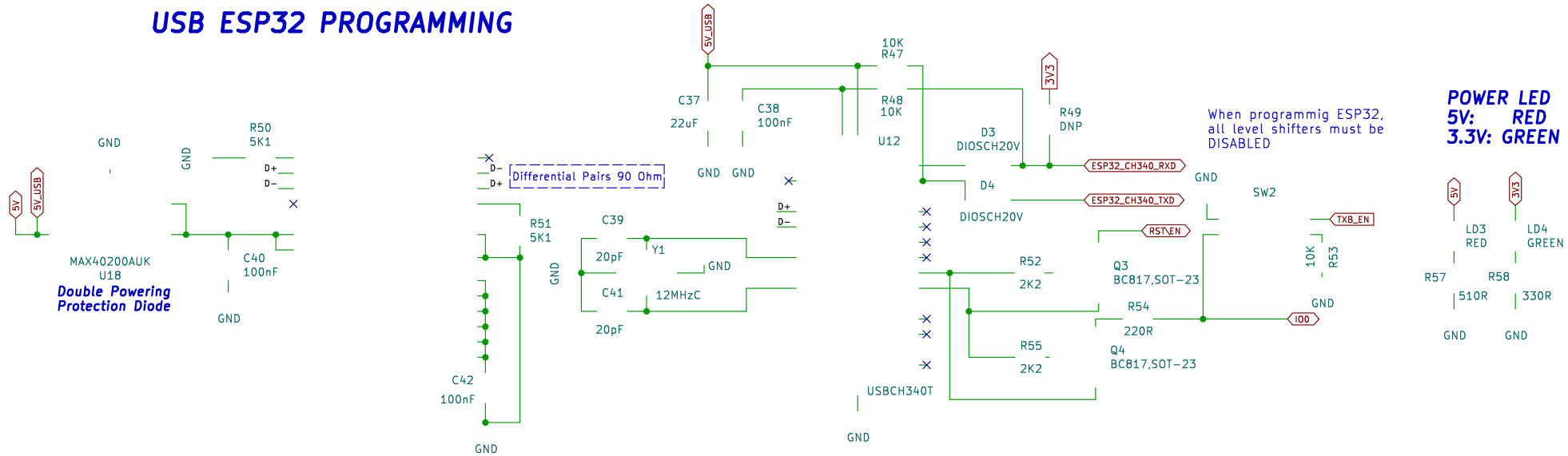
Date: 2025-10-17

Rev: 1.0

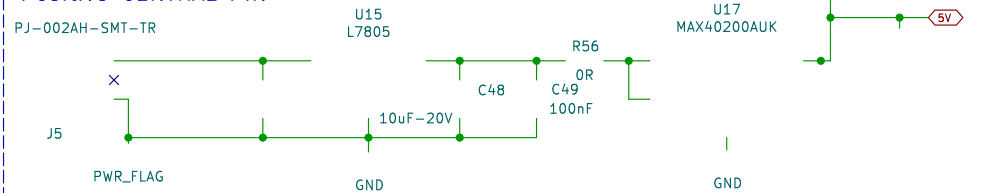
KiCad E.D.A. 9.0.5

Id: 3/7

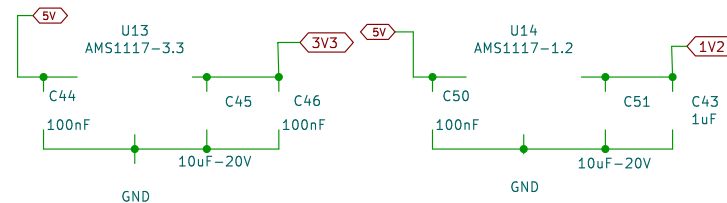
## USB ESP32 PROGRAMMING



POWER INPUT: from 5VDC...24VDC  
Positive CENTRAL PIN



**POWER 3.3V & POWER 1.2V**



**RetroBit Lab**

Sheet: /PowerSupply/

File: powersupply.sch

Title: POWERSUPPLY and USB

Size: A4

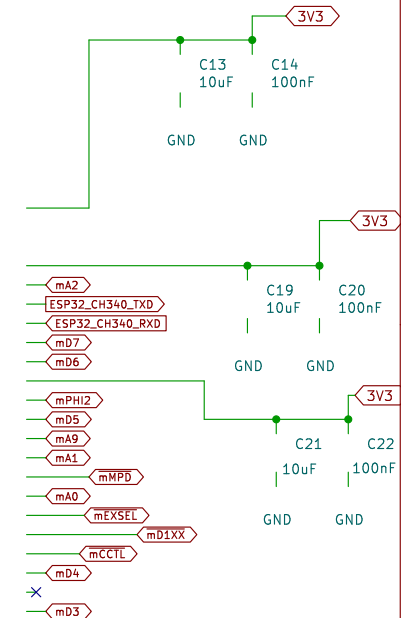
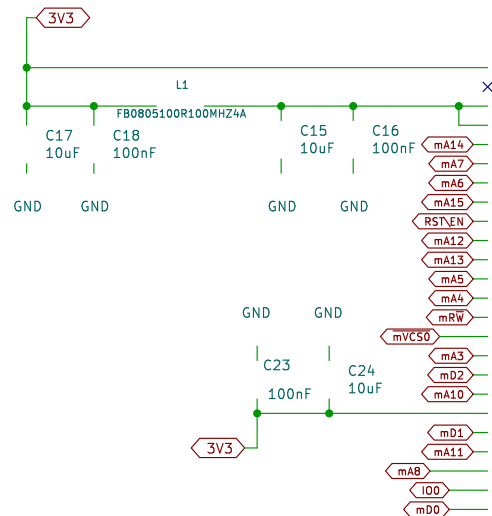
Date: 2025-10-17

Rev: 1.0

Id: 4/7

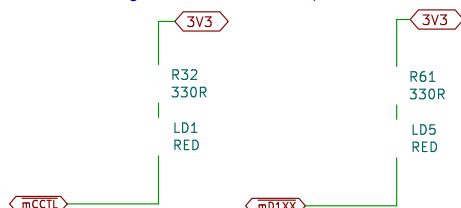
# PBI Bus Interface Decoder: \$D1XX, \$D1FF, MPD, \$D8XX-\$DFXX, EX(T)SEL

PBI DEVICE ID: software selectable only

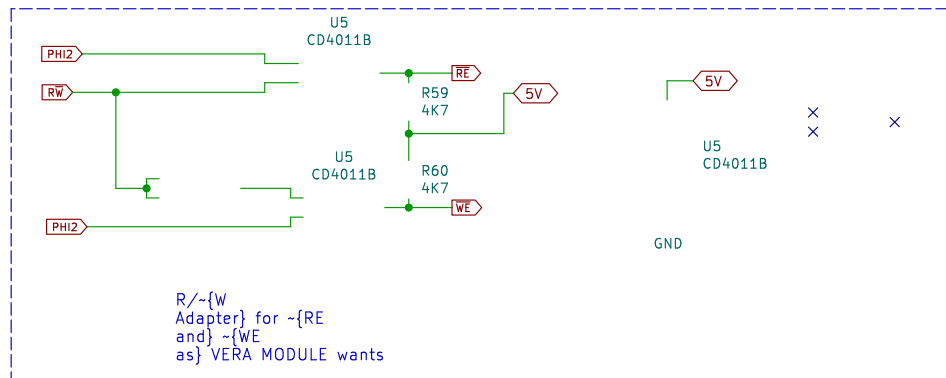


## Those signals are valid in ATARI XE only

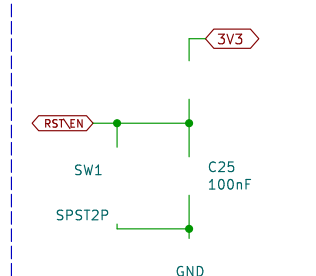
Accessing \$D5XX area space



Accessing \$D1XX area space



ESP32 RESET SWITCH



Internal Memory Setup:  
The range must be defined in software  
~{EXSEL

In} PBI Atari XL there is EXTENB signal output and EXTSEL signal input  
In PBI Atari XE there is only the EXSEL signal output

mVCS0 active & A15..A0 \$D8XX-\$DFXX -> MPD active (Internal 2K ROM)

\$D1FF access & DATABUS = PBI DEVICE ID -> mVCS0 active/deactive

Gianluca Renzi

RetroBit Lab

Sheet: /BusDecoder/

File: busdecoder.sch

Title: BUS DECODER

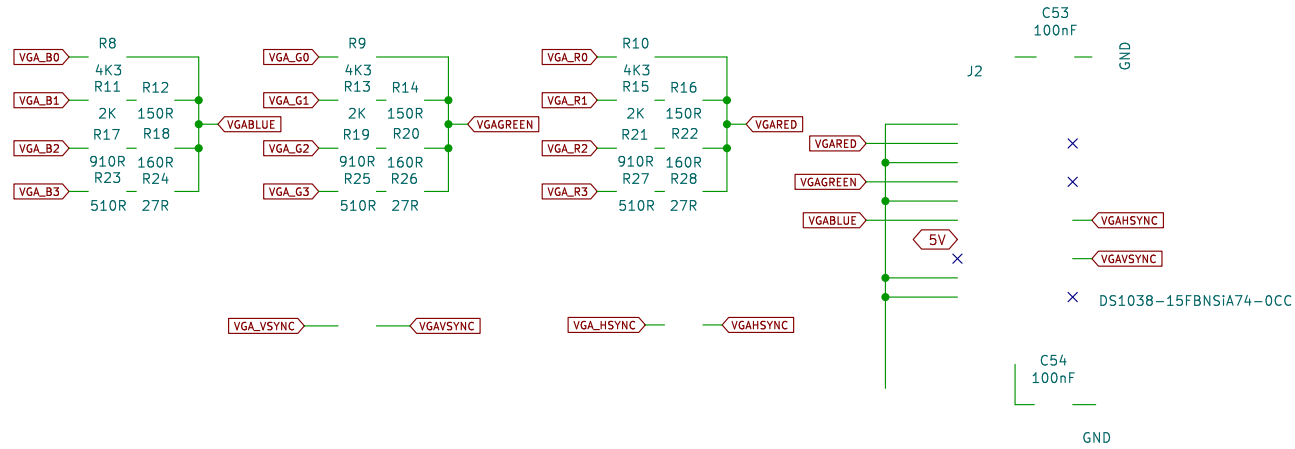
Size: A4 Date: 2025-10-17

KiCad E.D.A. 9.0.5

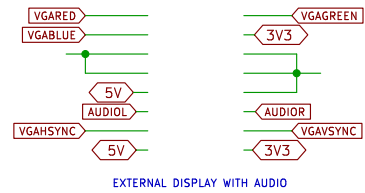
Rev: 1.0

Id: 5/7

# ANALOG VGA SIGNALS



# EXTERNAL VIDEO CONNECTOR



Gianluca Renzi  
**RetroBit Lab**

Sheet: /VGA Analog/  
File: vga-analog.sch

## Title: VGA ANALOG AND EXTERNAL VIDEO CONNECTOR

Size: A4

Date: 2025-10-17

Rev: 1.0

KiCad E.D.A. 9.0.5

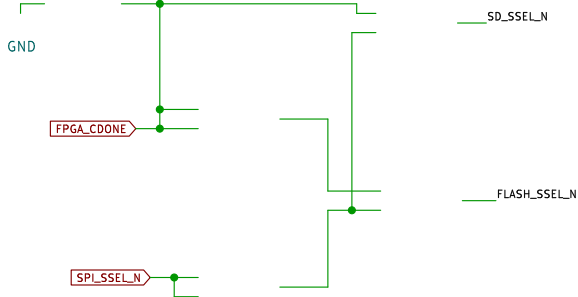
Id: 6/7

3V3

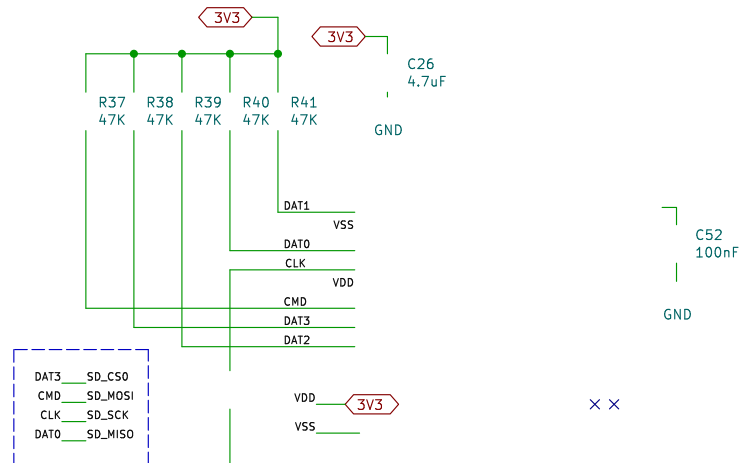
3V3

C28  
100nF

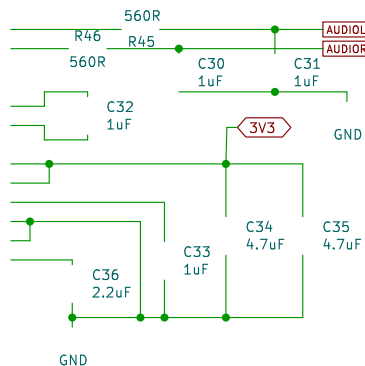
JP2  
Jumper\_2\_Open



SD\_CS0  
SD\_MOSI  
SD\_SCK  
SD\_MISO



ASYSCLK  
AUDIO\_BCK  
AUDIO\_LRCK  
AUDIO\_DATA

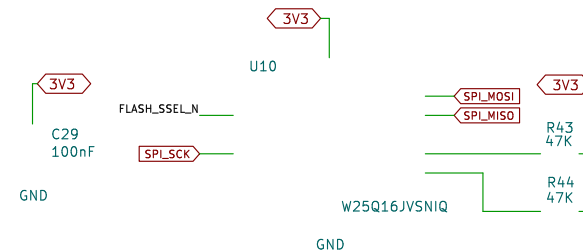


AUDIO1 — 560R — R67 —

AUDIO2 — 560R — R68 —

GND

**SPI 16MB FLASH**



Sheet: /Vera FPGA flash/  
File: vera-fpga-flash.sch

Size: A4	Date: 2025-10-17
KiCad E.D.A. 9.0.5	

Rev: 1.0  
Id: 7/7