Sheet: VeraModule

VERA FPGA

File: vera-fpga.sch

Sheet: BusDecoder

BUS DECODER

File: busdecoder.sch

Sheet: Vera FPGA flash

VERA SPI FLASH
SD CARD INTERFACE

File: vera-fpga-flash.sch

Sheet: CartridgeInterface

CARTRIDGE INTERFACE

File: cartridgeInterface.sch

Sheet: PowerSupply

POWER SUPPLY

File: powersupply.sch

FIDUCIAL TOP

FID3 Fiducial FID4 Fiducial

FIDUCIAL BOTTOM

FID2 Fiducial FID1 Fiducial

LOGO1 VERA X16 LOGO

LOGO2 ATARI READY

LOGO3 KiCAD DESIGN

LOGO4 ATARI DUO BUS

LOGO5 ESP32_BOBOARD

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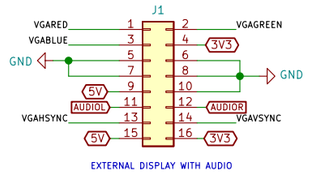
RetroBit Lab

Sheet: /
File: VERA-MODULE-RBL.sch

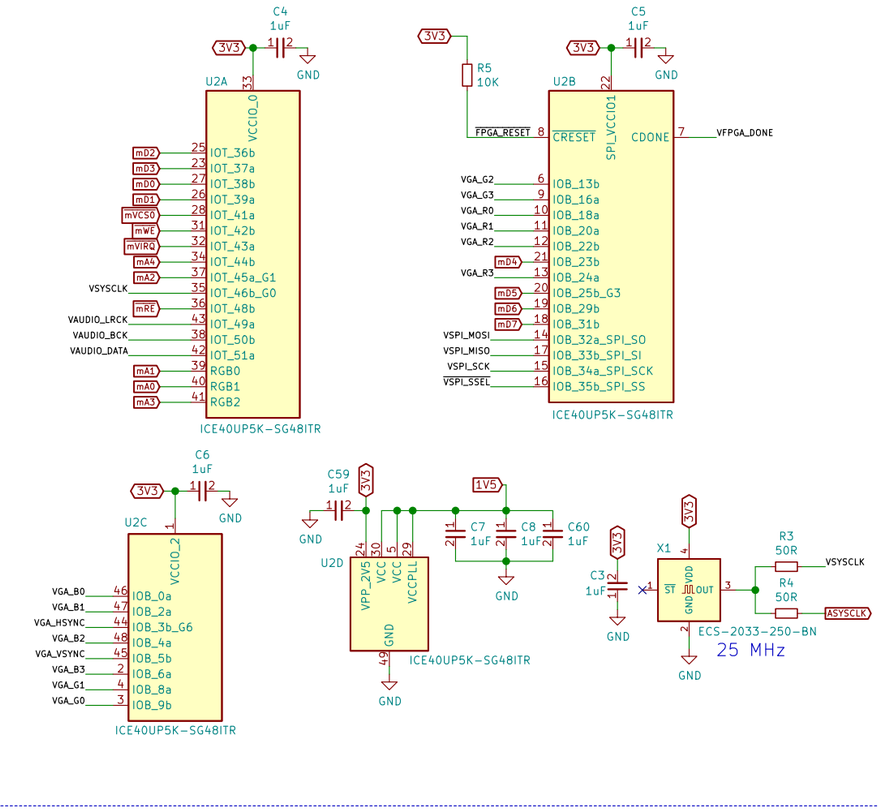
Title: VERA FPGA Audio & Video Board

Size: A4	Date: 2025-09-16	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 1/6

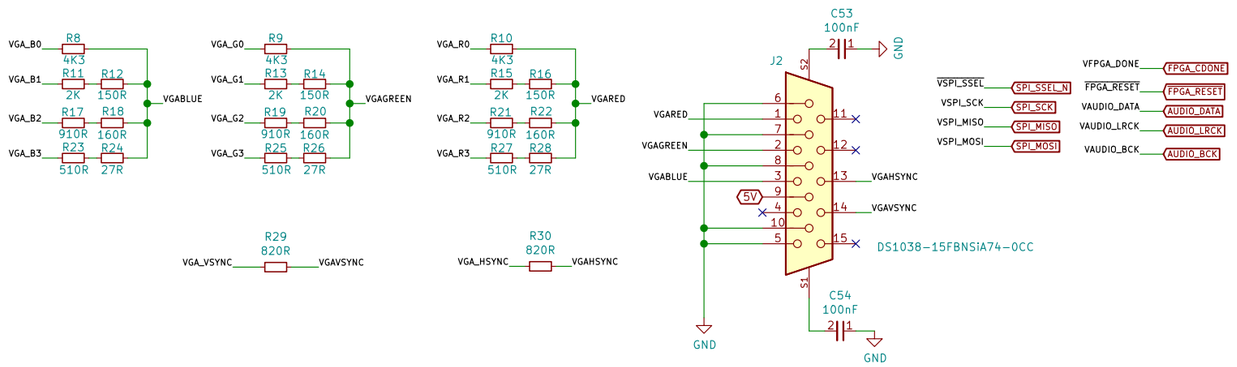
EXTERNAL VIDEO CONNECTOR



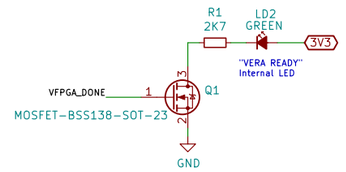
FPGA VERA LOGIC VIDEO & AUDIO CARD



ANALOG VGA SIGNALS



VERA FPGA PROGRAMMED OK



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RetroBit Lab

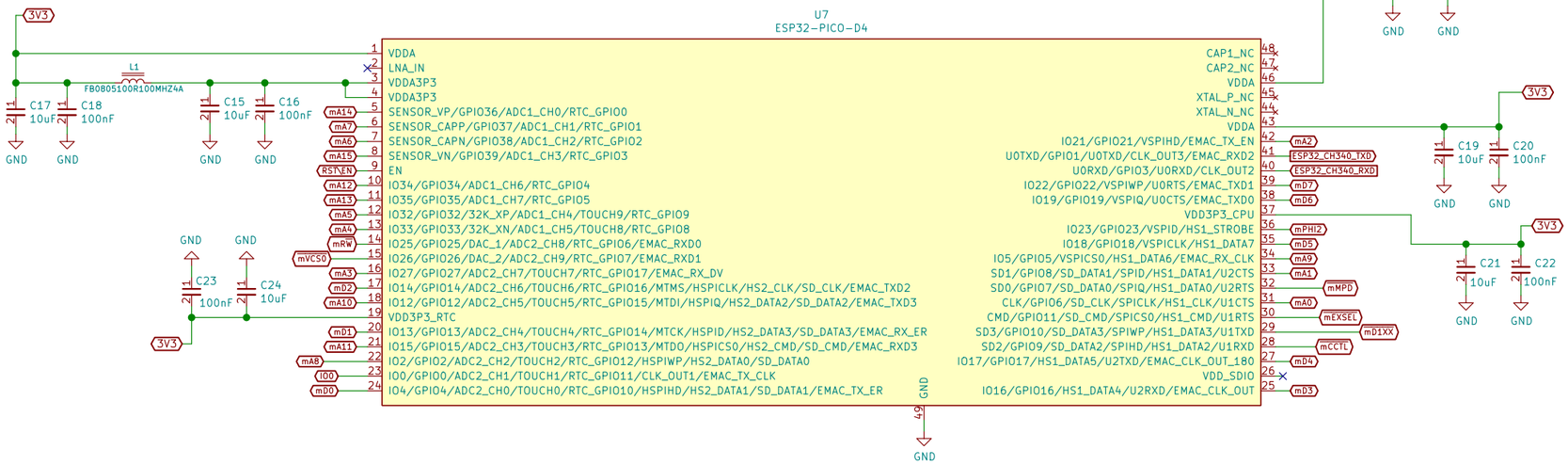
Sheet: /VeraModule/
File: vera-fpga.sch

Title: VERA MODULE AND EXTERNAL VIDEO CONNECTOR

Size: A3	Date: 2025-09-16	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 2/6

PBI Bus Interface Decoder:
$D1XX, $D1FF, MPD, $D8XX–$DFXX, EX(T)SEL

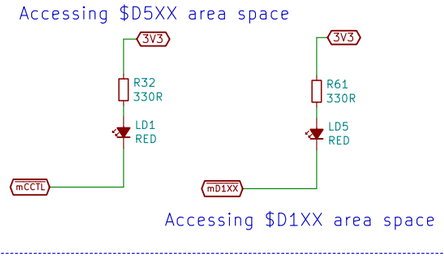
PBI DEVICE ID: software selectable only

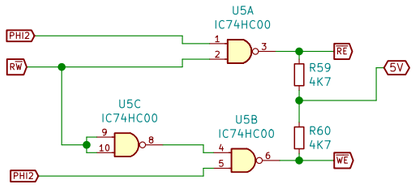


mVCS0 active & A15..A0 $D8XX–$DFXX –> MPD active (Internal 2K ROM)

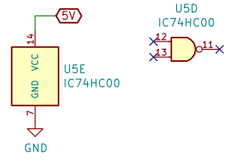
$D1FF access & DATABUS = PBI DEVICE ID –> mVCS0 active/deactive

Those signals are valid in ATARI XE only



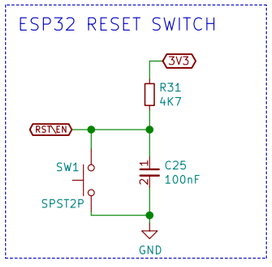


R/$\overline{W}$
Adapter for $\overline{RE}$
and $\overline{WE}$
as VERA MODULE wants



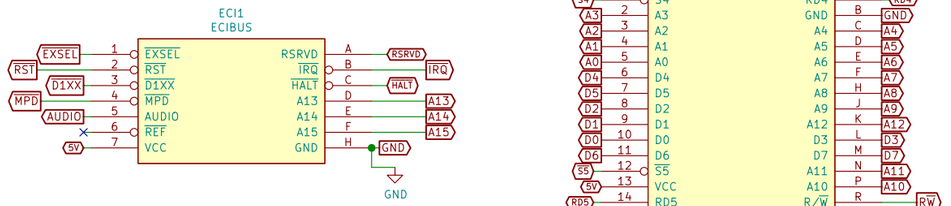
Enternal Memory Setup:
The range must be defined in software
EXSEL

In PBI Atari XL there is EXTENB signal output and EXTSEL signal input
In PBI Atari XE there is only the EXSEL signal output



Gianluca Renzi **RetroBit Lab**		
Sheet: /BusDecoder/ File: busdecoder.sch		
Title: BUS DECODER		
Size: A3	Date: 2025–09–16	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1–1+deb11u1		Id: 3/6

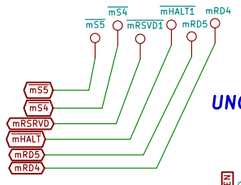
ATARI 130XE ECI & CARTRIDGE INTERFACE

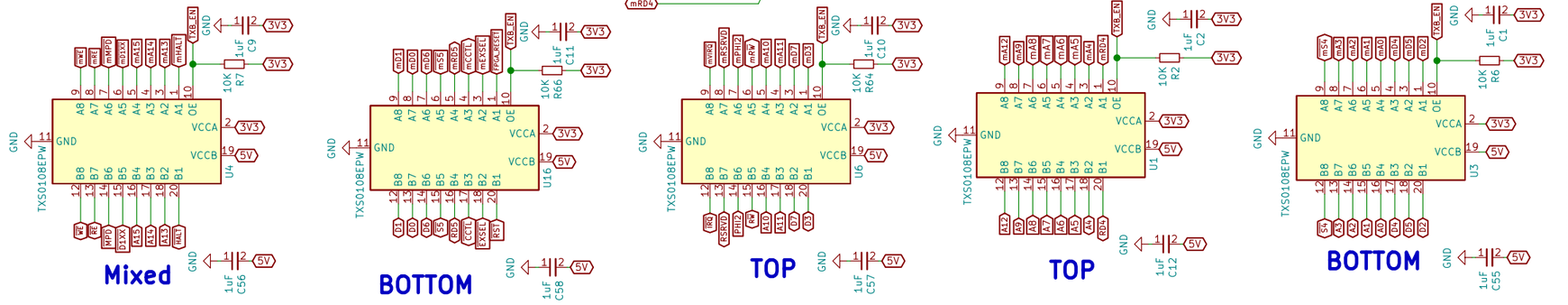


BUS LOGIC LEVEL SHIFTERS

All 8-Bit signals must be shifted from 5V to 3.3V and vice versa

UNCONNECTED IN THIS PROJECT





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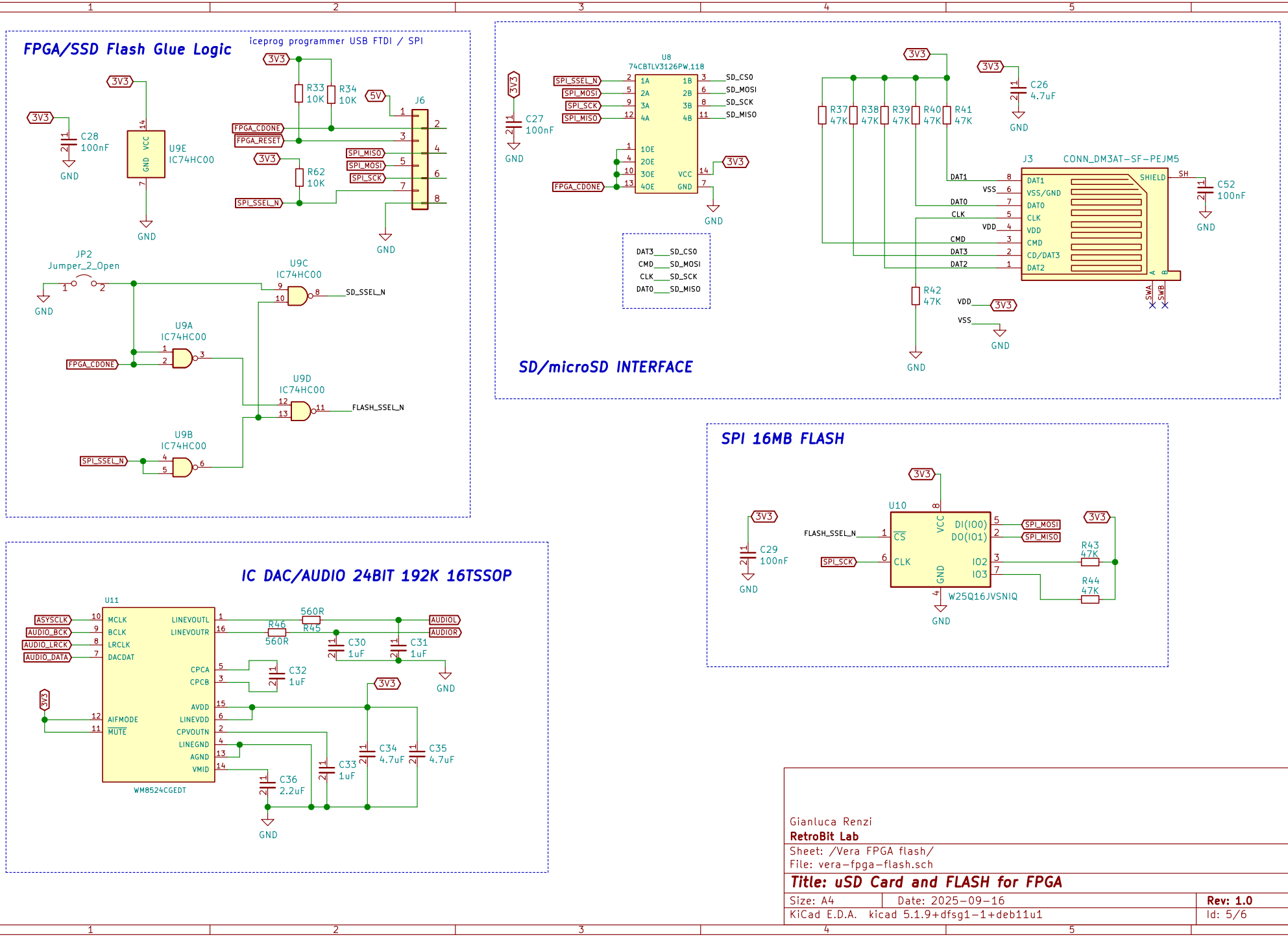
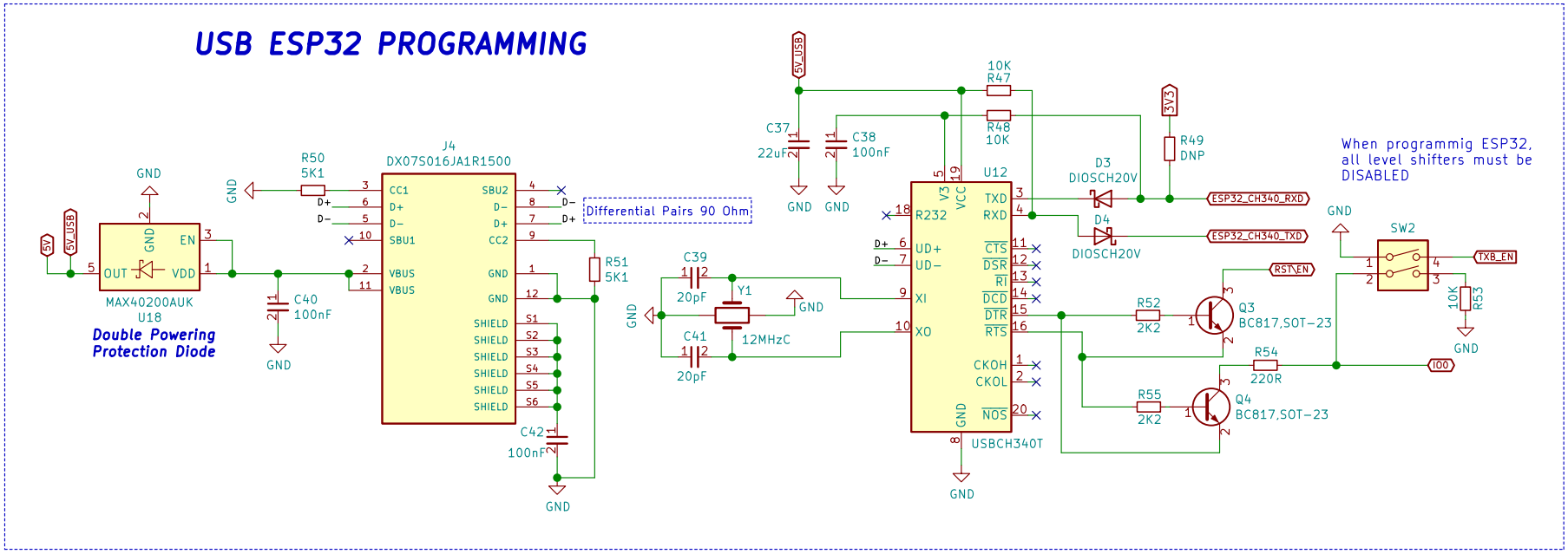
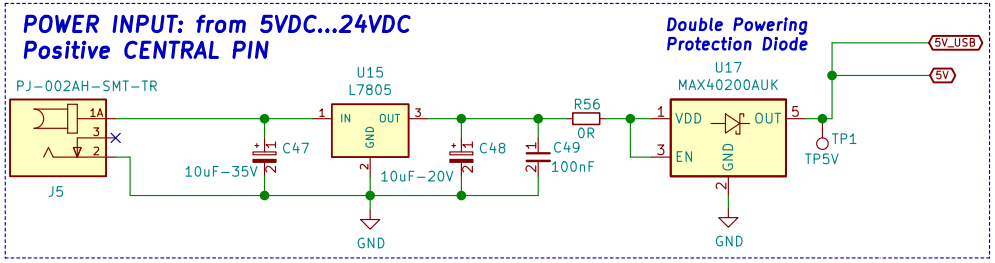
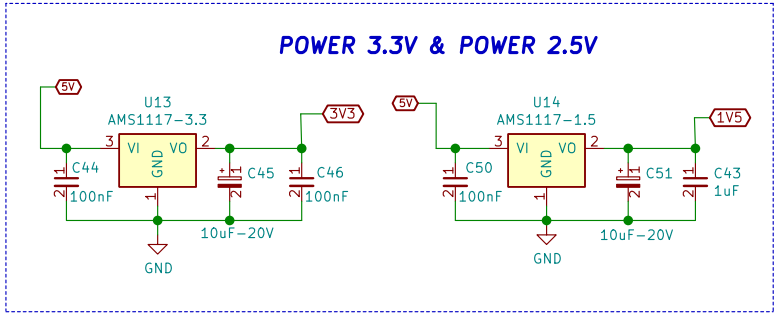
RetroBit Lab

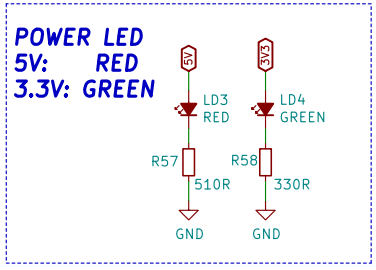
Sheet: /CartridgeInterface/		
File: cartridgeInterface.sch		
Title: CARTRIDGE INTEFACE AND BUS LEVEL SHIFTERS		
Size: A3	Date: 2025-09-16	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 4/6


FPGA/SSD Flash Glue Logic
iceprog programmer USB FTDI / SPI
3V3
C28
100nF
GND
U9E
IC74HC00
R33
10K
R34
10K
5V
J6
FPGA_CDONE
FPGA_RESET
SPI_MISO
SPI_MOSI
SPI_SCK
R62
10K
SPI_SSEL_N
JP2
Jumper_2_Open
U9C
IC74HC00
SD_SSEL_N
U9A
IC74HC00
U9D
IC74HC00
FLASH_SSEL_N
U9B
IC74HC00
U8
74CBTLV3126PW,118
SD_CS0
SD_MOSI
SD_SCK
SD_MISO
C27
100nF
DAT3 SD_CS0
CMD SD_MOSI
CLK SD_SCK
DAT0 SD_MISO
R37
47K
R38
47K
R39
47K
R40
47K
R41
47K
C26
4.7uF
J3
CONN_DM3AT-SF-PEJM5
DAT1
VSS
DAT0
CLK
VDD
CMD
DAT3
DAT2
SHIELD
SH
C52
100nF
R42
47K
SWA
SWB
SD/microSD INTERFACE
SPI 16MB FLASH
U10
FLASH_SSEL_N
SPI_SCK
DI(IO0)
DO(IO1)
IO2
IO3
W25Q16JVSNIQ
C29
100nF
R43
47K
R44
47K
IC DAC/AUDIO 24BIT 192K 16TSSOP
U11
ASYSCLK
AUDIO_BCK
AUDIO_LRCK
AUDIO_DATA
MCLK
BCLK
LRCLK
DACDAT
LINEVOUTL
LINEVOUTR
CPCA
CPCB
AVDD
LINEVDD
CPVOUTN
LINEGND
AGND
VMID
AIFMODE
MUTE
WM8524CGEDT
560R
R46
560R
R45
AUDIOL
AUDIOR
C30
1uF
C31
1uF
C32
1uF
C33
1uF
C34
4.7uF
C35
4.7uF
C36
2.2uF
Gianluca Renzi
RetroBit Lab
Sheet: /Vera FPGA flash/
File: vera-fpga-flash.sch
Title: uSD Card and FLASH for FPGA
Size: A4
Date: 2025-09-16
Rev: 1.0
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1
Id: 5/6









Gianluca Renzi	
RetroBit Lab	
Sheet: /PowerSupply/	
File: powersupply.sch	
Title: POWERSUPPLY and USB	
Size: A4	Date: 2025-09-16
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1	Id: 6/6
	Rev: 1.0