Sheet: VeraModule

VERA FPGA

File: vera-fpga.sch

Sheet: BusDecoder

BUS DECODER

File: busdecoder.sch

Sheet: Vera FPGA flash

VERA SPI FLASH
SD CARD INTERFACE

File: vera-fpga-flash.sch

Sheet: CartridgeInterface

CARTRIDGE INTERFACE

File: cartridgeInterface.sch

Sheet: PowerSupply

POWER SUPPLY

File: powersupply.sch

FIDUCIAL TOP

FID3 Fiducial   FID4 Fiducial

FIDUCIAL BOTTOM

FID2 Fiducial   FID1 Fiducial

LOGO1
VERA X16 LOGO

LOGO3
KiCAD DESIGN

LOGO5
ESP32_BOBOARD
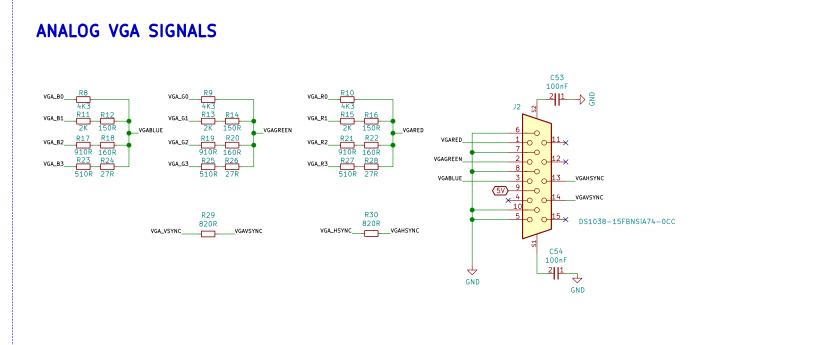
LOGO2
ATARI READY

LOGO4
ATARI DUO BUS

Gianluca Renzi
RetroBit Lab

Sheet: /
File: VERA-MODULE-RBL.sch

Title: VERA FPGA Audio & Video Board

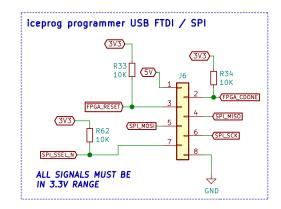| Size: A3	Date: 2025-09-19	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 1/6

FPGA VERA LOGIC VIDEO & AUDIO CARD

U2A — ICE40UP5K-SG48ITR

```
C4 1uF
3V3 — C4 — GND
VCCIO_0 (33)

U2A
25  mD2 — IOT_36b
23  mD3 — IOT_37a
27  mD0 — IOT_38b
26  mD1 — IOT_39a
28  mVCC50 — IOT_41a
31  mWE — IOT_42b
32       — IOT_43a
34  mA4 — IOT_44b
37  mA2 — IOT_45a_G1
35       — IOT_46b_G0
36  mRE — IOT_48b
43       — IOT_49a
38  VAUDIO_LRCK — IOT_50b
42  VAUDIO_BCK — IOT_51a
    VAUDIO_DATA
39  mA1 — RGB0
40  mA0 — RGB1
41  mA3 — RGB2

3V3 — R65 10K
mVIRQ
VSYSCLK
```
ICE40UP5K-SG48ITR

U2B — ICE40UP5K-SG48ITR

```
C5 1uF
3V3 — R5 10K      3V3 — C5 — GND    3V3 — R63 10K

U2B
FPGA_RESET 8 — CRESET
SPI_VCCIO1 — CDONE 7 — VFPGA_DONE

6   VGA_G2 — IOB_13b
9   VGA_G3 — IOB_16a
10  VGA_R0 — IOB_18a
11  VGA_R1 — IOB_20a
12  VGA_R2 — IOB_22b
21  mD4 — IOB_23b
13  VGA_R3 — IOB_24a
20  mD5 — IOB_25b_G3
19  mD6 — IOB_29b
18  mD7 — IOB_31b
14  VSPI_MOSI — IOB_32a_SPI_SO
17  VSPI_MISO — IOB_33b_SPI_SI
15  VSPI_SCK — IOB_34a_SPI_SCK
16  VSPI_SSEL — IOB_35b_SPI_SS
```
ICE40UP5K-SG48ITR

U2C — ICE40UP5K-SG48ITR

```
C6 1uF
3V3 — C6 — GND

U2C
VCCIO_2
46  VGA_B0 — IOB_0a
47  VGA_B1 — IOB_2a
44  VGA_HSYNC — IOB_3b_G6
48  VGA_B2 — IOB_4a
45  VGA_VSYNC — IOB_5b
2   VGA_B3 — IOB_6a
4   VGA_G1 — IOB_8a
3   VGA_G0 — IOB_9b
```
ICE40UP5K-SG48ITR

U2D — ICE40UP5K-SG48ITR

```
C59 1uF    1V2
3V3 — C59 — GND

U2D
24  VPP_2V5
30  VCC
5   VCC
29  VCCPLL
         GND 49

C7 1uF   C8 1uF   C60 1uF
GND

C3 1uF — GND

X1
ST  VDD
GND  OUT 3 — R3 50R — VSYSCLK
       — R4 50R — ASYSCLK
ECS-2033-250-BN
25 MHz
3V3
GND
```

Net labels
```
VSPI_SSEL — SPI_SSEL_N      VFPGA_DONE — FPGA_CDONE
VSPI_SCK  — SPI_SCK         FPGA_RESET — FPGA_RESET
VSPI_MISO — SPI_MISO        VAUDIO_DATA — AUDIO_DATA
VSPI_MOSI — SPI_MOSI        VAUDIO_LRCK — AUDIO_LRCK
                           VAUDIO_BCK  — AUDIO_BCK
```

ANALOG VGA SIGNALS

```
VGA_B0 — R8 4K3
VGA_B1 — R11 2K — R12 150R
VGA_B2 — R17 910R — R18 160R        VGABLUE
VGA_B3 — R23 510R — R24 27R

VGA_G0 — R9 4K3
VGA_G1 — R13 2K — R14 150R
VGA_G2 — R19 910R — R20 160R        VGAGREEN
VGA_G3 — R25 510R — R26 27R

VGA_R0 — R10 4K3
VGA_R1 — R15 2K — R16 150R
VGA_R2 — R21 910R — R22 160R        VGARED
VGA_R3 — R27 510R — R28 27R

VGA_VSYNC — R29 820R — VGAVSYNC
VGA_HSYNC — R30 820R — VGAHSYNC
```

```
C53 100nF — GND

J2
VGARED    6
VGAGREEN  7  11
VGABLUE   1  2
          8  12
          9  3
          4  13  VGAHSYNC
5V        10 14  VGAVSYNC
          5  15
DS1038-15FBNSIA74-0CC

C54 100nF — GND
GND
```

VERA FPGA PROGRAMMED OK

```
R1 2K7    LD2 GREEN
                    3V3
"VERA READY"
Internal LED

VFPGA_DONE 1 — Q1
MOSFET-BSS138-SOT-23
GND
```

EXTERNAL VIDEO CONNECTOR

```
J1
VGARED    1  2  VGAGREEN
VGABLUE   3  4  3V3
GND       5  6  GND
          7  8
5V        9  10
AUDIOL    11 12 AUDIOR
          13 14
VGAHSYNC  15 16 VGAVSYNC
5V              3V3
```
EXTERNAL DISPLAY WITH AUDIO

Iceprog programmer USB FTDI / SPI

```
3V3            3V3
R33 10K   5V   R34 10K

J6
           1  2  FPGA_CDONE
FPGA_RESET 3  4  SPI_MISO
SPI_MOSI   5  6  SPI_SCK
3V3 — R62 10K
SPI_SSEL_N 7  8
GND
```
ALL SIGNALS MUST BE
IN 3.3V RANGE

PBI Bus Interface Decoder:
$D1XX, $D1FF, MPD, $D8XX−$DFXX, EX(T)SEL

PBI DEVICE ID: software selectable only

U7
ESP32−PICO−D4

Pin	Left
1	VDDA
2	LNA_IN
3	VDDA3P3
4	VDDA3P3
5	SENSOR_VP/GPIO36/ADC1_CH0/RTC_GPIO0
6	SENSOR_CAPP/GPIO37/ADC1_CH1/RTC_GPIO1
7	SENSOR_CAPN/GPIO38/ADC1_CH2/RTC_GPIO2
8	SENSOR_VN/GPIO39/ADC1_CH3/RTC_GPIO3
9	EN
10	IO34/GPIO34/ADC1_CH6/RTC_GPIO4
11	IO35/GPIO35/ADC1_CH7/RTC_GPIO5
12	IO32/GPIO32/32K_XP/ADC1_CH4/TOUCH9/RTC_GPIO9
13	IO33/GPIO33/32K_XN/ADC1_CH5/TOUCH8/RTC_GPIO8
14	IO25/GPIO25/DAC_1/ADC2_CH8/RTC_GPIO6/EMAC_RXD0
15	IO26/GPIO26/DAC_2/ADC2_CH9/RTC_GPIO7/EMAC_RXD1
16	IO27/GPIO27/ADC2_CH7/TOUCH7/RTC_GPIO17/EMAC_RX_DV
17	IO14/GPIO14/ADC2_CH6/TOUCH6/RTC_GPIO16/MTMS/HSPICLK/HS2_CLK/SD_CLK/EMAC_TXD2
18	IO12/GPIO12/ADC2_CH5/TOUCH5/RTC_GPIO15/MTDI/HSPIQ/HS2_DATA2/SD_DATA2/EMAC_TXD3
19	VDD3P3_RTC
20	IO13/GPIO13/ADC2_CH4/TOUCH4/RTC_GPIO14/MTCK/HSPID/HS2_DATA3/SD_DATA3/EMAC_RX_ER
21	IO15/GPIO15/ADC2_CH3/TOUCH3/RTC_GPIO13/MTDO/HSPICS0/HS2_CMD/SD_CMD/EMAC_RXD3
22	IO2/GPIO2/ADC2_CH2/TOUCH2/RTC_GPIO12/HSPIWP/HS2_DATA0/SD_DATA0
23	IO0/GPIO0/ADC2_CH1/TOUCH1/RTC_GPIO11/CLK_OUT1/EMAC_TX_CLK
24	IO4/GPIO4/ADC2_CH0/TOUCH0/RTC_GPIO10/HSPIHD/HS2_DATA1/SD_DATA1/EMAC_TX_CLK

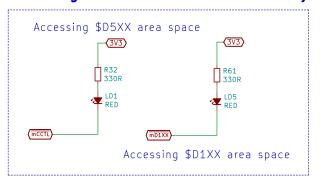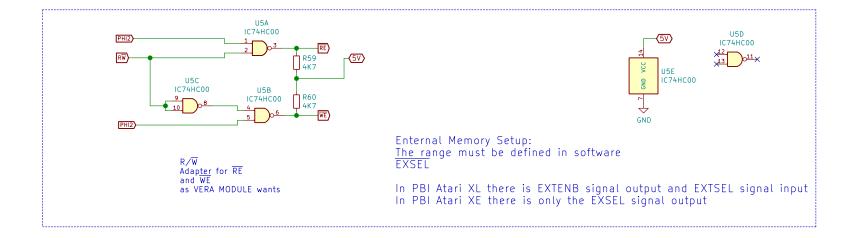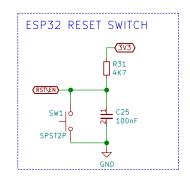| Pin	Right
48	CAP1_NC
47	CAP2_NC
46	VDDA
45	XTAL_P_NC
44	XTAL_N_NC
43	VDDA
42	IO21/GPIO21/VSPIHD/EMAC_TX_EN
41	U0TXD/GPIO1/U0TXD/CLK_OUT3/EMAC_RXD2
40	U0RXD/GPIO3/U0RXD/CLK_OUT2
39	IO22/GPIO22/VSPIWP/U0RTS/EMAC_TXD1
38	IO19/GPIO19/VSPIQ/U0CTS/EMAC_TXD0
37	VDD3P3_CPU
36	IO23/GPIO23/VSPID/HS1_STROBE
35	IO18/GPIO18/VSPICLK/HS1_DATA7
34	IO5/GPIO5/VSPICS0/HS1_DATA6/EMAC_RX_CLK
33	SD1/GPIO8/SD_DATA1/SPID/HS1_DATA1/U2CTS
32	SD0/GPIO7/SD_DATA0/SPIQ/HS1_DATA0/U2RTS
31	CLK/GPIO6/SD_CLK/SPICLK/HS1_CLK/U1CTS
30	CMD/GPIO11/SD_CMD/SPICS0/HS1_CMD/U1RTS
29	SD3/GPIO10/SD_DATA3/SPIWP/HS1_DATA3/U1TXD
28	SD2/GPIO9/SD_DATA2/SPIHD/HS1_DATA2/U1RXD
27	IO17/GPIO17/HS1_DATA5/U2TXD/EMAC_CLK_OUT_180
26	VDD_SDIO
25	IO16/GPIO16/HS1_DATA4/U2RXD/EMAC_CLK_OUT
49	GND

mVCS0 active & A15..A0 $D8XX−$DFXX −> MPD active (Internal 2K ROM)

$D1FF access & DATABUS = PBI DEVICE ID −> mVCS0 active/deactive
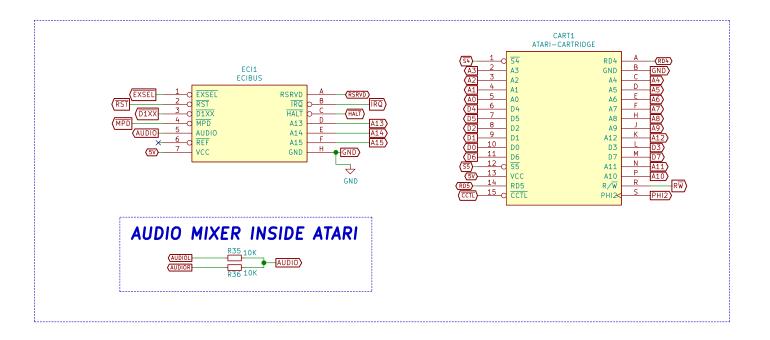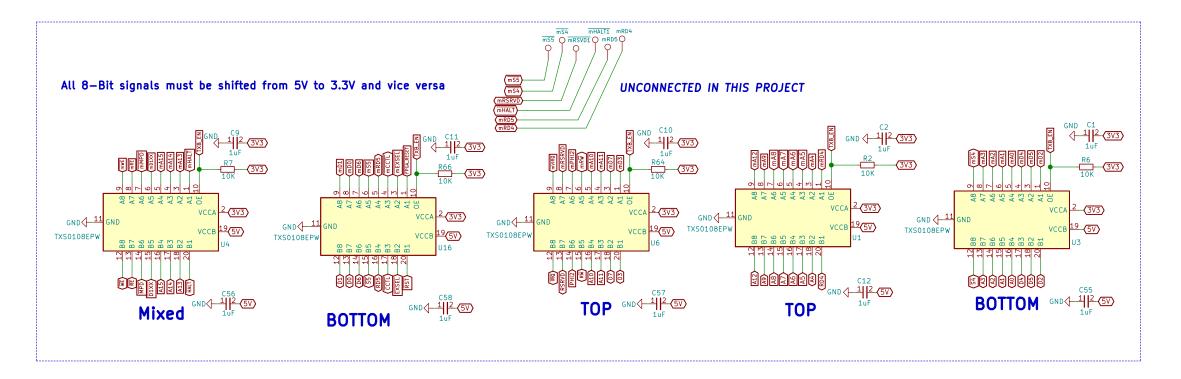
Those signals are valid in ATARI XE only

Accessing $D5XX area space

R32 330R
LD1 RED
mCCTL

R61 330R
LD5 RED
mD1XX

Accessing $D1XX area space

U5A IC74HC00
U5C IC74HC00
U5B IC74HC00
R59 4K7
R60 4K7
PHI2
RW
RE
WE

R/W Adapter for RE and WE as VERA MODULE wants

U5D IC74HC00
U5E IC74HC00

Enternal Memory Setup:
The range must be defined in software
EXSEL

In PBI Atari XL there is EXTENB signal output and EXTSEL signal input
In PBI Atari XE there is only the EXSEL signal output

ESP32 RESET SWITCH

R31 4K7
RST\EN
SW1
SPST2P
C25 100nF

Capacitors: C13 10uF, C14 100nF, C17 10uF, C18 100nF, C15 10uF, C16 100nF, C23 100nF, C24 10uF, C19 10uF, C20 100nF, C21 10uF, C22 100nF

L1 FB0805100R100MHZ4A

ATARI 130XE ECI & CARTRIDGE INTERFACE

ECI1
ECIBUS

Pin	Signal		Signal
1	EXSEL	RSRVD	A
2	RST	IRQ	B
3	D1XX	HALT	C
4	MPD	A13	D
5	AUDIO	A14	E
6	REF	A15	F
7	VCC	GND	H

CART1
ATARI-CARTRIDGE

Pin	Signal		Signal	Pin
1	S4	RD4	A
2	A3	GND	B
3	A2	A4	D
4	A1	A5	E
5	A0	A6	F
6	D4	A7	H
7	D5	A8	J
8	D2	A9	K
9	D1	A12	L
10	D0	D3	M
11	D6	D7	N
12	S5	A11	P
13	VCC	A10	R
14	RD5	R/W	S
15	CCTL	PHI2	T

AUDIO MIXER INSIDE ATARI

R35 10K
AUDIOL

R36 10K
AUDIOR

AUDIO

BUS LOGIC LEVEL SHIFTERS

All 8-Bit signals must be shifted from 5V to 3.3V and vice versa

mS5 mS4 mRSVD1 mHALT1 mRD4
mRD5

mS5
mS4
mRSVD
mHALT
mRD5
mRD4

UNCONNECTED IN THIS PROJECT

C9 1uF 3V3
R7 10K 3V3
TXS0108EPW U4
C56 1uF 5V
Mixed

C11 1uF 3V3
R66 10K 3V3
TXS0108EPW U16
C58 1uF 5V
BOTTOM

C10 1uF 3V3
R64 10K 3V3
TXS0108EPW U6
C57 1uF 5V
TOP

C2 1uF 3V3
R2 10K 3V3
TXS0108EPW U1
C12 1uF 5V
TOP

C1 1uF 3V3
R6 10K 3V3
TXS0108EPW U3
C55 1uF 5V
BOTTOM

FPGA/SSD Flash Glue Logic

When programming SPI FLASH for bitstream, the JP2 jumper must be closed. Should be open in a normal operational mode.

JP2
Jumper_2_Open

U9E IC74HC00
U9C IC74HC00 — SD_SSEL_N
U9A IC74HC00
U9D IC74HC00 — FLASH_SSEL_N
U9B IC74HC00

C28 100nF

FPGA_CDONE
SPI_SSEL_N

SD/microSD INTERFACE

U8
74CBTLV3126PW,118

SD_SSEL_N — 1A
SPI_MOSI — 2A
SPI_SCK — 3A
SPI_MISO — 4A
1B — SD_CS0
2B — SD_MOSI
3B — SD_SCK
4B — SD_MISO

1OE
2OE
3OE
FPGA_CDONE — 4OE

C27 100nF

C26 4.7uF

R37 47K
R38 47K
R39 47K
R40 47K
R41 47K

R42 47K

J3 CONN_DM3AT-SF-PEJM5

DAT1
VSS/GND
DAT0
CLK
VDD
CMD
CD/DAT3
DAT2
SHIELD — SH

C52 100nF

The microSD BUS will be available only when FPGA is ready and programmed

DAT3 ___ SD_CS0
CMD ___ SD_MOSI
CLK ___ SD_SCK
DAT0 ___ SD_MISO

AUDIO SECTION

IC DAC/AUDIO 24BIT 192K 16TSSOP

U11

ASYSCLK — MCLK
AUDIO_BCK — BCLK
AUDIO_LRCK — LRCLK
AUDIO_DATA — DACDAT

MCLK
BCLK
LRCLK
DACDAT

LINEVOUTL
LINEVOUTR
CPCA
CPCB
AVDD
LINEVDD
CPVOUTN
LINEGND
AGND
VMID

AIFMODE
MUTE

R46 560R
R45 560R

C30 1uF
C31 1uF

C32 1uF
C33 1uF
C34 4.7uF
C35 4.7uF
C36 2.2uF

AUDIOL
AUDIOR

WM8524CGEDT

AUDIO 3.5mm OUTPUT

AUDIOL — R67 560R
AUDIOR — R68 560R

J7
SJ-3523-SMT-TR

SPI 16MB FLASH

U10

FLASH_SSEL_N — CS
SPI_SCK — CLK

VCC
DI(IO0) — SPI_MOSI
DO(IO1) — SPI_MISO
IO2
IO3
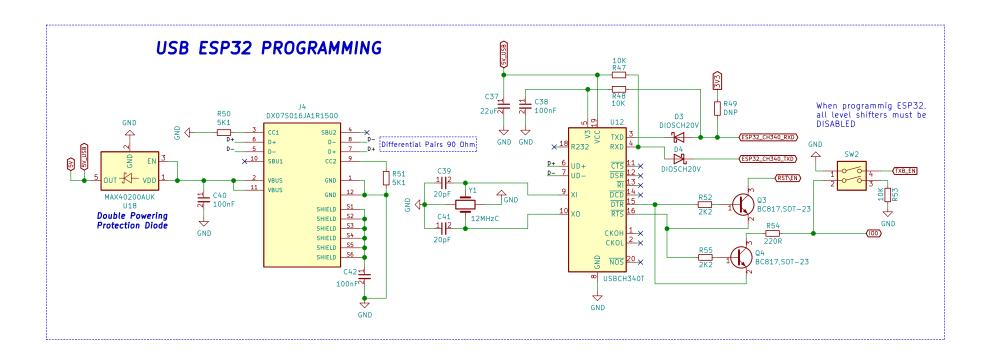
C29 100nF

R43 47K
R44 47K
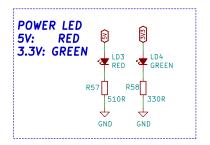
W25Q16JVSNIQ

Gianluca Renzi
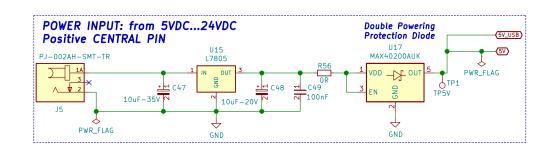**RetroBit Lab**
Sheet: /Vera FPGA flash/
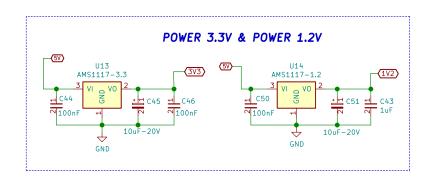File: vera-fpga-flash.sch
Title: uSD Card and FLASH for FPGA
Size: A3   Date: 2025-09-19   Rev: 1.0
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1   Id: 5/6

USB ESP32 PROGRAMMING

J4
DX07S016JA1R1500

R50
5K1

R51
5K1

MAX40200AUK
U18

**Double Powering
Protection Diode**

C40
100nF

C42
100nF

Differential Pairs 90 Ohm

C37
22uF

C38
100nF

10K
R47

R48
10K

U12
R232

D3
DIOSCH20V

D4
DIOSCH20V

R49
DNP

ESP32_CH340_RXD

ESP32_CH340_TXD

When programmig ESP32,
all level shifters must be
DISABLED

SW2

RST\EN

C39
20pF

Y1
12MHzC

C41
20pF

R52
2K2

Q3
BC817,SOT-23

R54
220R

100

R55
2K2

Q4
BC817,SOT-23

10K
R53

TXB_EN

USBCH340T

POWER LED
5V: RED
3.3V: GREEN

LD3
RED

LD4
GREEN

R57
510R

R58
330R

POWER INPUT: from 5VDC...24VDC
Positive CENTRAL PIN

PJ-002AH-SMT-TR

U15
L7805

C47
10uF-35V

C48
10uF-20V

R56
0R

C49
100nF

**Double Powering
Protection Diode**

U17
MAX40200AUK

TP1
TP5V

5V_USB

5V

PWR_FLAG

J5

PWR_FLAG

POWER 3.3V & POWER 1.2V

5V

U13
AMS1117-3.3

C44
100nF

C45
10uF-20V

C46
100nF

3V3

5V

U14
AMS1117-1.2

C50
100nF

C51
10uF-20V

C43
1uF

1V2