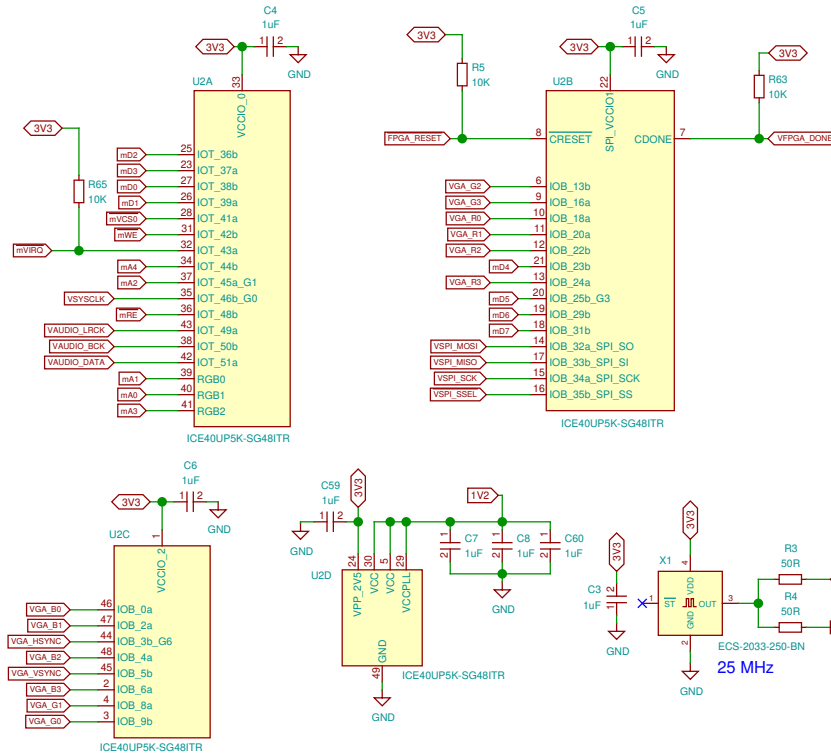
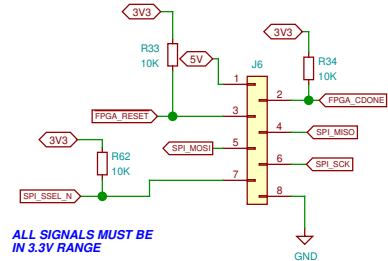


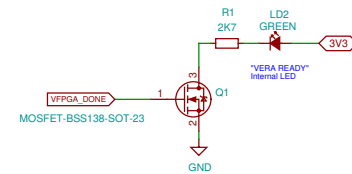
## FPGA VERA LOGIC VIDEO & AUDIO CARD



## iceprog programmer USB FTDI / SPI



**VERA FPGA PROGRAMMED OK**



Gianluca Renzi

RetroBit Lab

Sheet: /VeraModule/

File: vera-fpga.sch

Title: VeraModule

Size: A4

Date: 2025-10-27

Rev: 1.0

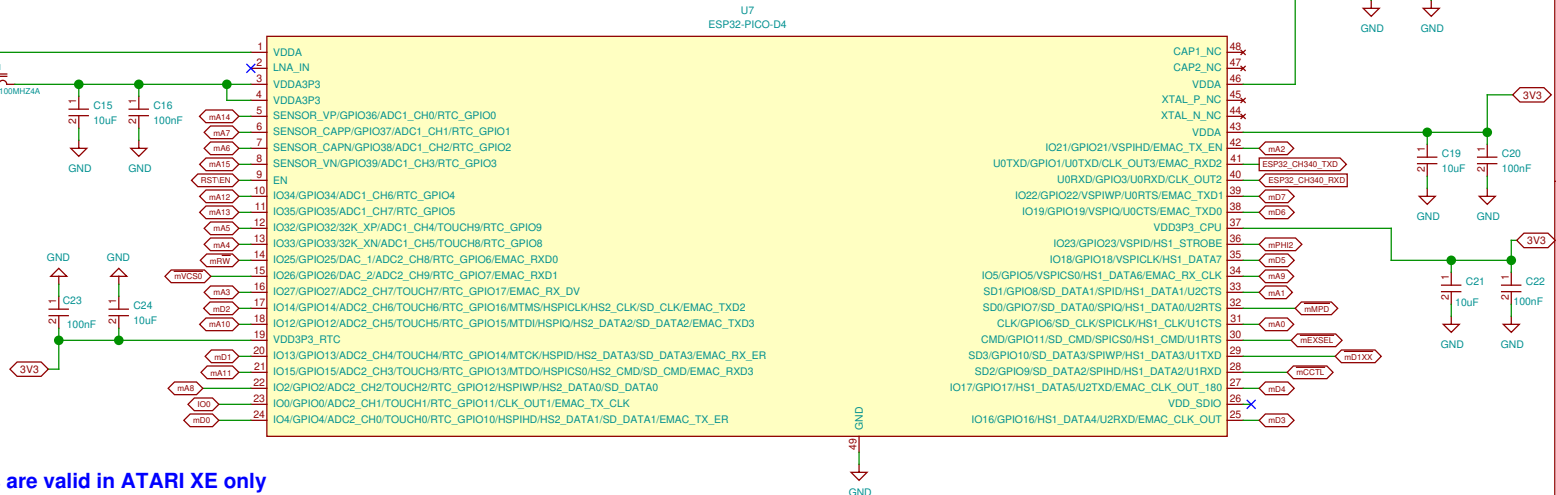
Plotted by eeshow 3a954ac 20251029-15:26Z

Id: 2/7

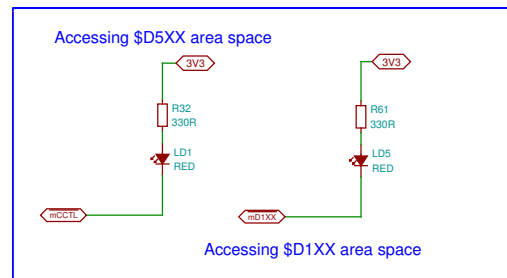
**PBI Bus Interface Decoder:**  
**\$D1XX, \$D1FF, MPD, \$D8XX-\$DFXX, EX(T)SEL**

**PBI DEVICE ID: software selectable only**

U7  
ESP32-PICO-D4



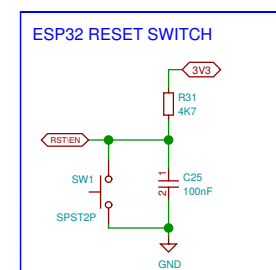
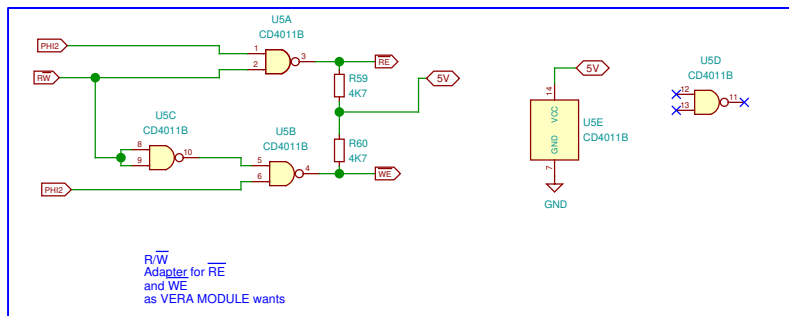
**Those signals are valid in ATARI XE only**



**Internal Memory Setup:**  
**The range must be defined in software**  
**EXSEL**

In PBI Atari XL there is EXTENB signal output and EXTSEL signal input  
 In PBI Atari XE there is only the EXSEL signal output

mVCS0 active & A15..A0 \$D8XX-\$DFXX -> MPD active (Internal 2K ROM)  
 \$D1FF access & DATABUS = PBI DEVICE ID -> mVCS0 active/deactive



Gianluca Renzi  
 RetroBit Lab

Sheet: /BusDecoder/  
 File: busdecoder.sch

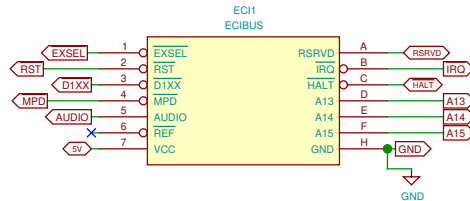
**Title: BusDecoder**

Size: A4 Date: 2025-10-27  
 Plotted by eeshow 3a954ac 20251029-15:26Z

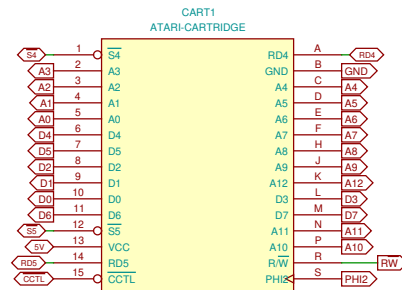
Rev: 1.0  
 Id: 3/7

# ATARI 130XE ECI & CARTRIDGE INTERFACE

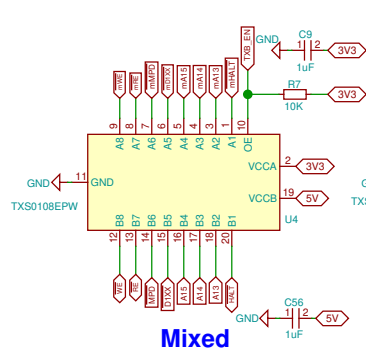
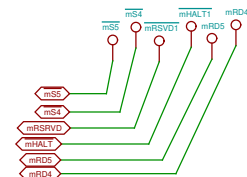
All 8-Bit signals must be shifted from 5V to 3.3V and vice versa



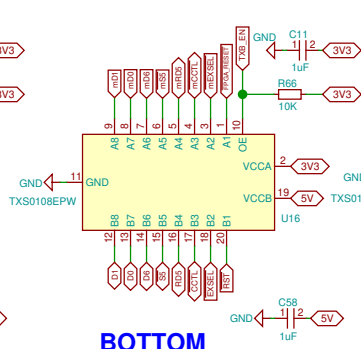
## AUDIO MIXER INSIDE ATARI



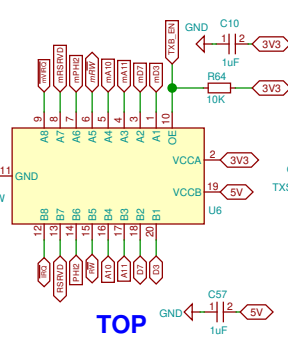
UNCONNECTED IN THIS PROJECT



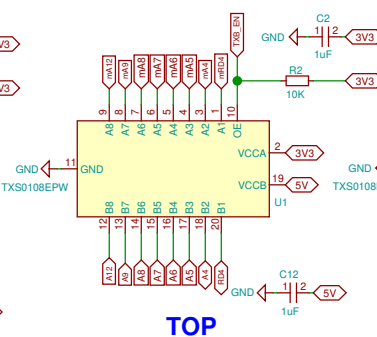
Mixed



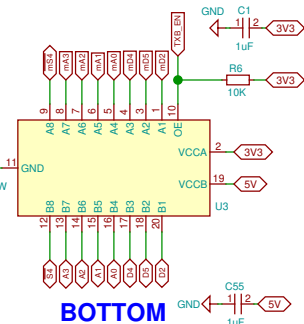
BOTTOM



TOP



TOP



BOTTOM

## BUS LOGIC LEVEL SHIFTERS

Gianluca Renzi

RetroBit Lab

Sheet: /CartridgeInterface/

File: cartridgeInterface.sch

Title: CartridgeInterface

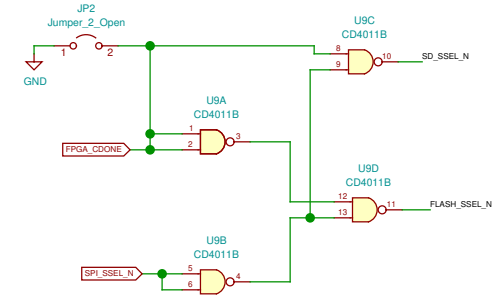
Size: A4

Date: 2025-10-27

Rev: 1.0

Plotted by eeshow 3a954ac 20251029-15:26Z

Id: 4/7

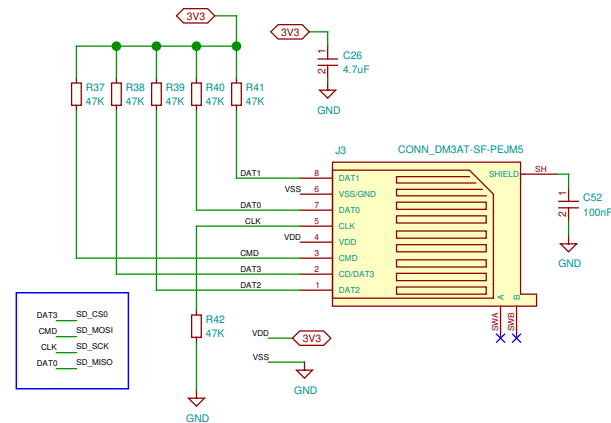
[illegible]

UB  
74CBT1V2125PW:118

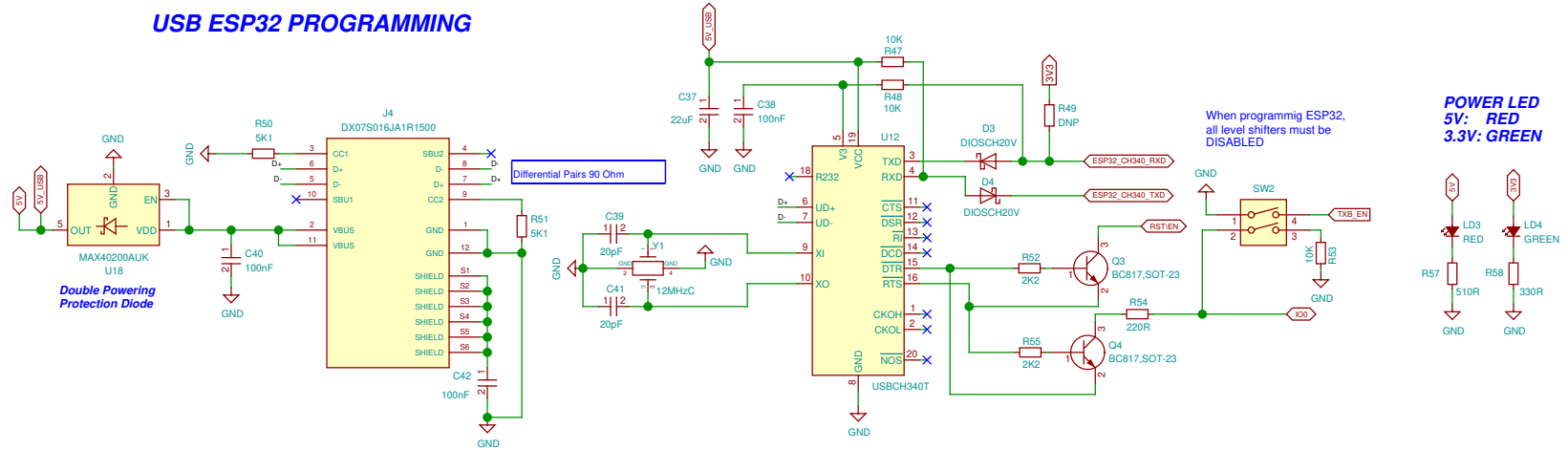
Pin	Signal	Pin	Signal
1	3V3	9	SPI_SCK
2	SD_SSEL_N	10	FPGA_CDONE
3	SD_CS	11	SD_MISO
4	SPI_MOSI	12	SD_MISO
5	SPI_MISO	13	VCC
6	SD_MOSI	14	VCC
7	SD_SCK	15	GND
8	SD_CS	16	3V3

C27  
100nF

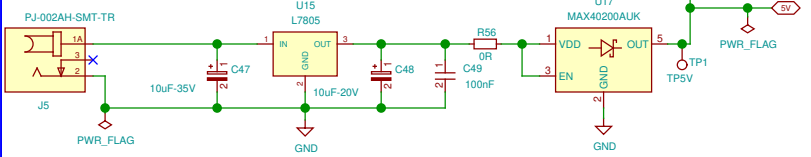
The microSD BUS will be available only when FPGA is ready and programmed



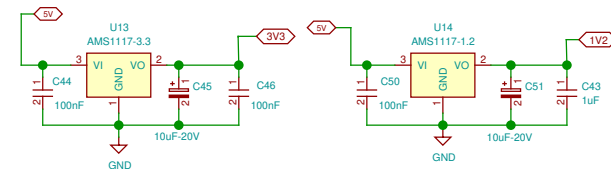
## USB ESP32 PROGRAMMING



**POWER INPUT: from 5VDC...24VDC**  
**Positive CENTRAL PIN**



**POWER 3.3V & POWER 1.2V**



Gianluca Renzi  
RetroBit Lab

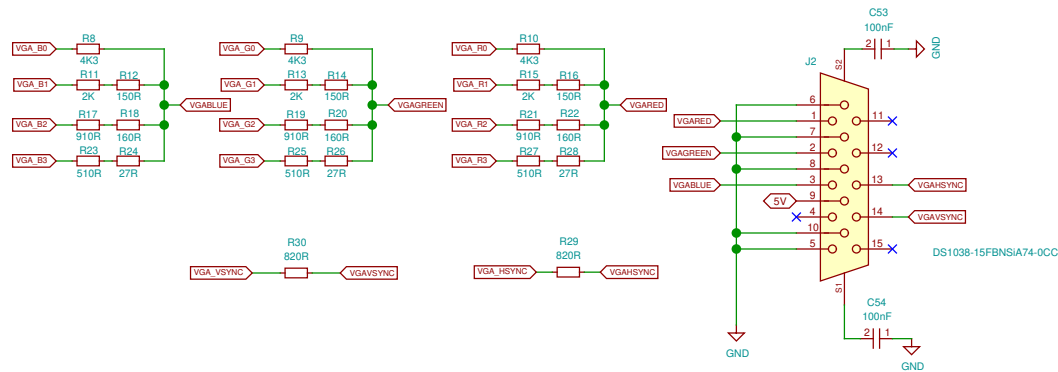
Sheet: /PowerSupply/  
File: powersupply.sch

Title: PowerSupply

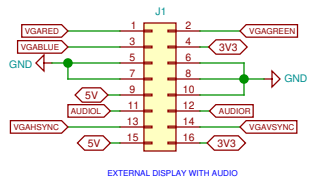
Size: A4	Date: 2025-10-27
Plotted by eeshow 3a954ac 20251029-15:26Z	

Rev: 1.0
Id: 6/7

## ANALOG VGA SIGNALS



## EXTERNAL VIDEO CONNECTOR



Gianluca Renzi  
RetroBit Lab

Sheet: /VGA Analog/  
File: vga-analog.sch

Title: VGA Analog

Size: A4 Date: 2025-10-27  
Plotted by eeshow 3a954ac 20251029-15:26Z

Rev: 1.0  
Id: 7/7