

Sheet: VeraModule

VERA FPGA

File: vera-fpga.sch

Sheet: BusDecoder

BUS DECODER

File: busdecoder.sch

Sheet: Vera FPGA flash

VERA SPI FLASH  
SD CARD INTERFACE

File: vera-fpga-flash.sch

Sheet: CartridgeInterface

CARTRIDGE INTERFACE

File: cartridgeInterface.sch

Sheet: PowerSupply

POWER SUPPLY

File: powersupply.sch

FIDUCIAL TOP



FIDUCIAL BOTTOM



LOGO1  
VERA X16 LOGO

Gianluca Renzi  
**RetroBit Lab**

Sheet: /  
File: VERA-MODULE-RBL.sch

**Title: VERA FPGA Audio & Video Board**

Size: A4	Date: 2025-09-08	Rev: 1.0
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 1/6

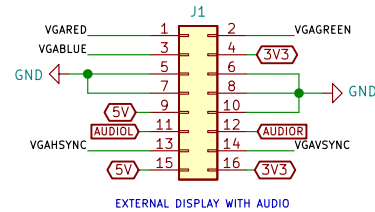
# EXTERNAL VIDEO CONNECTOR

The diagram illustrates the pin configuration for an external video connector, labeled J1. The connector has 16 pins arranged in two rows of 8. The connections are as follows:

- Pin 1:** VGARED
- Pin 2:** VGAGREEN
- Pin 3:** VGBLUE
- Pin 4:** 3V3 (Power)
- Pin 5:** GND (Ground)
- Pin 6:** 3V3 (Power)
- Pin 7:** GND (Ground)
- Pin 8:** 3V3 (Power)
- Pin 9:** 5V (Power)
- Pin 10:** 5V (Power)
- Pin 11:** AUDIOL (Audio Left)
- Pin 12:** AUDIOR (Audio Right)
- Pin 13:** 5V (Power)
- Pin 14:** 5V (Power)
- Pin 15:** 5V (Power)
- Pin 16:** 3V3 (Power)

Additional labels include VGAREDB, VGBLUEB, and VGBLUEC, which are connected to pins 1, 3, and 5 respectively. The diagram also shows a GND symbol connected to pin 5 and a 3V3 symbol connected to pin 4.

EXTERNAL DISPLAY WITH AUDIO



# FPGA VERA LOGIC VIDEO & AUDIO CARD

The image displays four circuit diagrams for an FPGA VERA Logic Video & Audio Card, showing the connections for the VCCIO pins of the ICE40UP5K-SG48ITR chips.

**Top Left Diagram (U2A):** Shows the VCCIO\_0 pin of U2A connected to various I/O pins (mD2, mD3, mD0, mD1, mVC50, mWE, mVIRQ, mA4, mA2, VSYSCLK, mRE, VAUDIO\_LRCK, VAUDIO\_BCK, VAUDIO\_DATA, mA1, mA0, mA3) and power pins (VCCIO\_0, GND).

**Top Right Diagram (U2B):** Shows the VCCIO1 pin of U2B connected to various I/O pins (VGA\_G2, VGA\_G3, VGA\_R0, VGA\_R1, VGA\_R2, VGA\_R3, mD4, mD5, mD6, mD7, VSPL\_MOSI, VSPL\_MISO, VSPL\_SCK, VSPL\_SSEL) and power pins (VCCIO1, GND).

**Bottom Left Diagram (U2C):** Shows the VCCIO\_2 pin of U2C connected to various I/O pins (VGA\_B0, VGA\_B1, VGA\_HSYNC, VGA\_B2, VGA\_B3, VGA\_G1, VGA\_G0) and power pins (VCCIO\_2, GND).

**Bottom Right Diagram (U2D):** Shows the VPP\_2V5 pin of U2D connected to various power pins (VPP\_2V5, VCC, VCC, VCCPLL, GND) and a 3V3 supply. It also shows a 25 MHz clock source (ECS-2033-250-BN) connected to the VSYSCLK and ASYSCLK pins.

# ANALOG VGA SIGNALS

The diagram illustrates the analog VGA signal connections for an ICD15S13E4GX00LF display module. The connections are as follows:

- Red Channel:** VGA\_R0 (4K3) and VGA\_R1 (2K) are connected to R8 (4K3) and R11 (2K). R12 (150R) is connected to the output. VGA\_R2 (910R) and VGA\_R3 (510R) are connected to R17 (910R) and R23 (510R). R18 (160R) and R24 (27R) are connected to the output.
- Green Channel:** VGA\_G0 (4K3) and VGA\_G1 (2K) are connected to R9 (4K3) and R13 (2K). R14 (150R) is connected to the output. VGA\_G2 (910R) and VGA\_G3 (510R) are connected to R19 (910R) and R25 (510R). R20 (160R) and R26 (27R) are connected to the output.
- Blue Channel:** VGA\_B0 (4K3) and VGA\_B1 (2K) are connected to R10 (4K3) and R15 (2K). R16 (150R) is connected to the output. VGA\_B2 (910R) and VGA\_B3 (510R) are connected to R21 (910R) and R27 (510R). R22 (160R) and R28 (27R) are connected to the output.
- Sync Signals:** VGA\_VSYNC (820R) is connected to R29 (820R). VGA\_HSYNC (820R) is connected to R30 (820R).
- Display Module:** The ICD15S13E4GX00LF module has pins 1-15. Pins 11, 12, 13, 14, and 15 are marked with an 'X'. The module is connected to a 5V supply and ground. A 100nF capacitor (C53) is connected between pins 52 and 15. A 100nF capacitor (C54) is connected between pins 15 and ground.
- Other Connections:** VFPGA\_DONE is connected to FPGA\_CDONE. VSPIL\_SSEL is connected to SPI\_SSEL\_N. VSPIL\_SCK is connected to SPI\_SCK. VSPIL\_MISO is connected to SPI\_MISO. VSPIL\_MOSI is connected to SPI\_MOSI. VFPGA\_RESET is connected to FPGA\_RESET. VAUDIO\_DATA is connected to AUDIO\_DATA. VAUDIO\_LRCK is connected to AUDIO\_LRCK. VAUDIO\_BCK is connected to AUDIO\_BCK.

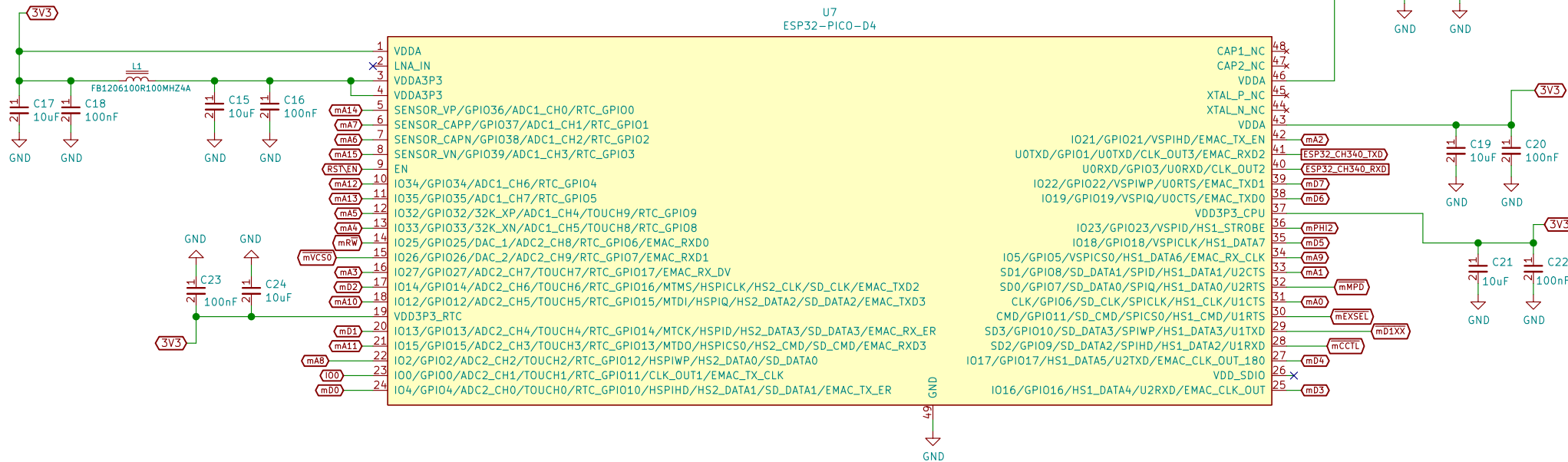
# VERA FPGA PROGRAMMED OK

The diagram shows a MOSFET (BSS138) circuit. The gate is connected to VFGPA\_DONE (pin 1). The drain is connected to a 2K7 resistor (R1) and a green LED (LD2) in series with a 3V3 supply. The LED is labeled "VERA\_READY Internal LED". The source is connected to GND (pin 2).

Id: 2/6

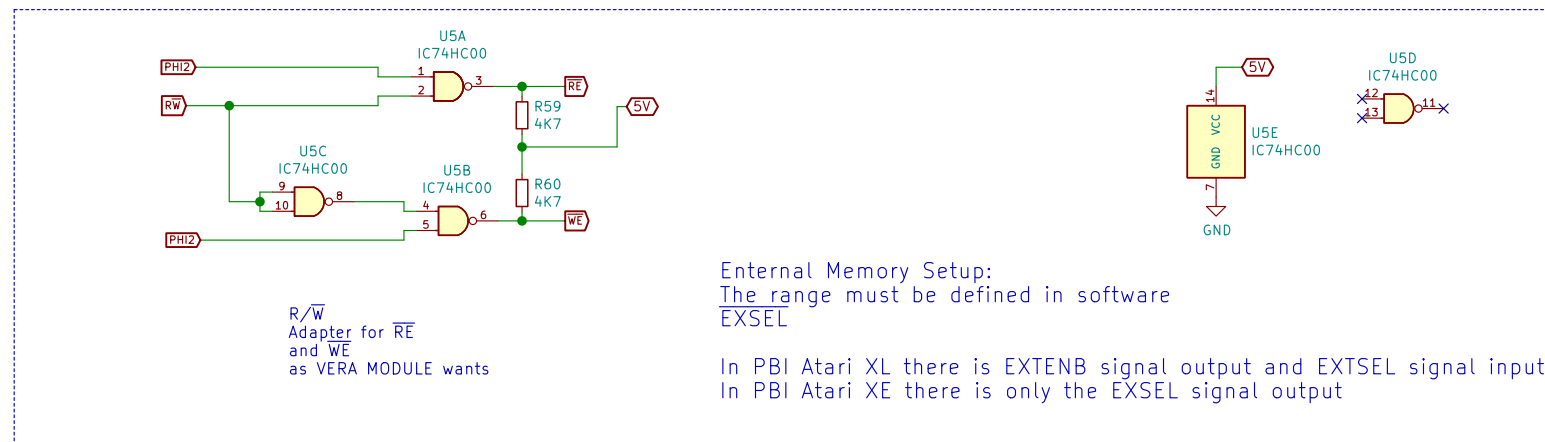
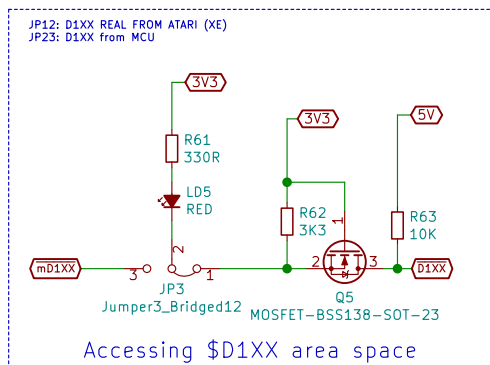
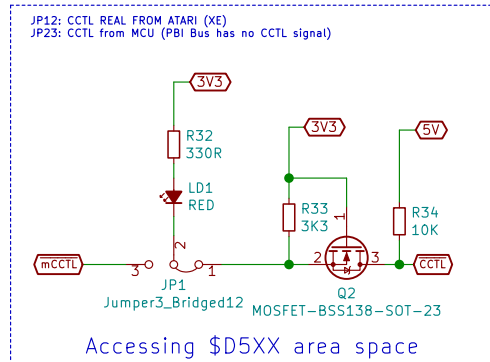
PBI Bus Interface Decoder:  
\$D1XX, \$D1FF, MPD, \$D8XX-\$DFXX, EX(T)SEL

PBI DEVICE ID: software selectable only



mVCS0 active & A15..A0 \$D8XX-\$DFXX -> MPD active (Internal 2K ROM)

\$D1FF access & DATABUS = PBI DEVICE ID -> mVCS0 active/deactive



External Memory Setup:  
The range must be defined in software  
EXSEL

In PBI Atari XL there is EXTENB signal output and EXTSEL signal input  
In PBI Atari XE there is only the EXSEL signal output

Gianluca Renzi

RetroBit Lab

Sheet: /BusDecoder/

File: busdecoder.sch

**Title: VERA FPGA Audio & Video Board**

Size: A3

Date: 2025-09-08

Rev: 1.0

KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1

Id: 3/6

The diagram illustrates the internal components of an Atari 2600 console, specifically focusing on the EC11 IC, the ATARI-CARTRIDGE, and the AUDIO MIXER circuit.

**EC11 IC (ECIBUS):** This integrated circuit is shown with its pins connected to various components. The pins are labeled as follows:

- 1: EXSEL
- 2: RST
- 3: D1XX
- 4: MPD
- 5: AUDIO
- 6: REF
- 7: VCC

The IC also has output pins labeled A through H, which are connected to other components like the ATARI-CARTRIDGE and the AUDIO MIXER.

**ATARI-CARTRIDGE:** This component is shown with its pins connected to the EC11 IC and the console's internal circuitry. The pins are labeled as follows:

- 1: S4
- 2: A3
- 3: A2
- 4: A1
- 5: A0
- 6: D4
- 7: D5
- 8: D2
- 9: D1
- 10: D0
- 11: D6
- 12: S5
- 13: VCC
- 14: RD5
- 15: CCTL

The cartridge also has output pins labeled RD4, GND, A4, A5, A6, A7, A8, A9, A12, D3, D7, A11, A10, R/W, and PH12.

**AUDIO MIXER INSIDE ATARI:** This circuit is shown within a dashed box, indicating it is internal to the console. It consists of two 2K7 resistors (R35 and R36) connected to the AUDIO and AUDIOI pins of the EC11 IC, and the AUDIO pin of the ATARI-CARTRIDGE.

All 8-Bit signals must be shifted from 5V to 3.3V and vice versa

Mixed

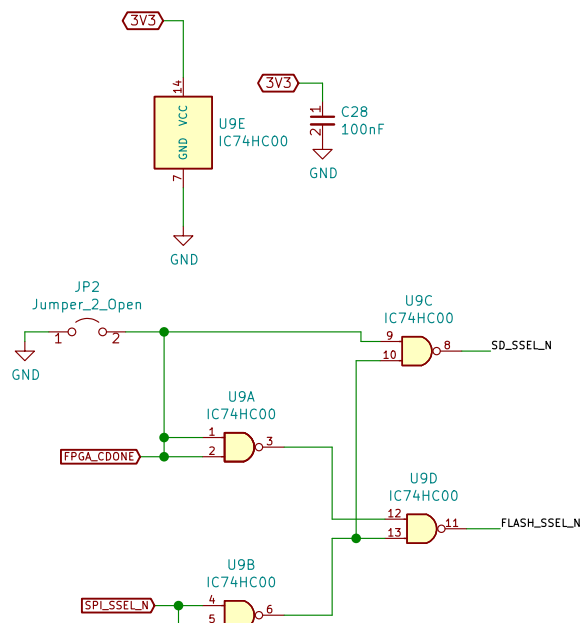
BOTTOM

TOP

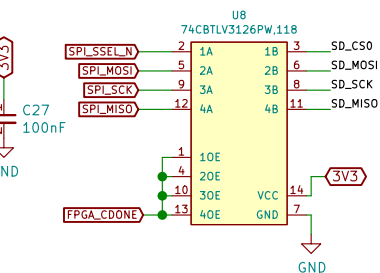
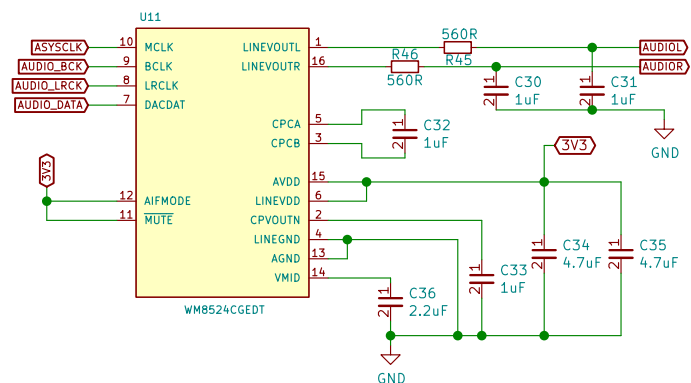
TOP

BOTTOM

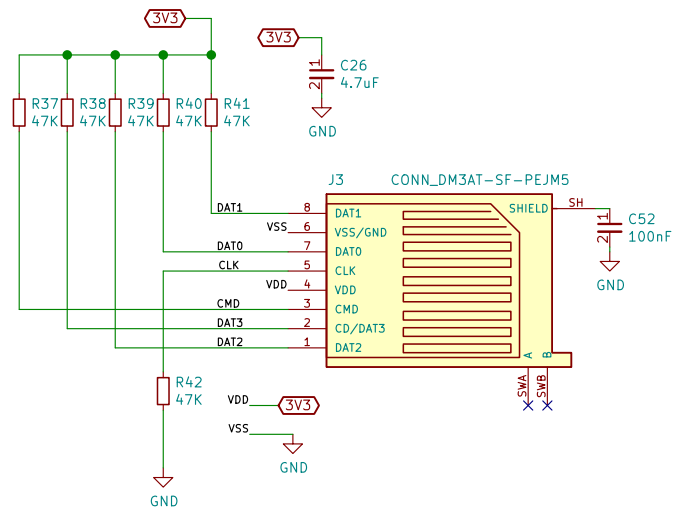
## FPGA/SSD Flash Glue Logic



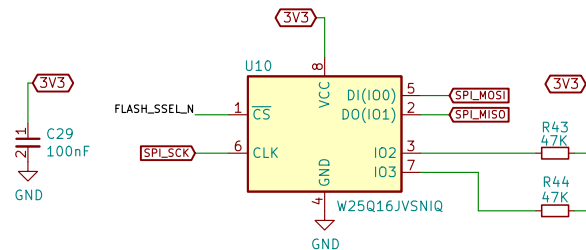
## IC DAC/AUDIO 24BIT 192K 16TSSOP



## SD/microSD INTERFACE



## SPI 16MB FLASH



Gianluca Renzi

**RetroBit Lab**

Sheet: /Vera FPGA flash/

File: vera-fpga-flash.sch

**Title: VERA FPGA Audio & Video Board**

Size: A4 Date: 2025-09-08

KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1

**Rev: 1.0**

Id: 5/6

**USB ESP32 PROGRAMMING**

When programming ESP32,  
all level shifters must be  
DISABLED

**POWER INPUT: from 5VDC...24VDC  
Positive CENTRAL PIN**

**Double Powering Protection Diode**

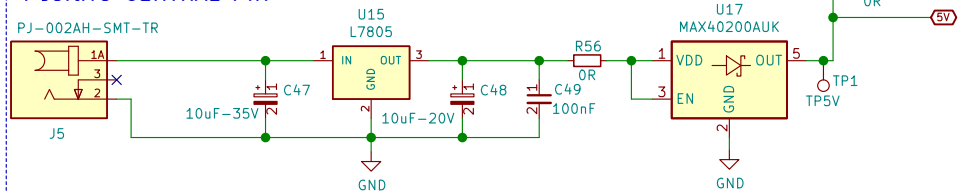
**POWER LED**  
**5V: RED**  
**3.3V: GREEN**

**POWER 3.3V & POWER 2.5V**

Gianluca Renzi  
RetroBit Lab  
Sheet: /PowerSupply/  
File: powersupply.sch  
**Title: VERA FPGA Audio & Video Board**  
Size: A4 Date: 2025-09-08 Rev: 1.0  
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1 Id: 6/6

When programming ESP32,  
all level shifters must be  
DISABLED

### Double Powering Protection Diode



Rev: 1.0  
Id: 6/6