

Sheet: VeraModule

VERA FPGA

File: vera-fpga.sch

Sheet: BusDecoder

BUS DECODER

File: busdecoder.sch

Sheet: Vera FPGA flash

VERA SPI FLASH  
SD CARD INTERFACE

File: vera-fpga-flash.sch

Sheet: CartridgeInterface

CARTRIDGE INTERFACE

File: cartridgeInterface.sch

Sheet: PowerSupply

POWER SUPPLY

File: powersupply.sch

FIDUCIAL TOP

FID3  
Fiducial

FID4  
Fiducial

FIDUCIAL BOTTOM

FID2  
Fiducial

FID1  
Fiducial

LOGO1  
VERA X16 LOGO

LOGO2  
ATARI READY

LOGO3  
KICAD DESIGN

LOGO4  
ATARI DUO BUS

LOGO5  
ESP32\_B0BOARD

Gianluca Renzi  
**RetroBit Lab**

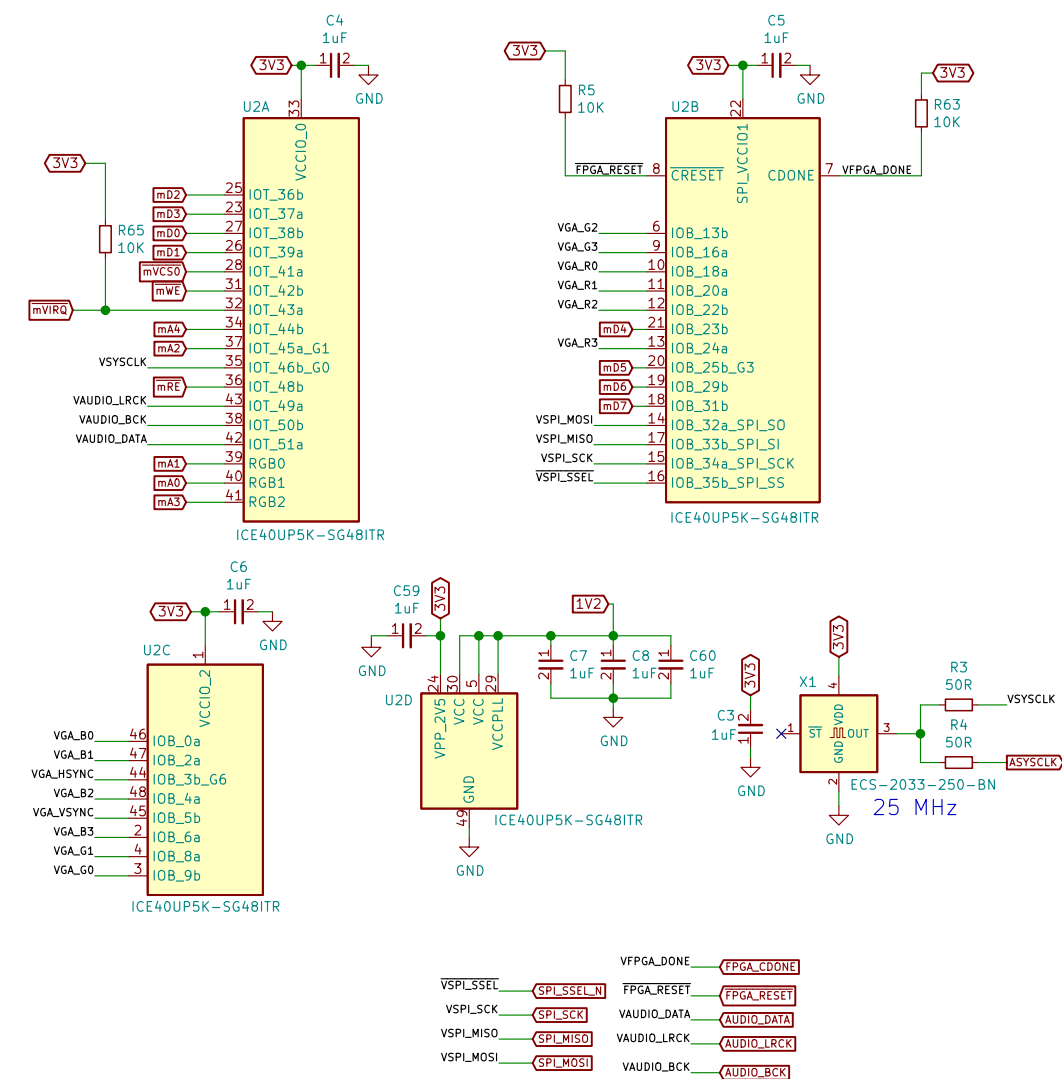
Sheet: /  
File: VERA-MODULE-RBL.sch

**Title: VERA FPGA Audio & Video Board**

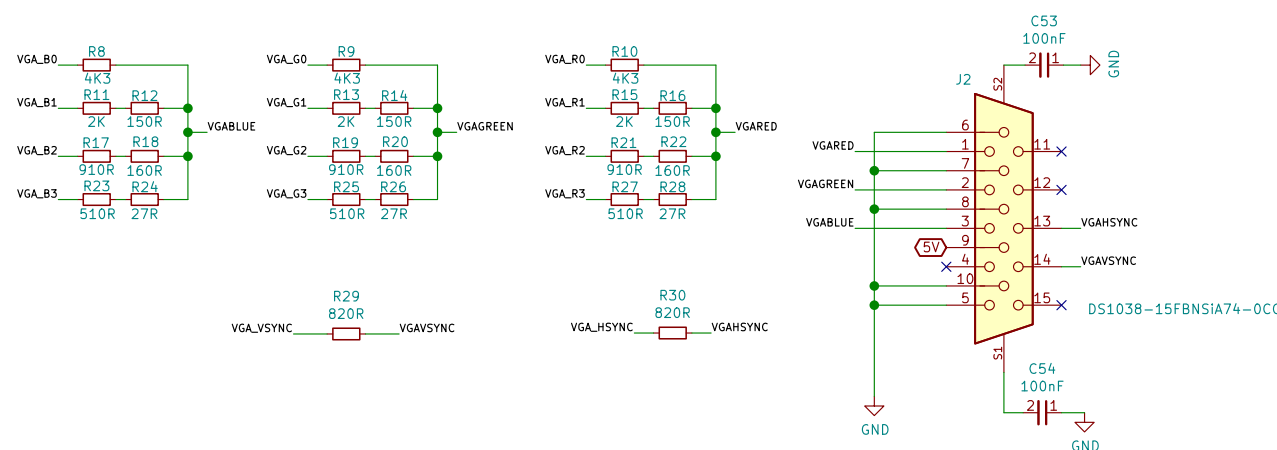
Size: A3      Date: 2025-09-17  
KiCad E.D.A.    kicad 5.1.9+dfsg1-1+deb11u1

**Rev: 1.0**  
Id: 1/6

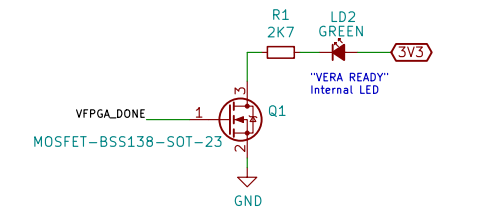
FPGA VERA LOGIC VIDEO & AUDIO CARD



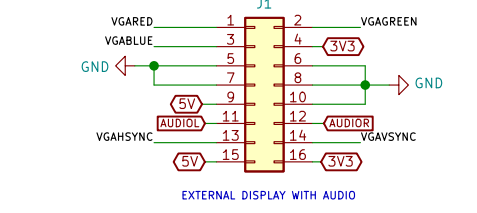
ANALOG VGA SIGNALS



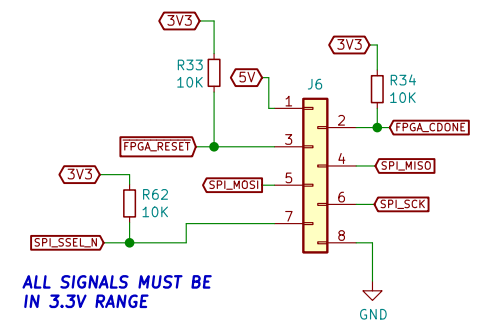
VERA FPGA PROGRAMMED OK



EXTERNAL VIDEO CONNECTOR

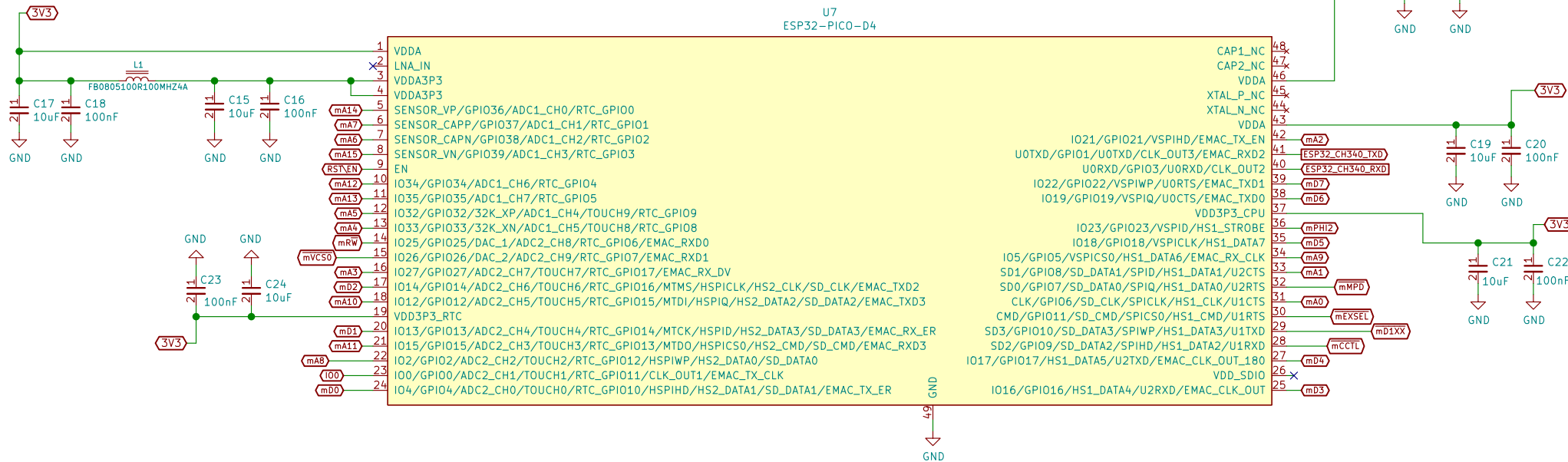


iceprog programmer USB FTDI / SPI



PBI Bus Interface Decoder:  
\$D1XX, \$D1FF, MPD, \$D8XX-\$DFXX, EX(T)SEL

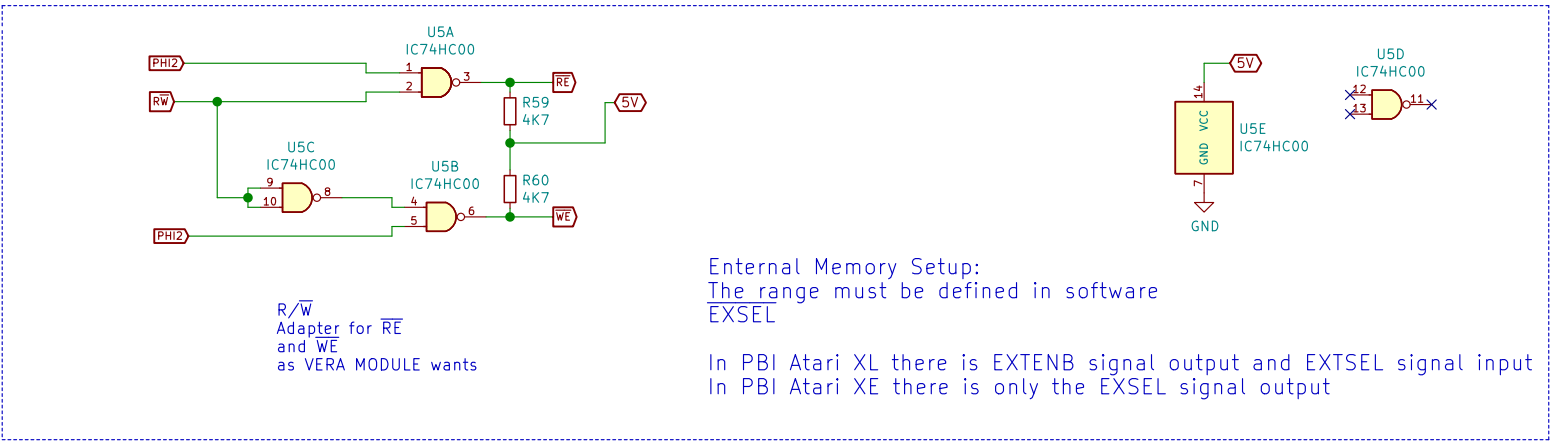
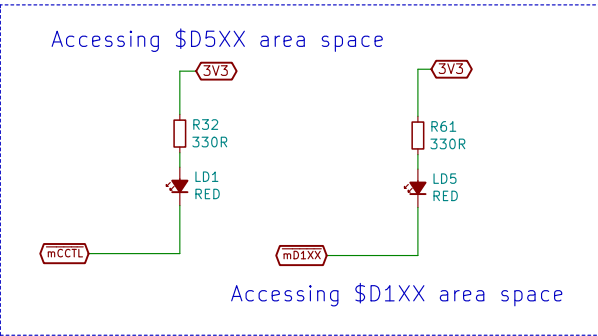
PBI DEVICE ID: software selectable only



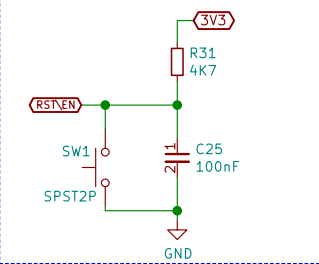
mVCS0 active & A15..A0 \$D8XX-\$DFXX -> MPD active (Internal 2K ROM)

\$D1FF access & DATABUS = PBI DEVICE ID -> mVCS0 active/deactive

Those signals are valid in ATARI XE only



ESP32 RESET SWITCH



Gianluca Renzi

RetroBit Lab

Sheet: /BusDecoder/

File: busdecoder.sch

Title: BUS DECODER

Size: A3

Date: 2025-09-17

Rev: 1.0

KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1

Id: 3/6

**AUDIO MIXER INSIDE ATARI**

The diagram shows the internal audio mixer circuit of the Atari 2600. It features the EC11 ECIBUS chip, which is connected to various components. The chip's pins are labeled: EXSEL (1), RST (2), D1XX (3), MPD (4), AUDIO (5), REF (6), VCC (7), RSRVD (A), IRQ (B), HALT (C), A13 (D), A14 (E), A15 (F), and GND (H). The chip is connected to a 5V supply, a GND, and a 2K7 resistor (R35) which is connected to the AUDIO pin. The chip is also connected to a 2K7 resistor (R36) which is connected to the AUDIO pin. The chip is connected to a 2K7 resistor (R35) which is connected to the AUDIO pin. The chip is connected to a 2K7 resistor (R36) which is connected to the AUDIO pin.

All 8-Bit signals must be shifted from 5V to 3.3V and vice versa

**Mixed**

**BOTTOM**

**TOP**

**BOTTOM**

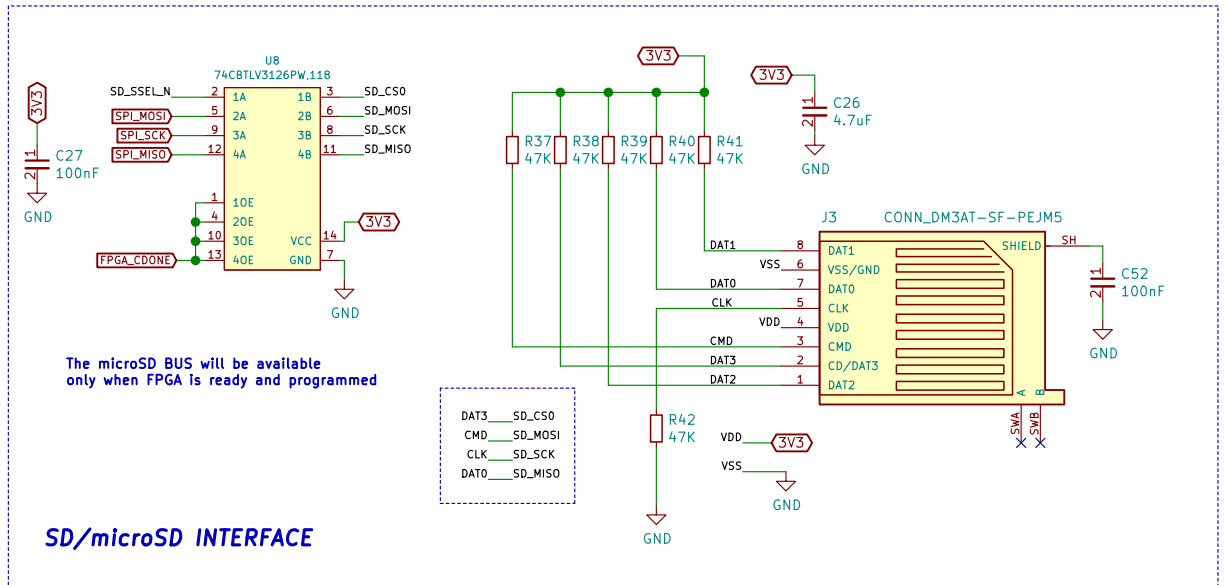
Rev: 1.0  
Id: 4/6

**FPGA/SSD Flash Glue Logic**

When programming SPI FLASH for bitstream, the JP2 jumper must be closed. Should be open in a normal operational mode.

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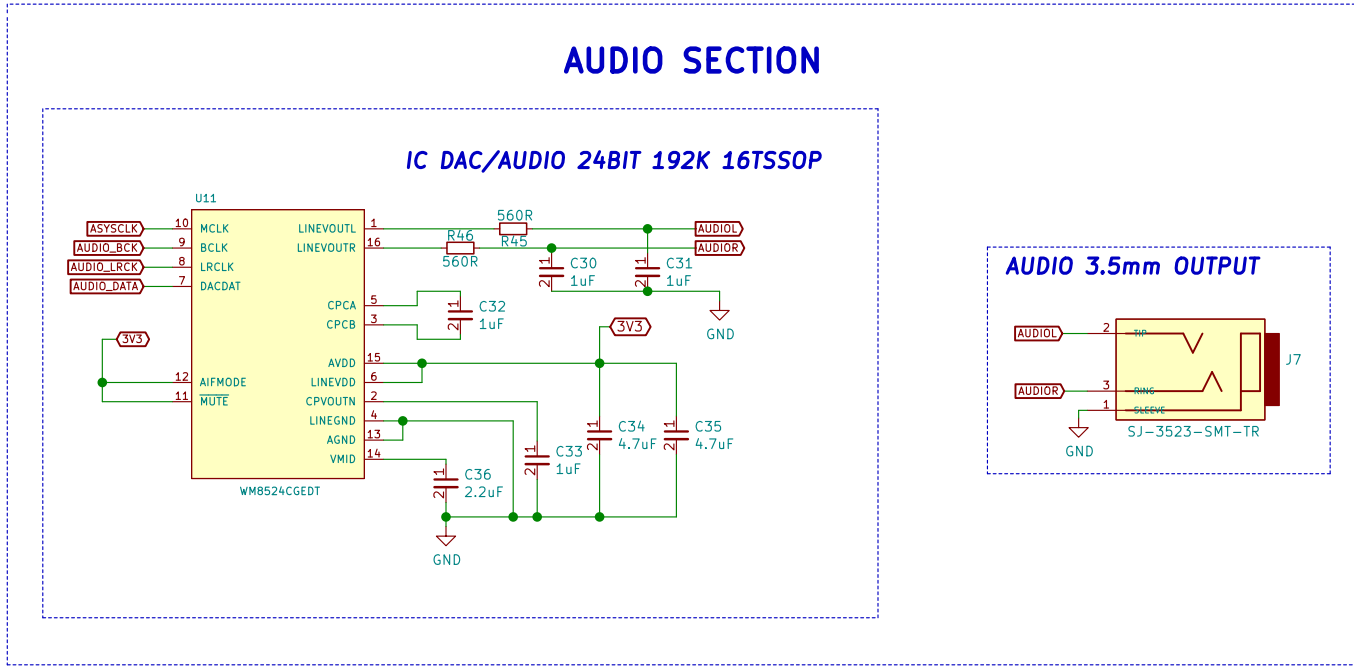


The microSD BUS will be available only when FPGA is ready and programmed

**SD/microSD INTERFACE**

The microSD BUS will be available only when FPGA is ready and programmed

**SD/microSD INTERFACE**

[illegible][illegible]

### AUDIO 3.5mm OUTPUT

AUDIOL 2 TR

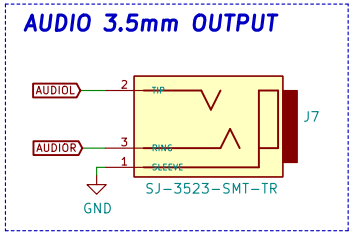
AUDIOR 3 RING

1 SLEEVE

GND

SJ-3523-SMT-TR

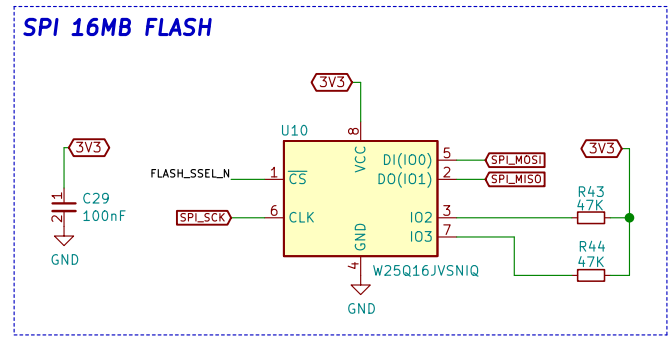
J7



The schematic diagram shows the SPI 16MB FLASH (U10) connected to a 3V3 supply and GND. The connections are as follows:

- VCC (Pin 8):** Connected to 3V3.
- DI (IO0) (Pin 5):** Connected to SPI\_MQSI.
- DO (IO1) (Pin 2):** Connected to SPI\_MISO.
- IO2 (Pin 3):** Connected to R43 (47K).
- IO3 (Pin 7):** Connected to R44 (47K).
- W25Q16JVSNQ (Pin 4):** Connected to GND.
- CLK (Pin 6):** Connected to SPI\_SCK.
- CS (Pin 1):** Connected to FLASH\_SSEL\_N.
- 3V3 (Pin 9):** Connected to 3V3.
- GND (Pin 10):** Connected to GND.

A capacitor C29 (100nF) is connected between the 3V3 supply and GND.



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