Sheet: VeraModule

VERA FPGA

File: vera-fpga.sch

Sheet: BusDecoder

BUS DECODER

File: busdecoder.sch

Sheet: Vera FPGA flash

VERA SPI FLASH
SD CARD INTERFACE

File: vera-fpga-flash.sch

Sheet: CartridgeInterface

CARTRIDGE INTERFACE

File: cartridgeInterface.sch

Sheet: PowerSupply

POWER SUPPLY

File: powersupply.sch

FIDUCIAL TOP

FID3 Fiducial

FID4 Fiducial

FIDUCIAL BOTTOM

FID2 Fiducial

FID1 Fiducial

LOGO1
VERA X16 LOGO

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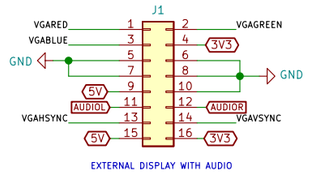
RetroBit Lab

Sheet: /
File: VERA-MODULE-RBL.sch

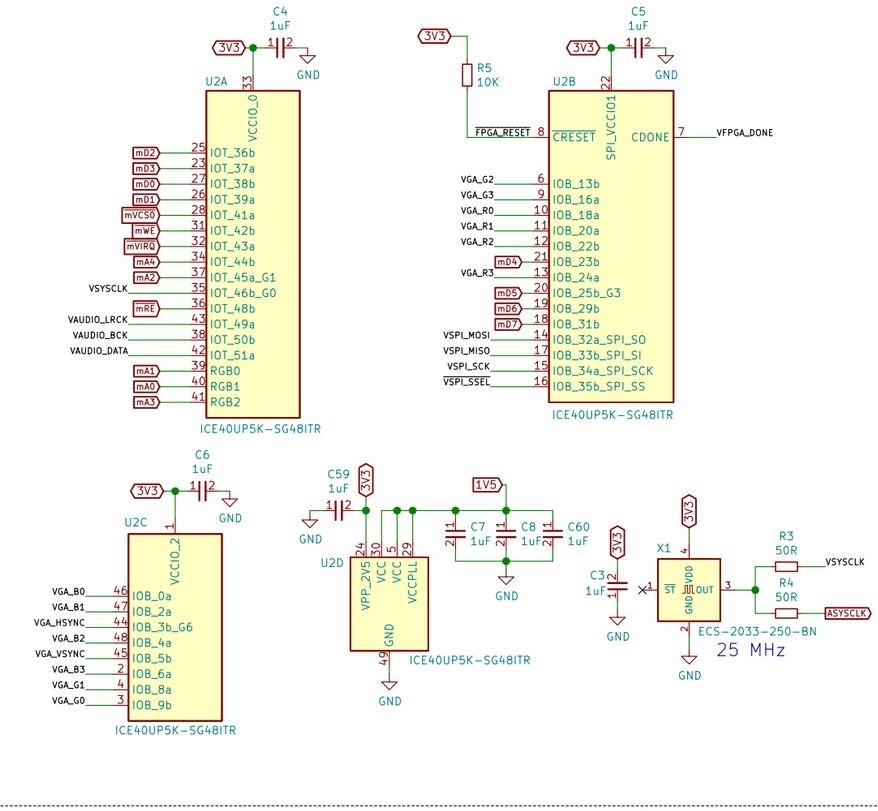
Title: VERA FPGA Audio & Video Board

Size: A4	Date: 2025-09-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 1/6

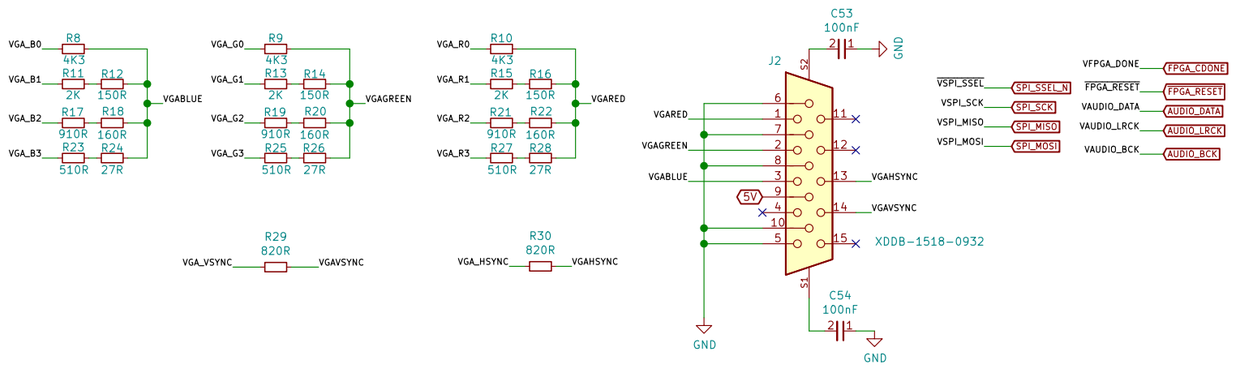
EXTERNAL VIDEO CONNECTOR



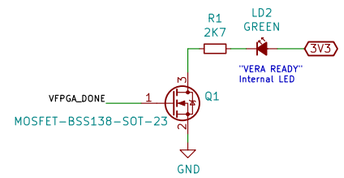
FPGA VERA LOGIC VIDEO & AUDIO CARD



ANALOG VGA SIGNALS



VERA FPGA PROGRAMMED OK



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RetroBit Lab

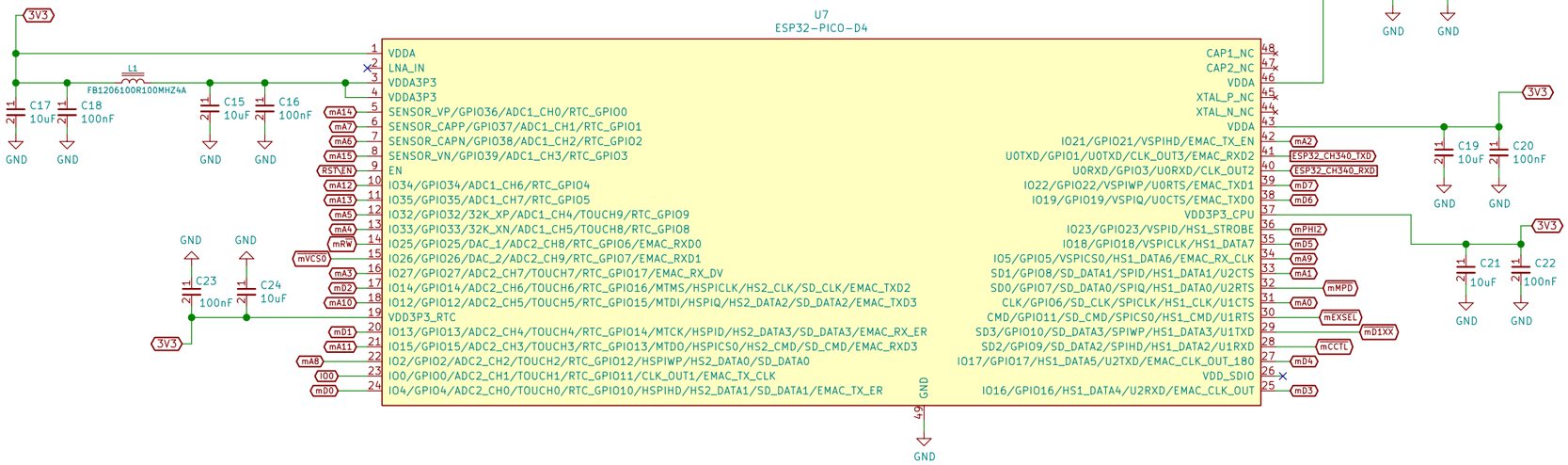
Sheet: /VeraModule/
File: vera-fpga.sch

Title: VERA MODULE AND EXTERNAL VIDEO CONNECTOR

Size: A3	Date: 2025-09-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 2/6

PBI Bus Interface Decoder:
$D1XX, $D1FF, MPD, $D8XX–$DFXX, EX(T)SEL

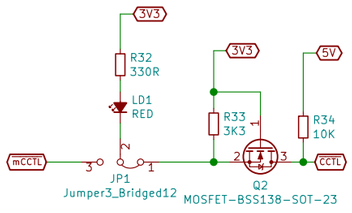
PBI DEVICE ID: software selectable only



mVCS0 active & A15..A0 $D8XX–$DFXX –> MPD active (Internal 2K ROM)

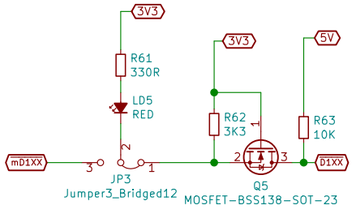
$D1FF access & DATABUS = PBI DEVICE ID –> mVCS0 active/deactive

JP12: CCTL REAL FROM ATARI (XE)
JP23: CCTL from MCU (PBI Bus has no CCTL signal)

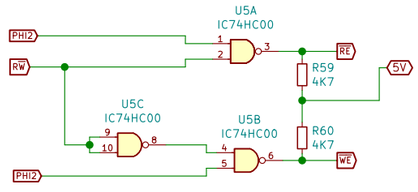


Accessing $D5XX area space

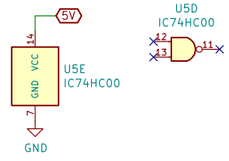
JP12: D1XX REAL FROM ATARI (XE)
JP23: D1XX from MCU



Accessing $D1XX area space



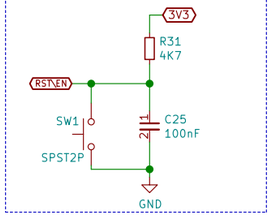
R/$\overline{W}$
Adapter for $\overline{RE}$
and $\overline{WE}$
as VERA MODULE wants



Enternal Memory Setup:
The range must be defined in software
EXSEL

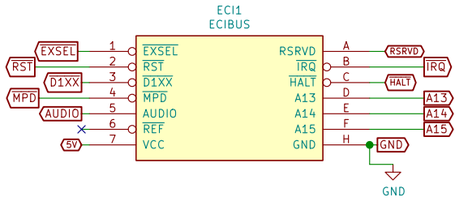
In PBI Atari XL there is EXTENB signal output and EXTSEL signal input
In PBI Atari XE there is only the EXSEL signal output

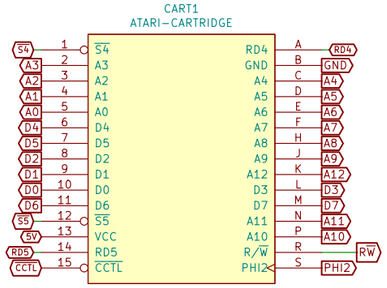
ESP32 RESET SWITCH



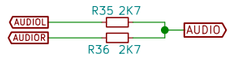
Gianluca Renzi **RetroBit Lab**		
Sheet: /BusDecoder/ File: busdecoder.sch		
Title: BUS DECODER		
Size: A3	Date: 2025-09-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 3/6

ATARI 130XE ECI & CARTRIDGE INTERFACE



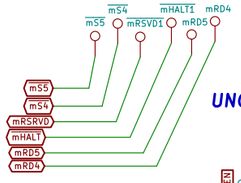


AUDIO MIXER INSIDE ATARI

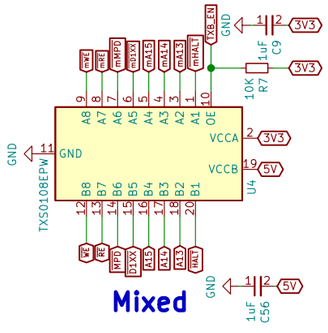


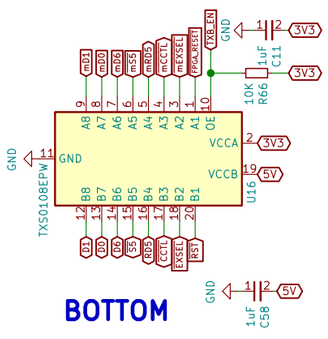
BUS LOGIC LEVEL SHIFTERS

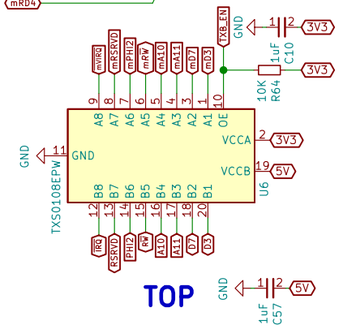
All 8-Bit signals must be shifted from 5V to 3.3V and vice versa

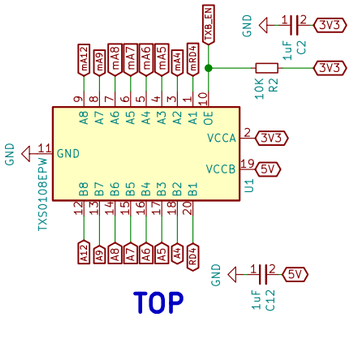


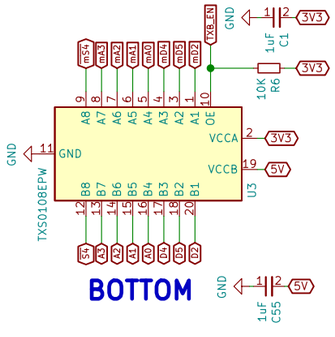
UNCONNECTED IN THIS PROJECT











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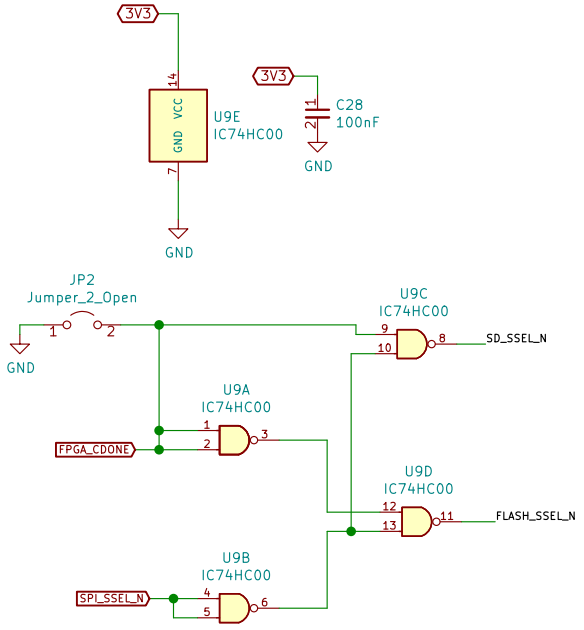
Sheet: /CartridgeInterface/
File: cartridgeInterface.sch

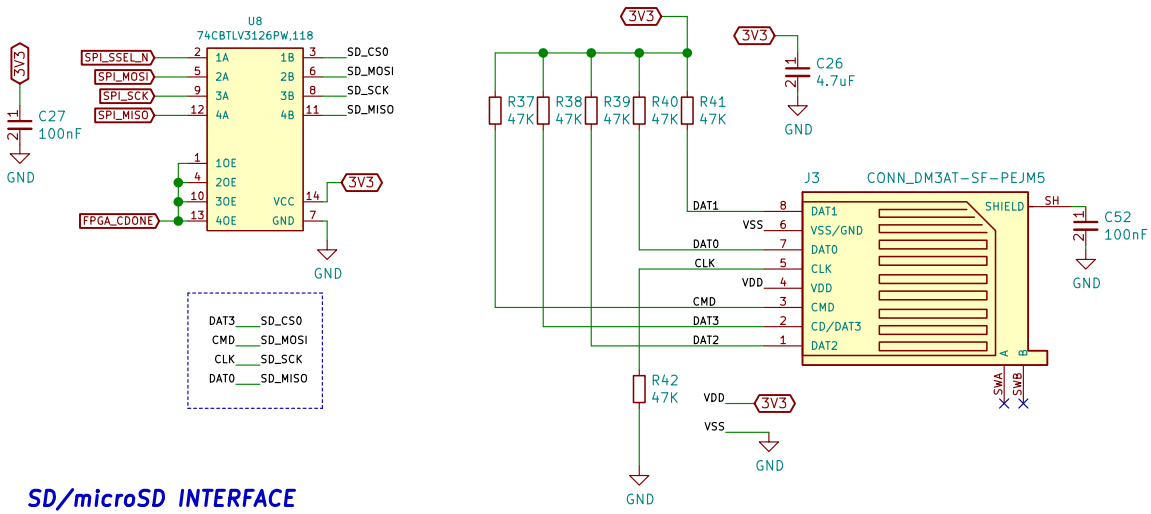
Title: CARTRIDGE INTEFACE AND BUS LEVEL SHIFTERS

Size: A3	Date: 2025-09-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 4/6

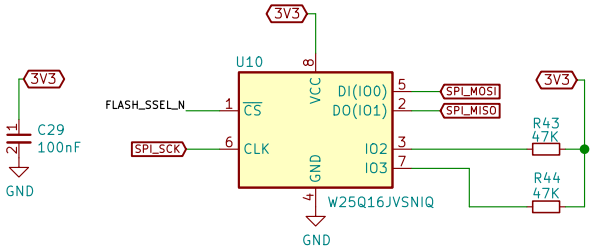
FPGA/SSD Flash Glue Logic



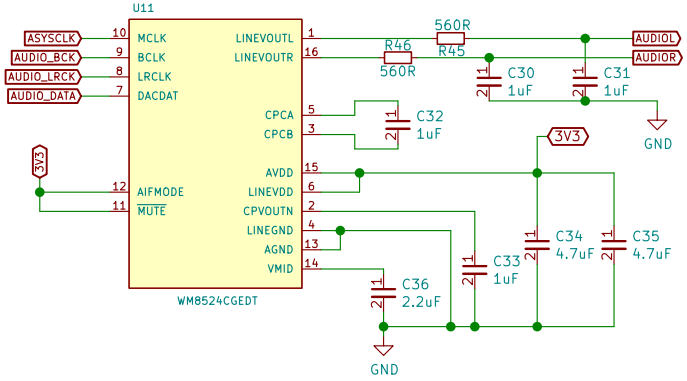
SD/microSD INTERFACE



SPI 16MB FLASH



IC DAC/AUDIO 24BIT 192K 16TSSOP



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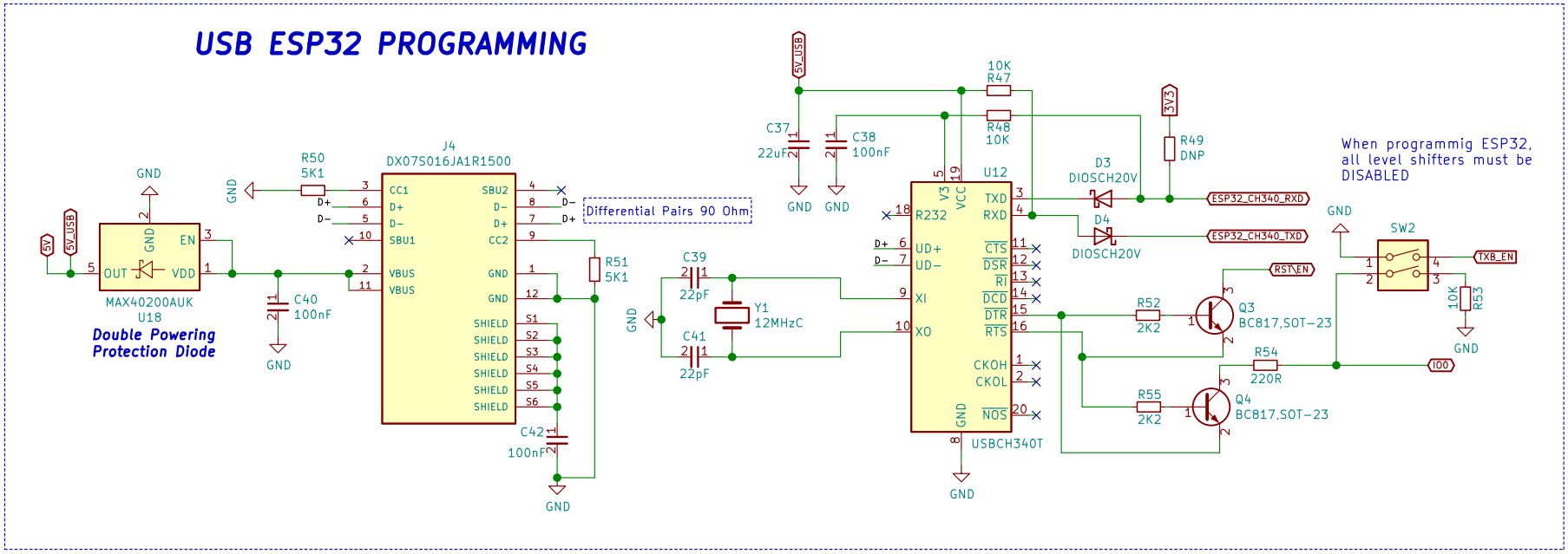
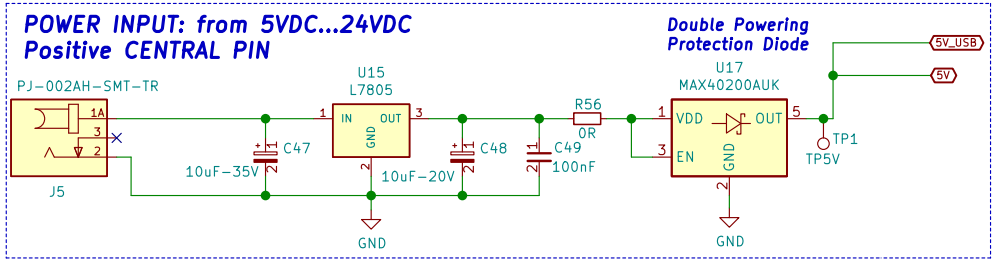
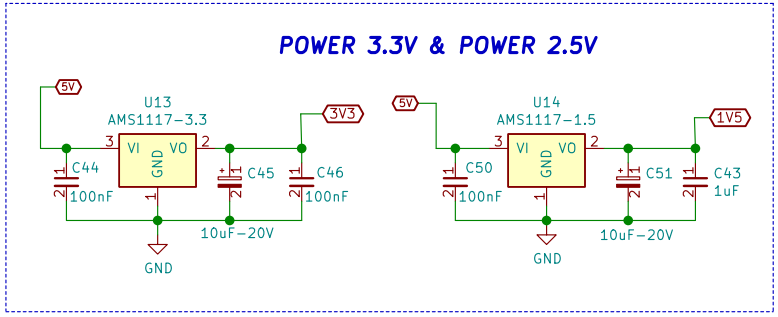
Sheet: /Vera FPGA flash/
File: vera-fpga-flash.sch

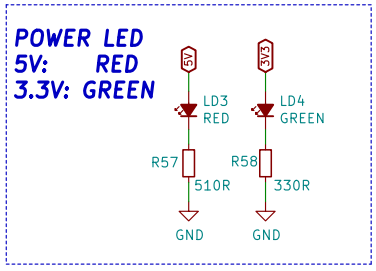
Title: uSD Card and FLASH for FPGA

Size: A4	Date: 2025-09-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 5/6









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Sheet: /PowerSupply/ File: powersupply.sch		
Title: POWERSUPPLY and USB		
Size: A4	Date: 2025-09-09	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 6/6