

Sheet: VeraModule

VERA FPGA

File: vera-fpga.sch

Sheet: BusDecoder

BUS DECODER

File: busdecoder.sch

Sheet: Vera FPGA flash

VERA SPI FLASH SD CARD INTERFACE

File: vera-fpga-flash.sch

Sheet: CartridgeInterface

CARTRIDGE INTERFACE

File: cartridgeInterface.sch

Sheet: PowerSupply

POWER SUPPLY

File: powersupply.sch

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Sheet: /
File: VERA-MODULE-RBL.sch

Title: VERA FPGA Audio & Video Board

Size: A4 Date: 2025-09-08

KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1

Rev: 1.0

Id: 1/6

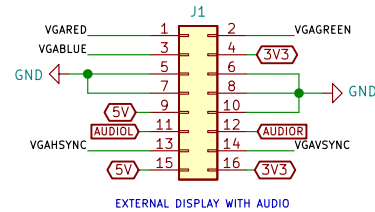
EXTERNAL VIDEO CONNECTOR

The diagram illustrates the pin configuration for an external video connector, labeled J1. The connector has 16 pins arranged in two rows of 8. The connections are as follows:

- Pin 1:** VGARED
- Pin 2:** VGAGREEN
- Pin 3:** VGBLUE
- Pin 4:** 3V3
- Pin 5:** GND
- Pin 6:** 3V3
- Pin 7:** GND
- Pin 8:** 3V3
- Pin 9:** 5V
- Pin 10:** 3V3
- Pin 11:** AUDIOL
- Pin 12:** AUDIOR
- Pin 13:** 5V
- Pin 14:** 3V3
- Pin 15:** 5V
- Pin 16:** 3V3

Additional labels include VGASync and VGBSync, which are connected to pins 11 and 12 respectively. The diagram also shows a 5V supply connected to pins 9 and 13, and a 3V3 supply connected to pins 4, 6, 8, 10, 14, and 16.

EXTERNAL DISPLAY WITH AUDIO



FPGA VERA LOGIC VIDEO & AUDIO CARD

The diagram illustrates the power and signal connections for the FPGA VERA Logic Video & Audio Card, featuring three ICE40UP5K-SG48ITR chips (U2A, U2B, U2C) and a clock divider (X1).

Power Connections:

- U2A and U2B:** Both chips are powered by a 3V3 supply. U2A's VCCIO_0 pin is connected to 3V3 via a 1uF capacitor (C4). U2B's VCCIO_1 pin is connected to 3V3 via a 1uF capacitor (C5).
- U2C:** The chip is powered by a 3V3 supply (VCCIO_2) and a 1V5 supply (VPP_2V5). Both are connected to 3V3 via 1uF capacitors (C6 and C59).

Signal Connections:

- U2A:** Various I/O pins are connected to the board, including OT_36b, OT_37a, OT_38b, OT_39a, OT_41a, OT_42b, OT_43a, OT_44b, OT_45a_G1, OT_46b_G0, OT_48b, OT_49a, OT_50b, OT_51a, RGB0, RGB1, and RGB2.
- U2B:** The chip is configured for SPI communication, with CSPL_VCCIO1 connected to 3V3 and CDONE connected to VFPGA_DONE. Various I/O pins are also connected, including IOB_13b, IOB_16a, IOB_18a, IOB_20a, IOB_22b, IOB_23b, IOB_24a, IOB_25b_G3, IOB_29b, IOB_31b, IOB_32a_SPL_S0, IOB_33b_SPL_S1, IOB_34a_SPL_SCK, and IOB_35b_SPL_SS.
- U2C:** The chip is configured for VGA and audio signals, including VGA_B0, VGA_B1, VGA_HSYNC, VGA_B2, VGA_B3, VGA_G1, VGA_G0, IOB_0a, IOB_2a, IOB_3b_G6, IOB_4a, IOB_5b, IOB_6a, IOB_8a, and IOB_9b.

Clock Divider (X1): The clock divider (ECS-2033-250-BN) takes a 25 MHz input and outputs a 25 MHz signal to the VSYSCLK pin of U2C.

ANALOG VGA SIGNALS

The diagram illustrates the analog VGA signal connections for an ICD15S13E4GX00LF display. The signals are organized into three main groups: Color Channels (Red, Green, Blue) and Sync Signals (Vsync, Hsync).

Color Channels:

- Red Channel:** VGA_R0 (4K3) and VGA_R1 (2K) are connected to the display's red input (pin 11). VGA_R2 (910R) and VGA_R3 (510R) are connected to the display's red input (pin 11).
- Green Channel:** VGA_G0 (4K3) and VGA_G1 (2K) are connected to the display's green input (pin 12). VGA_G2 (910R) and VGA_G3 (510R) are connected to the display's green input (pin 12).
- Blue Channel:** VGA_B0 (4K3) and VGA_B1 (2K) are connected to the display's blue input (pin 13). VGA_B2 (910R) and VGA_B3 (510R) are connected to the display's blue input (pin 13).

Sync Signals:

- Vsync:** VGA_VSYNC (820R) is connected to the display's Vsync input (pin 14).
- Hsync:** VGA_HSYNC (820R) is connected to the display's Hsync input (pin 15).

Display Module: The display module is represented by a yellow trapezoid with pins 1-15. Pins 11, 12, 13, 14, and 15 are connected to the color channels and sync signals. Pins 6, 7, 8, 9, and 10 are connected to ground. A 5V supply is connected to pin 4. Capacitors C53 and C54 (100nF) are connected to pins 52 and 15 respectively.

Legend:

Signal	Component	Value
VGA_R0	R8	4K3
VGA_R1	R11	2K
VGA_R2	R17	910R
VGA_R3	R23	510R
VGA_G0	R9	4K3
VGA_G1	R13	2K
VGA_G2	R19	910R
VGA_G3	R25	510R
VGA_B0	R10	4K3
VGA_B1	R15	2K
VGA_B2	R21	910R
VGA_B3	R27	510R
VGA_VSYNC	R29	820R
VGA_HSYNC	R30	820R

VERA FPGA PROGRAMMED OK

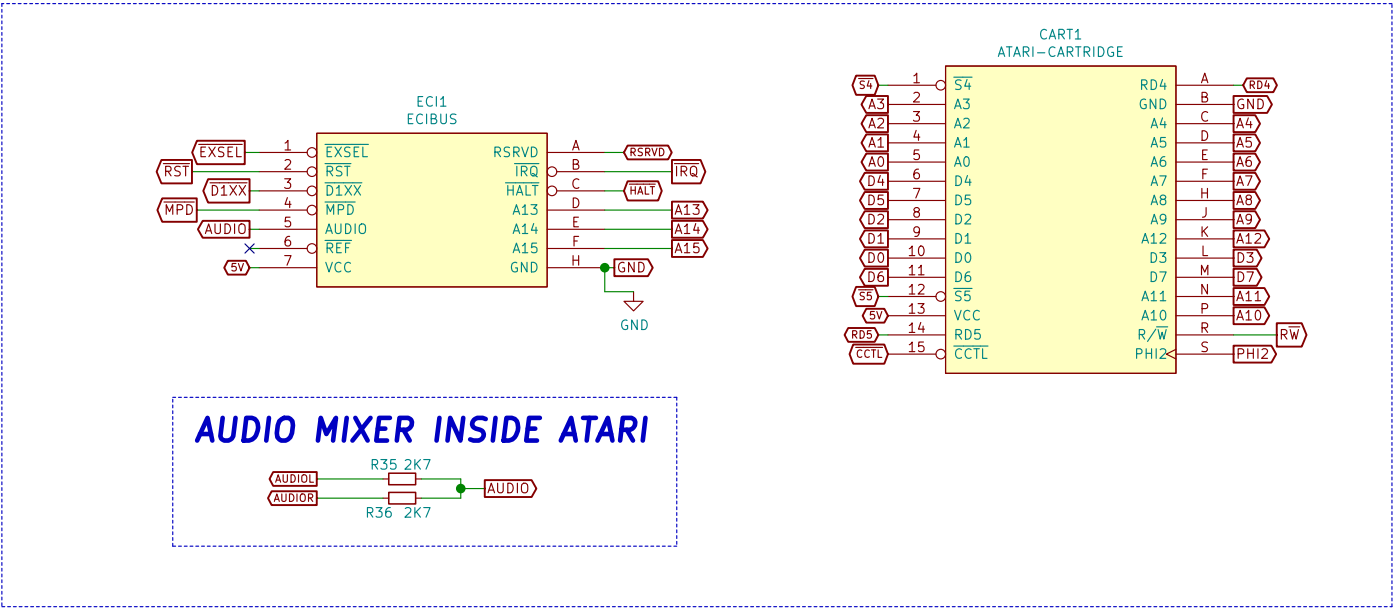
The diagram shows a MOSFET (BSS138) circuit. The gate is connected to VPPGA_DONE (pin 1). The drain is connected to a 2K7 resistor (R1) and the anode of a green LED (LD2). The LED is labeled "VERA READY Internal LED" and is connected to a 3V3 supply. The MOSFET's source is connected to ground (pin 2).

Id: 2/6

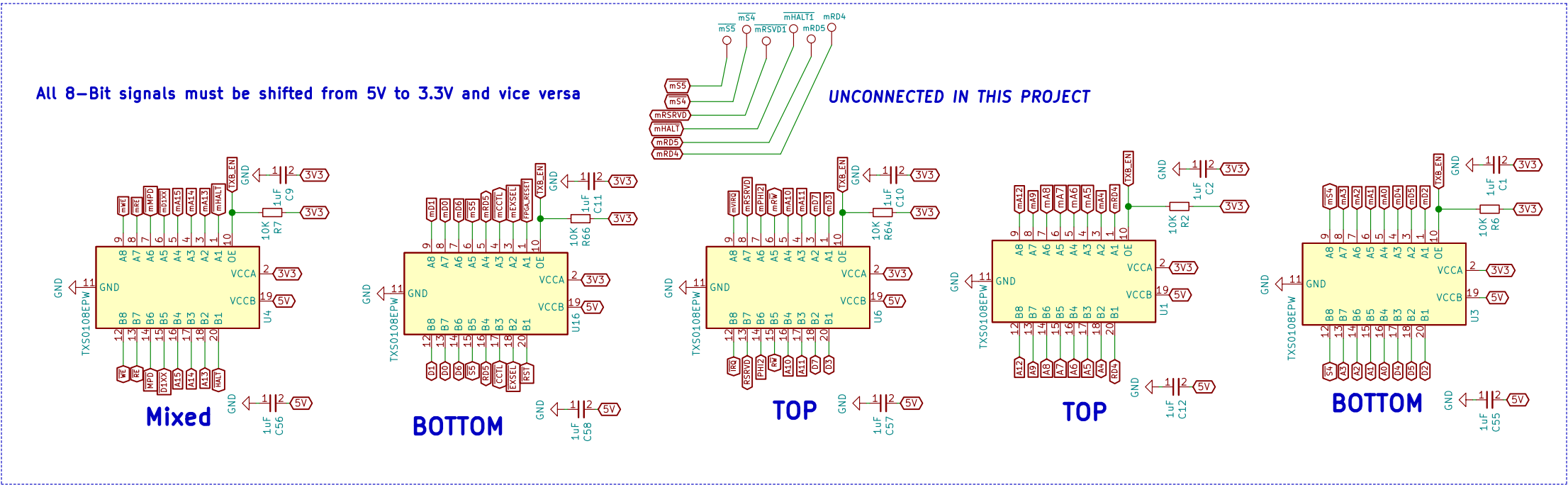
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ATARI 130XE ECI & CARTRIDGE INTERFACE



BUS LOGIC LEVEL SHIFTERS



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Sheet: /CartridgeInterface/

File: cartridgeInterface.sch

Title:

Size: A3 Date: 2025-09-08

KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1

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IC DAC/AUDIO 24BIT 192K 16TSSOP

The diagram shows the pin connections for the WM8524CGEDT DAC/Audio IC. The IC is a yellow rectangle with pins 1-16 on the top and bottom. The connections are as follows:

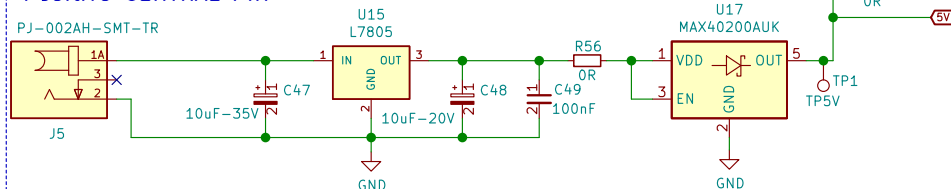
- Pin 10 (MCLK) is connected to ASYSCLK.
- Pin 9 (BCLK) is connected to AUDIO_BCK.
- Pin 8 (LRCLK) is connected to AUDIO_LRCLK.
- Pin 7 (DACDAT) is connected to AUDIO_DATA.
- Pin 12 (AIFMODE) is connected to 3V3.
- Pin 11 (MUTE) is connected to GND.
- Pin 1 (LINEVOUTL) is connected to R46 (560R) and R45 (560R) in series, then to C30 (2uF) and C31 (1uF) in parallel, and finally to AUDIOL.
- Pin 16 (LINEVOUTR) is connected to C32 (2uF) and C33 (1uF) in parallel, and finally to AUDIOR.
- Pin 5 (CPCA) is connected to C32.
- Pin 3 (CPCB) is connected to C32.
- Pin 15 (AVDD) is connected to 3V3.
- Pin 6 (LINEVDD) is connected to 3V3.
- Pin 2 (CPVOUTN) is connected to C34 (4.7uF) and C35 (4.7uF) in parallel, and finally to GND.
- Pin 4 (LINEGND) is connected to C34 and C35.
- Pin 13 (AGND) is connected to C34 and C35.
- Pin 14 (VMID) is connected to C36 (2.2uF) and C33 (1uF) in parallel, and finally to GND.

The IC is labeled WM8524CGEDT.

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SPI 16MB FLASH

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Id: 5/6

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RetroBit Lab

File: powersupply.sch

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Rev: 1.0

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