Sheet: VeraModule

VERA FPGA

File: vera-fpga.sch

Sheet: BusDecoder

BUS DECODER

File: busdecoder.sch

Sheet: Vera FPGA flash

VERA SPI FLASH
SD CARD INTERFACE

File: vera-fpga-flash.sch

Sheet: CartridgeInterface

CARTRIDGE INTERFACE

File: cartridgeInterface.sch

Sheet: PowerSupply

POWER SUPPLY

File: powersupply.sch

Sheet: VGA Analog

VGA ANALOG

File: vga-analog.sch

FIDUCIAL TOP

FID3 Fiducial
FID4 Fiducial

FIDUCIAL BOTTOM

FID2 Fiducial
FID1 Fiducial

LOGO1
VERA X16 LOGO

LOGO2
ATARI READY

LOGO3
KiCAD DESIGN

LOGO4
ATARI DUO BUS

LOGO5
ESP32_BOBOARD

LBL1

H1
MountingHole

H2
MountingHole

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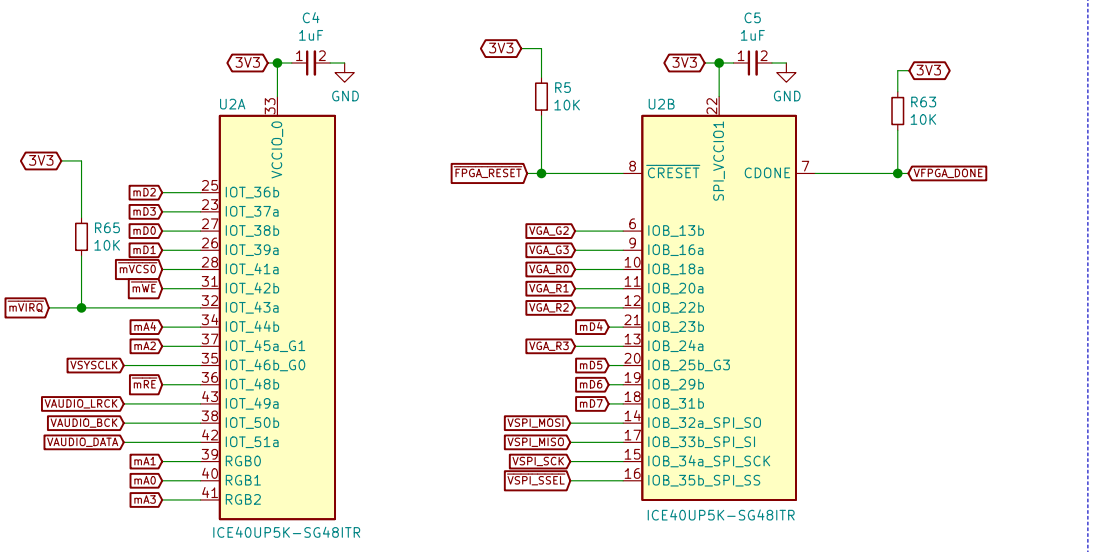
Sheet: /
File: VERA-MODULE-RBL.sch

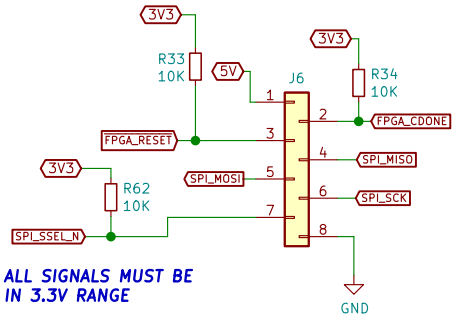
Title: VERA FPGA Audio & Video Board

Size: A4	Date: 2025-10-17	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 1/7

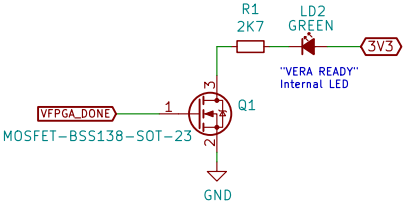
FPGA VERA LOGIC VIDEO & AUDIO CARD



iceprog programmer USB FTDI / SPI



VERA FPGA PROGRAMMED OK



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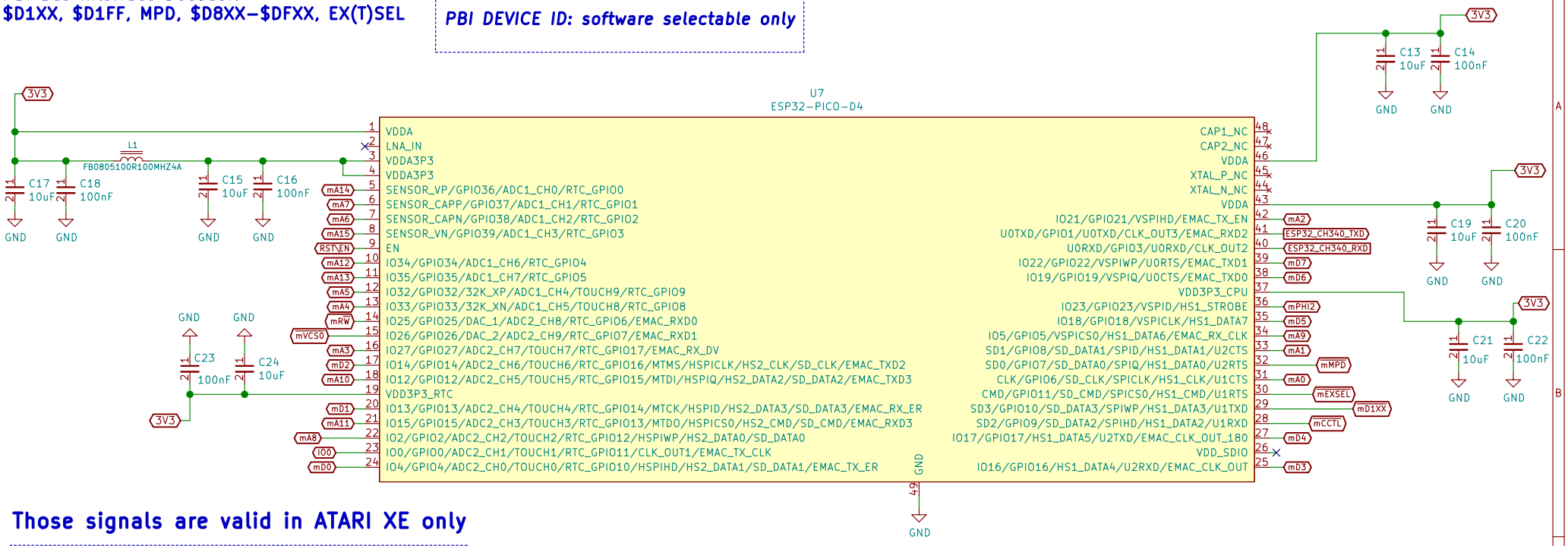
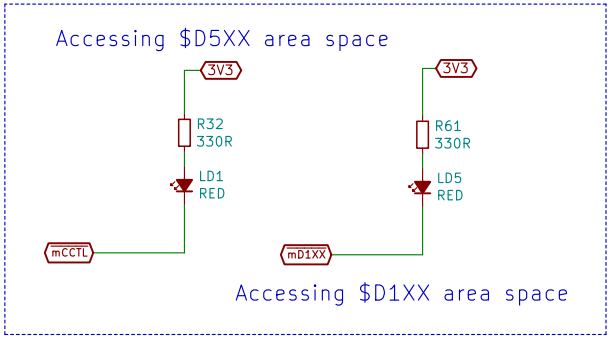
Sheet: /VeraModule/		
File: vera-fpga.sch		
Title: VERA MODULE AND PROGRAMMING CONNECTOR		
Size: A4	Date: 2025-10-17	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 2/7

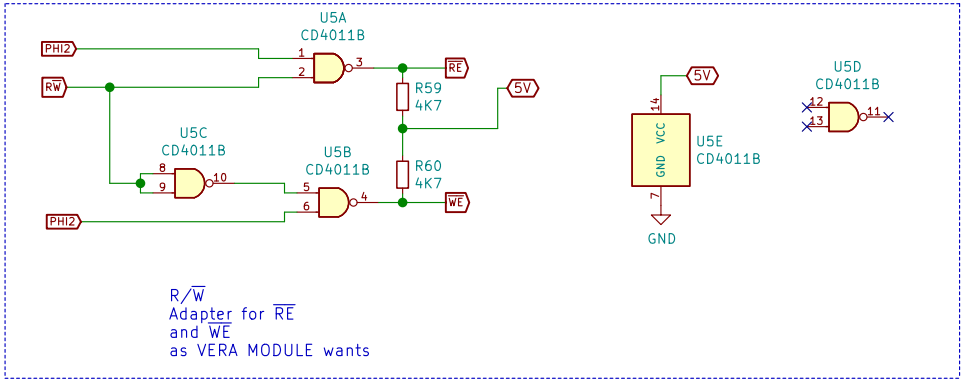
PBI Bus Interface Decoder:
$D1XX, $D1FF, MPD, $D8XX–$DFXX, EX(T)SEL

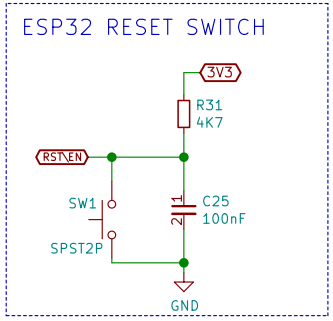
PBI DEVICE ID: software selectable only



Those signals are valid in ATARI XE only







Enternal Memory Setup:
The range must be defined in software
EXSEL

In PBI Atari XL there is EXTENB signal output and EXTSEL signal input
In PBI Atari XE there is only the EXSEL signal output

mVCS0 active & A15..A0 $D8XX–$DFXX –> MPD active (Internal 2K ROM)

$D1FF access & DATABUS = PBI DEVICE ID –> mVCS0 active/deactive

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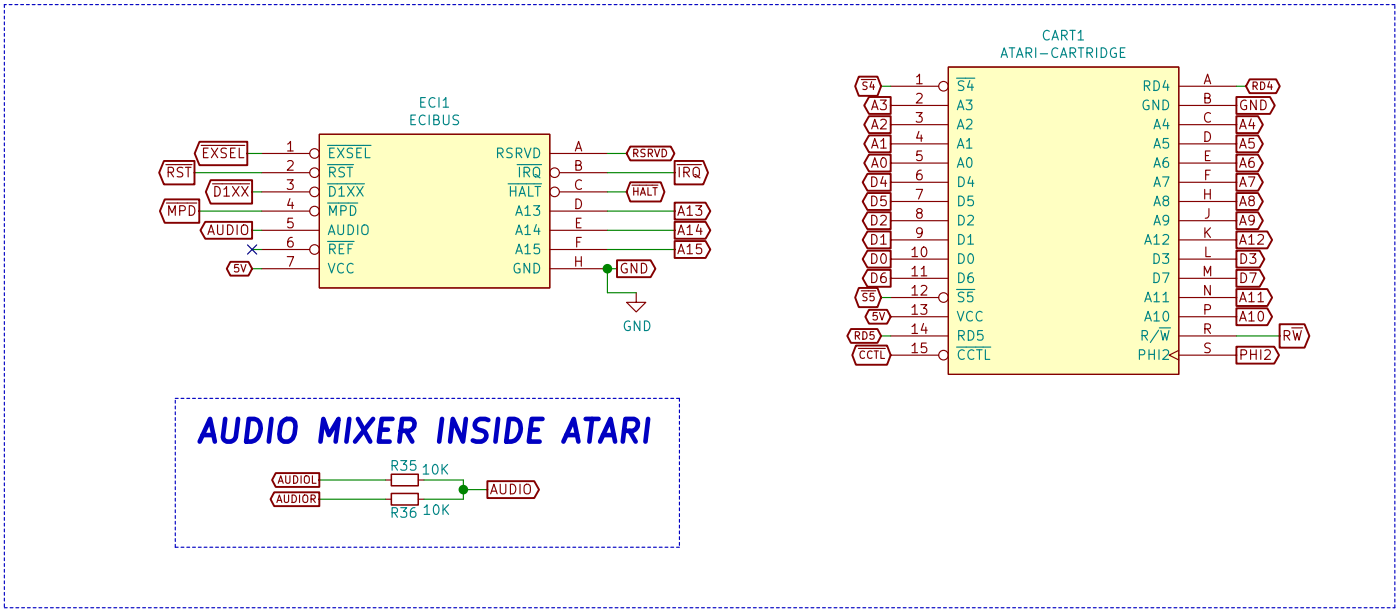
Sheet: /BusDecoder/
File: busdecoder.sch

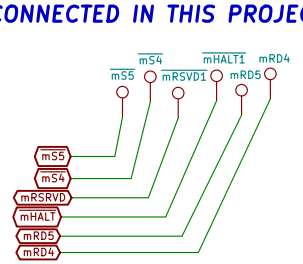
Title: BUS DECODER

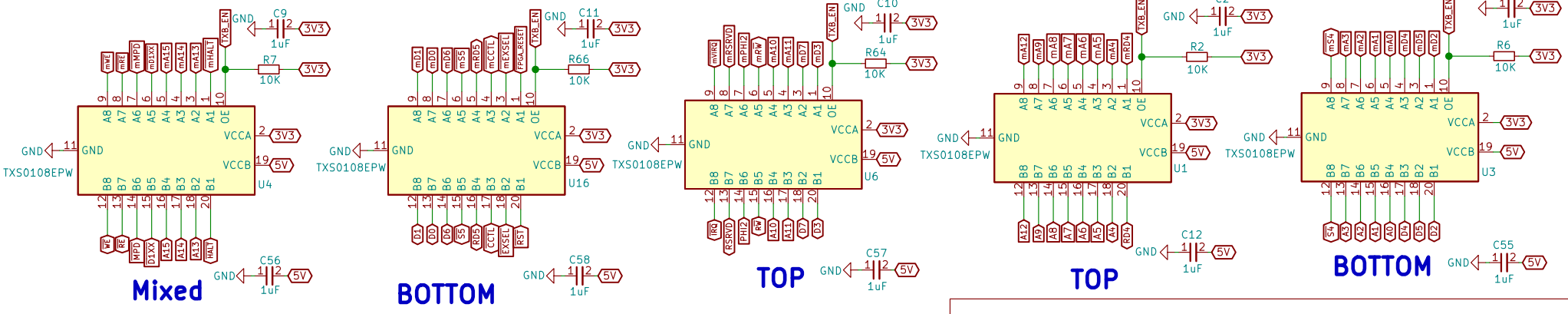
Size: A4	Date: 2025-10-17	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 3/7

ATARI 130XE ECI & CARTRIDGE INTERFACE

All 8-Bit signals must be shifted from 5V to 3.3V and vice versa







BUS LOGIC LEVEL SHIFTERS

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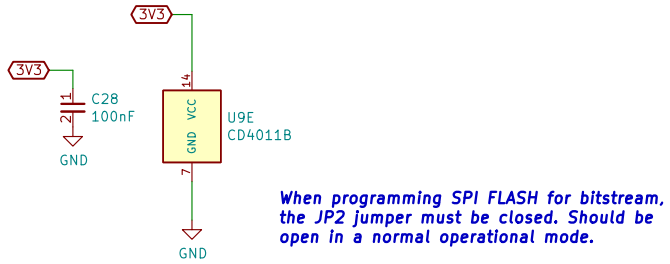
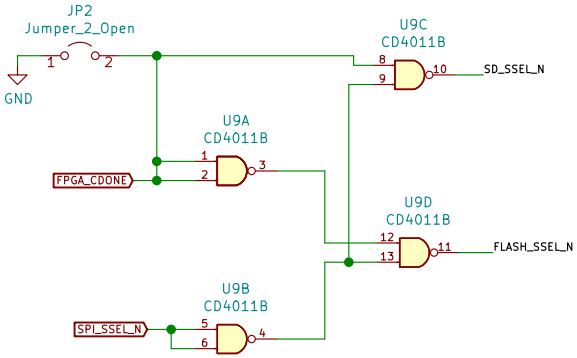
Sheet: /CartridgeInterface/
File: cartridgeInterface.sch

Title: CARTRIDGE INTEFACE AND BUS LEVEL SHIFTERS

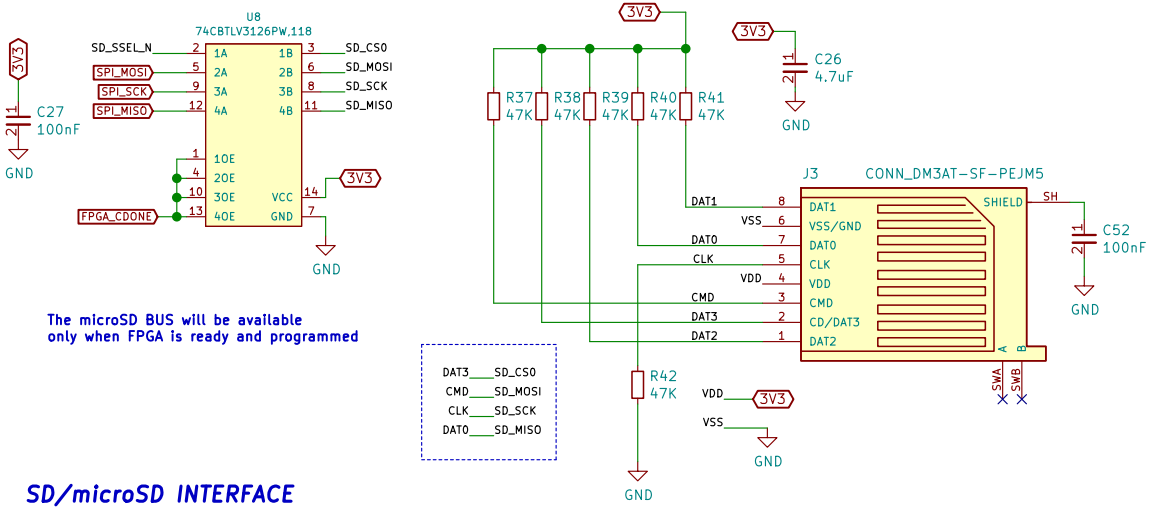
Size: A4	Date: 2025-10-17	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 4/7

FPGA/SSD Flash Glue Logic



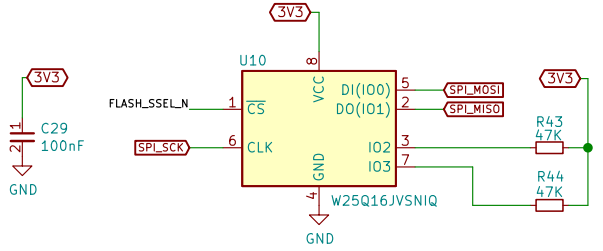


SD/microSD INTERFACE

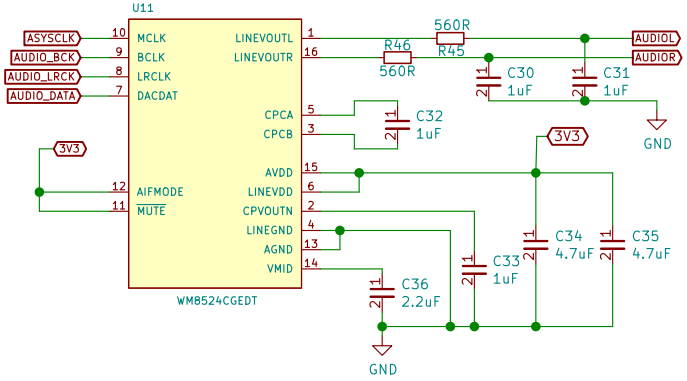


The microSD BUS will be available only when FPGA is ready and programmed

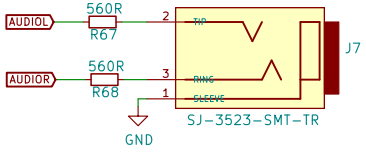
SPI 16MB FLASH



IC DAC/AUDIO 24BIT 192K 16TSSOP



AUDIO 3.5mm OUTPUT



AUDIO SECTION

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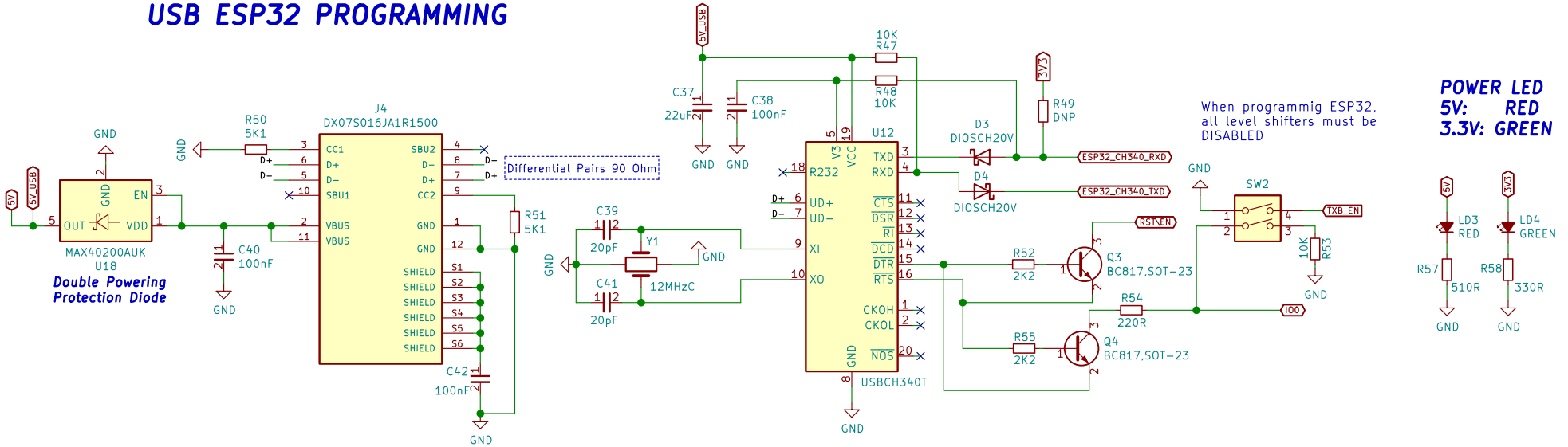
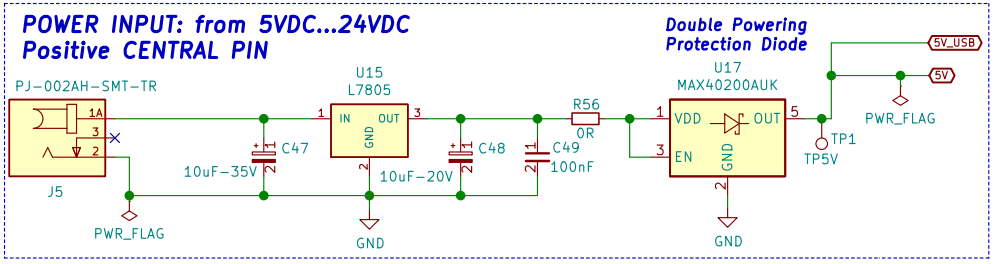
Sheet: /Vera FPGA flash/
File: vera-fpga-flash.sch

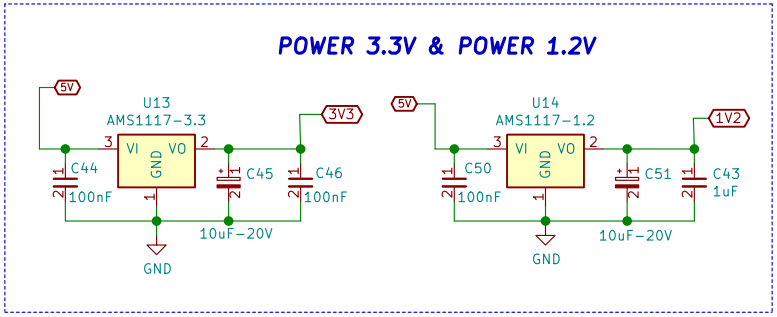
Title: uSD Card, FPGA FLASH and AUDIO SECTION

Size: A4	Date: 2025-10-17	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 5/7

USB ESP32 PROGRAMMING







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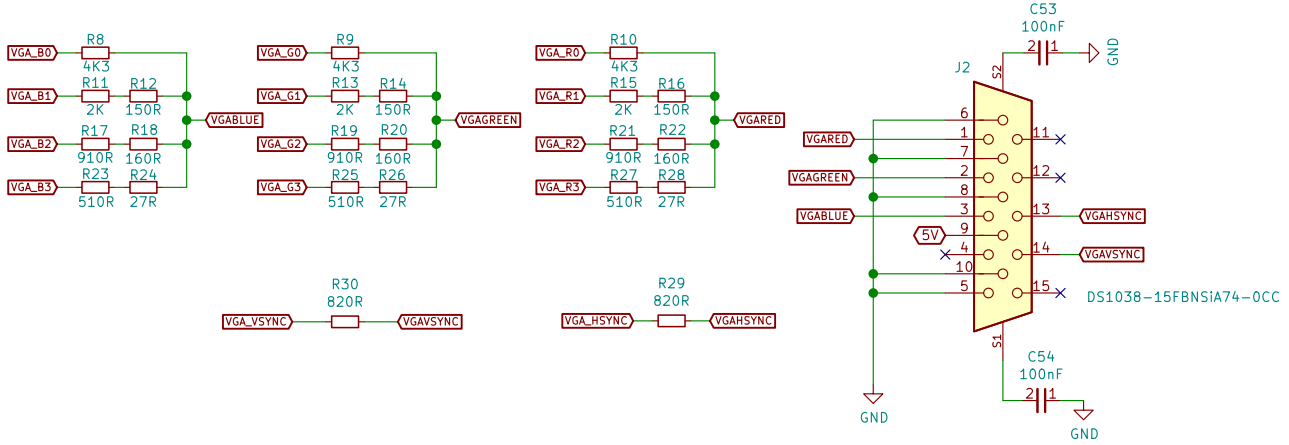
Sheet: /PowerSupply/
File: powersupply.sch

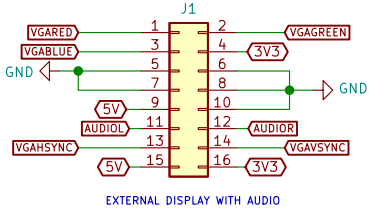
Title: POWERSUPPLY and USB

Size: A4	Date: 2025-10-17	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 6/7

ANALOG VGA SIGNALS



EXTERNAL VIDEO CONNECTOR



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Sheet: /VGA Analog/
File: vga-analog.sch

Title: VGA ANALOG AND EXTERNAL VIDEO CONNECTOR

Size: A4	Date: 2025-10-17	**Rev: 1.0**
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1		Id: 7/7