

Sheet: VeraModule

VERA FPGA

File: vera-fpga.sch

Sheet: BusDecoder

BUS DECODER

File: busdecoder.sch

Sheet: Vera FPGA flash

VERA SPI FLASH
SD CARD INTERFACE

File: vera-fpga-flash.sch

Sheet: CartridgeInterface

CARTRIDGE INTERFACE

File: cartridgeInterface.sch

Sheet: PowerSupply

POWER SUPPLY

File: powersupply.sch

Sheet: VGA Analog

VGA ANALOG

File: vga-analog.sch

FIDUCIAL TOP

FID3
Fiducial

FID4
Fiducial

FIDUCIAL BOTTOM

FID2
Fiducial

FID1
Fiducial

H1
MountingHole

H2
MountingHole

LOG01
VERA X16 LOGO

LOG03
KICAD DESIGN

LOG05
ESP32_BOBOARD

LBL1

LOG02
ATARI READY

LOG04
ATARI DUO BUS

Gianluca Renzi
RetroBit Lab

Sheet: /
File: VERA-MODULE-RBL.sch

Title: VERA FPGA Audio & Video Board

Size: A4

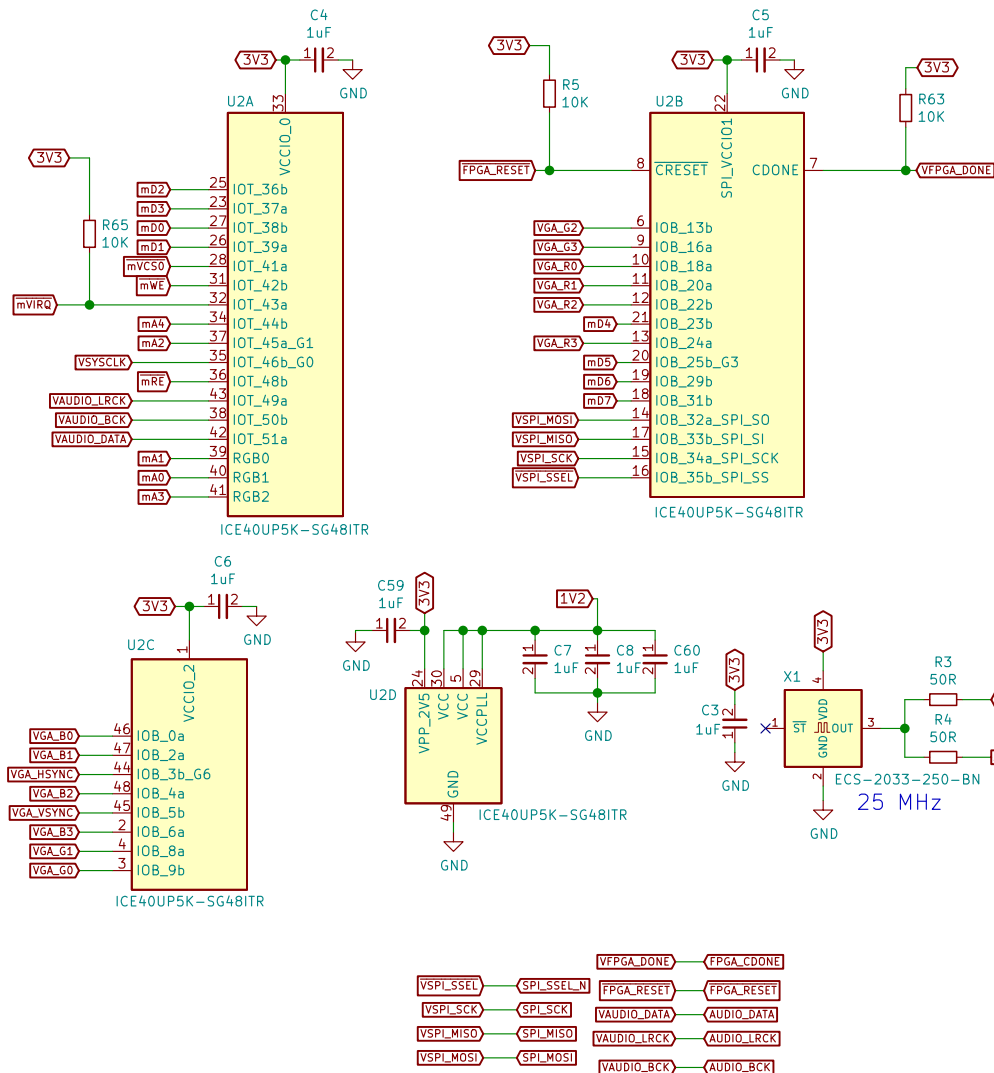
Date: 2025-10-17

KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1

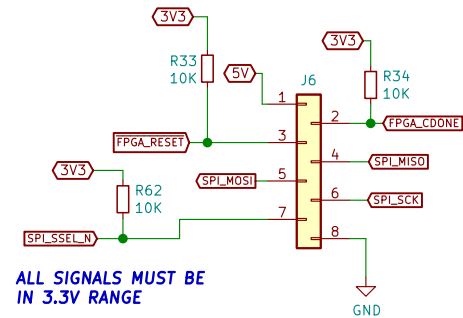
Rev: 1.0

Id: 1/7

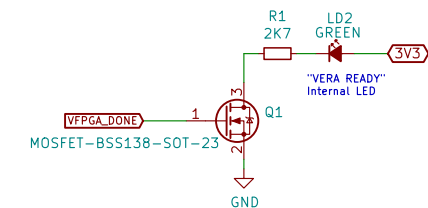
FPGA VERA LOGIC VIDEO & AUDIO CARD



Iceprog programmer USB FTDI / SPI



VERA FPGA PROGRAMMED OK



Gianluca Renzi

RetroBit Lab

Sheet: /VeraModule/

File: vera-fpga.sch

Title: VERA MODULE AND PROGRAMMING CONNECTOR

Size: A4

Date: 2025-10-17

Rev: 1.0

KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1

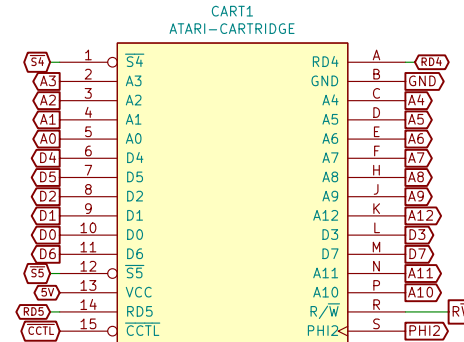
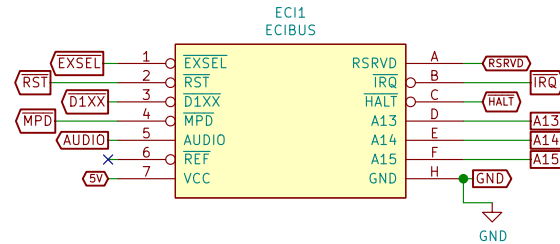
Id: 2/7

PBI DEVICE ID: software selectable only

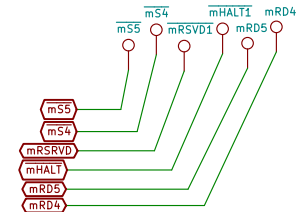


ATARI 130XE ECI & CARTRIDGE INTERFACE

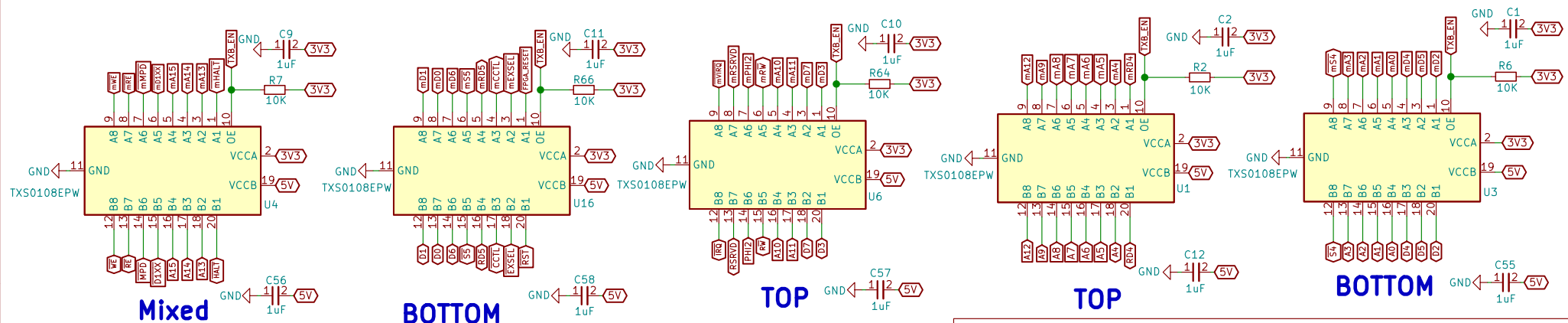
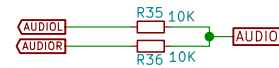
All 8-Bit signals must be shifted from 5V to 3.3V and vice versa



UNCONNECTED IN THIS PROJECT



AUDIO MIXER INSIDE ATARI



BUS LOGIC LEVEL SHIFTERS

Gianluca Renzi

RetroBit Lab

Sheet: /CartridgeInterface/

File: cartridgeInterface.sch

Title: CARTRIDGE INTERFACE AND BUS LEVEL SHIFTERS

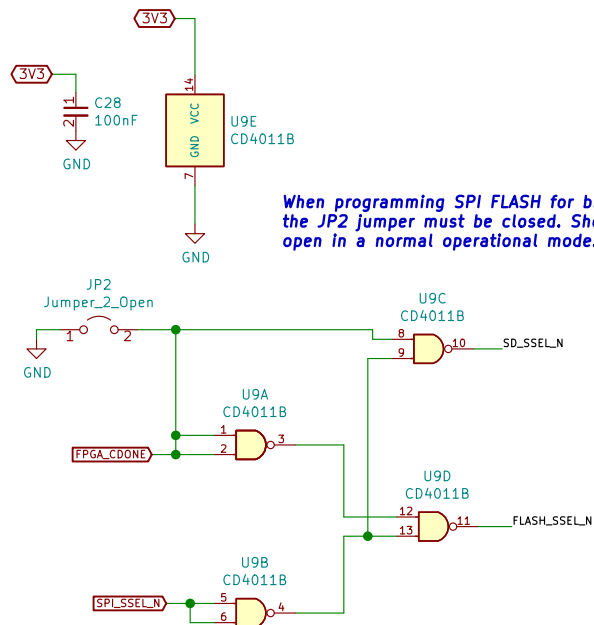
Size: A4 Date: 2025-10-17

KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1

Rev: 1.0

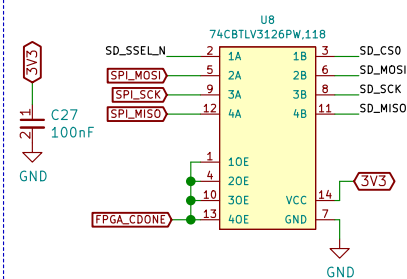
Id: 4/7

FPGA/SSD Flash Glue Logic

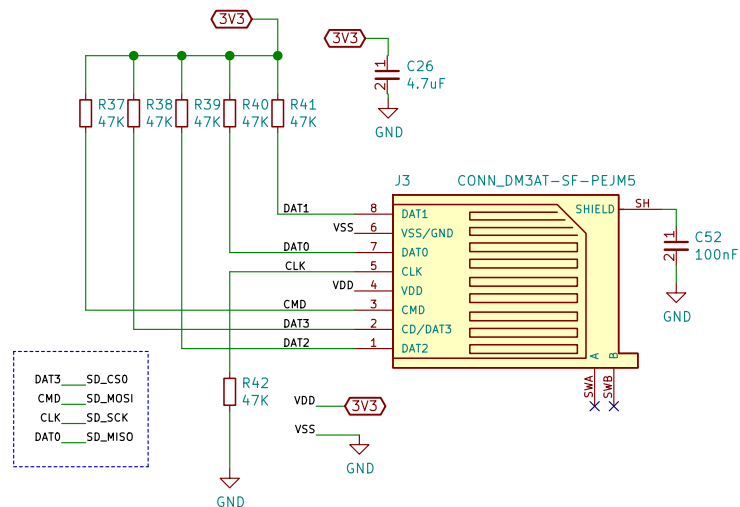


When programming SPI FLASH for bitstream, the JP2 jumper must be closed. Should be open in a normal operational mode.

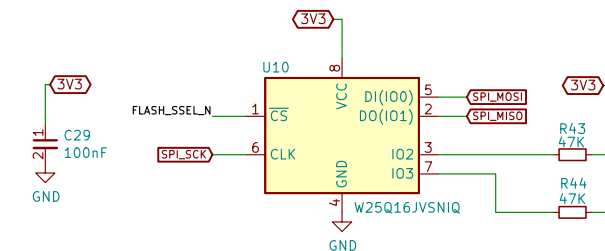
SD/microSD INTERFACE



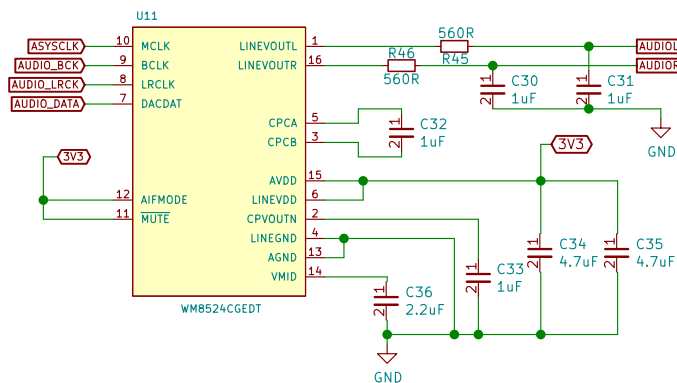
The microSD BUS will be available only when FPGA is ready and programmed



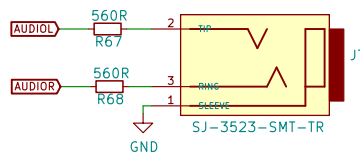
SPI 16MB FLASH



IC DAC/AUDIO 24BIT 192K 16TSSOP



AUDIO 3.5mm OUTPUT



AUDIO SECTION

Gianluca Renzi

RetroBit Lab

Sheet: /Vera FPGA flash/

File: vera-fpga-flash.sch

Title: uSD Card, FPGA FLASH and AUDIO SECTION

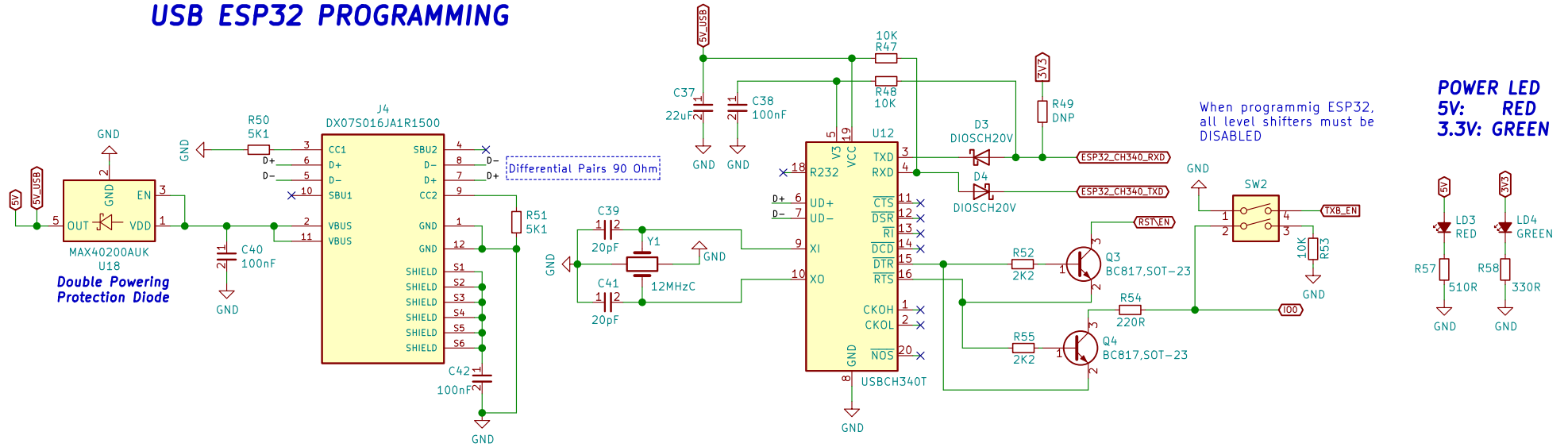
Size: A4	Date: 2025-10-17
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KiCad E.D.A.	kicad 5.1.9+dfsg1-1+deb11u1
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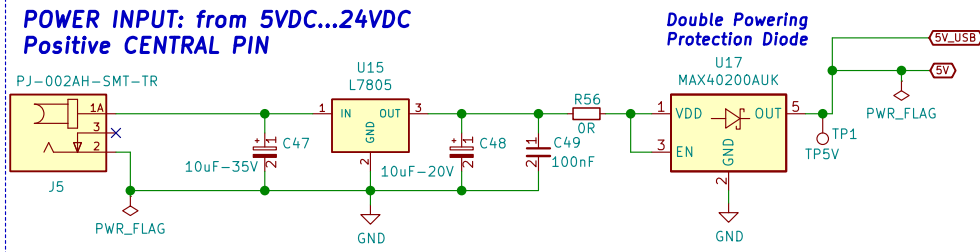
Rev: 1.0

Id: 5/7

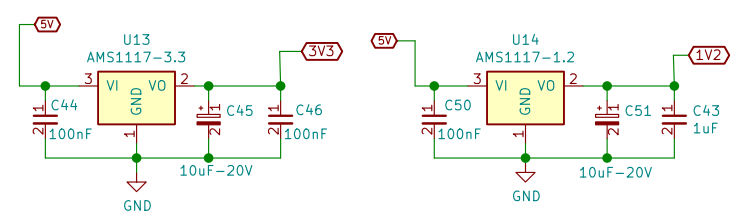
USB ESP32 PROGRAMMING



POWER INPUT: from 5VDC...24VDC
Positive CENTRAL PIN



POWER 3.3V & POWER 1.2V



Gianluca Renzi
RetroBit Lab

Sheet: /PowerSupply/
File: powersupply.sch

Title: POWERSUPPLY and USB

Size: A4	Date: 2025-10-17
KiCad E.D.A. kicad 5.1.9+dfsg1-1+deb11u1	

Rev: 1.0
Id: 6/7

ANALOG VGA SIGNALS

The schematic diagram illustrates the analog VGA signal path. It begins with three input signal groups: VGA_B0-B3, VGA_G0-G3, and VGA_R0-R3. Each group consists of four signals (B0, B1, B2, B3 for Blue; G0, G1, G2, G3 for Green; R0, R1, R2, R3 for Red) that pass through a series of resistors (R8-R24) to form a differential pair (e.g., VGABLUE, VGAGREEN, VGARED). These signals are then conditioned by a second set of resistors (R25-R28) and a 5V reference voltage. The conditioned signals are connected to a 15-pin D-sub connector (J2) labeled DS1038-15FBNSIA74-0CC. The connector pins are numbered 1 through 15, with pins 11, 12, 13, 14, and 15 labeled as VGASync, VGASync, VGASync, VGASync, and VGASync respectively. The connector is also connected to a 5V power supply and ground (GND) through capacitors C53 and C54 (100nF).

EXTERNAL VIDEO CONNECTOR

The diagram shows a 16-pin connector labeled J1. The pins are numbered 1 through 16. The connections are as follows:

- Pin 1: VGARED
- Pin 2: VGAGREEN
- Pin 3: VGABLUE
- Pin 4: 3V3
- Pin 5: GND
- Pin 6: 3V3
- Pin 7: GND
- Pin 8: 3V3
- Pin 9: 5V
- Pin 10: GND
- Pin 11: AUDIO
- Pin 12: AUDIO
- Pin 13: VGHSYNC
- Pin 14: VGAVSYNC
- Pin 15: 5V
- Pin 16: 3V3

EXTERNAL DISPLAY WITH AUDIO

Id: 7/7