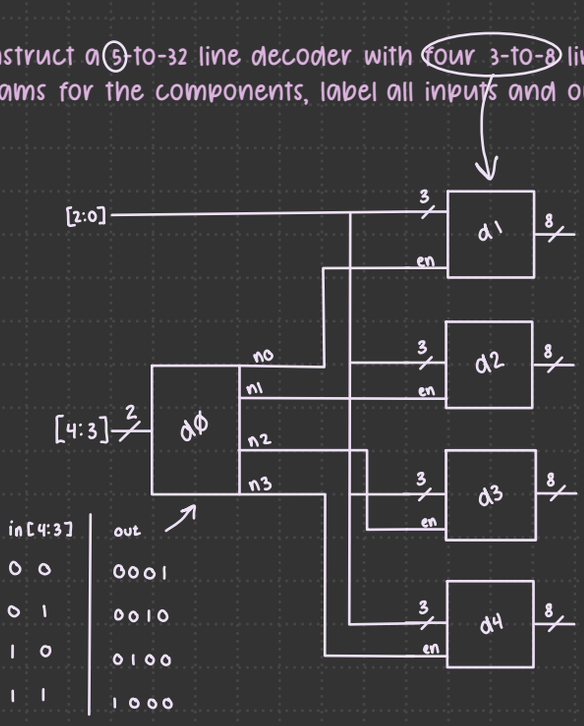
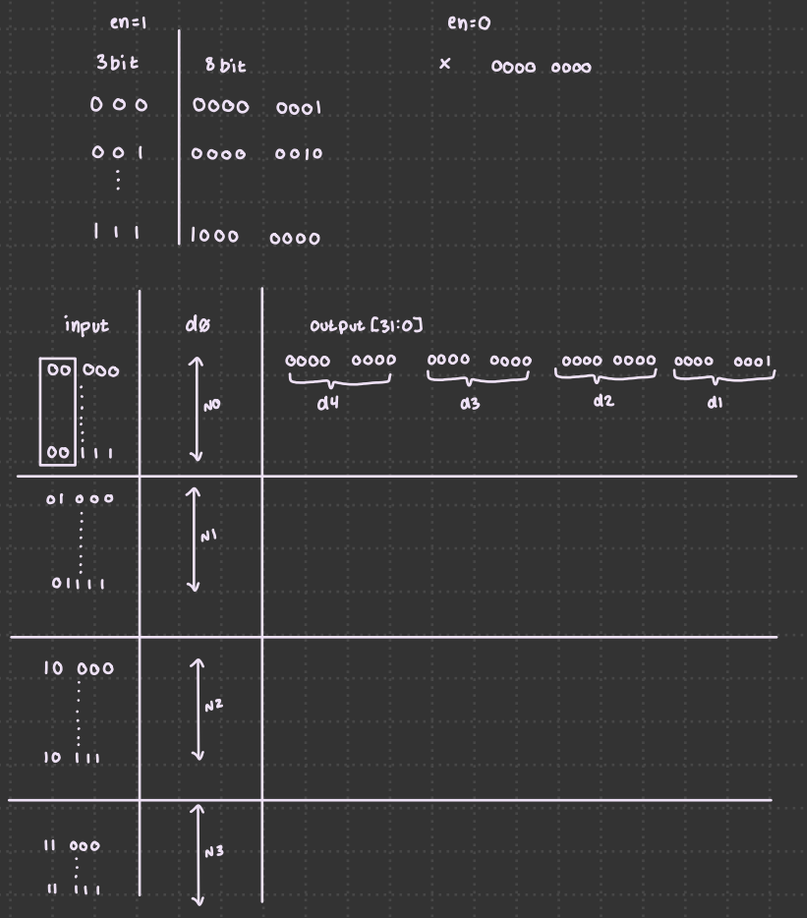
Title : hw 5 gianna galard

Date : 11 / 20 / 21

1. Construct a 5-to-32 line decoder with four 3-to-8 line decoder with enable and a 2-to-4 line decoder. Use block diagrams for the components, label all inputs and outputs.





2. A combinational circuit is defined by the following three Boolean functions:

F 1 = (y ′ + X) z

F 2 = y ′ z ′ + X ′ y + y z ′

F 3 = (X + y) z

Design the circuit with a decoder and external gates. Draw the diagram, and label all inputs and outputs. (Hints: turn each function to sum of minterms.)

d	x	y	z
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

$F1=(\bar{y}+x)z$

$=\bar{y}z+xz$

$=x\bar{y}z+\bar{x}\bar{y}z+xyz+x\bar{y}z$

101 001 111 101

5 1 7 5

$F2=\bar{y}\bar{z}+\bar{x}y+y\bar{z}$ (expand with redundancy law)

$=\boxed{x\bar{y}\bar{z}+\bar{x}\bar{y}\bar{z}}$

$\boxed{\bar{x}yz+\bar{x}y\bar{z}}$

$=\boxed{xy\bar{z}+\bar{x}y\bar{z}}$

$=x\bar{y}\bar{z}+\bar{x}\bar{y}\bar{z}+\bar{x}yz+\bar{x}y\bar{z}+xy\bar{z}+\bar{x}y\bar{z}$

100 000 011 010 110 010

4 0 3 2 6 2

$F3=(x+y)z$

$=xz+yz$

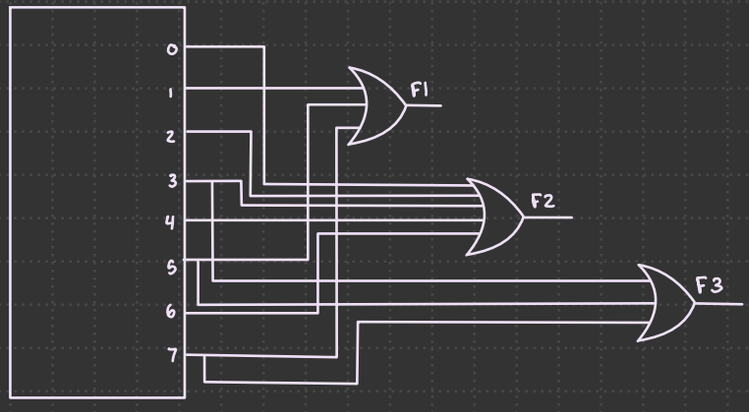
$=\boxed{xyz+x\bar{y}z}$

$=\boxed{xyz+\bar{x}yz}$

$=xyz+x\bar{y}z+xyz+\bar{x}yz$

111 101 111 011

7 5 7 3



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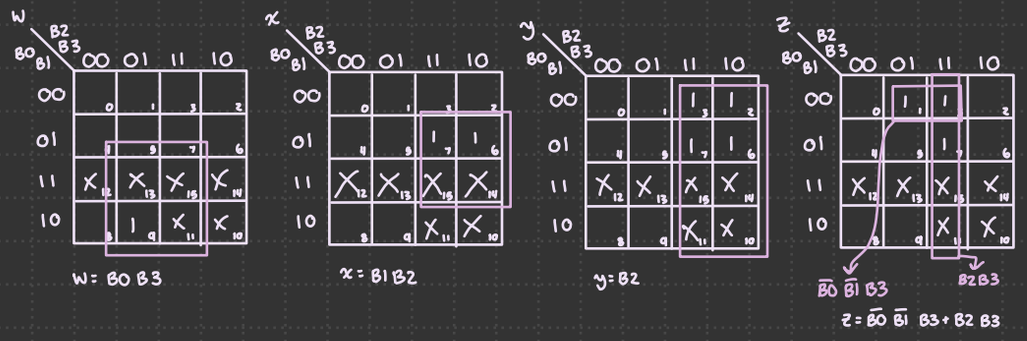
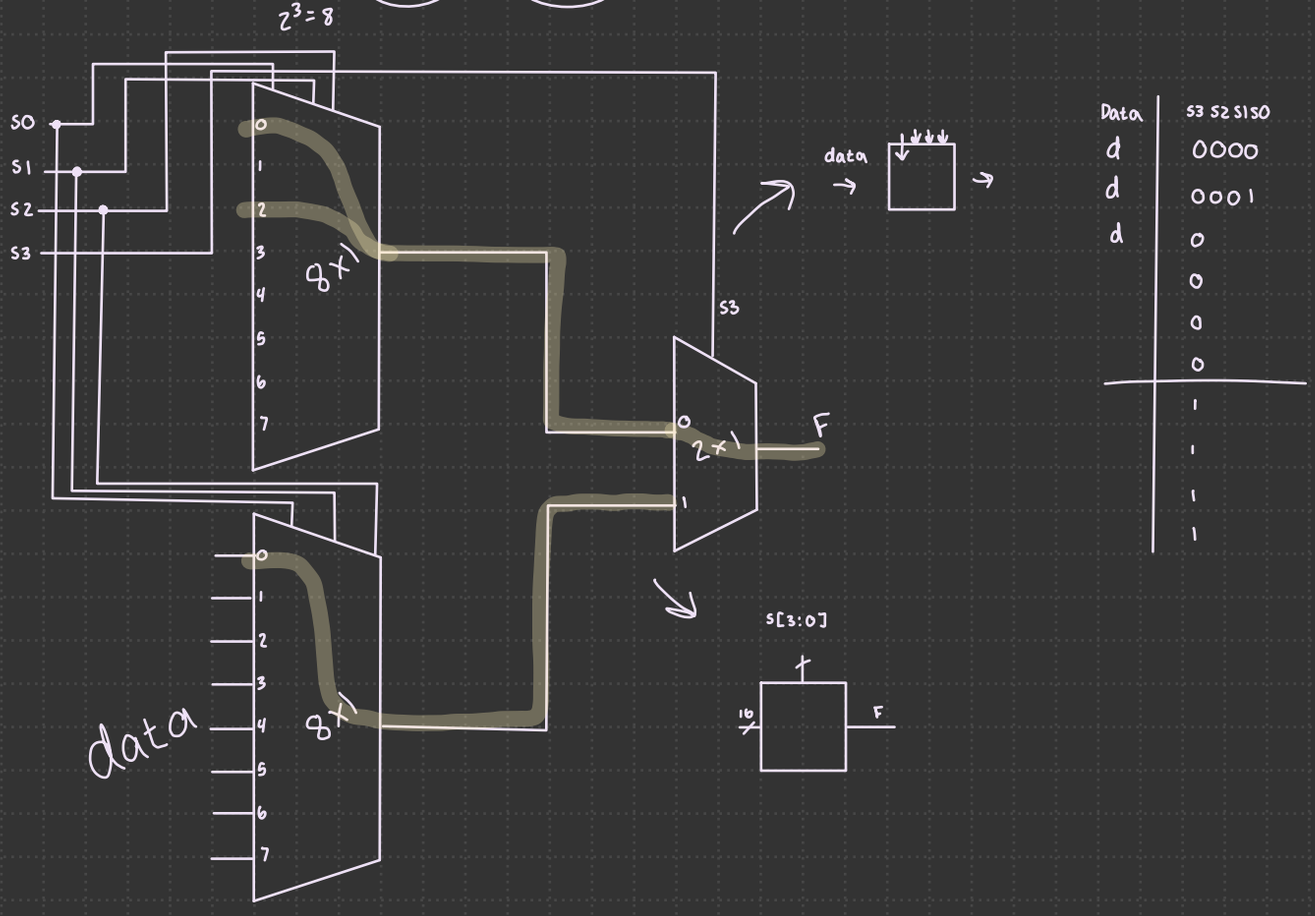
3. Design an active high BCD-to-decimal decoder using the unused combinations of the BCD code as don't-care conditions

B0	B1	B2	B3	w	x	y	z
0	0	0	0	0	0	0	0
0	0	0	1				
0	0	1	0				
0	0	1	1				
0	1	1	0				
0	1	1	1				
1	0	0	1	1	0	0	1
1	0	1	1	X	X	X	X
.	.	.	.	X	X	X	X
1	1	1	1	X	X	X	X



4. Construct a 16x1 multiplexer with two 8x1 and one 2x1 multiplexers. Use block diagrams and label all inputs and outputs.



Data	S3 S2 S1 S0
d	0000
d	0001
d	0
	0
	0
	0
	0
	1
	1
	1
	1

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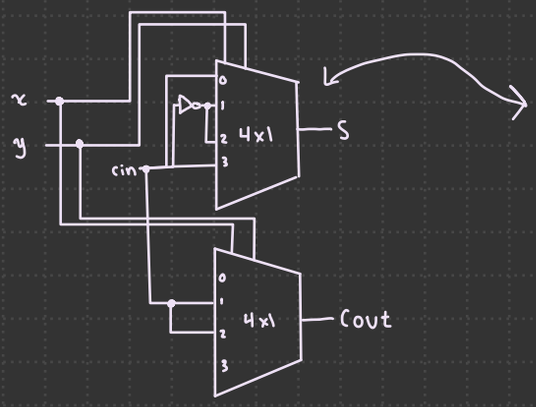
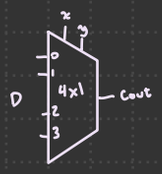
5. Implement a full adder with two 4x1 multiplexers. Draw the truth-table, diagram and label the inputs and outputs.

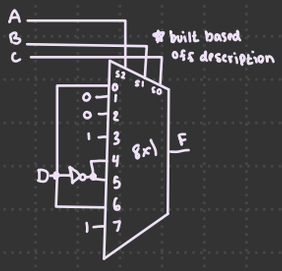
x	y	cin	s	cout	
0	0	0	0	0	S = cin, Cout = 0
0	0	1	1	0	
0	1	0	1	0	S = $\bar{cin}$, Cout = cin
0	1	1	0	1	
1	0	0	1	0	S = $\bar{cin}$, Cout = cin
1	0	1	0	1	
1	1	0	0	1	S = cin, Cout = 1
1	1	1	1	1	



x	y	Cout
0	0	0
0	1	1
1	0	2
1	1	3

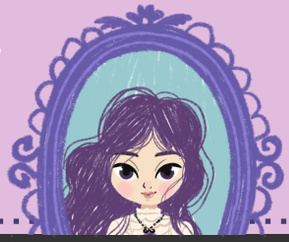


6. An 8x1 multiplexer has inputs A, B, And C connected to the selection inputs S2, S1, and S0, respectively. The data inputs I0 through I7 are as follows
I1 = I2 = 0, I3 = I7 = 1; I4 = I5 = D'; and I0 = I6 = D;
Determine the Boolean function that the multiplexer implements



Dec	A	B	C	D	F	
0	0	0	0	0	0	F=D
1	0	0	0	1	1	
						10
2	0	0	1	0	0	F=0
3	0	0	1	1	0	
						11
4	0	1	0	0	0	F=0
5	0	1	0	1	0	
						12
6	0	1	1	0	1	F=1
7	0	1	1	1	1	
						13
8	1	0	0	0	1	F=$\bar{D}$
9	1	0	0	1	0	
						14
10	1	0	1	0	1	F=$\bar{D}$
11	1	0	1	1	0	
						15
12	1	1	0	0	0	F=D
13	1	1	0	1	1	
						16
14	1	1	1	0	1	F=1
15	1	1	1	1	1	
						17

$F(A,B,C,D) = \bar{A}\bar{B}\bar{C}D + BC + A\bar{B}\bar{D} + ABD$



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7. Using a case statement, write an HDL behavioral description of an eight-bit arithmetic logic unit (ALU). The circuit has a three-bit select bus (Sel), 8-bit input datapaths (A[7:0] and B[7:0]), an eight-bit output datapath (y[7:0]), and performs the arithmetic and logic operations listed below.

Sel	Operation	Description
000	y = 8'b0	
001	y = A & B	Bitwise AND
010	y = A | B	Bitwise OR
011	y = A ^ B	Bitwise exclusive OR
100	y = ~ A	Bitwise complement
101	y = A - B	Subtract
110	y = A + B	Add (Assume A and B are unsigned)
111	y = 8'hFF	

```
module Alu(y,A,B,Sel)
// 8bit input datapaths
input [7:0] A,B;
// 3 bit bus
input [2:0] Sel;
output reg [7:0] y;

always @(A,B,Sel)
begin
case(Sel)
// follow given operations
    3'b000: y = 8'b0;
    3'b001: y = A & B;
    3'b010: y = A | B;
    3'b011: y = A ^ B;
    3'b100: y = ~A;
    3'b101: y = A - B;
    3'b110: y = A + B;
    3'b111: y = 8'hFF;
end case
end
endmodule
```