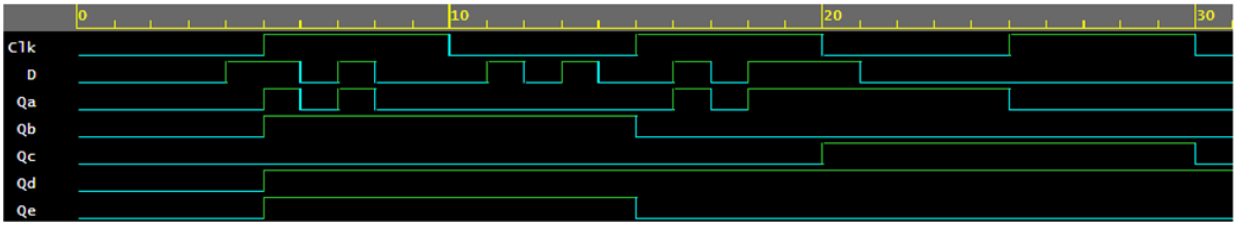
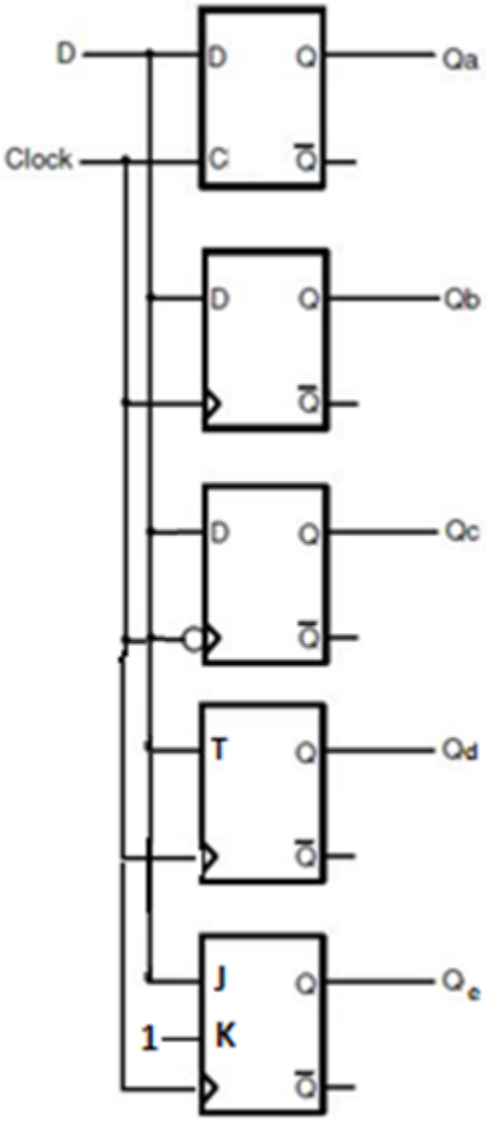
Homework: the following circuit and timing diagrams illustrate the differences between D-latch, rising edge triggered D flip-flop, falling edge triggered D flip-flop, T flip-flop, and JK flip-flop (the input K hardwired to 1). Write Verilog design codes and a testbench to reproduce the following waveforms. You need to initialize Q to 0 at the declaration (e.g. reg Q = 0;) for each flip-flop module. You can test all the flip-flops at once in one testbench.





Q_a = D (if C = 1)

Q_b = D (positive edge triggered)

Q_c = D (negative edge triggered)

Q_d = T Å Q_d (positive edge triggered)

Q_e = J Q_e' + K' Q_e (positive edge triggered), K =1

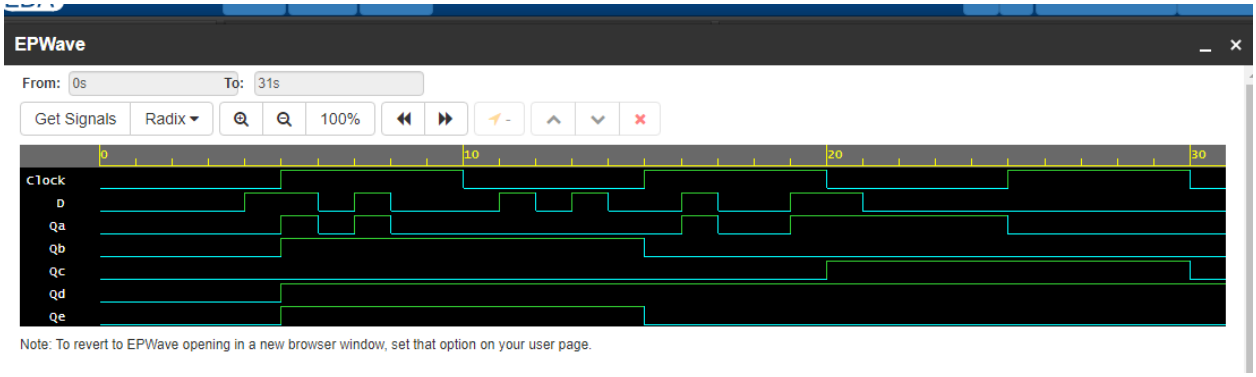
testbench.sv

```
// Gianna Rose
// Lab 10 HW
// https://www.edaplayground.com/x/7uAZ


  module testAll;
   // Clock and D inputs
   reg  Clock, D;
   // Qa-Qe are the outputs
         wire Qa, Qb, Qc, Qd, Qe;



    // instantiate the UUT
    differences uut(D, Clock, Qa, Qb, Qc, Qd, Qe);

   // generate the clock signal
    initial
       begin
            Clock = 0;
            forever  #5 Clock = ~Clock;
      #200 $finish;
      end

          initial
       begin
$dumpfile("dump.vcd");
   $dumpvars(1, testAll);

         D=0;
     #4 D=1;
     #2 D=0;
     #1 D=1;
     #1 D=0;
     #3 D=1;
     #1 D=0;
     #1 D=1;
     #1 D=0;
     #2 D=1;
     #1 D=0;
     #2 D=1;
     #2 D=0;
     #10 $finish;
```

```
   end
      endmodule
```

```
design.sv
// Gianna Rose
// Lab 10 HW
// https://www.edaplayground.com/x/7uAZ

module differences(D,Clock,Qa,Qb,Qc,Qd, Qe);

// input data and clock
input D, Clock;

// output registers
output reg Qa = 0,Qb = 0,Qc = 0,Qd = 0,Qe = 0;

// JK FF
 reg K = 1;
initial
  Qd <= 0;

//D-Latch
always@(*)
  if(Clock)
    Qa <= D;

  always @ (posedge Clock)
begin
  // rising edge triggered d flip flop
  Qb <= D;
if(D)
  // t flip flop
  Qd <= ~Qd;
end

  // falling edge triggered d flip flop
  always@(negedge Clock)
Qc <= D;

  // JK FF
  always@(posedge Clock)
    Qe <= (D & ~Qd) | (~K & Qd);

endmodule
```

Output



https://www.edaplayground.com/x/7uAZ