920768

Computer concepts CSCM53

Question 1

a) The problem faced in networking is corrision and delay in transferring packets from one node to another node because packets are carried to both directions. Before each node sends a message, it has to listen first to the channel if there is no other message being carried in the line.

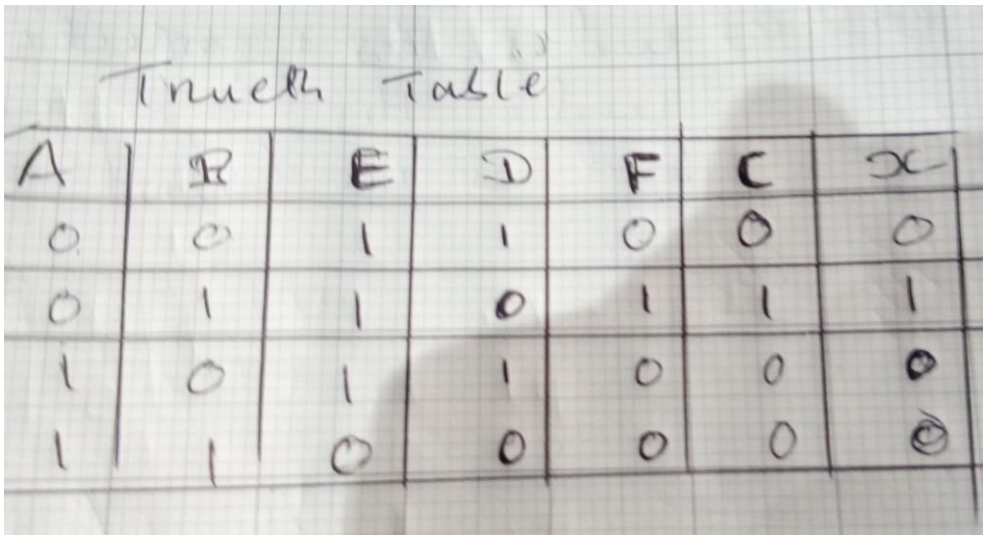
b) Carrier-sense multiple access with collision detection (CSMA/CD) is used to detect if the line is free and detect any errors if there was a collision so that the node should be informed to resend the packet again if another node is not using the line

c) The data rate transfer or bandwidth will decrease as more devices are scrambling for the same throughput, which later slows down the network and lead to delay in data transfer. Sometimes other users may not even be able to access some network resources to low network speed.

d) Yes the latency could be there if there are nodes that are connected. The more the nodes the wider the ring and the delay or the longer it takes in transferring packets from node to another

Question 2

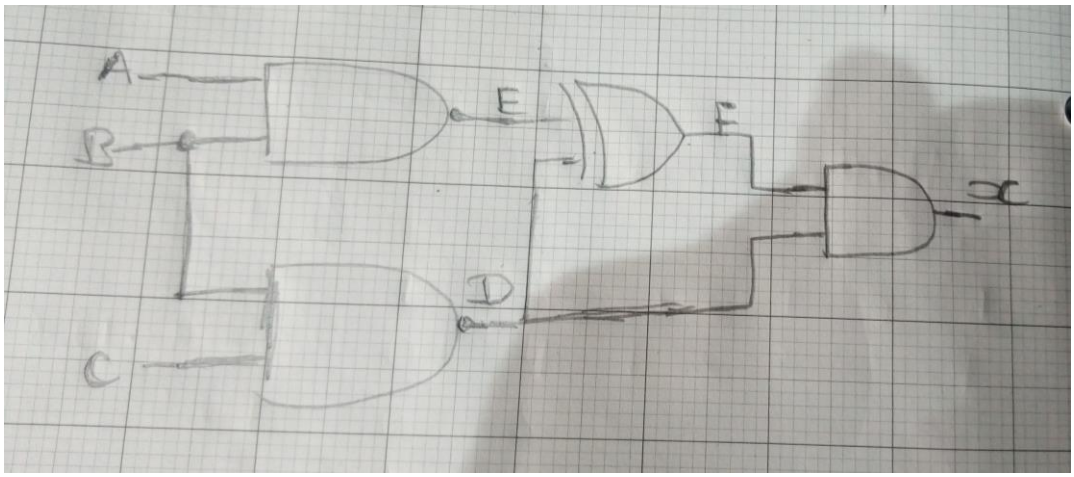
a)



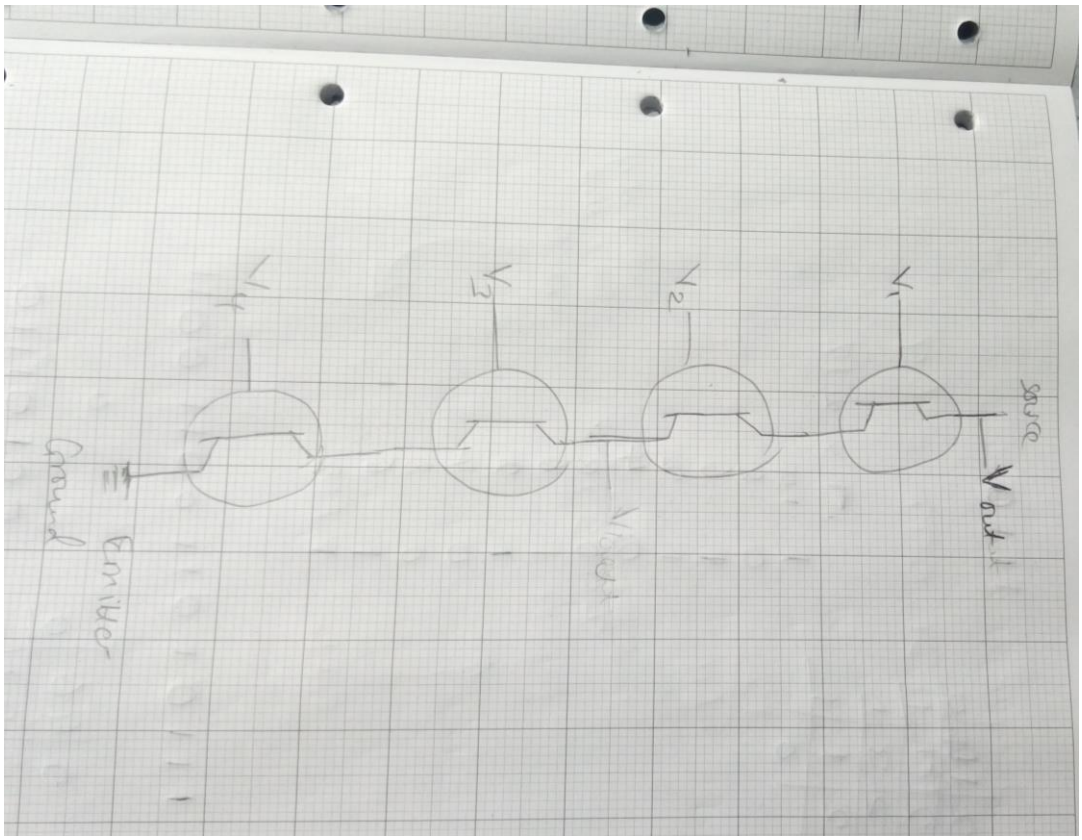
Truth Table

A	B	E	D	F	C	X
0	0	1	1	0	0	0
0	1	1	0	1	1	1
1	0	1	1	0	0	0
1	1	0	0	0	0	0

b)



c)



Question 3

a) 1110101100110011
b) -46 to 8bit 2's complement
00101110 then invert the bits

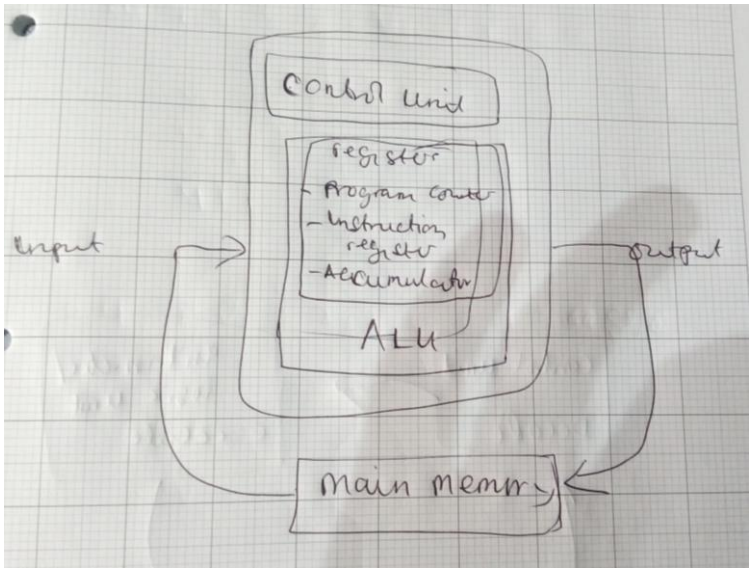
Therefore -46 = 11010010

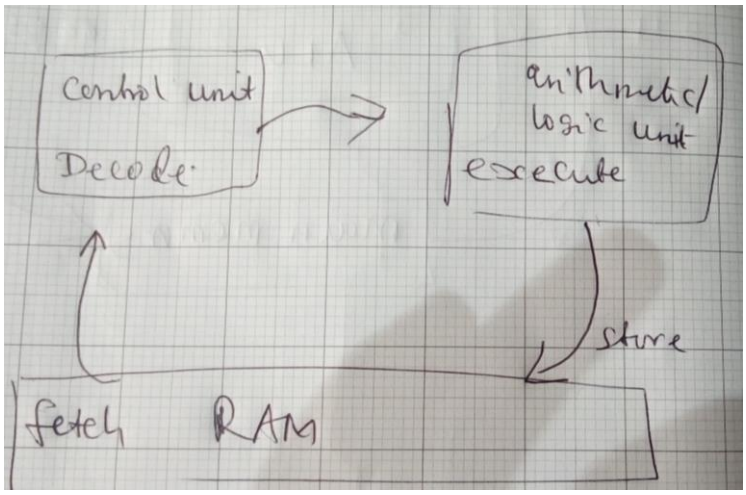
Question 4

a) 24, 7,8,3,2,2,2,0,0,1, *55,0
Compression Ration = 64:12
CR =**5.333**
b) The original file size is 131,072
Therefore after compressing the file size is **24,576**

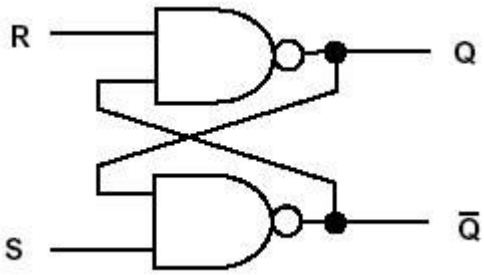
Question 5

a) The CPU fetches the instruction from the main memory into the registers where it is decoded and processed and executed. The program counter register store information the information the address of the next instruction to be executed. Next, we have the instruction register that stores the current instruction to be executed. Another register is the Accumulator which store data are taken from memory

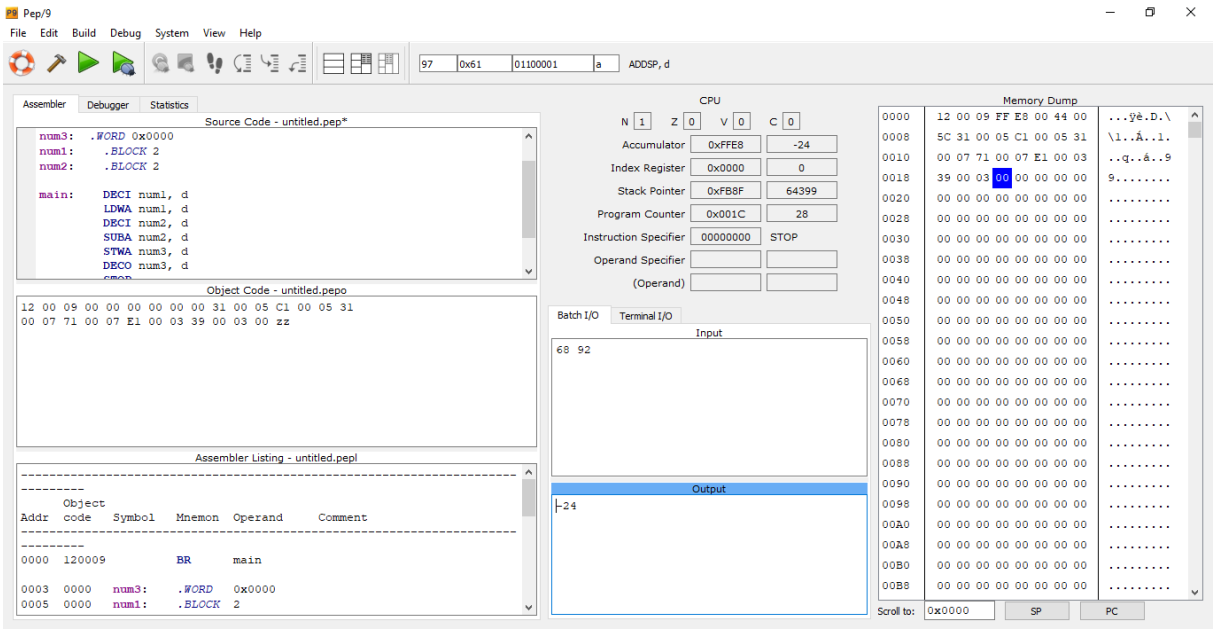




b) The Arithmetic/Logic Unit is the one that corresponds to the diagram below



c)



Source code

BR main

num3: .WORD 0x0000

num1: .BLOCK 2

num2: .BLOCK 2

main: DECI num1, d

LDWA num1, d

```
        DECI num2, d
        SUBA num2, d
        STWA num3, d
        DECO num3, d
        STOP
.END
```

Object code

```
12 00 09 00 00 00 00 00 00 31 00 05 C1 00 05 31
00 07 71 00 07 E1 00 03 39 00 03 00 zz
```

Assembler listing

```
-------------------------------------------------------------------------------
     Object
Addr  code   Symbol   Mnemon  Operand     Comment
-------------------------------------------------------------------------------
0000  120009         BR      main

0003  0000   num3:    .WORD   0x0000
0005  0000   num1:    .BLOCK  2
0007  0000   num2:    .BLOCK  2

0009  310005 main:    DECI    num1,d
000C  C10005          LDWA    num1,d
000F  310007          DECI    num2,d
0012  710007          SUBA    num2,d
0015  E10003          STWA    num3,d
0018  390003          DECO    num3,d
001B  00              STOP
```

001C .END

Symbol table

Symbol	Value	Symbol	Value
main	0009	num1	0005
num2	0007	num3	0003

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d) 0x0007, 0x0003