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CS271

ALL 4

untitled.S - [Unsaved] - Visual Studio Code

File Help

New Open Save Settings Tools Emulation Complete Line: 39 Column: 0

Execute Reset Step Backwards Step Forwards

Reset to continue editing code

```
1 ; Using Logical Shifts
2 ; In a logical shift, bits that "fall off" are discarded
3 ; 0's are always used to fill blanks
4 MOV r1, #0x12 ; r1 = 0000 ... 0000 0001 0010
5 ; Shift 4 bits or 1 hex digit to the left
6 LSL r2, r1, #4 ; r2 = 0000 ... 0001 0010 0000
7 ;
8 MOV r3, #0x12 ; r3 = 0000 ... 0000 0001 0010
9 ASR r4, r3, #2 ; r4 = 0000 ... 0000 0000 0100
10 ;
11 ; Shift r3 by number of bits in r4 (4), result in r5
12 LSL r5, r3, r4 ; using register addressing instead of immediate addressing
13 ;
14 ; Right Rotate Examples
15 MOV r1, #0x12 ; r1 = 0000 0000 ... 0000 0001 0010
16 ROR r2, r1, #1 ; r2 = 0000 0000 ... 0000 0000 1001
17 ROR r3, r2, #4 ; r3 = 1001 ... 0000 0000 0000
18 ;
19 ; Rotate left, instead rotate left x bits with ROR by (22-x)
20 MOV r5, #0x12 ; r5 = 0x12
21 ; Rotate r5 left 12 bits by ROR (32-12) = 20 bits; answer in r6
22 ROR r6, r5, #20 ; r6 = 0x12000
23 ;
24 ; TEST Comparison opcodes and observe the CPSR status bits
25 MOV r7, #1
26 MOV r8, #1
27 MOV r9, #3
28 ; ROR, #1 ; Complemented bit value of 3
29 ; and CRR examples
30 CMP r7, r8 ; SUBTRACT Same, so Zero flag set
31 CMP r7, r9 ; SUBTRACT Not the same so no flags
32 CMN r7, r8 ; ADD same, so no flags
33 CMN r7, r9 ; ADD Opposite sign, so Zero flag set
34 ; TEST examples; Pay attention to the N and Z flags
35 TST r7, r8 ; BITWISE ANDS
36 TST r7, r10 ; BITWISE ANDS
37 TEQ r7, r8 ; BITWISE EORS
38 TEQ r7, r10 ; BITWISE EORS
39
```

Register Window:

Register	Value	Dec	Bin	Hex
R0	0x0	0		
R1	0x10010	65536		
R2	0x1001	65537		
R3	0b100100000000000000000000...			
R4	0x100	256		
R5	0x10010	65536		
R6	0b100100000000000000000000...			
R7	0x11	17		
R8	0x11	17		
R9	0xFFFFFDD	4294967293		
R10	0b111111111111111111111111...			
R11	0x0	0		
R12	0x0	0		
R13	0xFF000000	4294967040		
LR	0x0	0		
PC	0x64	100		

Clock Cycles: Current Instruction: 1 Total: 23

CPSR Status Bits (NZCV): 1 0 1 0

untitled.S - [Unsaved] - Visual Studio Code

File Help

New Open Save Settings Tools Emulation Complete Line: 9 Column: 0

Execute Reset Step Backwards Step Forwards

Reset to continue editing code

```
1 MOV R1, #1
2 LSL R1, R1, #1
3 LSL R1, R1, #1
4 LSL R1, R1, #1
5 LSL R1, R1, #1
6 LSL R1, R1, #1
7 LSL R1, R1, #1
8 LSL R1, R1, #1
9 LSL R1, R1, #1
10
```

Register Window:

Register	Value	Dec	Bin	Hex
R0	0x0	0		
R1	256	256		
R2	0x0	0		
R3	0x0	0		
R4	0x0	0		
R5	0x0	0		
R6	0x0	0		
R7	0x0	0		
R8	0x0	0		
R9	0x0	0		
R10	0x0	0		
R11	0x0	0		
R12	0x0	0		
R13	0xFF000000	4294967040		
LR	0x0	0		
PC	0x28	40		

Clock Cycles: Current Instruction: 1 Total: 9

CPSR Status Bits (NZCV): 0 0 0 0

untitled5 - [Unsaved] - VisUAL

FileHelp

NewOpenSaveSettingsTools

Emulation CompleteLine: 1000000

ExecuteResetStep BackwardsStep Forwards

Reset to continue editing code

1MOV R1, #256

2LSR R1, R1, #1

3LSR R1, R1, #1

4LSR R1, R1, #1

5LSR R1, R1, #1

6LSR R1, R1, #1

7LSR R1, R1, #1

8LSR R1, R1, #1

9LSR R1, R1, #1

10

R00x0DecBinHex

R11DecBinHex

R20x0DecBinHex

R30x0DecBinHex

R40x0DecBinHex

R50x0DecBinHex

R60x0DecBinHex

R70x0DecBinHex

R80x0DecBinHex

R90x0DecBinHex

R100x0DecBinHex

R110x0DecBinHex

R120x0DecBinHex

R130xFF000000DecBinHex

LR0x0DecBinHex

PC0x28DecBinHex

Clock Cycles

Current Instruction: 1Total: 9

CSPR Status Bits (NZCV)0000