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1. Correct Design part 1 (90 pts)

   You need to run a timing analysis to determine the minimum period.

FYI: Clock Frequency is 1/period

Design	#number of LUTs (% util)	# of Dffs (%util)	Minimum Period (%logic, % route)	Clock Freq (MHz)
fifo.v	15 (1%)	6 (1%)	5.091 ns (60.2% logic, 39.8% route)	196.43 MHz

2. Question (5 pts): For your design, assume the write counter value is "3", and the read counter value is "5". How many elements are in the FIFO?

   6 Elements

3. Question (5 pts): A "memory collision" in a true dual port memory occurs when the same location is accessed in the same clock cycle by the two ports, either both write (write-write collision) or one read/one write (read-write collision). Reading the same location from both ports is not a collision. Your FIFO uses a true dual port memory. Specify a condition in which a memory collision can occur in your FIFO.

   If the FIFO is empty and a write and a read comes in on the same clock cycle this could cause a memory collision.