

NSLSAT3 payload system spec

Copyright

NSLComm Ltd

Kineret 12, Airport City

POB: 1033

ISRAEL

VAT Number: 515229169

*Notice*

The content of this document is subject of copyright of NSLComm. Therefore, this document shall not be disclosed to any third party without the prior written approval of NSLComm.

**Approval signatures**

|  |  |  |  |
| --- | --- | --- | --- |
|  | Name | Date | Signed |
| **Author** | Gilad Danin |  |  |
| **Reviewers** |  |  |  |
| **Ext. Reviewers** |  |  |  |
| **Approved** |  |  |  |

**Document control**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| Rev | Date | Section | Description of change | Reason for change |
| 1.0.0 |  |  |  |  |
|  |  |  |  |  |

**Related documents**

|  |  |  |
| --- | --- | --- |
| No. | Document name | Document reference |
| [RD-1] |  |  |

Contents

[1. Scope 6](#_Toc154329550)

[2. Glossary 7](#_Toc154329551)

[3. Mission Overview 8](#_Toc154329552)

[3.1. Satellite Services 8](#_Toc154329553)

[3.2. Satellite Description 8](#_Toc154329554)

[3.3. Payload Description 9](#_Toc154329555)

[4. Modes of operation 11](#_Toc154329556)

[4.1. Channelizer only 11](#_Toc154329557)

[4.2. Regenerative only 15](#_Toc154329558)

[4.3. Channelizer + regenerative mode 16](#_Toc154329559)

[4.4. Store and forward mode 18](#_Toc154329560)

[5. Algorithmic architecture 19](#_Toc154329561)

[5.1. Channelizer 21](#_Toc154329562)

[5.2. Regenerative Modem Specifications 22](#_Toc154329563)

[5.3. Channelizer to Modem Processing Stage (CMPS) 22](#_Toc154329564)

[6. HW architecture 23](#_Toc154329565)

[6.1. RF and RFFE 23](#_Toc154329566)

[6.2. IPB 23](#_Toc154329567)

[6.3. HW interfaces 23](#_Toc154329568)

[6.4. Power management and distribution 23](#_Toc154329569)

[7. The Versal 1502 component 24](#_Toc154329570)

[7.1. NoC (Network on chip) 25](#_Toc154329571)

[7.2. Platform Management Controller 25](#_Toc154329572)

[7.3. The Processing System (PS) 27](#_Toc154329573)

[7.4. Configurable Logic Block (CLB) 29](#_Toc154329574)

[7.5. Internal Memory 29](#_Toc154329575)

[7.6. Digital Signal Processing (DSP) 30](#_Toc154329576)

[7.7. Exact component definition and resource count 31](#_Toc154329577)

[8. FW architecture 33](#_Toc154329578)

[8.1. Modes of operation in details 33](#_Toc154329579)

[8.2. Chip organization 33](#_Toc154329580)

[9. SW architecture 34](#_Toc154329581)

[10. Mechanical and Thermal concepts 34](#_Toc154329582)

[10.1. Anntenas 35](#_Toc154329583)

[10.2. Gimbals 35](#_Toc154329584)

[11. FDIR and Redundancy and RDP 35](#_Toc154329585)

[12. Operation Concepts 35](#_Toc154329586)

[13. Verification and Validation 35](#_Toc154329587)

List of Figures:

Figure 1: Channelizer terminology 12

Figure 2: Channelizer mode terminals🡪 gateway spatial-spectral description. 12

Figure 3: Not allowed setups for channelizer 13

Figure 4:Channelizer mode Gateway🡪 terminals spatial-spectral description. 14

Figure 5: Channelizer mode – general block diagram 14

Figure 6: Regenerative mode terminals 🡪gateway spatial-spectral description. 15

Figure 7: spatial-spectral description 16

Figure 8: Regenerative mode - general block diagram 16

Figure 10: Channelizer+Regenerative mode input/output spectral view 17

Figure 11: Channlizer+Regenerative mode - general block diagram 18

Figure 12: store and forward mode - general block diagram 18

Figure 13: store and forward mode input/output spectral view 19

Figure 14: Versal Device Layout 25

Figure 15: Versal processing system and surrounding blocks 27

Figure 16: Versal CLB architecture 29

Figure 17: Versal DSP slice architecture 30

List of Tables:

[Table 1 Satellite’s main characteristics 8](#_Toc154329604)

[Table 2: Mission characteristics 9](#_Toc154329605)

[Table 3: principle channelizer characteristics 10](#_Toc154329606)

[Table 4: Payload principle characteristics 11](#_Toc154329607)

[Table 5: Channelizer mode parameters and spectral definitions 19](#_Toc154329608)

[Table 6:Regenerative mode parameters and spectral definitions 20](#_Toc154329609)

# Scope

This document contains system definitions and specifications of the payload of SAT3.

# Glossary

Each document shall include a table of glossary terms:

|  |  |
| --- | --- |
| Acronyms | |
| Term | Definition |
| ALC | Automatic Level Control |
| CH\_NFFT | Channelizer FFT size |
| CH\_BW | Channelizer band width |
| NPR | Noise Power Ratio |
| PS | Processing System |
| PL | Programmable Logic |
| NoC | Network On Chip |
| CMPS | Channelizer to Modem Processing Stage |
| WBA | Wide Beam Antenna |
| NBA | Narrow Beam Antenna |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |
|  |  |

# Mission Overview

## Satellite Services

NSLSAT3 provides a wide range of applications and services, including but not limited to:

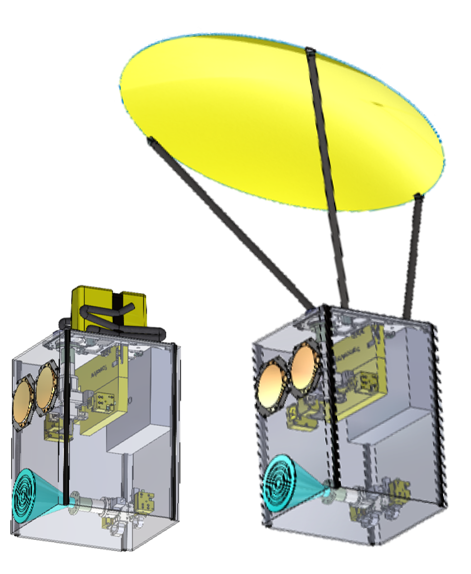
1. Several broadband links in Ka-band:
   * + Communication between remote two locations spanning hundreds of kilometers in a full duplex configuration. This service can be implemented with either digital bent pipe connectivity using a real-time relay channelizer or DVB-S2 regenerative mode (on-board space modem).
     + Ability for several terminals communication with GEO (channelizer) and once the LEO is passing by, they switch to the NanoSat, also channelizer and get a much higher bitrate for a few minutes.
2. Store and Forward capability with high storage memory.
3. Geo interference location: scan and locate Geo interferer using algorithm and scan of the wide beam and narrow beam.
4. Full duplex, two-way S-band connectivity enabling bidirectional Internet of Things (IoT) applications and demonstrating tactical comms on the move (optional).
5. Cross-connect between any antenna and any frequency band in both modes (Cross-Beam, Cross-Band).
6. Advanced research applications, such as LEO-GEO, geo-location capabilities and tactical 5G from space.

## Satellite Description

NSLSAT-3 is a nanosatellite platform hosting a full suite of avionics that will enable the spacecraft to meet all system requirements whilst leaving sufficient resources available for the payload.

|  |  |
| --- | --- |
| Feature | Description |
| Size | Up to ~12U |
| Mass | Up to ~20 kg |
| Propulsion | TBD [depends on the planned altitude and de-orbiting regulations] |
| Pointing accuracy | Expandable antenna 0.2 deg.  Wide beam 0.5 deg. |
| Power Consumption (Peak) | 90-140W (TBC) |
| TT&C Radio | VHF: 149 MHz  UHF: 402 MHz  LHCP/RHCP |

Table Satellite’s main characteristics



**Figure 1**: Illustration of NSLSAT-3

NSLSAT3 mission characteristics is described in

|  |  |
| --- | --- |
| Feature | Description |
| Size | CubeSat (up to ~12U) |
| Altitude | 500-720 km pending on suitable launch opportunity. |
| Lifetime | ~3 years |
| Orbit | SSO or inclined orbit |
| Earth coverage diameter (Field of View) | 1500-2500 km (depends on the final orbit altitude) |
| Payload operational duty cycle | 3 hours operation in a 24-hour period |
| Communication services | Ka band Real time relay (channelizer or regenerative)  Ka band Store and Forward (regenerative)  Optional: Two-way S band IoT and tactical comms. |

Table : Mission characteristics

## Payload Description

The payload consists of the following key elements:

* Hardware: An SDR based on Xilinx VERSAL SoC supporting both regenerative mode and digital transparent switching (channelizer).
* Firmware: Broadband channelizer, and regenerative “store and forward” modes.
* ~60 cm expandable, gimbaled Ka-band antenna.
* Additional small size wide beam Ka antenna to allow additional connectivity in high SNR conditions and enhanced operational connectivity and flexibility.
* Two-way S-band antenna with transmitting and receiving communication channels (optional).
* RF chain structure including transceiver, up/down converters, PA, LNA etc.
* Cameras for deployment accuracy measurements and space awareness (optional).

The following drawing depicts the payload high level architecture:

A diagram of a computer network

Description automatically generated

**Figure 2**: Payload Architecture

Table 3 summarizes the main payload characteristics. Values are estimated and may be changed according to the mission.

Table : principle channelizer characteristics

Table 4 depicts the principle payload characteristics:

|  |  |
| --- | --- |
| Feature | Description |
| Radio | 3 Full Duplex feeding systems: 2 in Ka band and 1 in S band  Digital Channelizer BW: up to 400 MHz  Regenerative mode SR: Tx: 200 MSps,  Rx: 60 MSps  Waveforms:   * DVBS2x up to 32APSK 9/10. Efficiency 4.5b/S * Proprietary: HiSky and others, TBD |
| Storage | 1 Tbyte |
| Ka-band expandable antenna | Tx: 19.2-21.2 GHz  Rx: 29-31 GHz  LHCP/RHCP  EIRP: 38.2 dBw  G/T 13.3 dB/K  Beam Diameter: 10-20Km |
| Ka band wide beam antenna | Tx: 19.2-21.2 GHz  Rx: 29-31 GHz  LHCP/RHCP  EIRP: 23 dBw  G/T: -1.8 dB/K  Beam Diameter: 75-115Km |
| S-band (optional) | Tx: 2.2-2.3 GHz  Rx: 2.2-2.3 GHz  LHCP/RHCP  EIRP: 6.5dBw  G/T: -19 dB/K |

Table : Payload principle characteristics

# Modes of operation

## Channelizer only

### Channelizer terminology

For clarity the following notation will be used to describe the channelizer spectral references:

* Signal – a wide band input or output to the channelizer. As there are 2 Ka RX/TX beams, each occupying 2 signals, situated side by side, there are up to 4 input signals and 4 output signals.
* Channel – a spectral band holding a communication waveform. There up to CH\_NFFT (to be defined in TBD) channels.
* Sub-channel – a spectral slice within the channelizer supported BW space, CH\_BW (to be defined in TBD). A sub channel can be occupied or not.

A diagram of a channel

Description automatically generated

Figure 1: Channelizer terminology

### Mission description

#### Terminals to gateway

A diagram of a satellite and a diagram of a planet

Description automatically generated

Figure 2: Channelizer mode terminals🡪 gateway spatial-spectral description.

Signals transmitted from terminals located within the spot of the wide beam antenna are received at various spectral bands and powers. The result is a wide band signal (whose band width is designated as BM\_BW, see Table 5), constructed from terminal related channels, at as defined in Table 5.

The target of the channelizer is to re-order the channels according to a pre-determined plan and transmit the resulting signal to the gateway.

The channels ensemble should obey to the following rules:

* Channel BW should not exceed CH\_MAX\_CHANNEL\_BW (see Table 5)
* Each sub-channel should occupy all or part of a single channel. That is, a situation where two channels share a sub channel is not allowed.

A diagram of a graph

Description automatically generated

Figure 3: Not allowed setups for channelizer

The granularity of the channelizer is defined by CH\_SUB\_CHANNEL\_BW (channelizer sub channel BW, see Table 5). It is determined by the CH\_NFFT parameter and some spectral characteristics of the RF chain, which drives/syncs the channelizer inputs/outputs (see TBD for details).

Processing characteristics:

* Any input sub-channel can be routed to any output sub-channel. This includes sub-channel duplication and nulling.
* Channelizer supplies digital amplification on a sub-channel basis for ALC implementation.

#### Gateway to terminals

The gateway to terminals communication is based on a muti-cast scheme. The gateway transmits a single carrier holding either:

1. Information aimed for all terminals.
2. Dedicated information, on an ID basis, encoded in the TBD layer.

A diagram of earth with a satellite

Description automatically generated

Figure 4:Channelizer mode Gateway🡪 terminals spatial-spectral description.

Practically the down link signal transmitted to the terminals is identical to the up-link signal received from the gateway. Thus, no computation is applied here (apart than a possible digital gain).

A simplified block diagram of the channelizer mode implementation is brough in Figure 5:

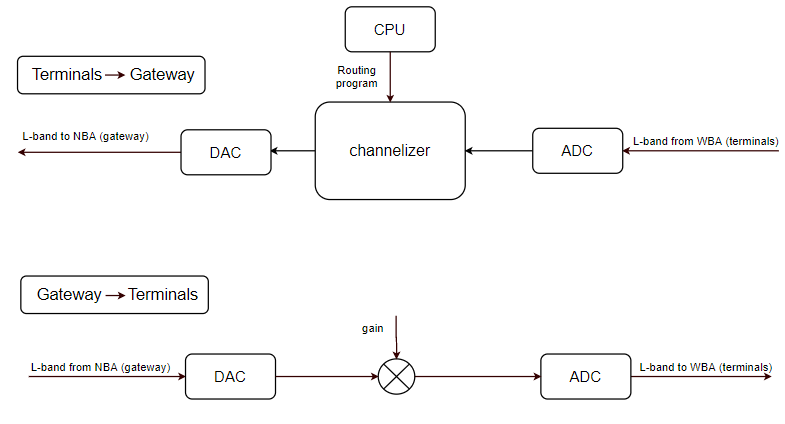
****

Figure : Channelizer mode – general block diagram

## Regenerative mode

### Terminals to gateway

Similar to the channelizer mode, the received signal is constructed from terminal related channels, at . Though, the spectral constraints on the terminal output signals are different, due to the computation demands from the SDR:

* Channel BW should not exceed RG\_TRM\_GW\_BW (see Table 6)
* Channels should lie with RG\_INTER\_CHANNEL\_SB from each other to ease the demodulation process.

The SDR supports up to RG\_N \_UL\_CHANNELS (Table 6). Thus, the beam BW is divided into equal slices, RG\_TRM\_GW\_BW wide, where:

RG\_TRM\_GW\_BW = BM\_BW/ to RG\_N \_UL\_CHANNELS

A diagram of a planet with different colored lines

Description automatically generated with medium confidence

Figure 6: Regenerative mode terminals 🡪 gateway spatial-spectral description.

After the terminals payloads were extracted, they are re-arranged and transmitted to the gateway as a single carrier signal.

Note:

The gradient coloring in Figure 6 designates that the channels are processed in a “regenerative” manner (unlike the “transparent” manner of the channelizer mode). This coloring differentiation will be used also in the hybrid mode to differentiate the channels according to their processing manner (see ‎4.3)

### Gateway to terminals

Similar to the channelizer (transparent) case, the uplink signal in principle is a replica of the uplink signal. In this case, though, it is being demodulated and re-modulated to enhance the link’s overall SNR.

A diagram of earth with a satellite

Description automatically generated

Figure 7: Regenerative mode gateway 🡪 terminals spatial-spectral description.

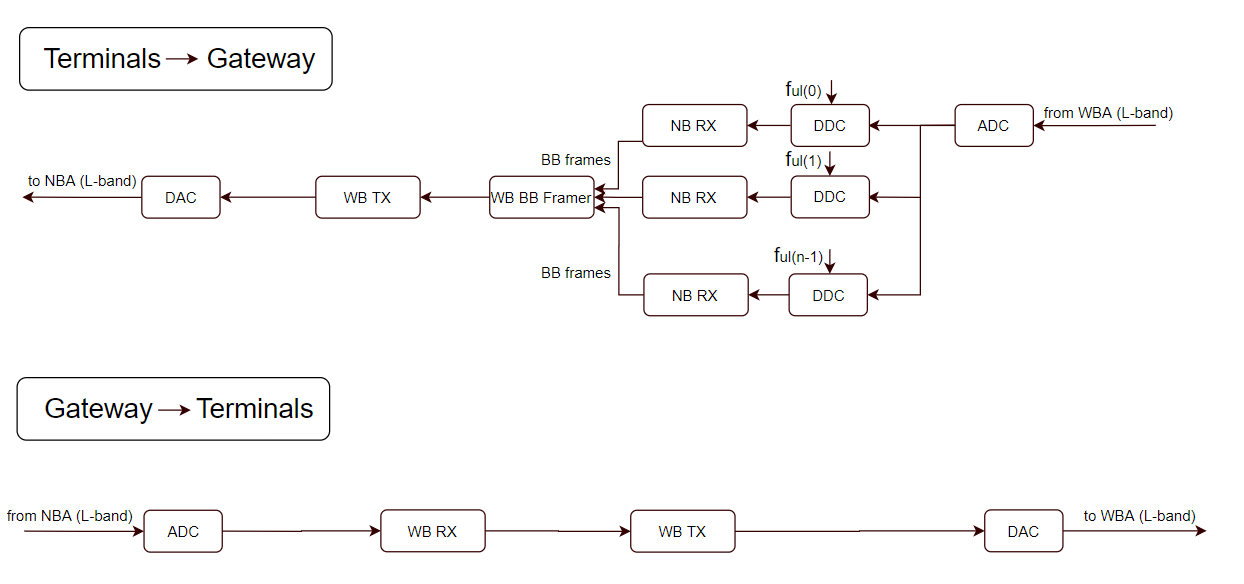
Principle block diagrams of both processing paths are brough in Figure 8. 

Figure : Regenerative mode - general block diagram

## Hybrid mode

The hybrid mode as its name implies is some mixture of previous channelizer and regenerative modes.

Two approaches are considered here:

### Orthogonal

Input and output beams spectra are divided to two separate, size equaled sections:

* Transparent
* Regenerative

Note the gradient coloring of the regenerative section.

A diagram of a satellite

Description automatically generated

Figure 9: Hybrid (orthogonal) mode terminals 🡪 gateway spatial-spectral description.

A diagram of a flowchart

Description automatically generated

Figure 10: Hybrid (orthogonal) mode - terminals 🡪 gateway general block diagram.

The gateway to terminals path processes a single carrier in a regenerative manner:

A diagram of a satellite

Description automatically generated

Figure 11:Hybrid (orthogonal) mode gateway 🡪 terminals spatial-spectral description.

Adequately the implementation is identical to the fully regenerative mode:

A white rectangular object with a black line

Description automatically generated with medium confidence

Figure 12: Hybrid (orthogonal) mode – gateway 🡪 terminals general block diagram

### True hybrid

Here, rather than splitting the input and output spectra to transparent and regenerative “zones”, channel regeneration is applied to chosen intermediate sub-channels.

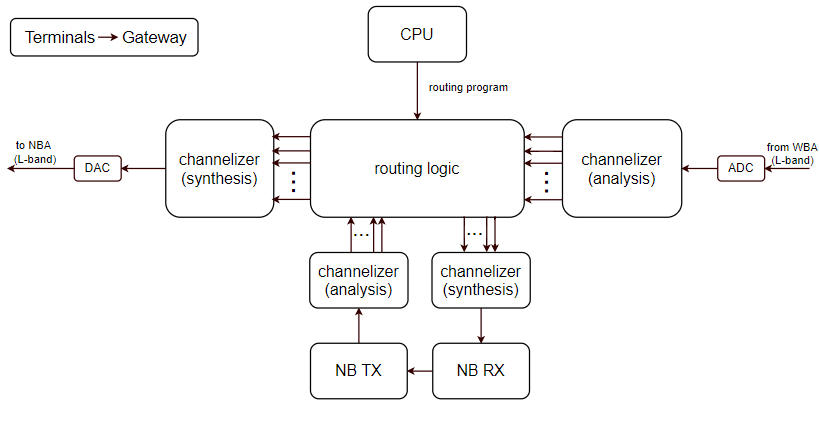


Figure 13:Hybrid (True) mode –terminals 🡪 gateway general block diagram.

The sampled signal is split into a vector of sub-channels (analysis channelizer). The routing program contains (in addition to the standard channelization program) the channels to be regenerated, and its corresponding sub-channels. These are fed into some additional signal processing, that prepares the data for regeneration. This RX pre-process relies mainly on a small synthesis channelizer, feeding a narrow band demodulator whose output (typically based band frames) are re-modulated. The resulting signal is then split into sub-channels again using an analysis channelizer. These replace the original band slices within the sub-channels structure. Finaly the transmitting signal is synthesized and transmitted towards the gateway.

The gateway to terminals path is identical to the orthogonal hybrid mode (see ‎4.3.1)

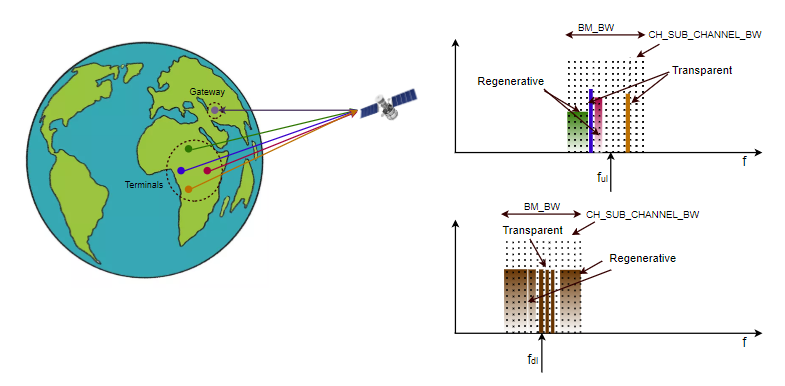


Figure 14:Hybrid (true) mode terminals 🡪 gateway spatial-spectral description.

## Store and forward mode

In this mode the gateway and terminals are located within a long mutual distance, forcing the SDR to store the received data (either from the gateway or the terminals) in its file system and re-transmit it once the target is reachable.

Naturally this process can be done only by complete de-modulation and decoding of the received signal, similar to the regenerative mode.

A diagram of a satellite

Description automatically generated

Figure 15:Store and forward mode terminals🡨🡪 Satellite spatial-spectral description.

A diagram of a planet

Description automatically generated

Figure 16:Store and forward mode gateway 🡨🡪 satellite spatial-spectral description.

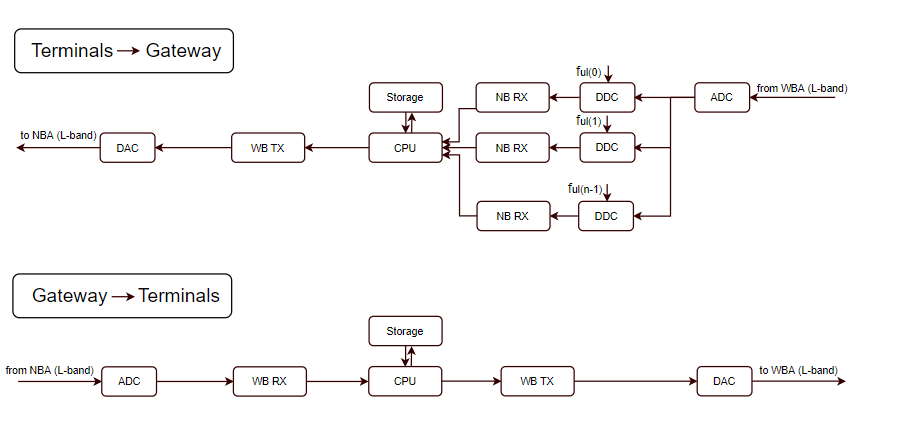


Figure 17:store and forward mode general block diagram.

# Algorithmic architecture

|  |  |  |
| --- | --- | --- |
| Name | Description | Value |
| BW\_BW | Beam band width | 500MHz |
| CH\_SUB\_CHANNEL\_BW | channelizer sub channel BW | 2.65MHz |
|  | RF frequency for up link | 29GHz (TBD) |
|  | RF frequency for down link | 21GHz (TBD) |
| CH\_MAX\_CHANNEL\_BW | Maximum BW allowed for a single channel (terminal) in channelizer mode | 250MHz |
| R\_N \_UL\_CHANNELS |  |  |

Table 5: Channelizer mode parameters and spectral definitions

|  |  |  |
| --- | --- | --- |
| Name | Description | Value |
| BW\_BW | Beam band width | 500MHz |
| RG\_N \_UL\_CHANNELS | Regenerative number of upload channels | 10 |
| RG\_TRM\_GW\_BW | BW of a single uplink channel in regenerative mode | 50MHz |
| RG\_INTER\_CHANNEL\_SB | Inter channel safe band in regenerative mode |  |
|  |  |  |
|  |  |  |

Table 6: Regenerative mode parameters and spectral definitions

A diagram of a diagram

Description automatically generated

A diagram of a process

Description automatically generated

## Channelizer

### Specifications

Table 3 depicts the principle channelizer characteristics:

|  |  |
| --- | --- |
| Parameter | Description |
| Signal bandwidth (CH\_BW) | 250 MHz |
| Beam sub-channel granularity | 2.75 MHz |
| Prototype filter transition bandwidth | ??? |
| Routing | Non-blocking any-to-any over the 2 ka antennas |
| Adjacent sub-channel rejection (digital domain) | ≥ 70 dBc (TBD by Shachar) |
| System Latency | << 1ms (TBD by Shachar) |
| NPR | > 45 dB (TBD by Shachar) |
| Configuration GUI | Core/lab application (TBD by Shachar) |
| Flatness | 1dB over 500MHz (TBD by Shachar) |
| Dynamic range | (TBD by Shachar) |
| FDIR | ??? |
| Sub channel Power control | < 0.1 dBm (TBD by Shachar) |
| Digital sub channels ALC | equalization and gain control functionality on each SCA and the entire BW (TBD by Shachar) |
| Digital FGM | fixed gain mode functionality on each signal (TBD by Shachar) |
| Payload interface | Electrical interface: (TBD by Shachar)  Data protocol:  Connectors type:  Etc. |
| FFT size (NFFT) | 128 |

**Table 4.1** Specification Table - Channelizer Configuration

### Algorithmic approach

Details from Sharar Shtadler

## Regenerative Modem Specifications

### Specifications

**Specification Table - Regenerative Proof of Concept**

|  |  |
| --- | --- |
| Parameter | Value |
| Supported waveform | DVB-S2X |
| Modcod | QPSK to 32 APSK |
| Demodulator latency | 2 frames |
| Supported downlink CSL rate | 1.9Gbps |
| Maximum Symbol rate CSL downlink | 460Msps |
| Maximum symbol rate CSL uplink | 460Msps |
| Channelization grid | 1/(2^n) (TBD by Ayecka) |
| Maximum n | 5 (TBD by Ayecka) |
| Maximal number of channels for CSL uplink/downlink | 16 (TBD by Ayecka) |
| Maximal uncompensated frequency uncertainty | +- 800KHz (TBD by Ayecka) |
| Maximal frequency acceleration | +-14Khz/sec (TBD by Ayecka) |
| Memory consumption per CSL uplink with 16 channels | 45% (TBD by Ayecka) |
| Signal acquisition time | 2 frames typically (TBD by Ayecka) |
| Minimal symbol rate CSL uplink | 460/32 Msps (TBD by Ayecka) |
| User packet size | 1500Bytes (TBD by Ayecka) |
| Encapsulation | GSE (TBD by Ayecka) |
| Flow control | Using AXI bus (TBD by Ayecka) |

### Algorithmic approach

Details from Avi

## Channelizer to Modem Processing Stage (CMPS)

# HW architecture

A diagram of a computer

Description automatically generated

## RF and RFFE

## IPB

## HW interfaces

## Power management and distribution

A diagram of a network connection

Description automatically generated

A diagram of a computer hardware system

Description automatically generated

A diagram of a bus

Description automatically generated

# The Versal 1502 component

Versal devices are built from a library of building blocks dedicated to processing, compute, acceleration, and connectivity. Figure 13 shows the layout of a device with the NoC connecting to an external host processor via the CPM and the various heterogeneous processing elements: PL, and scalar processing accelerators.

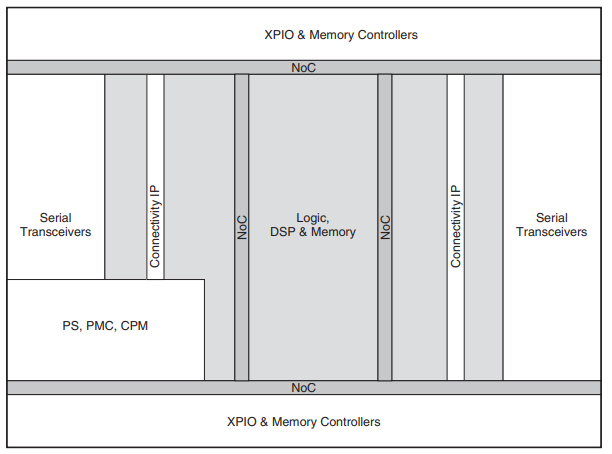


Figure : Versal Device Layout

Serial transceivers are located on the east and west edges of the device with XPIO and memory controllers on the south and north of the device. Connectivity IP is located in columns close to the serial transceivers. Resources are connected together through a matrix of programmable interconnect routes for local and regional signal connectivity as well as the NoC for high bandwidth and long distance communication around the device.

## NoC (Network on chip)

The programmable NoC is an AXI-4 based network of interconnect within the Versal architecture that easily enables high-bandwidth connections to be routed around the device. The NoC extends in both horizontal and vertical directions to the edges of the device. It exists to connect together areas of the device that demand and use large quantities of data alleviating any resource burden on the local and regional device interconnect. The NoC is a full blocking crossbar between memory controllers, programmable logic, processing system, AI Engines, and platform management controller.

Examples of NoC connections include:

* Sharing device access to DRAM (DDR memory)
* PL to PL connections
* Memory mapped access to the AI Engine array.
* Connecting between processing system (PS) and PL
* Connecting between the processing system and DDR memory In devices built using stacked silicon interconnect (SSI) technology, the vertical NoC columns connect between adjacent super logic regions (SLRs), which allows device configuration data to travel between primary and secondary SLRs.

## Platform Management Controller

The platform management controller is responsible for managing Versal devices with the following main categories of responsibility:

* securely booting and configuring the platform
* life-cycle management, which includes device integrity and debug, and system monitoring.

### Boot and Configuration

The platform management controller is responsible for booting Versal devices from the primary boot source in a multi-stage boot process that supports both a non-secure and a secure boot. For a secure boot, the AES-GCM, SHA3-384 decryption/authentication, and ECDSA/RSA blocks decrypt and authenticate the image. Upon reset, the mode pins are read to determine the primary boot device, such as quad SPI, octal SPI, SD, or eMMC. The platform management controller then proceeds to execute the code out of on-chip BootROM and copies the platform loader and manager (PLM) from the boot device to the on-chip memory while undergoing authentication and decryption. The configuration of the PL is also undertaken by the PLM. The device image is loaded from its storage medium, and after authentication and decryption, is sent to the PL configuration interface. It is also possible to reconfigure portions of the PL using Dynamic Function eXchange (DFX). A new device image for a portion of the PL can be loaded from the processing system, through the primary or secondary boot interfaces, e.g., PCIe or Ethernet. Upon reconfiguration, a portion of the PL provides the new functionality determined by the new device image, enabling users to quickly adapt the functionality of their design to changing system requirements.

### System Monitoring

The platform management controller contains system monitoring capability for monitoring voltage and temperature in the processing system and PL to enhance the overall safety, security, and reliability of the system. The core of the system monitor is a 10-bit 200kSPS ADC, which can be accessed via JTAG, PMBus, or I2C interfaces, via the processing system directly, and via the PL through the NoC.

### Device Integrity and Debug

JTAG is the primary interface for Versal device debug features. The JTAG architecture has two IEEE Std 1149.1 compliant TAP controllers that are connected in series:

* Arm DAP controller
* Platform management controller TAP controller

The Arm DAP controller is the main controller for debug functions supporting:

* Processing system
* CoreSight debug architecture
* Debug of the PL
* Programming of supported external flash memory
* eFUSE/BBRAM programming.

The TAP controller supports:

* Reading the device IDCODE
* Programming of the PL
* Boundary scan.

The platform management controller also contains a high-speed debug port (HSDP) that can be used as a faster debug method than the primary JTAG interface. The HSDP interface is a high-throughput interface consisting of separate ingress and egress simplex Aurora 64B/66B channels that leverage the transceivers to the north of the processing system. The HSDP allows daisy-chaining of channels from different devices. The HSDP can also be accessed by the serial transceivers in the PL via an Aurora bridge also in the PL.

### External Flash Memory Interfaces

The SD/eMMC controller supports 1- and 4-bit data interfaces at low, default, high-speed, and ultra-high-speed (UHS) clock rates. This controller also supports 1-, 4-, or 8-bit-wide eMMC interfaces that are compliant to the eMMC 4.51 specification. eMMC is one of the primary boot modes and supports boot from managed NAND devices. The controller has a built-in DMA for enhanced performance. The quad SPI controller is one of the primary boot devices. It supports 4-byte and 3-byte addressing modes. In both addressing modes, single, dual-stacked, and dual-parallel configurations are supported. Single mode supports a quad serial NOR flash memory, while in double stacked and double parallel modes, it supports two quad serial NOR flash memories. The octal SPI controller is one of the primary boot and configuration devices. It has an 8-pin interface and provides up to 400MB/s of bandwidth in double data rate mode and up to 166MB/s in single data rate mode. It has two chip-selects to support deeper memory and a built-in DMA for enhanced performance.

## The Processing System (PS)

A computer programmable logic

Description automatically generated

Figure : Versal processing system and surrounding blocks

Figure 14 shows a general overview of the versal 1502 processing system.

Main components will be described shortly:

### Application Processing Unit (APU)

The APU has a feature-rich dual-core Arm Cortex-A72 processor. Cortex-A72 cores are 64-bit-wide application processors based on the Arm-v8A architecture, which supports hardware virtualization. Each of the Cortex-A72 cores has:

* 48KB of instruction L1 cache and 32KB of data L1 cache, with parity and ECC protection respectively
* a NEON SIMD (Single Instruction Multiple Data) engine
* a single and double precision floating point unit.
* a snoop control unit that keeps the L1 caches coherent thus eliminating the need of spending software bandwidth for coherency.
* 1MB L2 cache with ECC protection to enhance system-level performance.
* a built-in interrupt controller supporting virtual interrupts

### Real-Time Processing Unit (RPU)

The RPU in the processing system contains a dual-core Arm Cortex-R5F processor. Cortex-R5F cores are 32-bit real-time processor cores based on the Arm-v7R architecture. Each of the Cortex-R5F cores has:

* 32KB of Level 1 (L1) instruction and data cache with ECC protection
* a 128KB tightly coupled memory (TCM) interface for real-time single cycle access.
* a dedicated interrupt controller
* a floating point unit.

### Connectivity Peripherals

In the processing system, many peripherals are used to connect to external devices over industry-standard protocols, including:

* 2 gigabit Ethernet controllers
* 2 SPI controllers
* 2 I2C controllers
* 2 CAN/CAN-FD controllers
* 2 UARTs
* GPIO
* 1 USB 2.0 (device and host) controller

### USB 2.0

The USB controller can be configured as host or device. The controller is compliant to the USB 2.0 specification and supports high, full, and low-speed modes in all configurations. In host mode, the USB controller is compliant with the Intel XHCI specification. In device mode, it supports up to the 12 endpoints. The Universal Low Peripheral Interface (ULPI) is used to connect the controller to an external PHY operating up to 480Mb/s.

### Ethernet MAC

The PS contains a pair of tri-speed Ethernet MACs support 10Mb/s, 100Mb/s, and 1Gb/s operations. They also support jumbo frames and timestamping through the interfaces based on IEEE Std 1588 v2. The Ethernet MACs can be connected through the MIO (RGMII), or through EMIO (GMII). The GMII interface can be converted to a different interface within the PL.

## Configurable Logic Block (CLB)

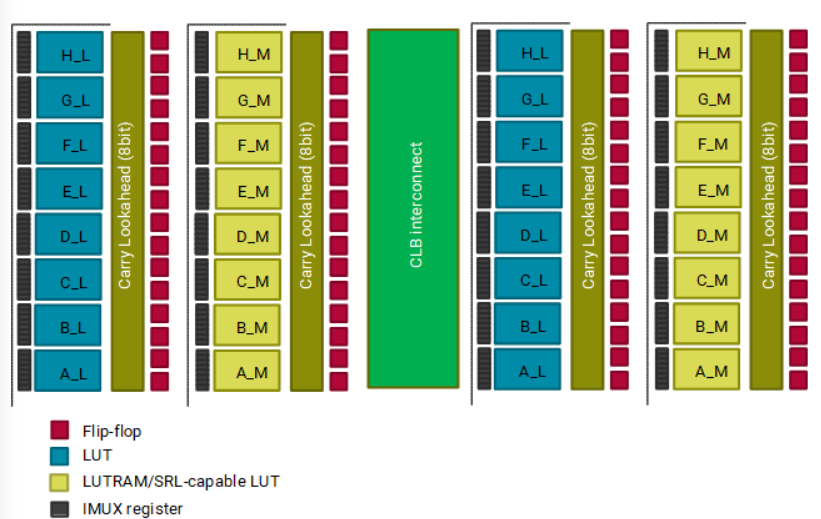


Figure : Versal CLB architecture

Every configurable logic block (CLB) contains:

* 32 look-up tables (LUTs)
* 64 flip-flops
* Arithmetic carry logic and multiplexers to create wider logic functions

The LUTs can be configured as either:

* 1 x 6-input LUT with one output
* 2 x 5-input LUTs with separate outputs but common inputs
* 2 x 64-bit RAM
* 1 x 32-bit shift register (SRL32)
* 2 x 16-bit shift registers (SRL16s)

Within every CLB are dedicated interconnect paths for connecting LUTs together without having to exit and re-enter a CLB and cascade muxes. This enables a flexible carry logic structure that allows a carry chain to start at any bit in the chain.

## Internal Memory

Each Versal device contains several programmable, internal storage capabilities. In addition to the distributed RAM capability in the CLB, there are dedicated blocks for building various size storage elements.

### On-Chip Memory (OCM)

In addition to the 32KB of L1 data cache, the RPU contains 256KB OCM with ECC. The OCM is accessed through two 128-bit AXI interfaces with one AXI interface dedicated to the two Cortex-R5F processors and the other AXI interface available to the APU and other masters. Memory accesses from the RPU are treated with higher priority than memory accesses through the general 128-bit AXI interface.

### Block RAM

True dual-port block RAMs, each having 36Kb of storage capacity, can be configured as either one 36Kb RAM, or two completely independent 18Kb RAMs. Each port can be configured as 4K × 9, 2K × 18, 1K × 36, or 512 x 72 in simple dual-port mode. The two ports can have different aspect ratios. Also, the read port width can be different from the write port width for each port.

### UltraRAM

Dual-port UltraRAMs, each having 288K bits of storage capacity, can be configured as one 288Kb RAM. Each port can be configured as 32K x 9, 16K x 18, 8K x 36, or 4K x 72. The two ports can have different aspect ratios.

### Multiport RAM

Multiport RAM (MPRAM) is an array of eight 5Mb RAMs, totaling 40Mb. Each RAM has one write and one read port of 128-bit data. In addition, up to two write and two read 128-bit ports provide access to all eight RAMs. Each 5Mb RAM can be accessed individually (unit access) in simple dual-port mode supporting simultaneous write and read at 128-bit. Total storage is 40960 words of 128-bit data. Two global read and two global write ports allow 128-bit access to all eight RAMs (global access), totaling 8x40960 words of 128-bit data (40Mb total). Global access can be combined with unit access, for example, global write with unit reads on multiple RAMs.

## Digital Signal Processing (DSP)

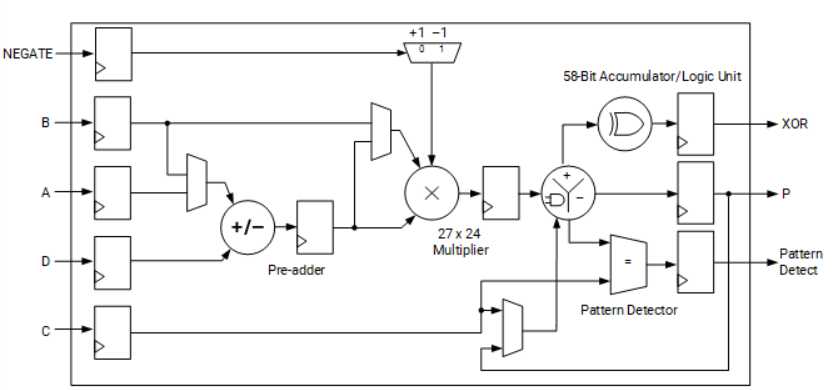


Figure : Versal DSP slice architecture

Each DSP Engine fundamentally consists of:

* a dedicated 27 × 24 bit twos complement multiplier
* 58-bit accumulator
* Additional pre-adder, typically used in symmetrical filters to save up to 50% of the DSP engines count.
* 116-bit-wide XOR function, programmable to 12, 22, 24, 34, 58, or 116-bit widths, is handy for implementing forward error correction and cyclic redundancy checking algorithms.
* 58-bit-wide pattern detector that can be used for convergent or symmetric rounding.

The DSP Engine layout enables new modes of operation in addition to the conventional fixed-point operation:

#### Three element vector / INT8 dot product

The DSP Engine can be used in vector fixed-point ALU mode in which the 27 x 24 bit multiplier is replaced by a three-dimensional vector dot-product unit. The dot-product unit supports element-wise product negation with negate pins.

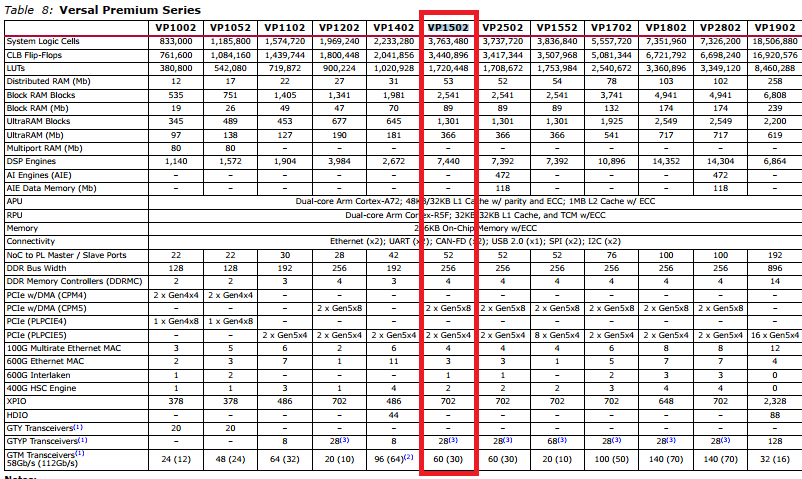
#### Complex 18b x 18b

Using two back to back DSP Engines, the Versal architecture enables creation of an 18 x 18 + 58 twos complement complex multiply accumulator in which each of the two complex inputs can be optionally conjugated.

#### Single precision floating point

The DSP Engine contains a floating-point multiplier and a floating-point adder with separate outputs in binary32 format. Each floating-point multiplier input can be in either binary32 (single-precision or FP32) or binary16 (half-precision or FP16) format.

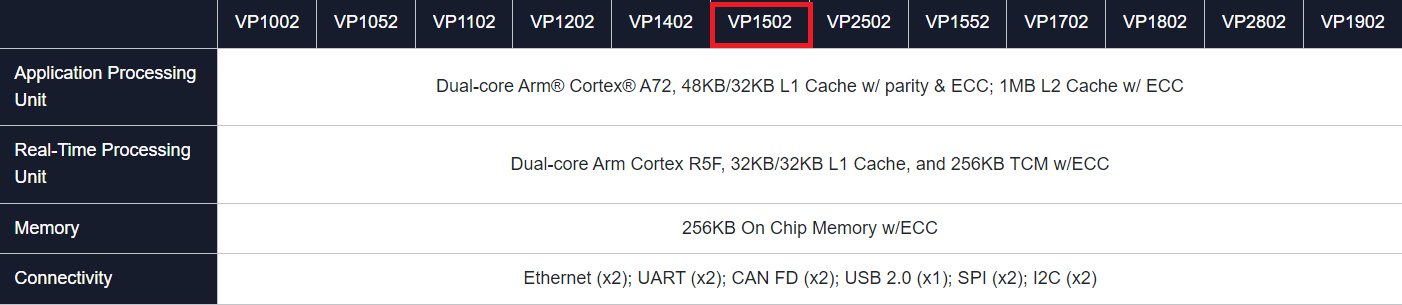
## Exact component definition and resource count



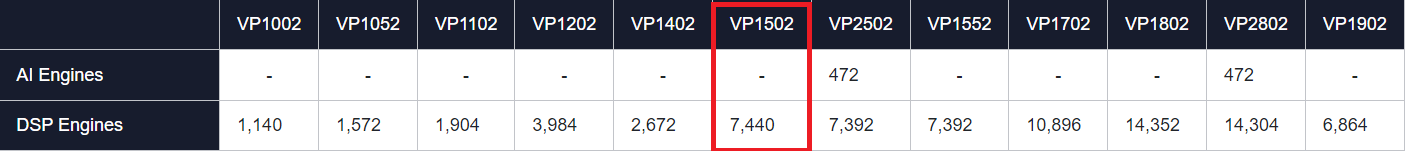
The exact component mounted on the OPR board is XCVP1502VSVA2785PKG

Following is a summary of the component resources:

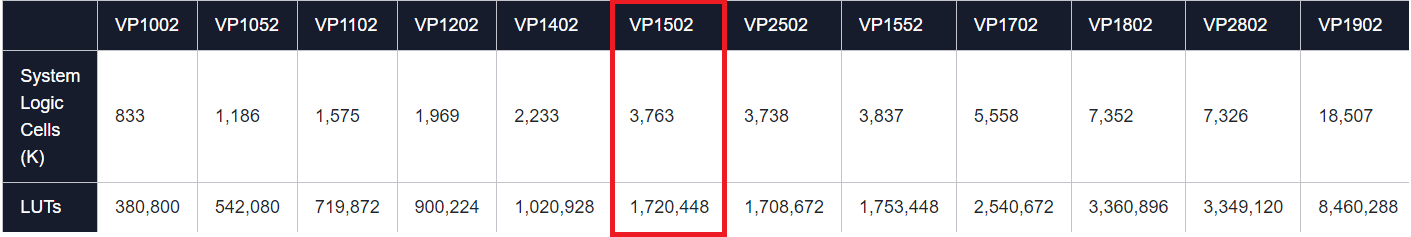
* Scalar Engines Features:



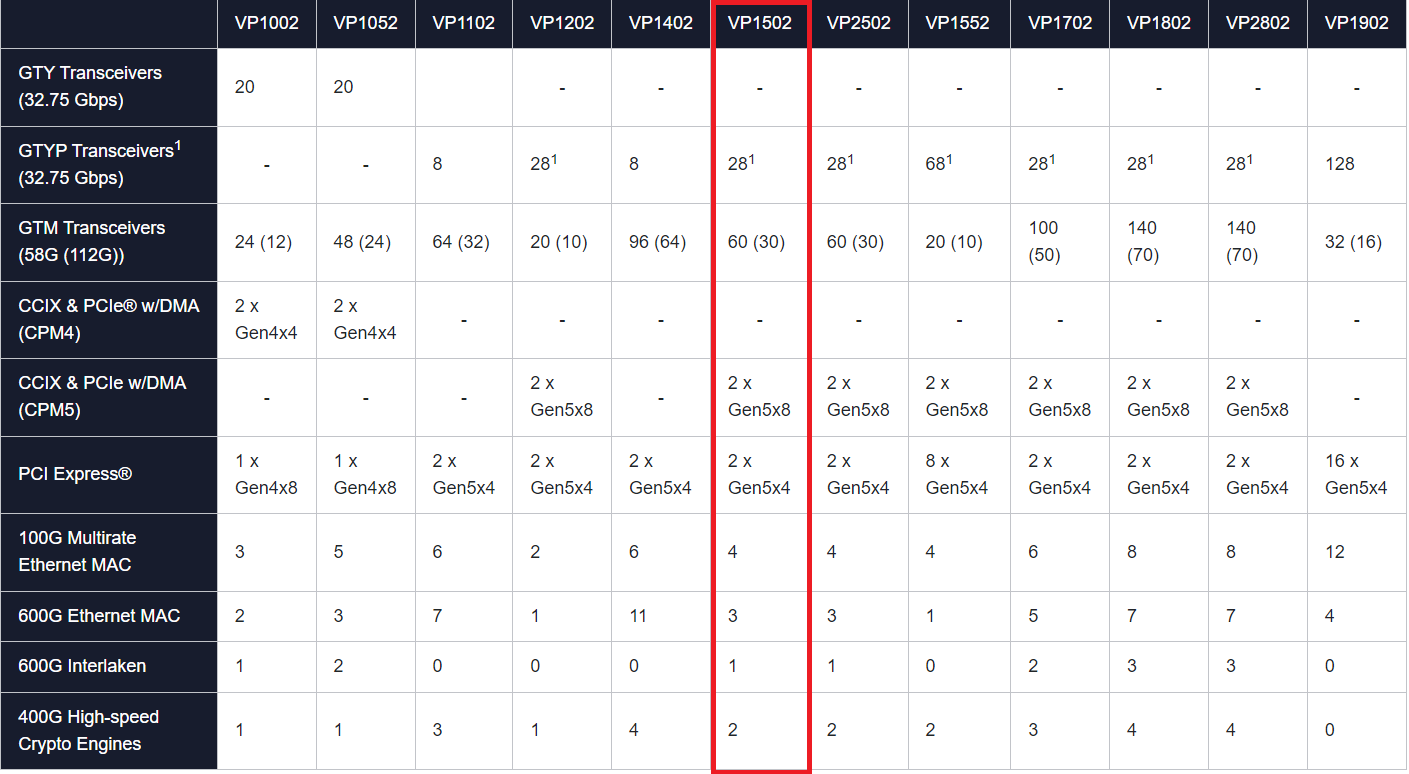
* Intelligent Engines Features:



* Adaptable Engines Features:



* Foundational Platform Features:



# FW architecture

## Modes of operation in details

### Channelizer only

#### Functionality

#### Data path

#### Control and configuration

## Chip organization

### Control

### Clocks

### Power management

### Register file

### Peripherals

# SW architecture

A diagram of software architecture

Description automatically generated

# Mechanical and Thermal concepts

## Anntenas

## Gimbals

# FDIR and Redundancy and RDP

# Operation Concepts

# Verification and Validation