悠景科技股份有限公司

UG-5696GSWAG01

Evaluation Kit User Guide

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Version: Preliminary

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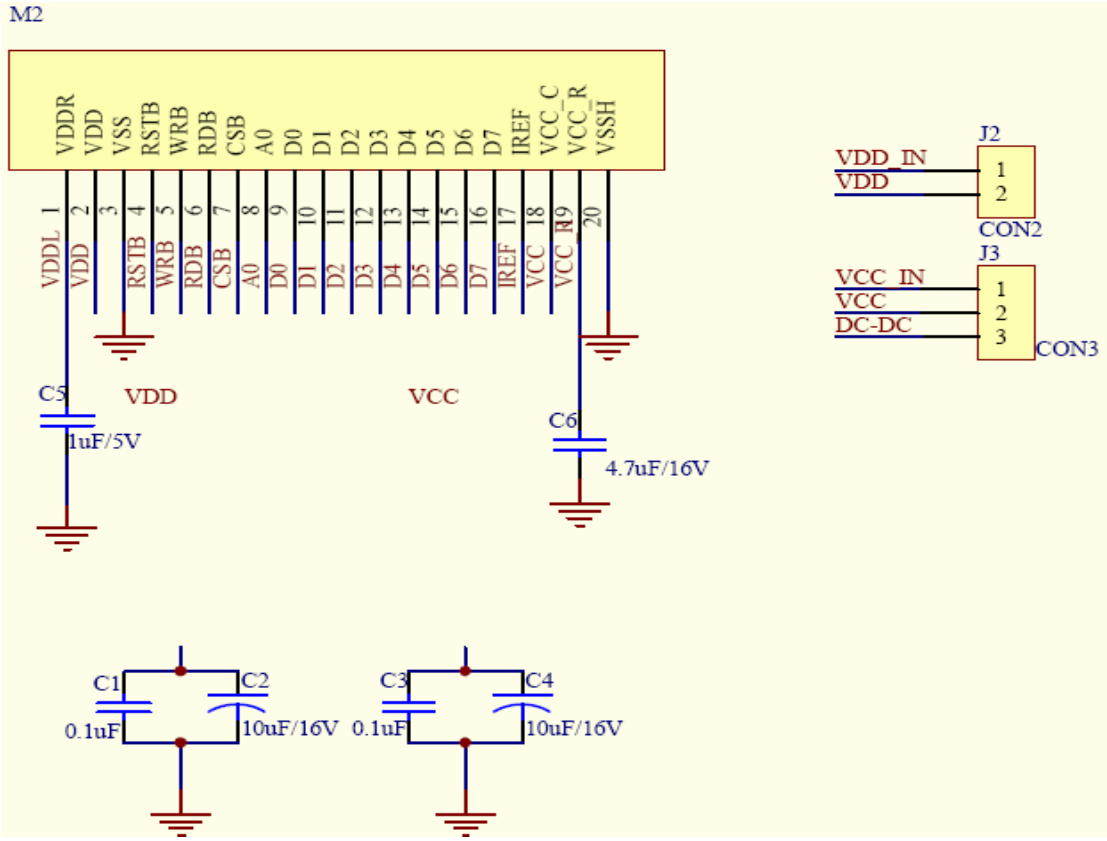
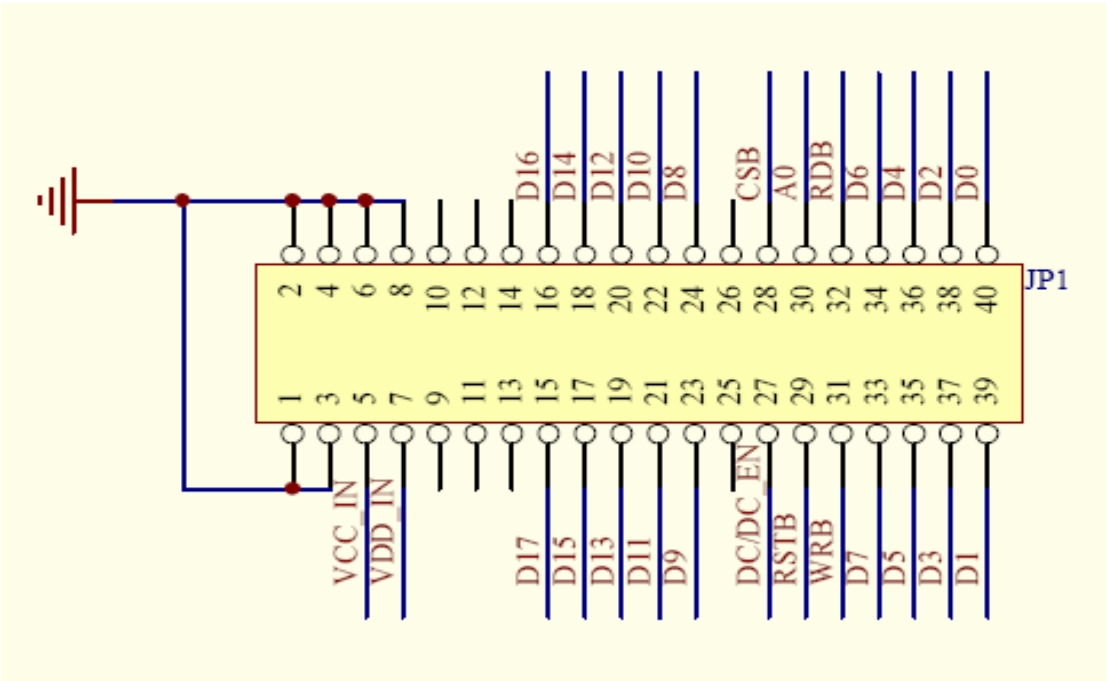
1. REVISION HISTORY

Date	Page	Contents	Version
2008/04/09	*	Preliminary	Preliminary 0.0

2. EVK Schematic





3. Symbol define

D17-D0：These pins are 18-bit bi-directional data bus to be connected to the MCU's data bus.
The D0~D7 are for command and data inputs (8bit parallel interface).

CSB：This pin is the chip select input. The chip is enabled for MCU communication only when CS is pulled low.

RDB：When connecting to an 8080-microprocessor, this pin receives the Read (RD) signal. Data read operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin RD must be connected to VSS.

WRB：When 8080 interface mode is selected, this pin will be the Write (WR) input. Data write operation is initiated when this pin is pulled low and the chip is selected. When serial interface is selected, this pin R/W must be connected to VSS.

A0: This pin is Data/Command control pin. When the pin is pulled high, the data at D0-D7 is treated as display data. When the pin is pulled low, the data at D0-D7 will be transferred to the command register. For detail relationship to MCU interface signals, please refer to the timing characteristics diagrams at following pages and datasheet.

RESB：Reset SEPS114A(active low).

VCC：External Column Driving Power Supply.

VDD：Logic power supply.

GND：Power supply ground.

4. TIMMING CHARACTERISTICS

一. 80-Series MPU parallel Interface

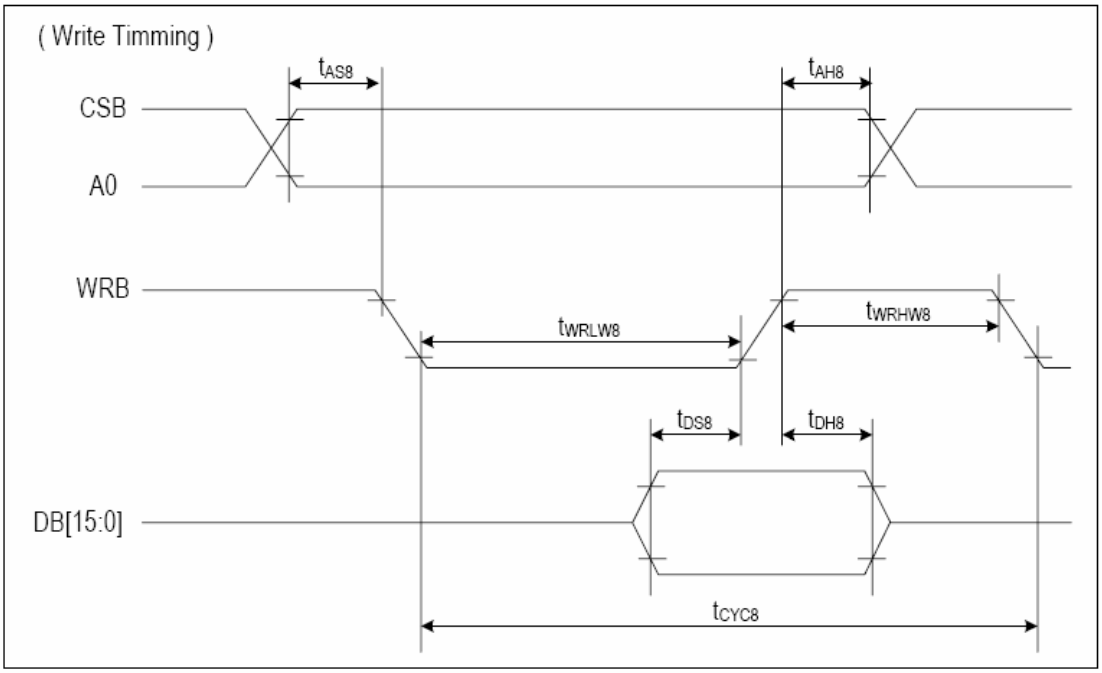


Figure 1 80-Series MPU 8-bit parallel Interface Timing Diagram

(VDD = 2.8V, Ta = 25℃)

ITEM	SYMBOL	CONDITION	MIN	MAX	UNIT	PORT
Address hold timing	t_{AH8}	-	5	-	ns	CSB
Address setup timing	t_{AS8}		5		ns	A0
System cycle timing	t_{CYC8}	-	100	-	ns	WRB
Write "L" pulse width	t_{WRLW8}		45		ns	
Write "H" pulse width	t_{WRHW8}		45		ns	
Data setup timing	t_{DS8}	-	30	-	ns	DB[15:0]
Data hold timing	t_{DH8}		10		ns	

notice) All the timing reference is 10% and 90% of VDDIO.

Table 1 80-Series MPU 8-bit parallel Interface Timing Characteristics

5. EVK use introduction

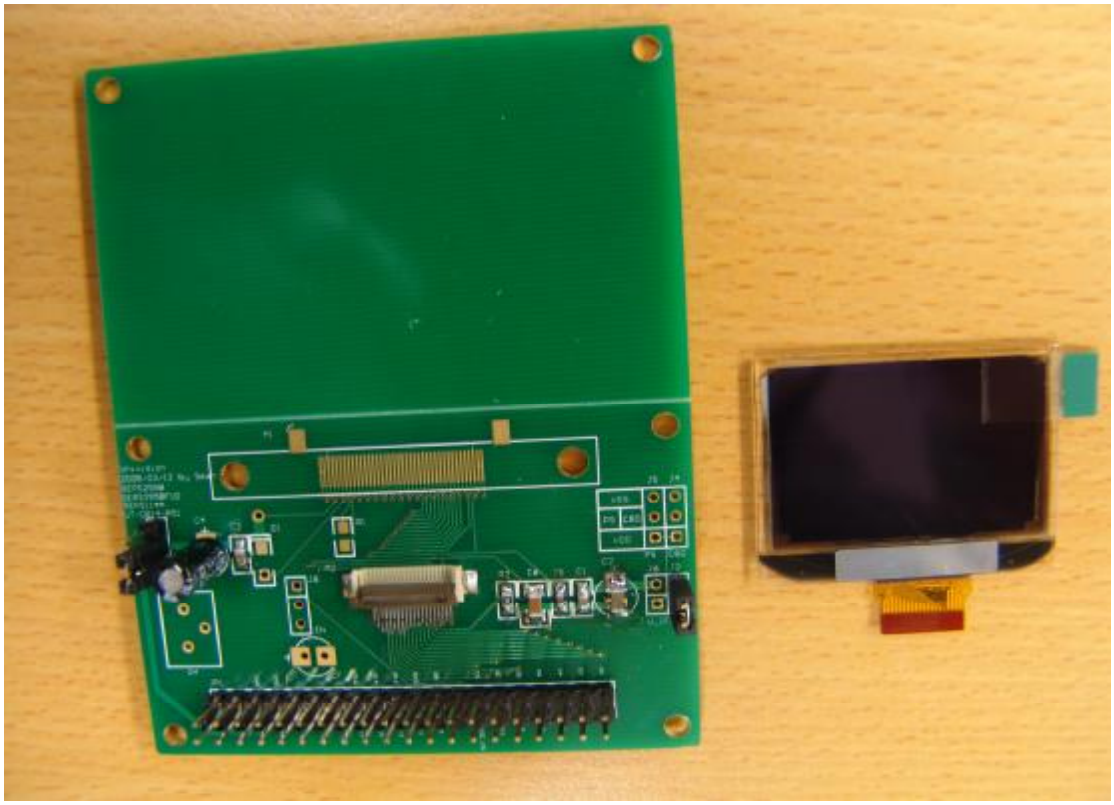


Figure 4 EVK PCB and OLED Module

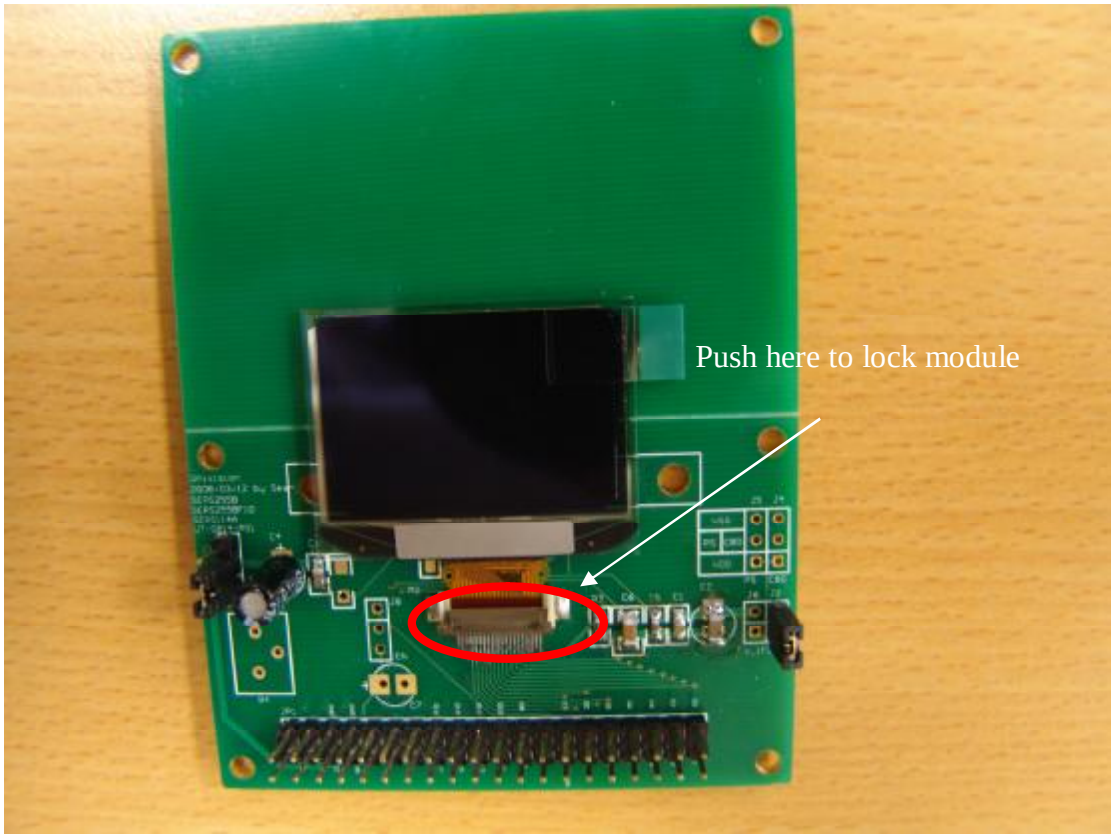


Figure5 The combination of the module and EVK

The SEPS114A is COG type package, that the connect pads are on the top of the module connector. When finished assembled the module and EVK, then push the locking pad to lock the module. See the Figure 4 and Figure6.

User can use leading wire to connect EVK with customer's system. The example shows as Figure 6

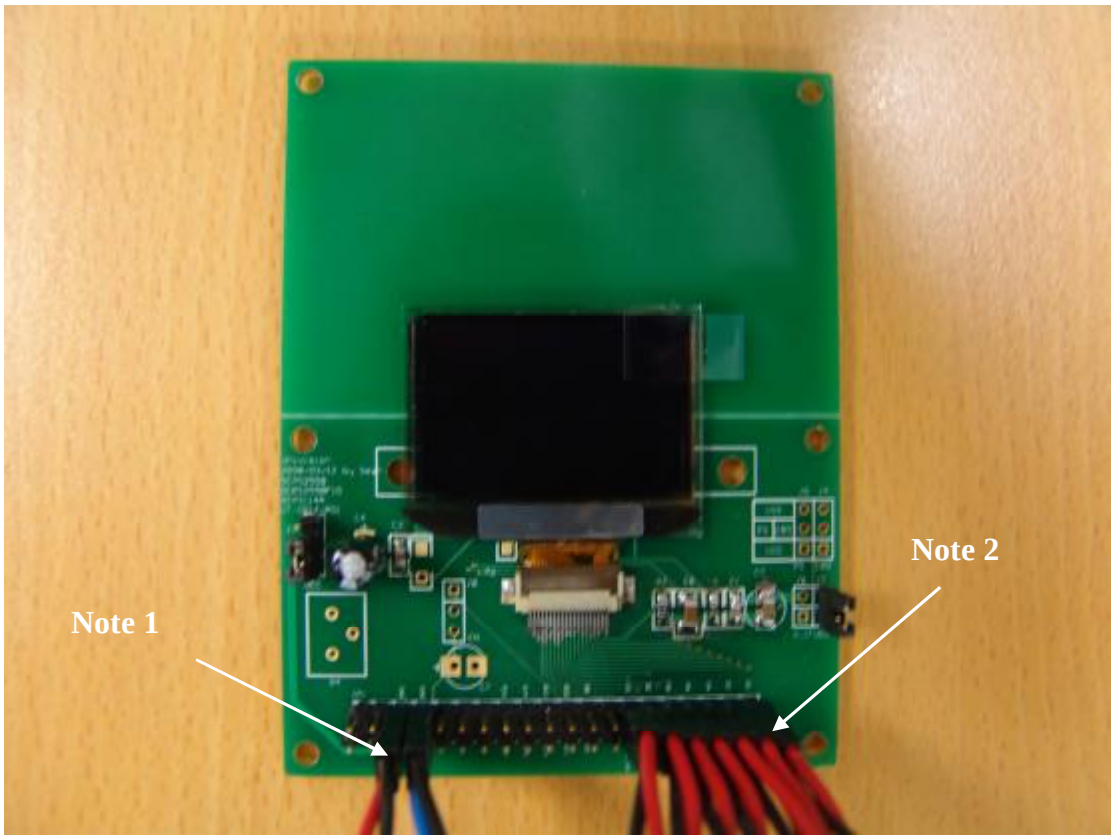


Fig 6 EVK with test platform

Note 1：It is the external most positive voltage supply. In this sample is connected to power supply.

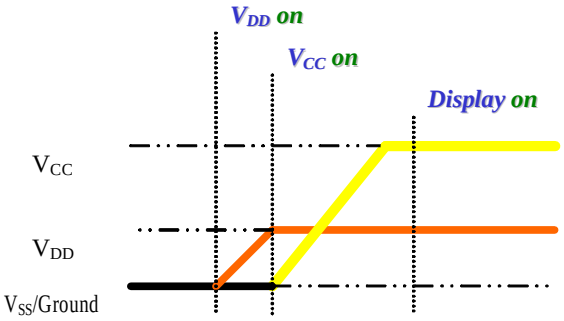
Note 2：The leading wire has 13 pins totally in this case.
(D7-D0, RDB,RS,WRB,RESB,CSB)

6. Power down and Power up Sequence

To protect OLED panel and extend the panel life time, the driver IC power up/down routine should include a delay period between high voltage and low voltage power sources during turn on/off. Such that panel has enough time to charge up or discharge before/after operation.

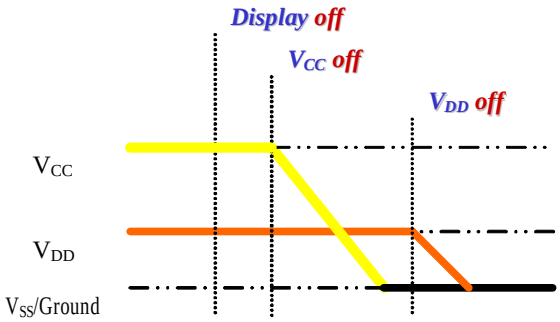
Power up Sequence:

1. Power up V_{DD}
2. Send Display off command
3. Driver IC Initial Setting
4. Clear Screen
5. Power up V_{DDH}
6. Delay 100ms
   (when V_{DD} is stable)
7. Send Display on command



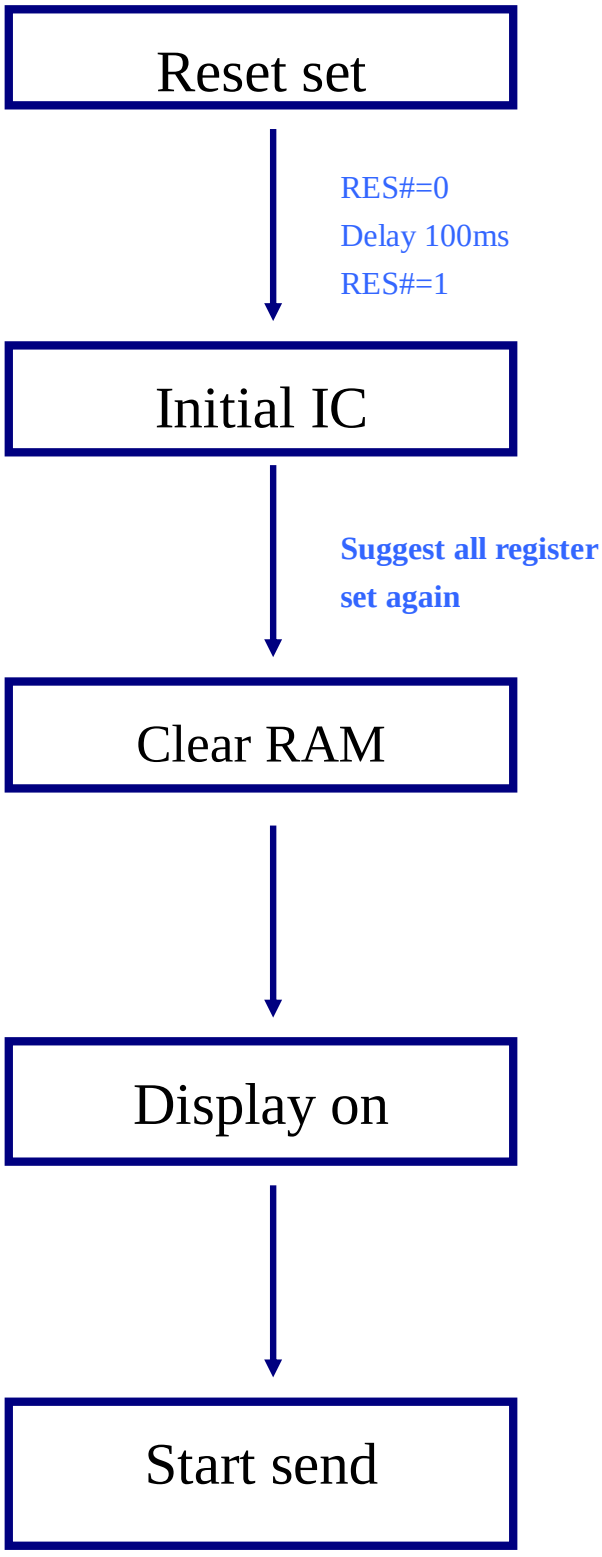
Power down Sequence:

1. Send Display off command
2. Power down V_{DDH}
3. Delay 100ms
   (when V_{DDH} is reach 0 and panel is completely discharges)
4. Power down V_{DD}



7. How to use SEPS114A module

7.1 Initial Step Flow



7.2 RD recommend Initial Code for 80 Interface

```
write_c(0x0F);          //ANALOG CONTROL
write_d(0x40);

write_c(0x14);          //STANDBY ON/OFF
write_d(0x00);

write_c(0x1A);          //OSC ADJUST
write_d(0x03);

write_c(0x09);          //ROW SCAN DIRECTION
write_d(0x00);

write_c(0x30);          //DISPLAY
write_d(0x1F);

write_c(0x31);
write_d(0x52);

write_c(0x32);
write_d(0x00);

write_c(0x33);
write_d(0x5F);

write_c(0x38);          //DISPLAYSTART
write_d(0x1F);

write_c(0x39);
write_d(0x00);

write_c(0x0D);          //CPU IF
write_d(0x02);

write_c(0x34);          //MEM
write_d(0x1F);

write_c(0x35);
write_d(0x52);

write_c(0x36);
write_d(0x00);

write_c(0x37);
write_d(0x5F);

write_c(0x1D);          //MEMORY WRITE/READ
write_d(0x00);

write_c(0x18);          //DISCHARGE TIME
write_d(0x08);

write_c(0x16);          //PEAK PULSE DELAY
write_d(0x05);

write_c(0x3A);          //PEAK PULSE WIDTH R
write_d(0x1F);

write_c(0x3B);          //PEAK PULSE WIDTH G
```

```
        write_d(0x1F);

        write_c(0x3C);          //PEAK PULSE WIDTH B
        write_d(0x1F);

        write_c(0x3D);          //PRECHARGE CURRENT R
        write_d(0x80);

        write_c(0x3E);          //PRECHARGE CURRENT G
        write_d(0x80);

        write_c(0x3F);          //PRECHARGE CURRENT B
        write_d(0x80);

        write_c(0x40);          //COLUMN CURRENT R
        write_d(0xFF);

        write_c(0x41);          //COLUMN CURRENT G
        write_d(0xFF);

        write_c(0x42);          //COLUMN CURRENT B
        write_d(0xFF);

        write_c(0x48);          //ROW OVERLAP
        write_d(0x03);

        write_c(0x49);          //SCAN OFF LEVEL
        write_d(0x03);

        write_c(0xE0);          //RGB IF
        write_d(0x20);

        write_c(0xE5);          //DISPLAY MODE CONTROL
        write_d(0x00);

        write_c(0x02);          //DISPLAY ON
        write_d(0x01);
```

7.2.1 Sub Function for 80 Interface

```
void write_c(unsigned char out_command)
{
        RS=0;
        CS=0;
        WR=0;

        P1=out_command;

        WR=1;
        CS=1;
        RS=1;
}

void write_d(unsigned char out_data)
{

        RS=1;
        CS=0;
        WR=0;
```

```
        P1=out_data;

        WR=1;
        CS=1;
        RS=0;
}


void White_pattern()
{
write_c(0x08);

        for(i=0;i<96;i++)
        {
                for(j=0;j<52;j++)
                {
                write_d(0xFF);
                write_d(0xFF);
                write_d(0xFF);
                }
        }
}}
```

Note：1.For 80 series CPU interface.

2.For 6 Bbit Ttiple Transfer 65K support.