Evan Y. Su

8875 Via Andar● San Diego, CA 92122 ● (310) 889-8841 ● evanysu@gmail.com ● US Citizen

Education

University of California, San Diego **September 2012 – Expected June 2014**
M.S. Electrical & Computer Engineering: *Electronic Circuits & Systems* GPA: 3.5

University of California, Los Angeles **September 2007 - June 2012**
B.S. Electrical Engineering: *Antennas and Microwaves*

Relevant Coursework

Electrical Engineering/ Computer Science

• VLSI Integrated Circuits • Advanced Digital Design • ASIC Implementation Flow • System-on-Chip Design • CMOS Analog Integrated Circuits • Microwave and RF • Computer Architecture • Data Structures

Work Experience

Space Exploration Technologies Corp.
RF Intern | Avionics department **January 2012 – June 2012**

- Oversaw environmental testing of various avionics components such as transmitters, LNAs, couplers, and filters
- Wrote programs in LabVIEW and python to automate testing procedures, which greatly increased production speed
- Performed various RF measurements such as spurious, VSWR, gain measurement, and impedance characterization using network analyzers, spectrum analyzers, and various other RF instruments

The Ozcan Research Group at UCLA
Undergraduate Research Assistant **April 2011 – June 2012**

- Designed a portable version of a multi-angle lensless holographic imaging platform
- Designed apparatus which tracks the behavior of sperm cells under different heat gradients
- Responsible for obtaining and modifying equipment necessary for performing various experiments

Eon Silicon Solution, Inc. Jubei, Taiwan
Intern **June 2010 – September 2010**

- Ran bench measurements with LCR meter and produced C-V curves on NOR type flash chips to characterize the technology
- Developed a set of design rules to ensure correctness of mask sets
- Responsible for the replacement and reparations of old equipment

Relevant Skills

Design Projects

Leakage Power Reduction

- Reduced post-route leakage power consumption by 50% through static timing analysis in Synopsys PrimeTime
- Developed sensitivity-based algorithm in Tcl script to identify and swap cells on non-critical paths
- Implemented timing recovery by up-swapping bottleneck cells

Synthesis for multi-mode operation (DVFS)

- Synthesized design which operates in a multi-mode condition using dynamic voltage and frequency scaling in Synopsis Design Compiler
- Optimized synthesis by finding the best compile option, voltage library and clock period combination

1 GHz Clock Distribution Network

- Designed and sized a chain of inverters to optimize power consumption when delivering a 1 GHz clock to four different loads at four different locations with a skew of less than 50ps and transition time below 100ps
- Used Cadence to design schematic and layout, run DRC and LVS checks, and obtain extracted simulation results

2.4 GHz E-pHEMT Low Noise Amplifier

- Used ADS to design a biasing network to turn on and to help stabilize ATF55143 transistor, while also providing input and output impedance matching
- Used Linecalc to find equivalent distributed components, while accounting for parasitics in order to optimize the circuit
- Completed PCB design, fabrication and assembly process

4 GHz Low Pass Filter

- Designed a lumped element prototype using Chebyshev polynomials according to design parameters
- Approximated Telegrapher's equations for transmission lines and used linecalc in ADS to create an equivalent distributed element model composed of sections of coupled lines
- Ran momentum simulation and completed fabrication, assembly, and testing process

Programs/ Computer Languages

- Synopsys Design Compiler, Synopsys PrimeTime, Apache PowerArtist, Apache RedHawk, Verilog HDL, Cadence Encounter, Cadence, SPICE, ADS, HFSS, C++, Python, Autodesk Inventor, MATLAB, LabVIEW