Chaoqun Zhu

3843 Miramar St. Apt.B•La Jolla, CA 92037•(858)900-7270•c9zhu@eng.ucsd.edu

OBJECTIVE

- To obtain a 2014 **Full Time** job as a **Software** Engineer.
- **C/C++, Java**, Python, SQLite, HTML/CSS, SVN, Assembly, Visual Studio, Eclipse, Linux, Windows, MCU

EDUCATION

University of California, San Diego — Expected Graduation Mar.2014

- **M.S.** in Computer Engineering. GPA: **3.71/4.00**

Zhejiang University, China — Sept.2008 - Jun.2012

- **B.S.** in Information & Communication Engineering. GPA: **3.87/4.00**

RELATED COURSES

Computer Networks, Advanced Data Structure, Algorithm Design and Analysis, Intro to OOP: Java
Database System, Computer Architecture, Principles of Operating Systems, Embedded Systems

WORKING EXPERIENCE

Software Intern in Tensorcom.Inc, Carlsbad, San Diego — Jun.2013 - Feb.2014

- Developed an assembler for RF ISA and a Microchip-based USB-to-SPI debugger in Java
- Built a DLL program with PC-to-ARM USB HID interface for JTAG On-Chip-Debug on target chip

COURSE PROJECTS

Computer Network, Unix TFTP network application — Apr. - Jun.2013

- Implemented a **client/server** TFTP(Trivial File Transfer Protocol) application via multi-thread and **sockets** programming that can handle timeout, packet loss and multiple simultaneous clients

Data Structure in **C++** — Apr. - Jun.2013

- Implemented file compression/decompression tools using Huffman Encoding and IO bitwise operations
- Built the back-end of a Boggle Player Game. Implemented essential functions with Trie Data Structure and Board-based backtracking algorithm for word-checking

Intro to Embedded Computing, **Power Optimization** for Qualcomm MSM8660 Phone — Feb. – Mar.2013

- Implemented Earliest Deadline First and Rate Monotonic scheduling policies with sample inputs in **Perl**
- Proposed a **DVFS** algorithm optimized for Energy Delay Product based on CPU workload decomposition
- Implemented the proposed algorithm in C as a Phone built-in governor and got 18% EDP saving(ranking 2nd)

Intro to Computer Architecture, Design of a New **Instruction Set Architecture** — Oct.2012

- Designed a 14-bit general purpose ISA with 34-bit data and address width, 16 registers and 17 instructions.
- Optimized it for specific benchmarks to achieve reduced Energy Delay Product
- Developed an **assembler** and a **simulator** for the ISA on given java framework and verified their functionality by creating assembly test programs and a simple Virtual Machine

Principles of Operating Systems — Oct. - Dec.2012

- Programmed FIFO, LIFO, ROUNDROBIN and PROPORTIONAL scheduling policies for the Umix kernel
- Utilized semaphores and shared memory to achieve **synchronization** in a single-lane car-driving program
- Implemented threads-related functions to build a user-level **thread** package