

Diseño de sistemas digitales.

Practica 5: Decodificador 0 - 9

Practica 6: Decodificador 0 - F

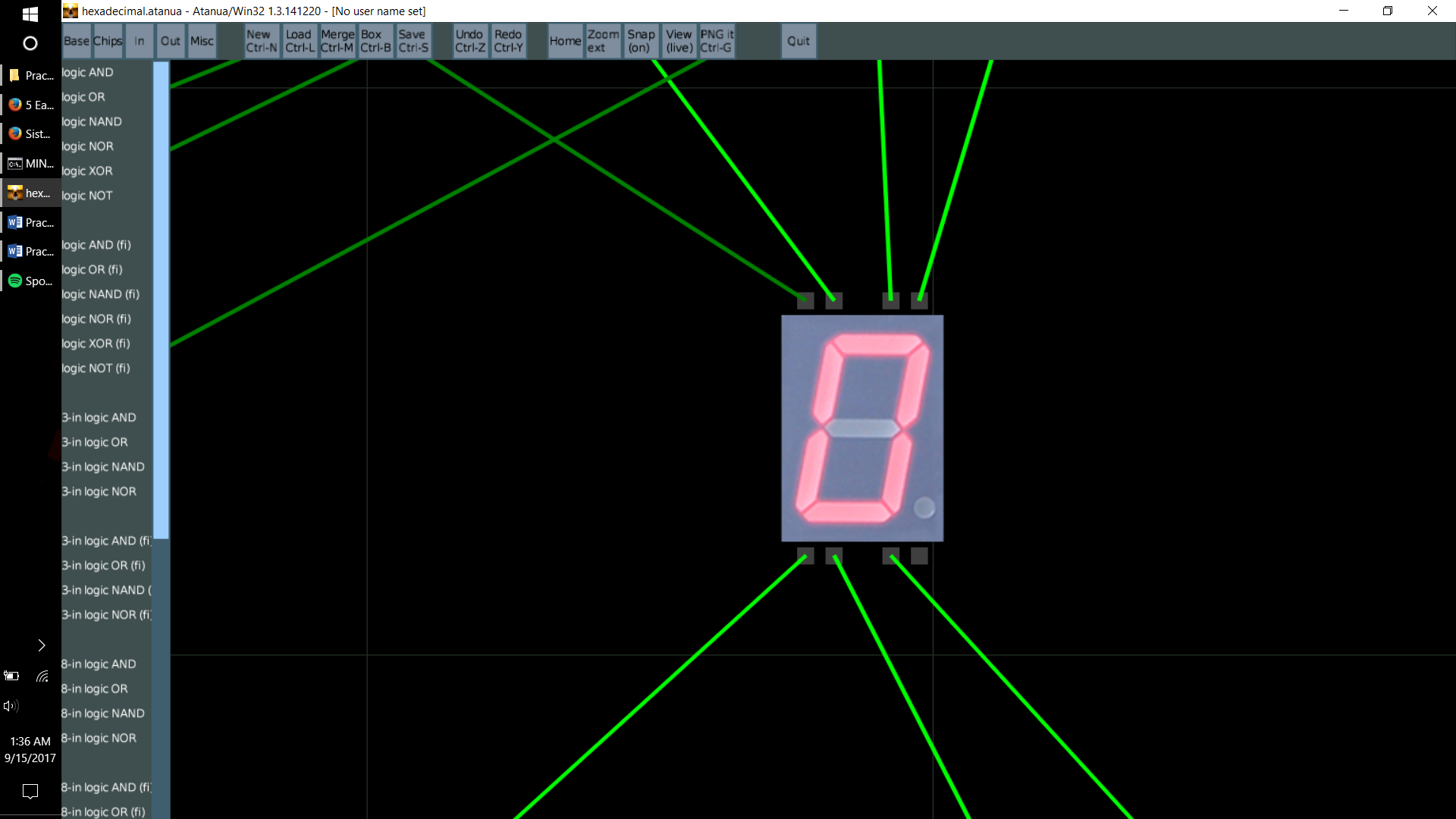
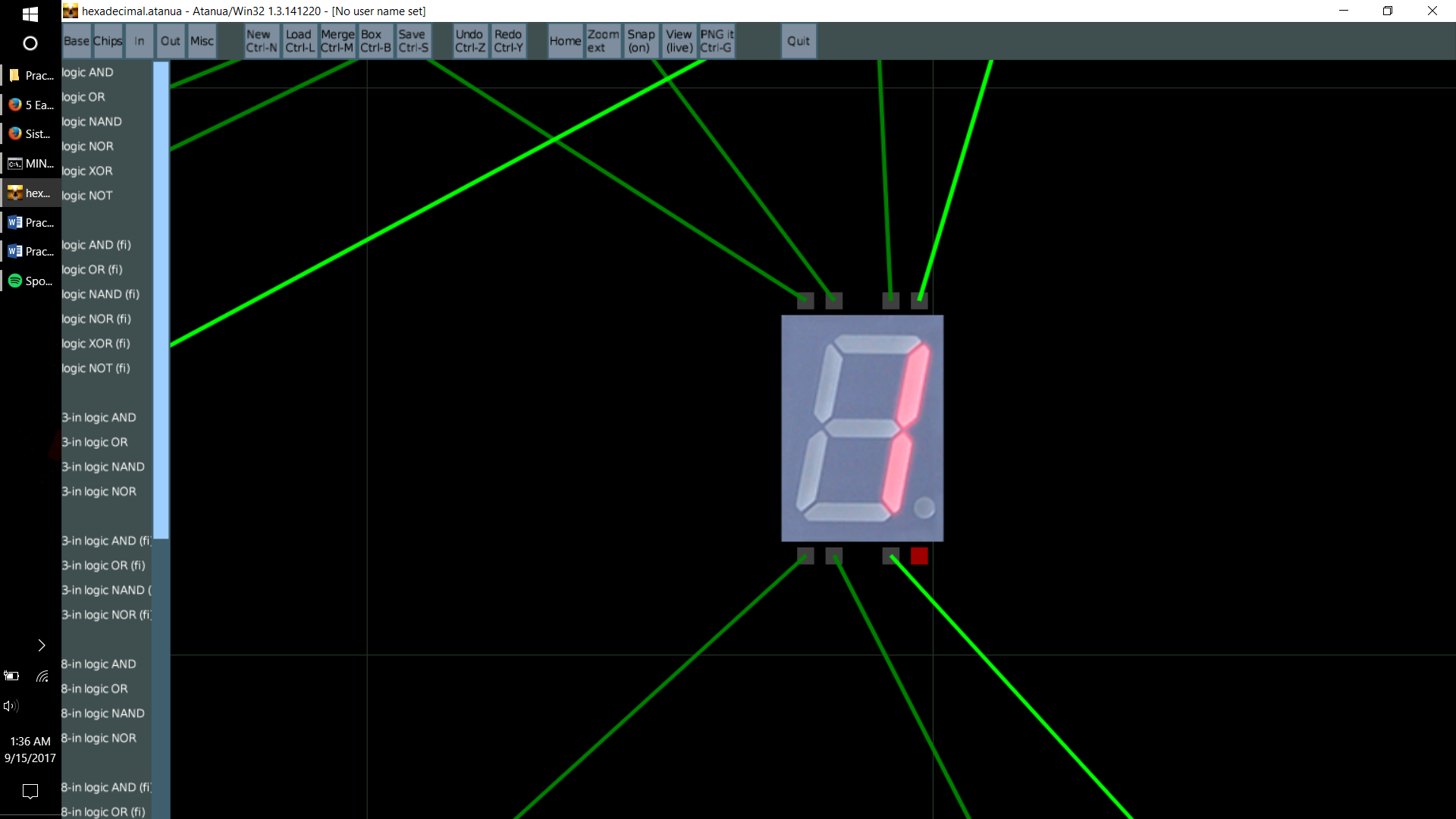
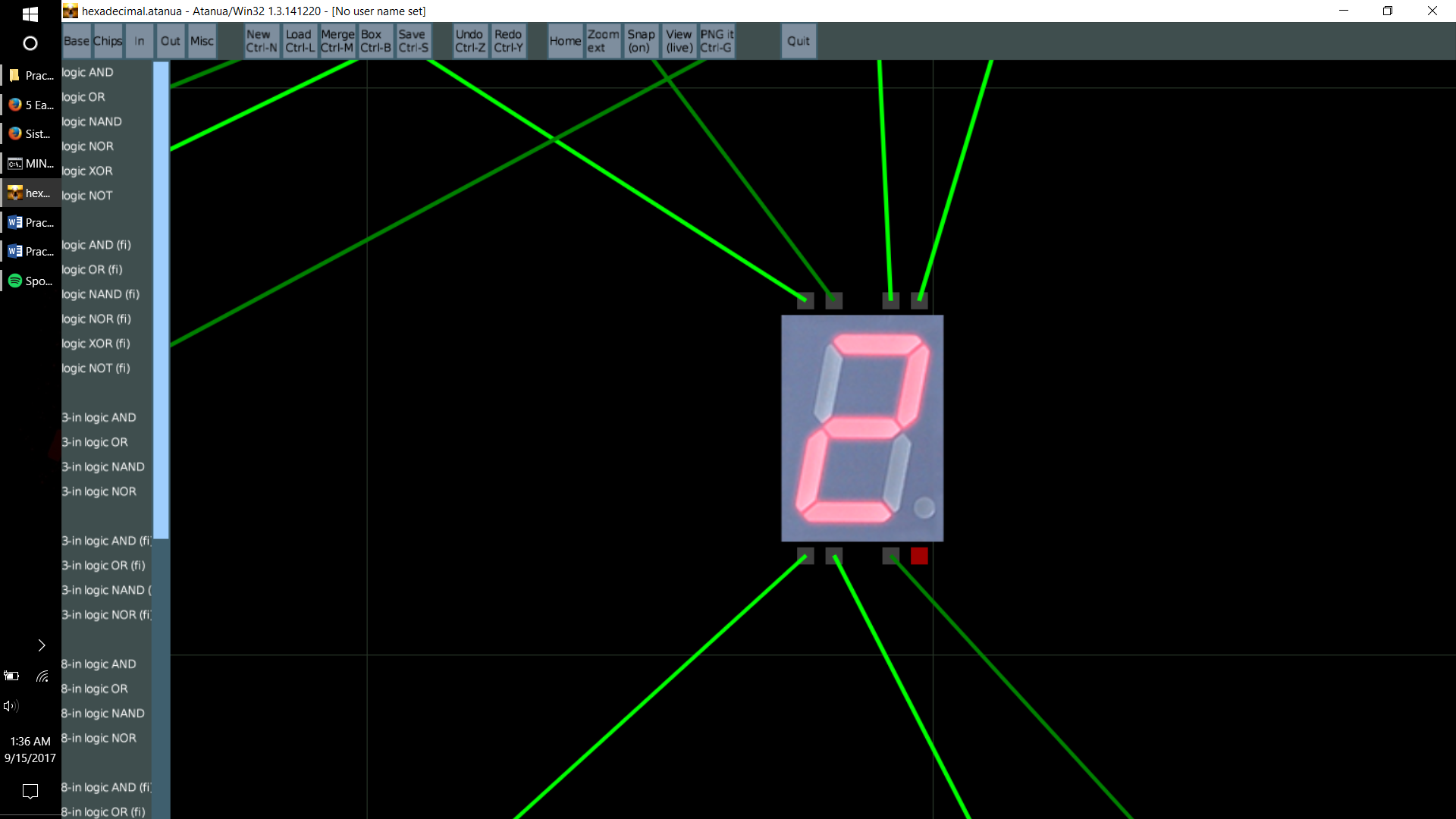
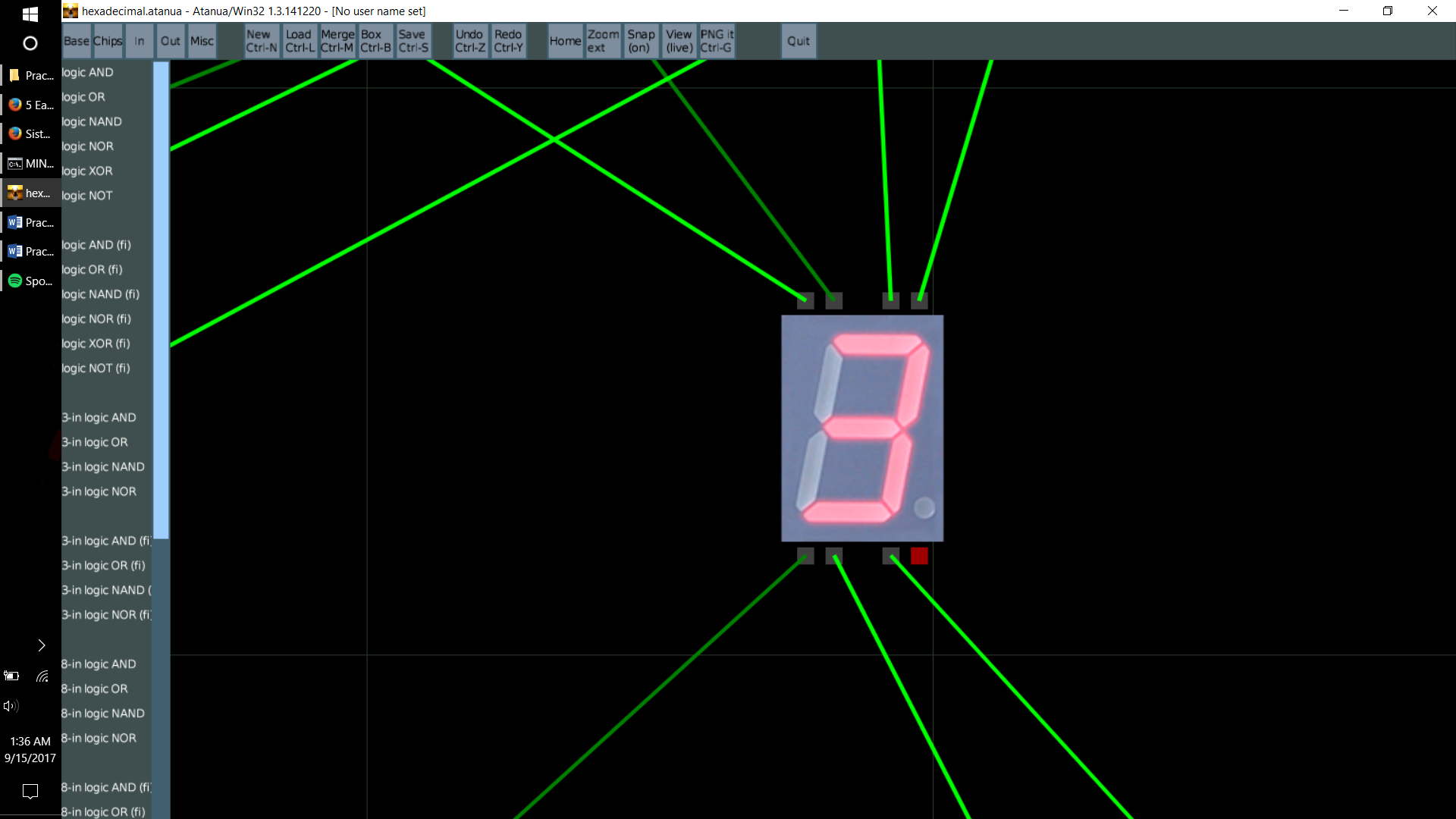
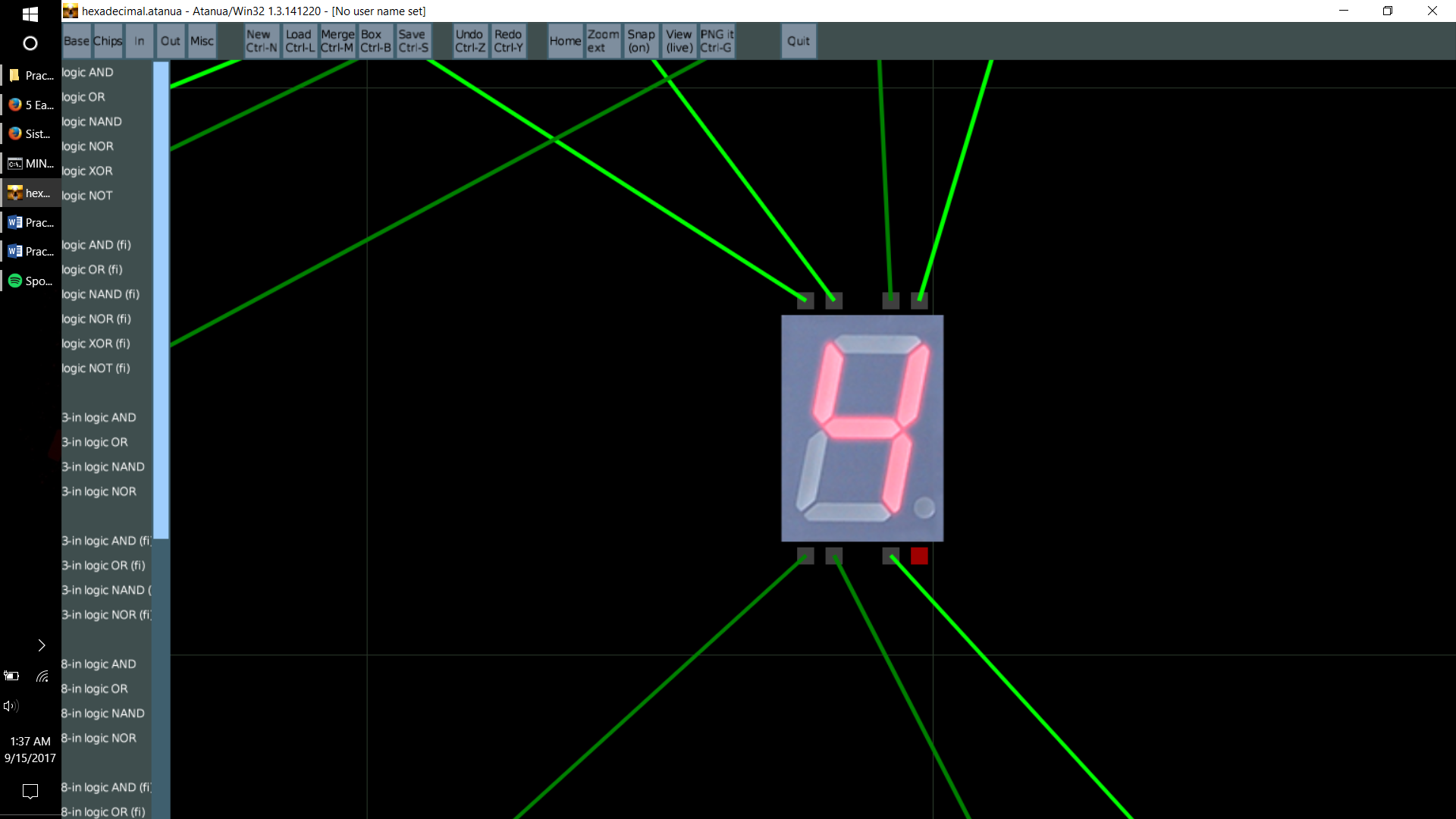
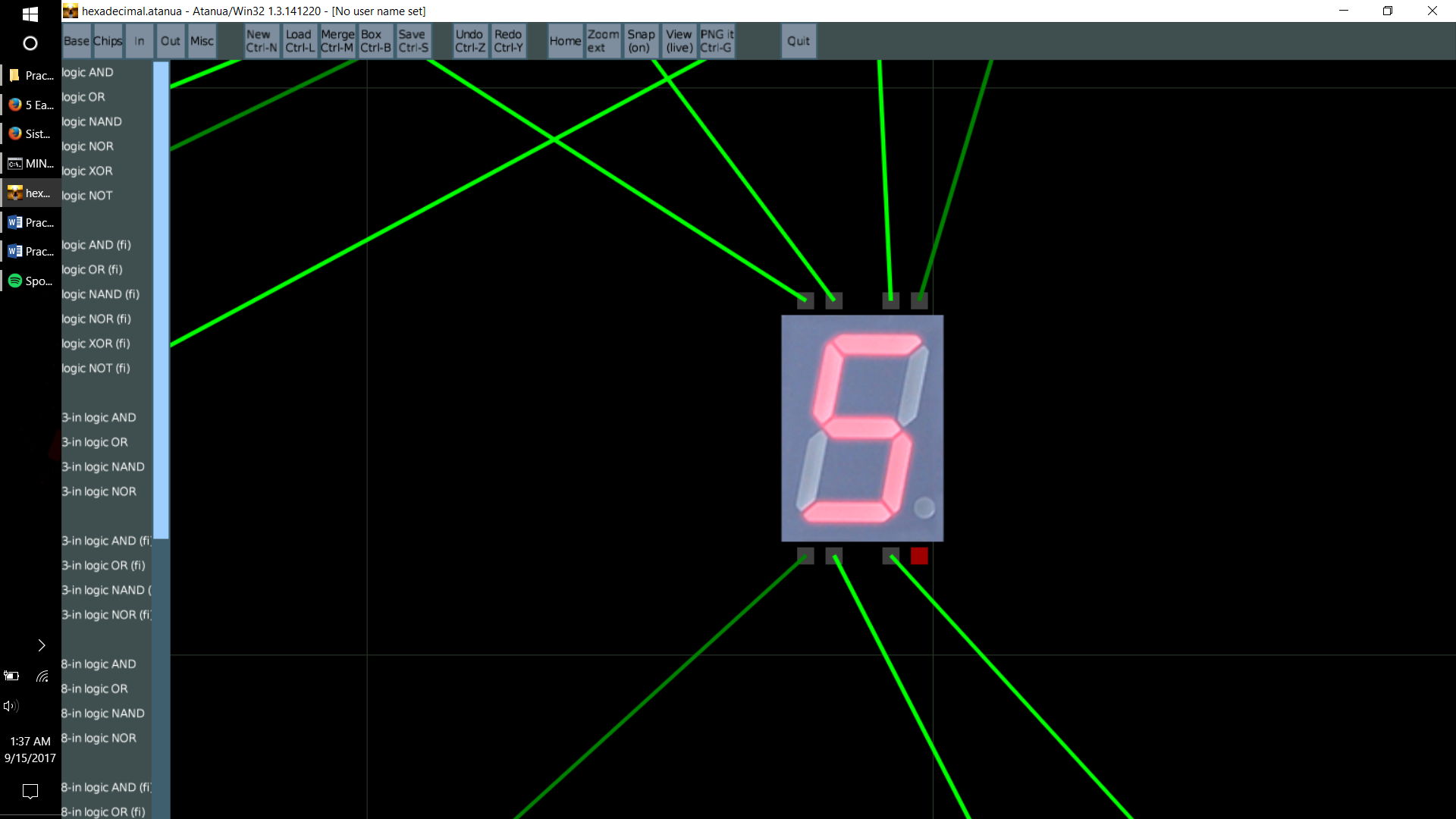
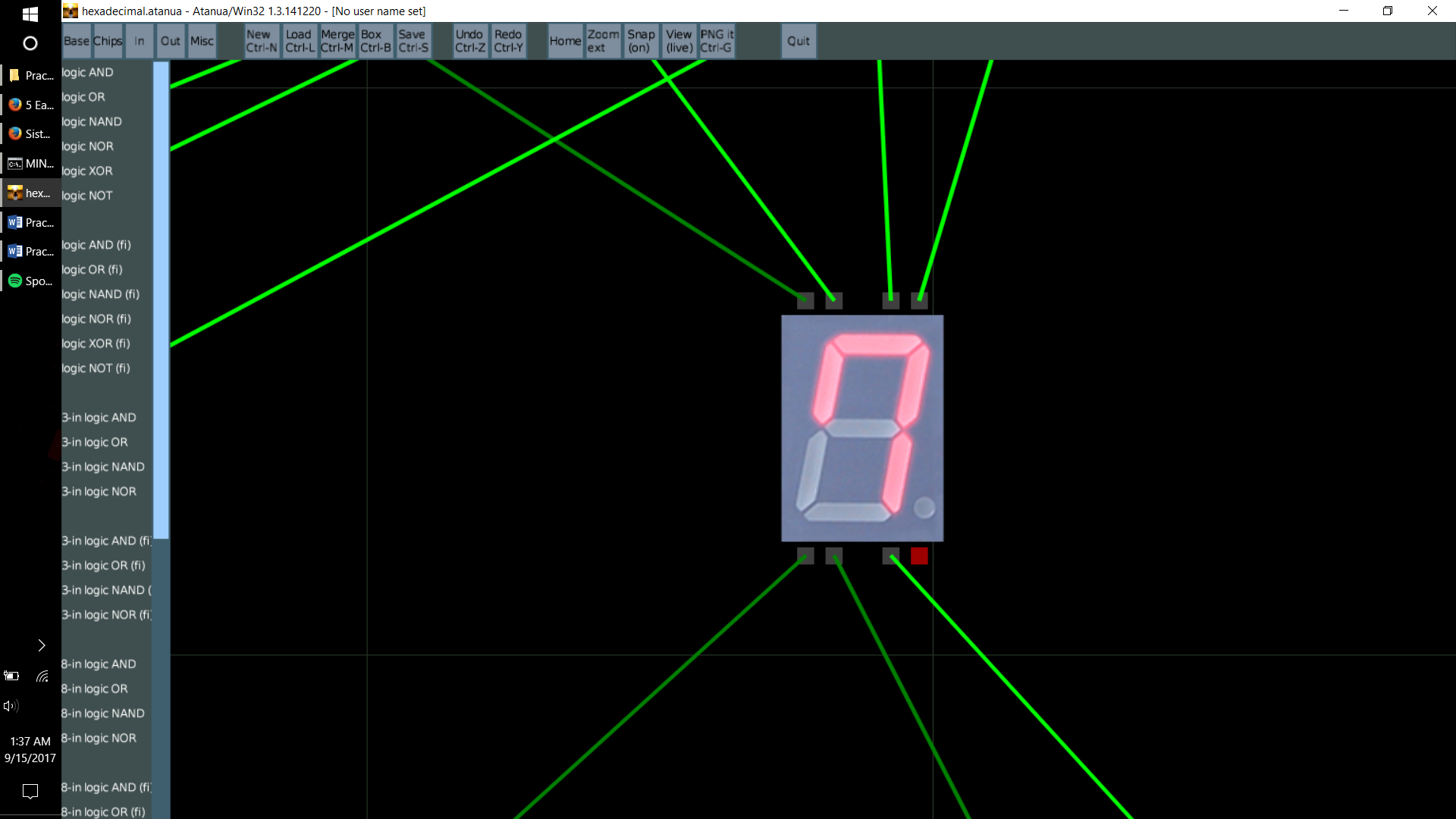
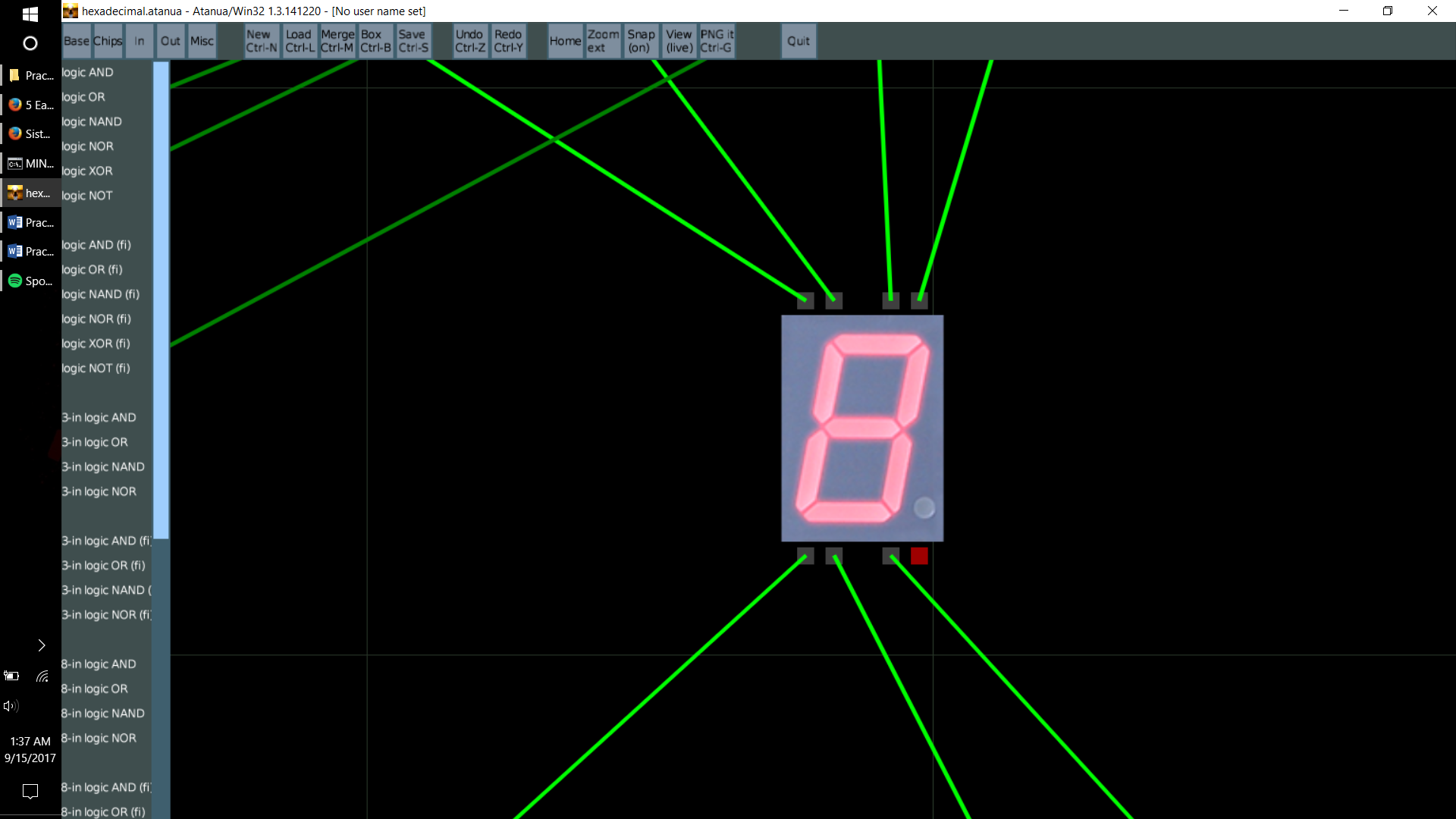
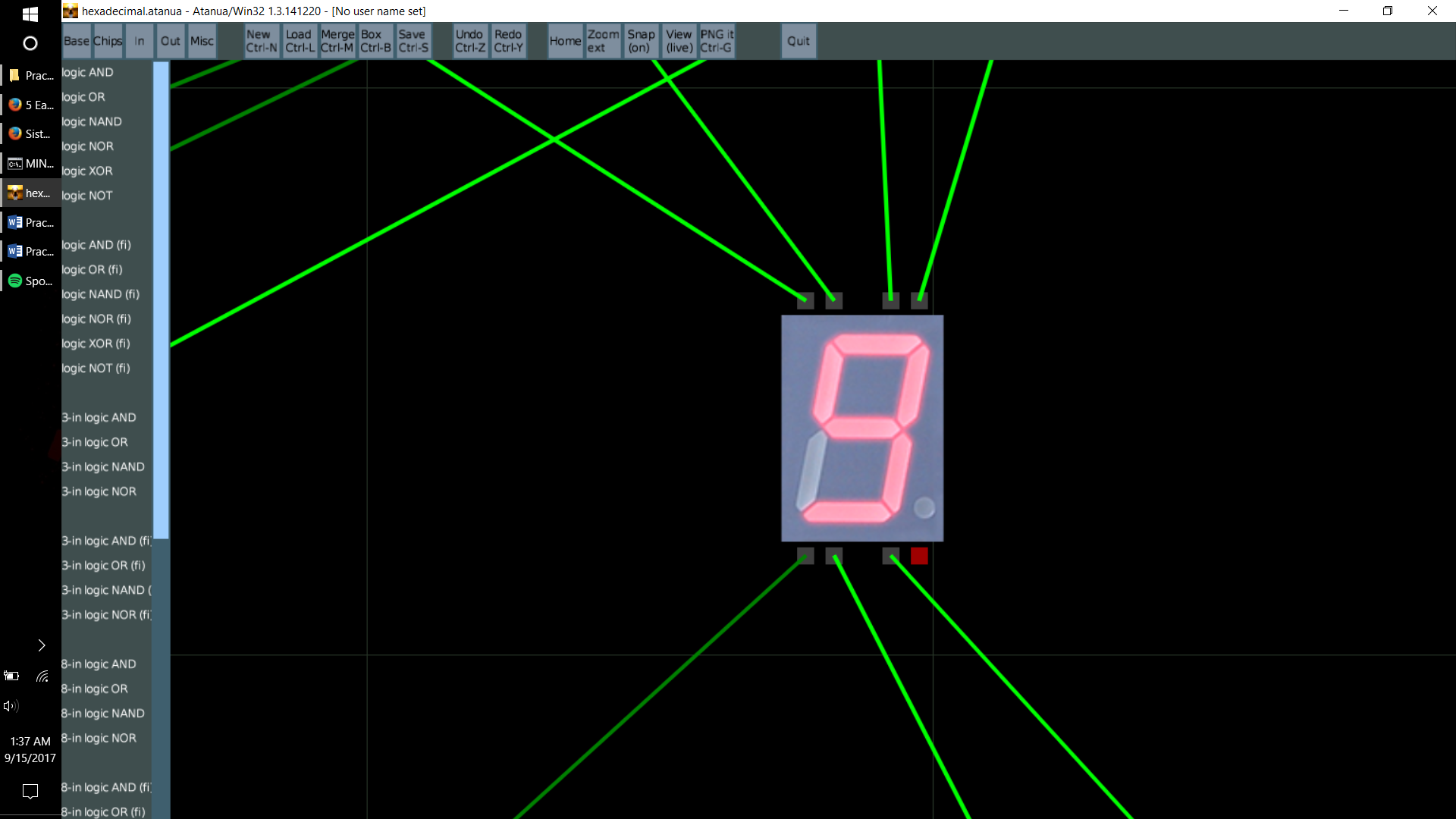
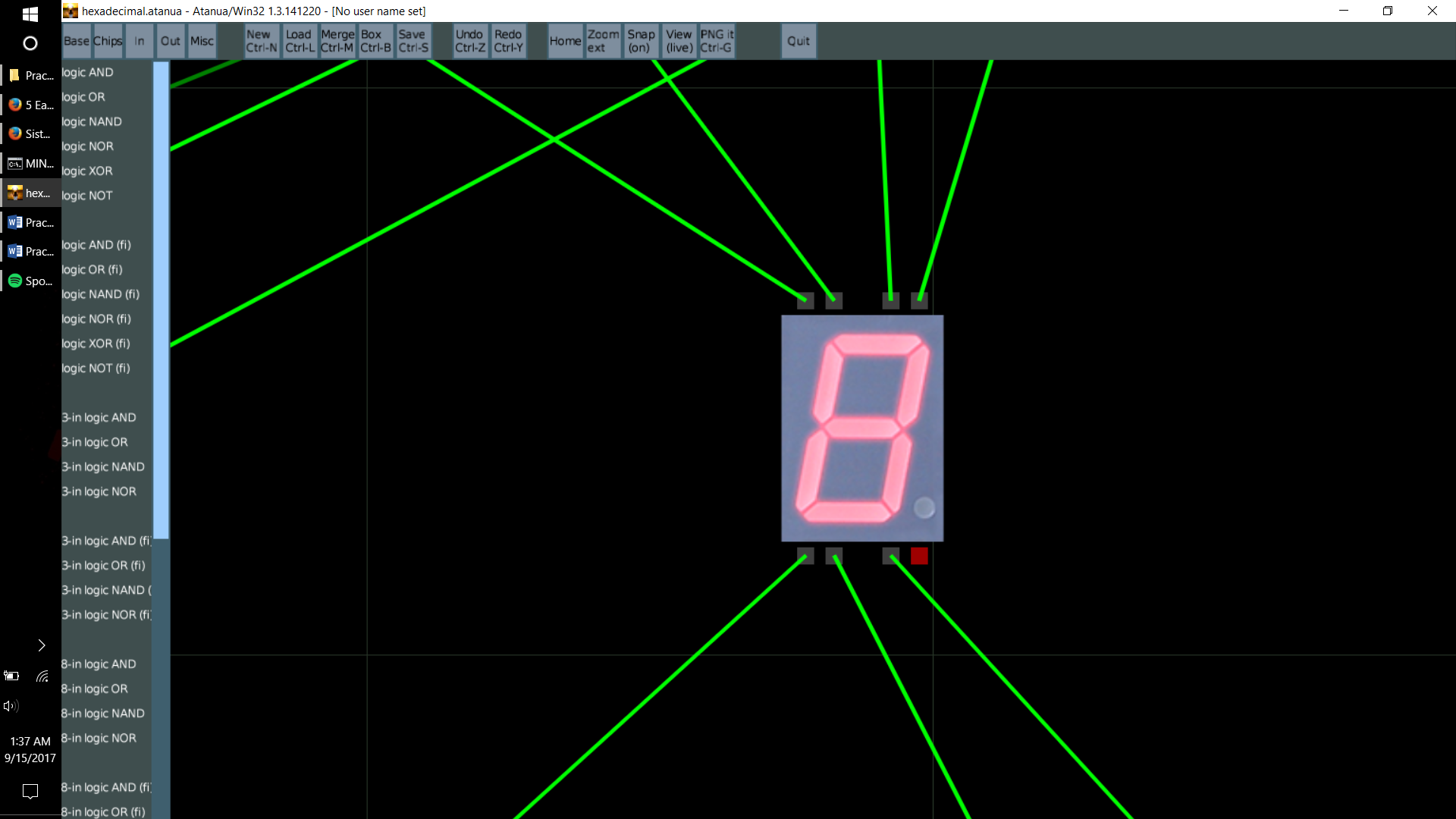
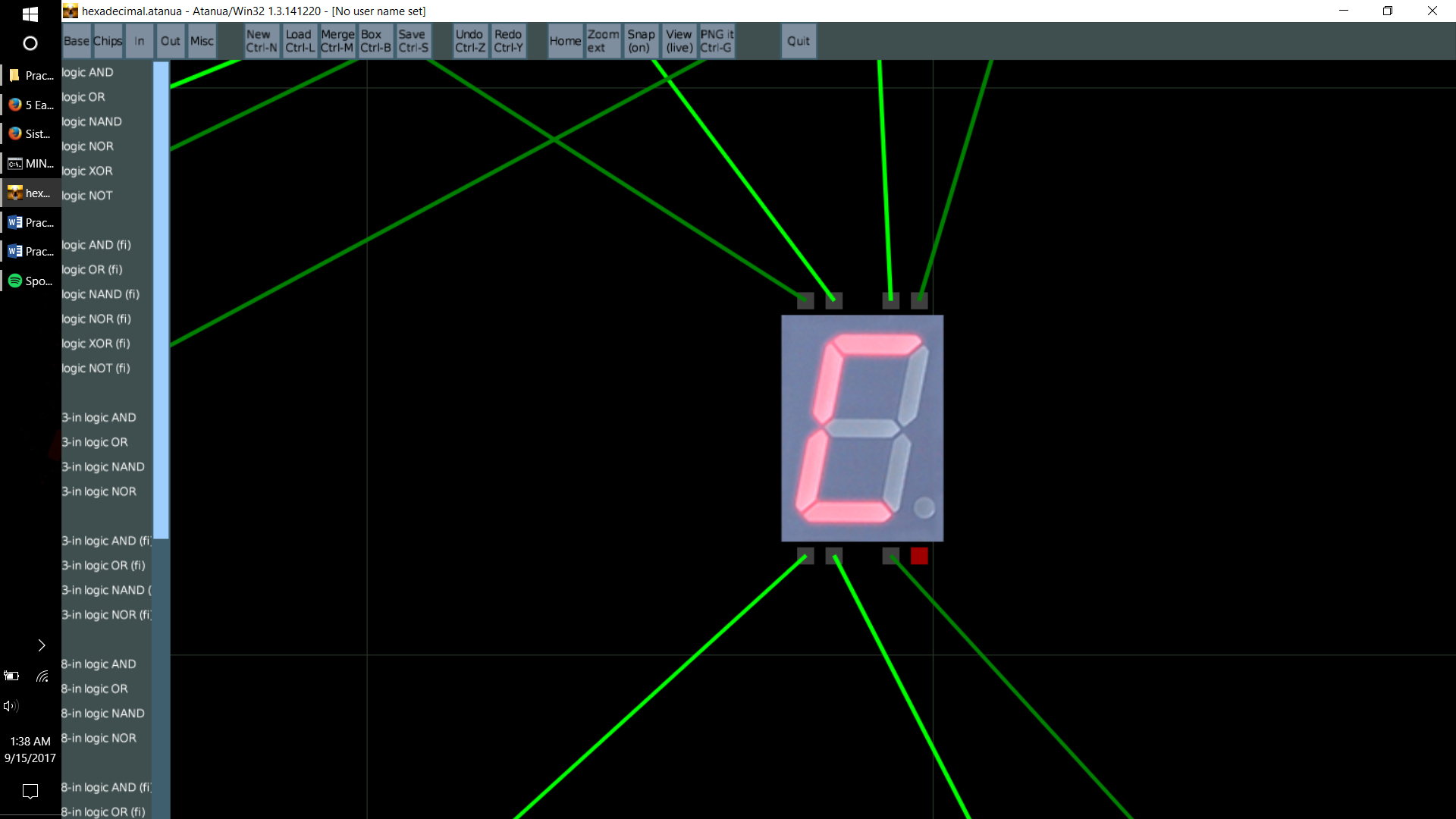
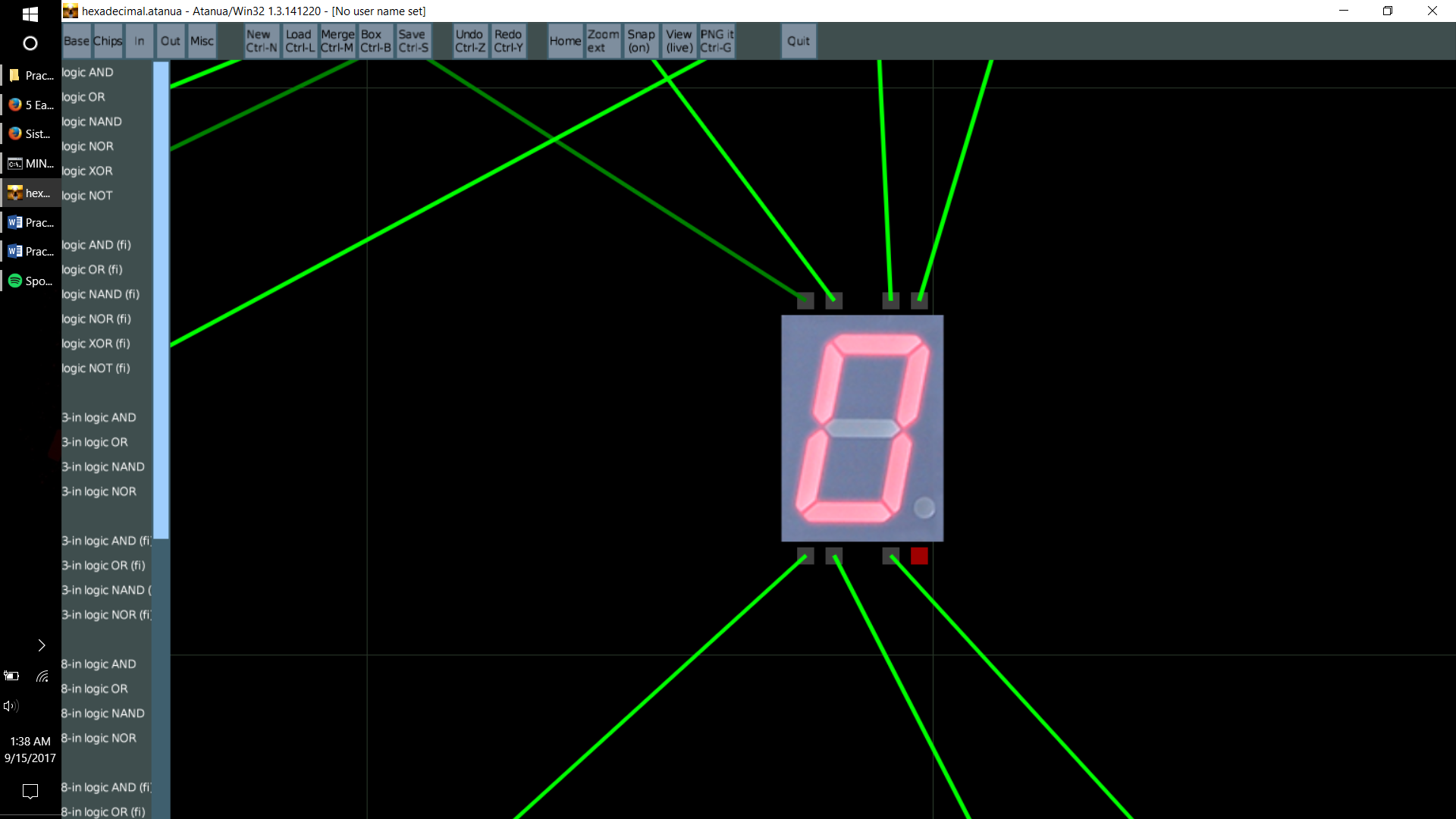
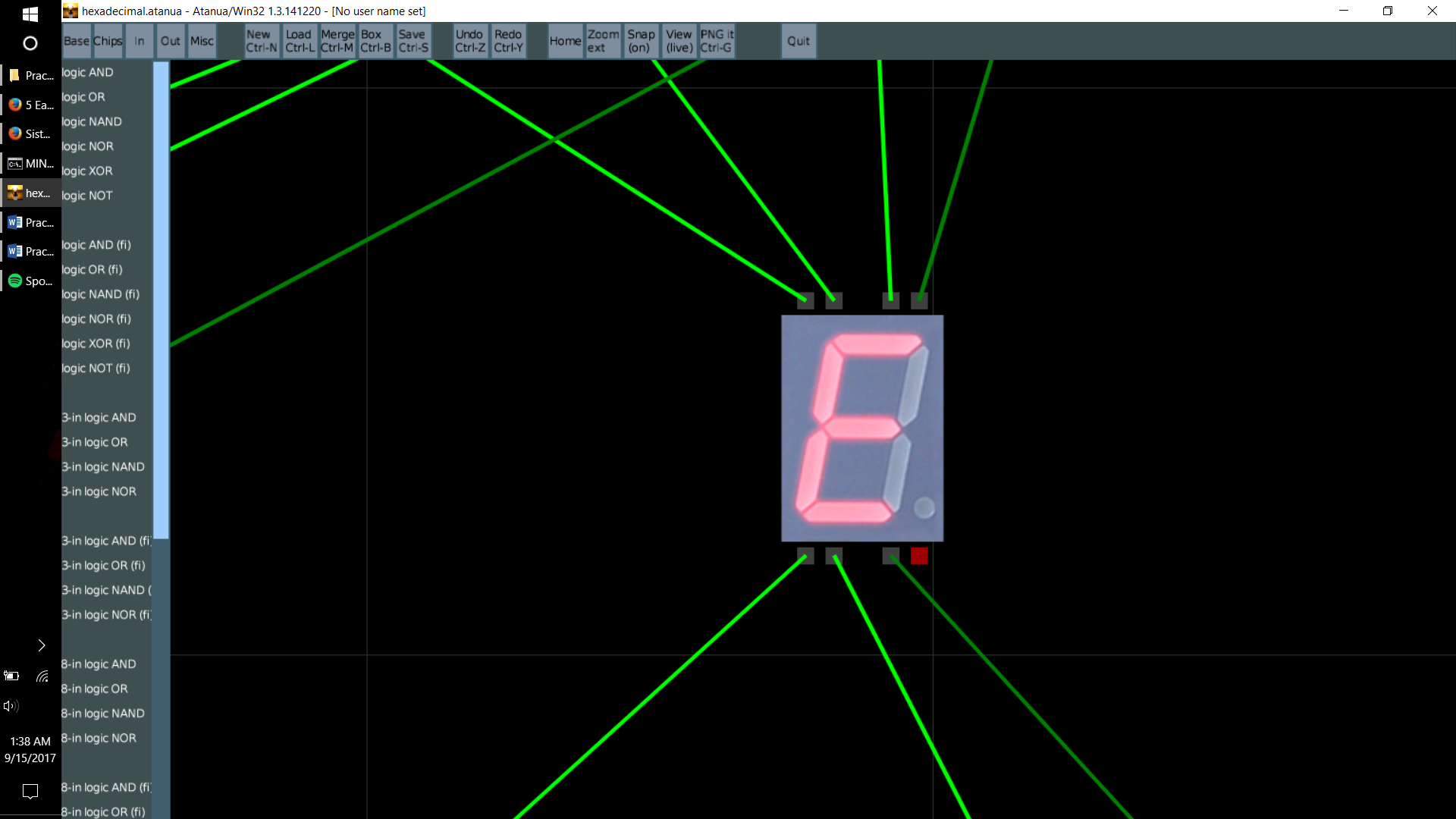
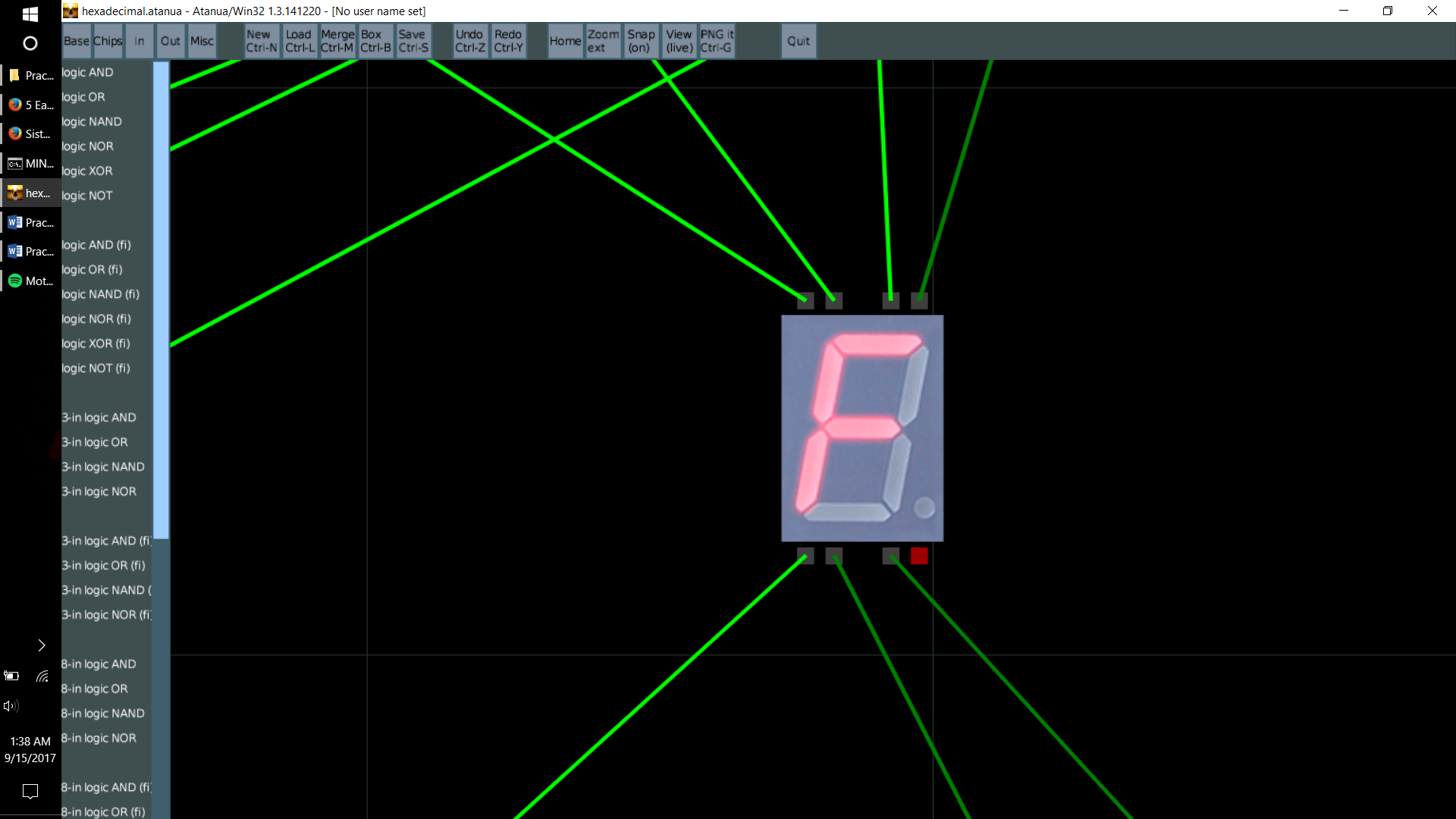
Adrián Emilio Vázquez Icedo

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15 septiembre de 2017

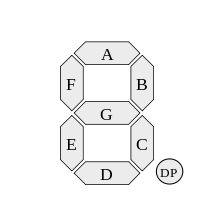
Hermosillo, Sonora

En estos podemos apreciar el despliegue de los elementos del conjunto de dígitos del sistema decimal y del sistema hexadecimal, cada uno calculado por medio de compuertas lógicas simples, y desplegado en un display de 7 segmentos.

Se presentan los 16 estados posibles del display.

Estos son generados por una tabla de verdad, cada columna es un segmento del display, estos 7 segmentos pueden ser controlados para mostrar los 16 estados con unicamente 4 bits, dado que estos dan 16 estados distintos.



|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  | A | B | C | D | E | F | G |  | Numero |
| 0 | 0 | 0 | 0 |  | 1 | 1 | 1 | 1 | 1 | 1 | 0 |  | 0 |
| 0 | 0 | 0 | 1 |  | 0 | 1 | 1 | 0 | 0 | 0 | 0 |  | 1 |
| 0 | 0 | 1 | 0 |  | 1 | 1 | 0 | 1 | 1 | 0 | 1 |  | 2 |
| 0 | 0 | 1 | 1 |  | 1 | 1 | 1 | 1 | 0 | 0 | 1 |  | 3 |
| 0 | 1 | 0 | 0 |  | 0 | 1 | 1 | 0 | 0 | 1 | 1 |  | 4 |
| 0 | 1 | 0 | 1 |  | 1 | 0 | 1 | 1 | 0 | 1 | 1 |  | 5 |
| 0 | 1 | 1 | 0 |  | 1 | 0 | 1 | 1 | 1 | 1 | 1 |  | 6 |
| 0 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 0 | 1 | 1 |  | 7 |
| 1 | 0 | 0 | 0 |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 8 |
| 1 | 0 | 0 | 1 |  | 1 | 1 | 1 | 1 | 0 | 1 | 1 |  | 9 |
| 1 | 0 | 1 | 0 |  | 1 | 1 | 1 | 0 | 1 | 1 | 1 |  | A |
| 1 | 0 | 1 | 1 |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | B |
| 1 | 1 | 0 | 0 |  | 1 | 0 | 0 | 1 | 1 | 1 | 0 |  | C |
| 1 | 1 | 0 | 1 |  | 1 | 1 | 1 | 1 | 1 | 1 | 0 |  | D |
| 1 | 1 | 1 | 0 |  | 1 | 0 | 0 | 1 | 1 | 1 | 1 |  | E |
| 1 | 1 | 1 | 1 |  | 1 | 0 | 0 | 0 | 1 | 1 | 1 |  | F |

Para representar esta tabla de verdad se utilizara AND(&), OR(|) y NOT(~)

Para el segmento llamado A, tenemos que sus valores de verdad para ser activado son

( ~a&~b&~c&~d ) | ( ~a&~b&c&~d ) | ( ~a&~b&c&d ) | ( ~a&b&~c&d ) |( ~a&b&c&~d ) | ( ~a&b&c&d ) | ( a&~b&~c&~d ) | ( a&~b&~c&d ) | ( a&~b&c&~d ) | ( a&~b&c&d ) | ( a&b&~c&~d ) | ( a&b&~c&d ) | (a&b&c&~d ) | ( a&b&c&d )

=> (~a&~b) & ((~b&d)|(b&~d))

Segmento B.

(~a&~b&~c&~d) | (~a&~b&~c&d) | (~a&~b&c&~d) | (~a&~b&c&d) | (~a&b&~c&~d) | (~a&b&c&d) | (a&~b&~c&~d) | (a&~b&~c&d) | (a&~b&c&~d) | (a&~b&c&d) | (a&b&~c&d)

=> (~a&b) & ((~c&d)|(c&~d))

Segmento C.

(~a&~b&~c&~d) | (~a&~b&~c&d) | (~a&~b&c&d) | (~a&b&~c&~d) | (~a&b&~c&d) | (~a&b&c&~d) | (~a&b&c&d) | (a&~b&~c&~d) | (a&~b&~c&d) | (a&~b&c&~d) | (a&~b&c&d) | (a&b&~c&d)

=> ~a&~b&c&~d

Segmento D.

(~a&~b&~c&~d) | (~a&~b&c&~d) | (~a&~b&c&d) | (~a&b&~c&d) | (~a&b&c&~d) | (~a&b&c&d) | (a&~b&~c&~d) | (a&~b&~c&d) | (a&~b&c&d) | (a&b&~c&~d) | (a&b&~c&d) | (a&b&c&~d)

=> ~a&((~b&~c&d)|(b&~c&~d)|(b&c&d))

Segmento E.

(~a&~b&~c&~d) | (~a&~b&c&~d) | (~a&b&c&~d)| (~a&b&c&~d)| (a&~b&~c&~d)| (a&~b&~c&~d)| (a&~b&c&~d)| (a&~b&c&d)| (a&b&~c&~d)| (a&b&~c&d)| (a&b&c&~d)| (a&b&c&d)

=> ~d & ((~b&~c) | (~a&c))

Segmento F.

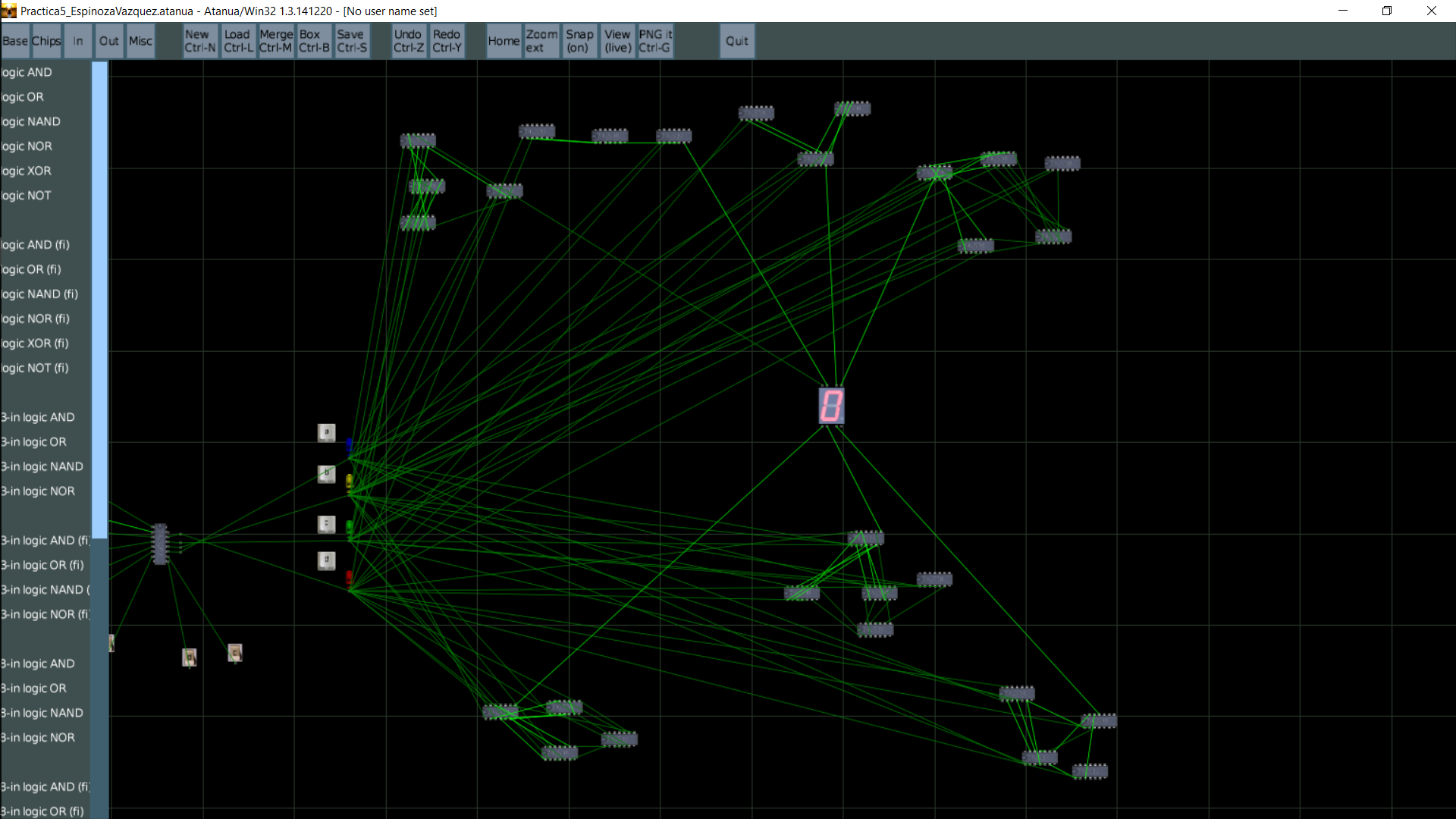
(~a&~b&~c&~d) | (~a&b&~c&~d) | (~a&b&~c&d) | (~a&b&c&~d) | (~a&b&c&d) | (a&~b&~c&~d) | (a&~b&~c&d) | (a&~b&c&~d) | (a&~b&c&d) | (a&b&~c&~d) | (a&b&~c&d) | (a&b&c&~d) | (a&b&c&d)

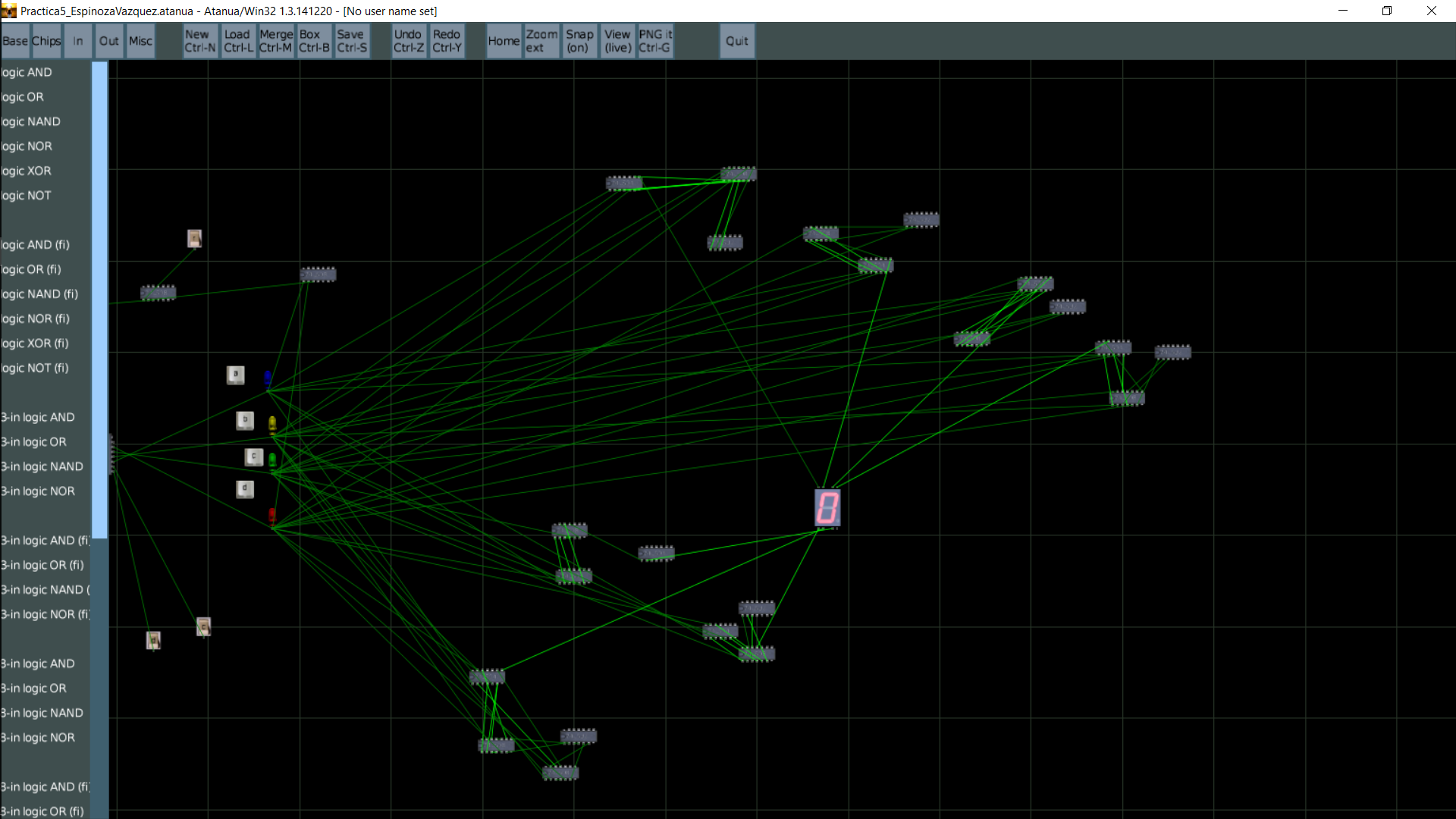
=> (~a&~b) & ((~c&d)|c)

Segmento G.

(~a&~b&c&~d) | (~a&~b&c&d) | (~a&b&~c&~d) | (~a&b&~c&d) | (~a&b&c&~d) | (~a&b&c&d) | (a&~b&~c&~d) | (a&~b&~c&d) | (a&~b&c&~d) | (a&~b&c&d) | (a&b&c&~d) | (a&b&c&d)

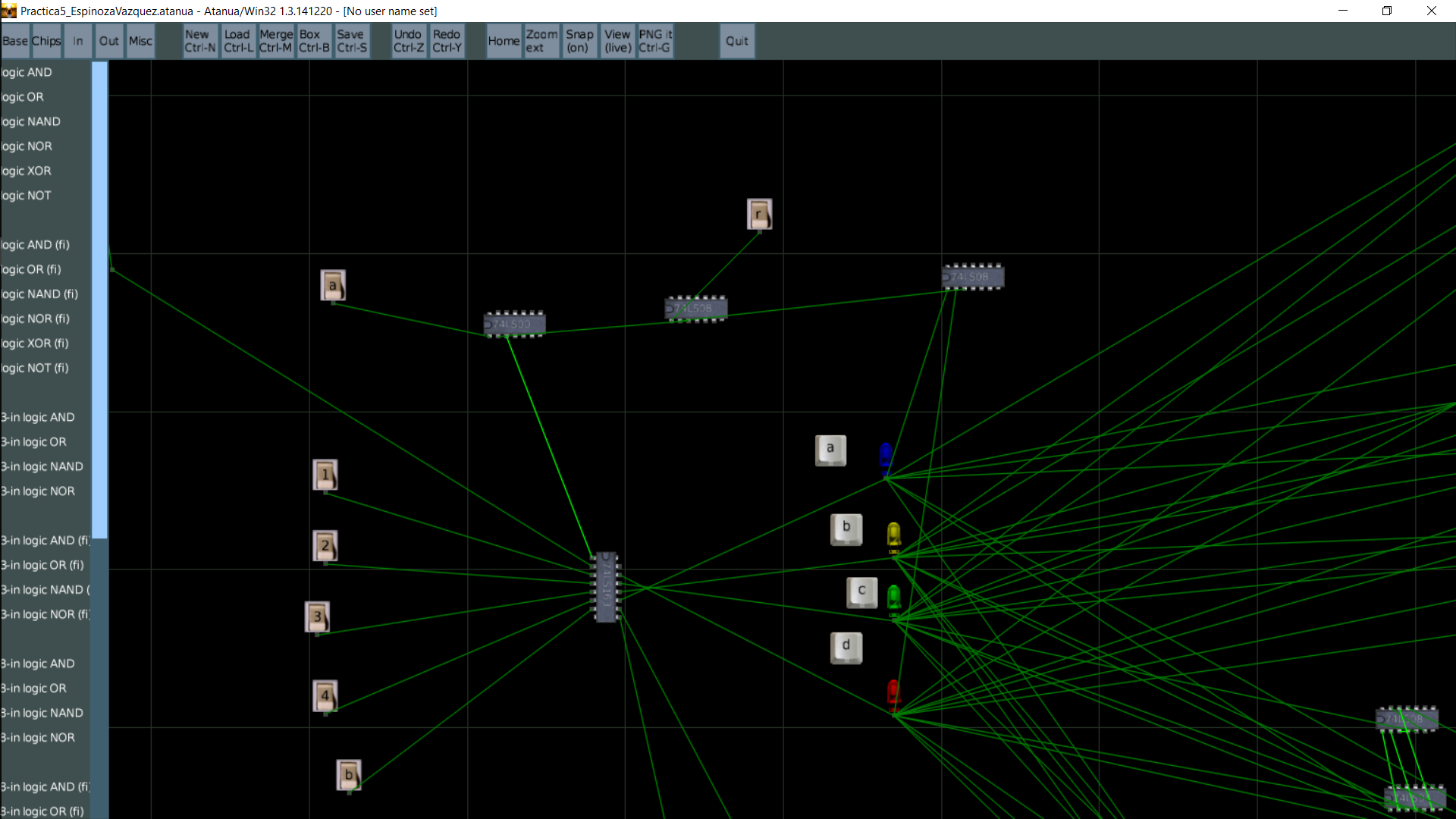
=> ~a & ((~b&~c)|(b&c&d))

Apreciacion de la cantidad total de circuitos logicos para la manipulacion de los 16 estados. Se pueden observar 7 grupos de ciruitos logicos conectados al display; cada uno de estos grupos maneja cada un segmento del mismo, cada grupo esta en forma reducida.

Grupos de circuitos logicos para la visualizacion de solo 10 estados de la combiancion de los 4 bits, de igual manera se aprecian 7 grupos de circuitos logicos, uno para cada segmento. En este modelo se utilizan menos estados, por lo que los circuitos pueden ser reducidos ya que la tabla de verdad es de la siguiente forma.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
|  |  |  |  |  | A | B | C | D | E | F | G |  | Numero |
| 0 | 0 | 0 | 0 |  | 1 | 1 | 1 | 1 | 1 | 1 | 0 |  | 0 |
| 0 | 0 | 0 | 1 |  | 0 | 1 | 1 | 0 | 0 | 0 | 0 |  | 1 |
| 0 | 0 | 1 | 0 |  | 1 | 1 | 0 | 1 | 1 | 0 | 1 |  | 2 |
| 0 | 0 | 1 | 1 |  | 1 | 1 | 1 | 1 | 0 | 0 | 1 |  | 3 |
| 0 | 1 | 0 | 0 |  | 0 | 1 | 1 | 0 | 0 | 1 | 1 |  | 4 |
| 0 | 1 | 0 | 1 |  | 1 | 0 | 1 | 1 | 0 | 1 | 1 |  | 5 |
| 0 | 1 | 1 | 0 |  | 1 | 0 | 1 | 1 | 1 | 1 | 1 |  | 6 |
| 0 | 1 | 1 | 1 |  | 1 | 1 | 1 | 1 | 0 | 1 | 1 |  | 7 |
| 1 | 0 | 0 | 0 |  | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  | 8 |
| 1 | 0 | 0 | 1 |  | 1 | 1 | 1 | 1 | 0 | 1 | 1 |  | 9 |
| 1 | 0 | 1 | 0 |  | - | R | E | S | E | T | - |  | A |
| 1 | 0 | 1 | 1 |  |  |  | N | / | A |  |  |  | B |
| 1 | 1 | 0 | 0 |  |  |  | N | / | A |  |  |  | C |
| 1 | 1 | 0 | 1 |  |  |  | N | / | A |  |  |  | D |
| 1 | 1 | 1 | 0 |  |  |  | N | / | A |  |  |  | E |
| 1 | 1 | 1 | 1 |  |  |  | N | / | A |  |  |  | F |

Por lo tanto se pueden ignorar bastantes estados y los cirucitos logicos llegan a ser mas sencillos que los de 16 estados.

Este conjunto de chips ajeno al manejo del display sirve para cuando se llegue al estado numero 10 (1001) el contador se reinicie y vuelva a 0, dando como resultado los 10 estados necesarios para visualizar los diez digitos del sistema decimal