

# ASSEMBLY TO QUANTUM COMPILER

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## ABSTRACT

This research presents a novel approach in quantum computing by transforming ARM assembly instructions for use in quantum algorithms. The core achievement is the development of a method to directly map the ARM assembly language, a staple in classical computing, to quantum computing paradigms. The practical application of this methodology is demonstrated through the computation of the Fibonacci sequence. This example serves to validate the approach and underscores its potential in simplifying quantum algorithms. Grover's Algorithm was realized through the use of quantum-specific instructions. These transformations were developed as part of an open-source assembly-to-quantum compiler ([github.com/arhaverly/AssemblyToQuantumCompiler](https://github.com/arhaverly/AssemblyToQuantumCompiler)). This effort introduces a novel approach to utilizing classical instruction sets in quantum computing and offers insight into potential future developments in the field. The AssemblyToQuantumCompiler streamlines quantum programming and enables computer scientists to transition more easily from classical to quantum computer programming.

## 1. INTRODUCTION

Quantum computing extends beyond the limits of classical computation by exploiting fundamental principles such as superposition and entanglement. Superposition permits a quantum system to occupy multiple states concurrently until measurement, resulting in an exponential expansion of the computational state space as the number of qubits increases. Entanglement, a defining quantum property, allows pairs or groups of qubits to exist in correlated states such that the state of one qubit instantaneously influences the state of another, irrespective of spatial separation. This intrinsic correlation enables complex multi-qubit operations and forms the basis of quantum computing's capacity to achieve exceptional computational efficiency. Through the exploitation of these phenomena, quantum computers can execute certain computations significantly faster and with fewer operations than classical systems, leading to substantial gains in computational capability and efficiency.

Many classical algorithms lack straightforward mappings

to quantum algorithms due to the fundamental differences between classical and quantum computational models. Nevertheless, the ability to compile classical algorithms into quantum equivalents remains valuable. In the context of Grover's algorithm, for instance, the oracle can be implemented using Boolean-like operations, as demonstrated in applications to the Boolean satisfiability problem [1, 2]. Extending such Boolean-like operations broadens the range of problems to which Grover's algorithm can be effectively applied.

Quantum gates are the basic components of quantum circuits, similar to logic gates in classical computing [3]. Many of these gates are listed below.

## Pauli Gates

- **X Gate:** Applies the Pauli-X transformation, corresponding to a  $\pi$ -radian rotation of the qubit about the X-axis.
- **Y Gate:** Applies the Pauli-Y transformation, corresponding to a  $\pi$ -radian rotation of the qubit about the Y-axis.
- **Z Gate:** Applies the Pauli-Z transformation, corresponding to a  $\pi$ -radian rotation of the qubit about the Z-axis.

## Clifford Gates

- **Hadamard (H) Gate:** Transforms a computational basis state into an equal superposition of  $|0\rangle$  and  $|1\rangle$ .
- **S Gate:** A phase-shift gate that applies a phase of  $\pi/2$ .
- **Sdg Gate:** The Hermitian adjoint of the S gate.
- **CNOT Gate:** Performs a controlled-NOT operation on a pair of qubits.
- **SWAP Gate:** Exchanges the quantum states of two qubits.

## Phase Gates

- **T Gate:** Applies a phase shift of  $\pi/4$ .
- **Tdg Gate:** The Hermitian adjoint of the T gate.
- **U Gates:** General single-qubit unitary operations (U1, U2, U3) capable of representing any single-qubit transformation.

## Rotation Gates

- **RX Gate:** Performs a rotation of a qubit by a specified angle about the X-axis.
- **RY Gate:** Performs a rotation of a qubit by a specified angle about the Y-axis.
- **RZ Gate:** Performs a rotation of a qubit by a specified angle about the Z-axis.

## Controlled Gates

- **Controlled U Gates:** Including CU1, CU2, and CU3, which apply controlled versions of single-qubit unitary operations.
- **CCX Gate (Toffoli Gate):** A NOT operation controlled by two qubits.
- **CSWAP Gate (Fredkin Gate):** Executes a controlled swap between two qubits.

## Advanced Quantum Gates

- **Barrier:** A circuit directive used to delineate and prevent reordering of quantum operations.
- **CRX, CRY, CRZ Gates:** Controlled single-axis rotation gates.
- **Quantum Fourier Transform (QFT)–Related Gates:** Gates commonly employed in algorithms that rely on Fourier transforms.

## Additional Quantum Gates in Qiskit [4]

- **Multi-Controlled Gates:** Gates such as multi-controlled Toffoli (MCT) gates, which extend the CCX gate to an arbitrary number of control qubits.
- **Ising Gates:** Including XX, YY, and ZZ gates, primarily used in quantum simulations of Ising-type Hamiltonians.
- **RXX, RYY, RZZ Gates:** Two-qubit rotation gates about the XX, YY, and ZZ interaction axes.
- **Reset Gate:** Reinitializes a qubit to the  $|0\rangle$  state.

- **Identity Gate (I):** Implements the identity operation, leaving the qubit state unchanged.
- **R Gate:** A general single-qubit rotation gate parameterized by both rotation angle and phase.
- **SX Gate:** Represents the square root of the X gate, also referred to as the  $\sqrt{\text{NOT}}$  gate.
- **SXdg Gate:** The Hermitian adjoint of the SX gate.

These gates collectively form a foundational toolkit for exploiting quantum mechanical phenomena in computation, including superposition, entanglement, and quantum interference.

This manuscript presents a mapping from assembly instructions to quantum circuits, applies these circuits to compute the Fibonacci sequence, implements Grover's algorithm using assembly-level instructions, introduces the open-source project associated with this work, and concludes with a summary of findings.

## 2. MAPPING ASSEMBLY INSTRUCTIONS TO QUANTUM CIRCUITS

While many quantum gates are unique to quantum computation, several have clear analogues in classical assembly instructions. In this work, ARM Assembly Language is adopted as the classical reference [5, 6]. Tables 1 and 2 present a correspondence between ARM assembly operations and their closest equivalents in quantum circuit form.

It should be noted that all subtraction operations discussed here employ reset operations to reduce overall circuit size. In scenarios where quantum coherence must be preserved, coherence can be maintained by introducing additional ancilla qubits and avoiding reset operations.

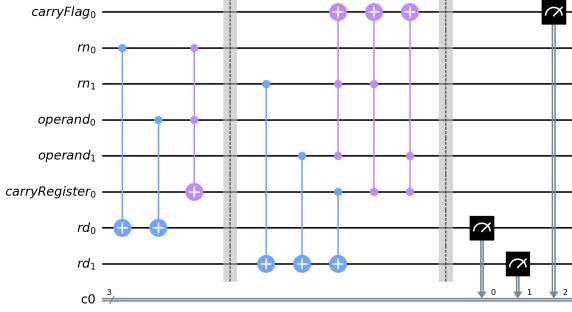
**Table 1:** Mapping of Assembly Instructions to Quantum Operations

Mnemonic	Instruction	Classical		Quantum		
		Action	Example	Quantum Transformation	Coherence Maintaining?	Additional Notes
ADC	Add with carry	$Rd := Rn + Op2 + \text{Carry}$	ADC Rd, Rn, Operand2	Figure 1	Yes	
ADD	Add	$Rd := Rn + Op2$	ADD Rd, Rn, Rm	Figure 2	Yes	
AND	AND	$Rd := Rn \text{ AND } Op2$	AND Rd, Rn, Operand2	Figure 3	Yes	
B	Branch	$R15 := \text{address}$	B label	N/A	Yes	Unravel the branch
BEQ	Branch if Equal	$R15 := \text{address if Z flag is set}$	BEQ label	N/A	Yes	Unravel the branch, then use controlled gates to conditionally run operations
BIC	Bit Clear	$Rd := Rn \text{ AND NOT } Op2$	BIC Rd, Rn, Operand2	Figure 4	Yes	
BL	Branch with Link	$R14 := R15, R15 := \text{address}$	BL label	N/A	N/A	
BNE	Branch if Not Equal	$R15 := \text{address if Z flag is clear}$	BNE label	N/A	Yes	Unravel the branch, then use controlled gates to conditionally run operations
BX	Branch and Exchange	$R15 := Rn, T \text{ bit := } Rn[0]$	Not translatable	N/A	N/A	
CDP	Coprocessor Data Processing	(Coprocessor-specific)	(Coprocessor-specific)	N/A	N/A	
CMN	Compare Negative	$\text{CPSR flags} := Rn + Op2$	CMN Rn, Operand2	Figure 5	Yes	
CMP	Compare	$\text{CPSR flags} := Rn - Op2$	CMP Rn, Operand2	Figure 6	Yes	
EOR	Exclusive OR	$Rd := (Rn \text{ AND NOT } Op2) \text{ OR } (Op2 \text{ AND NOT } Rn)$	EOR Rd, Rn, Operand2	Figure 7	Yes	
LDC	Load coprocessor from memory	Coprocessor load	(Coprocessor-specific)	N/A	N/A	
LDM	Load multiple registers	Stack manipulation (Pop)	LDM Rn, Rlist	N/A	No	
LDR	Load register from memory	$Rd := (\text{address})$	LDR Rd, [Rn, Offset]	Figure 8	No	
LSL	Logical Shift Left	$Rd := Rm \text{ LSL } \#imm$	LSL Rd, Rn, #shift	Figure 9	Yes	
LSR	Logical Shift Right	$Rd := Rm \text{ LSR } \#imm$	LSR Rd, Rn, #shift	Figure 10	Yes	
MCR	Move CPU register to coprocessor register	$cRn := rRn \mid op \& cRm$	(Coprocessor-specific)	N/A	N/A	
MLA	Multiply Accumulate	$Rd := (Rm * Rs) + Rn$	MLA Rd, Rm, Rs, Rn	Figure 11	Yes	

**Table 2:** Mapping of Assembly Instructions to Quantum Operations Continued

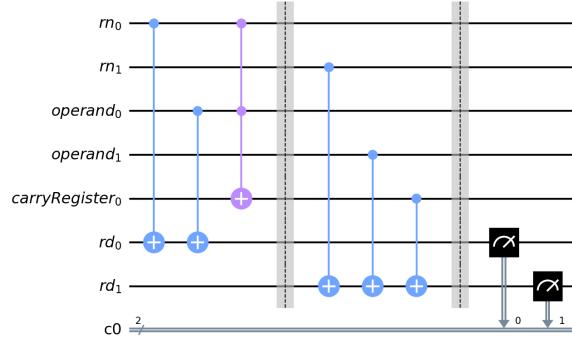
Mnemonic	Instruction	Classical		Quantum		
		Action	Example	Quantum Transformation	Coherence Maintaining?	Additional Notes
MOV	Move register or constant	Rd := Op2	MOV Rd, Operand2	Figure 13	Yes	
MRC	Move from coprocessor register to CPU register	Rn := cRn ; op;cRm	(Coprocessor-specific)	N/A	N/A	
MRS	Move PSR status flags to register	Rn := PSR	MRS Rd, CPSR	Figure 14	Yes	
MSR	Move register to PSR status flags	PSR := Rm	MSR CPSR, Rn	Figure 15	Yes	
MUL	Multiply	Rd := Rm * Rs	MUL Rd, Rm, Rs	Figure 12	Yes	
MVN	Move negative register	Rd := 0xFFFFFFFF EOR Op2	MVN Rd, Operand2	Figure 16	Yes	
ORR	OR	Rd := Rn OR Op2	ORR Rd, Rn, Operand2	Figure 17	Yes	
RSB	Reverse Subtract	Rd := Op2 - Rn	RSB Rd, Rn, Operand2	Figure 18	Yes	
RSC	Reverse Subtract with Carry	Rd := Op2 - Rn - 1 + Carry	RSC Rd, Rn, Operand2	Figure 19	Yes	
SBC	Subtract with Carry	Rd := Rn - Op2 - 1 + Carry	SBC Rd, Rn, Operand2	Figure 20	Yes	
STC	Store coprocessor register to memory	address := CRn	(Coprocessor-specific)	N/A	N/A	
STM	Store Multiple	Stack manipulation (Push)	STM Rn, Rlist	N/A	No	
STR	Store register to memory	[address] <sub>i</sub> := Rd	STR Rd, [Rn, Offset]	Figure 21	No	
SUB	Subtract	Rd := Rn - Op2	SUB Rd, Rn, Operand2	Figure 22	Yes	
SWI	Software Interrupt	OS call	SWI #immediate	N/A	N/A	
SWP	Swap register with memory	Rd := [Rn], [Rn] := Rm	SWP Rd, Rm, [Rn]	N/A	No	
TEQ	Test bitwise equality	CPSR flags := Rn EOR Op2	TEQ Rn, Operand2	Figure 23	Yes	
TST	Test bits	CPSR flags := Rn AND Op2	TST Rn, Operand2	Figure 24	Yes	

**ADC:** Figure 1 illustrates the mapping of the assembly-level ADC instruction to its quantum near-equivalent. The circuit consists of two input registers,  $rn$  and  $operand$ . A full or ripple-carry adder is employed to compute the sum, with the result stored in  $rd$ . The  $carryFlag$  is determined using an auxiliary  $carryRegister$ .



**Fig. 1:** ADC Quantum Equivalent Circuit: A full or ripple carry adder that also sets the Carry Flag.

**ADD:** Figure 2 depicts the mapping of the assembly ADD instruction to its quantum near-equivalent. The circuit utilizes two input registers,  $rn$  and  $operand$ , and employs a full or ripple-carry adder to compute the sum, which is stored in  $rd$ .

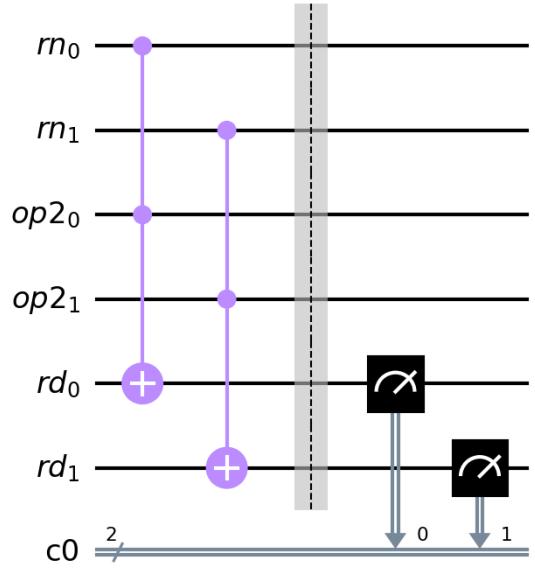


**Fig. 2:** ADD Quantum Equivalent Circuit: A full or ripple carry adder.

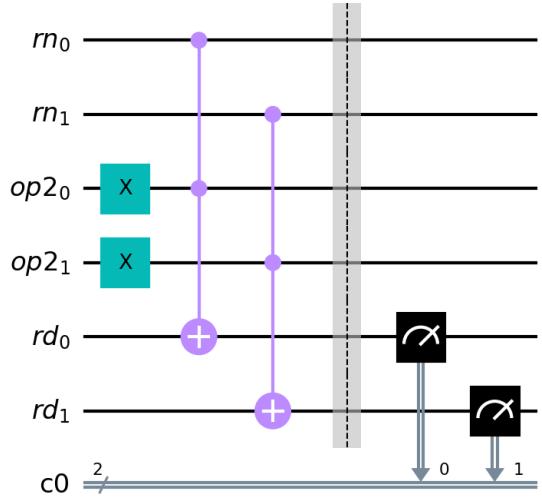
**AND:** Figure 3 illustrates the mapping of the assembly AND instruction to its quantum near-equivalent. The circuit features two input registers,  $rn$  and  $op2$ , and uses MCT gates to compute the AND operation, storing the result in  $rd$ .

**BIC:** Figure 4 depicts the mapping of the assembly BIC instruction to its quantum near-equivalent. The circuit includes two input registers,  $rn$  and  $op2$ , and implements the BIC operation on  $rd$  using a combination of X gates and MCT gates.

**CMN:** Figure 5 illustrates the mapping of the assembly CMN instruction to its quantum near-equivalent. The circuit uses two input registers,  $rn$  and  $op2$ , and employs a full or



**Fig. 3:** AND Quantum Equivalent Circuit: A Multiply-Controlled Toffoli gate is applied to each bit in the registers.



**Fig. 4:** BIC Quantum Equivalent Circuit: Op2 is inverted then a Multiply-Controlled Toffoli gate is applied to each bit in the registers.

ripple-carry adder to compute their sum. The *Carry* flag is set if the addition produces a carry, the *Zero* flag is determined by checking whether all result bits are zero, the *Negative* flag is set based on the most significant bit (MSB), and the *Overflow* flag is computed by XORing the MSBs of the input registers.

**CMP:** Figure 6 depicts the mapping of the assembly CMP instruction to its quantum near-equivalent. The circuit consists of two input registers,  $rn$  and  $op2$ , and uses a full or ripple-carry adder to perform the subtraction of  $op2$  from  $rn$ . The *Carry* flag is set if the operation generates a carry, the *Zero* flag is determined by checking whether all result bits are zero, the *Negative* flag is set based on the most significant bit (MSB), and the *Overflow* flag is computed by XORing the MSBs of the input registers.

**EOR:** Figure 7 illustrates the mapping of the assembly EOR instruction to its quantum near-equivalent. The circuit includes two input registers,  $rn$  and  $op2$ , and implements the bitwise XOR operation using a combination of X gates, MCT gates, and quantum OR gates.

**LDR:** Figure 8 depicts the mapping of the assembly LDR instruction to its quantum near-equivalent. The circuit uses a single input register,  $rn$ , and employs an initialization gate to assign a classically known value to the register. If applied improperly, this operation can lead to decoherence.

**LSL:** Figure 9 illustrates the mapping of the assembly LSL instruction to its quantum near-equivalent. The circuit utilizes a single input register,  $rn$ , transfers its bits to  $rd$ , and performs a left shift by a classically specified number of positions.

**LSR:** Figure 10 depicts the mapping of the assembly LSR instruction to its quantum near-equivalent. The circuit uses a single input register,  $rn$ , transfers its bits to  $rd$ , and performs a right shift by a classically specified number of positions.

**MLA:** Figure 11 illustrates the mapping of the assembly MLA instruction to its quantum near-equivalent. The circuit employs three input registers,  $rm$ ,  $rs$ , and  $rn$ . Boolean operations are used to compute each bit of the multiplication efficiently according to the logic  $R_0 \&= A_0 \wedge B_0$ ,  $R_1 \&= (A_0 \wedge B_1) + (A_1 \wedge B_0)$ ,  $R_2 \&= (A_1 \wedge B_1) + \text{Carry from } R_1$ ,  $R_3 \&= \text{Carry from } R_2$  implemented with CNOT and MCT gates. Following the multiplication, a ripple-carry adder is used to add the value of  $rn$  to the result in  $rd$ .

**MUL:** Figure 12 illustrates the mapping of the assembly MUL instruction to its quantum near-equivalent. The circuit uses two input registers,  $rm$  and  $rs$ , and employs Boolean operations to compute each bit of the multiplication efficiently according to the logic:  $R_0 \&= A_0 \wedge B_0$ ,  $R_1 \&= (A_0 \wedge B_1) + (A_1 \wedge B_0)$ ,  $R_2 \&= (A_1 \wedge B_1) + \text{Carry from } R_1$ ,  $R_3 \&= \text{Carry from } R_2$  using CNOT and MCT.

**MOV:** Figure 13 depicts the mapping of the assembly MOV instruction to its quantum near-equivalent. The circuit utilizes a single register,  $rd$ , and applies an initialization gate to assign it a classically known value. If applied improperly, this operation may cause decoherence.

**MRS:** Figure 14 illustrates the mapping of the assembly MRS instruction to its quantum near-equivalent. The circuit uses a single input register,  $rn$ , and transfers the bits from the PSR register to  $rn$  using CNOT gates.

**MSR:** Figure 15 depicts the mapping of the assembly MSR instruction to its quantum near-equivalent. The circuit uses a single input register,  $rn$ , and transfers its bits to the PSR register via CNOT gates.

**MVN:** Figure 16 illustrates the mapping of the assembly MVN instruction to its quantum near-equivalent. The circuit uses a single register,  $rd$ , and applies an initialization gate to assign it the classically known value in inverted form. If applied improperly, this operation may induce decoherence.

**ORR:** Figure 17 depicts the mapping of the assembly ORR instruction to its quantum near-equivalent. The circuit utilizes two input registers,  $rn$  and  $op2$ , and implements the bitwise OR operation using a combination of X and MCT gates.

**RSB:** Figure 18 illustrates the mapping of the assembly RSB instruction to its quantum near-equivalent. The circuit includes two input registers,  $rn$  and  $op2$ , and performs the operation by negating the value in  $rn$  and then adding it to  $op2$  using a combination of X, CNOT, and MCT gates.

**RSC:** Figure 19 illustrates the mapping of the assembly RSC instruction to its quantum near-equivalent. The circuit utilizes two input registers,  $rn$  and  $op2$ , and implements the operation by negating  $rn$ , adding it to  $op2$ , and then incorporating the carry flag minus one, using a combination of X, CNOT, and MCT gates.

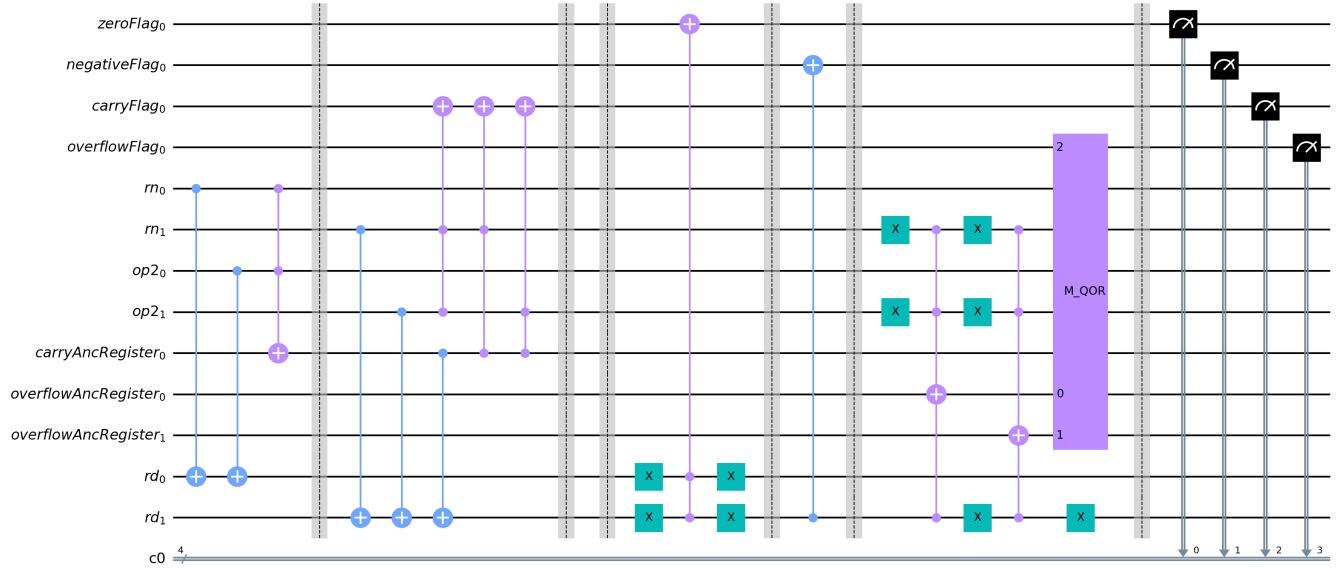
**SBC:** Figure 20 depicts the mapping of the assembly SBC instruction to its quantum near-equivalent. The circuit uses two input registers,  $rn$  and  $op2$ , and performs the operation by negating  $op2$ , adding it to  $rn$ , and then incorporating the carry flag minus one, using a combination of X, CNOT, and MCT gates.

**STR:** Figure 21 illustrates the mapping of the assembly STR instruction to its quantum near-equivalent. The circuit uses a single input register,  $rd$ , and applies a measurement gate to store its value classically. This operation inherently causes decoherence.

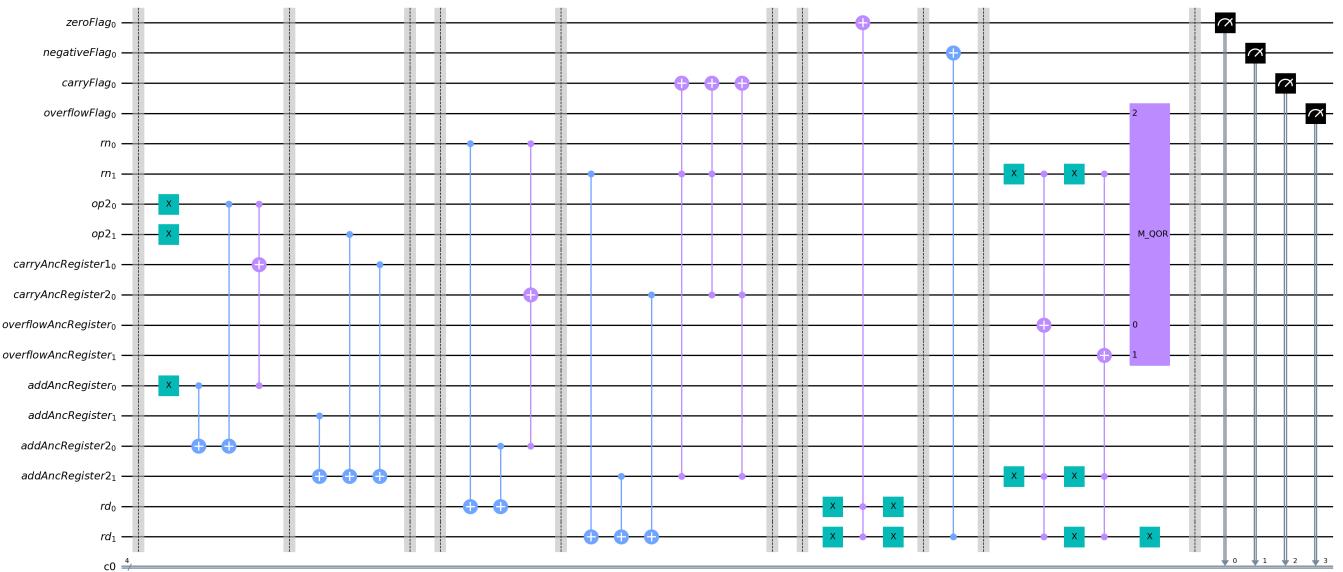
**SUB:** Figure 22 depicts the mapping of the assembly SUB instruction to its quantum near-equivalent. The circuit uses two input registers,  $rn$  and  $op2$ , and performs the subtraction by negating  $op2$  and adding it to  $rn$  using a combination of X, CNOT, and MCT gates.

**TEQ:** Figure 23 illustrates the mapping of the assembly TEQ instruction to its quantum near-equivalent. The circuit uses two input registers,  $rn$  and  $op2$ , and performs a bitwise exclusive OR between them. The *Carry* flag is set if the operation produces a carry, the *Zero* flag is determined by checking whether all result bits are zero, the *Negative* flag is set based on the most significant bit (MSB), and the *Overflow* flag is computed by XORing the MSBs of the input registers.

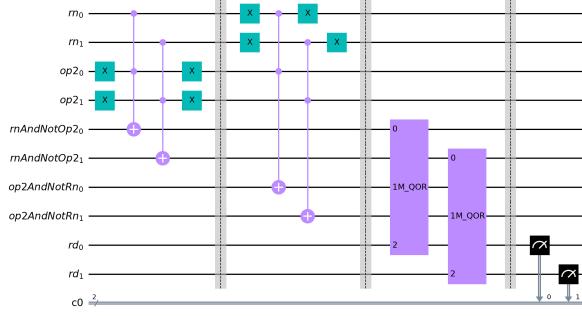
**TST:** Figure 24 illustrates the mapping of the assembly



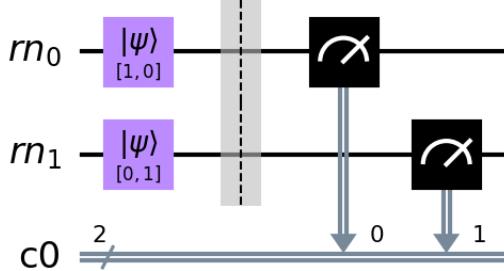
**Fig. 5:** CMN Quantum Equivalent Circuit: Adds Rn and Op2 then determine the values for the Zero, Negative, Carry, and Overflow flags.



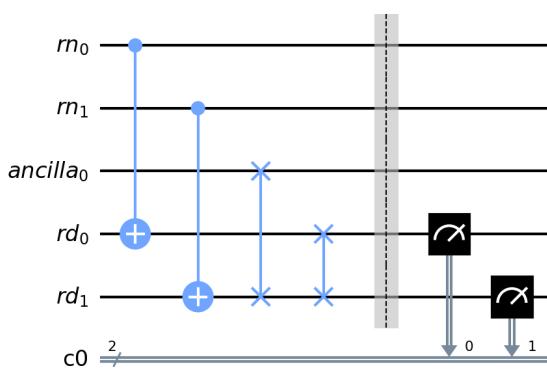
**Fig. 6:** CMP Quantum Equivalent Circuit: Subtracts Op2 from Rn then determine the values for the Zero, Negative, Carry, and Overflow flags.



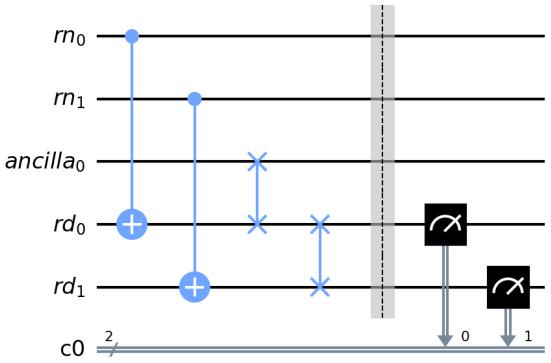
**Fig. 7:** EOR Quantum Equivalent Circuit: The logic  $(A \wedge \neg B) \vee (\neg A \wedge B)$  is implemented using X, Multiply-Controlled Toffoli, and Quantum OR gates.



**Fig. 8:** LDR Quantum Equivalent Circuit: Classically stores the value of the register.



**Fig. 9:** LSL Quantum Equivalent Circuit: Copies Rn to Rd then shifts using swap gates.



**Fig. 10:** LSR Quantum Equivalent Circuit: Copies Rn to Rd then shifts using swap gates.

TST instruction to its quantum near-equivalent. The circuit uses two input registers,  $rn$  and  $op2$ , and performs a bitwise AND between them. The *Carry* flag is set if the operation generates a carry, the *Zero* flag is determined by checking whether all result bits are zero, the *Negative* flag is based on the most significant bit (MSB), and the *Overflow* flag is computed by XORing the MSBs of the input registers.

### 3. EVALUATION: CALCULATING THE FIBONACCI SEQUENCE

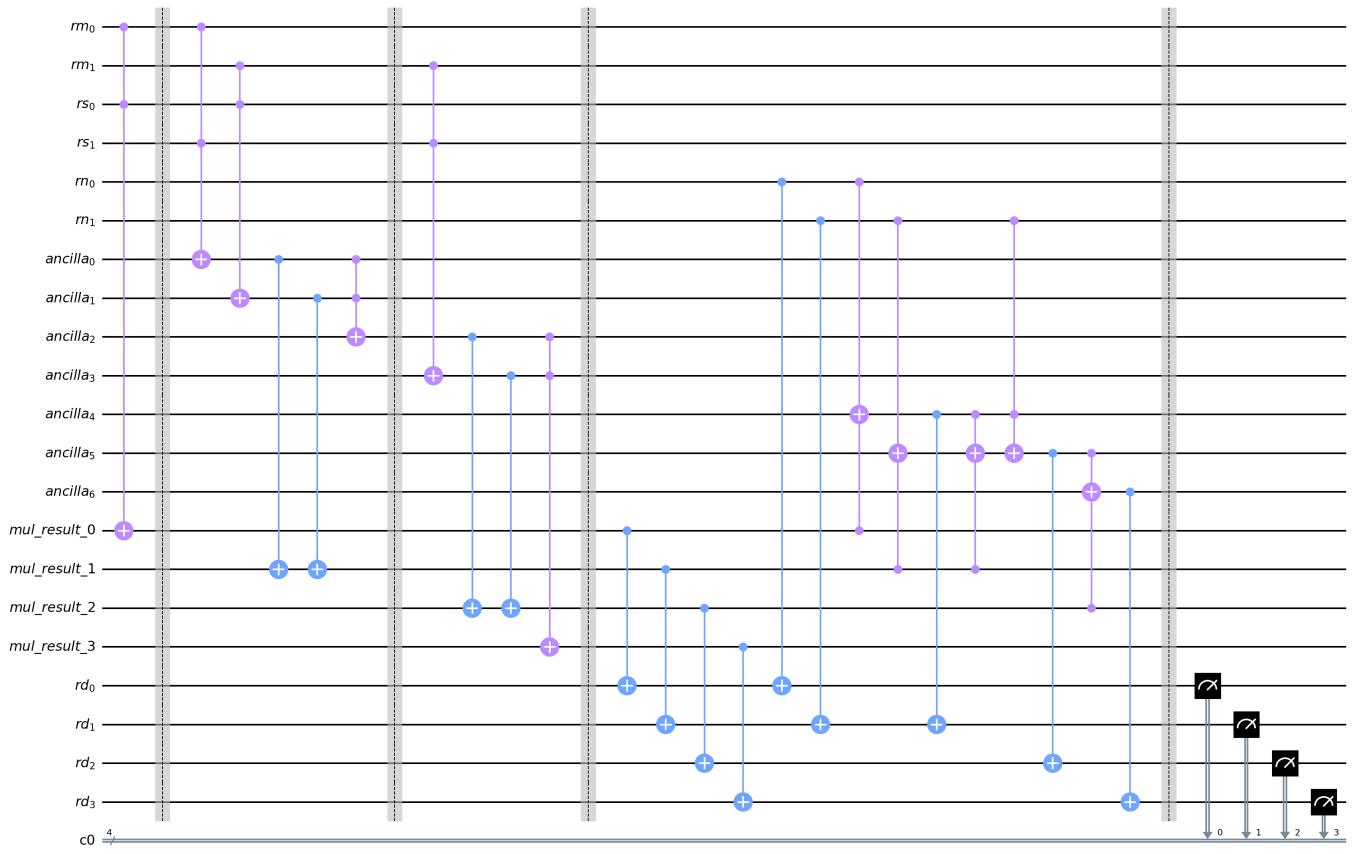
With a significant number of assembly instructions now mapped to their quantum equivalents, we can demonstrate their practical utility. One non-trivial example is computing the Fibonacci sequence. The first five Fibonacci numbers are 0, 1, 1, 2, 3 [7]. The following presents an assembly program for calculating the first  $N$  Fibonacci numbers.

```

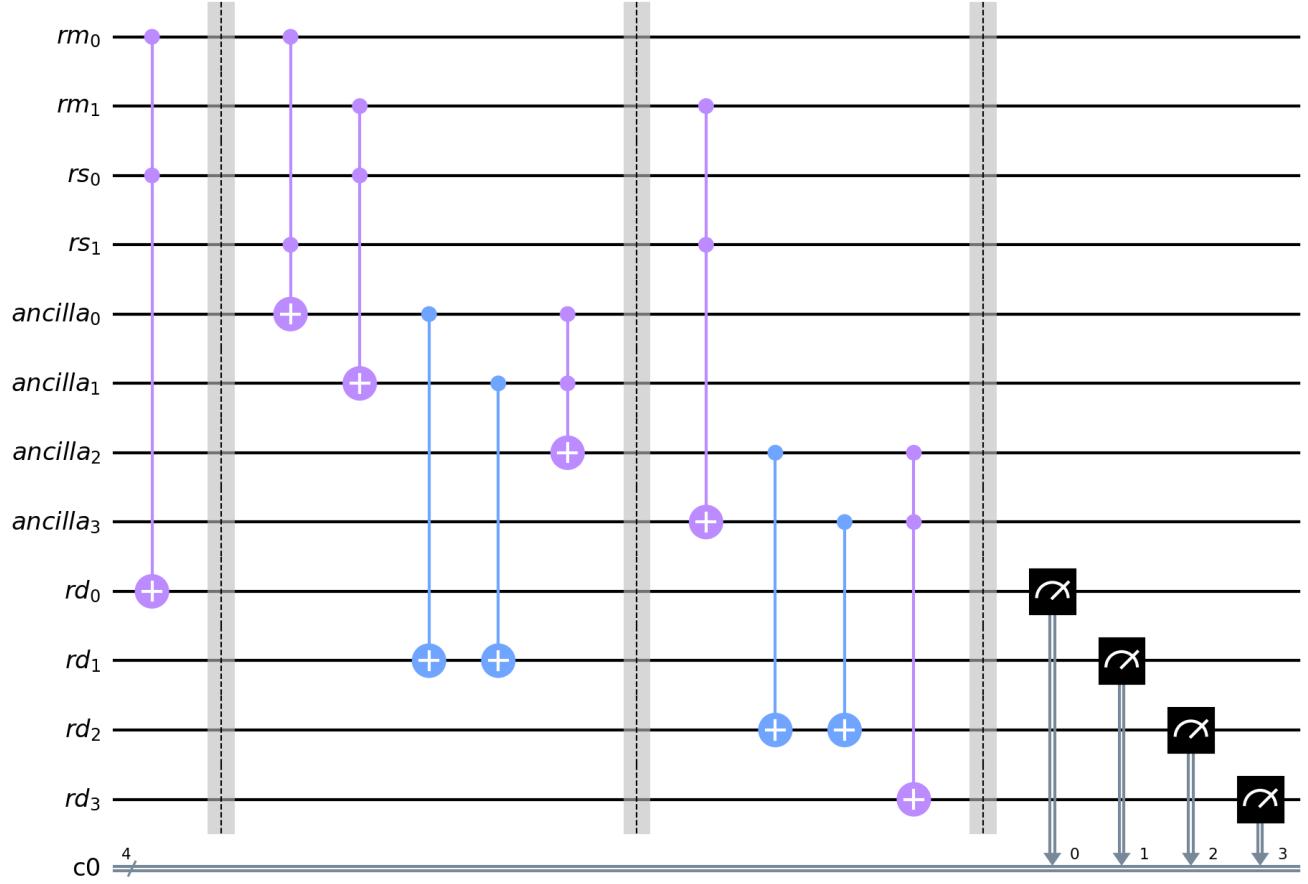
1  MOV R1, #0          ; Initialize R1 with 0, F(0)
2  MOV R2, #1          ; Initialize R2 with 1, F(1)
3  MOV R3, #N           ; R3 holds the value of N,
                       ; the number of Fibonacci numbers to generate
4  MOV R4, #1           ; Initialize loop counter R4
                       ; with 1

5
6 FIB_LOOP:
7   CMP R4, R3         ; Compare loop counter with
8   BGE FIB_DONE        ; If counter >= N, finish
9
10 ADD R5, R1, R2       ; R5 = R1 + R2, calculate
                           ; the next Fibonacci number
11 MOV R1, R2           ; Update R1 to the next
                           ; Fibonacci number
12 MOV R2, R5           ; Update R2 to the new next
                           ; Fibonacci number
13
14 ADD R4, R4, #1       ; Increment the counter
15 B FIB_LOOP          ; Repeat the loop
16
17 FIB_DONE:

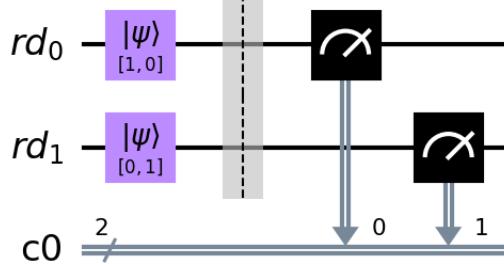
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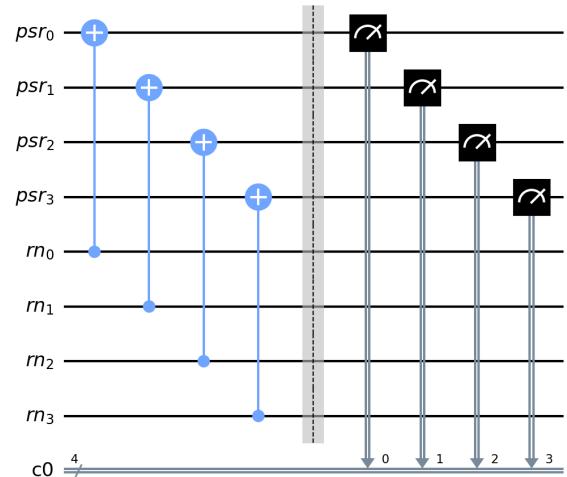
**Fig. 11:** MLA Quantum Equivalent Circuit: The logic for multiplication is  $R_0 \&= A_0 \wedge B_0$ ,  $R_1 \&= (A_0 \wedge B_1) + (A_1 \wedge B_0)$ ,  $R_2 \&= (A_1 \wedge B_1) + \text{Carry from } R_1$ ,  $R_3 \&= \text{Carry from } R_2$  then adds  $R_n$  using a ripple carry adder.



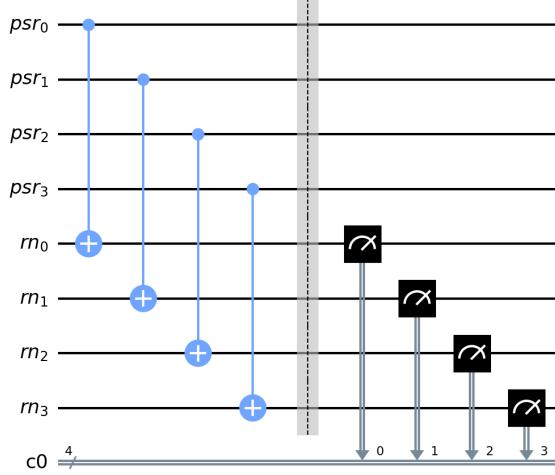
**Fig. 12:** MUL Quantum Equivalent Circuit: The logic for multiplication is  $R_0 \&= A_0 \wedge B_0$ ,  $R_1 \&= (A_0 \wedge B_1) + (A_1 \wedge B_0)$ ,  $R_2 \&= (A_1 \wedge B_1) + \text{Carry from } R_1$ ,  $R_3 \&= \text{Carry from } R_2$



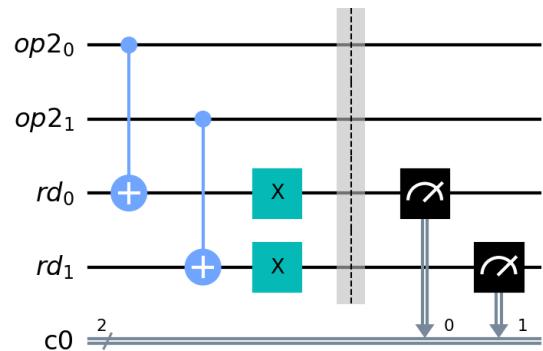
**Fig. 13:** MOV Quantum Equivalent Circuit: Assigns values to Rd.



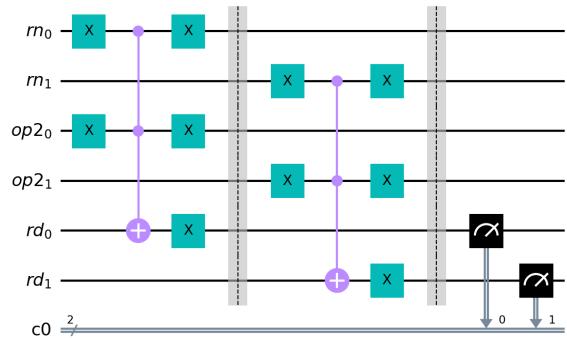
**Fig. 15:** MSR Quantum Equivalent Circuit: Moves the value of the Rn register to the PSR register using controlled-not gates.



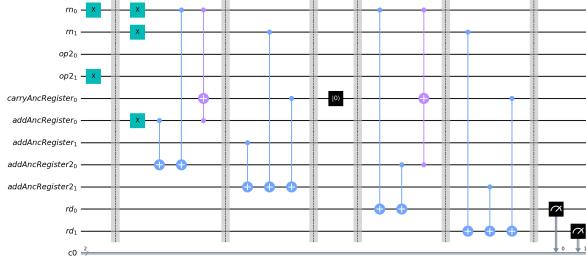
**Fig. 14:** MRS Quantum Equivalent Circuit: Moves the value of the PSR register to the Rn register using controlled-not gates.



**Fig. 16:** MVN Quantum Equivalent Circuit: Moves the inverted value from Op2 to Rd using controlled-not and X gates.



**Fig. 17:** ORR Quantum Equivalent Circuit: Bitwise  $Rd = Rn \vee Op2$  using X and Multiply-Controlled Toffoli gates.



**Fig. 18:** RSB Quantum Equivalent Circuit:  $Rd = Op2 - Rn$  using X, controlled-not, multiply-controlled Toffoli, and reset gates.

```

18 ; At this point, R1 contains the last
19   Fibonacci number generated
20 ; The program ends here
21 NOP           ; No Operation (End of
                  program)

```

Next, we transform the program into a form that can be directly mapped to a quantum circuit. Several modifications are required:

1. Unravel the loop, eliminating the counter, labels, and branch instructions.
2. Remove all NOP instructions.
3. Due to qubit limitations, compute only up to the fifth Fibonacci number.

The assembly program below incorporates these adjustments.

```

1 MOV R1, #0      ; Initialize R1 with 0, F(0)
2 MOV R2, #1      ; Initialize R2 with 1, F(1)
3
4 ; calculate F(2)
5 ADD R3, R1, R2 ; R3 = R1 + R2, calculate
                  the next Fibonacci number
6 MOV R1, R2      ; Update R1 to the next
                  Fibonacci number
7 MOV R2, R3      ; Update R2 to the new next
                  Fibonacci number
8
9 ; calculate F(3)
10 ADD R3, R1, R2 ; R3 = R1 + R2, calculate
                  the next Fibonacci number
11 MOV R1, R2      ; Update R1 to the next
                  Fibonacci number
12 MOV R2, R3      ; Update R2 to the new next
                  Fibonacci number
13
14 ; calculate F(4)
15 ADD R3, R1, R2 ; R3 = R1 + R2, calculate
                  the next Fibonacci number
16 MOV R1, R2      ; Update R1 to the next
                  Fibonacci number
17 MOV R2, R3      ; Update R2 to the new next
                  Fibonacci number

```

The corresponding quantum circuit is presented in Figure 25, with its simulation results displayed in Figure 27. The results confirm that the quantum circuit accurately computes the fifth Fibonacci number (3) using a coherence-breaking approach.

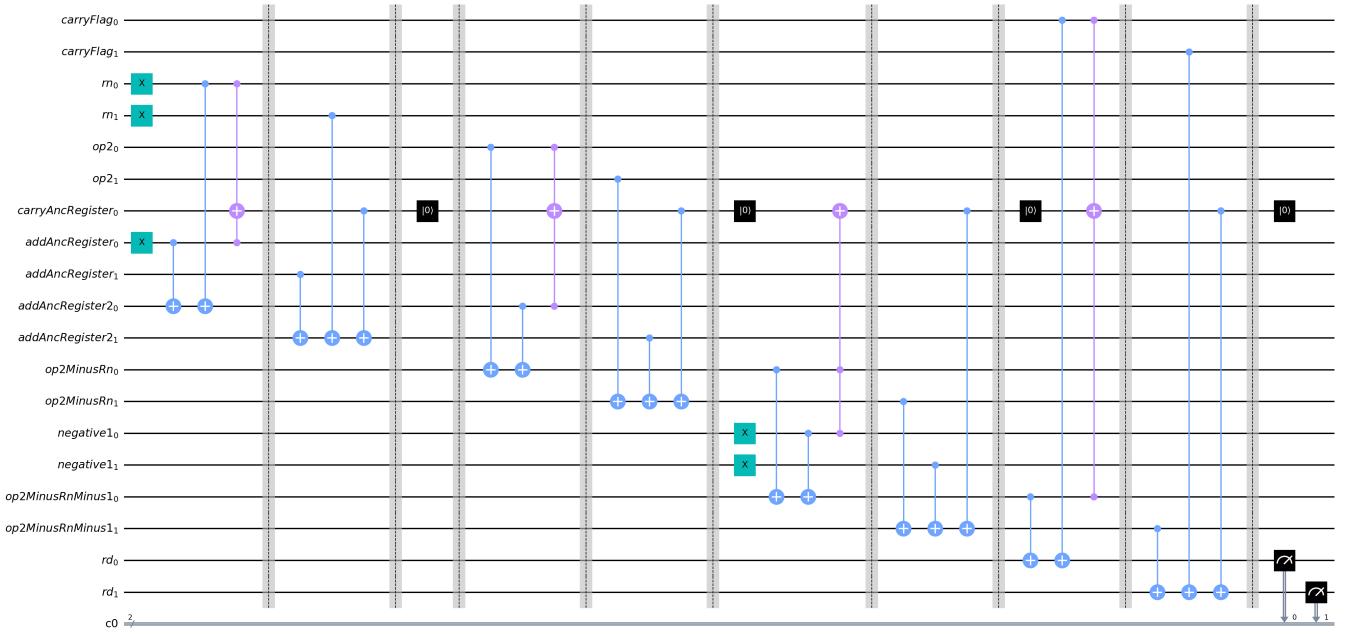
Reset gates disrupt coherence, which may be undesirable. To preserve coherence while calculating the Fibonacci sequence, the assembly program can be modified to avoid using reset gates and to ensure that qubits are not reused during computation. These modifications are incorporated in the following program:

```

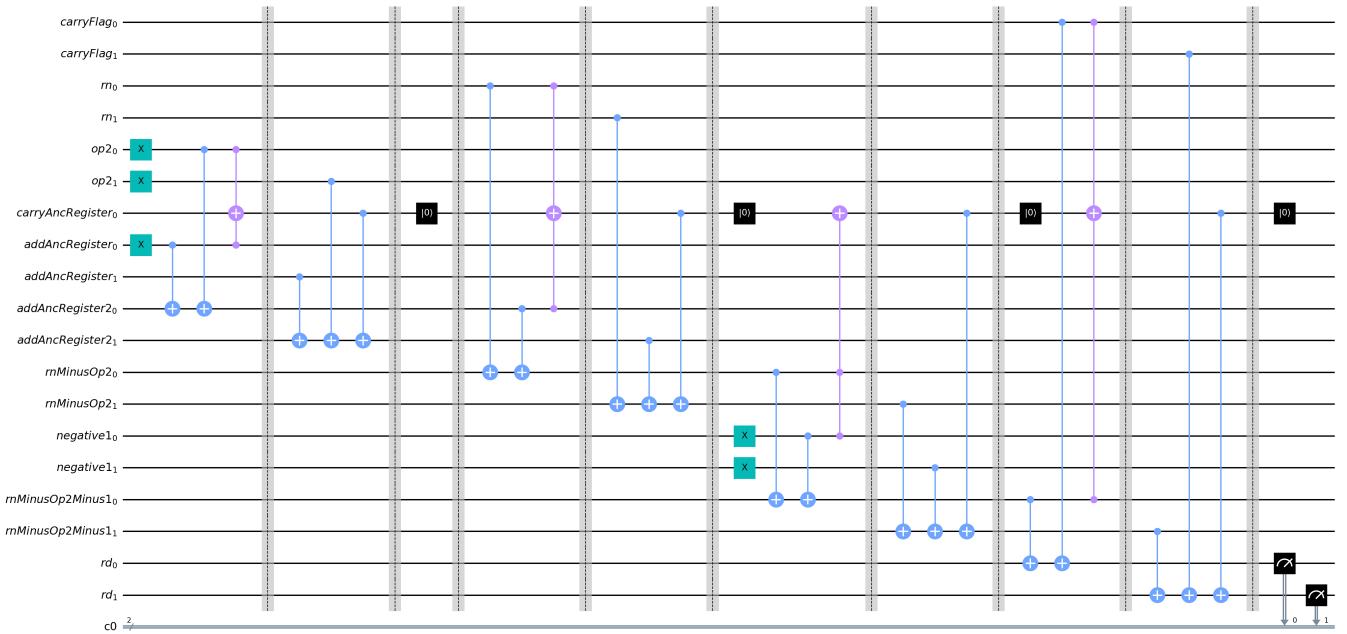
1 MOV R1, #0      ; Initialize R1 with 0, F(0)
2 MOV R2, #1      ; Initialize R2 with 1, F(1)
3
4 ; calculate F(2)
5 ADD R3, R1, R2 ; R3 = R1 + R2, calculate the
                  next Fibonacci number (F(2))
6
7 ; calculate F(3)
8 ADD R4, R2, R3 ; R4 = R2 + R3, calculate the
                  next Fibonacci number (F(3))
9
10 ; calculate F(4)
11 ADD R5, R3, R4 ; R5 = R3 + R4, calculate the
                  next Fibonacci number (F(4))

```

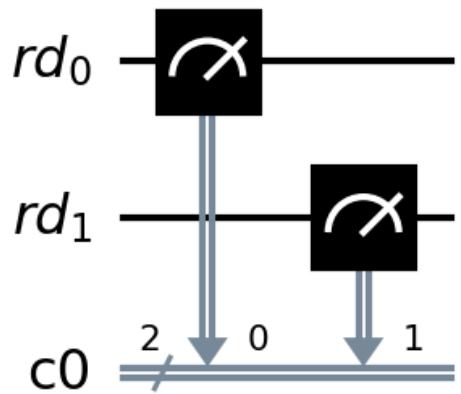
Figure 26 shows the coherence maintaining circuit and Figure 28 shows the simulation results.



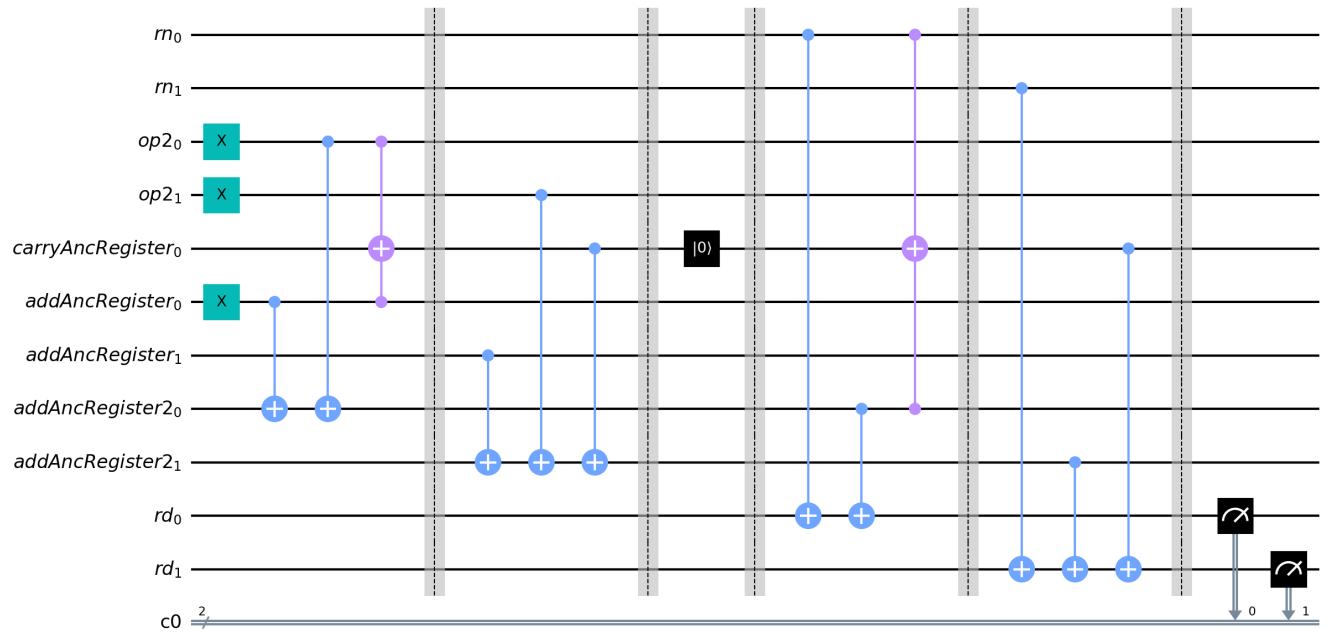
**Fig. 19:** RSC Quantum Equivalent Circuit:  $Rd := Op2 - Rn + Carry - 1$  using X, controlled-not, multiply-controlled Toffoli, and reset gates.



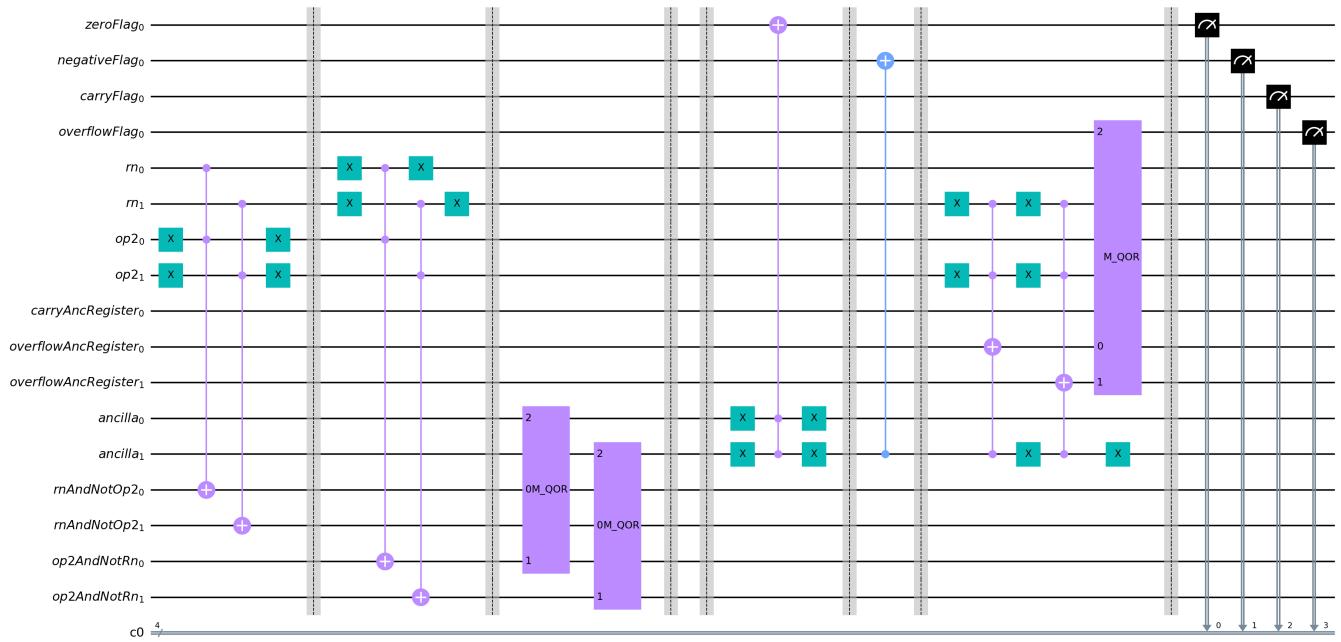
**Fig. 20:** SBC Quantum Equivalent Circuit:  $Rd := Rn - Op2 - 1 - Carry$  using X, controlled-not, multiply-controlled Toffoli, and reset gates.



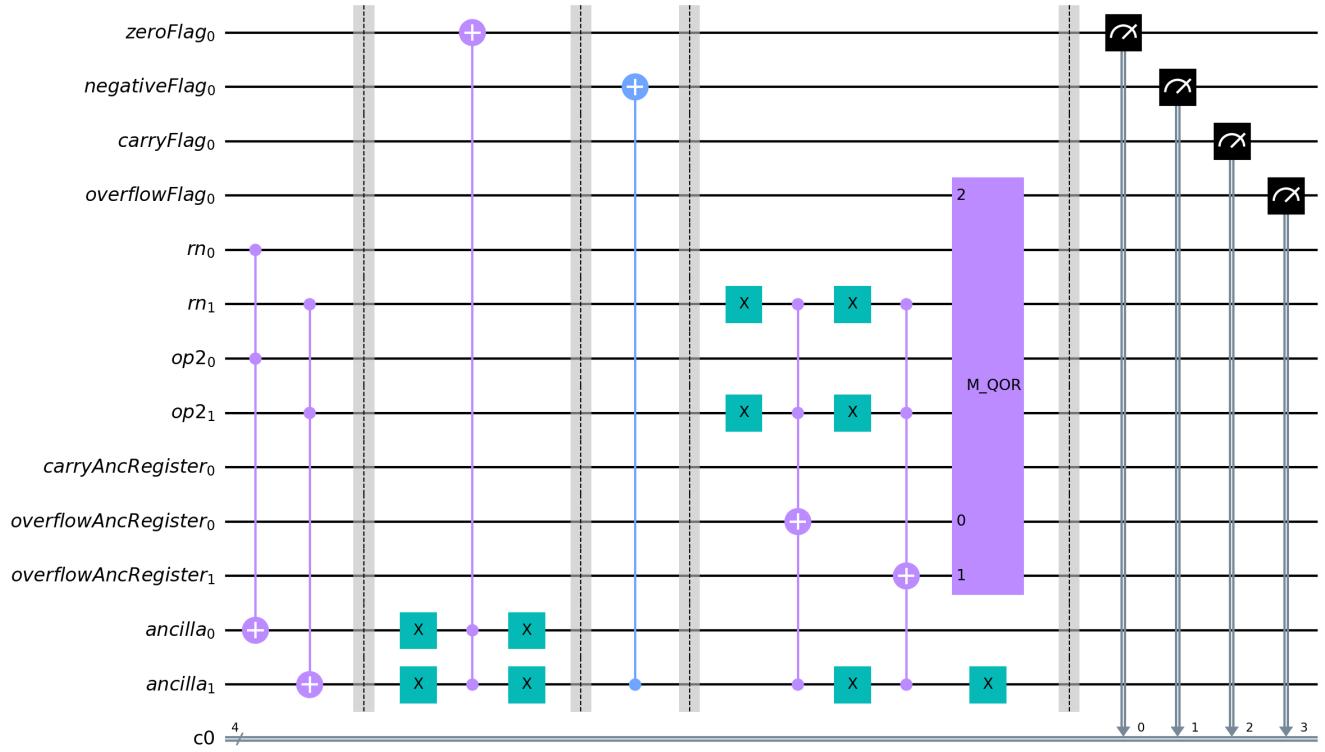
**Fig. 21:** STR Quantum Equivalent Circuit: Classically stores a quantum register.



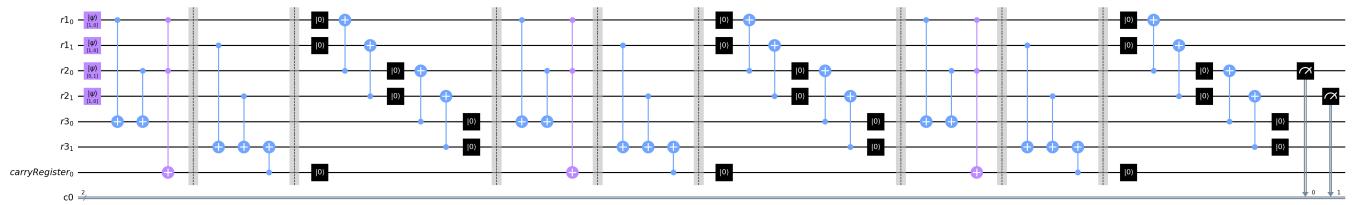
**Fig. 22:** SUB Quantum Equivalent Circuit:  $Rd := Rn - Op2$  using X, controlled-not, multiply-controlled Toffoli, and reset gates.



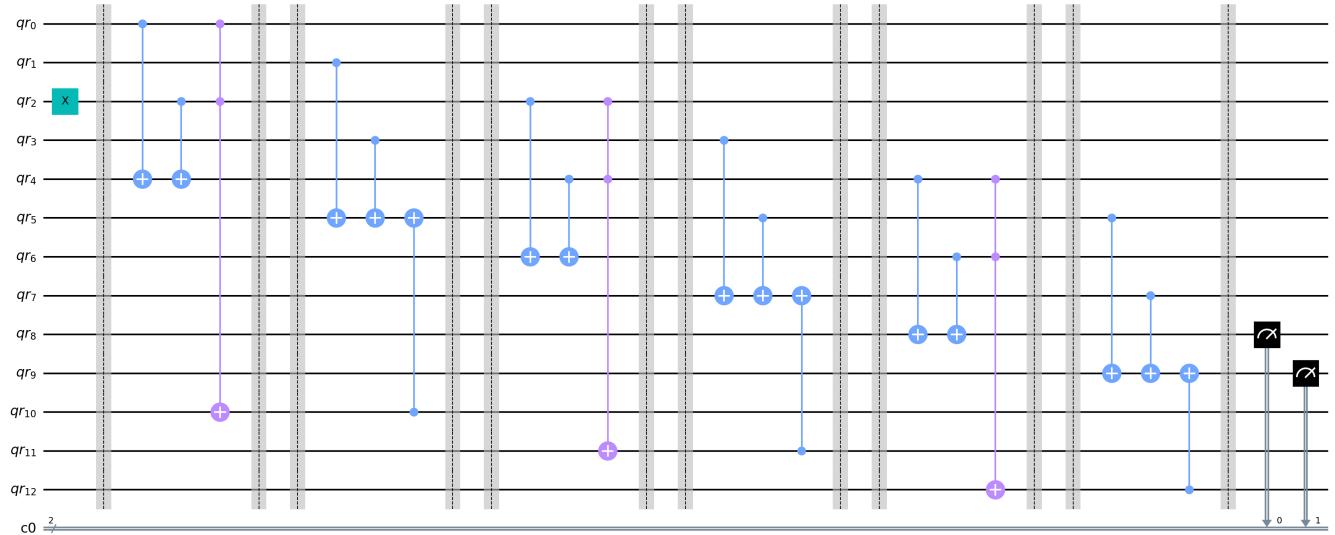
**Fig. 23:** TEQ Quantum Equivalent Circuit: Performs a bitwise exclusive OR on  $Rn$  and  $Op2$ , then assigns the Zero, Negative, Carry, and Overflow flags accordingly using X, controlled-not, and MCT gates.



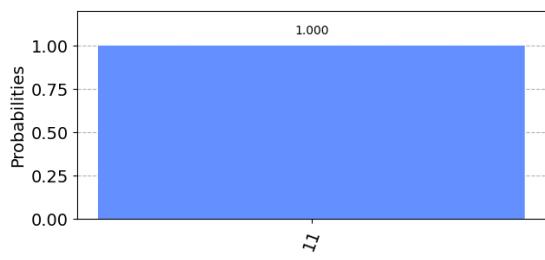
**Fig. 24:** TST Quantum Equivalent Circuit: Performs a bitwise AND on Rn and Op2, then assigns the Zero, Negative, Carry, and Overflow flags accordingly using X, controlled-not, and MCT gates.



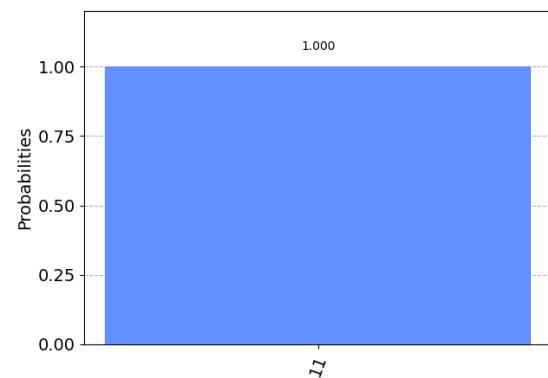
**Fig. 25:** Fibonacci Coherence Breaking Quantum Equivalent Circuit



**Fig. 26:** Fibonacci Coherence Maintaining Quantum Equivalent Circuit



**Fig. 27:** Fibonacci Coherence Breaking Quantum Equivalent Circuit Simulation Results



**Fig. 28:** Fibonacci Coherence Maintaining Quantum Equivalent Circuit Simulation Results

#### 4. GROVER'S ALGORITHM IMPLEMENTATION

Although the mapping of assembly instructions to quantum operations is useful for constructing Grover's Algorithm oracles, Grover's Algorithm also requires additional operations. To address these needs, new quantum operations were implemented. Table 3 lists these added operations.

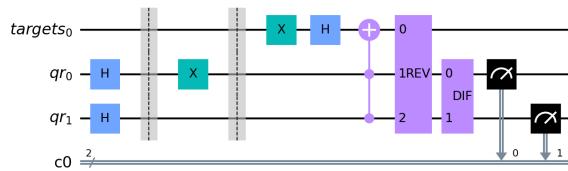
Additionally, the oracle begins with the instruction “ORACLE,” ends with “END\_ORACLE,” and the reverse of the first half of the oracle is applied using “REVERSE\_ORACLE.”

These operations can now be used to implement Grover's Algorithm. The following code generates the circuit shown in Figure 29, with its simulation results displayed in Figure 30. The results demonstrate that Grover's Algorithm can be executed successfully using only these assembly-to-quantum transformations.

```

1 {"register_size": 2}
2 ;hadamard
3 HAD R1
4 BAR
5 ORACLE
6   MOV R1, #1
7 END_ORACLE
8 BAR
9 ;applies all bits from R1 to the target using a
   Multiply-Controlled Toffoli Gate
10 MCT R1
11 REVERSE_ORACLE
12 ;diffuser
13 DIF {R1}
14 STR CR1, R1

```

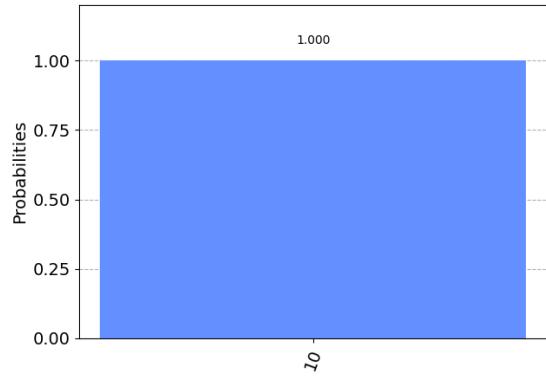


**Fig. 29:** Simple Grover's Algorithm Circuit

#### 5. OPEN SOURCE PROJECT

This compiler is open-source and available under the MIT License at  
<https://github.com/arhaverly/AssemblyToQuantumCompiler>.

The compiler takes a simplified ARM assembly file as input and generates the corresponding quantum circuit. Parameters can be configured via a JSON block at the beginning of the file, with currently supported options including register size, decoding, execution, and display settings. Example files are included in the repository.



**Fig. 30:** Simple Grover's Algorithm Circuit Simulation Results

#### 6. CONCLUSION

This study achieved the transformation of ARM assembly instructions into a quantum computing format, focusing on their application in quantum algorithms. The main accomplishment was mapping ARM instructions to quantum operations. The Fibonacci sequence computation, simulated using these quantum mappings, served as a practical demonstration of this approach. This simulation not only proved the technical feasibility but also highlighted the potential for applying classical programming techniques in quantum computing. Additionally, Grover's Algorithm was implemented using quantum-specific commands. The results are particularly relevant for simplifying algorithms like Grover's in quantum environments. These transformations were implemented to make an open-source assembly to quantum compiler: [github.com/arhaverly/AssemblyToQuantumCompiler](https://github.com/arhaverly/AssemblyToQuantumCompiler). This research contributes to integrating classical and quantum computing, paving the way for further explorations in this area.

#### 7. ACKNOWLEDGEMENTS

Portions of this work were previously included in the first author's doctoral dissertation at Mississippi State University, 2025.

#### 8. REFERENCES

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**Table 3:** Quantum-Specific Operations

Mnemonic	Instruction	Action	Example	Coherence Maintaining?
HAD	Apply Hadamard gates	$Rd :=  +\rangle$	HAD Rd	Yes
XXX	Apply Pauli X gates	$Rd := qc.x(Rd)$	XXX Rd	Yes
TGT	Apply CNot gate from flag or $Rd[0]$ to target	$qc.cx(Rd[0], \text{target})$	TGT Rd	Yes
DIF	Apply Diffuser	Diffuser applied to RList	DIF RList	Yes
BAR	N/A	Create barrier in circuit diagram	BAR	N/A

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