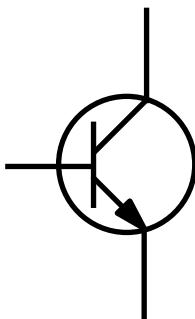


# PRIMER | SEMICONDUCTOR INDUSTRY

An overview of the global chip market, from design architecture to powering AI.

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AKHIL KATAKAM

# INDUSTRY OVERVIEW

## WHAT IS A SEMICONDUCTOR?

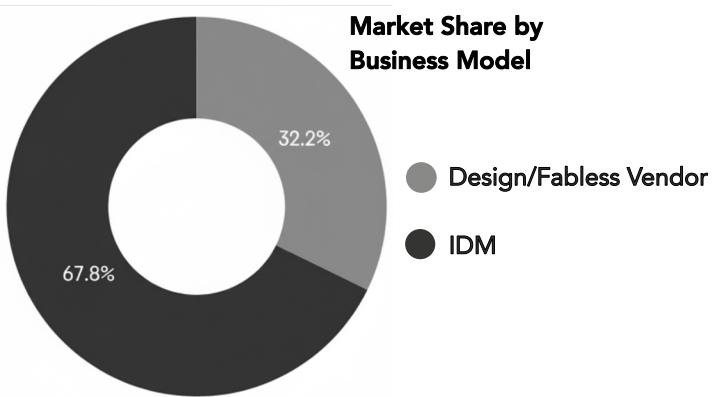
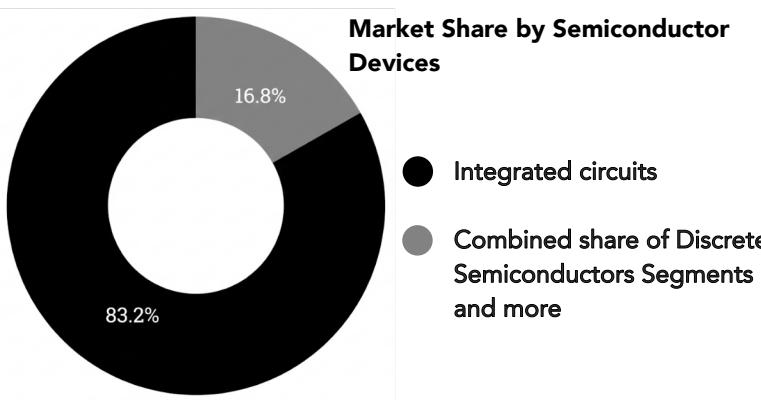
Semiconductors are materials (primarily silicon) that partially conduct electricity, enabling chips to process, store, and transmit data in electronic systems.

They perform three core functions:

**LOGIC:** Compute/control (CPUs, GPUs, MCUs)

**MEMORY:** Store data (DRAM, NAND flash)

**ANALOG:** Interface with real world (sensors, power)



## TIMELINE OVER THE YEARS

**1947**

**Transistor invented:** Bell Labs invents the transistor, replacing bulky vacuum tubes and launching modern semiconductor electronics.

**1958**

**Integrated circuit (IC):** Kilby (TI) and Noyce (Fairchild) independently create the IC, putting multiple transistors on a single chip.

**1971**

**First commercial microprocessor (Intel 4004):** A full CPU on one chip powers calculators and starts the microprocessor era.

**1980s**

**PCs and DRAM boom:** Personal computers and commodity DRAM drive rapid growth and shift the industry toward mass-market computing.

**1990s**

**Mobile & fabless-foundry model:** Cell phones, game consoles, and the rise of TSMC's pure-play foundry model reshape the value chain.

**2000s**

**Smartphones & broadband:** Convergence of phone, camera, and internet into smartphones massively scales demand for SoCs and mobile memory.

**2010s**

**Cloud, AI, and FinFET:** Cloud data centers, GPUs for AI, and FinFET transistors at advanced nodes push performance and power efficiency.

**2020s**

**5G, chip shortages, geopolitics:** 5G, EVs, and AI surge demand; US-China tensions make semiconductors a strategic priority globally.

DRIVER and IMPACT TIMELINE(yrs)	(~) % IMPACT ON CAGR	GEOGRAPHIC RELEVANCE
Explosive data-center demand for AI accelerators (2-4)	+1.8%	North America, China, Western Europe
Ubiquitous edge-AI in consumer IoT devices(2-4)	+1.2%	North America, Western Europe, East Asia
Automotive zonal-architecture migration(>4)	+0.9%	Europe, North America, China, Japan
Incentives across the US, EU, India, MENA(2-4)	+0.7%	North America, Europe, India, North Africa
Heterogeneous integration cost-down inflection(2-4)	+0.5%	Advanced manufacturing hubs
Chiplet marketplace commercialization (UCle/IP) (>4)	+0.4%	North America, East Asia

## DRIVERS

## IMPACT

## INDUSTRY STRUCTURE



**Fabless:** Focus only on chip design (examples – NVIDIA, Qualcomm).  
No fabs, lighter capex, high margins.



**Foundry:** Manufacture chips for others (TSMC, Samsung Foundry).  
Extremely capex-intensive, scale gives edge.



**IDM (Integrated Device Manufacturer):** Do both design and manufacturing in-house (Intel, TI, Infineon).  
Enables control but limits flexibility.



**OSAT (Outsourced Assembly and Test):** Handle packaging, assembly, final testing (ASE, Amkor, JCET).  
Mostly based in Asia, low margins but massive volumes.



**Equipment & EDA:** Companies making chip-making tools (ASML, Applied Materials)  
or design software (Synopsys, Cadence). High entry barriers;  
these players quietly power the ecosystem.

## Semiconductor Industry CAGR, Growth rate by region 2025-2030



By 2030, the semiconductor landscape will be defined by **Asia-Pacific's** continued 81.3% dominance (led by Taiwan's 3nm/5nm leadership and South Korean memory), **North America's** \$540B domestic manufacturing resurgence under the CHIPS Act, and **Europe's** push for 20% global share via automotive and power-chip niches. Meanwhile, **India** and other emerging hubs are aggressively funding local ecosystems to pivot from importers to specialty manufacturers.

### POLITICAL



Trump tariffs + Biden export controls tighten on China (Dec 2024 rules); South Korea martial law exposes Asia concentration risk. 10+ global "chips acts" drive friendshoring.

### ECONOMIC



Global GDP growth moderating (2025 forecasts); chip sales hit \$772B (+22.5%). Capex supercycle continues but tariffs raise costs 25%+ for China-sourced goods.

### PESTEL ANALYSIS

#### SOCIAL



AI/data center boom + EV adoption deepen societal chip dependence. Talent shortage worsens; India/US STEM programs ramp up. Smart devices/IoT hit 181ZB data by 2025.

#### TECH



2nm pilots (Rapidus), GaN/SiC power surge, AI/HPC drive HBM demand. Besi/assembly equipment adapts to chiplets/heterogeneous integration.

#### ENVIRONMENTAL



Climate risks top Europe/Asia concerns; fabs face water/energy scrutiny. EU pushes sustainable manufacturing amid \$233B cloud spend.

#### LEGAL



US export rules expand to metrology/inspection tools (Dec 2024). India political donation scrutiny on Tata/Murugappa chip projects. Antitrust hits consolidation.

## KEY TERMS

• **Node/Nanometer (nm):** Chip feature size. Smaller = more transistors, faster chips. 3nm → 20B+ transistors vs 28nm → 1B transistors

• **Moore's Law:** Transistor density doubles every ~2 years (slowing since 2010s)

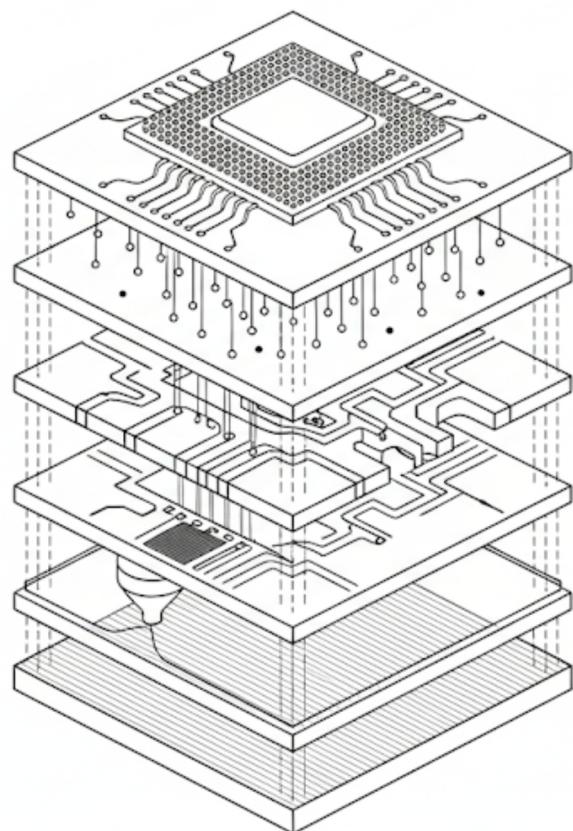
• **Capex:** Capital expenditure – money spent on factories/equipment. Advanced fabs cost \$20B+ each

• **HBM:** High Bandwidth Memory – fast memory for AI/GPUs (Samsung, SK Hynix)

• **EUV:** Extreme Ultraviolet lithography – enables 5nm/3nm nodes (ASML monopoly)

• **Chiplet:** Modular chip design – multiple small dies in one package (AMD, Intel)

## HOW SEMICONDUCTORS ARE MADE



INSTRUCTION SET ARCHITECTURE | CHIP DESIGN | FABRICATION  
EQUIPMENT AND SOFTWARE | PACKAGING AND TESTING

# 1\*INSTRUCTION SET ARCHITECTURE

## OVERVIEW

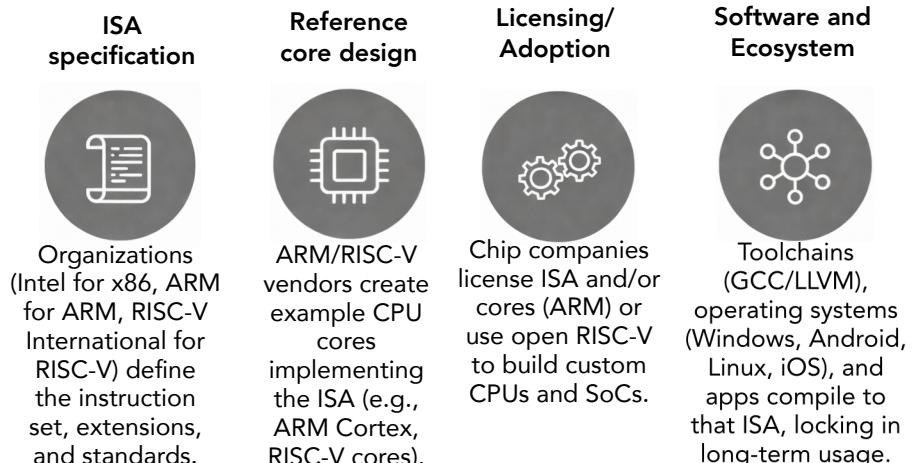
The Instruction Set Architecture (ISA) defines the set of machine instructions that software can use and how they are encoded. It is the contract between software (compilers, OS, apps) and hardware (CPUs/SoCs), specifying registers, instruction formats, addressing modes, and behavior.

**Strategic Role:** ISAs shape entire ecosystems — which operating systems run, which compilers exist, and how easy it is for developers to target a platform. Control over an ISA (x86, ARM) gives leverage over who can design compatible chips and where they can be used.

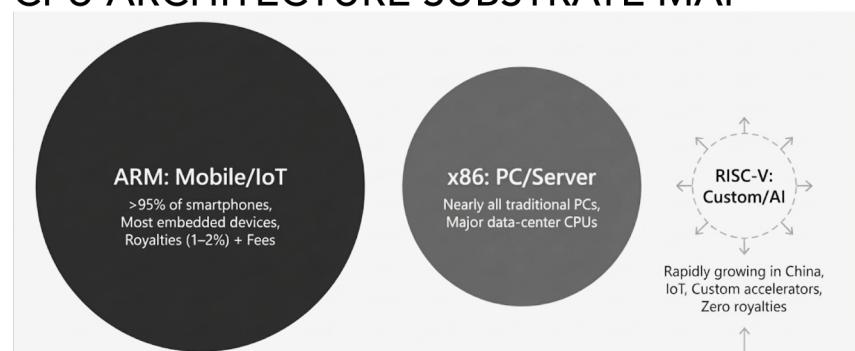
## KEY/TOP PLAYERS



## VALUE CHAIN FLOW



## CPU ARCHITECTURE SUBSTRATE MAP



## GROWTH DRIVERS AND IMPORTANCE

**Node scaling & complexity:** Transition to 3nm, 2nm, and beyond requires new generations of EUV, high-NA tools, advanced deposition/etch, and more sophisticated EDA flows.

**Chiplets & advanced packaging:** Heterogeneous integration and 3D stacking demand new design tools (for system-level planning) and packaging equipment.

**Process control & yield:** As dimensions shrink, defect density and variability control become critical, pushing demand for inspection and metrology tools.

## CHALLENGES

**Export controls & geopolitics:** Restrictions on selling advanced equipment (especially EUV and some DUV/inspection tools) to China limit market access and complicate supply chains.

**Long qualification cycles:** New tools must be co-developed and qualified with leading foundries, taking years before full production deployment and revenue ramp.

**Customer concentration:** A handful of mega-customers (TSMC, Samsung, Intel, SK Hynix, Micron) dominate demand, increasing bargaining power and cyclical exposure.

# 2\*CHIP

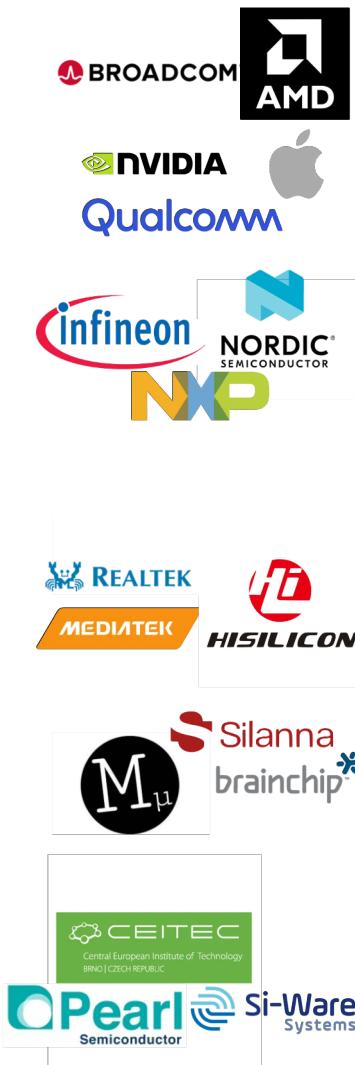
# DESIGN

## OVERVIEW

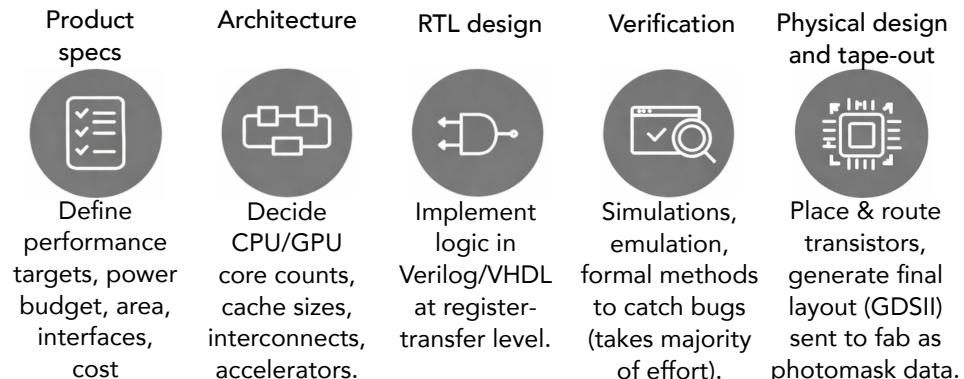
Chip design converts product requirements (performance, power, cost, features) into a detailed circuit description and physical layout that can be manufactured in a fab. It is done by fabless companies (NVIDIA, Qualcomm) and IDMs (Intel, TI) using specialized EDA software.

**Strategic Role:** Design quality, architecture choices, and time-to-market determine how competitive a chip is versus peers, making this one of the highest value-adding parts of the semiconductor stack.

## KEY/TOP PLAYERS



## VALUE CHAIN FLOW



## KEY NUMBERS

	Design cycle: <b>2–3 years</b> for a leading-edge chip
	Project cost: <b>USD 100M–500M</b> at 5nm and below
	Effort split: <b>60–70%</b> time in verification & validation
	Team size: <b>100–500+ engineers</b> for a flagship SoC or GPU

## GROWTH DRIVERS AND IMPORTANCE

**AI & custom accelerators:** Hyperscalers and car OEMs design in-house chips (TPUs, FSD, custom NPUs) to optimize performance per watt and reduce dependence on off-the-shelf parts.

**Heterogeneous SoCs:** Integration of CPU, GPU, NPU, modem, and power management on a single die increases design complexity and value capture for top design houses.

**Foundry partnerships:** Tight co-optimization between design firms and foundries (TSMC, Samsung) enables better performance and yield at advanced nodes

## CHALLENGES

**Rising complexity:** 3nm and below means tens of billions of transistors; verifying all corner cases and timing scenarios is extremely hard and error-prone.

**Soaring costs:** Each new node adds tens to hundreds of millions of dollars in design and mask costs, making only a few players able to afford true leading-edge designs.

**Talent bottlenecks:** Shortage of skilled RTL, verification, and physical design engineers slows schedules and increases salary pressure, especially in AI and automotive chips.

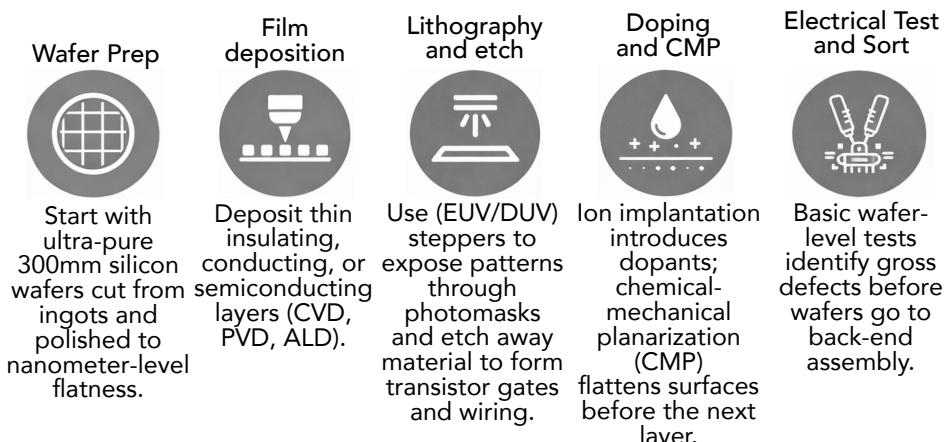
# 3\* FABRICATION FRONT - END

## OVERVIEW

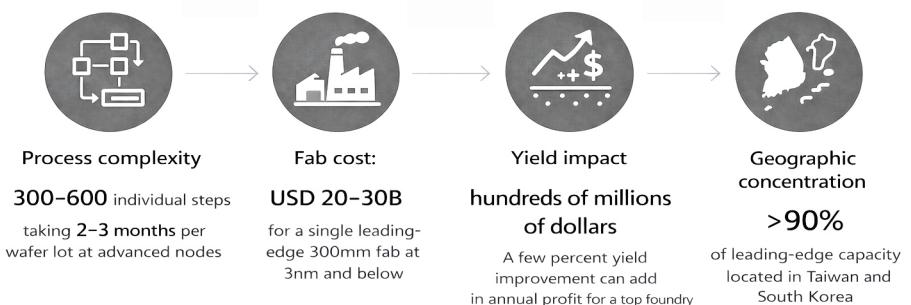
**Fabrication (fab)** is the process of turning blank silicon wafers into patterned wafers containing billions of transistors and interconnect layers using deposition, lithography, etch, implantation, and cleaning steps. Foundries such as TSMC, Samsung, and GlobalFoundries, along with IDM's like Intel, run these fabs at various technology "nodes" (e.g., 28nm, 7nm, 3nm).

**Strategic Role:** Fab capacity and process leadership are among the biggest barriers to entry in semiconductors; leading-edge fabs cost tens of billions of dollars and are geographically concentrated, making them both an economic moat and a geopolitical chokepoint.

## VALUE CHAIN FLOW



## KEY NUMBERS



## GROWTH DRIVERS AND IMPORTANCE

**AI & high-performance computing:** Training and inference workloads demand cutting-edge nodes (3nm, 2nm), driving steady wafer demand and premium pricing for advanced processes.

**Mobile & consumer SoCs:** Flagship smartphone and PC processors continue migrating to newer nodes for better performance per watt, sustaining utilization at leading fabs.

**Mature-node resilience:** Automotive, industrial, and IoT devices rely heavily on 28nm and above, keeping older fabs full and economically important.

## CHALLENGES

**Capex intensity & risk:** Multi-billion-dollar fab investments require high utilization for a decade; demand mis-forecasting can destroy returns.

**Technology scaling limits:** As features approach a few nanometers, variability, power leakage, and lithography challenges increase, raising R&D and process-integration complexity.

**Geopolitical & supply-chain risk:** Taiwan Strait tensions, export controls on advanced tools, and potential natural disasters create systemic risk for the whole industry.



North Americas



Europe



Asia



Oceania America/  
Africa



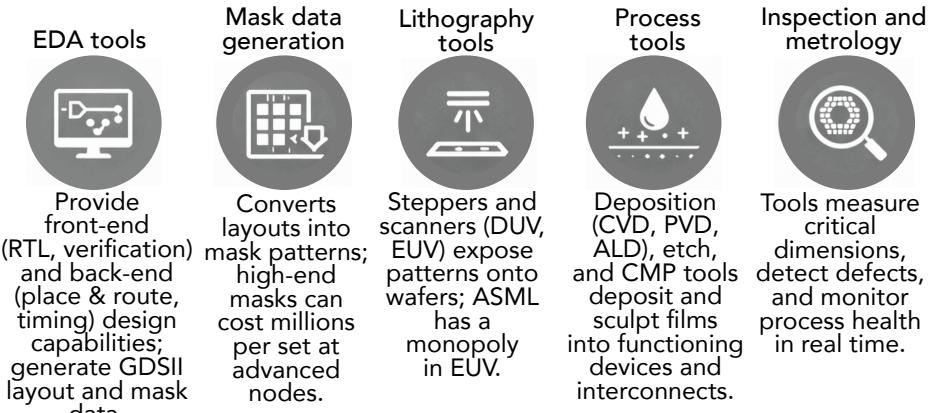
# 4\* EQUIPMENT AND SOFTWARE (EDA)

## OVERVIEW

This layer provides the tools that make chip design and manufacturing possible. Semiconductor equipment companies (ASML, Applied Materials, Lam, Tokyo Electron) build lithography, deposition, etch, and inspection machines for fabs, while EDA vendors (Synopsys, Cadence, Siemens) supply software used for architecture, RTL, verification, and physical design.

**Strategic Role:** Equipment and EDA firms capture a smaller share of semiconductor revenue but have high margins, deep moats, and enormous influence, since no fab or design house can operate without their tools.

## VALUE CHAIN FLOW



## KEY NUMBERS

	North America
	Europe
	Asia
	Oceania / South America / Africa

## DEMAND DRIVERS AND IMPORTANCE

**Node scaling & complexity:** Transition to 3nm, 2nm, and beyond requires new generations of EUV, high-NA tools, advanced deposition/etch, and more sophisticated EDA flows.

**Chiplets & advanced packaging:** Heterogeneous integration and 3D stacking demand new design tools (for system-level planning) and packaging equipment.

**Process control & yield:** As dimensions shrink, defect density and variability control become critical, pushing demand for inspection and metrology tools.

## CHALLENGES

**Export controls & geopolitics:** Restrictions on selling advanced equipment (especially EUV and some DUV/inspection tools) to China limit market access and complicate supply chains.

**Long qualification cycles:** New tools must be co-developed and qualified with leading foundries, taking years before full production deployment and revenue ramp.

**Customer concentration:** A handful of mega-customers (TSMC, Samsung, Intel, SK Hynix, Micron) dominate demand, increasing bargaining power and cyclical exposure.

# 5\*PACKAGING AND TESTING

## OVERVIEW

After wafers are fabricated, they are cut into individual dies, assembled into packages, connected to the outside world (via wires, bumps, or balls), and then tested for functionality and reliability. This "back-end" work is done by IDMs and specialized OSAT (Outsourced Semiconductor Assembly and Test) players such as ASE, Amkor, and JCET.

**Strategic Role:** Packaging and testing determine a chip's final size, thermals, power delivery, and reliability. With chiplets and 3D integration, advanced packaging has become a major performance and cost lever rather than just a low-margin afterthought.



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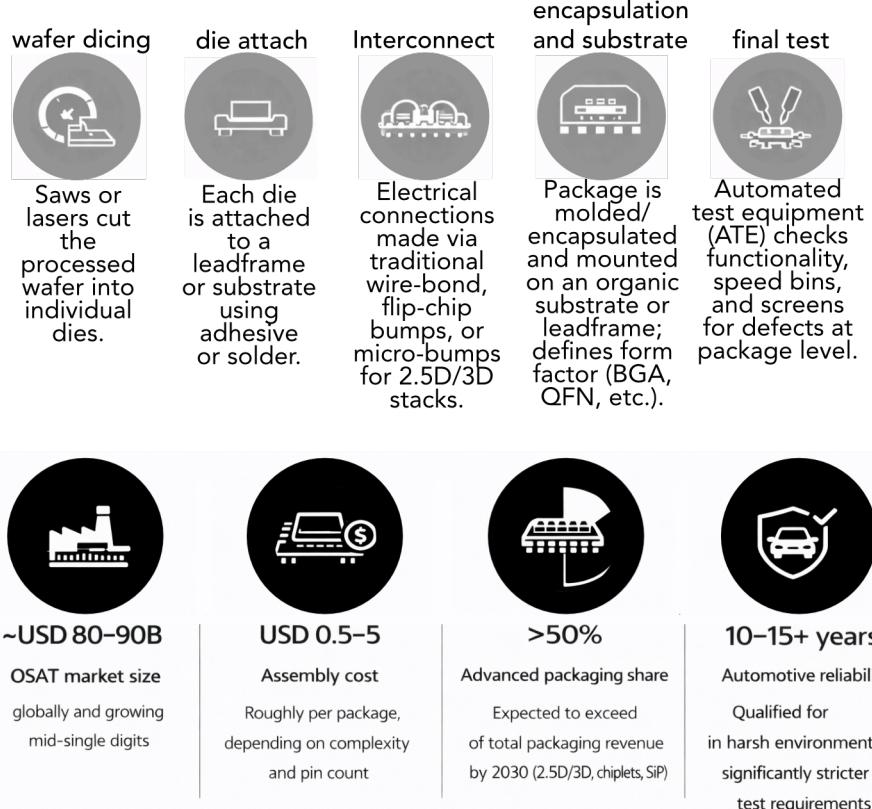
North America

Europe

Asia

South America/  
Africa

## VALUE CHAIN FLOW



## DEMAND DRIVERS AND IMPORTANCE

**Chiplets & 3D integration:** Breaking large chips into multiple dies and stacking them increases yield and performance but shifts complexity to packaging.

**High-bandwidth memory (HBM) for AI:** Stacked DRAM around GPUs/AI accelerators requires advanced interposer or 3D packaging flows.

**Automotive & industrial:** Safety-critical systems (ADAS, powertrain, factory control) need robust packaging and long-term reliability, supporting higher value-add for OSATs.

## CHALLENGES

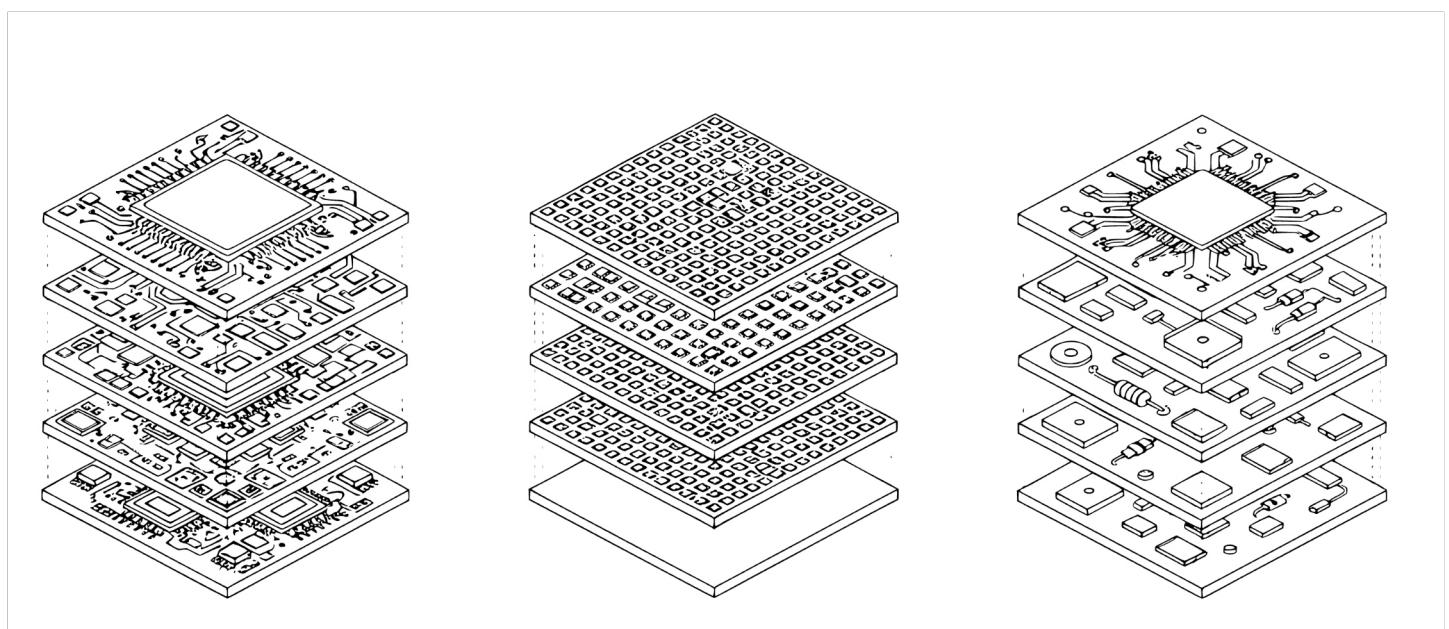
**Margin pressure:** Traditional wire-bond and commodity packages face price competition and overcapacity, keeping margins in the single digits.

**Substrate & material bottlenecks:** Limited supply of advanced substrates and high-density interposers can delay high-end GPU/CPU shipments.

**Geopolitical shifts:** OSAT capacity is concentrated in China, Taiwan, and Southeast Asia; "China+1" and reshoring strategies are pushing gradual diversification to India, Vietnam, and Mexico but require ecosystem buildup.



# TYPES OF SEMICONDUCTORS



LOGIC | MEMORY | ANALOG

# LOGIC SEMICONDUCTORS

## 1\*What They Do

Logic chips are the "brain" that reads software instructions and turns them into actions – doing math, making decisions, and controlling other parts

## 2\*Main Types Of Chips

-  CPUs (like Intel i7 in your laptop) → run Windows/Office
-  GPUs (NVIDIA RTX in gaming PCs) → draw graphics, train ChatGPT
-  Phone SoCs (Snapdragon in Samsung) → handle camera/games/apps
-  MCUs (in your fridge/AC) → turn motors on/off
-  FPGAs (in 5G towers) → change function after built

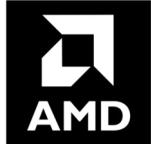
## 3\*How Small And Advanced They Are

Size scale: 3nm (top iPhones) → 40nm (cheap appliances)  
Transistor count: 1 phone chip = 50+ BILLION tiny switches  
Special tricks: 3D "fins" stack transistors taller for more power

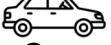
## 4\*How Much They Cost To Make

Design cost: \$100M+ (2-3 years, 500 engineers)  
Most are "fabless" → design only, pay TSMC to build  
Market: \$208B (2024) → \$267B (2025)

## 5\*Top Companies That Make Them



## 6\*Where They End Up Working

-  Data Centres
-  Cars
-  Phones

## 7\*What's Driving Sales

AI explosion → ChatGPT needs NVIDIA GPUs (23% growth)  
Phones upgrade yearly → New Snapdragon chips every fall  
Electric cars → More controllers per Tesla

## 8\*Bigest Headaches

Design hell → 1 bug in 50B transistors = disaster  
TSMC bottleneck → Everyone waits for Taiwan factory slots  
US-China fight → Can't sell best chips to China

# MEMORY SEMICONDUCTORS

## 1\*What They Do

Memory chips store data – DRAM holds it temporarily while your phone/laptop works (like RAM), NAND keeps it forever even when powered off (like SSDs in your laptop).

## 2\*Main Types

-  → DRAM (phone/PC RAM) → super fast but forgets when powered off
-  → NAND Flash (SSDs, phone storage) → keeps data forever, slower than DRAM
-  → HBM (AI special memory) → ultra-fast stacks for ChatGPT training
-  → SRAM (inside CPUs) → fastest memory but expensive/small

## 3\*How Small And Advanced They Are

Size scale: 10nm-20nm (DRAM), 100+ layers 3D NAND

Storage metric: 1 phone NAND = 1 trillion bits (1TB)

Special tricks: NAND stacks 200+ layers vertically like a skyscraper

## 4\*How Much They Cost To Make

Factory cost: \$20B+ megafabs (bigger than football stadiums)

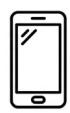
All are IDMs → design AND build their own factories

Market: \$191B (2025), crazy boom-bust prices

## 5\*Top Companies That Make Them



## 6\*Where They End Up Working



Phones



Data centres



Memory cards

## 7\*Whats Driving Sales

AI data centers → HBM memory shortage (SK Hynix +56% share)

Phone storage doubles → 1TB phones need more NAND

SSDs replace HDDs → Laptops/servers upgrade storage

## 8\*Bigest Headaches

Price rollercoaster → NAND prices crash 70% then boom back

Factory overbuild → Too many fabs = bankruptcies

US-China fight → Can't sell best memory to China

# ANALOG SEMICONDUCTORS

## 1\*What They Do

Analog chips connect digital world to real world – they handle sound, light, temperature, power, and radio waves (not just 0s/1s)

## 2\*Main Types



Power chips (PMICs) → charge phone battery, power laptop



Sensors → measure temperature, light, motion in your smartwatch



Audio chips → microphone/speakers in earbuds, phone calls



Radio chips → WiFi/Bluetooth/5G signals

## 3\*How Small And Advanced They Are

Size scale: 40nm-180nm (don't need super-small like CPUs)

Special tricks: Handle heat/voltage (100V+), work 10-15 years

Long life: Car chips last entire vehicle lifetime

## 4\*How Much They Cost To Make

Design cost: \$10-50M (easier than logic chips)

Most are IDMs → own factories, sell directly

Market: \$107B (2025) → steady 6% growth

## 5\*Top Companies That Make Them



## 6\*Where They End Up Working



Cars



Smart Homes



Factories

## 7\*What's Driving Sales

Electric cars → Battery/power management chips explode

Smart factories → Sensors control robots/machines

Smart homes → Thermostats, lights, security cams

## 8\*Bigest Headaches

Car standards → Must work 15+ years in heat/cold

Power limits → Chips handle 100V+ without exploding

China competition → Cheap copies flood market

# SOURCES

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