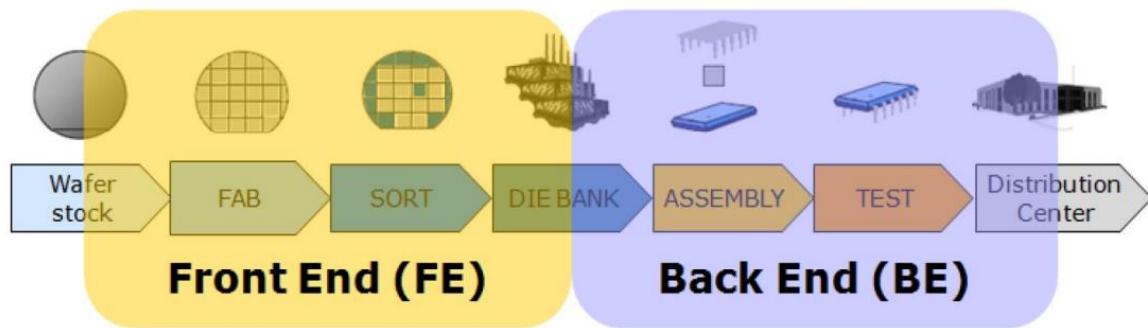


# SEMICONDUCTOR BACK-END PROCESS SERIES



Source - Infineon



Hanol Publishing

## Episode 1: Understanding Semiconductor Testing



### Semiconductor Back-End Process Episode 1

#### Understanding Semiconductor Testing

The process of making semiconductors is split into two main stages: the front-end process of manufacturing wafers and engraving circuits, and the back-end process of packaging the chips. As the miniaturization of semiconductors has now nearly reached its limit, the importance of the back-end process has been growing.

This episode will explain the various packaging and testing practices that are required in the later stages of semiconductor manufacturing to ensure the accuracy and quality of the products.

#### **The Back-end Process of Semiconductors**

The simple order of the manufacturing process consists of the wafer process, the packaging process, and testing. The front-end process refers to the manufacturing of wafers, while the back-end process consists of packaging and testing. Even the wafer manufacturing process is split into a front-end and back-end process. The front-end typically consists of the CMOS-making process, and the back-end refers to the metal wiring formation process that comes after CMOS is made.

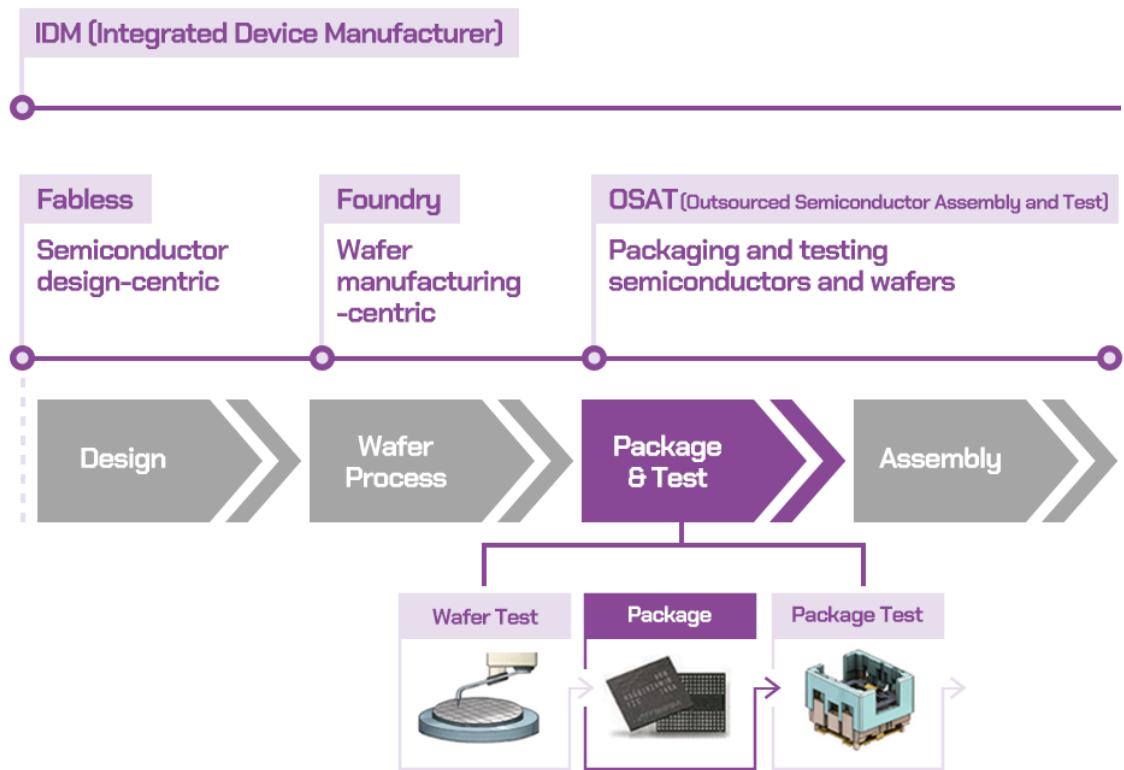


Figure 1 The relationship between the semiconductor manufacturing process and the semiconductor industry (Source: Hanol Publishing)

Figure 1 is a flow chart that shows the relationship between the semiconductor manufacturing process and the semiconductor industry. Companies like Qualcomm and Apple that only design semiconductors are called “fabless.” Products designed by fabless companies are made into wafers, and the facilities that produce these wafers are called “foundries.” Global companies with these facilities include Taiwan’s TSMC and UMC. Then, there are companies that test and package products that were designed by fabless vendors and, later, made into wafers at foundries. These are called OSAT (Outsourced Assembly and Test) which include companies such as ASE and Amkor. Finally, there are the companies that do everything from design, wafer production, and packaging, to testing. These companies are called IDMs (Integrated Device Manufacturer), and SK hynix is one of the leading IDMs in the world.

As shown in Figure 1, the first phase of the packaging and testing process is wafer testing. Afterwards, packages are made in the packaging process and followed by the package test stage.

One of the main reasons for semiconductor testing is to prevent the shipment of defective products. Therefore, it’s necessary to have an exhaustive inspection process that includes various types of testing to secure the quality and reliability of the products. But these

extensive processes increase testing time, equipment, required manpower, and manufacturing costs.

### Testing Temperature, Speed, and Movement

Table 1 Test classification (Source: Hanol Publishing)

Test by Temperature	Test by Speed	Test by Operation
Hot Test	Core Test	DC Test
Cold Test	Speed Test	AC Test
Room Test		Function Test

Tests can be divided into wafer tests and package tests depending on the form of the subject being tested, but the types of testing can be divided into temperature, speed and operation—as shown in Table 1.

The temperature applied to the test subject is the standard for temperature tests. Hot tests apply a temperature of 10% or more above the maximum temperature stated in the products' spec<sup>1</sup>, while cold tests apply a temperature 10% or less than the minimum temperature. Room tests usually apply a temperature of 25°C (77°F). Since semiconductor products are used in different settings with various temperatures, these tests exist to verify the product's ability to operate under various temperatures and to know their temperature margins.

<sup>1</sup>*Spec:* As the abbreviation for “specifications,” the term refers to the blueprint that outlines what’s required during the manufacturing of products such as design regulations, manufacturing methods, or regulations of desired properties in products.

Speed tests are divided into core tests and speed tests. Core tests evaluate whether the core operation, or the main purpose, of a semiconductor performs properly. In the case of semiconductor memories that store data, testing looks at whether data is properly stored in the cell area. Speed tests measure the operating speed, so products are evaluated on whether they can operate at the desired speed.

Operation tests can be divided into three categories: DC tests, AC tests, and function tests. DC tests allow currents to pass into DC so electrical measurements are shown in the form of

currents or voltage. Function tests turn on each function of a product to check if they operate properly.

### The Process of the Wafer Test

Wafer tests inspect the properties and qualities of the numerous chips that are on a wafer. For the test, the testing equipment and the chips need to be connected to send currents and signals to the chips.

Since packaged products have pins like solder balls to connect to the system, electrical connection with the test equipment is relatively easy. However, in the case of wafers, a probe card is required.

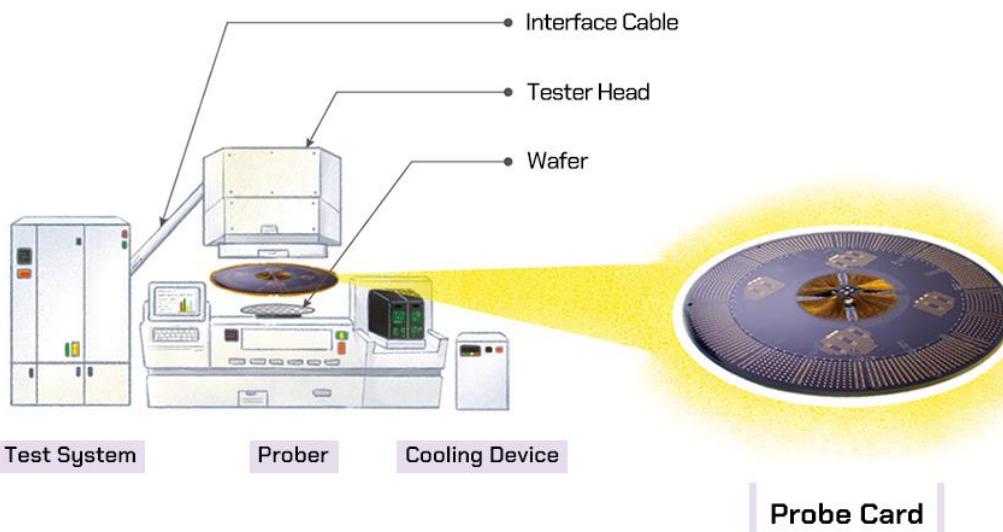


Figure 2 Infographic of wafer testing system (Source: Hanol Publishing)

As shown in Figure 2, many probes<sup>2</sup> are built on the top of the card to make physical contact with the pad of the wafer. The wiring that connects the probe and the test equipment is built into the card. These probe cards are mounted on the tester head so they can make contact with the wafer on the prober where they are loaded.

**<sup>2</sup>Probe:** A needle that makes physical and electrical contact with the wafer pad on the probe card.

When a wafer is loaded with the front side facing up, the probe card on the right is turned over. Then, a probe is mounted on a tester head so that the wafer and probe card can come into contact. At the same time, the temperature control device can apply a temperature in

accordance with the test temperature condition. The test system applies the current and signal through the probe card and then reads the test results from it.

Wafer testing usually follows the following process: EPM (Electrical Parameter Monitoring) → Wafer Burn-in → Test → Repair → Test. These steps are described below.

### EPM (Electrical Parameter Monitoring)

The purpose of testing is to filter out defective products, but it also has the goal of improving products that are under development or being mass-produced by providing feedback on their deficiencies. The main purpose of EPM is to give feedback on the wafer manufacturing process by evaluating and analyzing the electrical characteristics of the product's unit devices. This is a process of measuring transistor characteristics and contact resistance using electrical methods before actual testing to verify whether the manufactured wafer satisfies the basic properties suggested by the design and device departments.

### Wafer Burn-in

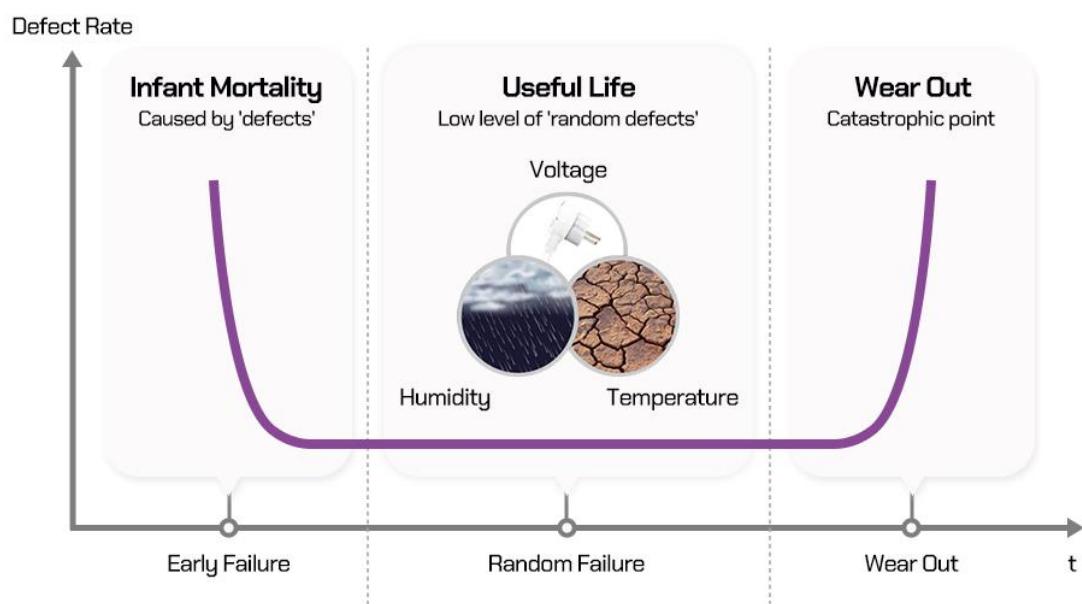


Figure 3 Defect rate according to product usage time (Source: Hanol Publishing)

Figure 3 shows the defect rate during product life as a function of time. As it resembles the shape of a bathtub, it's also called a bathtub graph. In the early stages of its lifecycle, there are many early failures, or failures caused by manufacturing defects. When defects from manufacturing are resolved, random failures, or the defect rate during the service life of the product, happen less often. Moreover, when the product wears out, defect rates rise again.

Burn-in is carried out to detect early defects in advance by prompting potential product defects on purpose. Wafer burn-in applies temperature and voltage to stress the wafer product, so any defects that may appear in the initial failure period are exposed.

### **Wafer Test**

Wafers that went through early failure tests via wafer burn-in are then tested with a probe card for a wafer test. Wafer testing is the process of examining the electrical characteristics of a chip at the wafer level. The test serves several purposes including pre-detection of defective chips, giving device and design feedback through wafer-level verification, and sorting out defects that will occur during packaging/mounting<sup>3</sup> ahead of time. This last procedure ensures that the cause of defects at the wafer level can be analyzed and feedback on the manufacturing process can be provided. If defects are sorted in the wafer test, some of the defective cells<sup>4</sup> can be replaced with redundancy cells through a process called repair.

*<sup>3</sup>**Mounting:** The process of assembling a board or system by mechanically and electrically attaching components.*

*<sup>4</sup>**Cell:** Refers to the minimum set of elements required to store data in a memory element. A cell in DRAM consists of one transistor and one capacitor.*

### **Repair**

Mainly performed with semiconductor memories, the process of repair replaces defective cells with surplus cells by applying the repair algorithm. For example, if 1 bit is defective as a result of a wafer test consisting of a DRAM 256-bit memory, the product will have 255 functioning bits. However, if a surplus cell replaces the defective cell, the chip becomes a quality product that satisfies the 256-bit spec again and can be sold to customers. Through repair, yields eventually increase. For this reason, semiconductor memories create surplus cells during design so they can make substitutes according to test results.

### **Packaging Test**

A chip determined to be a quality product in the wafer test undergoes a packaging process, and the completed package undergoes a packaging test again. Even if the wafer is found to be a quality product during the wafer test, defects may occur during the packaging process. Therefore, the packaging test is essential.

For the packaging test, the package pin (the solder ball in #3 of Figure 4) should be faced down and put into the socket so that it can come into contact with the pins in the socket. Then, the packaging test socket is mounted on a package test board to perform a packaging test.

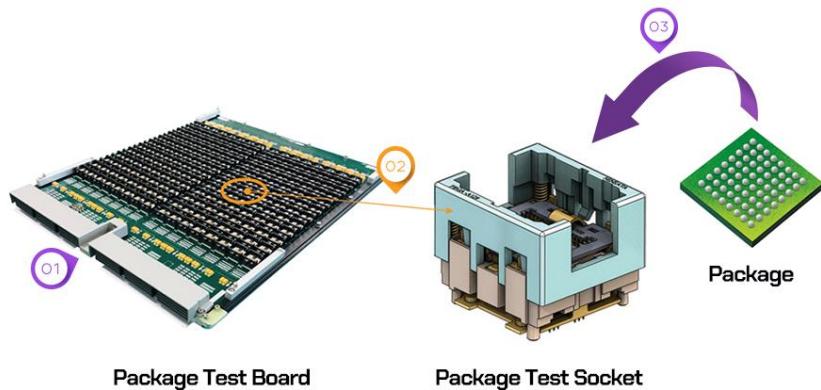


Figure 4 Packaging test system (Source: Hanol Publishing)

### TDBI (Test During Burn-in)

Burn-in is a test that stresses a product with voltage and temperature in order to eliminate potential defects in the product at an early stage. Burn-in performed after packaging is called TDBI. Burn-in can be performed on the wafer or on the package, but most semiconductor manufacturers burn-in the wafer and the package simultaneously.

#### Test

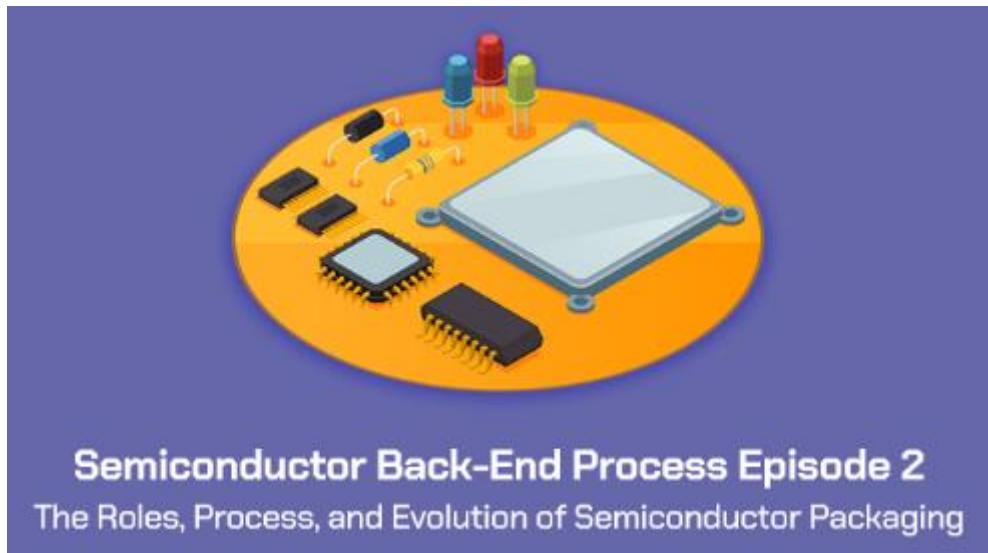
This is the process of determining whether a semiconductor operates normally in the user's environment as defined in the datasheet<sup>5</sup>. A temperature corner test is performed to verify that the product meets the specifications for AC/DC factor weakness and operations requested by the customer in the Cell & Peripherals areas.

<sup>5</sup>**Datasheet:** A regulation document that defines the properties that can be found in a semiconductor product.

#### Visual Test

When testing is completed, the test results must be recorded on the exterior of the package and, consequently, laser marking is required. After the package test has been completed and marked, the quality package is placed in the package tray. Now, the only remaining step is to ship the product to the customer. Therefore, it is necessary to conduct a final visual inspection before shipping to the customer to sort out defects in the exterior. During the visual test, manufacturers look for cracks, markings, improper tray placements, and other defects. For solder balls, manufacturers sort out pressed balls, missing balls, and other defects.

## Episode 2: The Roles, Process, and Evolution of Semiconductor Packaging



When sending fragile items in the mail, it is vital to use appropriate packaging to ensure the package arrives at its destination in one piece. Styrofoam, bubble wrap, and a solid box are all required to protect a package's contents. Likewise, packaging is a critical stage of the semiconductor manufacturing process that protects the chip from mechanical and chemical damage. However, the role of semiconductor packaging is not limited to protection.

In this second article of our back-end process series, we will explain the different levels, diverse roles, and evolution of packaging technology.

### The Four Levels of the Semiconductor Packaging Process

Electronic packaging technology is related to the hardware structure of devices. These hardware structures consist of active elements<sup>1</sup> such as semiconductors and passive elements<sup>2</sup> including resistors and capacitors<sup>3</sup>. Accordingly, electronic packaging is a very broad technology that can be categorized into four different levels that range from level 0 to level 3 packaging. Figure 5 shows the whole semiconductor packaging process starting from level 0 packaging which consists of detaching chips through wafer sawing. This is followed by level 1 packaging which is essentially chip-level packaging. Next, level 2 packaging mounts the chip on a module or a card before level 3 packaging equips a card that is mounted with the chip and the module to a system board. In a broad sense, this entire process is commonly referred to as "packaging" or "assembly." In the semiconductor industry, however, semiconductor packaging generally only refers to the process of wafer sawing and chip-level packaging.

<sup>1</sup>**Active element:** A device that performs a function due to the circuit implementation, just like a semiconductor memory or a logic semiconductor.

<sup>2</sup>**Passive element:** A device that does not have an active function such as amplification or conversion of electrical energy.

<sup>3</sup> **Capacitor:** An element that stores electrons and, consequently, provides electrical capacity.

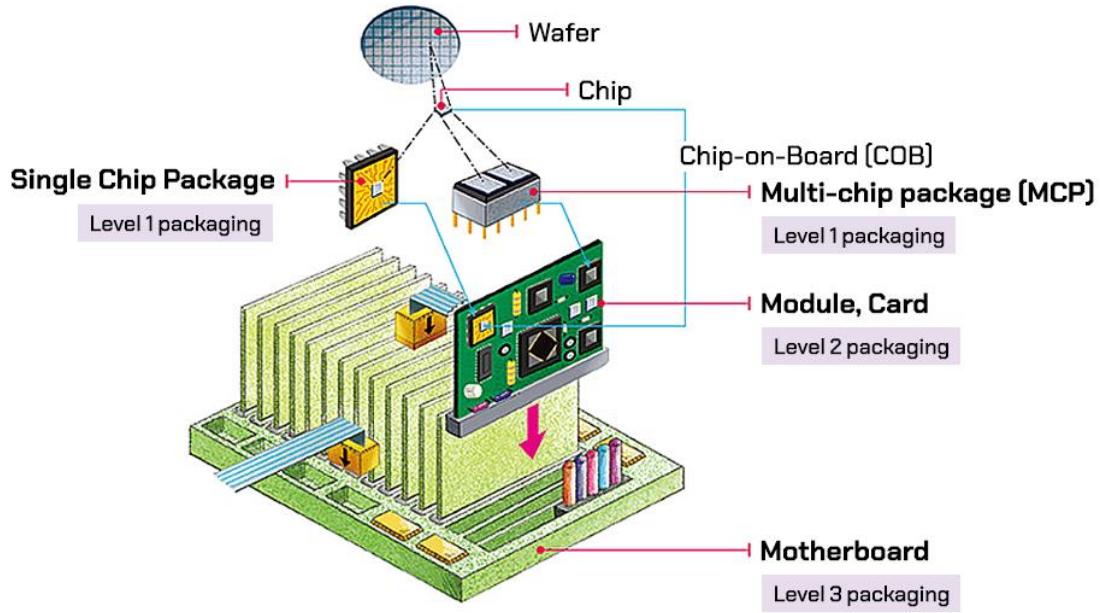
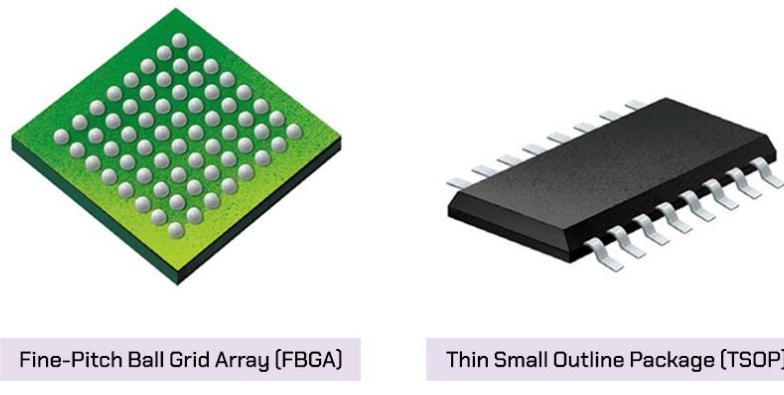


Figure 5 The packaging levels of a semiconductor (Source: Principle of Electronic Packaging, p. 5)

The package generally takes the form of either the fine-pitch ball grid array (FBGA) or the thin small outline package (TSOP) as shown in Figure 6. While solder<sup>4</sup> balls on a FBGA and lead<sup>5</sup> on a TSOP act as pins, these packages allow the chip to be electrically and mechanically connected with external components.

<sup>4</sup> **Solder:** A metal that is capable of both electrical and mechanical bonding as it can melt at low temperature.

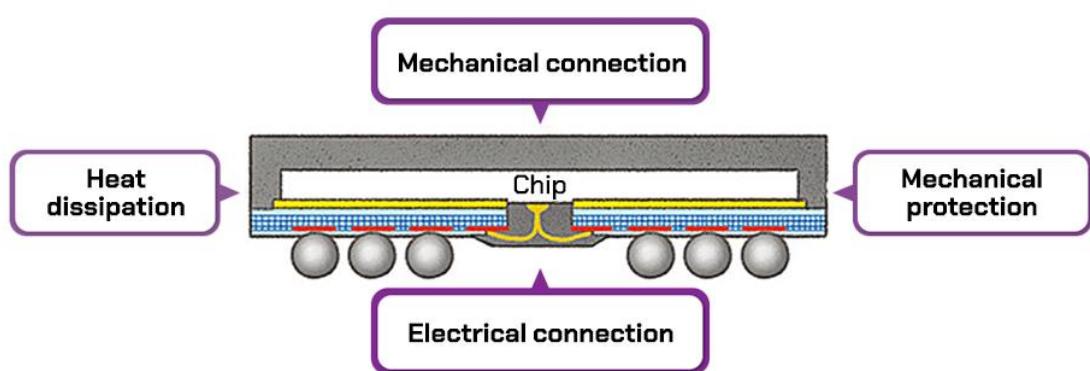
<sup>5</sup> **Lead:** A wire that emerges from the terminals of an electronic circuit or component to allow connections to a circuit board.



*Figure 6 Examples of semiconductor packages (Source: Hanol Publishing)*

### The Roles of Semiconductor Packaging

Figure 7 shows the four main roles of a semiconductor package: mechanical protection, electrical connections, mechanical connections, and heat dissipation. Of these four roles, the main function of a semiconductor package is to protect the chip and devices from external mechanical and chemical damage by sealing them in package materials such as epoxy mold compound (EMC). Although semiconductor chips are made from hundreds of wafer processes to perform various functions, their base material is silicon. Silicon by itself can break as easily as a piece of glass, and the same applies for structures formed after the numerous wafer processes that are also vulnerable to mechanical and chemical damage. Thus, packaging materials prove to be essential in protecting the chips.



*Figure 7 Roles of semiconductor packaging (Source: Hanol Publishing)*

Additionally, the semiconductor package is responsible for electrically and mechanically connecting the chip to the system. The package electrically connects the chip to the system to provide power to the chip while also creating a pathway for the input and output of signals. As for the role of mechanical connection, the chip needs to be well connected to the system to ensure they remain physically attached while in use.

At the same time, the packaging needs to quickly dissipate the heat generated by the semiconductor chip and device. When a semiconductor product is operating, a current is flowing. This inevitably creates resistance and then generates heat. As Figure 3 shows, semiconductor packages completely surround chips. If the semiconductor package cannot efficiently dissipate heat, the chip may overheat and cause the internal transistors to heat up too much to operate. Thus, it is essential for the semiconductor package to dissipate heat effectively. As semiconductor products become faster and possess more functions, the cooling function of the package has become increasingly important.

### **Development Trends in Semiconductor Packaging**

Figure 8 outlines the six development trends in semiconductor packaging technology over the years. When considering these trends, we can see how packaging has evolved to fulfill its roles.

First off, materials with good thermal conductivity<sup>6</sup> and package structures that can effectively dissipate heat have been developed as heat dissipation has become an important factor in the packaging process.

<sup>6</sup> **Thermal conductivity:** A measure of the transfer of heat from a high temperature area to a bordering lower temperature area without involving the movement of matter.

The packaging technology which can support high-speed electrical signal transmission is also an important trend, as the packaging can limit the speed of the semiconductor product. For example, if a semiconductor chip or device that can reach a speed of 20 gigabits per second (Gbps) is connected with a semiconductor package that can only support 2 Gbps, the system will perceive the semiconductor to have a speed of 2 Gbps. Regardless of how fast the chip is, the speed of the semiconductor product is greatly affected by the package as the electrical pathway heading to the system is created in the package. This emphasizes how increases in chip speeds need to be followed by similar advancements in semiconductor packages to realize high transmission speeds. This especially applies to technologies in artificial intelligence and 5G wireless communication. In light of this, package technologies such as flip chip<sup>7</sup> packaging and through-silicon via (TSV)<sup>8</sup> have been developed to support high-speed electrical signal transmission.

<sup>7</sup> **Flip chip:** An interconnection technology which connects chips and substrates electrically with bumps on the substrate flipped over.

<sup>8</sup> **Through-silicon via (TSV)**: A type of vertical interconnect access (via) that completely passes through a silicon die or wafer to enable the stacking of silicon dice.

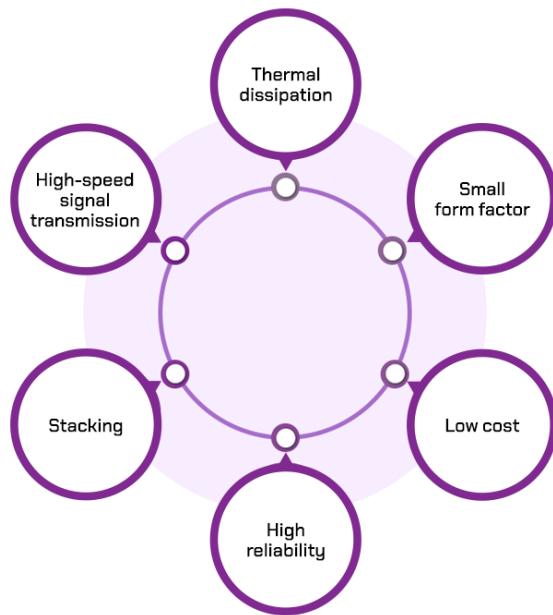


Figure 8 Development trends in semiconductor packaging technology (Source: Hanol Publishing)

Moving on to the next trend, three-dimensional semiconductor stacking technology has become a revolutionary development in the semiconductor packaging field. While only one chip was packaged in the past, there are now technologies that pack multiple chips into one package such as multi-chip package (MCP) and system-in-package (SiP)<sup>9</sup>.

<sup>9</sup> **System-in-package (SiP)**: A type of packaging that combines multiple devices into a single package to implement a system.

Miniaturization, the process of reducing the size of semiconductor devices, is a trend which has also been applied to packaging technology. As semiconductor products are being implemented in mobile and even wearable products, miniaturization is becoming an important requirement for customers. To meet this demand, many technologies have been developed to reduce packaging size.

Moreover, semiconductor products are increasingly being used in a diverse range of environments. In addition to everyday environments such as the gym, office, or home, they are used in tropical rainforests, polar regions, deep oceans, and even space. As the basic role of the package is to protect the semiconductor chip and device, it is necessary to develop highly reliable packaging technology to enable these semiconductor products to operate normally in these extreme environments.

Lastly, as the semiconductor package is the final product, it is important to develop packaging technologies that have low manufacturing costs and can fulfil desired functions.

Alongside the trends mentioned above that focused on advancing specific roles of packaging technology, another driving force behind the evolution of packaging is the development of the semiconductor industry as a whole. In Figure 9, the red line in the graph represents the change since the 1970s in the feature size of a PCB<sup>10</sup> mounted during the assembly process, and the green line shows the changes in the feature size of a CMOS transistor on the wafer. A decrease in the feature size allows smaller patterns to be drawn on the PCB and the wafer.

<sup>10</sup> **PCB (Printed Circuit Board):** A semiconductor board that's made up of electronic circuits and has components soldered on its surface. These boards are found in most electronic devices.

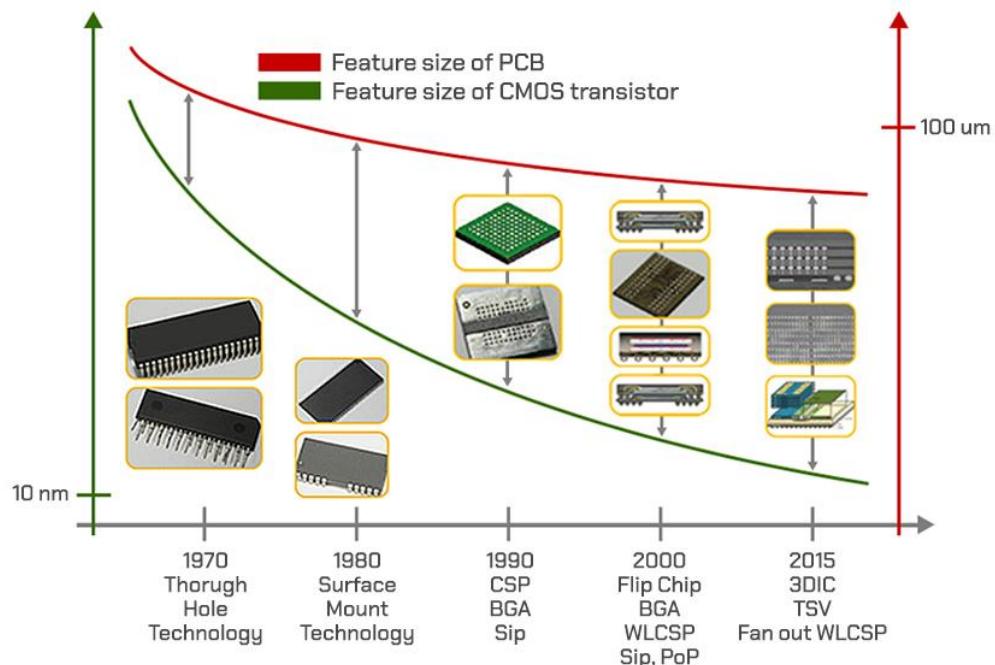


Figure 9 Changes over the years in the feature size of wafers and PCBs (Source: Hanol Publishing)

In the 1970s, the difference of the feature size in PCBs and wafers was relatively small. However, wafers today are being mass-produced and CMOS transistors are being developed to have feature sizes smaller than 10 nanometers (nm), while PCBs still have features sizes in the 100 micrometer (um) range. This gap has widened significantly over the decades.

As the boards are fabricated in the form of panels and there are other factors such as cost-saving tactics, the PCB's feature size has not changed too much. However, the feature size of CMOS transistors has shrunk dramatically due to advances in photolithography which has

widened the gap in sizes with PCBs. The problem is that a semiconductor package must compensate for this difference between a PCB and a wafer, as it is tasked with individualizing the chips cut from the wafer and mounting them on the PCB. This difference in the feature size was not significant in the past, so it was possible to use through-hole technology—where the semiconductor package's lead is inserted in the socket of the PCB—such as dual in-line package (DIP)<sup>11</sup> or zig-zag in-line package (ZIP)<sup>12</sup>. However, as the gap grew wider, it became necessary to use technology that attached leads to the surface of the board such as TSOP, which is a type of surface-mount technology (SMT)<sup>13</sup>. Subsequently, packaging technologies such as ball grid array (BGA), flip chip, fan out wafer level chip scale package (WLCSP)<sup>14</sup>, and through silicon via (TSV) were developed sequentially to compensate for the widening gap between the wafer and board's sizes.

<sup>11</sup> **Dual in-line package (DIP)**: A package where electrical connection pins are arranged in two parallel rows.

<sup>12</sup> **Zig-zag in-line package (ZIP)**: A package where the pins are arranged in zig-zag form, a replacement for the dual in-line package to increase mounting density.

<sup>13</sup> **Surface Mount Technology (SMT)**: A package mounting method that fixes a chip to the system board surface via soldering.

<sup>14</sup> **Wafer level chip scale package (WLCSP)**: A variant of flip chip technology which packages integrated circuits at the wafer level. Fan out WLCSP features connections for the package which spread out ("fan out") beyond the chip's surface.

### Ensuring Effectiveness of Semiconductor Packaging Through Testing

There are two methods to develop a semiconductor package and ensure it works effectively. The first involves using existing packaging technology to create a package suitable for a newly-developed semiconductor chip and evaluating the package. The second method is to develop a new semiconductor packaging technology and then apply it to an existing chip to evaluate the new package's effectiveness.

In general, it is not common to develop a new chip and apply a new packaging technology at the same time as it is difficult to identify the cause of any problems after the packaging is completed if both the chip and the packaging are untested. Therefore, new packaging technologies are tested with existing mass-produced chips that are known to have few defects in order to verify the packaging technology alone. Once a packaging technology is verified, it can then be applied to the development of new chips and, furthermore, lead to the production of semiconductor products.

Figure 10 shows the packaging development process for a new chip. Normally, the design of the chip and the package is developed together when fabricating a semiconductor product so that their characteristics can be optimized holistically. For this reason, the packaging department looks at whether the chip is packageable before it is designed. During this

feasibility study, the package's design is roughly tested so the electrical, thermal, and structural evaluations can be analyzed to ensure that there would be no problems in the actual mass-production stage. In this context, semiconductor packaging design refers to the wiring design of the substrate or leadframe, which is the medium for the chip to be mounted on the board.

The package department provides feedback to the chip designers on the packages' feasibility based on the results of the package's temporary design and analysis. The chip design is only completed when the package feasibility study is finished. This process is followed by wafer fabrication. While the wafers are being fabricated, the package department designs the substrate or leadframe required for package production and proceeds with its production through a company that carries out the back-end process. At the same time, tools for the package process are prepared in advance, and package production begins immediately when the wafers are delivered to the package department after the wafer test.

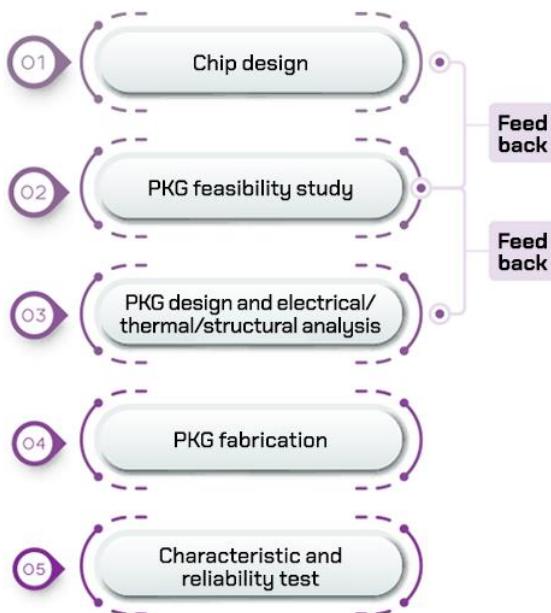


Figure 10 The development process for semiconductor packaging (Source: Hanol Publishing)

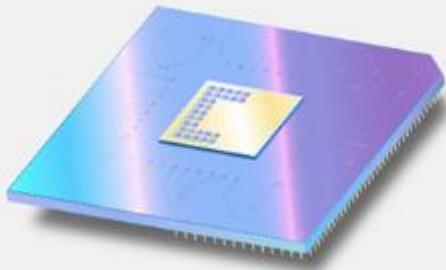
Semiconductor products must be manufactured in packages so that their physical characteristics can be measured and verified. Meanwhile, the design and the processes can be checked with evaluation methods such as a reliability test. If the characteristics and reliability are not satisfied, the cause is investigated and the process is repeated again from the stage where the cause can be resolved. Ultimately, development is only completed after the desired characteristics and reliability standards can be met.

### **Looking Beyond the Roles of Semiconductor Packaging**

As we looked into packaging technology's role of protecting and connecting various components of a semiconductor, it will also be vital to know which materials and methods are used in this process. The next episode will touch on the differences between conventional and wafer-level packaging while observing how different packaging methods affect the quality and efficiency of this fundamental process.

## Episode 3: Understanding the Different Types of Semiconductor

### Packages Part 1



### Semiconductor Back-End Process Episode 3

Understanding the Different Types of Semiconductor Packages

[In the previous episode](#), it was established that semiconductors require packaging for protection. These packages come in all different shapes and sizes while using different methods to protect and connect delicate integrated circuits. This episode will explore the various categorizations of semiconductor packages, including the types of materials used to make them, their distinct manufacturing techniques, and their application cases.

#### Classification of Semiconductor Packages

Figure 11 shows the various types of semiconductor packages broken down into two main categories: conventional and wafer-level packaging. In conventional packaging, the wafer is sawed before the chip is packaged, while wafer-level packaging involves a part, or all, of the packaging process being performed at the wafer level before proceeding with wafer sawing.

## Semiconductor Package Classifications

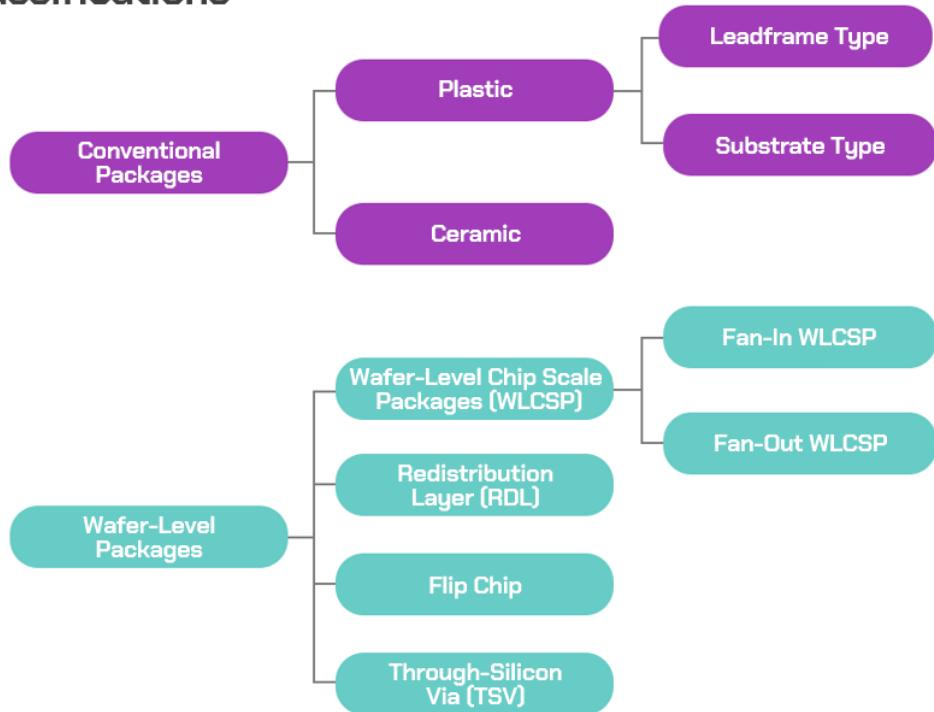


Figure 11 Types of semiconductor packages (Source: Hanol Publishing)

Based on the materials being packaged, conventional packages can be divided into ceramic and plastic packaging. Plastic packages can be further categorized into leadframe or substrate packages depending on the medium of the package.

As for wafer-level packages, they can be categorized into four different types: 1) wafer-level chip scale packages (WLCSP) in which wiring and solder balls are formed on top of the wafer without a substrate 2) redistribution layers (RDL) that use a wafer-level process to rearrange the pads<sup>1</sup> on the chip that are electrically connected to the outside 3) flip chip packages in which solder bumps<sup>2</sup> are formed on the wafer to undergo the packaging process, and lastly 4) through-silicon via (TSV) packages that utilize TSV to make internal connections within stacked chips.

For WLCSP, it is divided into fan-in and fan-out WLCSP. The process for fan-in WLCSP involves attaching wiring and solder balls on top of the wafer, while fan-out WLCSP involves rearranging the chips into a molding<sup>3</sup> wafer. This is done to form wiring through a wafer-level process and to attach solder balls onto a package larger than the chip.

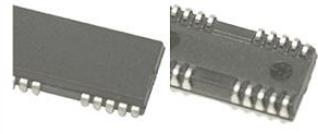
<sup>1</sup>**Pad:** A passageway that electrically connects to other mediums. On a chip, pads are made to electrically connect with the outside through wires or flip chip bumps. On a substrate, pads are made to connect the chips to each other.

<sup>2</sup>**Solder bump:** A conductive bump that connects a chip to a substrate through flip chip bonding. It also connects ball grid arrays (BGA) or chip scale packages (CSP) to a circuit board.

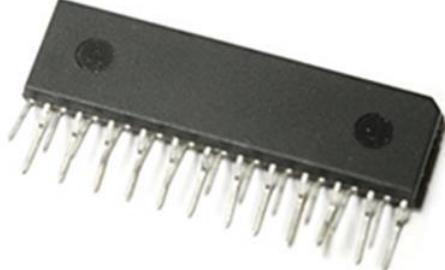
<sup>3</sup>**Molding:** The process of sealing wire-bonded or flip chip bonded semiconductor products with an epoxy molding compound (EMC).

## Conventional Packages

### Plastic Packages: Leadframe

QFP/TQFP	TSOP	SOJ
[Thin] Quad flat package: Four-sided lead type	Thin small outline package: Two-sided, gull-form lead Surface mounting type	Small outline J-leaded package: J-form lead Surface mounting type
		

▲ Surface mounting types where the leads are attached to the surface

DIP	ZIP
Dual in-line package: Pin insert type [through hole]	Zig-zag in-line package: One-sided lead type
	

▲ Through hole types where the leads are inserted into holes in the PCB

Figure 12 Types of leadframe packages (Source: Hanol Publishing)

In a plastic package, the chip is covered in plastic materials such as epoxy mold compound (EMC)<sup>4</sup>. A leadframe package is a type of plastic package that uses a metal lead called a leadframe as its substrate. The leadframe uses an etching method to form wiring on thin metal plates.

*<sup>4</sup>Epoxy mold compound (EMC): A thermosetting plastic with excellent mechanical and electrical insulation in addition to temperature resistance properties. It is a resin with relatively small molecular weight capable of three-dimensional curing in the presence of a curing agent or catalyst.*

Figure 12 shows the different types of leadframe packages. In the 1970s, through hole types like dual in-line packages (DIP) or zig-zag in-line packages (ZIP) in which leads are inserted into holes in the printed circuit board (PCB) were commonly used. Later, as the number of pins increased and the design of PCBs became more complex, techniques inserting leads into holes started to reach their limitations. This eventually led to the development of surface-mounting types such as thin small outline packages (TSOP), quad flat packages (QFP), and small outline J-leaded packages (SOJ). For products that require a large number of I/O pins like logic chips, packages like QFP in which leads are attached on all four sides are applied. Packages such as thin QFP (TQFP) and TSOP were also developed as system environments required thinner packages.

As higher speeds became more important for semiconductor products, substrate packages which can support multi-layer wiring designs became the mainstream packaging technology. Nevertheless, leadframe packages such as TSOP are still widely used because of their low manufacturing costs. Since leadframes are made by stamping or etching wiring shapes on metal plates, they are cheaper than substrates that have a relatively complex manufacturing process. Therefore, leadframe packages are still the preferred choice for the production of semiconductor products that do not require high-speed electrical characteristics.

### Plastic Packages: Substrate

As the name suggests, substrate packages use a substrate as the medium. They are sometimes referred to as laminated packages because the substrate is made using multiple layers of film. Unlike leadframe packages which only have one metal layer in the wiring as they are made with a leadframe—a metal plate unable to form more than two metal layers—substrate packages can feature several layers of wiring. This leads to better electrical characteristics and a smaller package size. Another key difference between leadframe and substrate packages is the wiring connection process. The wiring connecting the chip and the system must be separately implemented on the leadframe and the substrate. If the wiring needs to cross each other, a substrate can make a wire cross to another metal layer while a leadframe is unable to do this as it only has one metal layer.

As shown in Figure 13, substrate packages can also feature a large number of pins by arranging the solder balls that serve as the pins on one entire side. In contrast, the leads

acting as pins of leadframe packages can only be formed on the edges of one side. This also improves the electrical characteristics of substrate packages in the process. As for the size of the packages, leadframe packages are generally larger as they consist of the main frame and the space taken up by the lead on the sides. However, substrate packages are smaller as the pins are on the bottom of the package to save space.

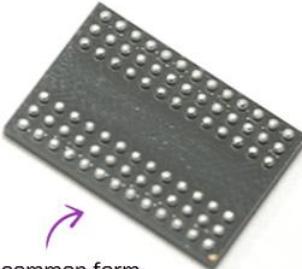
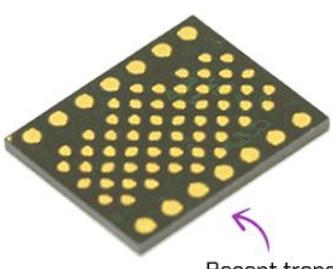
BGA/FBGA	LGA
[Fine pitch] Ball grid array package: Solder balls attached to package substrates	Land grid array: No solder ball land array on substrate
	

Figure 13 Comparison of BGA and LGA (Source: Hanol Publishing)

Due to these advantages, most semiconductor packages today are substrate types. The most common type of substrate package is the ball grid array (BGA) package, but land grid array (LGA) packages, which feature a ball land structure consisting of flat contacts instead of balls as seen in Figure 3, have also been used in recent times.

### Ceramic Packages

Ceramic packages have a ceramic body which provides excellent heat dissipation and reliability. However, as the process of manufacturing ceramics is expensive, the overall cost of manufacturing the packages is also high. Consequently, these packages are mainly used for logic semiconductors that require high reliability as well as for verifying packages made for CMOS image sensors (CIS).

### **Wafer-Level Packages**

#### Fan-In WLCSP

WLCSP is a prime example of a wafer-level package as most of the manufacturing process takes place at the wafer level. In a broader sense, however, any package that is even partially processed at the wafer level is considered a wafer-level package. Examples include packages that use RDL, flip chip technology, and TSV. In regards to fan-in WLCSP and fan-out WLCSP, the term “fan” refers to the chip’s size. A fan-in WLCSP has package wiring, an insulation

layer, and solder balls directly on top of the wafer, contributing to various advantages and disadvantages when compared to conventional packages.

As the size of the package is equal to the size of the chip in fan-in WLCSP packages, they can be manufactured to the smallest dimensions. Furthermore, as the solder balls are directly attached to the chip without a medium such as a substrate, the electrical transmission path is relatively short and, thus, improves electrical characteristics. Lastly, these packages can be processed at a low cost as there is no need for package materials such as substrates and wires. As the package is processed all at once at the wafer level, it can further save costs if there is a large number of net dies—the chips on the wafer—and a high yield.

As for the downsides, fan-in WLCSP packages have weak physical and chemical protection capabilities due to the silicon (Si) chip acting as the package itself. For this same reason, these packages' coefficient of thermal expansion<sup>5</sup> is vastly different to the PCB substrate to which they will be attached. This puts more stress on the solder balls connecting the two and makes solder joint reliability<sup>6</sup> relatively weak.

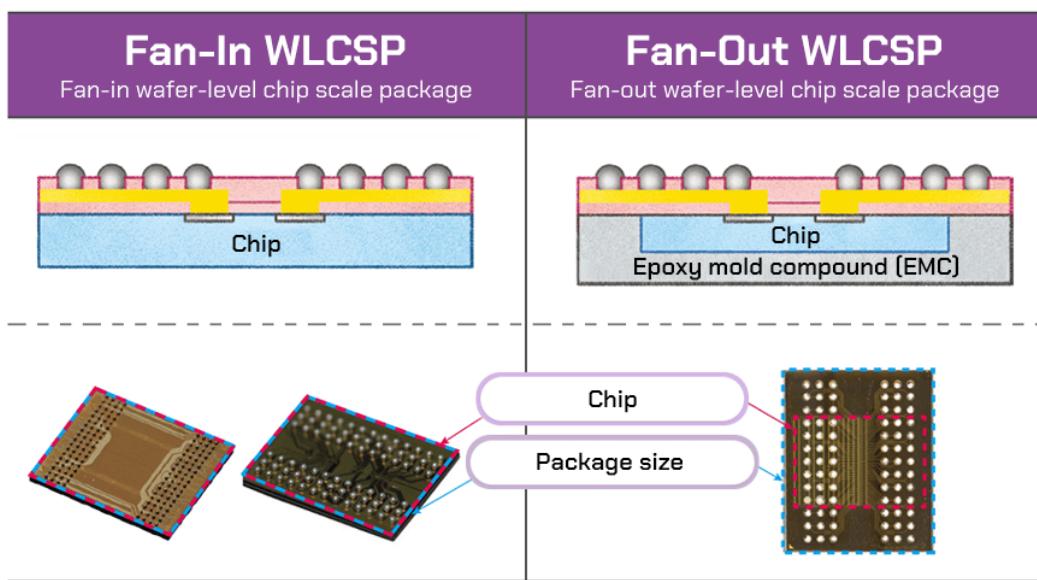
*<sup>5</sup>Coefficient of thermal expansion: The rate at which the volume of an object increases with rising temperature due to constant pressure. The expansion or contraction is linearly related to the increase or decrease in temperature.*

*<sup>6</sup>Solder joint reliability: The quality that ensures the joint can conduct its intended purpose of making a mechanical and electrical connection during the life of the package when it is connected to a PCB with soldering.*

Another disadvantage of fan-in WLCSP packages is the inability to use existing infrastructure for package testing. And if the package ball layout is larger than the chip size, packaging is not possible at all as the solder ball layout cannot be made on a package. Finally, the packaging costs for fan-in WLCSP can be higher than conventional packaging if the number of chips on the wafer is small and the yield is low.

### Fan-Out WLCSP

Fan-out WLCSP possesses the advantages of fan-in WLCSP while overcoming its disadvantages. Figure 14 shows this comparison between fan-in and fan-out WLCSP.



*Figure 14 Comparison of fan-in WLCSP and fan-out WLCSP (Source: Hanol Publishing)*

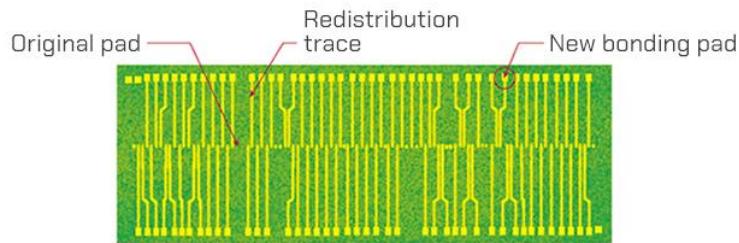
In a fan-in WLCSP, all of the solder balls for the package are on the chip's surface, while a fan-out WLCSP features solder balls for the package which can be “fanned out” away from the chip. For fan-in WLCSP, the wafer is sawed after the packaging process is complete rather than in the middle of the process. Consequently, the size of the chip and the package must be the same, and the solder balls must be within the chip's size. Fan-out WLCSP, on the other hand, involves sawing the chips before the packaging process and arranging the sawed chips on a carrier to reshape the wafer. During this time, the space between the chips is filled with EMC to form a wafer. The wafers are then removed from the carrier, subjected to wafer-level processing, and sawed to make a unit of fan-out WLCSP.

In addition to offering good electrical characteristics just like fan-in WLCSP, fan-out WLCSP overcomes several disadvantages of fan-in WLCSP. These include the inability to use existing infrastructure for package testing, the inability to package products when the ball layout is larger than the chip's size, and increased processing costs arising from the need to package defective chips all together. Due to these advantages of fan-out WLCSP, the application of these packages has been growing in recent years.

### RDL

RDL technology refers to the act of rewiring. The purpose of this technology is to rearrange the bonding pads that are already formed on the wafer by adding additional metal layers. Figure 15 shows a diagram and a cross-sectional structure of a center pad chip in which the pads have been redistributed to the edges using RDL technology. RDL technology is a wafer-level process that only reconfigures the pads, and the wafers that have gone through RDL undergo a conventional packaging process to complete the package.

## Chips With RDL Technology



## Cross-Sectional Chip Diagram

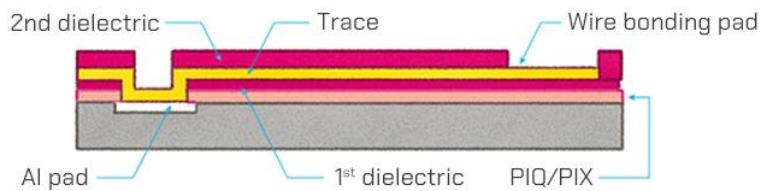


Figure 15 A cross-sectional view of a chip with RDL technology (Source: Hanol Publishing)

When a customer requests a unique pad arrangement on a wafer, it is more efficient to rearrange the pads on an existing wafer using RDL technology during its packaging rather than going through a new wafer fabrication process. Additionally, RDL technology is also used for chip stacking of center pad chips.

### Flip Chip

Flip chip technology gets its name because the bumps formed on the chip are flipped and attached to the package body such as a substrate. It is an interconnection method that electrically connects chips and boards such as substrates, just like traditional wire bonding.

Flip chip technology has mostly replaced wire bonding, however, due to its superior electrical properties. There are two reasons for this: I/O pins that can be electrically connected are not as limited in number or placement as in wire bonding, and the electrical signal transmission path is also shorter compared to wire bonding.

The placement of metal pads on top of a chip used in wire bonding is one-dimensional, limiting their placement to the edges or center of a chip. Flip chip bonding, on the other hand, has no process constraints when it is bonded to the substrate and when the solder bumps are formed. So, the metal pad can be arranged in a two-dimensional manner by using a whole entire side of the chip, which increases the number of metal pads by the power of two. In addition, the pads that will form the bumps can be placed anywhere on top of the chip. Moreover, pads that supply power can be placed near areas where power is required, further enhancing the electrical characteristics. As Figure 16 shows, the signal path for flip

chip bonding becomes much shorter compared to wire bonding when exporting information from the chip to the same package ball. It further boosts the electrical characteristics.

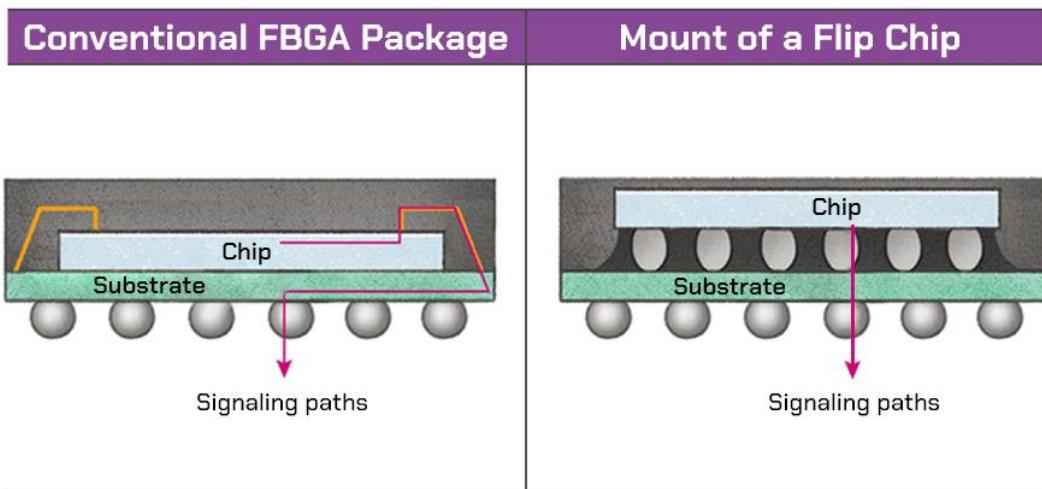


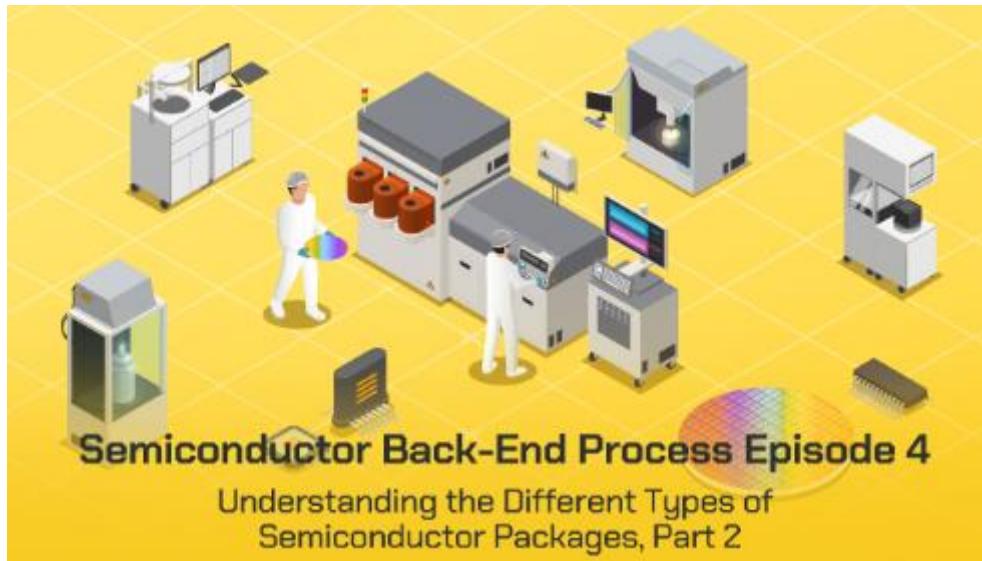
Figure 16 Comparison of signal transmission paths for wire bonding and flip chip bonding (Source: Hanol Publishing)

As explained, WLCSP and flip chip both form solder balls on top of a wafer. Although both technologies can be mounted directly on a PCB board, there is a fundamental difference between the two—the size of the solder.

With WLCSP, the diameter of its solder balls is typically a few hundred micrometers ( $\mu\text{m}$ ), but the solders formed on the flip chip are only a couple dozens of  $\mu\text{m}$ . Due to its small size, the solder formed on the flip chip is often referred to as a solder bump rather than a solder ball and it is difficult to ensure solder joint reliability with this solder alone. WLCSP solder balls can handle the stress from the difference in the coefficient of thermal expansion between the substrate and the chip. Flip chip solder bumps, on the other hand, cannot. Therefore, to ensure solder joint reliability, a polymer-type underfill material must be used to fill between the flip chip bumps. The underfill material disperses the stress on the bumps and ensures solder joint reliability.

As there are a wide variety of semiconductor package types in addition to the ones explained in this article, the next episode will put a special focus on stack packages and system-in-packages, while subcategories such as wire bonding and TSV will also be explained.

## Episode 4: Understanding the Different Types of Semiconductor Packages, Part 2



Continuing from the previous episode which introduced conventional and wafer-level packages, this article will explore packaging technologies that combine multiple packages and components within a single product. In particular, it will explain package stacking and system-in-package (SiP) technologies which reduce the required development space and increase the efficiency of the packaging process.

### Stacked Packages

Imagine a housing complex consisting of numerous low-rise buildings for thousands of people. It would require a very large area to accommodate the residents. However, the same number of residents could fit in a single skyscraper. This example clearly shows one of the key benefits of stacked packages. Compared to a product made with multiple packages spread horizontally across a wide area, a product consisting of stacked packages offers enhanced performance within a much smaller space. In addition to being an important packaging technology, stacked packaging is also an essential method in product development.

It used to be common for products to have only one chip per package, but it is now possible to develop a multi-chip package that has different functions or to place multiple memory chips in a single package that has an increased capacity. Furthermore, the development of SiP has allowed various system components to be implemented in a single package. Such technologies have enabled semiconductor companies to create high value-added products while also responding to the diverse needs of the market.

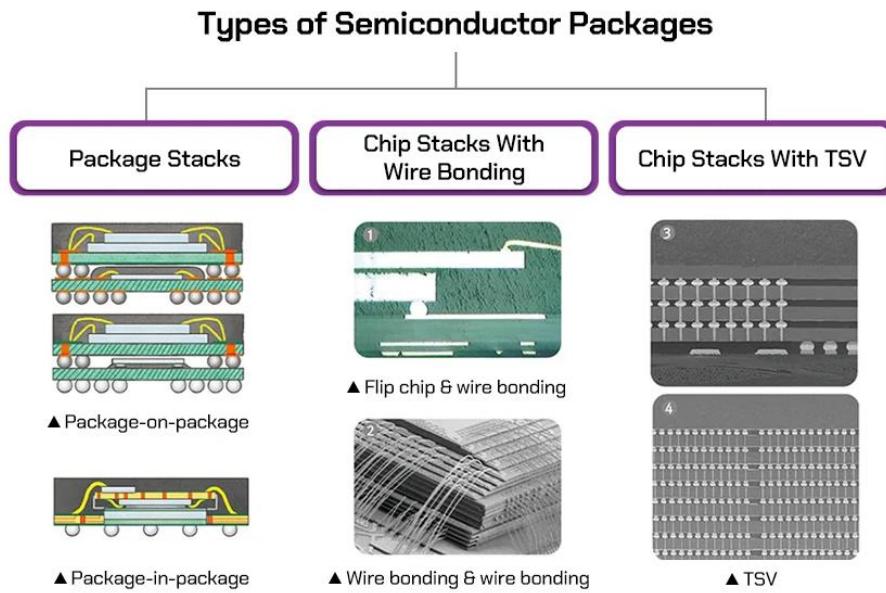


Figure 17 Different methods of stacking packages (Source: Hanol Publishing)

As Figure 17 shows, stacked packages are categorized into three major types based on their distinct development techniques: 1) package stacks that are made by vertically stacking the packages, 2) chip stack packages that use wire bonding to stack chips within a single package, and 3) chip stack packages that use through-silicon via (TSV)<sup>1</sup> rather than traditional wire bonding for the internal electrical interconnections. Each of these stacked packages has different features and various advantages and limitations which will determine their future applications.

<sup>1</sup>**Through-silicon via (TSV):** A type of vertical interconnect access (via) that completely passes through a silicon die or wafer to enable the stacking of silicon dice.

## #1. Package Stacks

A package stack is made by vertically stacking the packages. Consequently, its advantages and disadvantages are opposite to that of chip stack packages. The package stack method places packages on top of each other once they have completed testing, so it is possible to easily replace a package that fails a test with a properly functioning package. This, in turn, results in better test yields compared to chip stack packages. However, due to package stacks' larger size and longer signal paths, their electrical characteristics can be inferior to that of chip stack packages.

One of the most common package stacking methods is package-on-package (PoP), which is widely used in mobile devices. For a PoP in a mobile device, the types and functions of the chips used in the upper and lower packages may vary while the chip manufacturers can also differ.

In general, the upper packages mainly include memory chips made by semiconductor memory companies while the packages stacked below feature chips with a mobile processor that are designed by fabless companies and produced in foundries and Outsourced Semiconductor Assembly and Test (OSAT) facilities. As the packages are manufactured by different parties, quality testing is conducted before being stacked. Even if a defect occurs after stacking, it can be reworked by just replacing the defective part with a new package. Accordingly, it is clear that the mobile business sees significant benefits from package stacking.

### **#2. Chip Stacks with Wire Bonding**

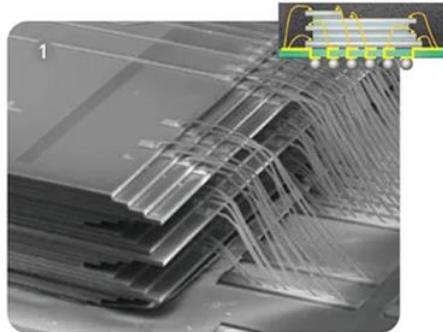
When placing multiple chips in a package, they can either be stacked vertically or attached horizontally to the board. Given that the horizontal layout may result in a larger package size, vertical stacking has become the preferred method. Compared to package stacks, chip stack packages are smaller in size and possess enhanced electrical characteristics due to their shorter electrical signal paths. However, even if a defect is found in a single chip during testing, the entire package needs to be discarded. Thus, chip stack packages have relatively low test yield rates.

In chip stack packages, the memory capacity increases as more chips are stacked in the package. This has resulted in the development of technologies which enable more chips to be layered in a package. However, as it is undesirable for the package to get thicker even as more chips are stacked, technologies that limit the package's thickness have been under development. To do so, everything that affects the thickness of a package including the chip and the substrate must be made thinner, and the gap between the uppermost chip and the surface above the package needs to be reduced. This poses many challenges in the packaging process because chips are more likely to get damaged as they become thinner. That is why developments in packaging processes are underway to overcome these challenges.

### **#3. Chip Stacks with TSV**

TSV is a chip stacking technique that drills holes through silicon to accommodate electrodes. Instead of using the traditional method of wiring to connect chip-to-chip or chip-to-substrate, TSV connects chips vertically by drilling holes in the chip and filling them with conductive materials such as metal. Although a chip-level process is used when stacking with TSV, a wafer-level process is used to form TSV and solder bumps on the front and back of the chip. Therefore, TSV is classified as a wafer-level package technology.

Chip Stacks With  
Wire Bonding



Chip Stacks With TSV

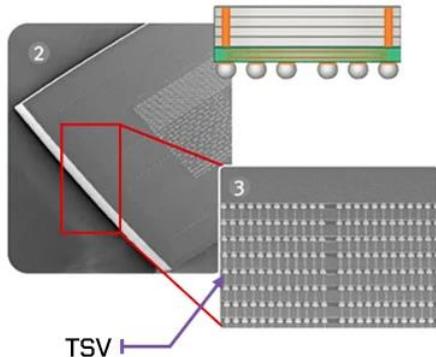


Figure 18 A cross-sectional view of a chip which applied TSV technology (Source: Hanol Publishing)

The main advantages of packages using TSV are the high level of performance and smaller package size. As shown in Figure 18, the chip stack package with wire bonding has wires connected to the sides of each stacked chip. As there are more stacked chips and connected pins, the wiring becomes more complex, with more space needed to connect them. In contrast, the chip stack with TSV does not require complicated wiring and, therefore, allows reduction in package size.

As explained in the previous episode, flip chips have good electrical properties due to several reasons: it is easier to form I/O pins in desired locations, there is an increase in the number of pins, and they have short electrical signal transmission paths. These are the same reasons that give TSV packages strong electrical properties. When sending an electrical signal from a chip to the chip right below it, TSV allows the signal to go straight down. In contrast, if wire bonding is used, the signal transmission path becomes much longer as the signal has to go down to the substrate before making its way up to the chip. As shown in the image of a chip stack with wiring in Figure 18, wiring connections cannot be made in the center of the chip. Contrastingly, TSV packages allow the center of the chip to be drilled, made into electrodes, and connected with other chips. Unlike wiring connections, TSV enables the number of pins to be significantly increased.

High Bandwidth Memory (HBM) utilizes a new DRAM architecture that takes advantage of this ability to increase the number of pins. Typically, an “X4” in DRAM specification implies that there are four pins that can send information, or 4 bits of information can be simultaneously sent from the DRAM. Accordingly, X8 refers to 8 bits, X16 refers to 16 bits, and so on. It is favorable to increase the number of these pins as it allows more information

to be sent simultaneously. However, chip stacking with wiring could only reach X32 due to limitations, while stacking through TSV does not have such limitations, enabling HBM to go up to X1,024.

Current mass-produced memory products that apply TSV to DRAM include HBM and 3D stacked memory (3DS). The former is used in graphics, networking, and high-performance computing (HPC) applications, while the latter is primarily used as a DRAM memory module.

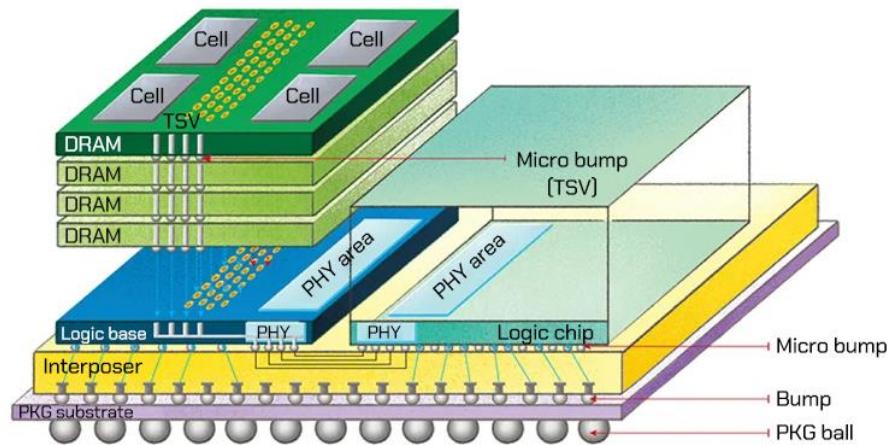


Figure 19 A 2.5D package using HBM (Source: Hanol Publishing)

Rather than being a fully packaged product, HBM is a semi-packaged product. When an HBM product is sent to a system semiconductor manufacturer, they use an interposer<sup>2</sup> to make a 2.5D package<sup>3</sup>, with an HBM placed side-by-side to a logic chip as shown in Figure 19. Since substrates in 2.5D packages are unable to provide pads that can support all the I/O pins of both HBMs and logic chips, interposers come in to accommodate HBMs and logic chips by creating pads and metal wiring. Then, these interposers connect back with the substrate. As for these 2.5D packages, they are considered as a type of SiP.

3DS memory, another product that uses TSV, is a type of memory module with a BGA<sup>4</sup> package mounted on a PCB board. Although DRAM memory modules in servers require high speed and a large capacity, chip stack packages that use wiring are unable to meet these requirements due to their speed limitations. This has led to the use of modules made from TSV-applied chip stack packages for high-end systems such as servers.

<sup>2</sup>**Interposer:** Wide and extremely fast electrical signal conduits used between die in a 2.5D configuration.

<sup>3</sup>**2.5D package:** 2.5D and 3D packages include multiple integrated circuits inside each package. In the 2.5D structure, two or more active semiconductor chips are placed side-by-

*side on a silicon interposer. In the 3D structure, active chips are integrated by die stacking vertically.*

***<sup>4</sup>Ball grid array (BGA): A type of surface mount chip package that uses a grid of solder balls as its connectors.***

### ***System-In-Package (SiP)***

*A package consisting of HBM and a logic chip is a type of SiP. As its name suggests, SiP implements a system in a single package. While components such as sensors, analog-to-digital (A/D) converters, logic chips, memory chips, batteries, and antennas must also be included to form a complete system, it is not possible to include all these system components into a single package with the current developments in technology. It has therefore become the goal of researchers to continue developing package technologies in this area, and SiPs today usually refer to combining some of the system components in a single package. For instance, packages that have applied HBM combine HBM and the logic chip into a single package to create an SiP.*

*Unlike SiP, system-on-chip (SoC) implements system functions on the chip-level. In other words, several system functions are implemented on one chip. As an example, most processors today have static RAM (SRAM) memory within the chip, allowing the logic functions of the processor and the memory functions of the SRAM to be implemented together on a single chip. Therefore, these processors are classified as an SoC.*

*SoCs have a complex and lengthy development process because they require multiple functions to be packed into a single chip. Moreover, upgrading the functions of a single element in an already developed SoCs requires one to design and develop them from scratch. SiPs, on the other hand, are easier and quicker to develop because they are made by collecting already developed chips and devices into a single package. Even if the device has a completely different structure, the chip itself is developed and manufactured separately, making it relatively easy to make it into a single package. Also, if just a single aspect of the function needs an upgrade, the newly developed device can be implemented in the chip without developing the whole package from scratch. However, if a product is going to be used in large quantities over an extended period of time, it may be more efficient to develop it as an SoC rather than an SiP as the latter requires more materials to be manufactured and leads to a larger package size to fit multiple chips in a single package.*

*Despite the various differences between SoCs and SiPs, it is not necessary to choose between one of these two technologies. In fact, they can be combined to create synergies. Once an SoC is developed, it can be packaged with other functional chips into a single package and implemented as an enhanced SiP.*

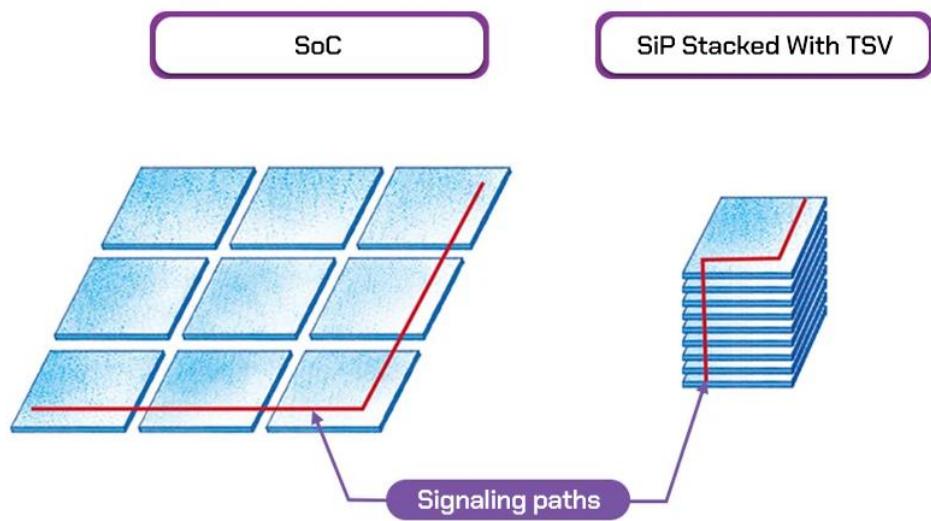
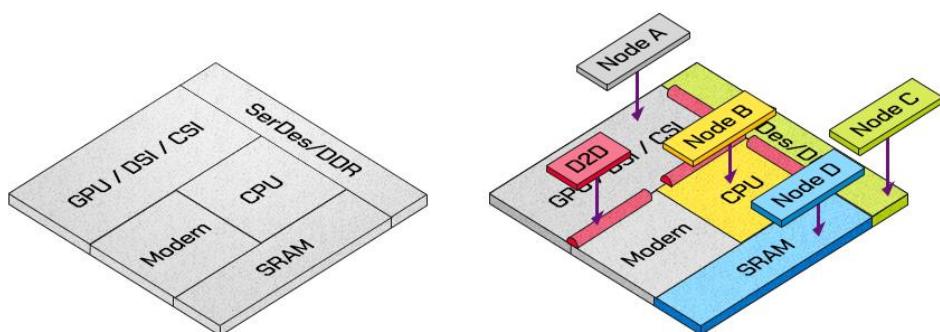


Figure 20 Comparison of signal transmission path length of SoC and SiP stacked with TSV (Source: Hanol Publishing)

When comparing the performance of SiPs and SoCs, it was originally thought that the electrical characteristics of SoCs were better due to their implementation on a single chip. However, with the advent of chip stacking technology such as TSV, SiPs can have electrical characteristics that are on par with SoCs. Figure 20 shows a comparison of the signal transmission paths of SoCs and SiPs stacked with TSV. When a signal is transmitted from one end of an SoC chip to the opposite corner, the path is much shorter if the SoC is divided into nine parts and stacked with TSV.



**Monolithic chip**  
A single chip

**Chiplet**  
A technology that divides existing logic chips by function and connects them with TSV

Figure 21 Conceptual diagram of a chiplet

In addition to a focus on the various advantages of SiPs stacked with TSV, a technology called chiplets has gained a lot of attention recently. As shown in Figure 21, it is a technology that divides existing logic chips by function and connects them with TSV. Chiplets have three main advantages over monolithic chips.

First, the chiplets offer a yield improvement over monolithic chips. The wafer yield is limited if the size of a single chip on the wafer is big, but making the chips smaller can increase wafer yield and thus reduce manufacturing costs. Take the example of a 300 mm wafer cut into 100 or 1,000 chips (net die). If the wafer process causes five chips to fail because five impurities are evenly distributed across the front of the wafer, the product with 100 chips has a yield of 95% and the product with 1,000 chips has a yield of 99.5%. The yield is therefore much higher for products with more net dies, or with a smaller chip size. Therefore, it is more cost-effective to cut up a chip by functions and implement it as SiP rather than as a single chip through SoC.

The second advantage is streamlined development. With a single chip, the entire chip needs to be redeveloped in order to upgrade its functionality or apply the latest technology. However, dividing the chips can shorten the development period and make the process more efficient as only the chip with the relevant function needs to be upgraded or developed with the latest technology. For example, some of the segmented chips use the existing 20 nanometer (nm) technology, while others use the latest sub-10 nm technology to increase development efficiency.

The third benefit is the centralization of technological development. By dividing chips by function, it is not necessary to develop a chip for every function. Only the chips used for the core technology need to be developed, and everything else can be purchased or outsourced so companies can focus on developing their own core technologies.

Thanks to these advantages, major semiconductor companies are introducing chiplet-based semiconductor products or have added them to their roadmaps.

Following the previous episode that looked into the various conventional and wafer-level packaging technologies, we finished the roundup of packaging technologies and their distinct characteristics. While stacked packages and SiPs have come a long way in their development, semiconductor researchers will continue efforts to enhance the capability of these high-quality technologies with numerous functions that take up a minimal amount of space. These efforts are expected to increase the efficiency of the packaging process as a whole through the production of packages with advantages in size, functionality, and performance.

## Episode 5: Package Design and Analysis



In recent years, semiconductor packages have become increasingly complex which has led to a growing emphasis on design. The semiconductor package design process involves various engineers and industry players sharing information about materials, conducting feasibility tests, and optimizing characteristics of the package. Having explored the different types of packages [in the previous episode](#), this article will explain the stages of the semiconductor design process in detail and introduce the different analyses that ensure the packages act as high-quality interconnection platforms for semiconductors.

### The Process of Semiconductor Package Design

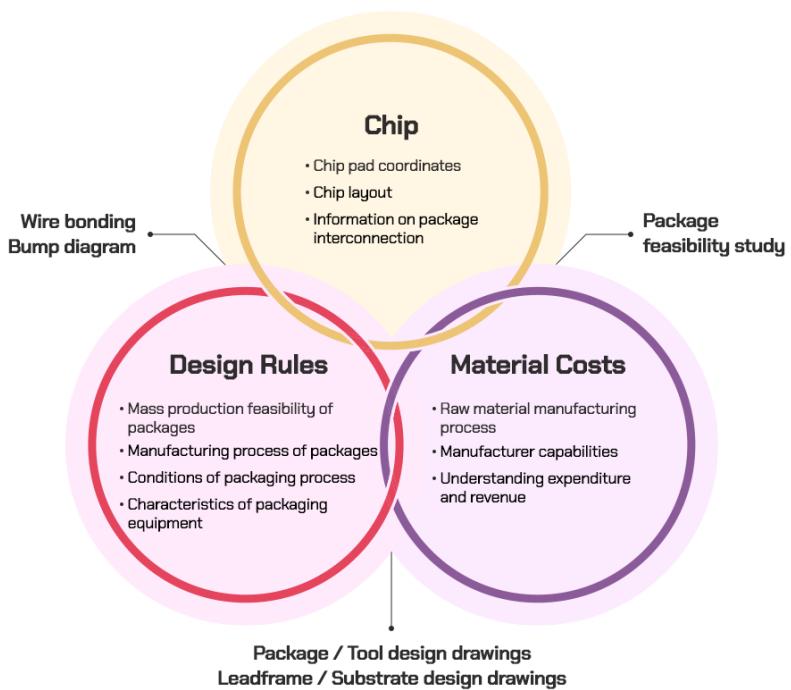


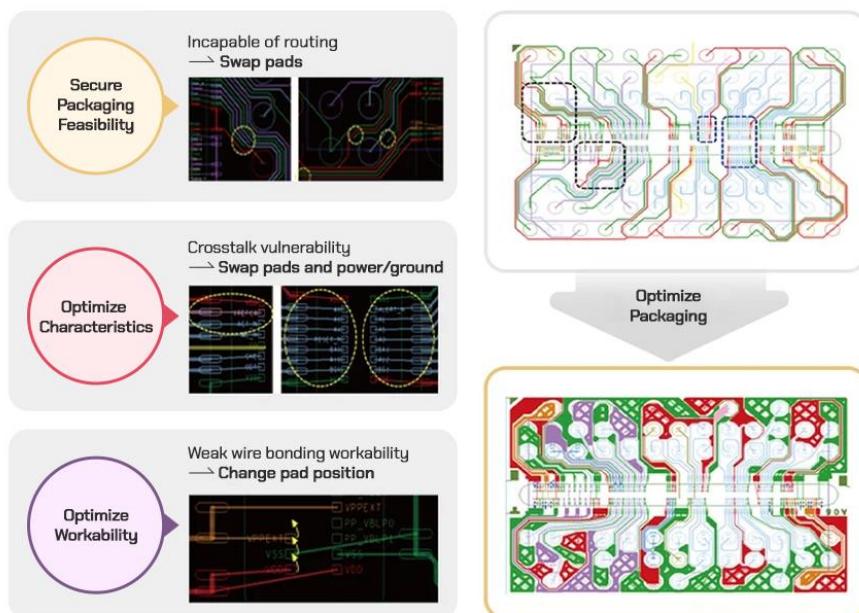
Figure 22 Aspects of semiconductor package design (Source: Hanol Publishing)

Figure 22 displays the various aspects of semiconductor package design. The design process begins with the department responsible for the chip design providing key information, including the chip pad coordinates, chip layout, and package interconnection data. Then, based on the packaging material, the team designs the structure of the semiconductor package which consists of the substrate and the leadframe. This process involves applying design rules that consider the package's mass production, manufacturing process, process condition, and required equipment.

The package's feasibility should be reviewed at the beginning of development and, afterwards, given to chip and product designers for feedback. Once the feasibility study is completed, orders must be placed to system semiconductor manufacturers with design drawings of the package, tools, leadframe, and substrate. While the wafers are being delivered to be packaged, tools, leadframe materials, and substrates on top of design drawings for the connection of wires or solder bumps need to be prepared. For the package process, design drawings for wire or solder bump connections must be shared in advance with package process and manufacturing engineers.

When these design drawings are shared, package design engineers conduct a feasibility test by connecting the package solder ball layout and the chip's pad sequence to check whether wiring is possible. Through the pre-feasibility phase, the engineers propose the package solder ball arrangement, package size, and specifications to improve the characteristics and process of the semiconductor chip and device.

### **Optimizing the Characteristics of the Package**



*Figure 23 The process of package design optimization (Source: Hanol Publishing)*

The package design optimization process is shown in Figure 23. The optimal pad placement is proposed in the initial stage of the package feasibility review before work is made on securing the possibility for wiring and optimizing characteristics as well as the workability of packages. To optimize these features, analyses of the structural, thermal, and electrical characteristics are performed.

Today, it is imperative to enhance all of these characteristics to meet the semiconductor industry's increasing demands for improvements in speed, integration, and performance. In the case of electrical characteristics, solder balls are created in the package to increase the number of pins connecting the package to the PCB board and more wiring is added. As a result, the designs of board substrates, leadframes, and PCBs are becoming finer and more complex. However, there are limits when manufacturing these devices related to the process capabilities of the packaging company and the manufacturers that produce components such as the substrate. In package design, therefore, design rules concerning materials, processes, and equipment are created, reviewed periodically, and shared between chip designers and manufacturers of substrates and packages in order to prevent quality issues.

By sharing the design rules, package process engineers and process engineers from substrate manufacturers may work together to reduce the size and pitch of package solder balls in addition to the width and spacing of the signal wiring. Likewise, design rules are used to specify items that range from process capabilities to electrical specifications. Additionally, the methods of managing the tolerance<sup>1</sup> of the package and substrate—as well as the package's process capabilities—are detailed in the design rules.

More specifically, the rules also manage the tolerance that satisfies the rigorous electrical specifications. To meet the electrical specifications, drawings are created based on pre-validated design data to manage and specify the tolerance of three areas in order: each high-speed signal line, the dielectric<sup>2</sup> thickness to manage the impedance<sup>3</sup> coherency of each signal line, and the via size<sup>4</sup> for an optimal low-power design. On the other hand, to improve the efficiency and mass production during the package process, the standard marking pattern is taken into account when designing devices like substrates and managed as a design rule.

<sup>1</sup> **Tolerance:** *The range of errors in space or values created from the difference of work capabilities.*

<sup>2</sup> **Dielectric:** *An electrical insulator that can be polarized by applying an electric field.*

<sup>3</sup> **Impedance:** *A measure of the extent to which a circuit opposes the flow of electricity.*

<sup>4</sup> **Via size:** *The size of holes used for electrical connection between different layers of a printed circuit board.*

## Analyzing the Packaging Structures

Computer simulation is used to analyze semiconductor packaging structures. Typically, analysis through computer simulation involves applying the derived general equations to specific conditions in order to understand a certain phenomenon. There are four steps involved in the standard computer simulation process.

First, factors that govern a natural phenomenon and the relationship between the factors are placed in mathematical expressions such as the governing equation<sup>5</sup>, and then the phenomenon that is the subject of analysis is modeled so that it can undergo computer simulation. Next, the governing equation is applied to the model to calculate it mathematically, and, finally, the result is applied to the phenomenon to analyze it. The methods of analysis through computer simulation are mainly divided into the finite difference method, finite element method (FEM), and finite volume method. FEM is most widely used to analyze semiconductor structures. The engineering aspect of FEM refers to its ability to convert infinite number of points and degrees of freedom<sup>6</sup> into finite number of points and degrees of freedom. These points are then computed as linear system of equations.

<sup>5</sup> **Governing equation:** *The mathematical formulae that form the basis of a computational code. For computational modeling, they govern the predicted behavior of fluids in the subsurface provided by the code.*

<sup>6</sup> **Degrees of freedom:** *The number of values in the final calculation of a statistic that are free to vary.*

FEM is composed of a finite number of building blocks called elements. Each element has a finite number of points and a governing equation, while a value is obtained by solving the equation. To understand structural analysis, it is essential to understand three key properties of materials that are required for such analysis: coefficient of thermal expansion (CTE), Poisson's ratio, and stress.

CTE is a property which describes the extent a material changes in length due to fluctuations in temperature. In general, a material expands as the temperature increases and it contracts as the temperature decreases. CTE is therefore defined as the fractional increase in the length of a material per unit rise in temperature. Meanwhile, Poisson's ratio is the expansion or contraction of a material in directions perpendicular to the specific direction of loading. To understand this ratio, it is helpful to consider the effect of pushing and pulling on an object. If you pull on an object lengthwise from both ends and apply a tensile force, it stretches in the direction of its length and contracts in the direction of its width. However, if you push it from both ends lengthwise and apply a compressive force, it will shrink in the direction of the force and stretch in the direction of its width. Lastly, stress is the internal force created within an object to resist an external force while maintaining its shape. It is measured in units of pressure.

These material properties are applied to the three main areas of structural analysis utilized in semiconductor packages: package warpage, solder joint reliability, and package strength.

### **Warpage Analysis**

When the temperature rises and goes back down to room temperature during the packaging process, the CTE between dissimilar materials may differ and cause the package to warp and create defects. Therefore, structurally analyzing the package based on the product structure, the material's elastic modulus<sup>7</sup>, the CTE, the process temperature, and time, makes it possible to predict warpage and prevent defects from occurring.

<sup>7</sup> **Elastic modulus:** A value that represents the stiffness of a material in solid mechanics. It is defined as the ratio of stress and strain.

### **Solder Joint Reliability**

Solders serve as mechanical and electrical connections between the semiconductor package and the PCB substrate. As the reliability of solder joints is very important, the joints should undergo structural analysis before a package is made in order to improve the package structure and materials.

Failure mechanisms in solders are primarily a combination of shear cracking caused by in-plane shrinkage and tensile cracking caused by axial tension. Therefore, structural analysis of solder joints is performed by analyzing the amount of stress applied to the solder joint under various process or usage conditions.

### **Strength Analysis**

As the package serves to protect the chip from external forces, the chip's robustness to external impacts is represented by the package strength. To determine the robustness of a package, a universal testing machine (UTM)<sup>8</sup> is used to perform three-point bending or four-point bending which calculate the breaking strength. Structural analysis simulates these UTM tests to deduce the stress levels in each area of the package and uses the breaking strength of a specific material as a reference to predict the breaking strength of the whole product.

<sup>8</sup> **Universal testing machine (UTM):** A tester that measures the strength of a material by pulling or compressing a material with a set weight to measure its tensile, flexural, and compressive strengths.

### **Heat Interpretation**

Electronic devices consume power and generate heat as they operate. This heat raises the temperature of components that include semiconductor products, which can compromise the functionality, reliability, and safety of electronic equipment. Therefore, electronic equipment must have proper cooling systems to keep the temperature of components below a certain level in any environment.

Thermal analysis, thus, becomes an essential test as heat dissipation is one of the crucial roles of semiconductor packages. Therefore, generated heat, the heat dissipation effect of the package material and structure, and the temperature effect when the semiconductor package is applied to the system must be accurately understood in advance to be reflected in the package design.

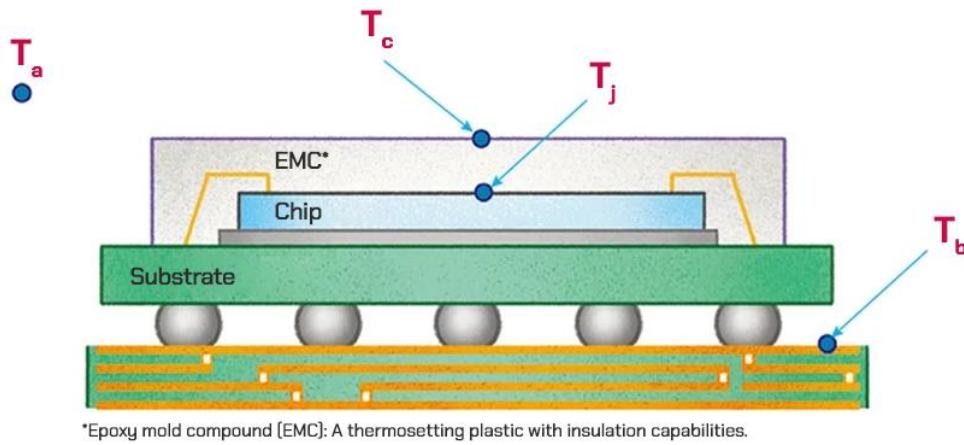


Figure 24 Key temperature points of the package (Source: Hanol Publishing)

In order to perform and utilize thermal analysis on a semiconductor package, it is necessary to define the key temperature points on the package. The main temperature points of the package are ambient temperature ( $T_a$ ), junction temperature ( $T_j$ ), case temperature ( $T_c$ ), and board temperature ( $T_b$ ). The temperature for package specifications is usually either  $T_j$  max. or  $T_c$  max., terms which refer to the maximum temperature that ensures the semiconductor device operates normally. Figure 24 shows each temperature point in the schematic diagram of a package.

Symbol	Name	Formula
$J_a$	Junction-to-ambient thermal resistance	$[T_j - T_a] / P$
$J_c$	Junction-to-case thermal resistance	$[T_j - T_c] / P$
$J_b$	Junction-to-board thermal resistance	$[T_j - T_b] / P$

P = Power consumption (W)

Figure 25 Types of heat characteristics in packages (Source: Hanol Publishing)

By using the main temperature points of the package, it becomes possible to calculate thermal resistance—the most important characteristic for heat protection. Package thermal resistance is an index expressed in units of °C/W which identifies the temperature increase of a semiconductor product in relation to the surrounding temperature when 1 watt of heat is generated by the chip. This ratio changes according to each product and the environmental conditions. Common types of thermal resistance include junction-to-ambient (Ja), junction-to-board (Jb), and junction-to-case (Jc), and they reveal indications such as the package's resistance and immunity to heat.

### Electrical Simulation

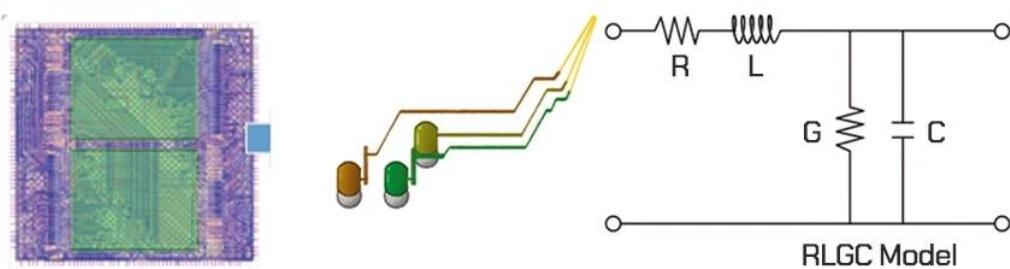
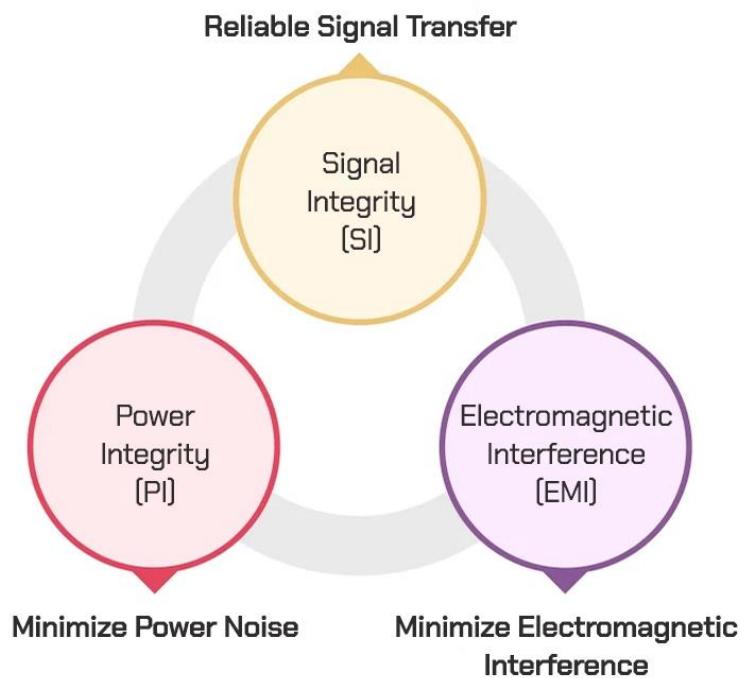


Figure 26 An example of a packaged RLGC model (Source: Hanol Publishing)

As semiconductor chips become faster and denser, packages also have a significant impact on the characteristics of semiconductor products. In particular, when a high-performance semiconductor chip is packaged, accurate electrical simulation of the package state is essential. To predict the electrical problems arising from the complex wiring of high-performance semiconductor chips, modeling such as RLGC is used. Thus, electrical simulation creates models and uses them to predict the timing of data transmission, the signal quality, and the shape accuracy in high-speed digital systems.

The basic elements of an electrical model for the electrical analysis of a package are resistance, inductance, and capacitance. Just strong enough to obstruct the flow of a current, resistance is inversely proportional to the unit current flowing on an object. Inductance is the ratio of counter electromotive force that forms from electromagnetic induction caused by a change in the current flowing in a circuit. Finally, as the physical quantity that shows how much charge can be stored, capacitance is the charge stored by a capacitor at unit voltage.



*Figure 27 Areas of electrical analysis (Source: Hanol Publishing)*

Using modeling such as RLGC, it becomes possible to predict the most important characteristics, namely signal integrity (SI), power integrity (PI) and electromagnetic interference (EMI) as shown in Figure 26. SI is the measure of an electrical signal's quality, while PI measures the power transmission's quality. Lastly, EMI is an electromagnetic disturbance where radiated or conducted electromagnetic waves interfere with the functioning of other devices. Thus, noise problems should be checked in advance to minimize the developing period and ensure that the integrity and power delivery system can support the creation of a reliable board. SI, PI, and EMI have a close and organic relationship with each other, so a comprehensive design that considers all three is essential for electrical analysis.

### **Supporting the Advancement of Semiconductors**

No matter how much individual chip performances improve, the overall system performance cannot be guaranteed unless the electromagnetic characteristics of the pathways connecting the chips on the package and the power supply grid are properly managed. The package design process and related analyses are therefore vital to ensuring the operation and continued advancement of chips. By following certain design rules, it is possible to create the blueprint for semiconductor packages with optimal characteristics. This optimization of a package's characteristics is then realized through structural, thermal and electrical analyses. Ultimately, these stages of design and analysis make it possible to meet the increasing demands for improvements in semiconductors' speed, integration, and performance.

## Episode 6: The Eight Steps of Assembling Conventional Packages



[In an earlier episode](#), it was established that the two main categories of semiconductor packages are conventional and wafer-level packages. Going forward, this series will focus on these package types and their differences in assembly methods and functions starting with this article which will cover conventional packages.

### Overview of Assembling Conventional Packages

Figure 28 shows the assembly process for plastic packages, which are a type of conventional package. Plastic packages are categorized into leadframe and substrate packages. The first half of the packaging process for these two packages is the same, but the second half differs in how the connection pins are applied.

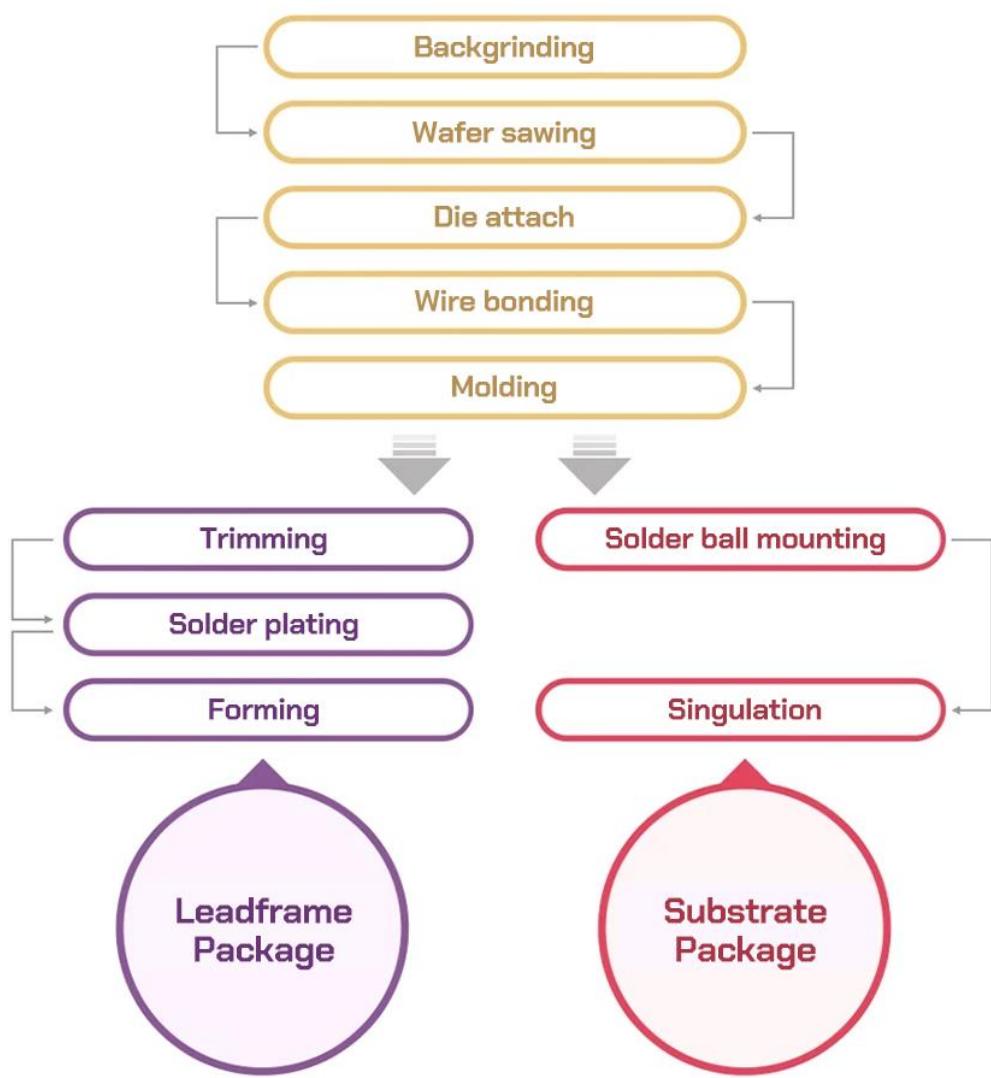


Figure 28 The steps of assembling leadframe and substrate packages (Source: Hanol Publishing)

Once the wafers are tested, they first go through backgrinding to become the desired thickness. Wafer sawing then follows so the wafers can be cut into chips. Afterwards, chips that are deemed to be of good quality are selected and attached to the leadframe or substrate through the die attach process. The chips are then electrically connected to the substrate through wire bonding before they are sealed with an epoxy molding compound (EMC) for protection. Both leadframe and substrate packages share these steps.

In the next stage, leadframe packages undergo several processes: trimming<sup>1</sup> that separates the leads, solder plating that applies solders to the ends of the leads, and, lastly, forming. The process of forming separates the packages into single units and bends the leads so they can be attached to the system board. As for substrate packages, they are molded before going through solder ball mounting where solder balls are attached to the substrate pads.

This is followed by a process of cutting and forming individual packages called singulation. In the following section, the process of assembling conventional packages with an emphasis on the eight steps of producing substrate packages will be explained.

<sup>1</sup> **Trimming:** A process applied to leadframe packages that removes the dambar, which connects the space between the leads, using a cutting punch.

### Step One: Backgrinding

The backgrinding process ensures a wafer is processed with the optimal thickness for its package's characteristics. This includes processing the wafer's back and mounting it to a ring frame, as shown in Figure 29.

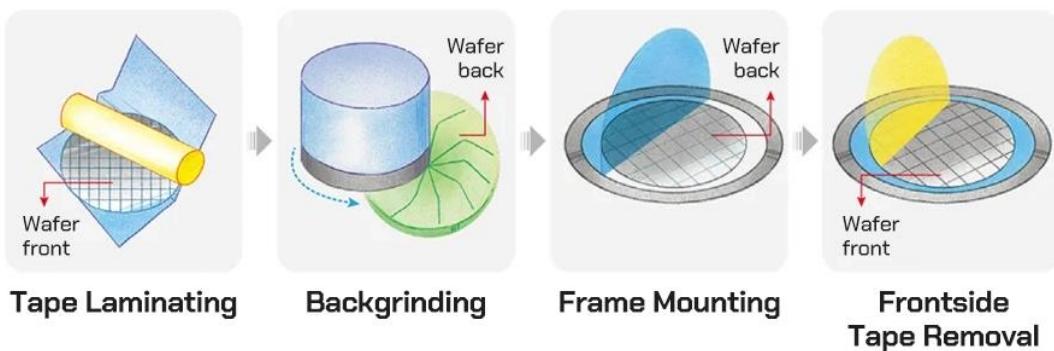


Figure 29 The four steps of the wafer backgrinding process (Source: Hanol Publishing)

Before grinding the backside of the wafer, a protective tape known as a backgrinding tape is laminated onto the wafer's front. This is to prevent physical damage to the frontside where the circuit was formed. Next, grinding wheels are applied to the backside of the wafer to make it thinner. A rough grinding wheel is first used at high speed to remove most of the excess material before a fine grinding wheel grinds more delicately and accurately to reach the wafer's target thickness. Afterwards, a fine pad is used for polishing to smooth the wafer's surface. If the wafer's surface is rough, cracks are more likely to occur when stress is applied during subsequent processes and result in the chip breaking. Therefore, it is crucial to reduce the chances of chip breakage by polishing that prevents the formation of cracks.

For packages consisting of a single chip, the wafer is generally grinded to a thickness of about 200 to 250 micrometers ( $\mu\text{m}$ ). As for stacked packages, the chips—and essentially the wafers as well—need to be even thinner as multiple chips are stacked on the package. However, the residual stress from grinding the wafer's backside causes shrinkage on the frontside and can potentially bend the wafer into the shape of a smile. Furthermore, the degree of bending becomes more severe as the wafer is thinned. To flatten out the wafer, mounting tape is first applied to the backside of the wafer and then it is attached to the ring frame. The backgrinding tape that was applied to protect the devices on the wafer's front is

then removed again, exposing the semiconductor devices to complete the backgrinding process.

### Step Two: Wafer Sawing/Dicing

Wafer sawing is the process of cutting along the scribe lanes<sup>2</sup> of a wafer in order to break it into chips or dies. Also referred to as the dicing process, wafer sawing is a necessary procedure of the packaging process for chips or dies.

Figure 30 shows an example of a wafer being broken into chips through blade dicing, a method of wafer sawing that uses a wheel-shaped saw blade to cut and separate wafers. This saw blade with a wheel tip strengthened through diamond grit cuts along the wafer's scribe lanes—the lattice-shaped lines of the wafer on the left of the figure. As the saw blade creates a working tolerance<sup>3</sup> when it rotates, the scribe lane must be thicker than the wheel.

<sup>2</sup> **Scribe lane:** A space of sufficient width designated for cutting a chip or die from a wafer without affecting nearby devices while allowing for the distribution of the cut pieces.

<sup>3</sup> **Tolerance:** The range of errors in space or values created from the difference of work capabilities.

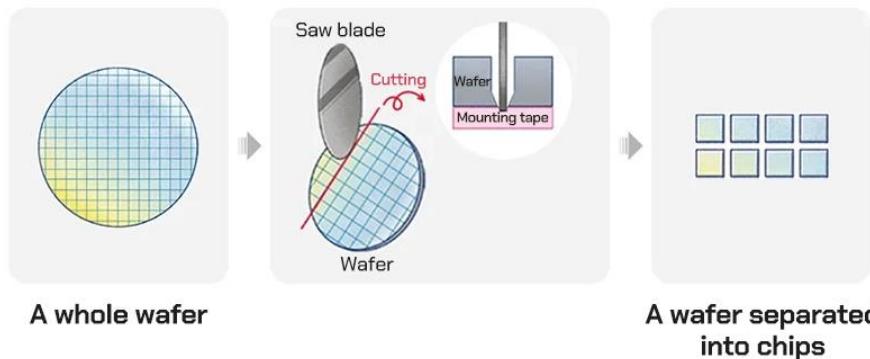


Figure 30 Sawing a wafer into chips through the blade dicing process (Source: Hanol Publishing)

One issue of blade dicing is that, as the blade physically contacts the wafers during the process, the wafers are more prone to breaking when they are requested to be made thinner. Laser dicing, another method of wafer sawing, resolves a lot of these issues as nothing physically contacts the wafer during the cutting process. Instead, a laser is shot from the back of the wafer during the dicing. Consequently, it is suitable for cutting thin wafers, while the chip remains robust due to the minimal damage to the wafer's surface.

As wafers have become thinner, there have been proposals to use dicing before grinding (DBG) which reverses the sequence of processes to reduce chip damage during wafer cutting. While the conventional process involves thinning the wafer by backgrinding before it is cut, DBG is a different method that partially cuts the wafer before it goes through backgrinding and completely cuts it off through mounting tape expand<sup>4</sup>.

<sup>4</sup> **Mounting tape expand (MTE):** Expansion of the mounting tape that is attached to the wafer after stealth dicing, a method of creating cracks in a wafer with a laser. Physical force is then applied to the relevant areas to break the wafer into chips.

### Step Three: Die Attach

As shown in Figure 31, die attach is the process of picking up the chips that have gone through the wafer cutting process from the mounting tape and attaching them to a substrate or leadframe that has been coated with an adhesive.

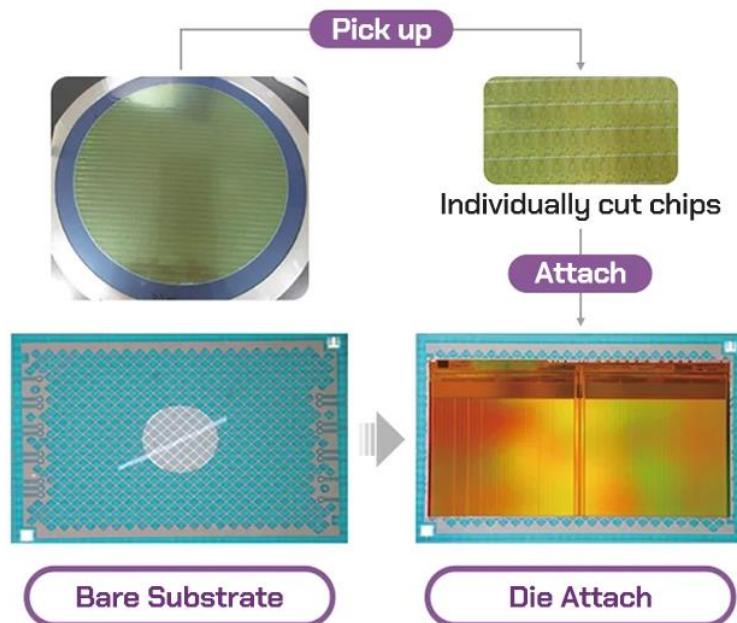


Figure 31 The die attach process (Source: Hanol Publishing)

During the wafer cutting process, the chip that has been cut should not fall off the mounting tape. However, in the attach process, the chip must be peeled off the mounting tape. As damage might be caused during the removal of the chip if the adhesion of the mounting tape is too strong, the adhesive should maintain a strong bond during wafer cutting and then weaken when it is exposed to ultraviolet light before the attach process. At this time, only chips that pass the wafer test are detached from the mounting tape.

While the removed chips must be reattached to the substrate with adhesive, there are differences depending on the type of adhesive used. If a liquid adhesive is used, it must be applied to the substrate in advance using a syringe-like dispenser or through stencil printing<sup>5</sup>. On the other hand, solid adhesives are usually in the form of a tape. Also known as die attach films (DAF) or wafer backside lamination (WBL) films, solid adhesives are especially preferred when chips need to be stacked. After backgrinding is complete, a DAF is attached between the mounting tape and the back of the wafer. When the wafer is cut, the

DAF is cut along with it. As the DAF and the chip attached to its back will fall off, the DAF can be glued on top of the substrate or chip.

<sup>5</sup> **Stencil printing:** A method of printing using a stencil mask to apply paste-type materials to devices such as substrates.

#### Step Four: Interconnection

Interconnection refers to the electrical connections between chips, chips and substrates, and other combinations within a package. The following section will introduce two interconnection methods: wire bonding and flip chip bonding.

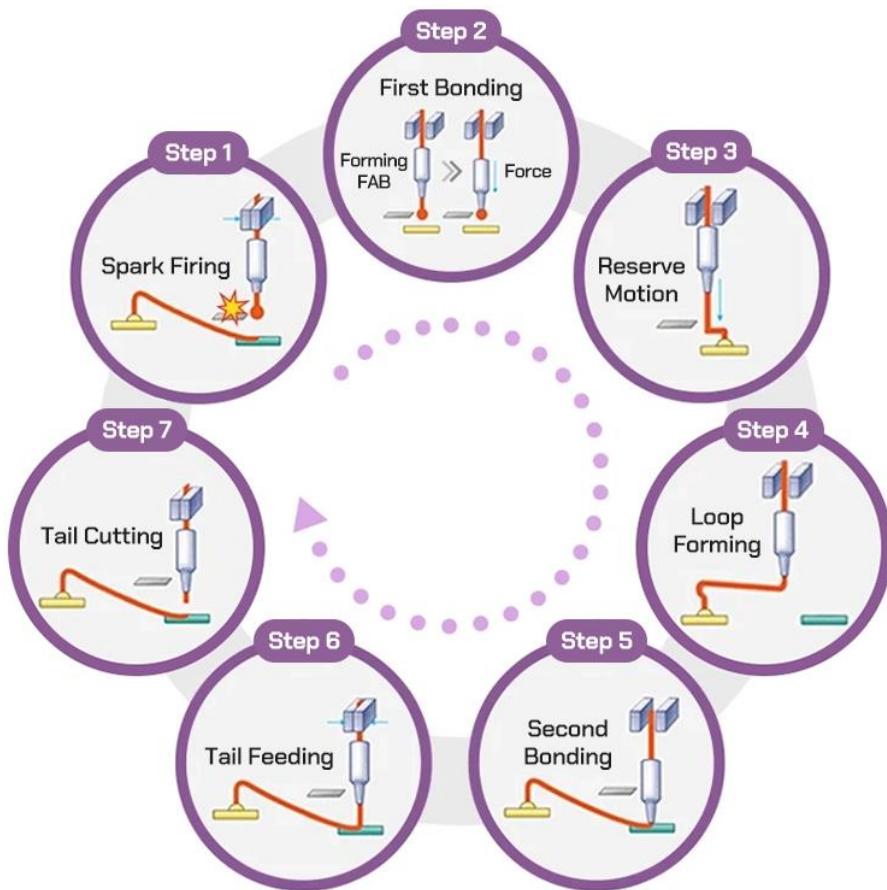


Figure 32 The seven steps of the wire bonding process (Source: Hanol Publishing)

#### Wire Bonding

Wire bonding uses heat, pressure, and vibration to electrically connect chips and substrates with metal wires. The wires are usually gold (Au) as they have good electrical conductivity and ductility. Wire bonding can be compared to sewing where the thread is the wire and the needle is the capillary<sup>6</sup>. The wire is rolled up onto a spool like a yarn and equipped to the machinery before it is pulled out and passed through the center of the capillary to form the tail at the end of the capillary. When the electronic flame-off (EFO)<sup>7</sup> gives a strong electrical

spark to the wire's tail, that part melts and solidifies to form a free air ball (FAB) that is essentially caused by surface tension.

After the FAB is created, it is attached to the chip's pad with force to form ball bonding. When the capillary is moved toward the substrate, the wire comes out like a thread to form a loop. Stitch bonding<sup>8</sup> is formed by pressing the wire against the bond finger—the part of the substrate that will make the electrical connection. The wire is then pulled back even more to form a tail, and the connection between the chip and the substrate made with wiring becomes complete after the tail is cut. This procedure is repeated on the other chip pads and the substrate's bond fingers during the wire bonding process.

<sup>6</sup> **Capillary:** A tool used in wire bonding machines to connect chip electrodes and lead terminals with wires.

<sup>7</sup> **Electronic flame-off (EFO):** A process which melts a wire tip by an electrical spark to form a FAB.

<sup>8</sup> **Stitch bonding:** The bonding of wires to a pad during the semiconductor packaging process by pressing and attaching the wires.

### **Flip Chip Bonding and Underfill**

Flip chip bonding creates a bump on top of the chip to make an electrical and mechanical connection with the substrate. Therefore, it has better electrical properties than wire bonding. There are two types of flip chip bonding: the mass reflow (MR) process and thermocompression. MR attaches the chip with the substrate by melting the junction's solder at a high temperature. The thermocompression process, on the other hand, applies heat and pressure to the juncture to make the connection between the chip and substrate.

Since the stress caused by the difference in the coefficient of thermal expansion<sup>9</sup> (CTE) between the chip and the substrate cannot be handled by the bump alone, an underfill process that fills the space between bumps with polymer is necessary to ensure solder joint reliability. There are two main underfill processes to fill up the space between bumps: post-filling, which fills the materials after flip chip bonding, and pre-applied underfill, which fills the materials before flip chip bonding. Additionally, post filling can be divided into capillary underfill (CUF) and molded underfill (MUF) depending on the underfill method. After flip chip bonding is applied, CUF fills in the gaps between bumps by using the capillary to inject underfill material into the side of the chip. As for MUF, it allows EMC to function as an underfill by using it to fill up the spaces between bumps.

<sup>9</sup> **Coefficient of thermal expansion (CTE):** A material property that indicates the extent to which a material expands upon heating.

## **Step Five: Molding**

Once the chip is wire bonded or flip chip bonded, it needs to be encapsulated to protect the structure from external impact. Such protection processes include molding, sealing, and welding, but only molding is used for plastic packages. The process of molding encloses EMC, which mixes thermosetting resin<sup>10</sup> with several inorganic materials, around parts including chips and wires to protect them from physical and chemical external impacts and to create the desired package size or shape.

*<sup>10</sup> Thermosetting resin: A stable polymer material that undergoes a polymerization reaction when heated to harden and form a polymer compound. It is primarily used for EMC that protects the electronics and electrical properties of semiconductor circuits by preventing thermal and mechanical damage in addition to corrosion.*

The molding process takes place in a mold. For transfer molding, a substrate with chips connected by wire bonding is placed on both molds while an EMC tablet is placed in the middle and heat and pressure is applied. This liquidizes the solid EMC to flow into both molds and fill up the space. Transfer molding faces challenges when the gap between the chip and the top of the package gets smaller as it becomes more difficult to be filled with a liquid such as EMC. Furthermore, when the substrate gets bigger, the mold has to increase in size accordingly and it therefore becomes harder for EMC to fill the space.

In recent years, the process of transfer molding reached its limits. As the number of chip stacks has increased while a package's thickness has generally decreased, the gap between the chip and the top of the package has continued to shrink. The size of the substrate is also growing as more chips are being processed in large batches to lower manufacturing costs. For this reason, compression molding has emerged as the solution to filling the small gap. In compression molding, the mold is pre-filled with EMC powder. When heat and pressure are applied after the substrate is placed in the mold, the EMC powder filled in the mold liquidizes and is eventually molded. In this case, the EMC immediately becomes liquid and fills the space without flowing, so there is no problem filling the small gap between the chip and the top of the package.

## **Step Six: Marking**

Marking is a process of engraving product information such as the semiconductor type or manufacturer, in addition to patterns, symbols, numbers, or letters requested by the customer, on the surface of semiconductor packages. This proves to be important when a semiconductor product fails to operate after it is packaged as the markings can assist in tracing the cause of the product's failure. Markings can either be engraved by burning materials such as EMC with a laser or by embossing using ink.

For plastic packages, they need to be molded before the requested information is displayed on the surface. Since laser marking is simply the act of engraving, a black EMC is usually the

preferred choice as it increases the legibility of the markings. This is because color cannot be applied to the engraved characters or symbols, so it is more visible to have engravings on a black background. The remaining two steps will cover the final stages of packaging substrate packages. This is where the difference lies between the processes of substrate and leadframe packages.

### Step Seven: Solder Ball Mounting

Solder balls in a substrate package do not only serve as an electrical pathway between the package and external circuitry, but they also provide mechanical connections. Solder ball mounting is the process of attaching a solder ball to a substrate pad. In the first step of the process, flux<sup>11</sup> is applied to the pad and then the solder balls are placed on the pad. Then, the reflow process melts and attaches the solder balls before the flux is washed and removed. The role of the flux here is to remove impurities and oxides from the surface of the solder balls during the reflow process. This allows the solder balls to melt uniformly and provides a clean surface. When these melted solder balls flow into a stencil on the substrate, they fill each hole in the stencil. Then, the substrate and stencil are separated but the solder balls remain on top of the substrate due to the adhesion of the flux. As there will be flux that has already been applied to the pad, the solder balls will be temporarily adhesive and attach to the pad.

<sup>11</sup> **Flux:** A water-soluble and oil-soluble solvent that makes solder balls adhere well to the copper of the ball land.

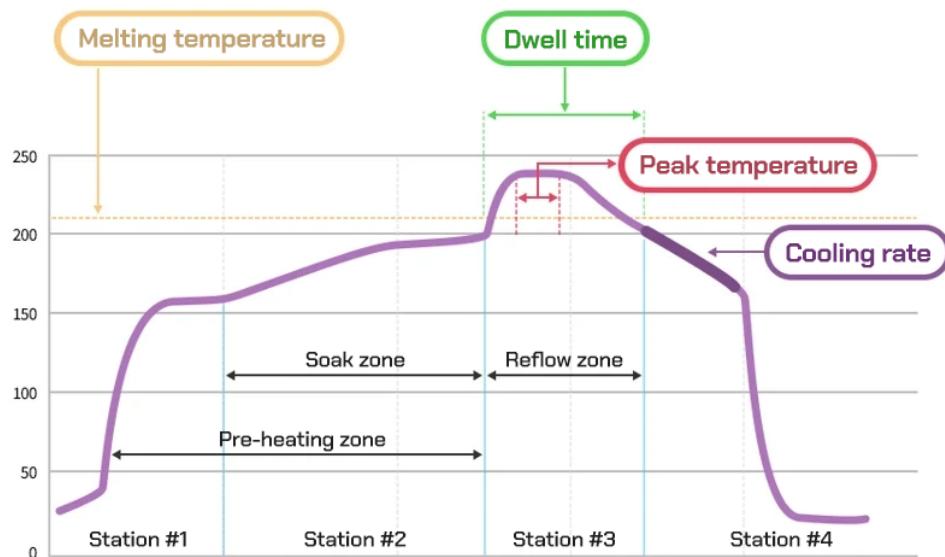


Figure 33 The temperature profile applied during the reflow process (Source: Hanol Publishing)

The solder balls attached to the substrate pad with flux melt through the reflow process. Figure 33 shows the temperature profile applied during this process. The flux is activated in the soak zone before the solder reaches its melting temperature, removing oxides and impurities from the surface of the solder balls. While the solder balls melt and attach to the pad when it is above the melting temperature, they do not flow off completely. Instead, they form a globular shape caused by surface tension in all areas except the parts where they adhere to the metal part of the pad. As the temperature decreases, they retain their shape and solidify again.

### **Step Eight: Singulation**

Singulation is the final process of creating a substrate package. The process involves using a blade to cut the finished substrate strips into individual packages. Once the singulation process is complete, the packages are placed on a tray for package testing and the rest of the process steps.

The various steps involved in assembling conventional packages highlight how factors such as precise alignment, optimal electrical connections, and robust protection against external damages are integral to their formation. In the next episode, wafer-level packages—the other main type of semiconductor packages—will be explored in detail.

## Episode 7: The Wafer-Level Packaging Process



### Semiconductor Back-End Process Episode 7 The Wafer-Level Packaging Process

Following on from [the previous article](#) which summarized the assembly process for conventional packages, this article will be the first of two episodes which focuses on the other main form of semiconductor packaging—wafer-level packaging (WLP). In particular, it will cover the five fundamental processes involved in WLP including photolithography, sputtering, electroplating, photoresist (PR) stripping, and metal etching.

#### Packaging With a Fully Intact Wafer

WLP refers to the process that is performed before the wafer is diced. It generally includes fan-in wafer-level chip scale packaging (WLCSP) and fan-out WLCSP in which the entire process is performed while the wafer is still fully intact. Nevertheless, redistribution layer (RDL) packaging, flip chip packaging, and through-silicon via<sup>1</sup>(TSV) packaging are also generally categorized as WLP even if only a part of their processes are performed before the wafer is diced. Depending on which of these types of packages is used, there are variations in the type of metal and pattern formed by electroplating<sup>2</sup>. However, they all follow a similar sequence during packaging as described below.

<sup>1</sup> **Through-silicon via (TSV)**: A type of vertical interconnect access (via) that completely passes through a silicon die or wafer to enable the stacking of silicon dice.

<sup>2</sup> **Electroplating**: A reaction where oxidation occurs at the positive plate to produce electrons which are transmitted to a wafer with a solution that has metal ions that are negative plates to become metal.

After wafer testing is performed, a dielectric layer is created on the wafers as needed. The dielectric layer then exposes the chip pad again, following the first exposure during testing, with photolithography.

Afterwards, a metal layer is applied on the surface of the wafer through sputtering<sup>3</sup>. This metal layer enhances the adhesion of the electroplated metal layer that will be formed and acts as a diffusion barrier to prevent the development of chemicals within metals. It also functions as a pathway for electrons during the electroplating process, and applies photoresist to create an electroplating layer while a pattern is created through photolithography. A thick metal layer is then formed by electroplating. When electroplating is completed, the next step is to proceed with the PR stripping process while the remaining thin metal layers are removed by etching. As a result, the electroplated metal layers are formed on top of the wafers in the desired patterns. This pattern serves as the wiring for fan-in WLCSP, the pad redistribution in RDL packaging, and the bumps in flip chip packaging. The following sections will take a closer look at each of these processes.

<sup>3</sup> **Sputtering:** A process in which plasma ions physically collide with a target and removes the target's material so it can be deposited onto the wafer.

## The Fan-In Wafer-Level Chip Scale Packaging (WLCSP) Process

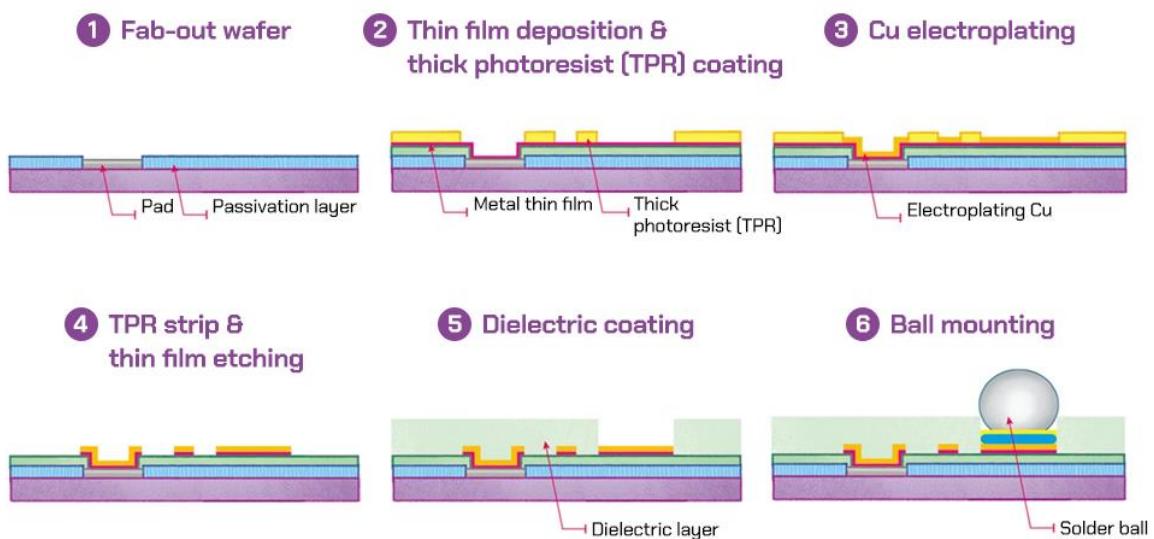
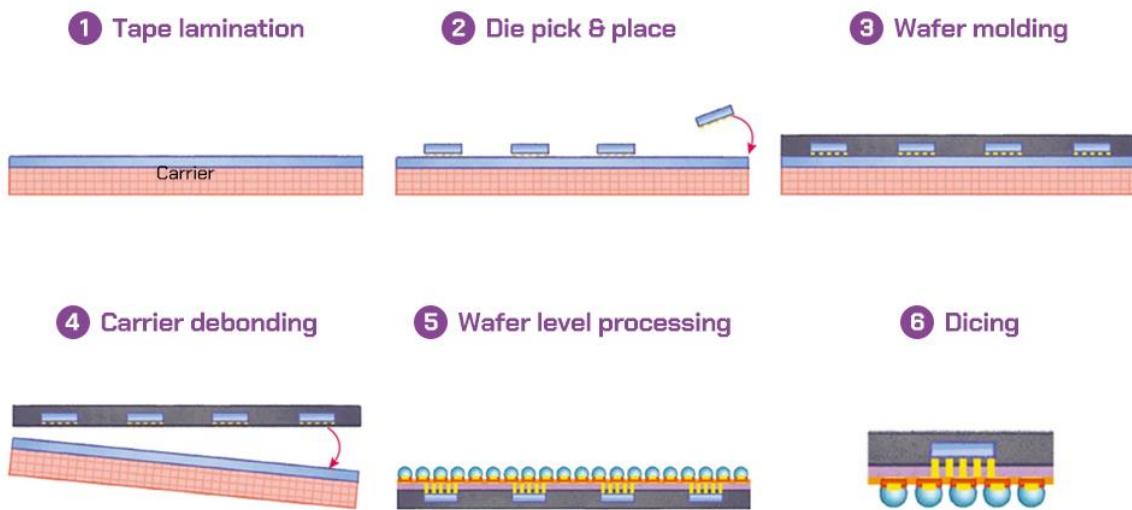
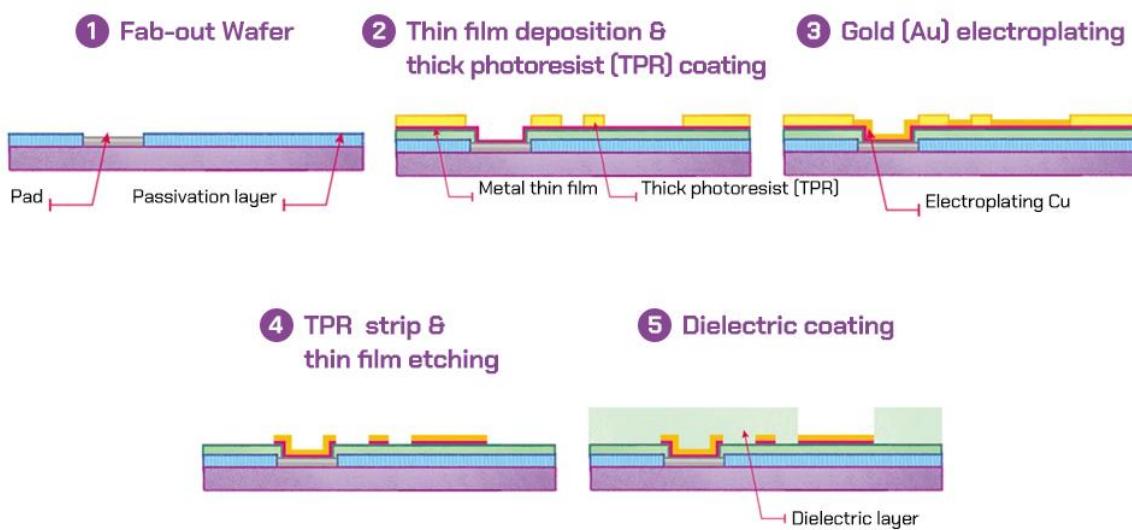


Figure 34 The steps involved in various wafer-level packaging processes

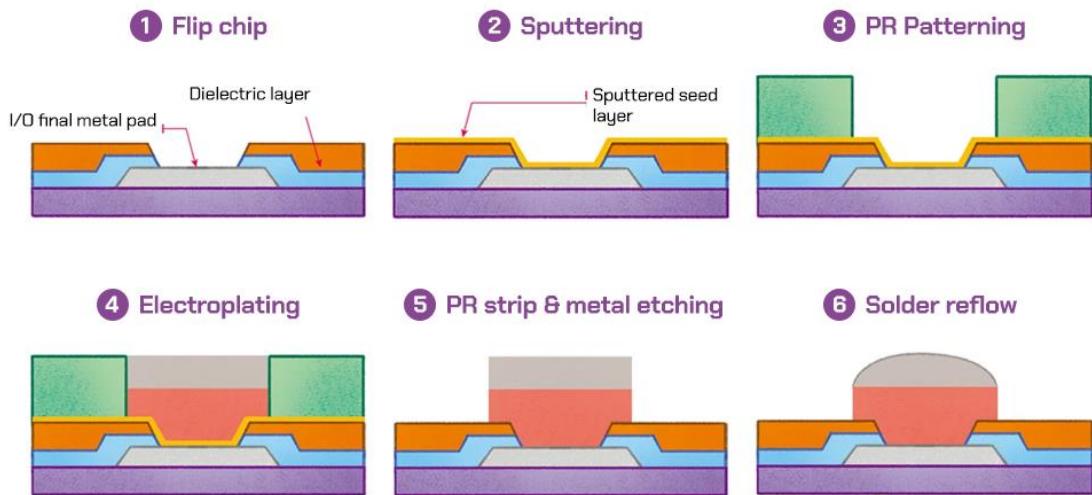
## The Fan-Out Wafer-Level Chip Scale Packaging (WLCSP) Process



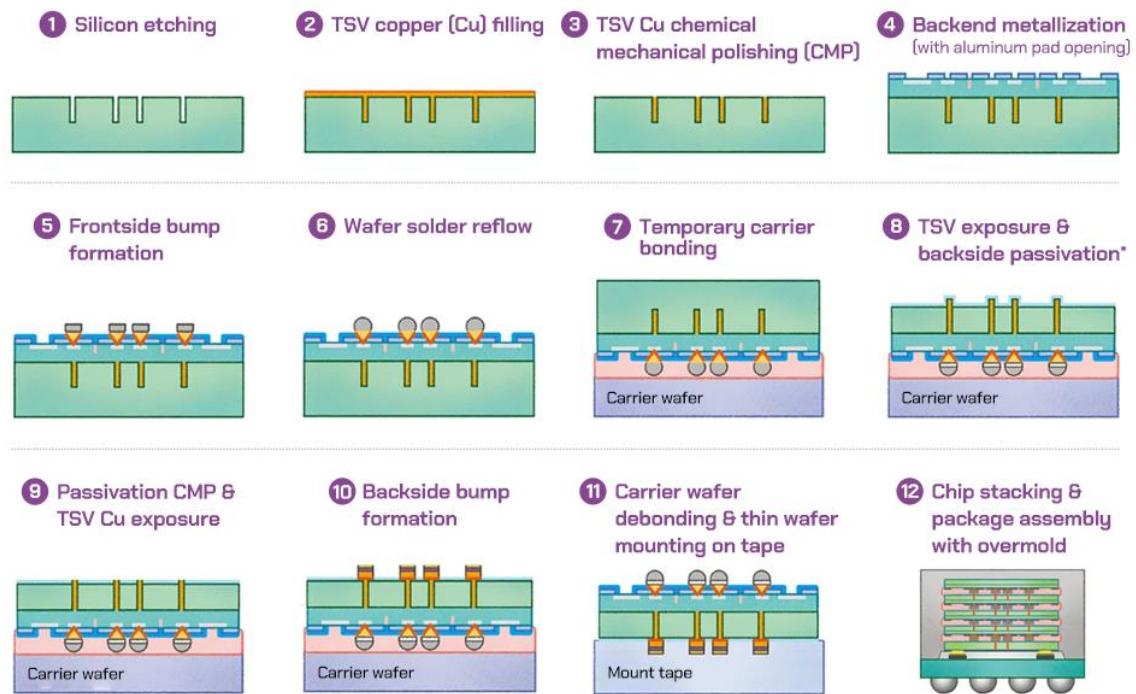
## The Redistribution Layer (RDL) Packaging Process



## The Flip Chip Packaging Process



## The Through-Silicon Via (TSV) Packaging Process



\*The process by which a semiconductor surface is coated to render it inert and remove any imperfections which can impact performance.

## Photolithography: Sketching Patterns on a Masked Wafer

Photolithography, a combination of “-litho” (stone) and “graphy (drawing),” refers to a printing technique. In other words, photolithography is a patterning process in which a photosensitive polymer called a photoresist is applied to the wafer and selectively exposed to light through a mask that has a desired pattern on it. The areas that are exposed to light are developed, and the required pattern or shape is created. The sequence of this process is shown in Figure 35.

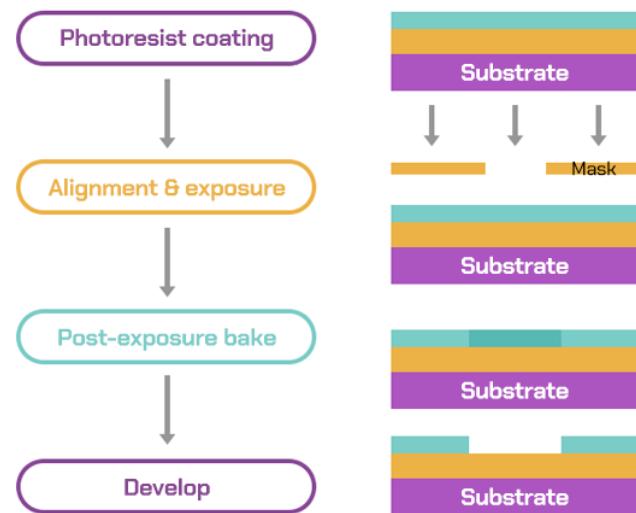


Figure 35 The steps of photolithography

In WLP, photolithography is primarily used to form patterns on dielectric layers, to create an electroplated layer by photoresist patterning, and to create metal wiring by etching diffusion layers.

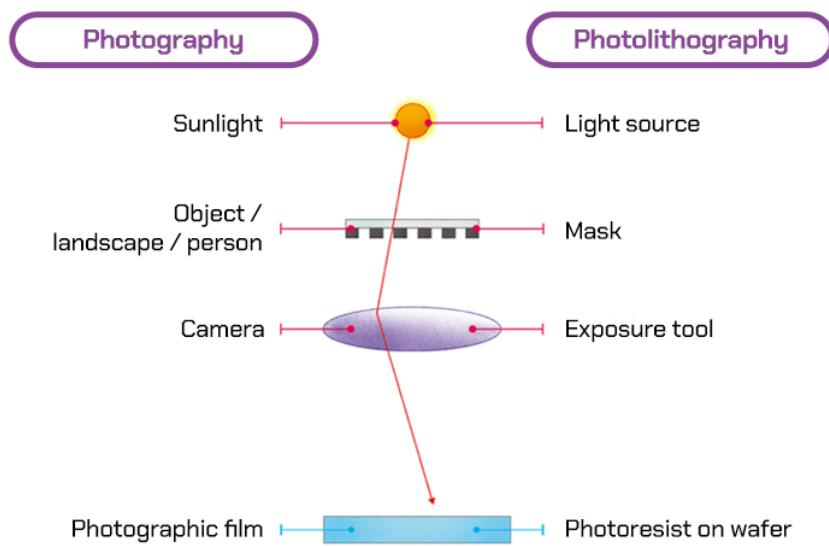


Figure 36 A comparison of photography and photolithography

To understand photolithography more clearly, it will be helpful to compare it with photography. As shown in Figure 36, photography uses sunlight as its light source to capture a photo of its subject, which could be an object, landscape, or a person. On the other hand, photolithography requires a specific light source to transfer patterns on a mask to an exposure tool. Lastly, the role of the film in a camera is equivalent to the photoresist that is applied to a wafer during photolithography. Consequently, there are three methods to apply a photoresist on the wafer as shown in Figure 37. They consist of spin coating, film lamination, and spray coating. After applying the photoresist, soft baking is performed to remove solvents to ensure that the viscous photoresist remains on the wafer and maintains its thickness.

As shown in Figure 38, spin coating places viscous photoresist onto the center of a spinning wafer so the photoresist is spread towards the edges due to centrifugal force. This makes the photoresist form a uniform thickness on the wafer. If the viscosity of the photoresist is high while the spin speed is low, the photoresist will be applied thickly. Conversely, if the viscosity is low and the spin speed is high, it is applied thinly. In the case of wafer-level packages, especially flip chip packages, they require a photoresist layer with a thickness ranging from 30 to 100 micrometers ( $\mu\text{m}$ ) to form solder bumps. However, it is not easy to achieve the desired thickness in a single spin coating. In some instances, it is necessary to repeat the application of photoresist and soft baking more than once. Accordingly, when a thick photoresist is required, it is effective to use lamination as it makes the film the desired photoresist thickness from the start. It is also more cost-effective because there is no waste from the wafer during processing. However, if there are rough surfaces on the wafer's structure, it can be difficult to adhere the film to the wafer which can lead to defects. For wafers that have very rough surfaces, a uniform thickness of photoresist can be achieved through spray coating.



Figure 37 The three methods to apply photoresist

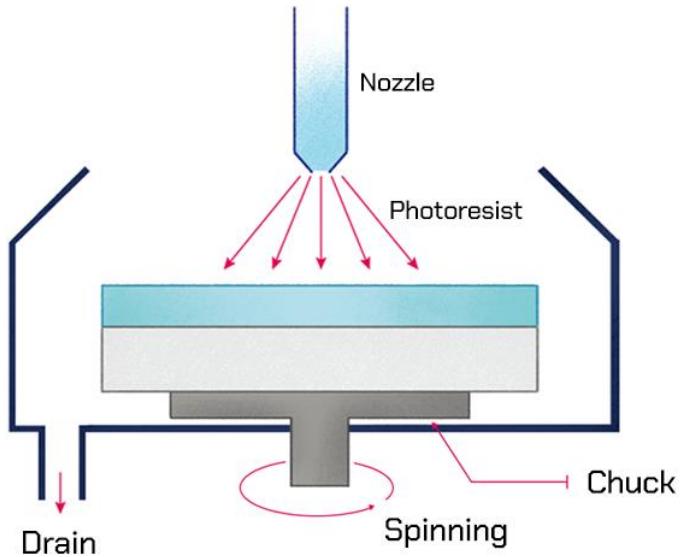


Figure 38 An overview of spin coating

After the photoresist is coated and soft baked, the next step is to expose it to light. By shining light through a pattern formed on the mask, the photoresist on the wafer receives the image of the pattern. When using a positive photoresist that weakens when exposed to light, the mask needs to have holes in areas that are going to be removed. However, when using a negative photoresist that hardens when exposed to light, the mask must have holes in the areas that need to remain. For WLP, a mask aligner<sup>4</sup> or a stepper<sup>5</sup> is typically used as the process equipment for photolithography.

<sup>4</sup> **Mask aligner:** One of the exposure tools that aligns the pattern on the mask and the wafer so that light can pass through them simultaneously.

<sup>5</sup> **Stepper:** A machine where the stage moves in steps and photolithography is performed by a shutter that opens and closes to allow light to pass through.

Development is the process of dissolving the parts of the photoresist that have been weakened through photolithography with a developer solution. As shown in Figure 39, there are three types of development: puddle development that pours the developer onto the center of the wafer so it spins at a low speed, tank development that immerses multiple wafers in the developer at the same time, and spray development that sprays the developer onto the wafer. Figure 40 shows an overview of a chamber for puddle development. After the puddle development is finished, the photoresist takes on the desired pattern through photolithography.



Figure 39 Three different methods of development

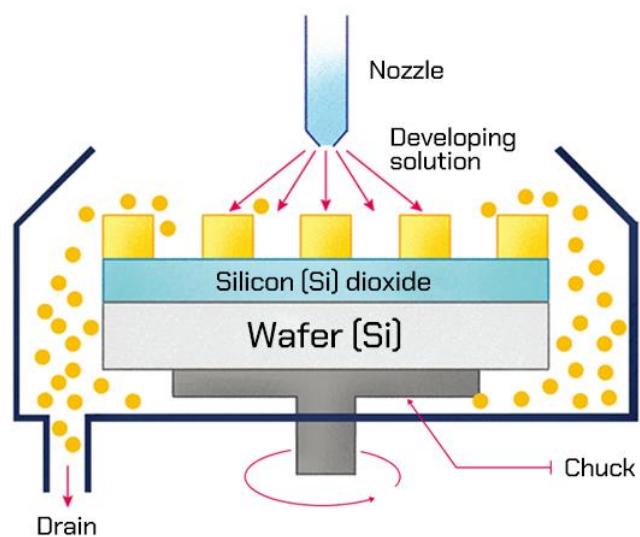


Figure 40 An overview of a chamber for puddle development

### Sputtering: Forming Thin Films on the Wafer

The process of sputtering is a type of physical vapor deposition<sup>6</sup> (PVD) that forms a thin film of metal on a wafer. If the metal film formed on the wafer is below the bumps as seen in flip chip packages, it is called an under bump metallurgy (UBM). Typically, it is in the form of two or three layers of metal film, including an adhesion layer, a current carrying layer that provides electrons during electroplating, and a diffusion barrier with solder wettability<sup>7</sup> that suppresses the formation of compounds between the plating layer and the metal. If the layers are comprised of titanium, copper, and nickel, the titanium acts as the adhesion layer, the copper acts as the current carrying layer, and the nickel acts as the diffusion barrier. Accordingly, the UBM has a significant impact on the quality and reliability of flip chip packages. As for metal layers like an RDL and a WLCSP that are used to form metal wiring, they usually consist of an adhesion layer and a current carrying layer that improves adhesion.

As Figure 41 shows the sputtering process, it starts with argon gas transforming into plasma<sup>8</sup> and colliding with a target that has the same composition as the metal on which positive argon ions will be deposited. The impact of the collision removes the metal particles from the target so they are deposited on the wafer. The metal particles deposited by sputtering have a consistent directionality. Even though a flat plate is deposited with a uniform thickness, plates in the shape of a trench or vertical interconnect access (via) can have different results. Such irregular shapes can make the deposition thickness of the wall's surface that is parallel to the metal deposition become thinner than the plate's floor that is perpendicular to the metal deposition.

<sup>6</sup> **Physical vapor deposition (PVD):** A process used to produce a metal vapor that can be deposited on electrically conductive materials as a thin and adhesive pure metal or alloy coating.

<sup>7</sup> **Wettability:** The phenomenon where a liquid spreads on the surface of a solid due to the interaction between the liquid and the solid surface.

<sup>8</sup> **Plasma:** A state of matter that is electrically neutral due to the coexistence of freely moving protons and electrons. When heat is continuously applied to a gaseous substance to raise its temperature, a collection of particles consisting of ions and free electrons is created. It is also called the "fourth state of matter" in addition to solid, liquid, and gas.

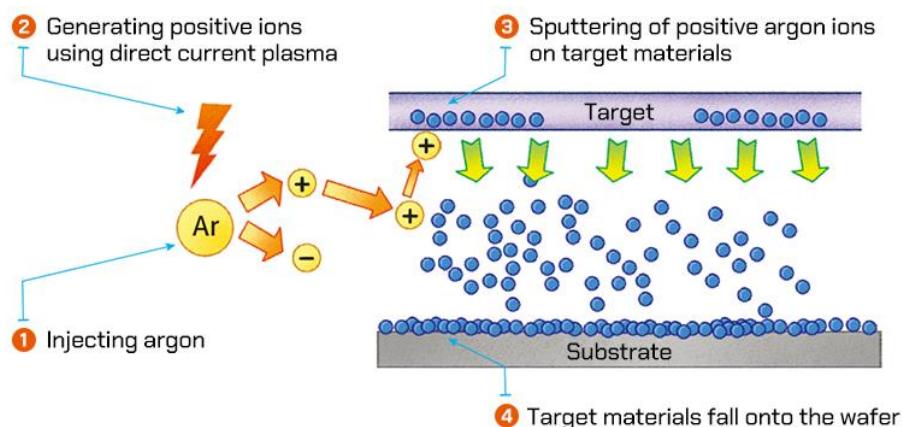


Figure 41 The fundamentals of sputtering

## Electroplating: Forming Metal Layers to Bond

Electroplating is the process of depositing metal ions of an electrolyte solution as metal on a wafer. This is possible through a reduction reaction using externally supplied electrons. In WLP, electroplating is used to form thick metal layers such as metal wiring for electrical connections or bumps for junctures. Just as Figure 42 illustrates, a metal undergoes oxidation at the anode to become an ion and releases electrons to the external circuit. The metal ions oxidized at the anode or present in the solution receive electrons and undergo a reduction reaction to become metal. In the electroplating process for WLP, the cathode plate becomes the wafer. The anode plate is made of the metal to be plated, but it also uses an insoluble electrode<sup>9</sup> such as platinum. If the anode plate is made of the metal to be plated, metal ions are dissolved from the anode plate and continuously distributed to maintain a consistent ion concentration in the solution. However, if an insoluble electrode is used, metal ions expended while being plated on the wafer must be periodically replenished in the solution to maintain the ion concentration. Figure 43 below shows the electrochemical reactions that occur at the cathode and anode, respectively.

<sup>9</sup> **Insoluble electrode:** An electrode used primarily in electrolysis and plating. It is neither chemically nor electrochemically soluble. Materials such as platinum are used for its creation.

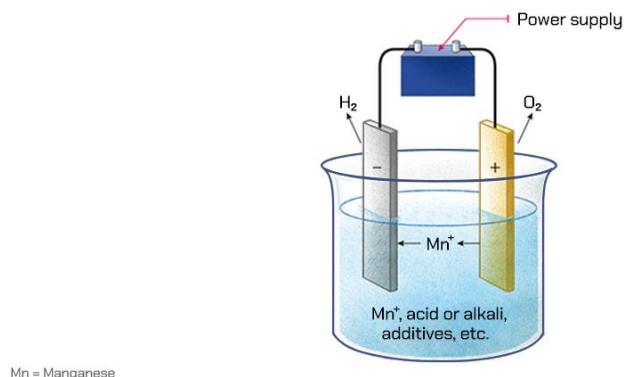


Figure 42 The process of electroplating

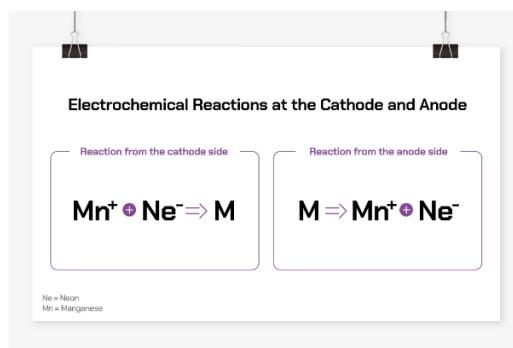


Figure 43 Electrochemical reactions at the cathode and anode expressed as formulae

The equipment that electroplates a wafer is typically placed so the side of the wafer to be plated faces down while the anode is positioned below the solution. Electroplating happens when the solution flows toward the wafer and forcefully collides with the surface. At this point, patterns formed from photoresist can come into contact with the solution on the parts of the wafer to be plated. Electrons are distributed through the electroplating equipment at the edge of the wafer and eventually meet the metal ions in the solution at the patterned parts. They then combine with metal ions inside the solution where the patterns are formed to go through a reduction reaction and grow to form metal wiring or bumps.

### **PR Stripping and Metal Etching: Removing the Photoresist**

Once the processes that use the photoresist pattern are complete, the photoresist must be removed via PR stripping. PR stripping is a wet process that uses a chemical solution called a stripper, and implements development methods such as puddle, tank, or spray. After a process like electroplating forms metal wiring or bumps, the metal film formed by sputtering must also be removed. This is necessary as the entire wafer will be electrically connected and result in a short circuit if the metal film is not taken off. The metal film is removed by wet etching with an acid-based etchant that can dissolve the metal. While the technique is similar to PR stripping, puddle development has been used more widely as metal patterns on the wafer have become finer.

### **A More Efficient and Reliable Packaging Process**

WLP strives for efficiency, miniaturization, and reliability through the above mentioned stages that begin with sketching patterns through photolithography and culminate in removing the applied photoresist through PR stripping. The next episode will look into the different types of WLP that use technologies such as fan-in and fan-out WLCSP, RDL, flip chip, and TSV.

## Episode 8: Exploring the Process Stages of Different Wafer-Level Packages



### Semiconductor Back-End Process Episode 8 The Process Stages of Wafer-Level Packages

Following an introduction to the basic process of assembling a wafer-level package in [the previous episode](#), this article will go over the multiple process stages of different types of wafer-level packages. These include the fan-in wafer-level chip-scale package (WLCSP), fan-out WLCSP, redistribution layer (RDL) package, flip chip package, and through-silicon via (TSV) package. Additional wafer-level processes that are applied in these packages such as photolithography, sputtering, electroplating, and wet processes will also be explained.

#### Fan-in Wafer-Level Chip-Scale Package (WLCSP) Process

In a fan-in WLCSP, a tested wafer enters the packaging line and a layer of metal film is created using sputtering. A thick layer of photoresist is then applied to the metal film as the photoresist must be thicker than the metal wiring used for packages. Photolithography is used to form patterns on the photoresist, and these exposed areas are copper electroplated to form the metal wiring. Next, the photoresist is stripped, and the excess thin metal film is removed using chemical etching. A dielectric layer is then formed on top, and photolithography is used to remove only the areas where the solder balls will be placed. Thus, this layer is also referred to as “solder resist.” It serves as the WLCSP’s passivation layer, or final protective layer, and distinguishes the area where the solder ball will be placed. Without this layer, solder balls would continue to melt on top of the metal layer and would not retain their globular shape when they are attached using methods such as reflow soldering.

Solder balls are attached to the dielectric layer through solder ball mounting after the layer forms a pattern through photolithography. Once the solder balls are mounted, the packaging process is complete and individual fan-in WLCSPs can then be created by dicing the wafer.

## Solder Ball Mounting Process

### Wafer-Level Reflow Equipment

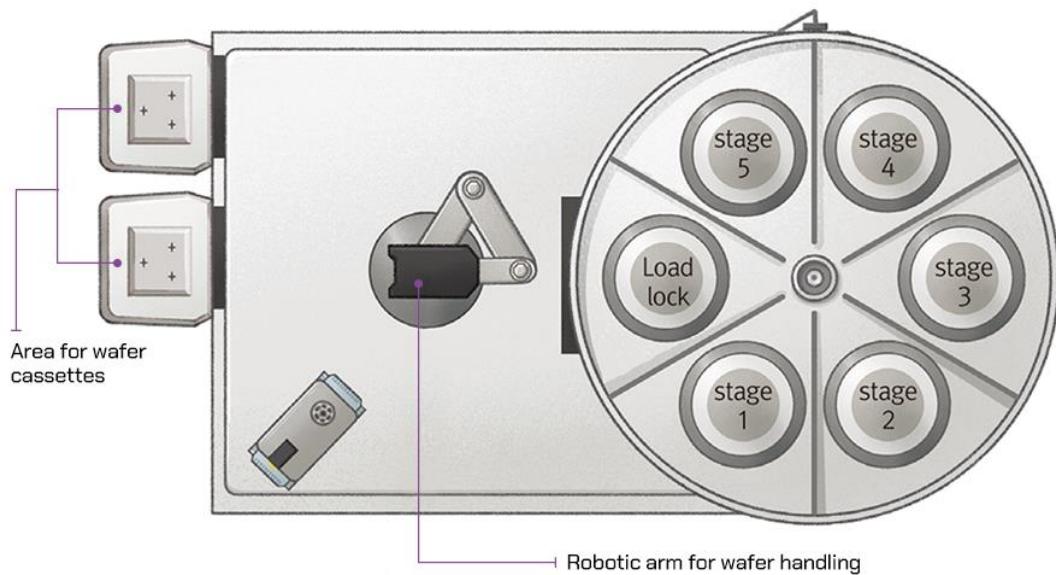


Figure 44 A bird's eye view of wafer-level reflow equipment (Source: Hanol Publishing)

The process of solder ball mounting involves attaching solder balls onto a WLCSP for packaging. The key distinction from placing solder balls on a substrate in conventional packaging lies in the fact that solder balls are placed atop a wafer. Thus, flux application, solder ball mounting, and the reflow process follow the same steps, except that the stencil utilized to applying flux and mounting solder balls has the same size as the wafer itself.

Additionally, the reflow equipment takes a hot plate-based approach, as depicted in Figure 44, as opposed to the convection reflow method involving conveyers. In wafer-level reflow equipment, different temperatures are applied to wafers as they progress through the various stages. This ensures that packaging can progress while maintaining a temperature profile for the reflow process.

## Flip Chip Bump Process

The process of forming bumps in a flip chip package is carried out in the wafer-level process, while the subsequent steps are conducted in the conventional packaging processes.

## The Flip Chip Packaging Process

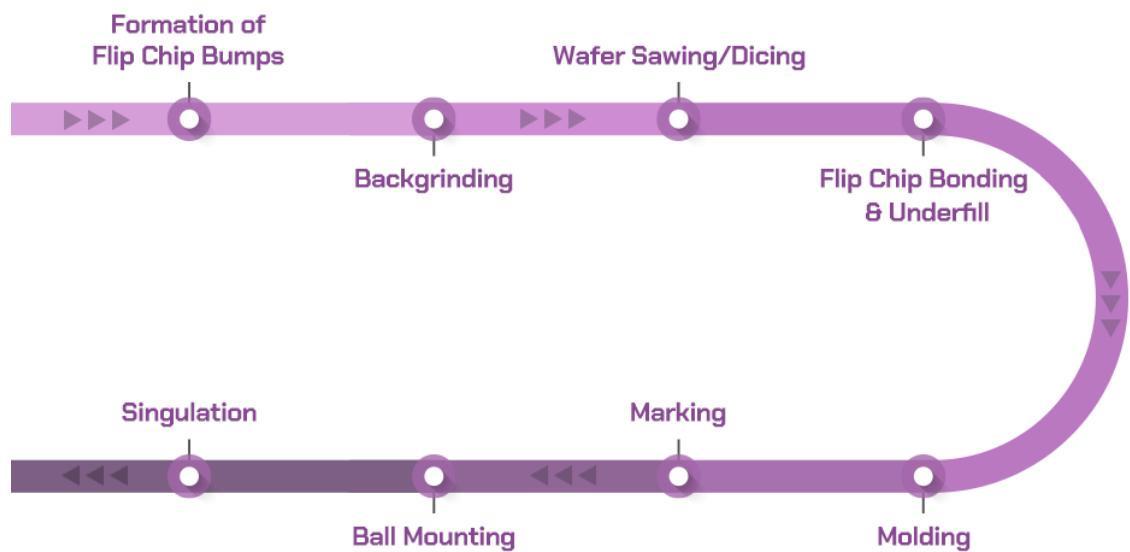


Figure 45 An overview of the flip chip packaging process

## The Flip Chip Bump Formation Process

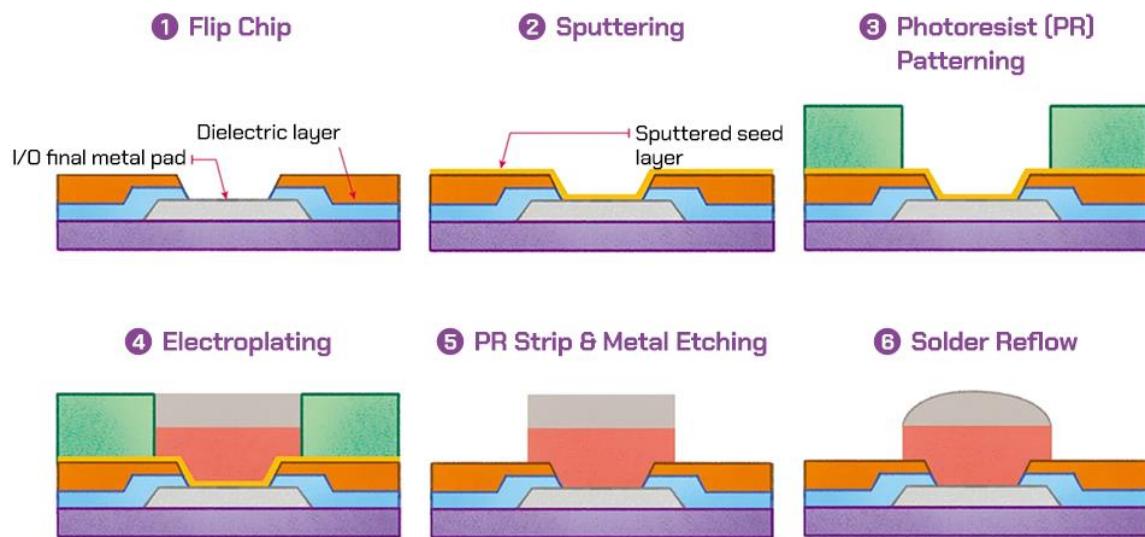


Figure 46 The steps for forming a flip chip bump

As the bumps must be sufficiently high, it is necessary to select a photoresist that can be thickly applied to the wafer-level package. Copper pillar bumps (CPB)<sup>1</sup> are formed through copper plating followed by solder plating. This solder is typically a lead-free tin/silver alloy. Once plating is complete, the photoresist is removed and the under bump metallurgy (UBM)<sup>2</sup> film formed by sputtering is removed via metal etching. The bumps are then molded into a spherical shape using wafer-level reflow equipment. The solder bump reflow process here serves to minimize height discrepancies among the bumps, reduce the surface roughness of the solder bumps, and eliminate oxides from the solder, all of which enhance the bonds during the flip chip bonding process.

<sup>1</sup>**Copper pillar bump (CPB):** The structure of the bump for flip chip bonding to reduce the gap between the bumps. Copper is used to form the pillars that have bumps on top of them.

<sup>2</sup>**Under bump metallurgy (UBM):** The metal layer formed under flip chip bumps.

### Redistribution Layer (RDL) Process

## The Redistribution Layer (RDL) Packaging Process

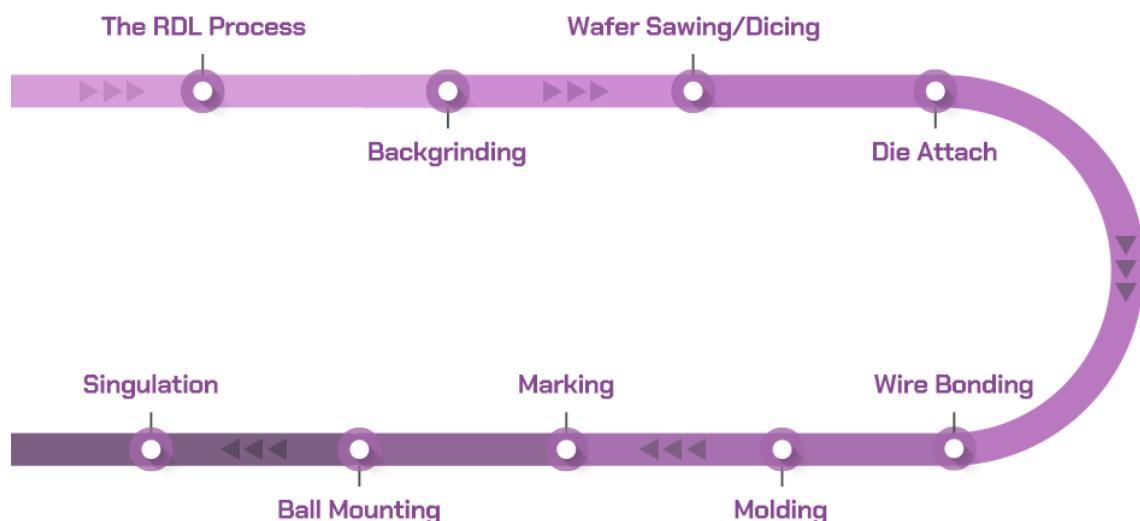


Figure 47 An overview of the packaging process using a redistribution layer (RDL)

## The Redistribution Layer (RDL) Formation Process

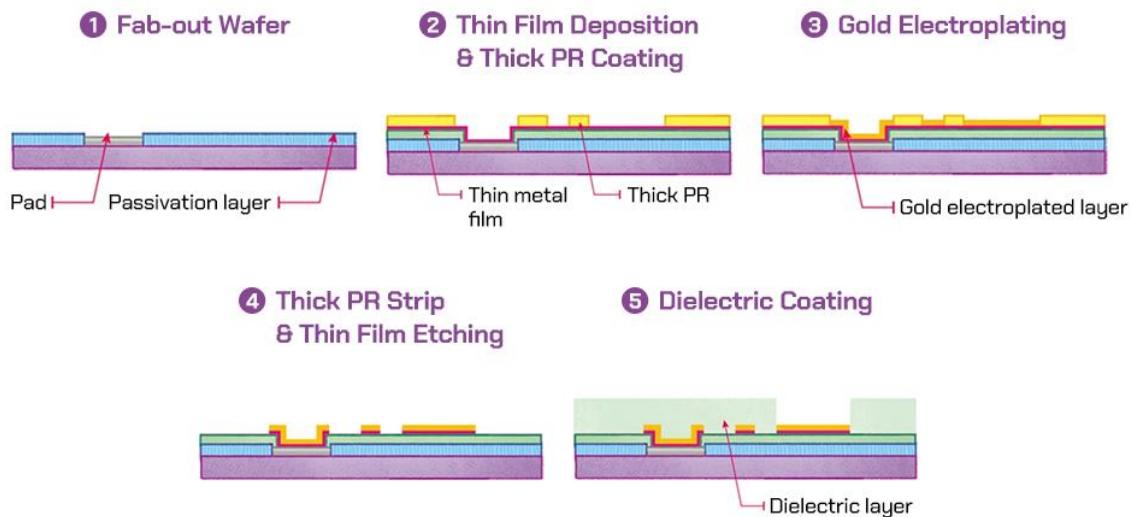


Figure 48 The steps for forming a redistribution layer (RDL)

Used for chip stacking, the redistribution layer (RDL) process creates a new pad by forming an extra layer of metal wiring over a pad formed on a wafer. Consequently, the packaging processes after the RDL process follow conventional packaging processes, as depicted in Figure 47. During chip stacking, the die attach and wire bonding steps are repeated equally for each chip that needs to be stacked.

In the RDL process, sputtering is first used to create a thin layer of metal film, which is covered with a thick layer of photoresist. A pattern is created through photolithography so that the exposed areas of the pattern can be electroplated with gold to form metal wiring. Since redistribution itself is a process of rebuilding the pad, the ability to form strong bonds is essential for wire bonding. This is why gold, which is widely applied for wire bonding, is used for plating.

### Fan-out Wafer-Level Chip-Scale Package (WLCSP) Process

The process of fabricating a fan-out WLCSP begins by applying tape to a wafer-shaped carrier. After wafer dicing, the high-quality chips are attached on top of the tape at regular intervals. The spaces between the chips are filled with wafer molding, resulting in a new shape. Once the wafer molding is complete, the carrier and tape are removed. Next, metal wiring is created on the newly formed wafer using wafer equipment, followed by the attachment of solder balls for packaging. Finally, the wafers are diced into individual packages.

## **Wafer Molding**

To create a fan-out WLCSP, wafer molding is an essential step. The wafer molding process entails placing a wafer—in the case of a fan-out WLCSP, a wafer-shaped carrier with chips attached to it—into a molding frame. An epoxy molding compound (EMC)<sup>3</sup>, which can be in the form of a liquid, powder, or granules, is then added to the frame and compression and heat are applied to mold the setup. Wafer molding is not only an essential process for fan-out WLCSPs, but it is also a requirement for a known good stacked die (KGSD)<sup>4</sup> that uses TSV, which will be discussed later.

*<sup>3</sup>Epoxy molding compound (EMC): A heat dissipation material based on an epoxy resin, or a type of thermosetting polymer. It seals semiconductor chips to protect them from external environmental factors such as heat, moisture, and shock.*

*<sup>4</sup>Known good stacked die (KGSD): A product comprised of stacked chips that have been tested and confirmed to be of good quality. A prime example is HBM.*

## **Through-Silicon Via (TSV) Package Process**

Figure 49 illustrates the process steps of fabricating a TSV package using a via-middle<sup>5</sup> approach. First, vias are formed during wafer fabrication. Subsequently, solder bumps are formed on the wafer's front side during the packaging process. The wafer is then attached to a carrier wafer and backgrinded. After bumps are formed on the backside of the wafer, the wafer is diced into units of chips and stacked.

*<sup>5</sup>Via middle: A type of TSV that fabricates TSVs after the formation of CMOS but before the metal layers are formed.*

To provide a brief overview of the process of forming TSVs with middle vias, transistors such as CMOS are initially fabricated on a wafer during the front-end of line (FEOL) process. Then, using a hard mask (HM)<sup>6</sup>, a pattern is created where the TSV will be formed. Next, the areas without the hard mask are removed through dry etching to create deep trenches. Insulating films, such as oxides, are subsequently deposited via chemical vapor deposition (CVD). This insulating film serves to isolate metals like copper that will later fill the trenches, preventing the metals from contaminating the silicon. Additionally, a thin layer of metal that acts as a barrier is created atop the insulating film.

*<sup>6</sup>Hard mask (HM): A mask that creates finer patterns as it is made up of harder materials than soft masks. Since an HM is not photosensitive in itself, additional patterning needs to be formed with the application of photoresist, followed by the subsequent etching process.*

This thin layer of metal is used to electroplate copper. After electroplating, the wafer's surface is smoothed through chemical mechanical polishing (CMP), which simultaneously eliminates all of the copper from the surface of the wafer, ensuring that copper remains solely within the trenches. This is followed by the back-end of line (BEOL) process to complete the wafer fabrication.

## The Through-Silicon Via (TSV) Packaging Process

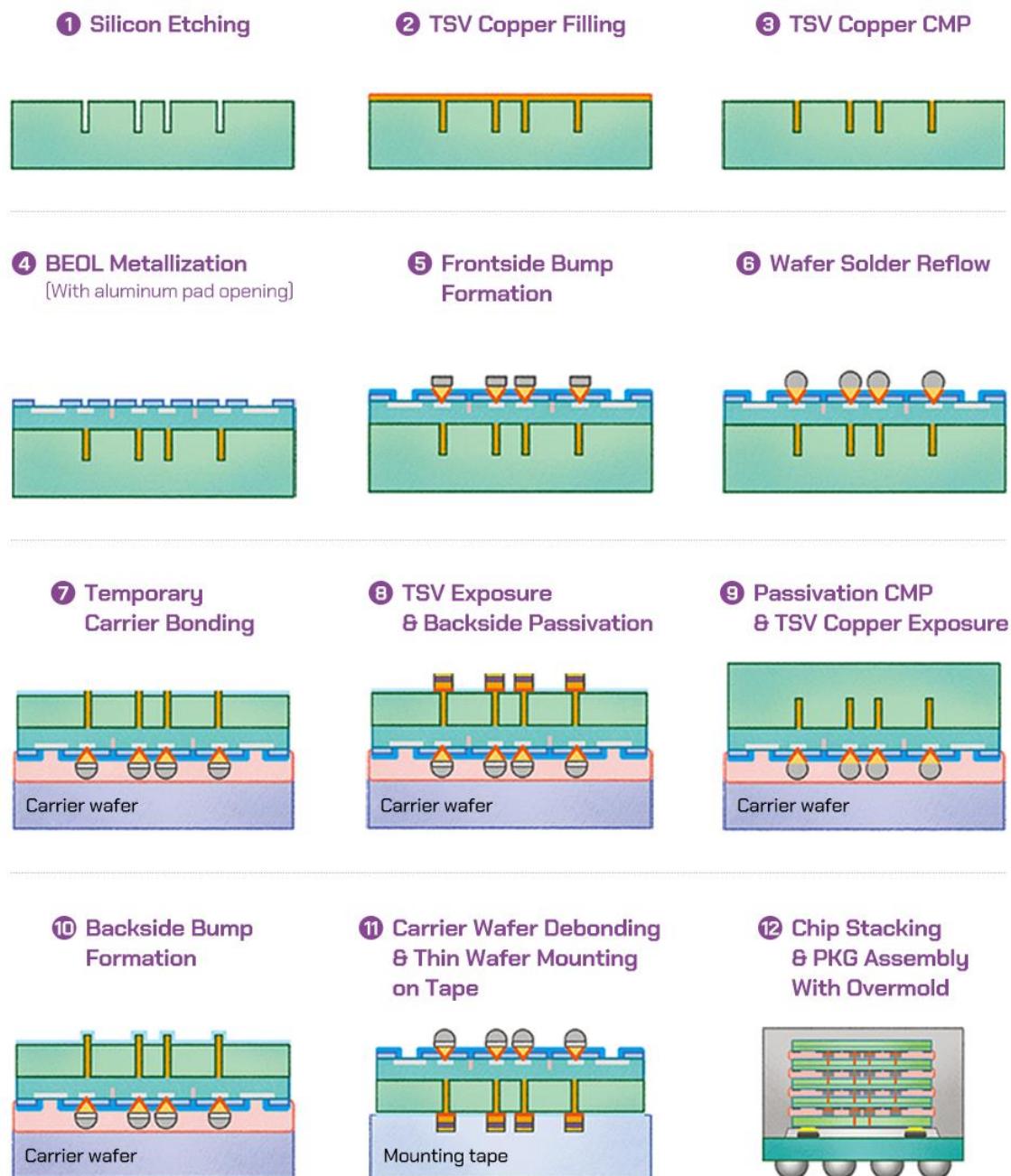


Figure 49 The steps of the TSV packaging process (Source: Hanol Publishing)

There are two main types of packages that can be created when producing chip stack packages using TSV technology. The first is a package that uses a substrate with 3D chip stacking technology. The second type involves creating a KGSD and then using it to make a 2.5D or 3D package. The following section will explain the processes of fabricating KGSDs and using them to create 2.5D packages.

As a chip stack package which uses TSV, KGSD has to undergo additional packaging processes such as 2.5D packaging, 3D packaging, and fan-out WLSCP. A prime example of a KGSD product is high bandwidth memory (HBM). Since a KGSD needs to go through additional packaging processes, the connection pins are formed as fine solder bumps rather than conventional solder balls. As a result, while chips in a 3DS package are stacked on a substrate, chips in a KGSD are stacked on a wafer, which also serves as the bottommost chip of the KGSD. In the case of HBM, the chip at the bottom is referred to as the base chip or base wafer, while the chips stacked above it are known as the core chips.

To explain the process steps, bumps are formed on the front surface of both the base and core wafers through a flip chip process. In the context of a 2.5D package, the base wafer necessitates the arrangement of bumps so that they can be attached to interposers.

Conversely, the core wafer forms a bump layout that facilitates chip stacking on the front of the wafer. After bumps are formed on the frontside of the wafer, the wafer should be thinned, and bumps should also be formed on the wafer's backside. However, as previously mentioned during the introduction of the backgrinding process, it is important to note that thinning the wafer can induce the wafer to warp. While conventional packaging makes it possible to have wafers taped to ring frames following the backgrinding to prevent wafer warpage, this method is not viable in TSV packaging where bump formation occurs on the wafer's backside. This is exactly why the wafer support system (WSS) was developed. Under the WSS, the frontside of the wafer with bumps is bonded to a carrier wafer with a temporary adhesive. At the same time, the backside of the wafer is grinded to thin it. Since it is attached to the carrier wafer, the thinned wafer does not warp.

Additionally, since the carrier wafer is also in the form of a wafer, it can be processed using wafer equipment. Using this structure, bumps are created on the core wafer's backside. Once bumps are formed on both sides of the core wafer, the carrier is debonded. Then, the wafer is taped to a ring frame and diced in the same manner as conventional packaging processes. The base wafer remains attached to the carrier wafer as it removes chips that are diced from the core wafer to stack on top of the base wafer. When chip stacking is complete, the base wafer is molded while the carrier wafer is debonded. In this way, the base wafer becomes a molded wafer with core chips stacked on it. This wafer is grinded to the target thickness suitable for making a 2.5D package and then diced into chips to form KGSDs. This finished HBM is packed and shipped to customers who will make 2.5D packages.

## **Wafer Support System (WSS) Process**

A WSS refers to a system that allows further processing on the backgrinded surface of a thinned wafer. This process occurs prior to the completed backgrinding process. The WSS process involves two main steps: carrier bonding, which involves attaching a carrier to a wafer for TSV packaging; and carrier debonding, where the carrier is detached after completing processes like forming bumps on the wafer's backside.

Figure 50 depicts the WSS process steps, where carrier bonding involves applying a temporary adhesive to the wafer before attaching it to the carrier. Carrier debonding involves removing the carrier after processes on the backside are completed and ensuring the wafer is cleaned to remove any residual adhesive.

## **The Wafer Support System (WSS) Process**

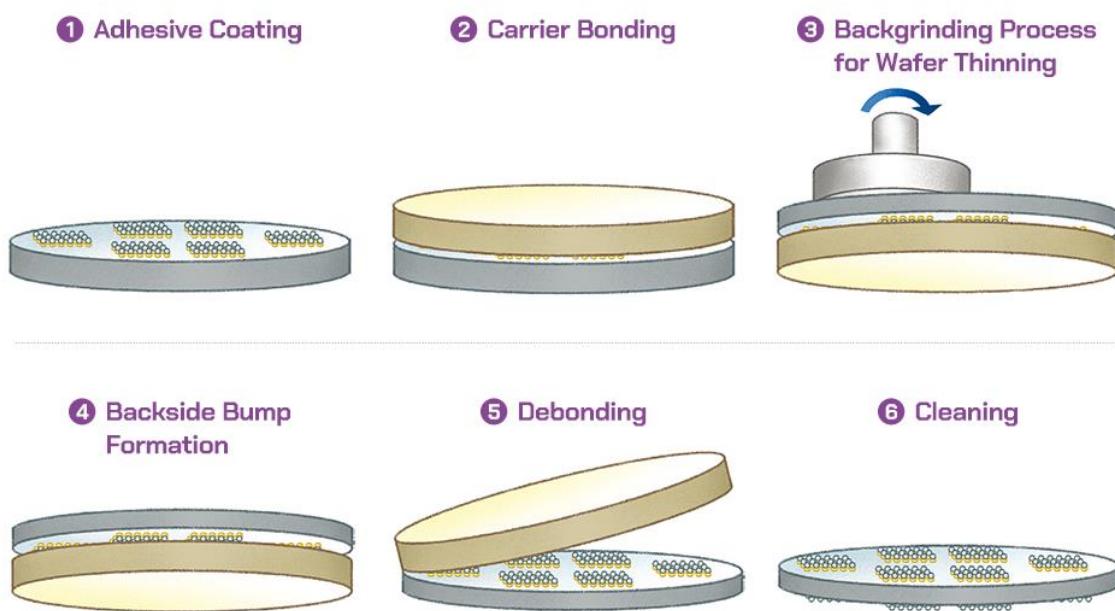


Figure 50 The steps of the wafer support system (WSS)

There are several considerations to be taken into account in carrier bonding: the overall thickness of the wafers bonded through carrier bonding should be uniform; there should be no voids at the bonded joints; the alignment of the two wafers should be accurate; there should be no adhesive-related contamination at the edge of the wafers; and wafer warpage should be minimized during the process. During the carrier debonding, there should also be: no damage such as chipping<sup>7</sup> or cracking to the wafer that is separated from the carrier; no adhesive residue; and no deformation of the bumps.

<sup>7</sup>**Chipping:** The breaking of the edges or corners of a chip or wafer.

Debonding stands out as a relatively complex and critical step within the WSS process. As a result, various debonding methods have been proposed and developed, accompanied by the development of different temporary adhesives for each method. Typical methods include thermal techniques, laser ablation followed by peel-off, chemical dissolution, and chemical cleaning after mechanical lift-off.

### Wafer Edge Trimming Process

## A Comparison of Untrimmed and Trimmed Wafer Edges

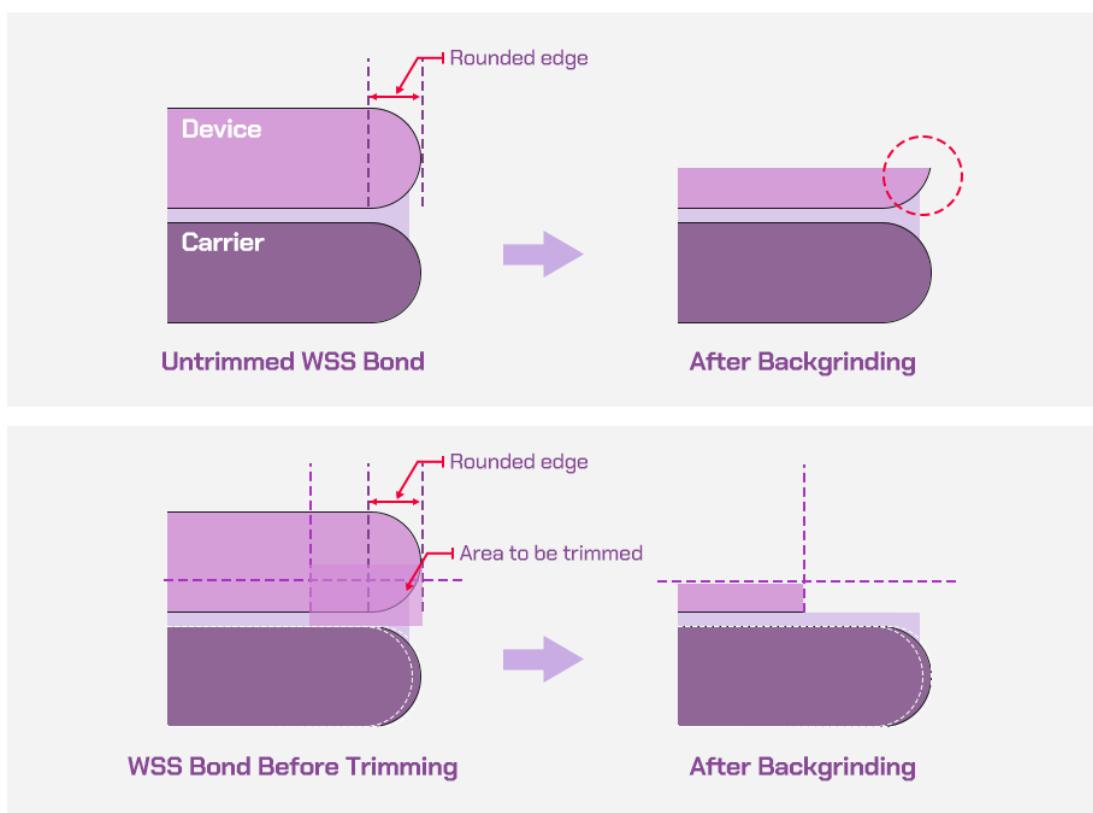


Figure 51 A comparison of the edges of untrimmed (upper image) and trimmed (lower image) wafers

After a wafer for a TSV package is bonded to a carrier wafer and then backgrinded, it will have sharp edges, as shown in the red circle in the upper image of Figure 51. In this state, the wafer undergoes subsequent processes such as photolithography, metal film formation, and electroplating to form bumps on the backside. However, these processes elevate the risk of chipping the wafer's edge. Cracks at the edge could propagate inward, eventually rendering further processing impossible, thereby resulting in significant yield loss. To preemptively overcome this problem, the edge of the frontside of the wafer designated for

TSV packaging is trimmed and removed before it is bonded with the carrier wafer. When the trimmed wafer is bonded to the carrier wafer and backgrinded, the sharp edge's prominence diminishes, as shown in the lower part of Figure 51. Consequently, the risk of chipping during subsequent processes is eliminated. The trimming process employs a rotating wafer dicing blade that traverses the wafer's edge, removing a designated segment of the edge.

### **Stacking Process**

In TSV packaging, the bumps formed on the front and back of wafers are bonded together for stacking. Like in flip chip bonding, mass reflow (MR) and thermocompression are used for bonding. Depending on the type of stacking, the processes are classified as chip-to-chip stacking, chip-to-wafer stacking, and wafer-to-wafer stacking.

When stacking chips with TSVs, micro bumps are used. Therefore, the gaps between these bumps are small, as is the spacing between stacked chips. This is why thermocompression, known for its high reliability, has been widely adopted. However, thermocompression has the disadvantages of taking a long time and has low productivity as heat and pressure must be applied for a certain period during bonding. As such, there's a growing trend toward adopting MR as an alternative bonding technique.

### **Looking Beyond the Types of Wafer Packaging**

After discussing the two main groups of conventional and wafer-level packages in these two last episodes, the next chapter in our series will delve into the materials that make up the various components of these packages. In particular, it will cover the unique properties of these small materials and analyze how they affect the performances of these semiconductor products.

## Episode 9: Exploring the Roles of Materials in Conventional Semiconductor Packaging



### Semiconductor Back-End Process Episode 9 Exploring the Roles of Materials in Conventional Semiconductor Packaging

Reliability and stability are key requirements of semiconductor products to ensure their smooth operation. Semiconductor devices must therefore be protected from physical, chemical, and thermal damage by their packages, and the materials used to make these packages must offer certain qualities. As semiconductor products are increasingly required to perform at higher speeds, packaging materials need to have enhanced electrical properties such as low permittivity<sup>1</sup> and low dielectric loss<sup>2</sup> for substrates. Materials used for semiconductor memory, as well as logic chips such as CPUs and GPUs, are also required to possess good thermal conductivity for quality thermal dissipation. This highlights the importance of ensuring the advancement of packaging materials to keep up with industry demands. The next two episodes will discuss the characteristics of materials used in the two major package types, starting with this article which covers the materials of conventional packages.

<sup>1</sup>**Permittivity:** The sensitivity to an external electric field, or the degree to which its internal charge responds when the electric field is applied to an insulator.

<sup>2</sup>**Dielectric loss:** The conversion of electrical energy when a dielectric is placed in an alternating electric field.

#### Primary and Subsidiary Packaging Materials

Packaging materials can be broadly categorized into primary and subsidiary materials. Primary materials make up the package itself and have a direct impact on the product's quality and reliability. Subsidiary materials, on the other hand, are not part of the product's structure as they are solely used during the packaging process and then removed.

## Common Processes in Conventional Packaging

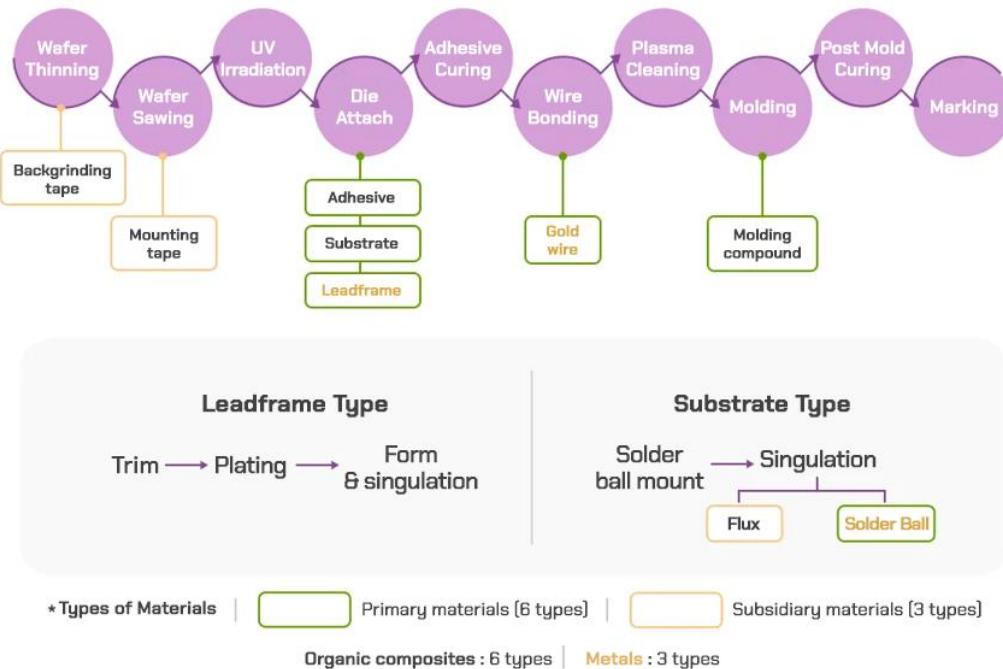


Figure 52 Materials used in the different stages of the conventional packaging process (Source: Hanol Publishing)

Figure 52 shows the different types of materials used in a typical conventional packaging process. There are six types of organic composites used as primary materials in conventional packaging: adhesives, substrates, epoxy molding compounds (EMC), leadframes, wires, and solder balls, with the latter three being metals. As for subsidiary materials, some examples include tapes and fluxes<sup>3</sup>. These small but fundamental materials will be explained with consideration of their crucial roles.

<sup>3</sup>**Flux:** A water-soluble and oil-soluble solvent that makes solder balls adhere well to the copper of the ball land.

### Leadframes: Metal Alloys for Internal Electrical Connections

Leadframes electrically connect the chip inside the package with the printed circuit board (PCB) located outside the package. The metal plate used to form a leadframe is usually made of Alloy 42<sup>4</sup> or alloys made of copper. Etching and stamping are the two methods used to produce a leadframe. In the etching process, the leadframe is created by applying photoresist to the metal plate along the pattern of the leadframe and exposing it to an etchant<sup>5</sup> so the areas not covered by the photoresist are removed. This method is typically used when a fine leadframe pattern is required. For stamping, a progressive die<sup>6</sup> is mounted on a high-speed press to create the leadframe.

<sup>4</sup>**Alloy 42:** An iron-based alloy with a coefficient of thermal expansion similar to silicon.

<sup>5</sup>**Etchant:** A general term for corroding substances such as chemical solutions and gases in the etching process.

<sup>6</sup>**Progressive die:** A mold technology that compresses several stages of processes into one continuous process.

### **Substrates: Copper, Glass Fabric & More Used in the Device's Foundation**

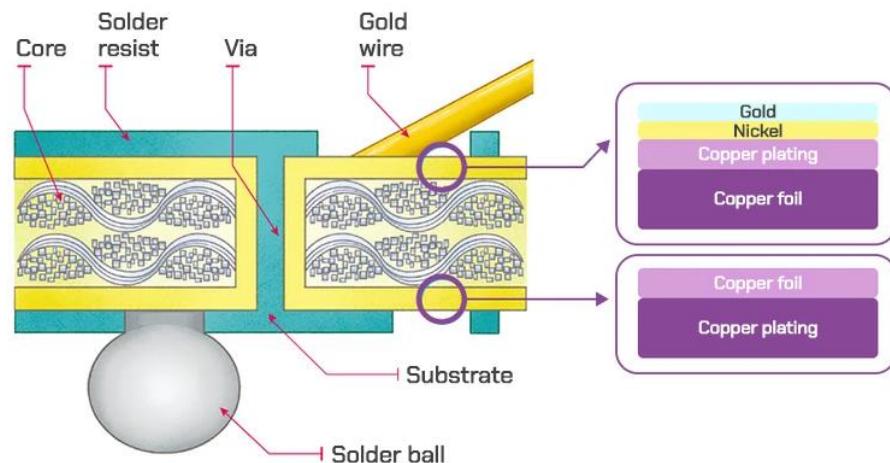


Figure 53 A side view of the substrate after going through the packaging process (Source: Hanol Publishing)

Just like leadframes, substrates also play a role in electrically connecting the chip inside the package to the PCB outside the package. Consequently, substrates are key components of semiconductor chips in ball grid array (BGA) packages that use solder balls instead of a leadframe. Figure 53 shows the side view of the substrate's structure after the packaging process. A solder ball is attached to the bottom and a wire is connected to the top. The center of the substrate is formed with a material called the “core” that consists of copper foil bonded to sides of a glass fabric impregnated<sup>7</sup> with bismaleimide triazine (BT)<sup>8</sup> resin that possesses thermal stability. Metal wiring is formed on the copper foil while solder resist is applied on top of it to expose the metal pad that serves as a protective layer.

<sup>7</sup>**Impregnation:** The process of filling gaps that are formed during the casting process to reduce coating failures during the plating process.

<sup>8</sup>**Bismaleimide triazine (BT):** A type of synthetic resin used in PCBs that is made by reacting heat-resistant bismaleimide and triazine.

### **Adhesives: Epoxy-Based Polymers for Bonding Key Components**

Adhesives are in either liquid form like pastes or solid form such as films. They are primarily composed of thermosetting, epoxy-based polymers and are used to bond chips to either a leadframe or substrate. They can also be used to bond chips together in chip stacking. For an adhesive to achieve high reliability in testing, it must have high adhesion, low moisture

absorption, appropriate mechanical properties, and low ionic impurities. In addition, to ensure the quality of the process, an adhesive must have excellent material flowability and wettability of the bonding interface during the high-temperature and high-pressure bonding process. Voids<sup>9</sup> must also be suppressed to achieve high interfacial adhesion. This requires optimization of rheological properties such as viscosity, thixotropy<sup>10</sup>, and hardening traits, as well as strong adhesion between the chip and the leadframe or substrate surface.

<sup>9</sup>**Voids:** Hollow holes or air pockets that form within a material. They are a defect that occurs during material manufacturing or processes involving heat treatment.

<sup>10</sup>**Thixotropy:** The property of a liquid substance to decrease in viscosity when a shear force, such as stirring, is applied and to increase in viscosity when no shear force is applied.

Liquid adhesives include epoxy and silicone adhesives. Solid adhesives include lead-on-chip (LOC) tapes that are used for leadframes, spacer tapes used to keep chips apart when stacking chips of the same size, and die attach films (DAFs) that are used for chip stacking or to attach chips to the substrate. DAFs are also called wafer backside laminate (WBL) films because they are applied to the backside of the wafer.

#### **Epoxy Molding Compounds (EMC): Thermosetting Polymers for Protection & Heat Dissipation**

EMCs are encapsulants<sup>11</sup> used in the semiconductor packaging process and are composites of inorganic silica and thermosetting epoxy polymer that form a three-dimensional bonding structure when heated. As EMCs encapsulate the chip, they must protect it from external physical and chemical damage and effectively dissipate heat that is generated when the chip is in operation. Moreover, EMCs should be easily moldable to achieve the desired package shape. Since they interface with other packaging materials such as substrates and chips, EMCs must strongly adhere to these materials to ensure the reliability of the package.

<sup>11</sup>**Encapsulants:** They consist of thermosetting polymers that form a three-dimensional structure which is hardened by external heat. Their function is to protect the contents from heat, moisture, and shock.

Tablet	Powder/Granule	Liquid
		
Transfer molding	Compression molding	Wafer molding

Figure 54 Types of EMCs

Figure 54 shows the types of EMCs and the processes in which each type is used. Tablet-type EMCs are mainly used for transfer molding, while powdered EMCs are commonly used for compression molding or to mold a large wafer. On the other hand, liquid EMCs are used for molding a wafer that is difficult to mold. Recently, vacuum lamination using film-type EMCs has also been used for fan-out wafer-level chip scale packages (WLCSP) and large-sized panel-level packages (PLPs). There are also EMCs for molded underfill (MUF), a process where underfilling and molding are performed simultaneously in the flip-chip process.

### Solders: From Tin to Unleaded Alloys for Mechanical & Electrical Connections

Solder is a metal that melts at low temperatures, and this property makes it widely used for electrical and mechanical connections in various structures. It is used to connect the package to the PCB in semiconductor packaging, as well as to connect the chip to the substrate in flip-chip packaging. The solder for connecting the package to the PCB is mainly in the form of balls that vary in size from 30 micrometers ( $\mu\text{m}$ ) to 760  $\mu\text{m}$ . Today, the number of pins connecting a package to the PCB is increasing to improve electrical properties, leading the solder balls to get smaller.

Solder balls must be uniform in alloy composition when made from solder alloy as a lack of uniformity can compromise reliability in its drop impact or temperature cycle tests. It is also important that they have good oxidation resistance as excessive oxide buildup on materials or during the reflow process can result in non-wetting defects where solder balls will not adhere and fall off. For this reason, fluxes are used to remove oxide film buildup during soldering, and an inert atmosphere needs to be created with nitrogen gas during reflow. In addition, there should be no voids as the solder volume will be insufficient due to voids and possibly lead to the reduction of the solder joints' reliability. The size of the solder balls is also crucial because uniformly sized solder balls increase the efficiency of the process. Lastly, the surface of the solder balls must also be free of contamination and dendrite<sup>12</sup> growth. These can increase the failure rate and reduce the reliability of the solder joints.

In the past, solder balls were often made of the tin alloy (Pb-Sn) which has good mechanical properties and electrical conductivity. However, as lead became subject to environmental regulations such as the EU's RoHS Directive<sup>13</sup> after it was found to be harmful to human health, unleaded solder with a lead content of 700 parts per million (ppm) or less is now mainly used.

<sup>12</sup>**Dendrites:** Crystals formed in the shape of tree branches; a type of fractal found in nature.

<sup>13</sup>**RoHS Directive:** The EU's Restriction of the Use of Certain Hazardous Substances in Electrical and Electronic Equipment (RoHS) Directive aims to protect the environment and human health by substituting hazardous materials for safer alternatives.

## Tapes: PSA For Permanent & Temporary Bonding

There are two types of tape that will be explained in this section. The first is adhesive tape used to permanently bond solid surfaces to homogenous or heterogenous surfaces. The other type is temporarily adhesive tape such as dicing and backgrinding tapes that are able to bond and be removed through cohesion and elasticity. The material used in these tapes is called pressure-sensitive adhesive (PSA).

Backgrinding tape is applied to the front of a wafer to protect the devices on the wafer during the backgrinding process. After the backgrinding process is complete, the tape must be removed so no adhesive residue is left on the wafer.

Dicing tape, also known as mounting tape, is used to fix a wafer in a ring frame and ensure that the chips on the wafer do not come off during the wafer dicing process. Thus, dicing tape must have good adhesion during wafer dicing, but it must also be easily detachable. Therefore, the tape is irradiated with ultraviolet light before the chips are removed as dicing tape contains PSA that reacts to the ultraviolet light. This weakens the adhesion and makes it easier to remove the chips. In the past, wafers were attached to the dicing tape after backgrinding, but with the wide use of WBL as an adhesive for chips, the wafers that have completed the backgrinding process are attached to the tape that combines WBL and dicing tape.

## Wires: From Gold to Copper for Electrical Chip Connections



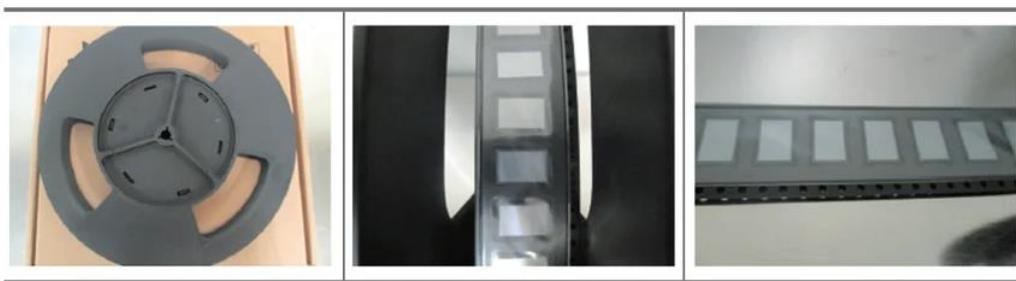
Figure 55 Gold (Au) wire

The wire that electrically connects a chip to a substrate or leadframe, or a chip to a chip, is typically made of high-purity gold. Gold has good malleability so it can be spread thin, as well as ductility to allow it to be stretched into a thread. These attributes are highly beneficial in the wiring process. In addition, gold's oxidation resistance makes it highly reliable, while its excellent electrical conductivity provides it with good electrical properties.

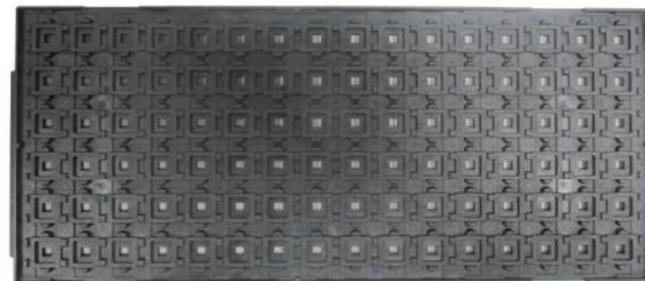
However, gold increases manufacturing costs due to its high price. For this reason, thinned gold wire is sometimes used, but it is more susceptible to breakage if stretched too much, limiting its use. Therefore, other metals such as silver are added to make alloys with gold, while gold-coated silver, copper, palladium-coated copper, and gold palladium-coated copper are also used.

Copper wires are increasingly used instead of gold wires due to their price competitiveness and the fact that copper wires also have good electrical conductivity while having slightly less malleability and ductility than gold wires. However, as copper is susceptible to oxidation, copper wires can be oxidized during and after the wiring process. Therefore, unlike gold wires, the wiring equipment for copper wires are sealed and the inside of the equipment is filled with nitrogen gas to prevent the copper wire from being exposed to air and being oxidized.

#### Packing Materials: Preparing for Shipment With Tape & Reel



▲ Tape & reel [T&R]



▲ Tray

Figure 56 Tape and reel packaging (above) and a tray (below)

After packaging and the package testing, semiconductor products are shipped to customers. Tape and reel (T&R), or tray packing, is used to pack the products. In T&R packing, the packages are placed on a tape with pockets that are the same size as the package. The tape is then rolled onto a reel and the package is packed for shipment to the customer. In tray packing, the packages are placed in a tray, which is then stacked and packed for shipment.

### **A Look Ahead to the Materials of Wafer-Level Packages**

Following this introduction of the materials used in the various processes that complete conventional packages, the next episode will look at the materials used in wafer-level packages. In addition to seeing what types of substances they are made of, the article will cover the crucial roles they play in ensuring the quality and durability of semiconductor products.

## Episode 10: Exploring the Roles of Materials in Wafer-Level Semiconductor Packaging



### Semiconductor Back-End Process Episode 10

Exploring the Roles of Materials  
in Wafer-Level Semiconductor Packaging

Following the [previous episode](#) which covered the materials that make up conventional packages, this article will examine the various materials used in wafer-level packaging (WLP). From the resin in a photoresist to the adhesive in a wafer support system (WSS), the various WLP materials play vital roles which will be explored throughout this penultimate installment of the series.

#### Photoresists (PR): Sensitizers, Resins, & Solvents Create Patterns & Barriers

Photoresists are compounds formed from melting soluble polymers and photosensitive materials—which undergo a chemical reaction such as degradation or fusion when exposed to light energy—in a solvent. They are used to create the intended pattern during photolithography in WLP, while they also serve as a barrier by plating metal wiring during the subsequent electroplating<sup>1</sup> process. The materials that make up a photoresist can be found below in Figure 57.

<sup>1</sup>**Electroplating:** A reaction where oxidation occurs at the positive plate to produce electrons which are transmitted to a wafer with a solution that has metal ions. These metal ions are negative plates that become metal.

Component	Role
Sensitizer <small>(Photoactive compound<sup>1</sup> / Photoacid generator<sup>2</sup>)</small>	Forms an image by reacting with light
Resin	Serves as a barrier during etching or electroplating
Solvent	Enables application to a surface by increasing the viscosity of a photoresist

<sup>1</sup>Photoactive compound (PAC): The component of a photoresist that is sensitive to light.

<sup>2</sup>Photoacid generator (PAG): A photoresist component which generates an acid upon exposure to light.

Figure 57 The components and roles of photoresists (Source: Hanol Publishing)

A photoresist is classified as positive or negative depending on how it responds to light. In a positive photoresist, the areas exposed to light undergo degradation which weakens the bonding, while unexposed areas experience cross-linking<sup>2</sup> that strengthens the bonds. Therefore, areas that have received light are removed during the development process. However, in the case of negative photoresists, the areas that are exposed to light experience cross-linking and harden, leading them to remain intact while unexposed areas are removed. As negative photoresists can be applied more thickly during the spin coating process as they tend to have a higher viscosity than positive photoresists, they are usually used when forming higher solder bumps. On the other hand, positive photoresists need to be applied at least two times.

The light used during photolithography can be classified according to its wavelength, which is measured in nanometers (nm). Light with shorter wavelengths has been used during photolithography to form finer patterns for semiconductors that have gone through scaling, leading to the enhancement of photoresists. Accordingly, photoactive compounds (PAC) are used for g-line<sup>3</sup> and i-line<sup>4</sup> photoresists with longer wavelengths, while chemically amplified resists (CAR)<sup>5</sup> are used for photoresists with shorter wavelengths. As for WLPs, they typically use i-line steppers<sup>6</sup>.

<sup>2</sup>**Cross-link:** A chemical reaction that links polymer chains through chemical bonds.

<sup>3</sup>**g-line:** A line of the mercury spectrum corresponding to a wavelength of about 436 nm.

<sup>4</sup>**i-line:** A line of the mercury spectrum corresponding to a wavelength of about 356 nm.

<sup>5</sup>**Chemically amplified resists (CAR):** A resist used to improve the photosensitivity of photoresist materials.

<sup>6</sup>**Stepper:** Equipment used to expose wafers. Different types of equipment are used for wafer exposure with varying degrees of accuracy depending on the type of light used.

## Plating Solutions: Metal Ions, Acids, & Additives For Controlled Electroplating

Plating solutions are used during electroplating. These solutions are comprised of metal ions to be plated during the electroplating process, acids that become solvents to dissolve metal ions in the solutions, and various additives that enhance the properties of the plating solution and plating layer. Some metals that can be plated during the electroplating process include nickel, gold, copper, tin, and tin/silver alloy. These metals exist as ions inside the plating solution. For solvents, some commonly used acids include sulfuric acid and methanesulfonic acid. Meanwhile, the additives include levelers which limit the buildup of materials and flatten the surface of the plating layer, and grain refiners that prevent the lateral growth of plating grains so they become finer as they grow.

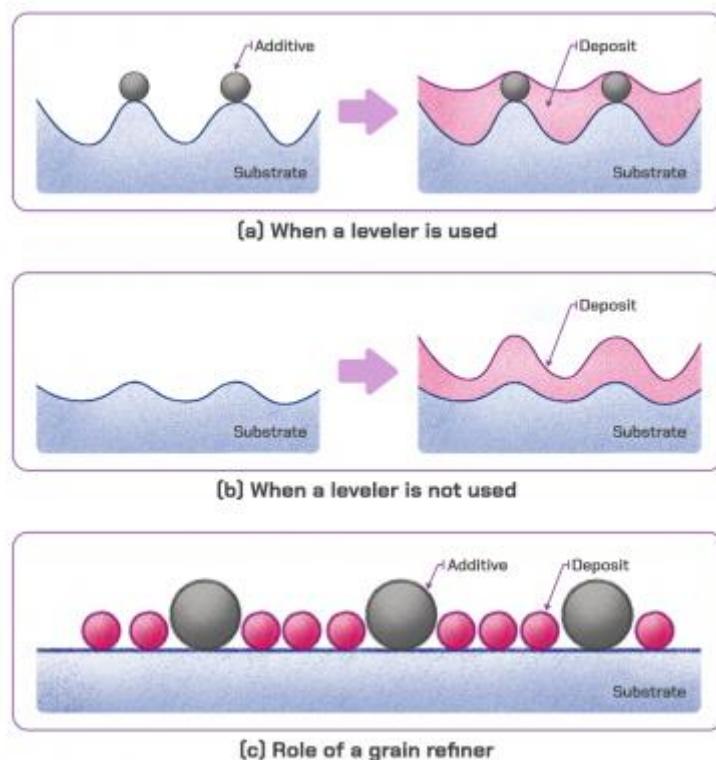


Figure 58 The roles of plating solution additives (Source: Hanol Publishing)

## Photoresist Strippers: Using Solvents to Remove Without a Trace

After the plating process is finished, the photoresist needs to be removed with a photoresist stripper without chemically damaging the wafer or leaving any residue. Figure 59 shows this process of removing a photoresist. First, the solvent of the photoresist stripper reacts when it contacts the photoresist surface, which starts to swell up. Then, the alkaline stripper breaks down and dissolves the swollen photoresist surface.

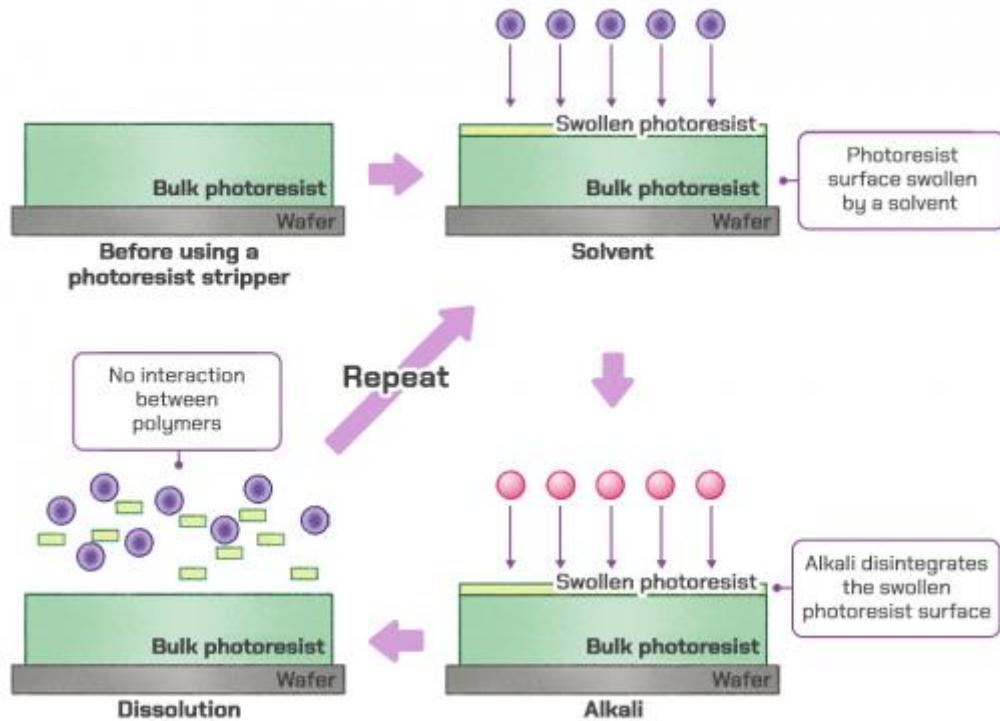


Figure 59 The sequence of a photoresist stripper removing a photoresist (Source: Hanol Publishing)

### Etchants: Using Acids, Hydrogen Peroxide & More to Precisely Dissolve Metals

WLP requires a sputtering<sup>7</sup> process to create a seed layer, a thin layer of sputtered or evaporated metal, for electroplating. This seed layer needs to be dissolved with an acid etchant after the completion of plating and photoresist stripping.

Figure 60 displays the primary components and roles of etchants. Depending on the metal to dissolve, copper etchants, titanium etchants, silver etchants, and other etchants are used. Such etchants should possess etch selectivity—the capability to selectively dissolve certain metals while leaving others undissolved or just slightly dissolved. They also should have a high etch rate to enhance the process efficiency, as well as process uniformity which enables the etchant to dissolve the metal at a uniform rate regardless of the metal's location on the wafer.

<sup>7</sup>**Sputtering:** A type of physical vapor deposition (PVD) in which high-energy ions are bombarded against a metal target, enabling the ejected metal ions to be deposited onto the wafer surface.

Component	Role	Material
Main oxidation agent	· Metal oxide	· Hydrogen peroxide
Sub oxidation agent	· Metal oxide	· Inorganic acid
Chelating agent <sup>1</sup>	· Forms a metal chelate · Stabilizes metal ions	· Amino and carboxylic compounds
	· Forms a metal chelate · Stabilizes metal ions · Regulates pH	· Organic acid
Inhibitor	· Inhibits metal etching · Forms a tapered etch profile	· Heterocyclic amine <sup>2</sup> compound
Additive	· Maintains etch rate · Stabilizes hydrogen peroxide · Accelerates the removal of etch residue	· Special additives

<sup>1</sup>Chelating agent: Chemical compounds capable of binding metal ions to form complex ring-like structure called chelates.

<sup>2</sup>Heterocyclic amine: Aromatic compounds that form under high heat conditions from creatinine, amino acids, and sugar through a series of reactions.

Figure 60 The main components and roles of etchants (Source: Hanol Publishing)

### Sputtering Targets: Depositing Metal Onto a Substrate

A sputtering target is used as a material when a thin metal film is deposited on a wafer with the sputtering method during the physical vapor deposition (PVD)<sup>8</sup> process. Figure 61 shows the process of how this target is fabricated. A cylinder is created using raw materials which have the same composition as the metal layer that is going to be sputtered, and then it is forged, pressed, heated treated, and finally shaped into a target.

**<sup>8</sup>Physical vapor deposition (PVD):** As one of the ways to deposit thin films, PVD physically separates and deposits a material on a surface.

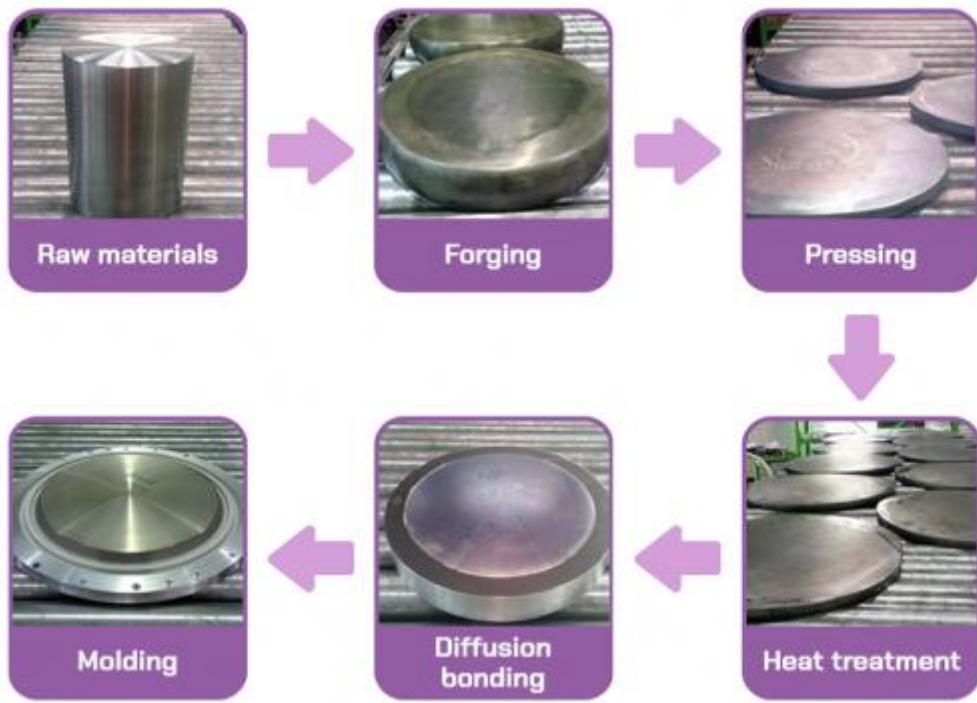


Figure 61 The process of fabricating a sputtering target (Source: Hanol Publishing)

### **Underfills: Filling Holes With EMC, Pastes, & Film for Joint Protection**

Underfills enhance joint reliability by filling spaces between the substrate and the chip or between chips that are connected by bumps just as in flip chip bonding. There are two main underfill processes that fill up the spaces between bumps. Post-filling fills the space between bumps after flip chip bonding, while pre-applied underfill fills the material before it. Furthermore, post-filling is further divided into capillary<sup>9</sup> underfill (CUF) and molded underfill (MUF). After flip chip bonding is applied, CUF fills in the gaps between bumps by using a capillary to inject underfill material into the side of the chip. This adds surface tension within the gap between the chip and the substrate. As for MUF, it allows epoxy molding compound (EMC)<sup>10</sup> to function as an underfill during molding and simplifies the process.

<sup>9</sup>**Capillary:** A very thin tube used to transfer the liquid encapsulant material into the semiconductor package.

<sup>10</sup>**Epoxy Molding Compound (EMC):** A composite of inorganic silica and a thermosetting epoxy polymeric material that creates three-dimensional bonds when heated.

During the pre-applied underfill process, the underfill is applied differently based on whether it is carried out at the chip level or at the wafer level. For the chip level, different processes and materials are used depending on whether the joints are filled with non-conductive paste (NCP) or non-conductive film (NCF). For the wafer level, NCF is primarily

used as the underfill. Figure 62 shows the types of materials used for underfill and the relevant processes.

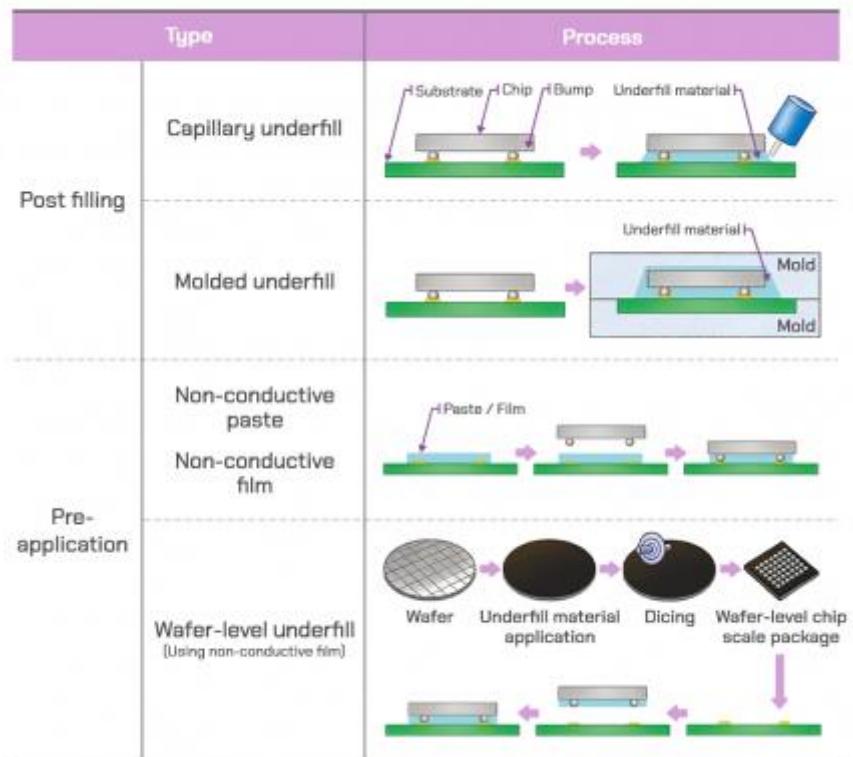


Figure 62 The different types of underfill processes (Source: Hanol Publishing)

The underfill material is a vital component to guarantee the reliability of joints in processes like flip chip and chip stacking using through-silicon via (TSV). Accordingly, the material needs to meet specific requirements for cavity filling, interfacial adhesion, coefficient of thermal expansion<sup>11</sup>, thermal conductivity, and thermal resistance.

<sup>11</sup>**Coefficient of thermal expansion (CTE):** A material property that indicates the extent to which a material expands upon heating.

### Wafer Support System: Using a Carrier, TBA, & Mounting Tape to Assemble the Package

The wafer support system (WSS) process requires a carrier that can support a thin wafer and a temporary bonding adhesive (TBA). After debonding the carrier, mounting tape is also required to firmly attach the thin wafer that formed bumps on its front and back to a ring frame.

Among all the materials that are involved in a WSS, the TBA is the most important. When the wafer and carrier are bonded together to form a TSV package, the TBA must maintain strong adhesion during the backside process without damaging the bumps on the wafer. Thus, there must be no outgassing<sup>12</sup>, voids<sup>13</sup>, delamination<sup>14</sup>, and bleeding out—the seeping out of adhesive from the sides of the wafer during bonding. Consequently, it is crucial to have

both thermal stability and chemical resistance, while the carrier must also be easy to remove without leaving any residue.

<sup>12</sup>**Outgassing:** *The release of a gas from a liquid or solid material. This gas can cause defects in semiconductor devices if it condenses on a surface and affects the device's properties.*

<sup>13</sup>**Voids:** *A gap in a material caused by the formation of air bubbles. These voids can expand during high-temperature processes or debonding, increasing the risk of damage or device failure.*

<sup>14</sup>**Delamination:** *The separation of two previously connected surfaces in a semiconductor package.*

Even though silicon carriers are preferred, glass carriers are also frequently used. This is especially true for processes that use light such as lasers during debonding as they require the use of glass carriers.

### **The Building Blocks of Semiconductor Packaging**

Throughout these articles on the materials that make up conventional packaging and WLP, it has become clear that the type and quality of materials have had to evolve to keep pace with the development of semiconductors. The various reliability tests for semiconductor packages will be introduced in the next episode, which will conclude the back-end process series.

## Episode 11: Reliability Tests and Standards for Semiconductor Packages



### Semiconductor Back-End Process Episode 11

#### Reliability Tests and Standards for Semiconductor Packages

[This series](#) has examined the semiconductor back-end process in detail, covering everything from the different types of semiconductor packages to the packaging process and materials. This final installment of the series will introduce the tests and standards that determine the reliability of semiconductor packages. In addition to detailing how these standards are evaluated and set, this article will also cover the assessments that test semiconductor packages' expected lifetime, reliability in various surrounding conditions, and mechanical reliability.

#### What Is Product Reliability?

The quality of a semiconductor product is determined by how successfully it meets the required standards and properties. Meanwhile, the reliability of a semiconductor device is defined as the probability that it can maintain its quality without failures over a set period of time, thereby increasing customer satisfaction and the likelihood of repeat purchases. In this case, failures refer to errors that occur during the use of the product, while defects are errors that occur during the product's manufacturing or inspection. Therefore, the product is said to be of poor quality if it has many defects, while it is considered to be unreliable if failures occur frequently or while it is under warranty.

## Quality vs Reliability

Types of Differences	Quality	Reliability
Relevance to time	N/A	Applicable
Relevant aspect	Product characteristics	Product lifetime
Target areas	Process quality (present)	Market quality (future)
Applied modeling	Normal distribution	Exponential, Weibull distribution, log-normal distribution
Rating scale	Defect rate	Lifetime, failure rate
Classification criteria	Good quality / defect	Functioning / failure

Figure 63 A table showing the differences between quality and reliability (Source: Hanol Publishing)

Figure 63 shows a more comprehensive breakdown of the differences in the meanings and characteristics of quality and reliability. To give a more detailed definition, reliability is the ability of a system, part, or material to maintain its initial quality and performance over a specific amount of time, distance, or amount of use. This must be achieved without experiencing failures under given conditions such as manner of usage or environmental factors. As a result, it is crucial for semiconductor companies to assess whether their quality and reliability levels have reached industry standards before commencing mass production. These levels should also be regularly examined while products are being mass produced.

As an important step to evaluating product reliability, the standards of reliability must be clearly defined in advance. In the case of a company that ships 100 products, some of the following questions would need to be considered: How many of the products should be operational after three years? What are the observable patterns in the product's operation time? Can it be guaranteed that 90 out of 100 products will be operational after five years? How long will 95 out of 100 products still function properly?

Tests are required to verify these standards. Although it would be ideal to run tests for three years, five years and even longer to determine a product's reliability at these stages, concentrating so much time on the product's evaluation would delay mass production for too long. Therefore, companies use accelerated testing and statistical techniques to assess reliability. Calculations such as reliability functions, lifetime distributions, and the average lifetime are also used to complete a reliability validation in a relatively short amount of time.

## **JEDEC Standards**

Companies that design and manufacture semiconductors evaluate the reliability of their own products and provide customers with the results. Customers can use the results to determine whether the product meets their needs or decide to perform their own reliability assessments. However, if a semiconductor company and its customers have different evaluation criteria, they must go through the trouble of aligning their different standards. As a solution, semiconductor companies usually adhere to standards from the JEDEC Solid State Technology Association<sup>1</sup>, commonly referred to as JEDEC, to satisfy the needs of the company and its customers.

*<sup>1</sup>JEDEC Solid State Technology Association: The leading organization in developing open standards and publications for the microelectronics industry.*

JEDEC's primary role is to enable manufacturers and organizations to jointly review and establish uniform standards for electronic devices such as integrated circuits (ICs). As the specifications set by JEDEC have become widely accepted as the international standard, JEDEC is in effect the standards-setting organization for the semiconductor industry worldwide.

The organization's board of directors (BoD) determines the policies and procedures and has the final approval of JEDEC standards. Additionally, there are also numerous JEDEC committees (JC) which set standards for the respective fields that they are specialized in. For the semiconductor industry, the following are some of the important committees and their roles: JC-14 Quality and Reliability of Solid State Products is responsible for reliability standards; JC-11 Mechanical Standardization sets standards for outlines of modules and semiconductor packages; JC-42 Solid State Memories sets standards for DRAMs; and JC-63 Multiple Chip Packages decides on standards for mobile multi-chip packages.

If a company needs to have a standard created for one of its products, the company submits a standard proposal to be voted on by the respective committee members. Each company has the right to one vote, regardless of its size. Proposals that are approved by a committee are then voted on again by the BoD, and proposals that are passed by the board are finally made into JEDEC standards and publicized to the respective industries.

## **Reliability Tests for Assessing Product Lifetimes**

In addition to international evaluation standards, there are also numerous metrics used to assess product reliability. These include the various assessments which evaluate the lifetime of semiconductor products.

### **Early Failure Rate**

The early failure rate (EFR) estimates the number of device failures which occur within a year in the user environment. For some product lines, however, this period can be reduced to six months or increased to over a year depending on the system's lifetime or products that

specifically require higher reliability. Burn-in<sup>2</sup> screens products that are likely to fail in a short amount of time, while the EFR is used to verify whether the potential failure rate of these screened products is maintained at an acceptable level (see Figure 64). The test conditions are set and evaluated using the acceleration factor for the temperature and voltage of the relevant semiconductor product.

*<sup>2</sup>Burn-in: A test that stresses a product with voltage and temperature in order to eliminate potential defects in the product at an early stage. Burn-in performed after packaging is called test during burn-in (TBDI).*

## An EFR Zone Inside a Reliability Bathtub Curve

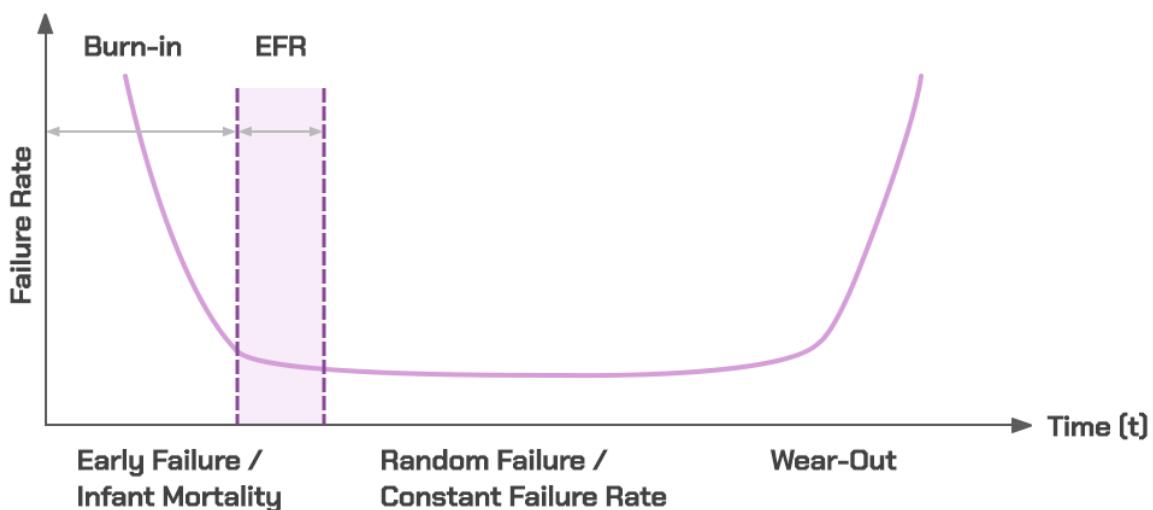


Figure 64 The early failure rate (EFR) zone within a bathtub curve, which represents three phases of a product's failure rate over time (Source: Hanol Publishing)

### High & Low Temperature Operating Life Tests

The high temperature operating life (HTOL) test is one of the most common types of product lifetime evaluations. It assesses issues that arise from temperature and voltage stress during a product's operation. The HTOL test is also considered to be comprehensive as it not only assesses premature failures but also identifies failures caused by accidents or wear and tear. Meanwhile, the low temperature operating life (LTOL) test assesses the likelihood of failures due to the impact of hot carriers<sup>3</sup>. However, due to the application of voltage and temperature, there is also the possibility of other failures occurring.

*<sup>3</sup>Hot carrier: Traveling electrons that become excessively mobile due to the high electric field deriving from transistors shrinking in size and causing the channel length to become shorter, which increases the electric field. This short channel effect occurs in semiconductor transistors.*

### High Temperature Storage Life

The high temperature storage life (HTSL) test evaluates the reliability of a product under high-temperature storage conditions. Such conditions can affect the lifetime of a product due to diffusion, oxidation, intermetallic growth, and chemical degradation of package materials.

### Endurance & Data Retention

The endurance test evaluates how many program/erase (PE) cycles products such as NAND flash memory can withstand. Regarding NAND, a key reliability factor of these products is data retention as it measures how long data will be stored in a cell for a given period of time even in the absence of power.

### **Reliability Tests for Various Surrounding Conditions**

There are numerous surrounding conditions that may contribute to the failure of a semiconductor product. This is why tests are required to assess the ability of products to withstand certain surrounding conditions before they are shipped to their respective destinations.

### Preconditioning

After a product has been shipped and stored, preconditioning assesses potential problems that may occur during a customer's manufacturing process as hygroscopic<sup>4</sup> and thermal stress can result in reliability issues. Preconditioning evaluates packaging reliability in humid conditions by replicating conditions where the product is sold, shipped to the customer, unpacked from its vacuum packaging, and mounted in the system. This treatment is used as a precursor for reliability tests of surrounding conditions, including temperature humidity bias (THB), the highly accelerated stress test (HAST), and thermal cycle (TC).

*<sup>4</sup>Hygroscopic: The phenomenon of absorbing moisture from the air. In semiconductors, this absorption of moisture can lead to failures.*

The evaluation follows the order of TC, bake, soak, and reflow. Figure 65 shows how preconditioning applies to the processes of packaging, transportation, and mounting to the system.

## Product Manufacturing and Preconditioning

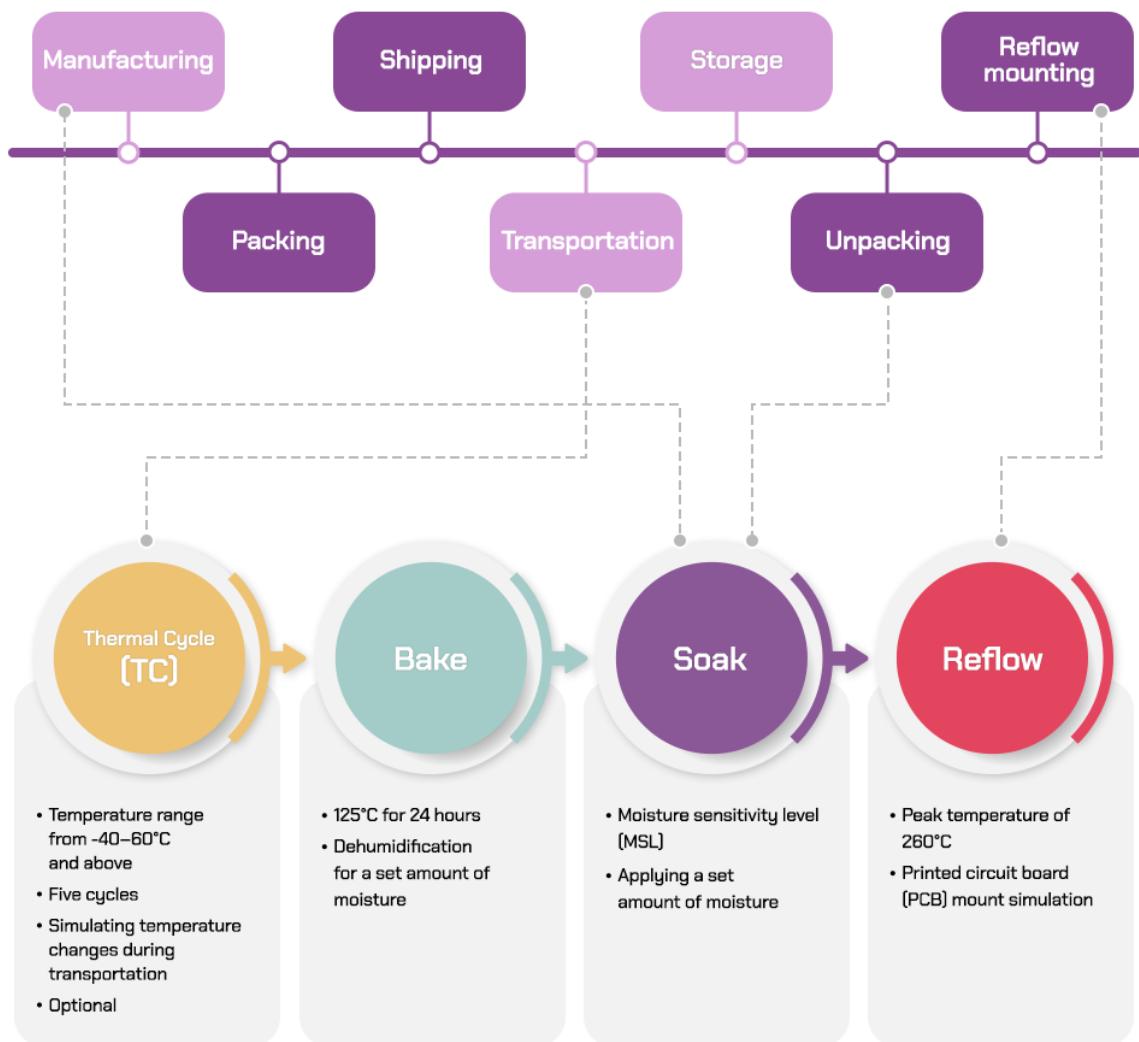


Figure 65 Relationship of production, transportation, and usage to preconditioning test conditions (Source: Hanol Publishing)

### Thermal Cycle

A thermal cycle (TC) assesses a product's tolerance to instantaneous temperature changes that may occur in different user environments. Semiconductor packages and modules are composed of various materials with different coefficients of thermal expansion<sup>5</sup> (CTE) which can lead to stress-induced fatigue failures. This stress is caused by shrinkage and expansion which occurs following thermal changes.

<sup>5</sup>**Coefficient of thermal expansion (CTE):** A material property that indicates the extent to which a material expands upon heating.

The primary purpose of a TC is to measure the stress tolerance of a semiconductor package in relation to temperature changes, but high and low temperature stresses can cause many other failures. Prolonged thermal shocks verify the potential for interfacial delamination<sup>6</sup>, internal and external package cracks, and chip cracks caused by factors such as stress from each package material or thermal expansion. In addition, as the importance of solder joints is increasing due to restrictions on the use of hazardous materials including lead and the expansion of applications such as mobile devices, a TC can effectively evaluate the reliability of solder joints.

<sup>6</sup>**Interfacial delamination:** *The separation of interfaces in a semiconductor package.*

#### Temperature Humidity Storage & Temperature Humidity Bias Tests

The temperature humidity storage (THS) test assesses the tolerance of semiconductor products in high temperatures and humidity. To determine the appropriate exposure time, it is recommended to simulate the actual user environment by measuring the amount of moisture absorption after opening the moisture-proof package. Meanwhile, temperature humidity bias (THB) evaluates moisture resistance by subjecting the product to an electrical bias<sup>7</sup>. Although most failures are caused by aluminum corrosion, other potential problems can arise from temperature stress. This test also identifies package reliability issues such as pad metal corrosion due to moisture penetrating through micro gaps between leads and mold pores, and failures caused by moisture infiltrating through pores or holes in the protective film.

<sup>7</sup>**Electrical bias:** *The deliberate application of direct current (DC) between two points for the purpose of controlling a circuit.*

#### Pressure Cooker Test

The pressure cooker test (PCT), which is more rigorous than THS and THB, is an ideal early assessment of moisture resistance. Also known as an autoclave<sup>8</sup>, the test evaluates the moisture resistance of a plastic mold compound and assesses the reliability of the mold structure by infiltrating moisture using 100% relative humidity and high pressure. Additionally, it identifies problems arising from moisture penetration between the leads and through pores in the mold.

<sup>8</sup>**Autoclave:** *A high-pressure cooker. When water is added while the cooker is sealed at high temperature, the water evaporates and increases the pressure and humidity to create the conditions necessary for the specimen inside the autoclave.*

Similar to THS, the PCT used to be an essential reliability test for thick semiconductor packages. However, recent international trends, including JEDEC's assessment, suggest that the stress magnitude is too high for current packages. Thus, the test is used selectively depending on the type of package. The PCT is used for leadframe products, while the unbiased highly accelerated stress test (UHAST) is used for substrate products.

## Unbiased Highly Accelerated Stress Test, Highly Accelerated Stress Test & High Accelerated Life Test

The UHAST evaluates reliability by applying stresses similar to those applied by a PCT to thin packages of substrate-type products, such as fine-pitch ball grid array (FBGA) packages. There are also similarities in their ability to identify and discover types of failures. While the PCT applies stress by using saturated humidity, or 100% relative humidity, the UHAST uses unsaturated humidified conditions at 85% relative humidity that is similar to the customer user environment. Galvanic corrosion<sup>9</sup> or direct chemical corrosion are mainly employed for this evaluation.

<sup>9</sup>**Galvanic corrosion:** An electrochemical process whereby a more active metal (anode) corrodes in preference to a more resistant metal (cathode) that it is in contact with through an electrolyte.

An additional evaluation is the highly accelerated stress test (HAST) which is used to assess the reliability of non-hermetic packages operating in humid environments. It uses the same method as THB, as pins with static bias applied undergo temperature, humidity, and pressure stresses. Lastly, the highly accelerated life test (HALT) is a quick stress test that helps identify and correct defects during the product design phase.

## **Reliability Tests for Mechanical Factors**

Semiconductor products are subjected to environmental stresses caused by mechanical, climatic, and electrical factors during their handling, storage, transportation, and operation. These loads significantly affect the design reliability of the equipment. For this reason, it is necessary to evaluate products under development or in mass production to identify abnormalities. Manufacturers can subject products to physical stresses such as vibration, shocks, and drops during the assessment process.

### Shock

Shock testing evaluates resistance to simulated impacts that may occur during handling and transportation. Typical shock tests include the hammer shock test, which involves fixing a test sample in place and striking it with a hammer, and the drop test, in which a product is subjected to a free-fall drop. The hammer shock test assesses how well a product withstands the force and pulse of the hammer, as well as the number of impacts it can endure. In the case of the drop test, the test subject is dropped in free fall from a height of 1 to 1.2 meters to reflect the actual working environment of the user.

### Vibration, Bending & Torsion

Vibration is an assessment of the product's resistance to vibrations that may occur when the product is being transported. It usually employs sine vibration<sup>10</sup> testing in compliance with JEDEC standards.

<sup>10</sup>**Sine vibration:** A vibration that varies in frequency over time.

Other tests include the bending test, which assesses solder joint defects caused by warping or bending on the printed circuit board (PCB), as well as the torsion test. Also referred to as the twist or torque test, the torsion test evaluates the resistance to solder joint problems and product warpage that may occur on the PCB when it is subjected to torsional stress.

### **Ensuring Reliable Semiconductor Products**

The reliability tests and standards discussed in this episode serve as the foundation for ensuring that these vital components meet the stringent demands of today's technology-driven world. From tests for surrounding conditions and mechanical factors to product lifetime evaluations, the various assessments show that the semiconductor industry is committed to producing reliable and durable products. In particular, SK hynix is doing its utmost to ensure its products meet the highest reliability standards and exceed customer expectations. Going forward, the company will continue refining and reviewing its reliability testing to keep pace with the ever-evolving technological landscape.

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