20

MCU Tips

For Board Designers

MCU BOARD DESIGN CHECK LIST

POWER SYSTEMS (Foundation - Must be designed first)

1. Decoupling Capacitor Method
2. Separate Analog/Digital Supplies
3. Voltage Monitoring
4. Real-Time-Clock Battery Backup

BOOT & RESET (Critical startup behavior)

5. Proper Reset Circuit
6. Booto Pin Handling

PIN PLANNING (Resource allocation before layout)

7. PINs Allocation using CubeMX
8. Use Remappable Pins Option
9. Pay attention to reserved Pins
10. Unused Pin Termination

SIGNAL INTEGRITY (Communication and timing)

11. External vs Internal Oscillator
12. Series Resistors on High-Speed Outputs
13. GPIO limits and Protection
14. PIN Voltage Awareness

PERIPHERAL INTERFACES (External connections)

15. Programming Access
16. External Memory Support
17. Timer Pin Selection Consideration

ANALOG DESIGN (Precision measurements)

18. ADC Input Proper Design

SYSTEM LIMITS (Operating boundaries)

19. GPIO Output Drive Limits

MANUFACTURING (Production support)

20. Debug & Test Points

INTRODUCTION

Modern MCU board design demands systematic approaches to prevent common failures and ensure reliable operation. This guide presents 20 critical design considerations that directly impact system functionality, manufacturability, and long-term reliability.
Each tip addresses specific failure modes observed across thousands of deployed systems.

CORE DESIGN PRINCIPLES:

- Power supply integrity forms the foundation of all other functions
- Signal conditioning prevents data corruption and communication failures
- Protection circuits safeguard against environmental and electrical stress
- Test accessibility enables efficient manufacturing and field support
- Pin allocation optimization simplifies layout and reduces costs

APPLICATION FOCUS

While this guide emphasizes STM32F series MCUs, the principles apply broadly to modern 32-bit MCU families. Design decisions should always be validated against specific device datasheets and application requirements.

USING THIS GUIDE

Each chapter follows a consistent structure with implementation guidelines, component selection criteria, and design validation requirements. Tables provide specific parameter values while text explains the underlying rationale.

DESIGN WORKFLOW:

- Review all 20 tips during initial schematic design
- Validate critical parameters before PCB layout
- Implement protection and monitoring circuits early
- Plan for test access and manufacturing requirements
- Document design decisions for future reference

1.DECOUPLING CAPACITOR

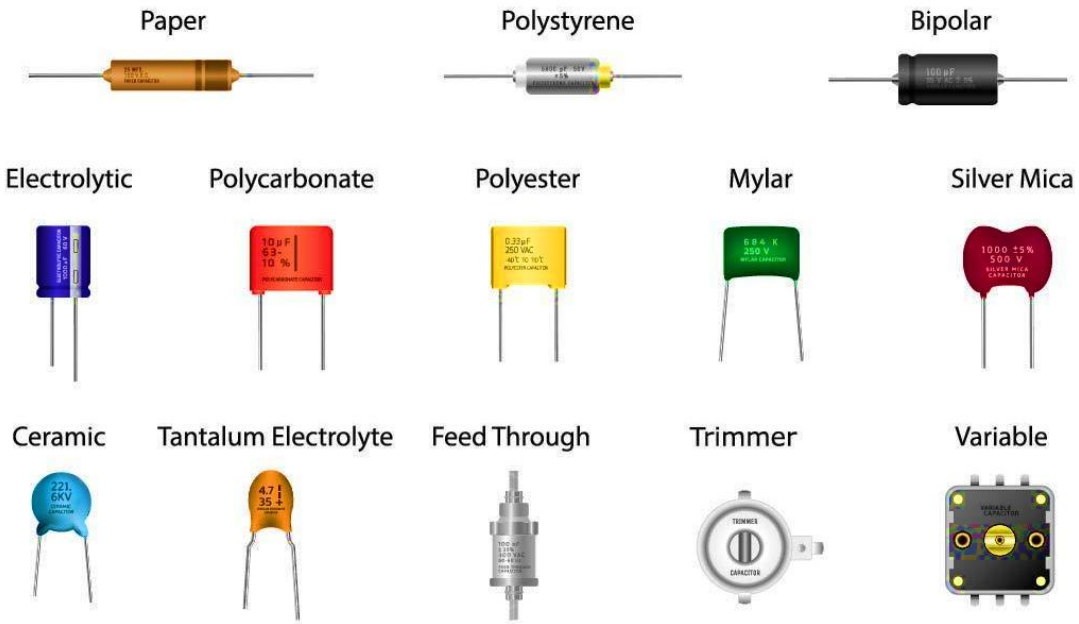
Proper decoupling capacitor placement forms the foundation of reliable MCU operation. Inadequate decoupling causes supply voltage fluctuations that manifest as reset conditions, communication errors, and intermittent failures.

1.1 CAPACITOR SELECTION CRITERIA

Multiple capacitor values provide effective decoupling across different frequency ranges. The combination addresses both high-frequency switching noise and lower-frequency load transients.

CAP SELECTION:

CAP VALUE	PRIMARY FUNCTION	DISTANCE
100nF	High-frequency decoupling	<5mm from VDD pin
1µF	Mid-frequency filtering	<10mm from VDD pin
10µF	Bulk capacitance	<20mm from VDD pin

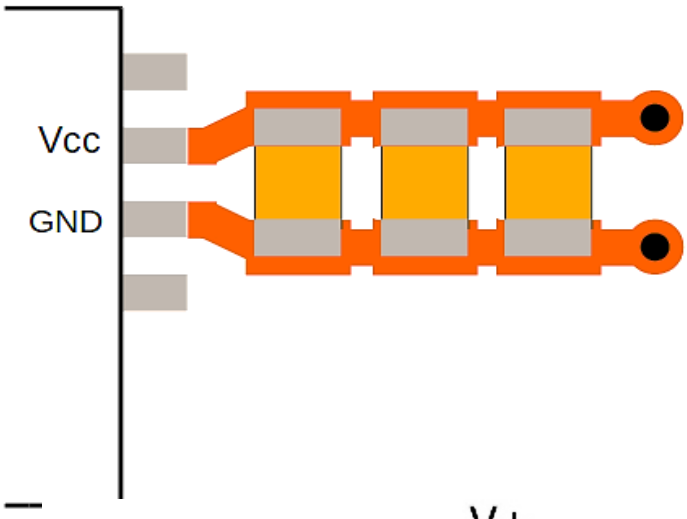


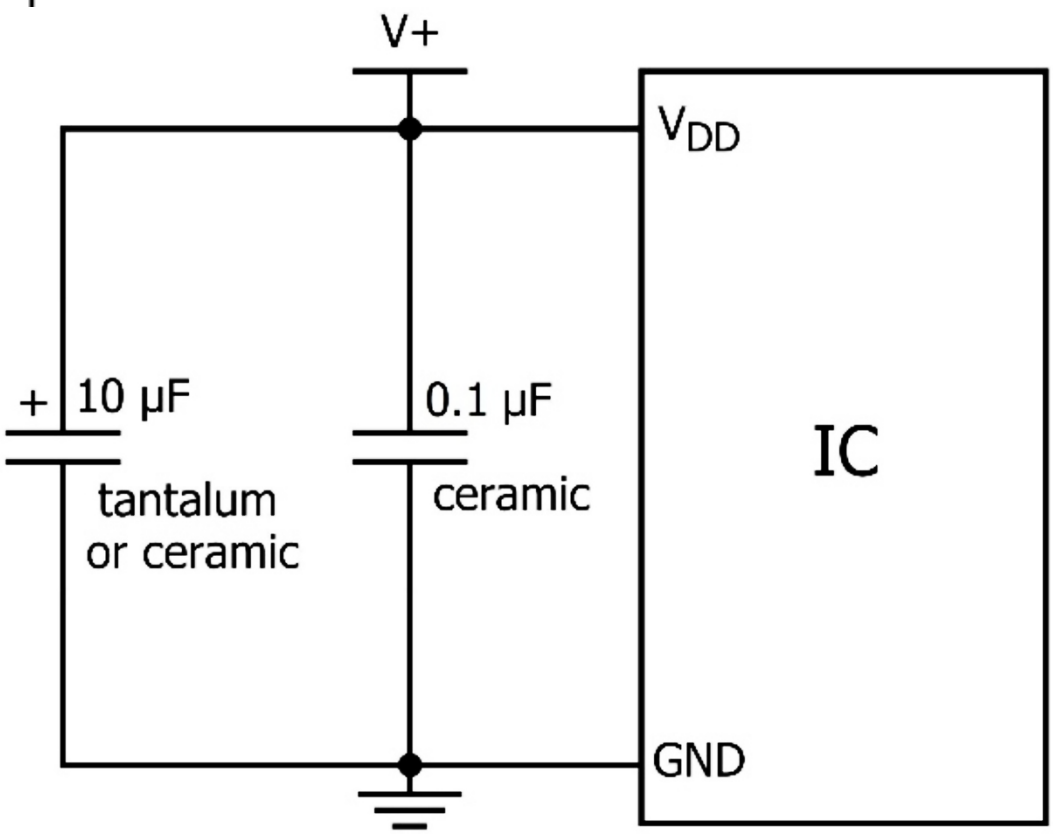
1.2 PLACEMENT GUIDELINES

Each VDD pin requires dedicated high-frequency decoupling. MCU devices typically have multiple VDD pins requiring individual attention.

KEY IMPLEMENTATION POINTS:

- Place 100nF capacitors on the same PCB layer as the MCU
- Minimize via count in decoupling paths
- Use shortest possible traces between capacitor and VDD/VSS pins
- Position bulk capacitance near the power input connector





2.ANALOG/DIGITAL RAILS

Analog and digital circuit separation reduces noise coupling and improves ADC performance. Proper supply domain design is critical for mixed-signal applications.

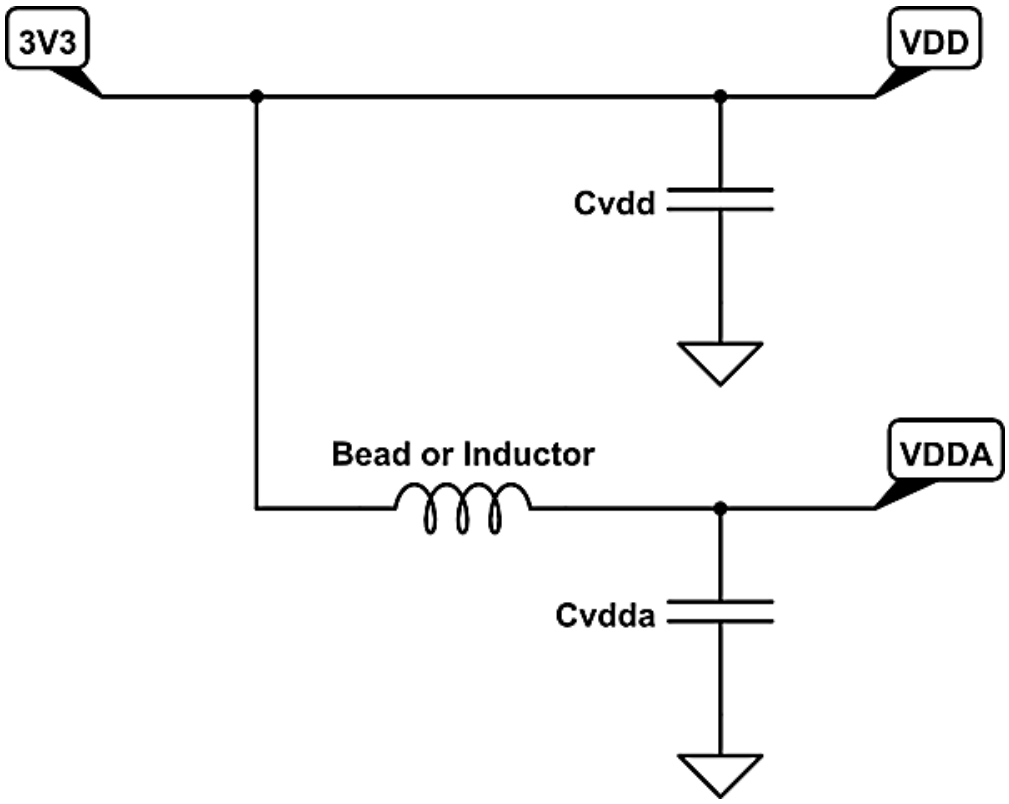
2.1 VDDA FILTERING DESIGN

Analog supply filtering removes digital switching noise that degrades ADC resolution and accuracy. Multi-stage filtering provides broadband noise reduction.

FILTERING STAGES:

1. Series ferrite bead (100Ω @ 100MHz)
2. Bulk capacitance (10µF to 100µF)
3. High-frequency bypassing (100nF)
4. Local decoupling at AVDD pins

Ferrite bead selection balances DC resistance and high-frequency impedance. Low DC resistance minimizes voltage drop while maintaining filtering effectiveness.



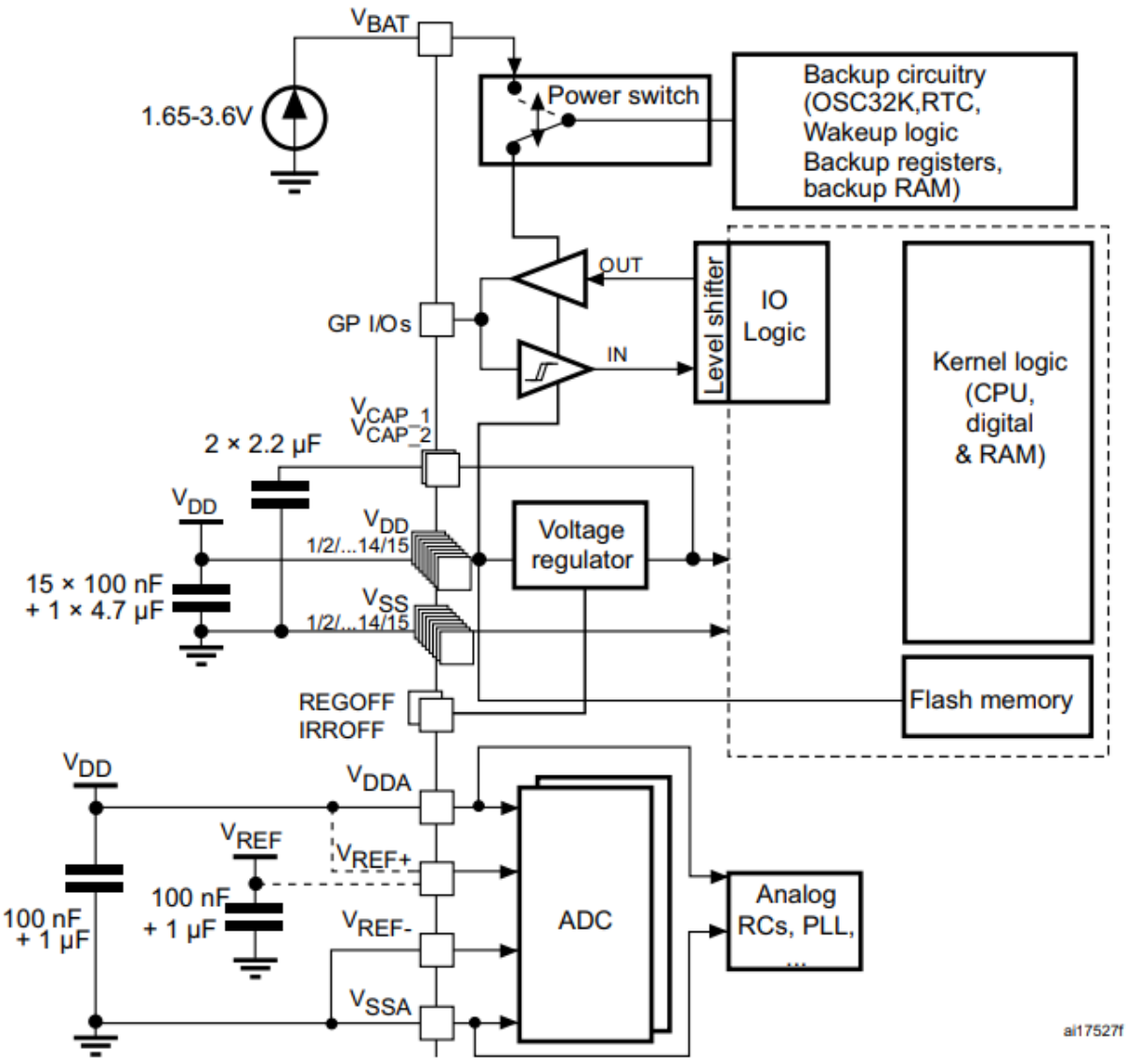
2.2 MCU POWER DESIGN

There are many Power pins and each one needs special attention.

Use the following Diagram to make sure the power lines are handled properly.

TYPES OF SUPPLIES AND POWER PINS:

- **VBAT** – Battery Supply
- **VDD** – Main Digital Supply
- **VSS** – Digital Ground
- **VDDA** – Analog Supply
- **VSSA** – Analog Ground
- **VREF** – ADC and DAC voltage reference



3.VOLTAGE MONITORING

Voltage monitoring enables real-time power supply supervision and fault detection through MCU ADC channels. Proper monitoring prevents system damage, enables predictive maintenance, and improves overall system reliability.

3.1 MONITORING CIRCUIT DESIGN

Voltage divider networks scale supply voltages to MCU ADC input ranges. Divider design must balance accuracy, power consumption, and input impedance requirements.

DESIGN REQUIREMENTS:

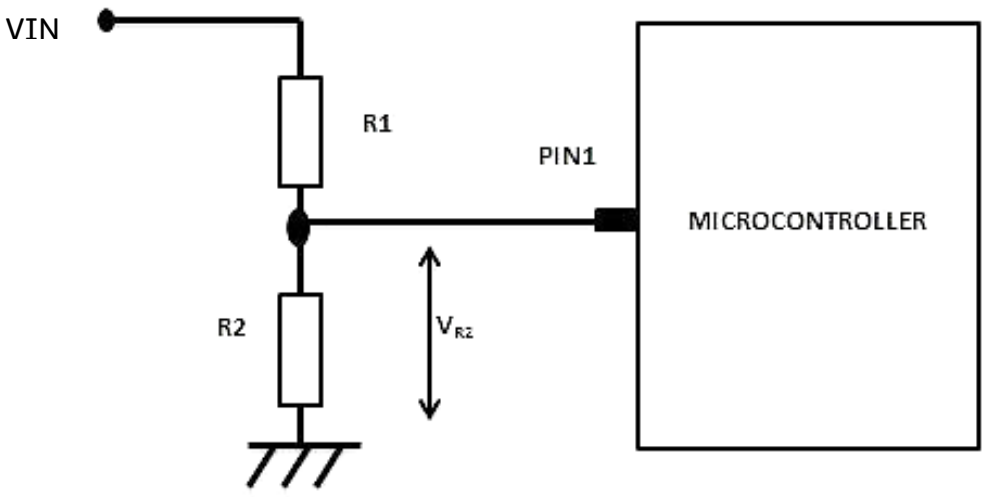
- Scale voltages to ADC input range (typically 0-3.3V)
- Maintain measurement accuracy across temperature
- Minimize power consumption through divider chain
- Provide adequate input impedance for ADC operation

DIVIDER CALCULATION:

VADC = VIN × R2 / (R1 + R2)

Where:

- VIN = Input voltage being monitored
- R1 = Upper divider resistor
- R2 = Lower divider resistor
- VADC = Voltage presented to ADC input



3.2 RESISTOR SELECTION

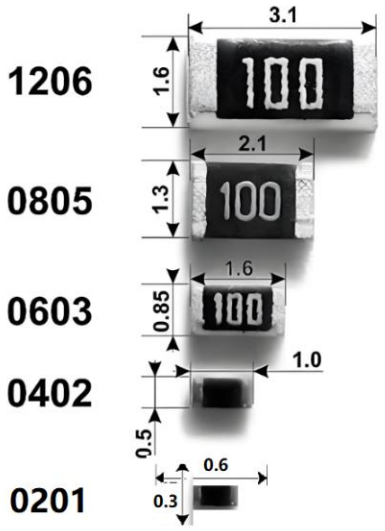
When multiple rails are being monitored each one will have its own ADC input with the proper voltage divider design.

IMPLEMENTATION CONSIDERATIONS:

- Calculate divider ratios for maximum ADC resolution utilization
- Consider supply voltage tolerance in divider design
- Use precision resistors (±1%) for accurate monitoring
- Include filtering capacitors to reduce noise on monitoring inputs
- Plan for temperature coefficient effects on divider accuracy

Selection Guidelines:

SUPPLY	R1 VALUE	R2 VALUE	CURRENT	ADC VOLTAGE
5V	10kΩ	6.8kΩ	297µA	2.02V
12V	22kΩ	6.8kΩ	417µA	2.83V
24V	47kΩ	6.8kΩ	446µA	3.04V
3.3V	Use Diode	NC	0µA	~3V



	Size	Power
0201	0. 6*0. 3MM	1/20W
0402	1. 0*0. 5MM	1/16W
0603	1. 6*0. 8MM	1/10W
0805	2. 0*1. 2MM	1/8W
1206	3. 2*1. 6MM	1/4W
1210	3. 2*2. 5MM	1/3W
1812	4. 8*3. 2MM	1/2W
2010	5. 0*2. 5MM	3/4W
2512	6. 4*3. 2MM	1W

FILTERING REQUIREMENTS:

Small capacitors (10nF to 100nF) across the lower divider resistor reduce high-frequency noise without affecting DC accuracy. Larger capacitors may introduce settling time delays.

4.REAL-TIME-CLOCK

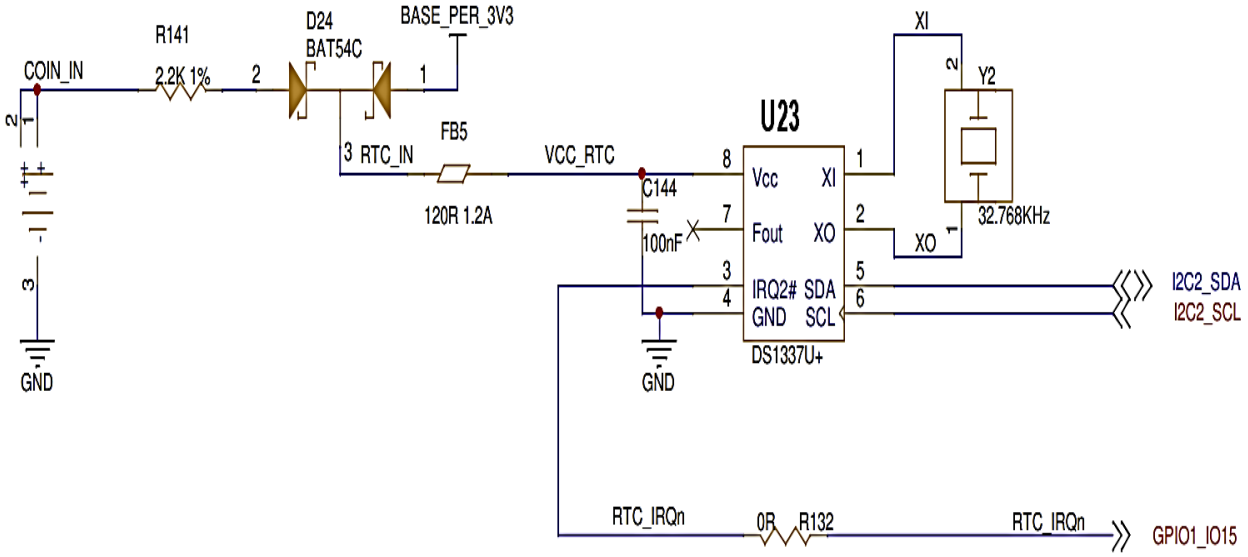
Real-Time Clock (RTC) circuits with battery backup maintain time and date during power loss. Proper battery backup design ensures reliable timekeeping and extends battery life.

4.1 BATTERY BACKUP CIRCUIT

Battery backup circuits automatically switch between main power and battery power. Diode networks and analog switches provide seamless power source switching.

BACKUP POWER SOURCES:

- Lithium coin cells: 3V, long life, temperature stable
- Super capacitors: Rechargeable, finite life, temperature sensitive
- NiMH batteries: Rechargeable, voltage matching challenges
- Primary lithium: Non-rechargeable, excellent shelf life



4.2 VBAT DOMAIN DESIGN

VBAT power domain includes RTC circuits, backup SRAM, and tamper detection functions.

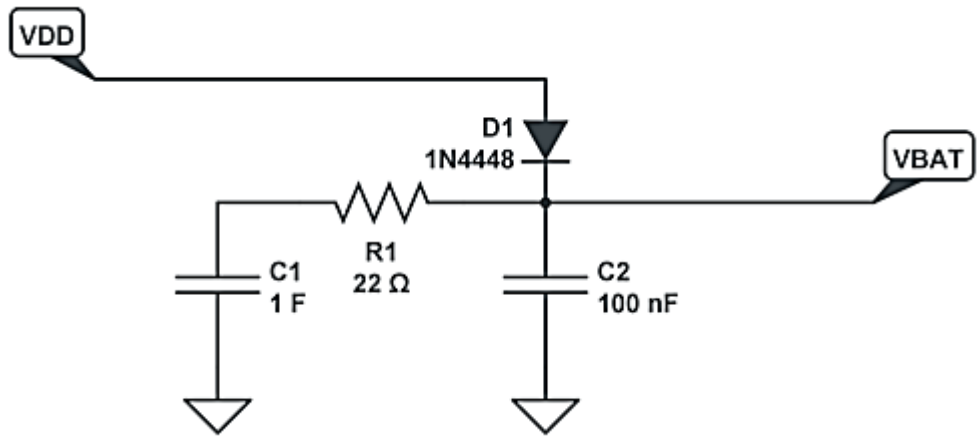
Domain isolation prevents main system power from loading battery backup.

VBAT DESIGN CONSIDERATIONS:

- Minimize current consumption: <1μA typical requirement
- Isolation switching: Prevent reverse current flow
- Crystal oscillator: Low-power 32.768 kHz operation
- Capacitive loading: Minimize to reduce power consumption

IMPLEMENTATION GUIDELINES:

- Use low-leakage components in VBAT domain
- Use Supercap as battery for RTC (C1)
- Consider temperature effects
- Decouple the supply (C2)



5.RESET CIRCUIT

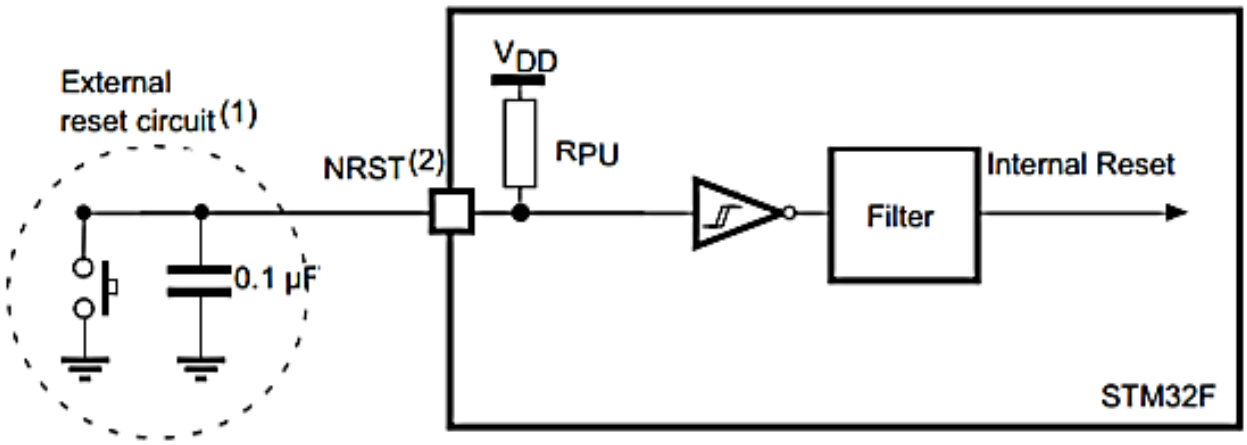
Reliable reset generation ensures consistent startup behavior across all operating conditions. Inadequate reset circuits cause erratic behavior during power transitions and brown-out conditions.

5.1 EXTERNAL RESET IC SELECTION

Dedicated reset ICs provide superior performance compared to simple RC circuits. These devices monitor supply voltage and generate clean reset pulses.

RECOMMENDED RESET IC FEATURES:

- Precise threshold voltage (typically 2.9V for 3.3V systems)
- Hysteresis to prevent oscillation
- Reset timeout period (100ms minimum)
- Low quiescent current (<10µA)
- Open-drain output for wired-OR configurations



5.2 RESET IC

A RESET IC is a tiny chip whose job is to ensure that a MCU or digital system always starts in a known, stable state. It continuously monitors the supply voltage and, if the voltage dips below a safe threshold, it holds the line active until power stabilizes.

RESET CIRCUIT STM1001:

compact reset circuit from STMicroelectronics.

It can monitor common supply rails (3 V, 3.3 V, and 5 V), provides an open-drain reset output, and guarantees a reset pulse of at least 30 ms or 140 ms depending on version.

RESET IC ADVATAGES:

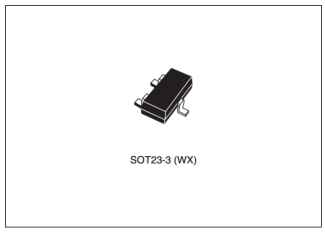
- Precise Startup:
- Reliable Brown-Out Detection:
- Noise Immunity:
- Consistent Reset Pulse:
- Extra Features:

STM1001

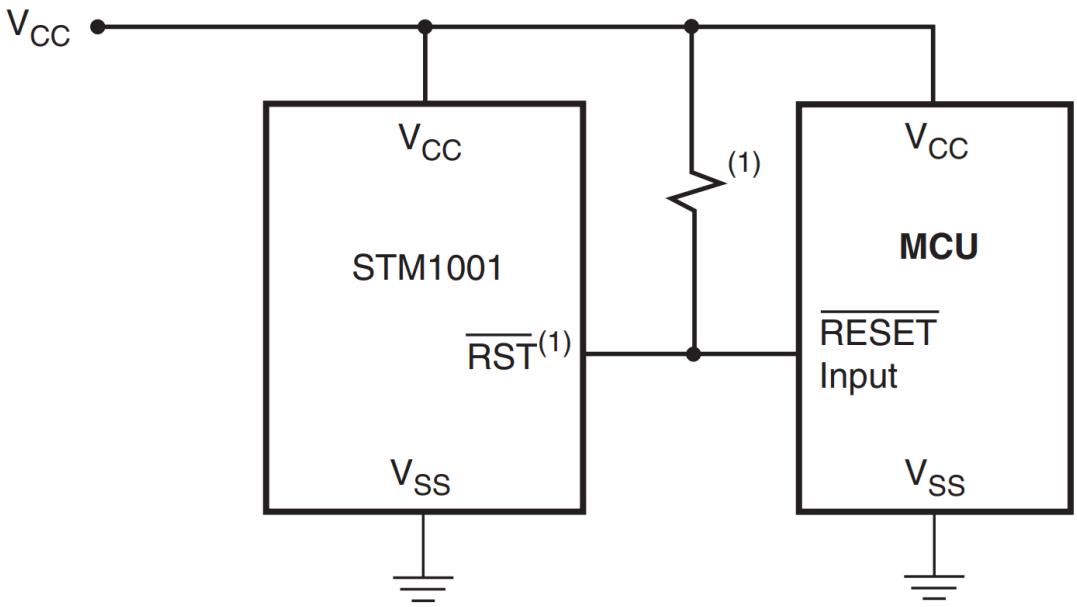
Reset circuit

Features

- Precision monitoring of 3 V, 3.3 V, and 5 V supply voltages
- Open drain $\overline{RST}$ output
- 30 ms or 140 ms reset pulse width (min)
- Low supply current - 6 µA (typ)
- Guaranteed $\overline{RST}$ assertion down to V_{CC}= 1.0 V
- Operating temperature:
  - –40 °C to 85 °C (industrial grade)
- Lead-free, small SOT23 package



SOT23-3 (WX)



6.BOOT0 PIN

Boot pin configuration determines the MCU's startup behavior. Improper handling causes unpredictable boot sequences and prevents normal program execution.

6.1 BOOT MODE SELECTION

STM32F devices support multiple boot modes determined by BOOT0 and BOOT1 pin states. Understanding these combinations prevents accidental boot loader entry. Production boards should default to main flash execution. Development boards may include jumpers or switches for boot mode selection.

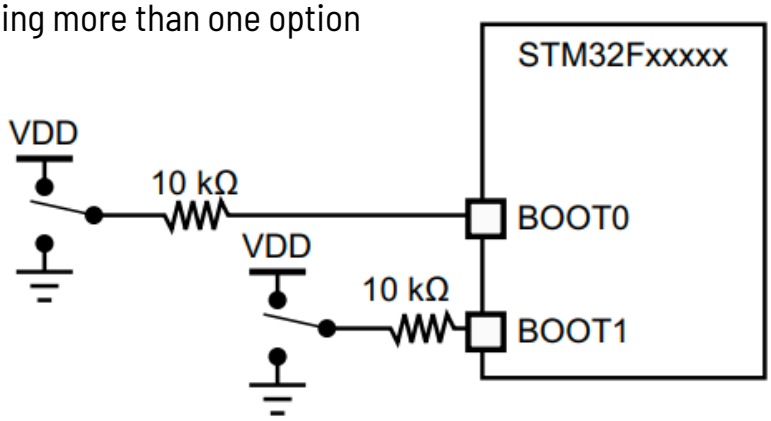
Boot mode selection pins		Boot mode	Aliasing
BOOT1	BOOT0		
x	0	Main Flash memory	Main Flash memory is selected as the boot area
0	1	System memory	System memory is selected as the boot area
1	1	Embedded SRAM	Embedded SRAM is selected as the boot area

6.2 PULL RESISTOR CONFIGURATION

The BOOT0 pin requires external bias to ensure predictable boot mode selection. Internal weak pull-downs may be insufficient under noisy conditions.

STANDARD CONFIGURATION:

- Normal operation: 10kΩ pull-down to ground
- Boot loader mode: 10kΩ pull-up to VDD (when required)
- Never leave BOOT0 floating
- Make the design flexible by allowing more than one option



7.PINS ALLOCATION

STM32CubeMX software enables systematic pin allocation and conflict resolution. Proper use prevents pin conflicts and optimizes peripheral placement for board layout efficiency.

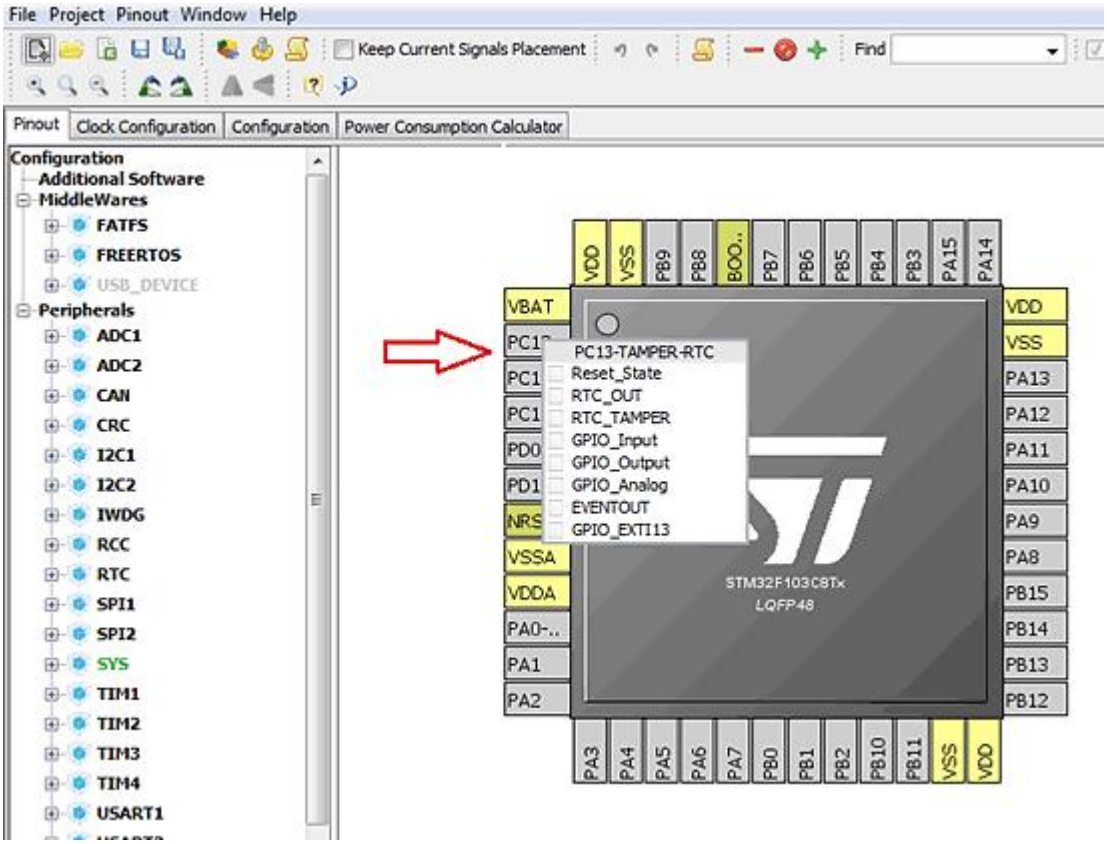
7.1 PIN CONFLICT RESOLUTION

Pin conflicts occur when multiple peripherals require the same physical pins. CubeMX identifies conflicts and suggests alternative configurations.

COMMON CONFLICT SOURCES:

- Shared alternate function pins
- Overlapping peripheral pin requirements
- Boot pin conflicts with peripheral functions
- Debug interface pin usage

CubeMX conflict resolution displays alternative pin assignments and highlights unavailable combinations. Systematic resolution prevents late-stage design changes.



7.2 PERIPHERAL MAPPING

Peripheral mapping optimization considers electrical requirements, PCB routing complexity, and mechanical constraints. Strategic pin assignment simplifies board layout.

PIN ASSIGNMENT PRIORITIES:

1. Critical timing signals (clocks, strobes)
2. High-speed communication interfaces
3. Analog inputs requiring special handling
4. Power-sensitive functions
5. General purpose I/O

MAPPING CONSIDERATIONS:

PERIPHERAL	PIN CONSTRAINTS	LAYOUT IMPACT
ADC inputs	Analog-capable pins only	Quiet routing areas
PWM outputs	Timer-capable pins	Power switching areas
Communication	alternate functions	Interface connector proximity
Boot/Reset pins	Dedicated functions	Programming header access

Transistor applications include pin function multiplexing and dynamic reconfiguration. Analog switches enable run-time pin function changes.

CUBEMX BEST PRACTICES:

- Start with critical peripherals requiring specific pins
- Group related functions on nearby pins for routing efficiency
- Consider package pin limitations early in design process
- Validate pin assignments against electrical requirements
- Export configuration for documentation and version control

7.3 JTAG CONSIDERATIONS

JTAG interfaces offer additional debugging capabilities but require more PCB real estate. Consider JTAG when advanced debugging features are essential.

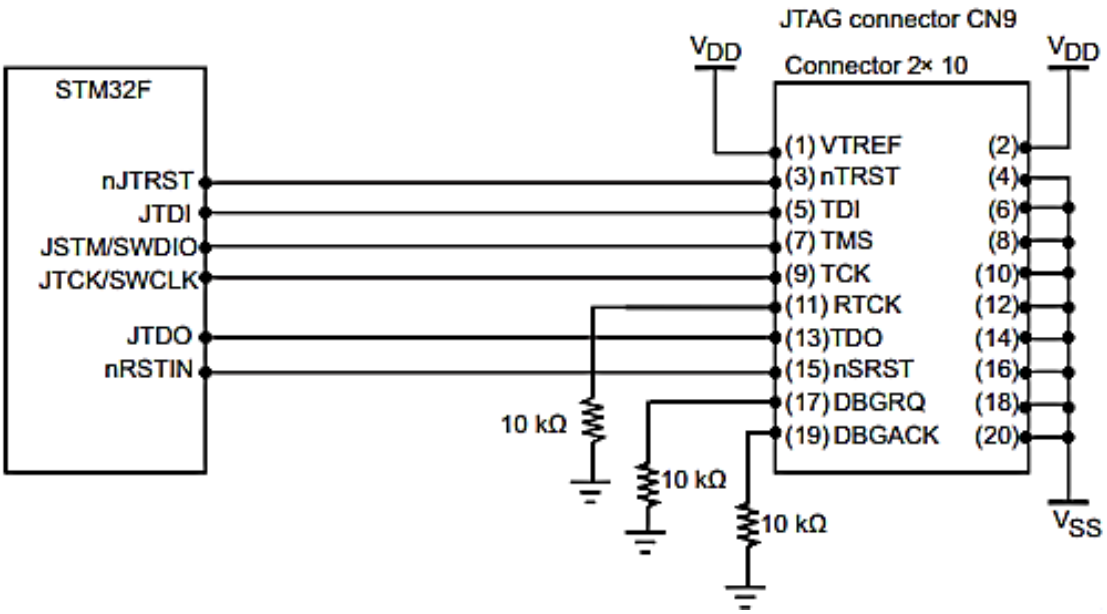
JTAG SIGNAL REQUIREMENTS:

- TMS (mode select)
- TCK (clock)
- TDI (data input)
- TDO (data output)
- NRST (reset)
- VDD and GND references

Transistor applications include level shifting between programmer voltage domains and target MCU levels. MOSFET-based level shifters handle bidirectional signals effectively.

DESIGN GUIDELINES:

- Use 22Ω series resistors on high-speed debug signals
- Maintain controlled impedance (50Ω) for debug traces
- Include pull-up resistors on TMS and TDI pins
- Position headers away from high-current switching circuits
- Consider ESD protection on exposed debug pins



8.REMAPPABLE PINS

Pin remapping features provide flexibility in peripheral placement and resolve pin conflicts. Understanding remapping capabilities enables optimal pin utilization.

8.1 ALTERNATE FUNCTIONS

Pin remapping allows peripheral functions to use alternative pin locations. This flexibility improves board layout efficiency and resolves resource conflicts.

REMAPPING APPLICATIONS:

- Resolve pin conflicts between peripherals
- Optimize PCB routing by moving functions to convenient locations
- Enable peripheral clustering for improved performance
- Provide design variations without hardware changes

Table 11. Alternate functions selected through GPIOA_AFR registers for port A

Pin name	AF0	AF1	AF2	AF3	AF4	AF5	AF6	AF7
PA0	-	USART2_CTS	-	-	USART4_TX(1)	-	-	-
PA1	EVENTOUT	USART2_RTS	-	-	USART4_RX(1)	TIM15_CH1N(1)	-	-
PA2	TIM15_CH1(1)	USART2_TX	-	-	-	-	-	-
PA3	TIM15_CH2(1)	USART2_RX	-	-	-	-	-	-
PA4	SPI1_NSS	USART2_CK	USB_NOE(2)	-	TIM14_CH1	-	-	-
PA5	SPI1_SCK	-	-	-	-	-	-	-
PA6	SPI1_MISO	TIM3_CH1	TIM1_BKIN	-	USART3_CTS(1)	TIM16_CH1	EVENTOUT	-
PA7	SPI1_MOSI	TIM3_CH2	TIM1_CH1N	-	TIM14_CH1	TIM17_CH1	EVENTOUT	-
PA8	MCO	USART1_CK	TIM1_CH1	EVENTOUT	-	-	-	-
PA9	TIM15_BKIN(1)	USART1_TX	TIM1_CH2	-	I2C1_SCL (2)	-	-	-
PA10	TIM17_BKIN	USART1_RX	TIM1_CH3	-	I2C1_SDA (2)	-	-	-
PA11	EVENTOUT	USART1_CTS	TIM1_CH4	-	-	-	-	-
PA12	EVENTOUT	USART1_RTS	TIM1_ETR	-	-	-	-	-
PA13	SWDIO	IR_OUT	USB_NOE	-	-	-	-	-
PA14	SWCLK	USART2_TX	-	-	-	-	-	-
PA15	SPI1_NSS	USART2_RX	-	EVENTOUT	USART4_RTS(1)	-	-	-

9.RESERVED PINS

Critical MCU pins require careful loading consideration. Heavy capacitive or resistive loads on boot, reset, or crystal pins cause startup failures and erratic behavior.

9.1 FIXED FUNCTION PINS

Dedicated Pins such as power or reset must be handled properly. Some of them can't be used as GPIOs and each one may demand different design.

STM32 SPECIAL PINS:

PIN	FUNCTION	BEST PRACTICE
VDD, VSS	Core power	Connect all pins, decouple with multiple caps
VDDA, VSSA	Analog supply	Decouple, do not merge with digital
VREF+	ADC/DAC REF	Supply clean, quiet reference voltage
NRST	Reset	Pull-up resistor
BOOT0/BOOT1	Boot mode	External PU/PD, accessible jumper
SWDIO, SWCLK	Program MCU	Route to accessible header/pads
OSC_IN, OSC_OUT	crystal oscillator	Short, matched layout, load caps near pin

GPIO FUNCTIONS:

<table>
<tr><th colspan="2">Configuration mode</th><th>CNF1</th><th>CNF0</th><th>MODE1</th><th>MODE0</th><th>PxODR register</th></tr>
<tr><td rowspan="2">General purpose output</td><td>Push-pull</td><td rowspan="2">0</td><td>0</td><td rowspan="4">01
10
11
see Table 21</td><td rowspan="4"></td><td>0 or 1</td></tr>
<tr><td>Open-drain</td><td>1</td><td>0 or 1</td></tr>
<tr><td rowspan="2">Alternate Function output</td><td>Push-pull</td><td rowspan="2">1</td><td>0</td><td>Don’t care</td></tr>
<tr><td>Open-drain</td><td>1</td><td>Don’t care</td></tr>
<tr><td rowspan="4">Input</td><td>Analog</td><td rowspan="2">0</td><td>0</td><td rowspan="4">00</td><td rowspan="4"></td><td>Don’t care</td></tr>
<tr><td>Input floating</td><td>1</td><td>Don’t care</td></tr>
<tr><td>Input pull-down</td><td rowspan="2">1</td><td rowspan="2">0</td><td>0</td></tr>
<tr><td>Input pull-up</td><td>1</td></tr>
</table>

10.UNUSED PIN

Proper unused pin termination prevents floating inputs and reduces power consumption. Floating pins act as antennas, introducing noise and causing unpredictable behavior.

10.1 INPUT CONFIGURATION

Configure unused pins as inputs with pull-up or pull-down resistors. This approach minimizes current consumption while providing defined logic states.

TERMINATION METHODS:

- Pull-up to VDD: Logic high default state
- Pull-down to ground: Logic low default state
- Internal pull-ups/pull-downs: When available and sufficient

Resistor values between 4.7kΩ and 47kΩ provide adequate bias without excessive current draw. Stronger pull-up/pull-down resistors (1kΩ to 4.7kΩ) may be necessary in high-noise environments.

10.2 OUTPUT TERMINATION

Configuring unused pins as outputs tied to defined logic levels eliminates floating conditions. This method provides maximum noise immunity but increases power consumption slightly.

OUTPUT CONFIGURATION GUIDELINES:

- Tie outputs to ground (logic low) when possible
- Use VDD connection for open-drain outputs requiring pull-up
- Avoid connecting outputs to power rails through low impedance paths
- Group adjacent unused pins for efficient PCB routing

11.EXT/INT OSCILLATOR

Clock source selection impacts timing accuracy, power consumption, and PCB complexity. Understanding trade-offs enables optimal choices for specific applications.

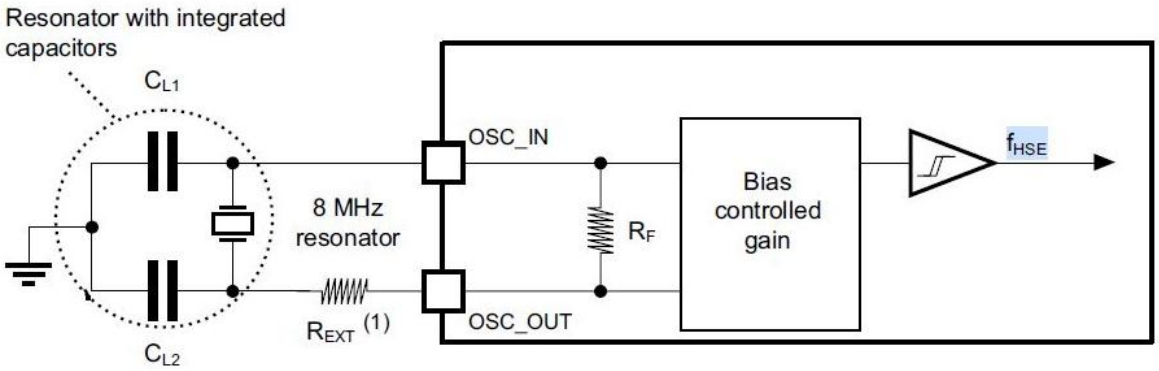
11.1 CRYSTAL SELECTION CRITERIA

External crystals provide superior frequency accuracy and stability compared to internal RC oscillators. Critical applications requiring precise timing mandate crystal oscillators.

CRYSTAL SELECTION PARAMETERS:

PARAMETER	TYPICAL RANGE	IMPACT
Load Capacitance	12-20 pF	Frequency accuracy
ESR	50-200 Ω	Startup reliability
Drive Level	10-100 µW	Power consumption
Frequency Tolerance	±20 to ±100 ppm	Initial accuracy

Crystal oscillator circuits require load capacitors calculated based on PCB parasitic capacitance and desired frequency accuracy.



11.2 INTERNAL RC ACCURACY

Internal RC oscillators provide convenience and cost savings but with reduced accuracy. Temperature and voltage variations affect frequency stability.

INTERNAL RC CHARACTERISTICS:

- Frequency accuracy: ±1% to ±3% at room temperature
- Temperature coefficient: ±0.5% over operating range
- Voltage coefficient: ±0.2% over supply range
- Startup time: Microseconds (vs milliseconds for crystals)

SELECTION GUIDELINES:

- Use crystals for: **UART**, **USB**, precise timing
- Use internal RC for: General purpose apps, low-power, cost-sensitive designs
- Consider hybrid approaches: RC for startup, crystal for precision operations
- Validate timing requirements against oscillator specifications

Table 42. HSI oscillator characteristics(1)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
f_{HSI}	Frequency	-	-	8	-	MHz
TRIM	HSI user trimming step	-	-	-	1(2)	%
$DuCy_{(HSI)}$	Duty cycle	-	45(2)	-	55(2)	%
ACC_{HSI}	Accuracy of the HSI oscillator (factory calibrated)	T_A = –40 to 105 °C	–3.8(3)	-	4.6(3)	%
		T_A = –10 to 85 °C	–2.9(3)	-	2.9(3)	%
		T_A = 0 to 70 °C	–2.3(3)	-	–2.2(3)	%
		T_A = 25 °C	–1	-	1	%
$t_{su(HSI)}$	HSI oscillator startup time	-	1(3)	-	2(3)	µs
$I_{DD(HSI)}$	HSI oscillator power consumption	-	-	80	100(3)	µA

12.GPIO TERMINATION

Series resistors on high-speed digital outputs reduce signal reflections, electromagnetic emissions, and improve signal integrity. Proper termination prevents data corruption and EMC failures.

12.1 IMPEDANCE MATCHING

Impedance matching minimizes overshoots, undershoots, and false triggering.

TERMINATION METHODS:

- Source termination: Series resistor at driver output
- Load termination: Parallel resistor at receiver input
- AC termination: Capacitor-coupled resistor networks
- Active termination: Voltage-controlled impedance

12.2 SERIES RESISTORS

High-speed signal integrity requires controlled impedance traces and proper termination. Signal quality degrades without appropriate termination techniques.

CRITICAL PARAMETERS:

- Rise/fall times: Determine transmission line effects
- Trace length: Electrical length vs signal wavelength
- Characteristic impedance: PCB stackup and geometry dependent
- Load capacitance: Total parasitic and input capacitance

SUGGEST VALUES:

SIGNAL TYPE	SERIES RESISTANCE	RATIONALE
SPI clock/data	22-33Ω	Hi-speed, short traces
I^2C bus	33-47Ω	Moderate speed, bus loading
UART	10-22Ω	Lo-speed, noise immunity
GPIO outputs	22-100Ω	Application dependent

13.GPIO LIMITS

GPIO pins have limited current drive capability

13.1 SPEED CONSIDERATIONS

The GPIO speed setting controls how fast the pin output can transition between logic levels by adjusting its slew rate. Higher speed modes enable faster edge transitions but increase power consumption and electromagnetic noise.

STM32 GPIO RATES:

SPEED SETTING	TYPICAL MAX FREQUENCY
LOW	UP TO 2–10 MHZ
MEDIUM	UP TO 25–50 MHZ
HIGH	UP TO 50–100 MHZ
VERY HIGH	UP TO 100–180 MHZ

13.2 CURRENT LIMITATIONS

TYPICAL GPIO LIMITS:

- Single pin: 8-25 mA maximum
- Total device: 100-200 mA maximum
- Voltage drop: 0.4V maximum at full load
- Temperature derating: Reduced capability at high temperatures

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all VDD power lines (source)(1)	120	mA
ΣI_{VSS}	Total current out of sum of all VSS ground lines (sink)(1)	-120	
$I_{VDD(PIN)}$	Maximum current into each VDD power pin (source)(1)	100	
$I_{VSS(PIN)}$	Maximum current out of each VSS ground pin (sink)(1)	-100	
$I_{IO(PIN)}$	Output current sunk by any I/O and control pin	25	
	Output current source by any I/O and control pin	-25	
$\Sigma I_{IO(PIN)}$	Total output current sunk by sum of all I/Os and control pins(2)	80	
	Total output current sourced by sum of all I/Os and control pins(2)	-80	
	Total output current sourced by sum of all I/Os supplied by VDDIO2	-40	
$I_{INJ(PIN)}$(3)	Injected current on B, FT and FTf pins	-5/+0(4)	
	Injected current on TC and RST pin	± 5	
	Injected current on TTa pins(5)	± 5	
$\Sigma I_{INJ(PIN)}$	Total injected current (sum of all I/O and control pins)(6)	± 25	

14.PIN VOLTAGE

Mixed-voltage systems require careful interface design to prevent damage and ensure reliable operation. Understanding voltage compatibility prevents costly design errors.

14.1 FIVE VOLT TOLERANCE

Not all MCU pins support 5V input levels. Datasheet verification prevents permanent damage from overvoltage conditions.

5V TOLERANCE CATEGORIES:

- 5V tolerant: Can accept 5V inputs safely
- 3.3V maximum: Require level shifting for 5V interfaces
- Analog inputs: Often limited to VDD + 0.3V maximum
- Power pins: Specific voltage requirements

STM32F devices vary in 5V tolerance by pin function. GPIO pins are typically 5V tolerant, while analog and specialized pins may have lower limits.

Name	Abbreviation	Definition
Pin Type	S	Supply pin
	I	Input only pin
	I/O	Input / output pin
I/O structure	FT(1)	Five-volt tolerant I/O pin
	TT(1)	Three-volt tolerant I/O pin
	TC	Three-volt capable I/O pin (Standard 3.3 V I/O)
	B	Dedicated boot pin
	RST	Bidirectional reset pin with embedded weak pull-up resistor

14.2 LEVEL SHIFTING REQUIREMENTS

Level shifters enable communication between different voltage domains. Selection depends on signal direction, speed, and power requirements.

LEVEL SHIFTER TYPES:

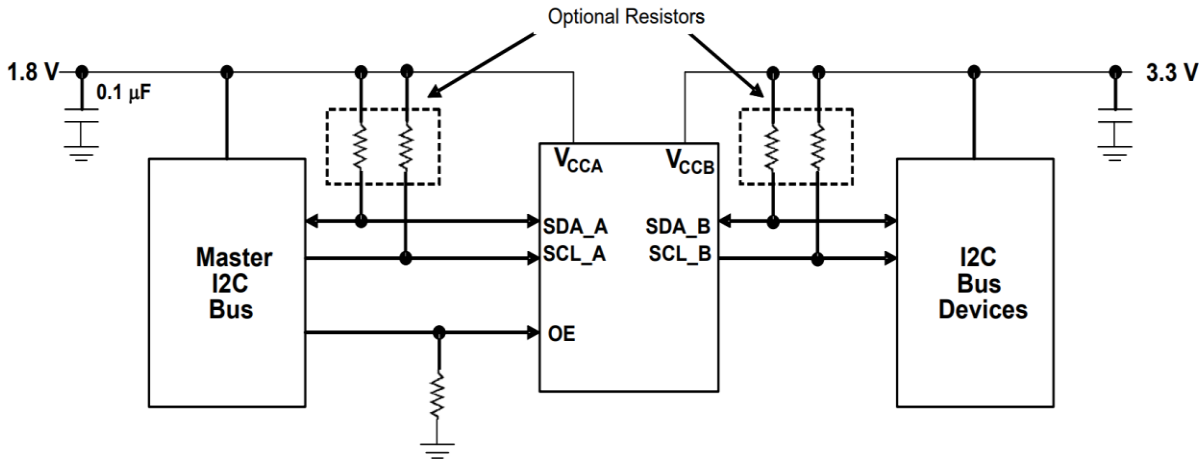
TYPE	DIRECTION	SPEED	POWER
Resistor divider	Unidirectional	Low	Very low
MOSFET	Bidirectional	Medium	Low
Dedicated IC	Bidirectional	High	Medium
OPAMP	Unidirectional	Very high	High

DESIGN CONSIDERATIONS:

- Calculate voltage division ratios for resistive level shifters
- Consider input/output impedances in level shifter design
- Verify level shifter propagation delays meet timing requirements
- Include pull-up resistors on open-drain level shifter outputs

IMPLEMENTATION GUIDELINES:

- Use dedicated level shifter ICs for high-speed buses (SPI, I^2C)
- Consider power consumption in battery-powered applications
- Validate level shifter performance across temperature range
- Document voltage domain boundaries clearly in schematics



15.PROGRAMMING

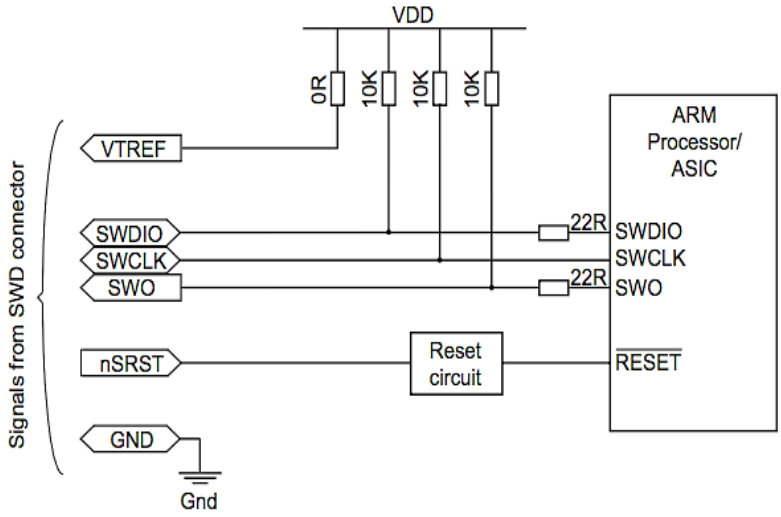
Accessible programming interfaces enable firmware updates and debugging throughout the product lifecycle. Poor interface design complicates manufacturing and field support.

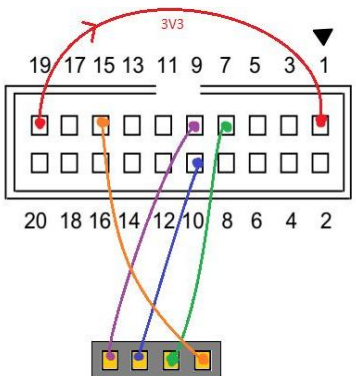
15.1 SWD HEADER DESIGN

Serial Wire Debug (SWD) provides efficient programming and debugging access with minimal pin count. The interface requires careful signal integrity considerations.

REQUIRED SWD SIGNALS:

- SWDIO (bidirectional data)
- SWCLK (clock)
- NRST (reset, optional but recommended)
- VDD (target voltage reference)
- GND (ground reference)





ST-LINK/V2
20-pin connector:

1 - MCU VDD - target voltage measurement
7 - SWDIO
9 - SWCLK
10 - GND
15 - NRST
19 - VDD (3.3V) source - output from ST-LINK

16.EXTERNAL MEMORY

External memory interfaces require careful signal integrity design and proper decoupling.

High-speed parallel and serial memory interfaces demand controlled impedance routing.

16.1 INTERFACE DECOUPLING

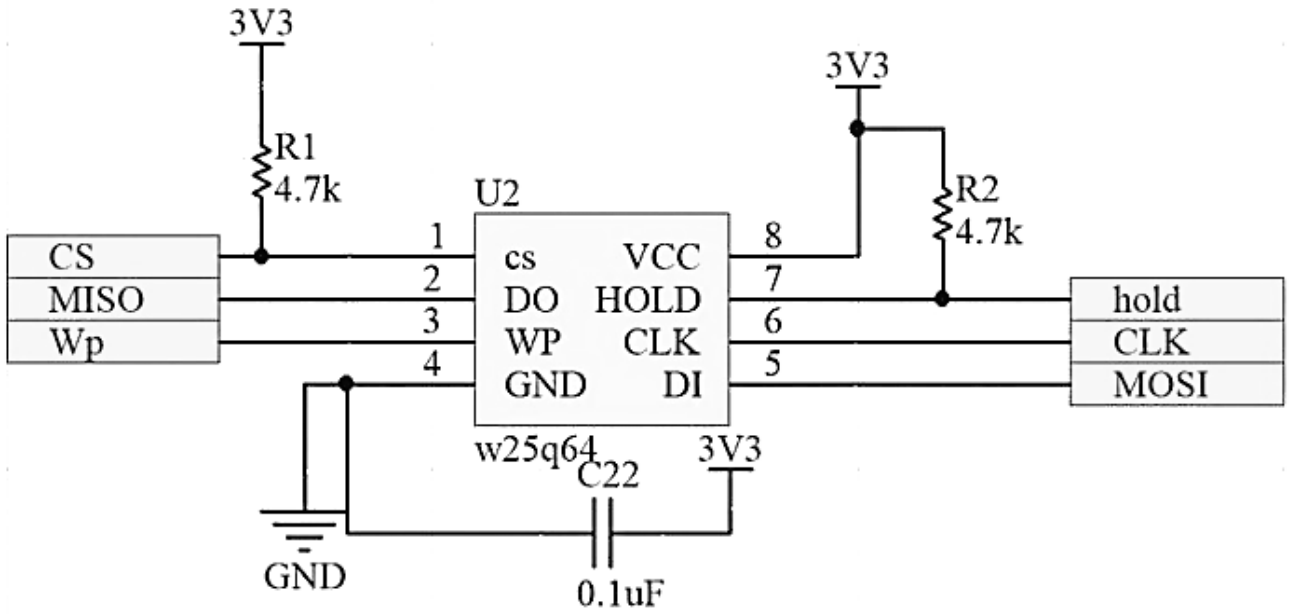
Memory interface power supply quality directly impacts data integrity. Switching currents create power supply noise requiring extensive decoupling.

Memory device placement affects decoupling effectiveness.

Close proximity to MCU reduces trace lengths and parasitic inductance.

FLASH MEMORIES:

MANUFACTURER	P/N	SIZE
Winbond	W25Q64JV	64 Mbit
GigaDevice	GD25Q128C	128 Mbit
Macronix	MX25L25645G	256 Mbit
Microchip (Adesto)	AT25SF641	64 Mbit
Cypress/Infineon	S25FL064L	64 Mbit



17.TIMER PINS

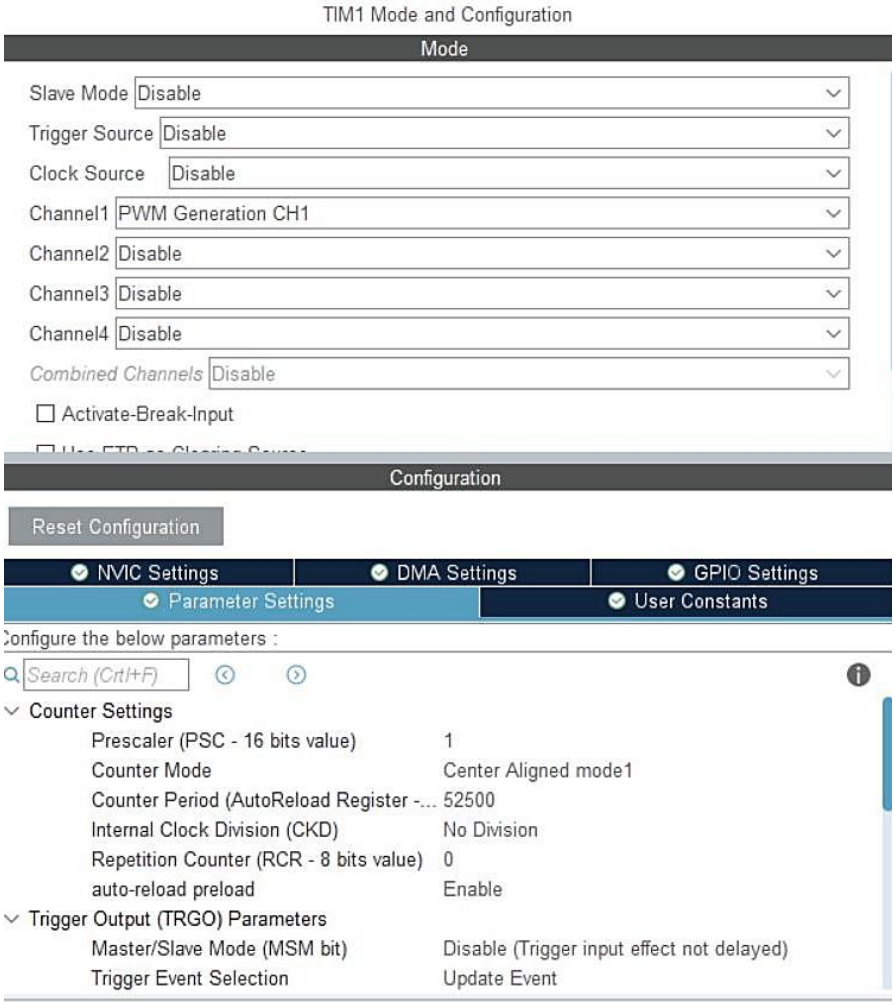
Timer peripheral pin selection affects PWM performance, resolution, and output drive capability. Understanding timer capabilities enables optimal pin assignment for timing-critical applications.

17.1 PWM OUTPUT SELECTION

PWM output pin selection influences signal quality, electromagnetic emissions, and load drive capability. Timer channel capabilities vary within the same peripheral.

PWM PIN CHARACTERISTICS:

- Output frequency range: Limited by timer clock and prescaler settings
- Resolution: Dependent on timer counter width and frequency
- Drive strength: Varies by pin location and configuration
- Complementary outputs: Available on advanced timer channels



17.2 TIMER CAPABILITIES

Different timer peripherals offer varying capabilities affecting pin selection.

Understanding limitations prevents performance issues in time-critical applications.

TIMER TYPES:

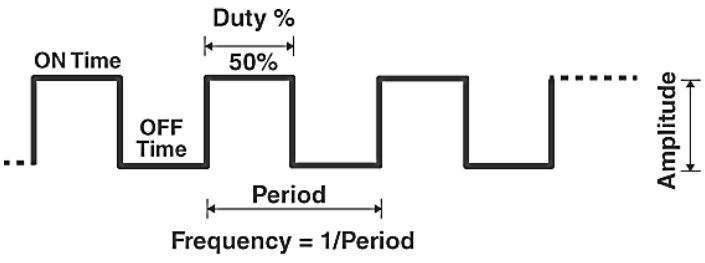
TYPE	TIMER NAMES	RESOLUTION	PWM SUPPORT
Advanced Control	TIM1, TIM8	16-bit	Yes
General Purpose	TIM2, TIM5	32-bit	Yes
General Purpose	TIM3, TIM4, TIM9-14	16-bit	Yes
Basic	TIM6, TIM7	16-bit	No

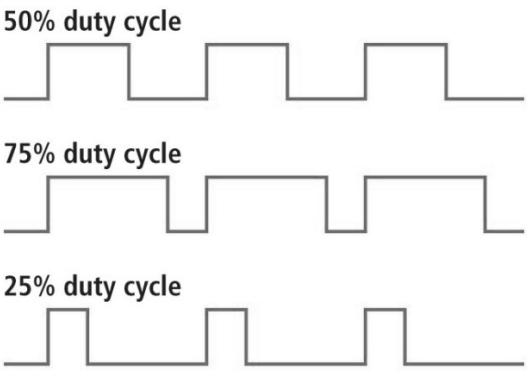
PIN SELECTION FACTORS:

- Required PWM frequency and resolution
- Load drive current requirements
- Electromagnetic compatibility considerations
- Complementary output requirements
- Timer synchronization needs

PWM DESIGN CONSIDERATIONS:

- Calculate resolution requirements based on application needs
- Consider timer clock source stability for precision applications
- Plan for dead time requirements in power switching circuits
- Use hardware PWM generation for consistent timing
- Include filtering for PWM-based analog outputs





18.ADC INPUT

Analog-to-Digital Converter (ADC) input design directly impacts measurement accuracy and resolution. Proper input conditioning, filtering, and reference design are essential for reliable analog measurements.

18.1 INPUT CONDITIONING

ADC input circuits must present signals within the converter's input range while maintaining signal integrity.

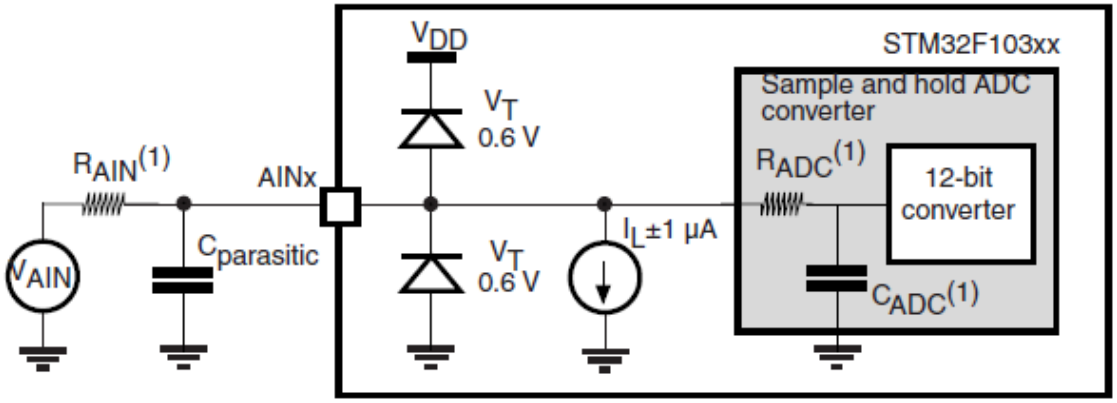
INPUT CONDITIONING ELEMENTS:

- Voltage dividers: Scale input signals to ADC range
- Operational amplifiers: Provide gain and buffering
- Anti-aliasing filters: Remove high-frequency noise

SOURCE IMPEDANCE REQUIREMENTS:

RESOLUTION	MAX IMPEDANCE	SETTLING TIME
8-bit	10 kΩ	Minimal
10-bit	2.5 kΩ	Moderate
12-bit	1 kΩ	Significant
16-bit	250 Ω	Critical

Higher resolution ADCs require lower source impedance for accurate measurements. Op-amp buffers provide impedance transformation when necessary.



18.2 ADC VREF

ADC reference voltage determines measurement range and accuracy.

REFERENCE TYPES:

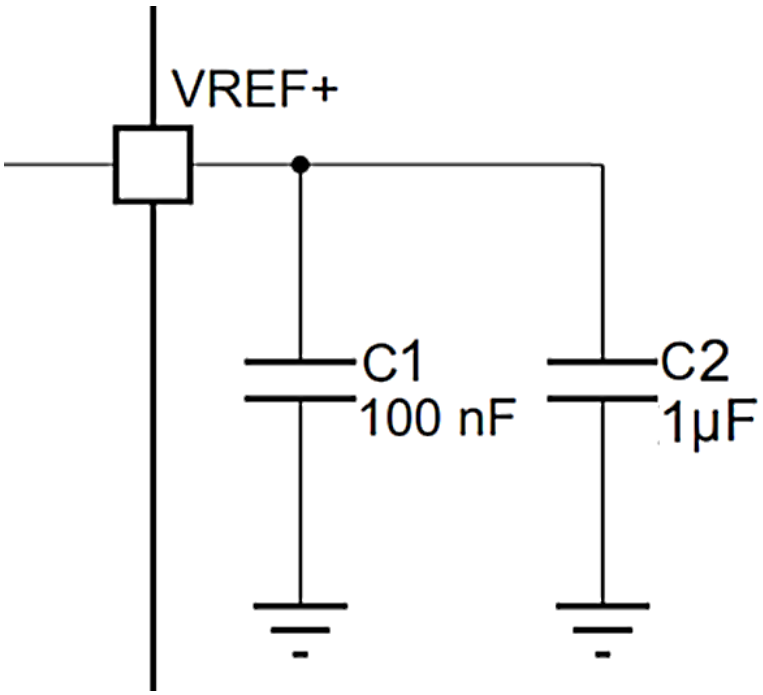
- Internal reference: Convenient, moderate accuracy
- External voltage reference: High accuracy, stable
- Supply-referenced: Simple, accuracy limited by supply regulation

REFERENCE SPECIFICATIONS:

External reference circuits require careful decoupling and thermal design. Reference IC placement affects noise coupling and temperature gradients.

DESIGN GUIDELINES:

- Use differential inputs when available for noise immunity
- Include anti-aliasing filters for sampled data systems
- Consider ADC input capacitance in source impedance calculations
- Use kelvin connections for precision voltage references
- Validate ADC performance across temperature and supply voltage ranges



19.INPUT PROTECTION

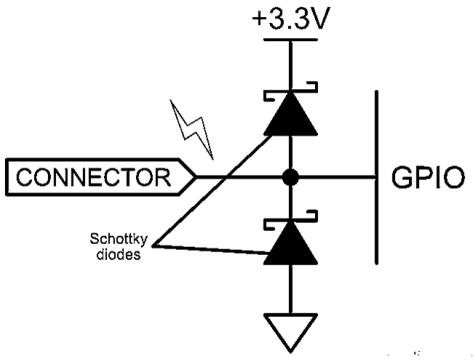
Input protection circuits safeguard MCU pins against overvoltage conditions and electrostatic discharge (ESD) events. Inadequate protection causes permanent damage and field failures.

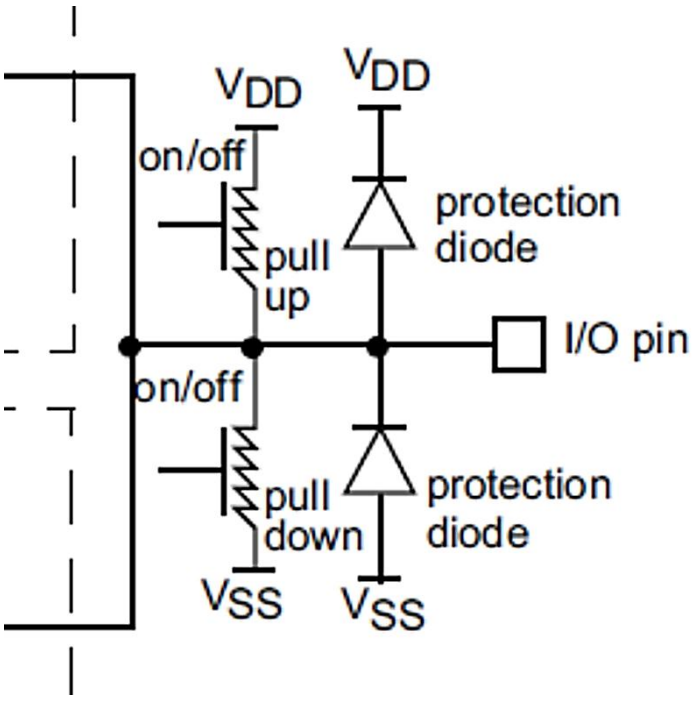
19.1 ESD PROTECTION METHODS

ESD protection requires coordinated approach combining board layout, component selection, and circuit design. Multiple protection stages provide robust defense against various threat levels.

PRIMARY PROTECTION COMPONENTS:

- Diodes: Fast response, low clamping voltage
- Series resistors: Current limiting, arc suppression
- Ferrite beads: High-frequency filtering
- Ceramic capacitors: Transient energy absorption





19.2 TVS DIODE PLACEMENT

TVS (Transient Voltage Suppressor) diodes provide primary overvoltage protection. Selection criteria include clamping voltage, power rating, and response time.

TVS SELECTION CRITERIA:

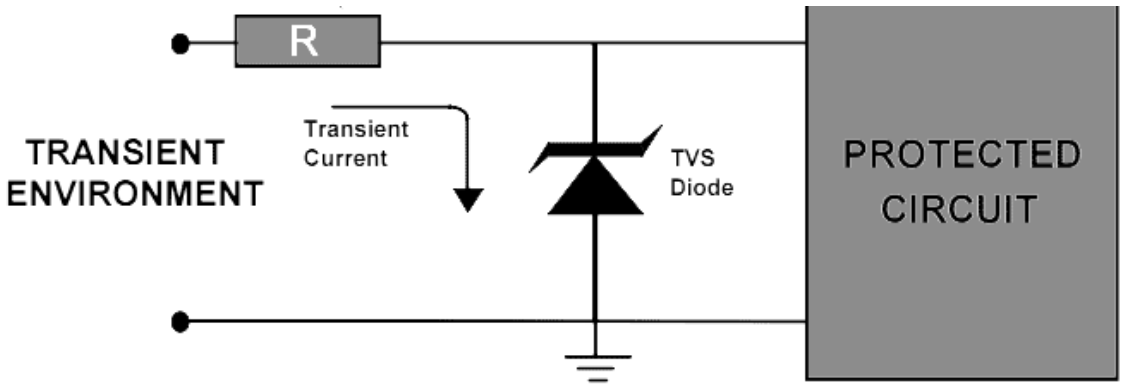
PARAMETER	REQUIREMENT	TYPICAL VALUE
Standby Voltage	>VDD max	>3.6V for 3.3V systems
Clamping Voltage	<VDD abs max	<4.0V for 3.3V systems
Peak Power	>Expected transient	400W minimum
Capacitance	<Pin max loading	<50 pF

IMPLEMENTATION GUIDELINES:

- Place TVS diodes close to protected pins
- Use series resistors (22Ω to 100Ω) before TVS diodes
- Provide low-inductance ground connections
- Consider bidirectional TVS for AC-coupled signals
- Include filtering capacitors after protection components

PROTECTION CIRCUIT DESIGN:

- Calculate maximum fault current through protection elements
- Verify protection device power ratings exceed worst-case conditions
- Consider multiple protection stages for harsh environments
- Test protection effectiveness with ESD simulation



20.DFT APPROACH

Accessible test points and Design for Test (DFT) features enable efficient manufacturing, debugging, and field service. Poor test access complicates production and increases support costs.

20.1 DFT IMPLEMENTATION

Design for Test features must be integrated from initial design phases. Post-layout test point addition is inefficient and often inadequate.

ESSENTIAL TEST POINTS:

- Power supply rails (VDD, AVDD, VBB)
- Reference voltages and bias levels
- Communication bus signals (SPI, I^2C, UART)
- Clock signals and timing references

20.2 ZERO OHM RESISTOR

0Ω APPLICATIONS:

- Power supply disconnect for external supply connection
- Signal path isolation for test signal injection
- Ground plane segmentation for noise analysis
- Component bypass for design variations

20.3 DFT ADVICES

CONSIDER THE FOLLOWING:

- Connect all Rails to ADC for monitoring
- Use Resistors for NC Pins
- Use Current Sensing for MCU Supply
- Use 2 options for UART TX/RX routing to prevent Re-Spin
- Allow Disconneting the Main VCC for external Supply test
- Use Indications

APPENDICES

ACRONYM

- **ADC**: Analog-to-Digital Converter
- **AVDD**: Analog Power Supply Voltage
- **BOOT0**: MCU Boot Pin 0 (controls boot mode)
- **DFT**: Design for Test (testability design approach)
- **ESD**: Electrostatic Discharge (protection against static electricity)
- **GPIO**: General Purpose Input/Output (programmable MCU pins)
- **MCU**: MCU Unit
- **NRST** (or Reset Pin): MCU Reset Input
- **PWM**: Pulse Width Modulation
- **RTC**: Real-Time Clock
- **SWD**: Serial Wire Debug (debug/programming interface)
- **TVS**: Transient Voltage Suppressor (diode for voltage spike protection)
- **VDD**: Digital Power Supply Voltage
- **VDDA**: Analog Power Supply Voltage
- **VSSA**: Analog Ground Reference
- **VBAT**: Battery Voltage Supply for RTC backup

GLOSSARY

- **AVDD**: Analog power supply pin for MCU to power analog circuits
- **Boot0 Pin**: A specific MCU pin that determines the boot mode/source on startup.
- **Capacitor Decoupling**: Use of capacitors near MCU power pins to stabilize voltage
- **Ferrite Bead**: A passive component used on power lines to block high-frequency noise.
- **Ground Plane**: Dedicated PCB copper layer connected to system ground
- **Level Shifter**: Circuit or IC that converts signals between different voltage domains.
- **Pin Multiplexing (Remapping)**: MCU feature to assign functions to physical pin
- **Power Plane**: PCB copper layer dedicated to supply power distribution.
- **Reset IC**: Dedicated integrated circuit that monitors voltage
- **Signal Integrity**: The quality and accuracy of electrical signals
- **SWD (Serial Wire Debug)**: Debug interface for programming and debugging ARM MCUs.