SPI

A basic overview

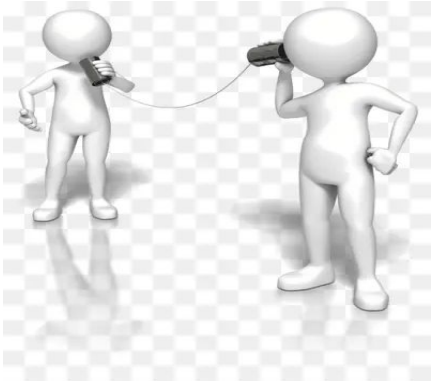
By
Nidhish & Bala Subramanian
Camera Services Firmware Team

Agenda

- What is Communication
- Types of Communication
- Transmission modes
- Communication protocols
- Serial Peripheral Interface (SPI)
- SPI Lines & Parameters
- SPI Modes
- Loop back Testing
- Test Procedure & Tools
- Pros & Cons
- Questions
- References

Communication

Process of exchanging information between two or more people or entities through a medium



Types of Communication

1. **Serial Communication**

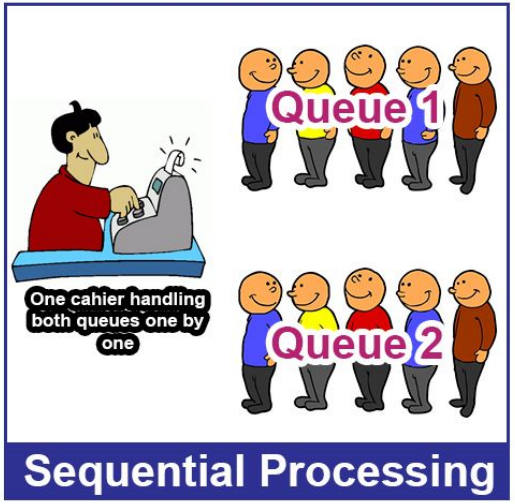
   Transmission of data *one bit at time*.

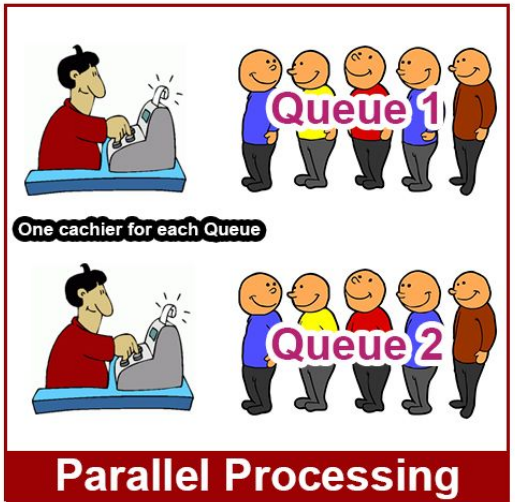
   In a ***Sequential*** manner. Suitable for Long distances.

2. **Parallel Communication**

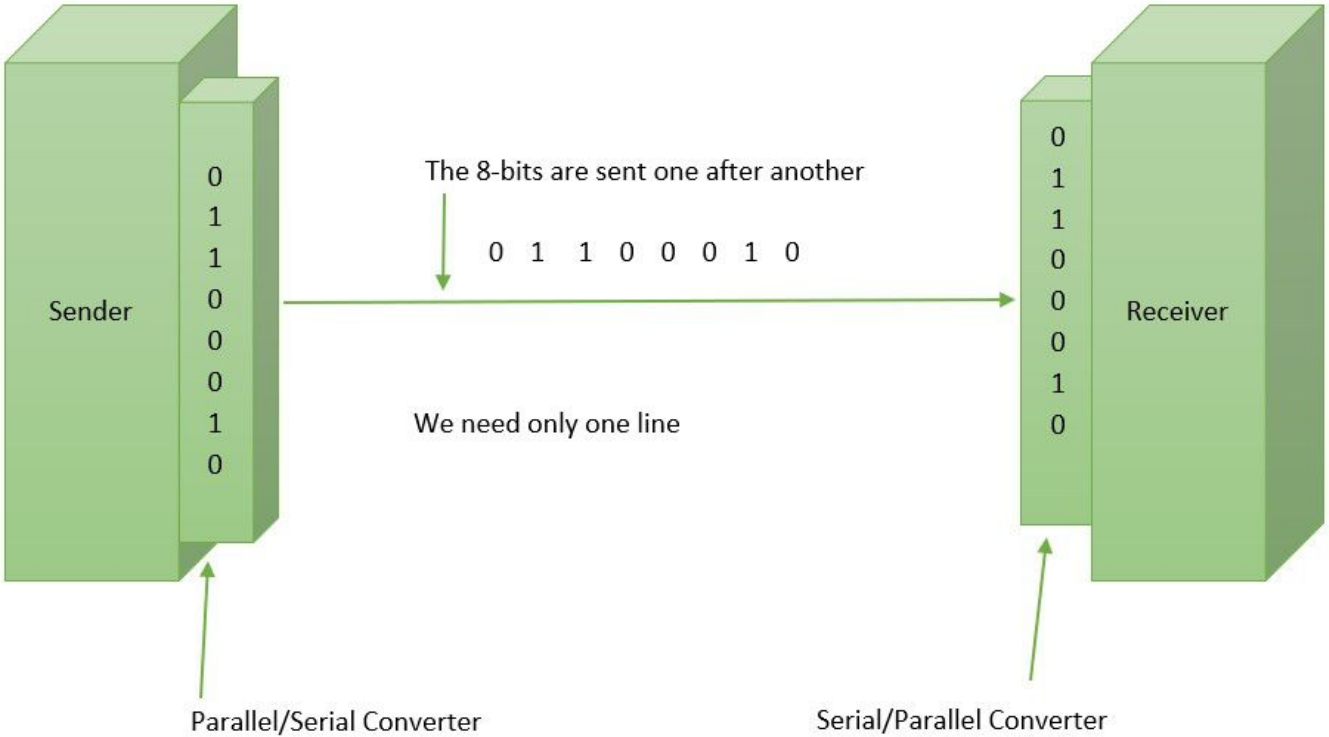
   Transmits *multiple bits* at a time ***simultaneously***.

   Short distance communication and more complex.

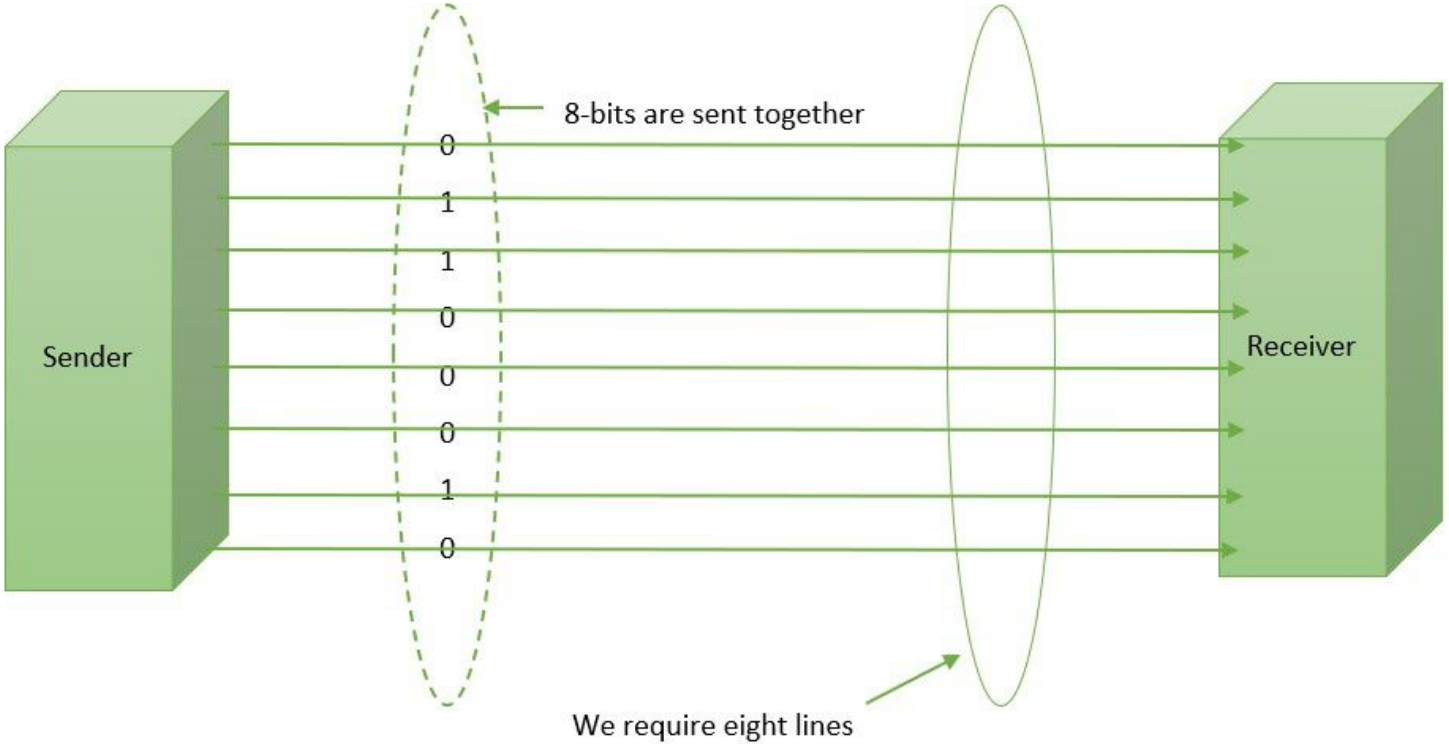




Serial Communication



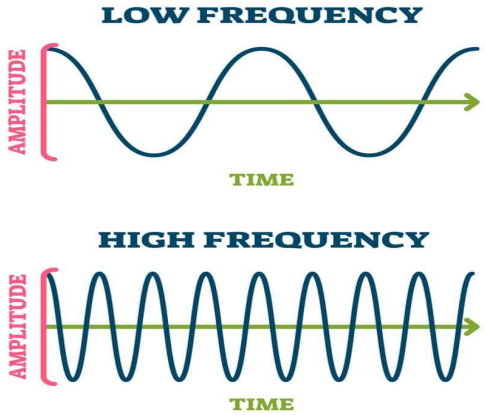
Parallel communication



Serial Vs Parallel Communication

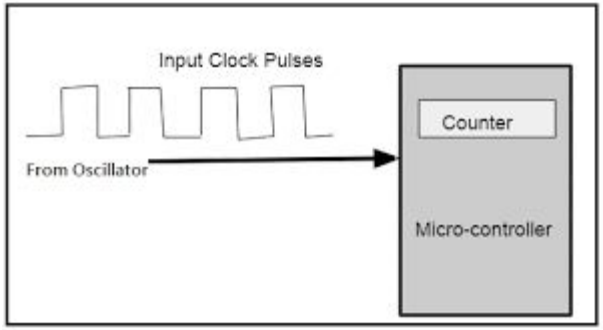
S.No	Serial Transmission	Parallel Transmission
1.	A **single communication link** is used to transfer data from one end to another	**Multiple parallels links** used to transmit the data
2.	Data(bit) flows in **bi-direction**.	Data flow is **unidirectional**.
3.	Cost-efficient.	Not cost-efficient.
4.	**One bit transferred at one clock pulse**.	**Eight bits transferred at one clock pulse**.
5.	Slow when compared to Parallel Transmission.	Faster than Serial Transmission.
6.	**Full duplex** as sender can send as well as receive the data	**Half-duplex** since the data is either send or received

Basic Terms: Clock, Data, Frequency



- **an electronic signal used to synchronize the operations**
- a **square wave signal** in which logic states H (high, logic 1) and L (low, logic 0) appear periodically

Frequency refers to the clock frequency, which is the signal that acts as the timebase for a microcontroller's CPU



Data

```
01010101
```

Synchronous

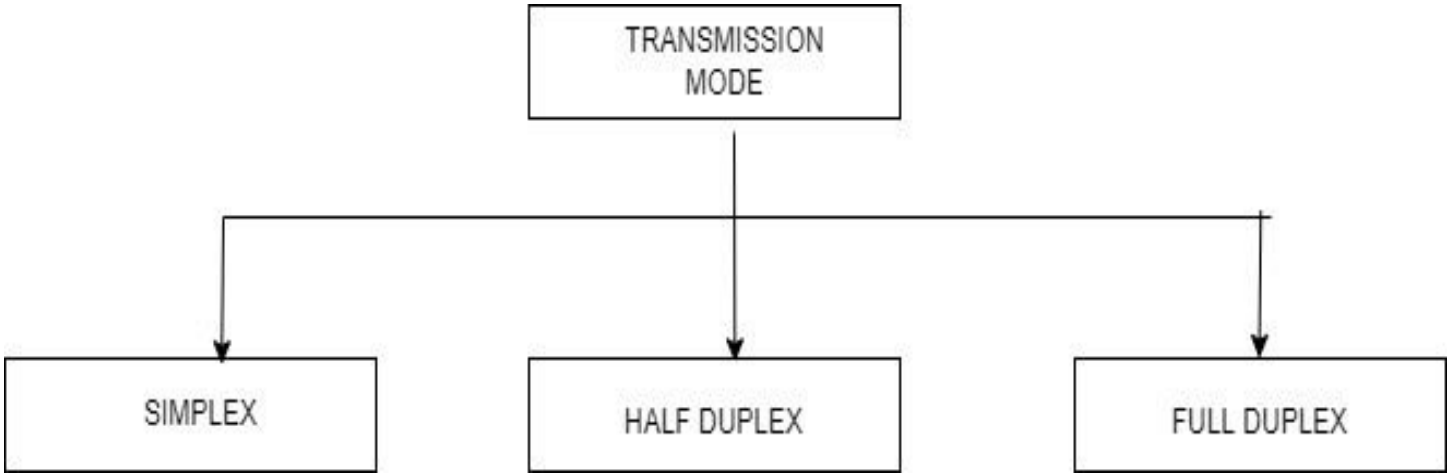
Same clock

Asynchronous

Independent clock

Transmission Modes

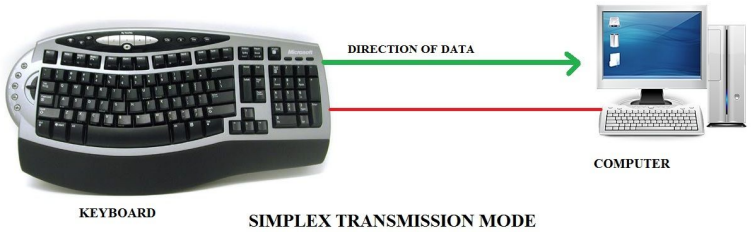
Transmission modes also known as **communication modes**, are methods of **transferring data** between devices on buses and networks designed to facilitate communication.



Simplex Mode

- data flows in only one direction. i.e., the flow of data is unidirectional
- Diagrammatically represented as,

A—>B .

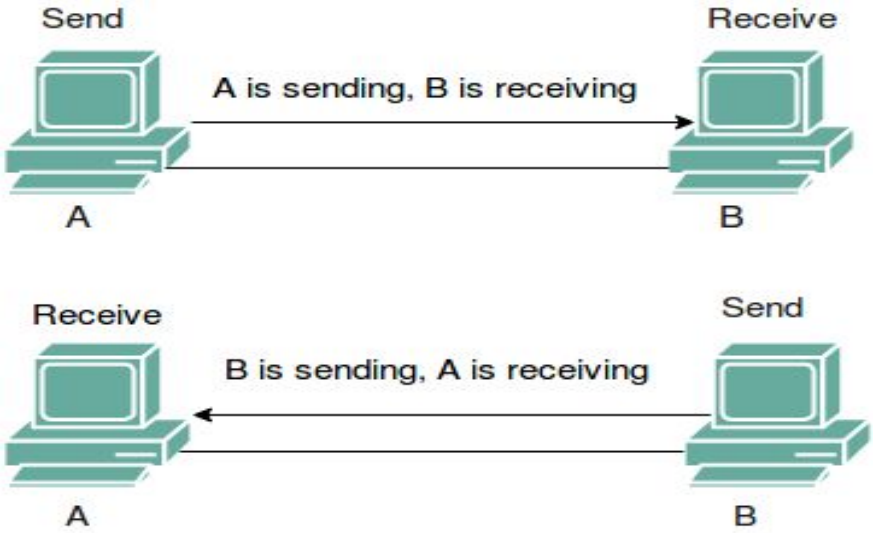


SIMPLEX TRANSMISSION MODE

Half Duplex

- data flows in both directions but **only in one direction at a time**.
- Diagrammatically represented as,

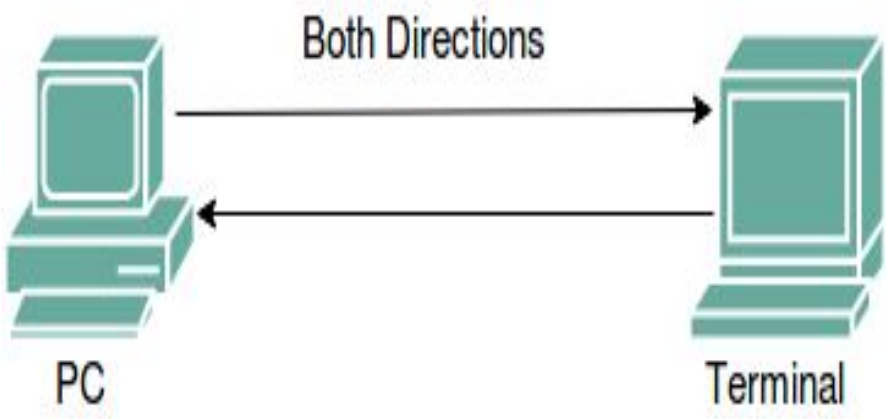
A—>B or B—>A



Full Duplex

- data flow in both directions **at the same time**.
- Diagrammatically represented as,

A—>B and B—>A



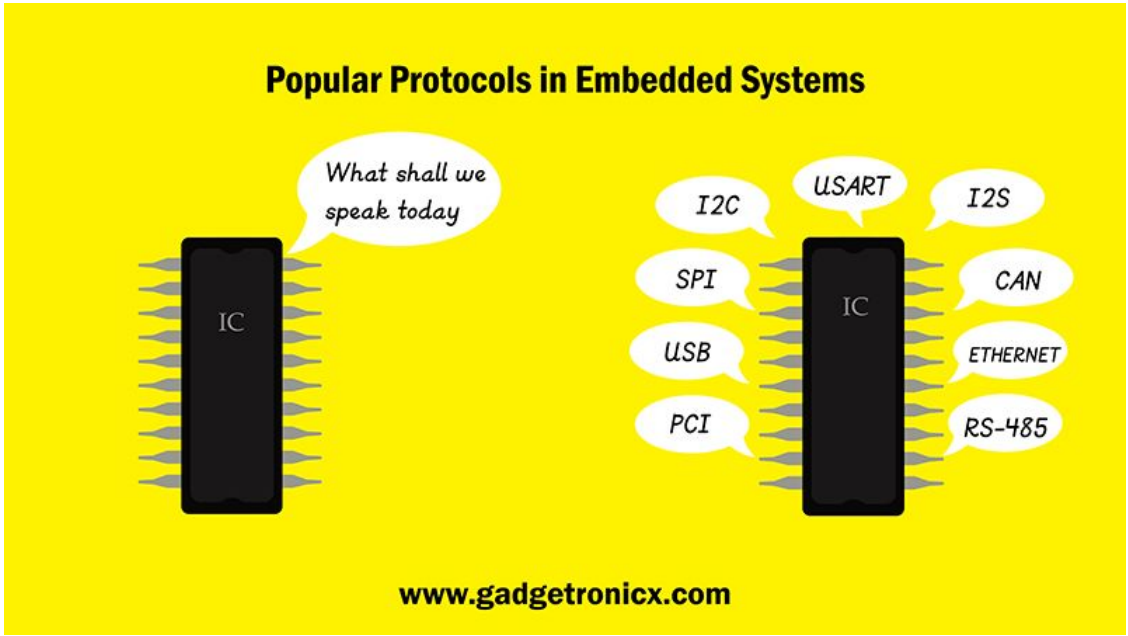
Communication Protocols

- ***System of rules*** and digital message ***formats*** enabling the transmission of information between devices.

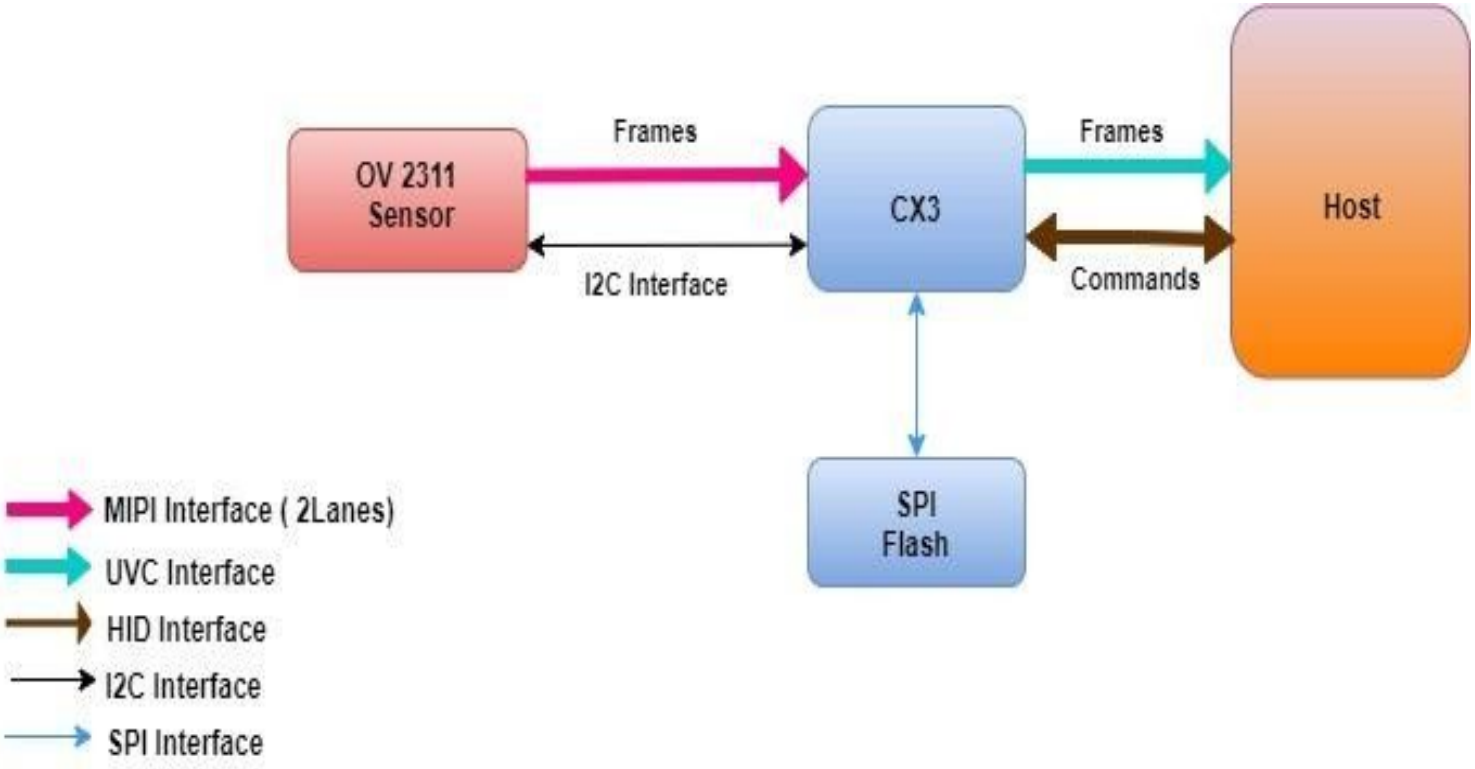
- follows a ***Master-Slave protocol*** exchange, where Masters (Eg.Microprocessors) command data transmission to and from Slaves (Eg. Sensors).

*A **protocol** allows various network-connected devices to communicate together irrespective of their design, structure, and internal processes.*

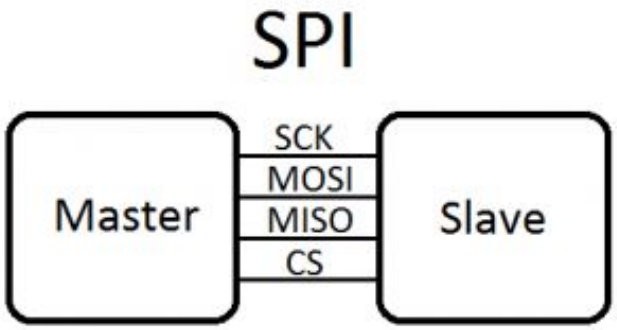

TRANSMISSION MEDIA
PROTOCOL
DEVICE 1
PROTOCOL
DEVICE 2


Popular Protocols in Embedded Systems
What shall we speak today
IC
I2C
USART
I2S
SPI
IC
CAN
USB
ETHERNET
PCI
RS-485
www.gadgetronicx.com

Sample Communication in Embedded Systems



SPI

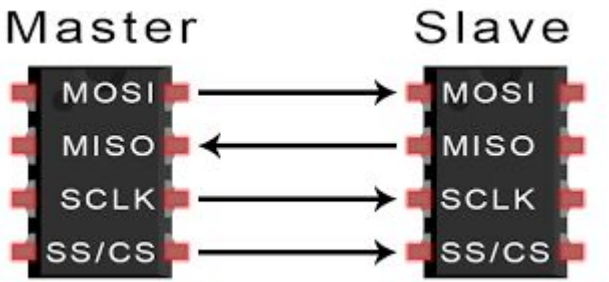


- Serial Peripheral Interface
- **4- wired**, short distance communication
- Invented by **Motorola** in the mid of 1980's
- **Full duplex** - many bits can be sent or received at a time simultaneously
- Used to connect l**ow speed devices**
- Commonly used for communication with flash memory, sensors, real-time clock (RTC), analog-to-digital-converters, etc.

SPI Lines

- SCK or SCLK : Serial Clock, clock generated by master
- MOSI or SDO : Master Output Slave Input, data output from master
- MISO or SDI : Master Input Slave Output, data output from slave
- SS or CS : Chip Select, Slave Select often an active low input of a slave

Data sheet snips



SPI Lines

1. **CS - Chip Select**

   Typically active low. Used to select slaves and communicate with it.

   Pulled high to disconnect the slave device from the SPI bus.

2. **SCLK - Serial Clock**

   Clock indicates when data should be sampled, when to read voltage levels.

   1 bit is read per clock cycle (usually in MHz)

   Can be **Idle low** or **idle high**

   Data can be sampled on **rising** or **falling** edge

*Users should consult the product **data sheet** for the clock frequency specification of the SPI interface.*

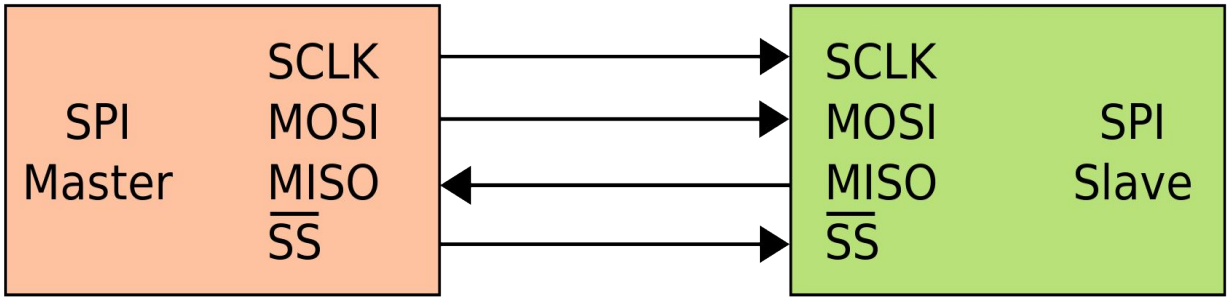
SPI Lines

3. **MOSI (SDO)**

   Transmits data from Master to Slave

4. **MISO (SDI)**

   Transmits data from Slave to Master



CLOCK POLARITY

- **CPOL bit** sets the polarity of the clock signal during the idle state
- The **idle state** is defined as the period when CS is high and transitioning to low at the start of the transmission and when CS is low and transitioning to high at the end of the transmission.

CLOCK PHASE

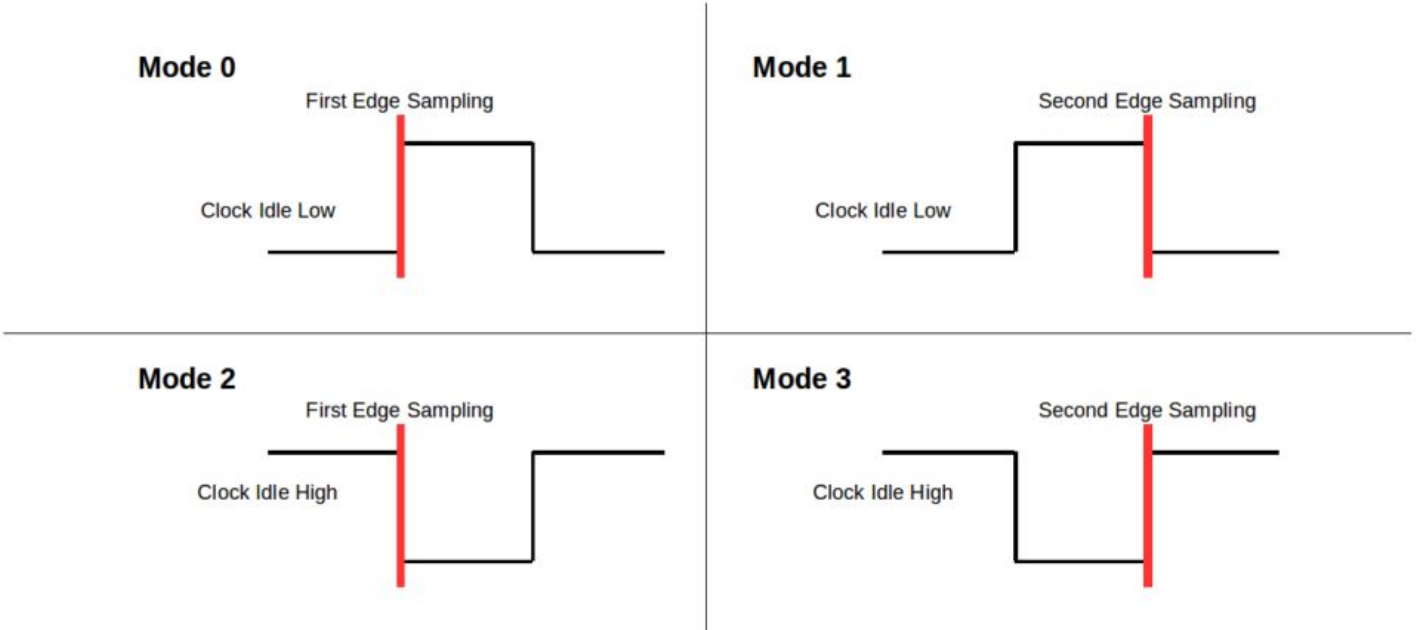
- **CPHA** bit selects the clock phase.
- the rising or falling clock edge is used to sample and/or shift the data.
- Master selects the Clock polarity and Clock phase as per the slave’s requirement.
- Used to decide from which edge sampling should be happened.

SPI MODES

Based on CPOL & CPHA SPI is classified into **4 operating modes**

SPI Modes

Mode	CPOL	CPHA
0	0	0
1	0	1
2	1	0
3	1	1



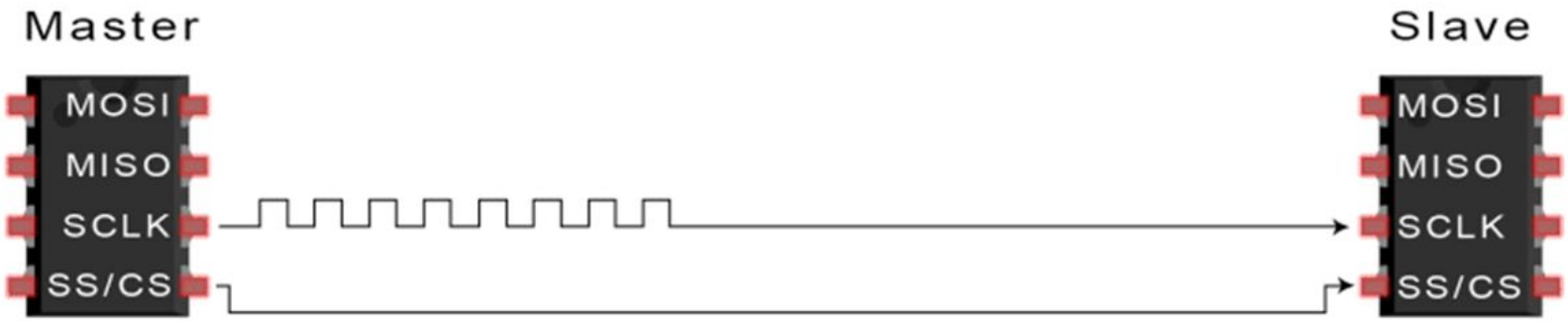
Operating modes

SPI Mode	CPOL	CPHA	Clock Polarity in IDLE state	Clock Phase used to sample and/or shift data
0	0	0	Logic low	Data sampled on rising edge and shifted out on the falling edge
1	0	1	Logic low	Data sampled on the falling edgeand shifted out on the rising edge
2	1	0	Logic high	Data sampled on the falling edge and shifted out on the rising edge
3	1	1	Logic high	Data sampled on the rising edge and shifted out on the falling edge

Data Transmission

STEP 1 :

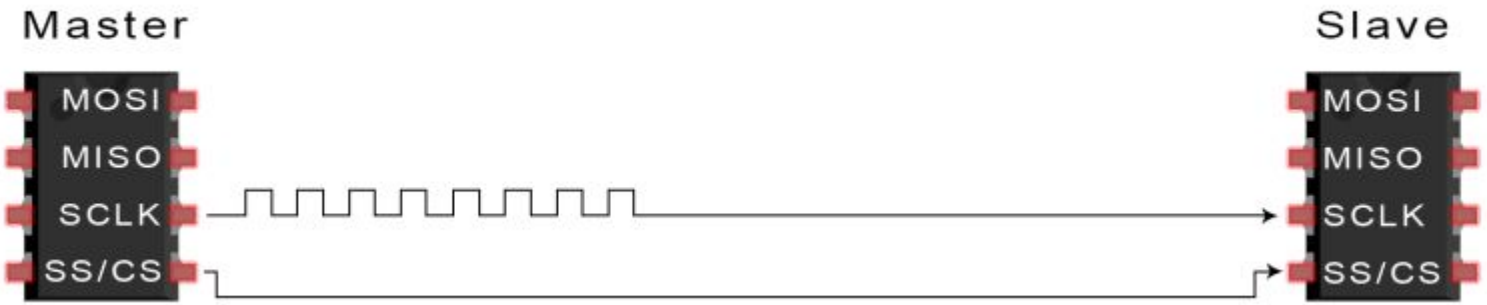
The master switches the SS/CS pin to a **low** voltage state, which activates the slave



Data Transmission

STEP 2 :

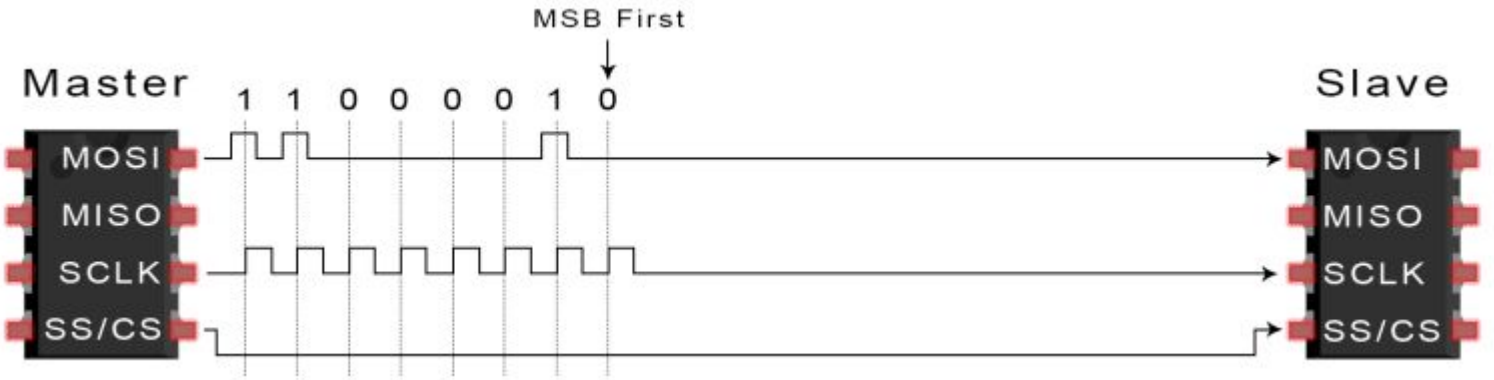
The master outputs the clock signal.



Data Transmission

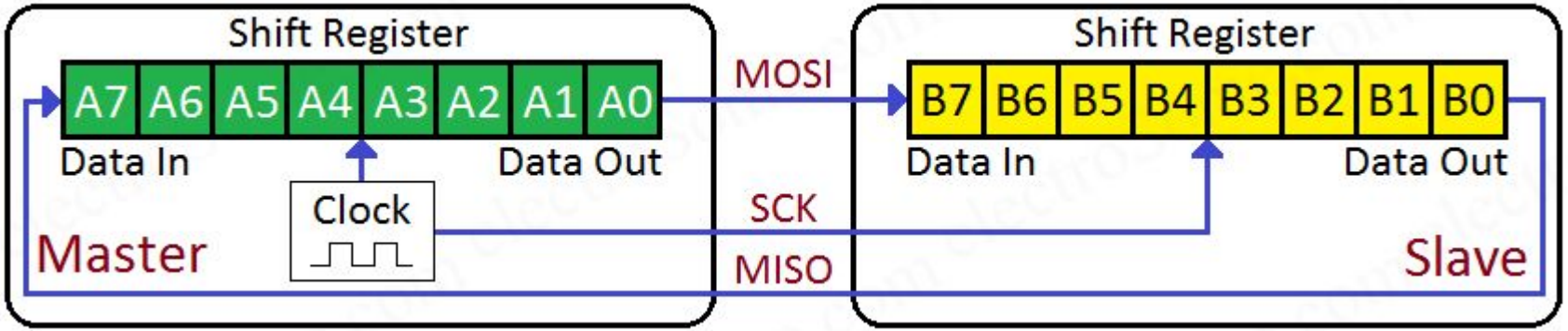
STEP 3 :

- The master sends the data one bit at a time to the slave along the MOSI line.
- The slave reads the bits in the order they receive it.



Working logic of SPI

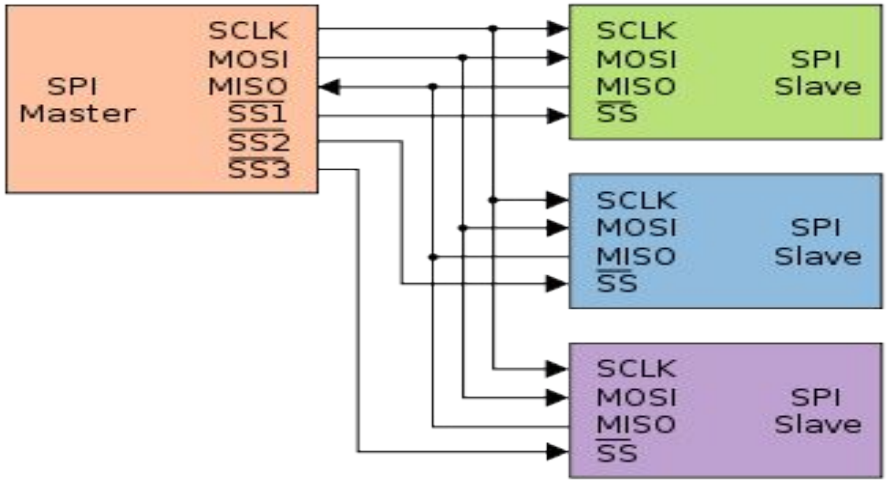
- Operation is based on shift registers (usually 8 bit). Each devices (master and slave) uses shift registers to shift data in and out of the system.



- **Master will generate clock whenever it wants to write data to a Slave device.** After 8 clock pulses data in the master device (A7 ~ A0) is transferred to slave device and data in the slave device (B7 ~ B0) is transferred to the master device.

Question

If you want to communicate with extra slaves as well what to do?



1 Master - Multiple Slaves

Pros & Cons

Pros

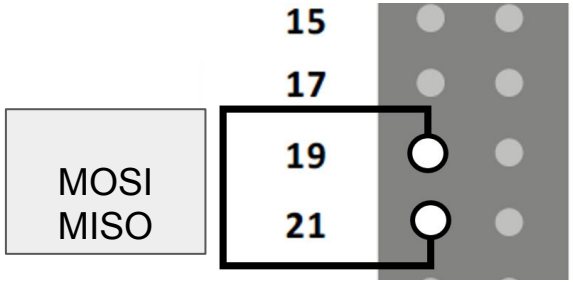
- ➔ Higher throughput than I²C
- ➔ Full duplex communication
- ➔ No start and stop bits, so the data can be streamed continuously without interruption

Cons

- ➔ Only allows for a single master
- ➔ No form of error checking like the parity bit in UART
- ➔ Uses four wires (I2C and UARTs use two)

Loopback Test in SPI

- ➔ Connect MOSI and MISO Lines: The MOSI and MISO lines are connected back-to-back, either through hardware or jumper wires.
- ➔ Verify Communication: Data sent on MOSI is received back on MISO, confirming the integrity of the SPI communication by comparing transmitted and received data.
- ➔ Slave Loopback: In some cases, the data clocked out by MOSI is received by a slave chip. which then sends it back to the master via the MISO line.



Test Procedure and Tools

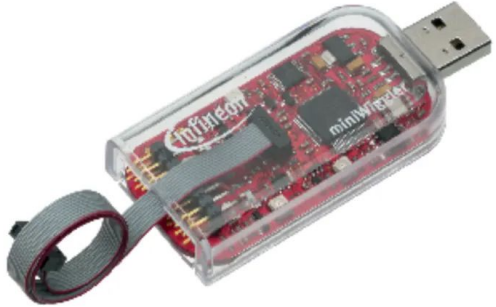
From Master Side:

For testing whether the clock frequency mode are properly configured and data is properly configured by

- Debug via JTAG
- Probe using a Oscilloscope
- Logic Analyzers.

Debug via JTAG:

- JTAG is a hardware interface used to flash, debug, and test firmware on embedded systems via a serial connection, often through USB or similar interfaces.



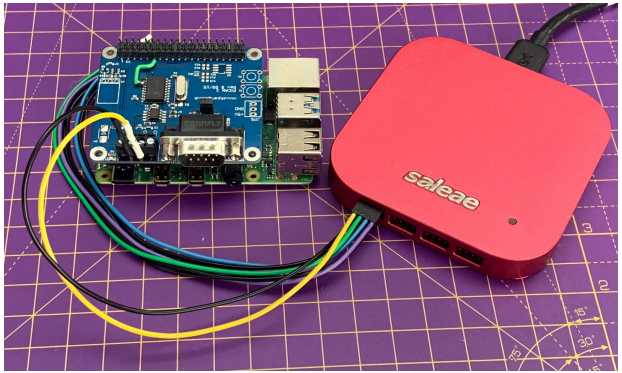
Probe Using Oscilloscope:

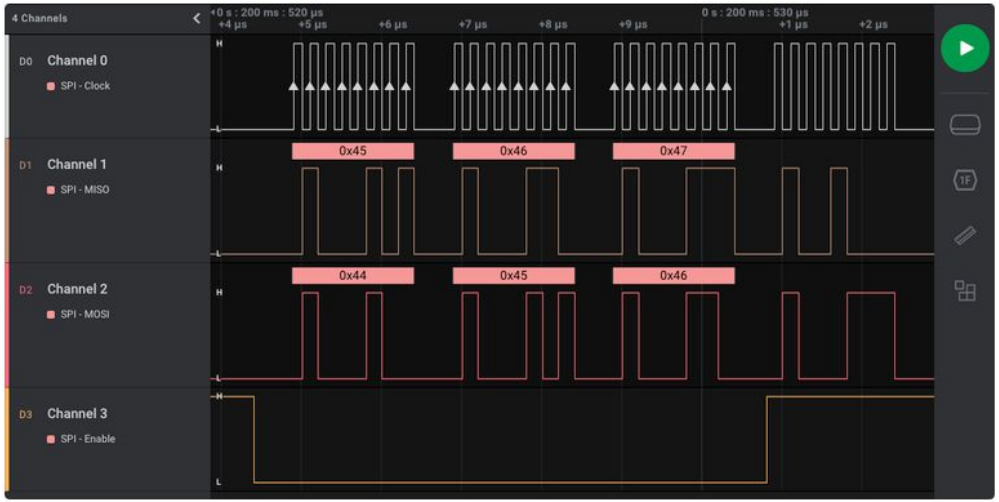
- An oscilloscope is an electronic test instrument that visually displays varying signal voltages over time, allowing users to analyze waveform characteristics like amplitude, frequency, and timing.

- It is commonly used for troubleshooting, measuring, and debugging electronic circuits and signals.

Logic Analyzer:

- A logic analyzer is an electronic test tool used to capture and analyze digital signals, allowing users to view and measure timing relationships between multiple digital signals in real-time.





From Slave Side:

For testing whether able to write and read a slave the following tools and procedures are employed

- spi-tools
- FT232H

spi-tools:

- spi-tools is a command line tool used to configure and transfer data via SPI bus in Linux.
- The following commands are used to install spi-tools and to configure spi bus and to send and receive data.

```
sudo apt-get install spi-tools
```

To install spi-tools

REFERENCES

1. Serial Communication

   https://en.wikipedia.org/wiki/Serial_communication

2. https://www.naukri.com/code360/library/transmission-modes

3. ttps://www.weare5vmedia.com/media/communication-protocols-for-an-embedded-engineer-to-know
4. https://uk.farnell.com/communication-network-protocols-trc-ar
5. Introduction to SPI Interface | Analog Devices - Whole SPI concepts
6. SPI - Serial Peripheral Interface Protocol Basics
7. https://www.google.com/url?sa=t&source=web&rct=j&opi=89978449&url=https://support.saleae.com/protocol-analyzers/analyzer-user-guides/using-spi&ved=2ahUKEwjRyomG_9qJAxVVTGwGHSy0EL8QFnoECBYQAQ&usg=AOvVaw0a8reBiEmDjDbB59P3v-Bq
8. https://github.com/cpb-/spi-tools
9. https://learn.adafruit.com/circuitpython-on-any-computer-with-ft232h/overiew
10. https://github.com/GiovanniGhezzi/SPI_with_Adafruit_FT232H
11. https://learn.adafruit.com/circuitpython-basics-i2c-and-spi/spi-devices

Questions and Doubts?

Thank You!!!!