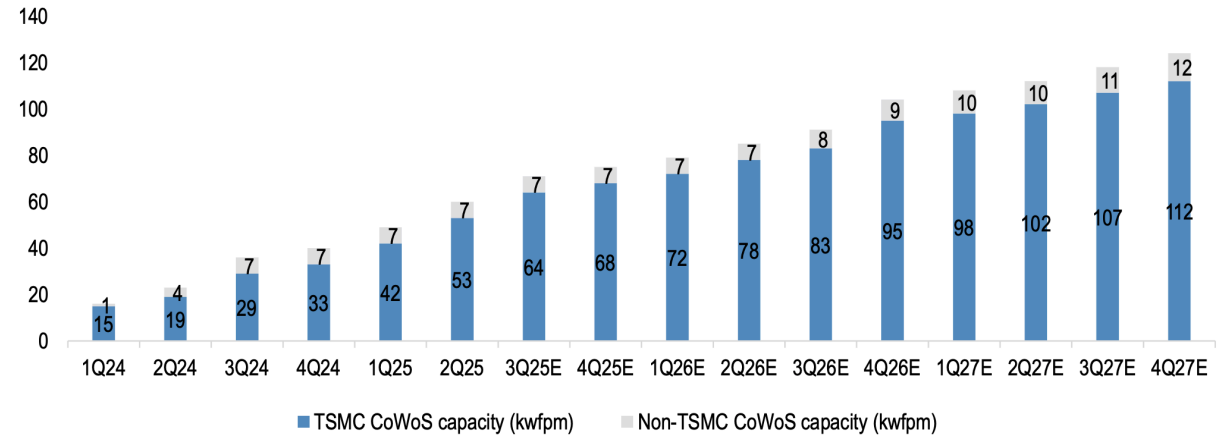
TSMC’s CoWoS & Advanced Backend – Implications for the AI Era

Executive Summary



Source: J.P. Morgan estimates, company data.

The semiconductor industry is entering a new phase where **advanced packaging and testing capacity—not wafer starts alone—determine the pace of AI hardware deployment.** TSMC, with its CoWoS (Chips-on-Wafer-on-Substrate), SoIC (System-on-Integrated-Chips), and WMCM (Wafer-level Multichip Module) technologies, sits at the core of this bottleneck.

By 2026, TSMC’s CoWoS capacity will grow to ~95,000 wafers per month, reaching 112,000 wafers per month by 2027. This expansion—anchored by the new AP8 fab in Tainan’s Southern Taiwan Science Park—will serve surging demand from NVIDIA, Broadcom, AMD, AWS, and Microsoft. However, demand is so strong that **OSATs (ASE, Amkor, SPIL)** will absorb more packaging and test workloads, making the ecosystem increasingly interdependent.

Context: Why Packaging is the Bottleneck

Traditionally, semiconductor scaling focused on lithography and transistor density. In the AI era, chips are assembled as **multi-die systems**, combining GPUs, CPUs, and stacks of HBM (High Bandwidth Memory) into a single module.

- These modules rely on **advanced interposers** (silicon or redistribution layers) to connect dies.
- **Packaging yields** and **test cycles** (burn-in, SLT, chip-probe) directly impact accelerator output.
- Even if wafer fabs are ready, packaging/test constraints can delay shipments —making them the new bottleneck.

TSMC’s Advanced Backend Expansion

CoWoS Capacity & Strategy

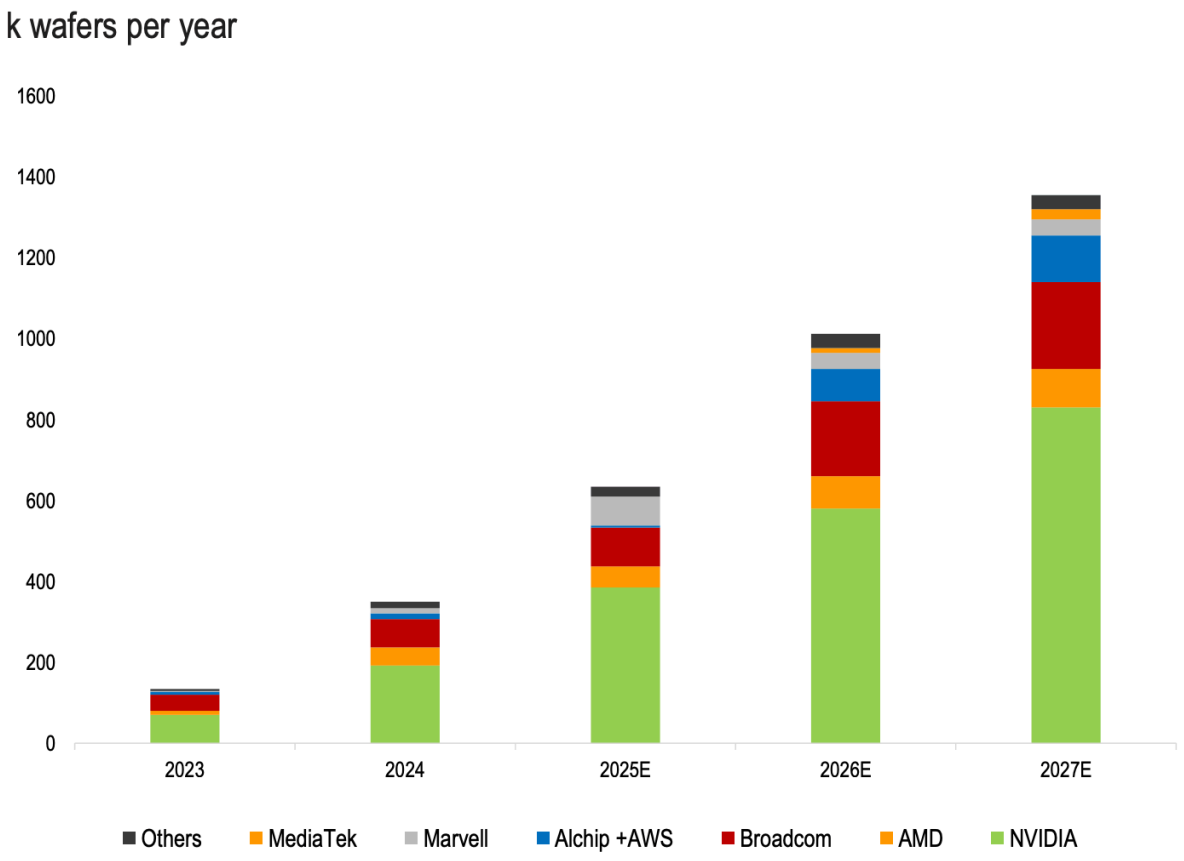
- **95k wafers/month (2026E)** → **112k wafers/month (2027E)**.
- AP8 in **Tainan STSP** is the flagship packaging expansion, converted from Innolux’s former LCD Fab 4.
- TSMC prioritizes CoWoS-L (Local Silicon Interconnect), outsourcing less critical or non-AI full-stack assembly to ASE.

SoIC & WMCM

- **SoIC** (3D hybrid bonding): Ramp begins at AP7 (Zhunan) in 2026 with Apple MacBooks; expected for AI ASICs from 2027–28.
- **WMCM**: Adopted by Apple’s 2026 iPhone A20 Pro line (205k wafers in 2026, 369k in 2027), showing how advanced backend is moving into consumer markets.

CoPoS (Next Generation)

- **Panel-based packaging** using 310mm × 310mm glass substrates.
- Engineering lines are being built at ASE/TSMC, with deployment expected beyond 2027 (earliest with NVIDIA’s “Feynman” GPU).



Source: J.P. Morgan estimates, Company data.

Customer Dynamics

1. **NVIDIA**
   - 6.3M AI GPUs in 2026.
   - Rubin GPU introduces **larger 9-die CoWoS-L packages**, raising wafer consumption.
   - Remains TSMC's largest CoWoS client (~580k wafers in 2026, 830k in 2027).
2. **Broadcom (Google TPU + ASICs)**
   - Fastest growth: 185k wafers in 2026, +93% YoY.
   - Driven by Google TPU v6p/v7p ramps and Meta/OpenAI custom ASICs.

- Networking ASIC demand also growing.

3. **AMD**
   - Weak 2025, recovery in 2026 via MI400/450 GPUs and Venice CPUs with HBM.
   - Volumes reach ~80k wafers in 2026, 95k in 2027.
4. **AWS (Trainium & Inferentia)**
   - Trainium-3 ramps in 2026 (~80k wafers, 70–75% via Alchip).
   - CoWoS outsourcing to ASE/Amkor possible later.
5. **Microsoft/Marvell**
   - Microsoft's custom ASIC (MAIA) begins late 2026.
   - Major driver for Marvell's packaging demand into 2027.
6. **MediaTek**
   - TPU project delayed to ≥4Q25.
   - 2026 demand cut to 12k wafers, real ramp likely in 2027–28.

Market Outlook

- **Total CoWoS demand:**
  - 634k wafers (2025E) → 1,012k (2026E) → 1,355k (2027E).
- **Customer distribution (2026E):**
  - NVIDIA 580k, Broadcom 185k, AMD 80k, AWS/Alchip 80k, MediaTek 12k, Others 75k.
- **Testing demand:** Rising faster than packaging due to N3 migration, chiplet proliferation, and HBM4 adoption.

Geographic Footprint of Advanced Backend

- **Zhunan (Miaoli County):** AP1–AP7 cluster (CoWoS, SoIC, WMCM).

- **Tainan STSP:** AP8 mega CoWoS fab (ex-Innolux Fab 4).
- **Kaohsiung:** ASE headquarters and advanced packaging hub; Amkor Taiwan site.
- **Taoyuan:** Substrate suppliers (Unimicron, Nan Ya, Kinsus).
- **Taichung:** SPIL operations (part of ASE).

This forms a **north–south corridor** in Taiwan integrating substrates, foundries, OSATs, and CSP customers.

AP8 Conversion Costs and Strategic Significance

In August 2024, TSMC acquired Innolux's former LCD Plant 4 in Tainan's Southern Taiwan Science Park for NT$17.14 billion (about US$530 million) and is in the process of converting it into its new AP8 advanced packaging facility focused on CoWoS. The conversion is still underway, with equipment installation ongoing and initial production expected to begin in the second half of 2025 before ramping through 2026. While TSMC has not disclosed the full conversion cost, industry benchmarks for repurposing a display fab to advanced packaging suggest a total investment of **US$1.8–2.2 billion** (including acquisition) for ~100k wafers/month capacity. This scale reflects the heavy capital intensity of cleanroom rebuilds, utility upgrades, specialized CoWoS/SoIC equipment, and test infrastructure. AP8 is set to become one of TSMC's largest backend investments to date, underscoring the strategic importance of packaging as the new bottleneck in scaling AI hardware.

Estimated CapEx Breakdown for AP8 Conversion

Category	Estimate (US$M)	Notes
Facility & Cleanroom Rebuild	300–600	Conversion of 96,000 m² LCD space into advanced packaging cleanrooms; includes HVAC, vibration control, water/gas systems.
Power & Utilities	150–250	Electrical upgrades, chilled water, chemical/waste handling, environmental systems.

Category	Estimate (US$M)	Notes
Core Process Tools	700–900	CoWoS (S/R/L) lines, RDL plating, wafer bonding, thinning, dicing, inspection & metrology.
Testing Infrastructure	200–300	Chip probe, burn-in ovens, system-level test (SLT) farms.
Substrate & Panel Handling	100–150	Panel-based (glass) readiness for CoPoS and high pin-count substrate attach.
Other (Staff, Training, Compliance)	50–100	Hiring, IT systems, yield ramp, regulatory compliance.
Subtotal (Conversion)	~1,500–2,000	Excluding acquisition.
Acquisition (Innolux Plant 4)	~530	Paid in Aug 2024.
Total Estimated Investment	~1,800–2,200	Conversion + acquisition, phased 2024–2026.

Industry Implications

TSMC is aggressively expanding advanced packaging on multiple fronts — scaling **CoWoS-L** capacity at AP8 in Tainan, ramping **SoIC** at AP7 in Zhunan, and broadening **WMCM** output for Apple's consumer products. This reflects a multi-directional investment strategy designed to meet surging AI demand while diversifying packaging technologies for both high-performance computing and mobile markets.

At the same time, TSMC is deliberately **leveraging OSAT partners (ASE, Amkor, SPIL)** to absorb increasing workloads. The rationale is twofold:

1. **Overflow Management:** CoWoS demand from AI accelerators (NVIDIA, Broadcom, AMD, AWS, Microsoft, Meta, OpenAI) exceeds TSMC's internal capacity through at least 2026.
2. **Application Segmentation:** TSMC encourages fabless and cloud customers to channel **non-AI products** — including **server CPUs, gaming GPUs, networking ASICs, and high-end PC CPUs** — to OSAT partners. These

products require advanced 2.5D or wafer-level fan-out packaging, but do not face the same urgency as AI accelerators.

This dual approach creates a more balanced and resilient ecosystem. TSMC secures its position as the anchor for bleeding-edge AI packaging, while OSATs scale into broader full-stack CoWoS-like businesses. Over time, this strengthens Taiwan's north–south backend corridor while also expanding the role of OSATs across Taiwan and Southeast Asia.

1. **Supply Chain Interdependence**
    - Foundry (TSMC) + OSATs (ASE, Amkor) + Substrate suppliers (Unimicron, Nan Ya, Kinsus) = inseparable ecosystem.
    - Any weakness in one node delays global AI datacenter buildouts.
2. **Shift from GPU Monopoly to ASIC Plurality**
    - NVIDIA still leads, but Broadcom TPUs, AWS Trainium, Microsoft MAIA, and Meta/OpenAI ASICs ensure diversity.
    - This reduces concentration risk and accelerates innovation.
3. **Advanced Packaging = Strategic Asset**
    - CoPoS and SoIC are the new scaling levers as Moore's Law slows.
    - Control of panel-level packaging and 3D stacking will determine long-term leadership.
4. **Regional Power Shift**
    - Taiwan remains central, but Malaysia/ASEAN (via ASE, Amkor, MPI) will capture more OSAT and substrate activity.
    - This creates a distributed advanced backend footprint across Asia.

What to Watch

- Ramp milestones at AP8 (Tainan) and SoIC lines at AP7 (Zhunan).
- OSAT announcements on CoPoS tooling and test expansions.
- CSP orders translating into OSAT bookings (TPU v7p, Trainium-3, MAIA-3).

- Yield/throughput progress on large-area CoWoS-L packages (NVIDIA Rubin).
- Glass substrate supply chain readiness for panel-based CoPoS.

Glossary of Key Terms

- **TSMC** – Taiwan Semiconductor Manufacturing Company, world's largest foundry.
- **CoWoS** – Chips-on-Wafer-on-Substrate; TSMC's 2.5D packaging platform.
  - **CoWoS-S:** With silicon interposer.
  - **CoWoS-R:** With redistribution layer interposer.
  - **CoWoS-L:** Hybrid with local silicon interconnect.
- **CoPoS** – Chip-on-Panel-on-Substrate; next-gen panel-based packaging.
- **SoIC** – System-on-Integrated-Chips; TSMC's 3D hybrid bonding technology.
- **WMCM** – Wafer-level Multichip Module; Apple's packaging for iPhones.
- **HBM** – High Bandwidth Memory; 3D-stacked DRAM used in AI accelerators.
- **OSAT** – Outsourced Semiconductor Assembly & Test; firms like ASE, Amkor.
- **SLT** – System-Level Test; testing of final packaged systems.
- **CSP** – Cloud Service Provider (e.g., Google, AWS, Microsoft, Meta).
- **ASIC** – Application-Specific Integrated Circuit; custom chips for AI and networking.
- **AP Fabs** – TSMC Advanced Packaging facilities (AP1–AP8).
- **STSP** – Southern Taiwan Science Park, home to AP8.

Closing Note

The next wave of AI infrastructure growth will be constrained not by chip designs or lithography nodes, but by packaging and testing bottlenecks. TSMC's CoWoS, SoIC, and WMCM technologies, together with OSAT partners, form the **backbone**

of global AI supply chains. Companies that secure capacity, optimize yields, and master chiplet-based integration will lead the next decade of compute.