

SEMICONDUCTOR DIGEST

NEWS AND INDUSTRY TRENDS

OCTOBER 2024

Semi-damascene
Metallization p. 28

How SiC is Conquering
E-mobility p. 34

Selecting an MES
Migration
Strategy p. 37

Maximizing the Value
of Wastewater p. 40

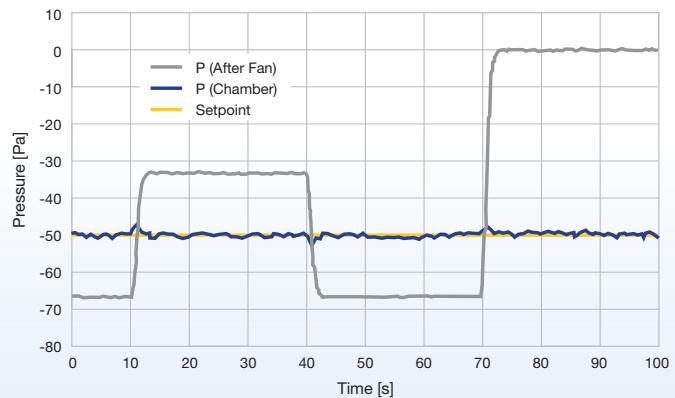
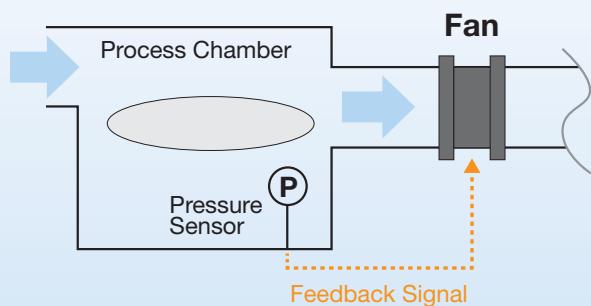


Ion Beam Technology Enabling Mobile Communications p. 20

DON'T LET YOUR EXHAUST CONTROL YOUR PROCESS!

Keep Your Chamber Pressure constant with the Levitronix® MagLev Fan!

Placed on the exhaust line, the fan compensates for pressure fluctuations due to an inconsistent or insufficient central exhaust.



LEVITRONIX® MAGLEV FAN

-  ATEX/IECEx certified
-  High flow capabilities
-  Chemically resistant
-  Low maintenance
-  Magnetically levitated rotor





COVER: Bosch has tailored its semiconductor development to the demands of the automotive industry (pg. 34). *Source: Bosch.*

Columns

2 EDITORIAL

Natcast Launches NSTC Membership Program

PETE SINGER, EDITOR-IN-CHIEF

INDUSTRY OBSERVATIONS

- 47 Navigating the Complexities of Semiconductor Supply Chains Amidst M&A Surge, TAMMY MAX, DIRECTOR OF TECHNICAL CONTENT AT ACCURIS

- 48 Managing the Impact of Semiconductor Manufacturers' Use of Freshwater,

VINCENT PUISOR, GLOBAL BUSINESS

DEVELOPMENT DIRECTOR, WATER AND WASTEWATER AT SCHNEIDER ELECTRIC

- 52 Cracking the Chip Code to Meet AI's Growing Demands, MOZ AHMED, EDGE & EMBEDDED TECHNOLOGY SOLUTIONS

MANAGER AT MOBICA

Departments

4 NEWS

50 AD INDEX

FEATURES

20 ION BEAMS

Ion Beam Technology – Enabling the Ever-evolving Mobile Communications Landscape

Ion beam technology ensures that today's mobile networks remain robust and efficient, paving the way for future innovations in the ever-evolving landscape of mobile communications. **MANDY GEBHARDT, SCIA SYSTEMS**

28 INTERCONNECTS

Semi-damascene Metallization: Inflection Point in Back-end-of-line Processing?

When used in combination with a patternable metal such as Ru, semi-damascene promises to be RC, area, cost and power efficient – offering an interconnect scaling path.

ZSOLT TOKEI, IMEC FELLOW, AND PROGRAM DIRECTOR OF NANO-INTERCONNECTS AT IMEC

34 MATERIALS

How Silicon Carbide Semiconductors Are Conquering E-mobility

Bosch has tailored its semiconductor development to the demands of the automotive industry.

37 FACTORY INTEGRATION

Selecting an MES Migration Strategy for Semiconductor Process Optimization

Migrating to a new MES platform can lower the total cost of ownership of automation and production assets, increase efficiency, revenue, and ultimately, profitability, safety and environmental sustainability. **TOM BEDNARZ, SALES MANAGER TECH EUROPE, CRITICAL MANUFACTURING**

40 WATER TREATMENT

Maximizing the Value of Wastewater Generated During Semiconductor Fabrication

The semiconductor aims to reduce pollutants and freshwater consumption, reuse water, and recycle resources.

ZHAOHUI YAN, GLOBAL MARKET SEGMENT LEAD FOR MICROELECTRONICS AT DUPONT WATER SOLUTIONS

44 WORKFORCE DEVELOPMENT

Solving the Skilled Tech Talent Gap

By implementing strategic workforce management and partnering with experienced experts, semiconductor companies can effectively navigate the talent shortage, build a sustainable workforce, and position themselves for long-term success. **CRAIG WALTERS, VICE PRESIDENT BUSINESS PROCESS OUTSOURCING, SEMICONDUCTOR, KELLY**

Editorial

Natcast Launches NSTC Membership Program



NATCAST, THE NON-PROFIT ENTITY DESIGNATED TO OPERATE THE National Semiconductor Technology Center (NSTC) by the U.S. Department of Commerce, officially launched its Membership program in late September.

NSTC members can benefit from dynamic and cross-sector collaboration; access to leading-edge R&D facilities; development of member-driven research agendas; unique opportunities to research, prototype, and scale up semiconductor technologies; and workforce best practices and initiatives developed through the NSTC Workforce Center of Excellence. These resources, several of which are planned to become available throughout 2025, are aimed at reducing barriers for members to bring new technologies from lab-to-fab as well as supporting member efforts to build and sustain a strong U.S. semiconductor workforce development ecosystem.

"As a public-private consortium, the NSTC represents a bold vision for U.S. semiconductor innovation," said Deirdre Hanford, Natcast CEO. "Today's launch of the NSTC Membership program is a critical step in our evolution as we can now welcome and officially admit members into the consortium."

The NSTC represents the foundation for the next wave of technological breakthroughs, serving as the anchor institution where we shape the future of semiconductor innovation," said Secretary of Commerce Gina Raimo.

The mission of the NSTC is to convene a diverse set of members from across the semiconductor ecosystem around three shared and strategic goals:

- **Strengthening U.S. semiconductor leadership:** Through innovative and member-driven research initiatives, the NSTC will address industry and academia's most pressing semiconductor R&D challenges and extend U.S. leadership in foundational technologies for future applications and industries.
- **Reducing time from lab-to-fab:** By providing members access to collaborative opportunities and leading-edge facilities and capabilities, the NSTC will reduce the time and cost to explore, prototype, and validate innovative semiconductor designs and technology.
- **Expanding the U.S. semiconductor workforce:** Developing and distributing critical workforce and education programming and resources, the NSTC will support members in expanding and sustaining a strong U.S. semiconductor workforce development ecosystem.

NSTC membership is offered in two categories, Core and Affiliate, tailored to support the needs of the broad semiconductor ecosystem. Core membership is designed for entities that are directly involved in semiconductor technology development of materials, tools, processes, design, package or systems. Affiliate membership is designed for organizations that do not conduct semiconductor research but would like to participate and contribute to the ecosystem in areas such as workforce, investments, consortia, or professional services. Learn more about the benefits of becoming an NSTC member and join the mission at natcast.org/NSTCmembership.

—Pete Singer, Editor-in-Chief

SEMICONDUCTOR DIGEST

NEWS AND INDUSTRY TRENDS



Kerry Hoffman, Publisher
kerryh@semiconductordigest.com
978-580-4205



Pete Singer, Editor-in-Chief
psinger@semiconductordigest.com
978-470-1806



Shannon Davis, Web and News Editor
sdavis@semiconductordigest.com

Dave Lammers, Contributing Editor
dplammers@att.net

John Blyler, Contributing Editor
jblyler@semiconductordigest.com

Dick James, Contributing Editor
dickjames@siliconics.ca

Cindy Chamberlin, Art Director

Rich Mehta, Website Design

October 2024 VOL. 6 NO. 7 •
Semiconductor Digest ©2024
ISSN 2643-7058 (print) ISSN 2643-7074 (online).
Semiconductor Digest is published eight times a year by Gold Flag Media LLC, 58 Summer St., Andover, MA 01810. Copyright © 2024 by Gold Flag Media LLC.
All rights reserved. Printed in the U.S.



Particle Defect Inspection

FM-PDS range



fast-micro.com



INNOVATED WITH
TNO

- 400 wafers per hour
- Replace multiple legacy systems for one; save floorspace
- Top- and bottom-side inspection without flipping
- For compound substrates, wafers, pellicles, reticles
- No moving parts: clean and robust
- Pre-scan to accelerate workflow for further particle analysis
- 100 nm sensitivity
- Manual and Automated up to 12-inch wafers

Indirect



Deposition



Direct



info@fast-micro.com

news

eBeam Initiative Survey Predicts Photomask Market Growth and Increasing Investments

The eBeam Initiative, a forum dedicated to the education and promotion of new semiconductor manufacturing approaches based on electron beam (eBeam) technologies, recently completed its 13th annual eBeam Initiative Luminaries survey. Industry luminaries representing 49 companies from across the semiconductor ecosystem – including photomasks, electronic design automation (EDA), chip design, equipment, materials, manufacturing and research – participated in this year's survey.

Mask Inspection, Multi-beam and Laser Mask Writers:
Positive Outlook for Purchasing New Equipment for Any Node*



New: What do you predict will happen to overall investment in equipment purchase for any node over the next 3 years?



* Note: Question was changed from last year which asked about 193i only purchases

Participants in the 13th Annual eBeam Initiative Luminaries survey predict increases in future equipment purchases for multi-beam mask writing and mask inspection over the next three years. Source: eBeam Initiative.

100 percent of survey respondents predict that mask revenues in 2024 will increase (74 percent) or stay the same (26 percent) compared to 2023. Luminaries were also positive on future equipment purchases over the next three years, with increases predicted for multi-beam mask writers (93%), mask inspection (85%) and laser mask writers (48%). In addition, the percentage of luminaries that believe that fabs without EUV can reach 5nm within 7 years has increased from 12 percent last year to 19 percent this year.

New questions were added to the Luminaries

Continued on page 6

First CHIPS Commercial Fabrication Facilities Award Goes to Polar Semiconductor

CHIPS Investment Expected to Nearly Double U.S. Production Capacity of Sensor and Power Chips at Bloomington, Minnesota Manufacturing Facility

The U.S. Department of Commerce announced its first award under the CHIPS Incentives Program's Funding Opportunity for Commercial Fabrication Facilities of up to \$123 million in direct funding to Polar Semiconductor. The award will expand and modernize the company's manufacturing facility in Bloomington, Minnesota. The Department will distribute the funds based on Polar's completion of project milestones.



The investment will support Polar's efforts to almost double its U.S. production capacity of sensor and power chips within two years. This award catalyzes a total investment of more than \$525 million from private, state, and federal sources to transform Polar from a majority foreign-owned in-house manufacturer to a majority U.S.-owned commercial foundry. Through Polar's semiconductor manufacturing operations, the Administration's investment is expected to create over 160 manufacturing and construction jobs in Minnesota.

Polar plans to:

- Double production capacity, ramping up from approximately 20,000 wafers per month to nearly 40,000 wafers per month
- Upgrade and modernize its facility to become globally competitive

Continued on page 8

You Need A MESTA.



Precision, power and control - everything you need for crystal growth and epitaxy operations.

Air-Cooled Induction Heating Power Supply.

- Parallel resonance topology increases system efficiency
- ± 3 Watts output power resolution for a 50kW unit
- Efficiency greater than 97%

Higher yields.
Improved quality.
Reduced costs.

MESTA
ELECTRONICS
an hps company



Continued from page 5

survey this year to gauge perceptions on EUV pellicles and high-NA stitching. 81 percent think that stitching for high-NA EUV masks will require designers to be aware of the stitching boundaries during design. 33 percent believe that EUV mask lifetime is at least 3x longer with pellicles than without.

Additional Perceptions from the Luminaries Survey (conducted in July 2024)

- 74 percent agree that curvilinear inverse lithography technology (ILT) is useful for 193i for non-EUV leading-edge nodes – with 29 percent strongly agreeing with that statement compared to 24 percent last year

- 55 percent say that some critical layers of leading-edge nodes are using ILT today, up from 46 percent last year and 35 percent from two years ago
- Mask shop software infrastructure continues to remain the biggest concern in producing masks with curvilinear shapes
- Predictions on deep learning adoption have slipped a year, with 54 percent predicting that deep learning will become a competitive advantage for any step in the mask making process by 2025, compared to 56 percent who said by 2024 in last year's survey

"We look forward to an exciting week at SPIE Photomask where the eBeam Initiative will be hosting

its 15th annual photomask meeting – demonstrating the continued strong support across the semiconductor ecosystem for this collaborative forum," stated Aki Fujimura, CEO of D2S, the managing company sponsor of the eBeam Initiative. "It's truly an exciting time to be a part of the photomask industry, which has seen such strong growth in recent years – a testament to the amazing talent within the mask community, as well as to the industry's growing importance in driving semiconductor innovation. It's welcome news that the vast majority of participants in this year's eBeam Initiative Luminaries survey, who represent top business and technology experts in the industry, see this growth trend continuing in 2024." 

\$400 Billion in 300mm Fab Equipment Investment Planned Over Next Three Years

Global spending on 300mm fab equipment is expected to reach a record US\$400 billion from 2025 to 2027, SEMI highlighted in its quarterly 300mm Fab Outlook Report to 2027 report. The robust spending is being driven by the regionalization of semiconductor fabs and the increasing demand for artificial intelligence (AI) chips used in data centers and edge devices.

Worldwide, 300mm fab equipment spending is projected to grow by 4% to US\$99.3 billion in 2024, and further increase by 24% to US\$123.2 billion in 2025, surpassing the US\$100 billion level for the first time. Spending is forecast to experience 11% growth to US\$136.2 billion in 2026 followed by a 3% increase to US\$140.8 billion in 2027.

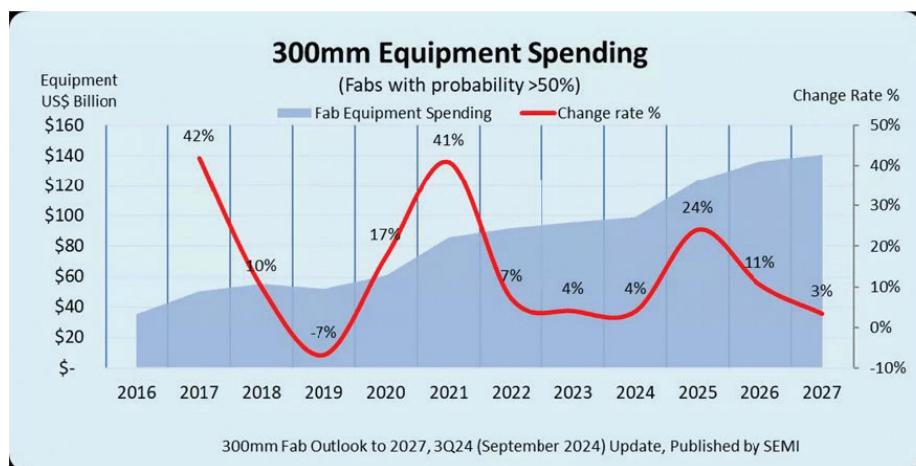
"The magnitude of the expected

ramp of global 300mm fab equipment spending in 2025 sets the stage for a record-setting three-year period of semiconductor manufacturing investments," said Ajit Manocha, SEMI President and CEO. "The world's ubiquitous need for chips is boosting spending on equipment for both leading-edge technologies addressing AI applications and mature technologies driven by automotive and IoT applications."

Regional growth

China is projected to maintain its position as the top spending region on 300mm equipment globally until 2027, investing over US\$100 billion in the next three years driven by its national self-sufficiency policies. However, spending is anticipated to gradually decrease from a peak of US\$45 billion in 2024 to US\$31 billion by 2027.

Korea is projected Continued on page 8



Measuring the Invisible

XM8000™

Automated X-ray Metrology



Advance your Semiconductor X-ray Metrology with XM8000™

Nordson's XM8000™ AXM system provides industry-leading measurement of micron-scale features in wafer and panel level advanced packaging applications.

- Using proprietary imaging chain including Nordson's own design X-ray tube and CMOS detectors to generate ultra-high resolution images capable of detecting and measuring hidden defects within complex semiconductor packages.
- Successfully being used to enhance packaging quality in a variety of applications including bump voiding, TSV/TGV measurement, fill analysis and chip gap height measurement.

Count on the XM8000 to improve your semiconductor advanced packaging yields, processes and productivity.

Continued from page 6

to rank second and invest US\$81 billion in the next three years to further its dominance in memory segments including DRAM, high-bandwidth memory (HBM), and 3D NAND Flash. Taiwan is forecast to spend US\$75 billion on 300mm equipment over the next three years, ranking third as the region's chipmakers build some new fabs overseas. Leading-edge logic below 3nm is the primary driver of Taiwan fab investments.

The Americas is projected to invest US\$63 billion from 2025 to 2027, while Japan, Europe & Mideast, and SE Asia are expected to spend US\$32 billion, US\$27 billion, and US\$13 billion, respectively, over the three-year period. Notably, these regions are anticipated to more than double their equipment investment in 2027 compared to 2024 due to policy incentives earmarked to alleviate concerns on the supply of crucial semiconductors.

Segment growth

Foundry equipment spending is projected to reach approximately US\$230 billion between 2025 and 2027, fueled by investments in sub-3nm cutting-edge nodes as well as continued spending on mature nodes. Investment in 2nm logic processes and development of key technologies at 2nm, such as gate-all-around (GAA) transistor structure and back-side power delivery technology, is crucial to meet future high-performance and energy-efficient computing needs, particularly for AI applications. Cost-effective 22nm and 28nm processes are expected to see growth due to increasing demand for automotive electronics and IoT applications.

The Logic and Micro segment is projected to spearhead the equipment spending expansion over the next three years, with an anticipated total investment of US\$173 billion. Memory comes in second, expected to contribute over US\$120 billion in spending

during the same period, marking the beginning of another segment growth cycle. Within Memory, investment in DRAM-related equipment is projected to surpass US\$75 billion, while investment in 3D NAND is expected to reach US\$45 billion.

The Power-related segment ranks third, with an expected investment of over US\$30 billion over the next three years, including around US\$14 billion for compound semiconductor projects. The Analog and Mixed-signal segment is projected to reach US\$23 billion during the same period followed by Opto/Sensors at US\$12.8 billion.

Part of the SEMI Fab Forecast database, the SEMI 300mm Fab Outlook Report to 2027 report lists 420 facilities and lines globally, including 79 high-probability facilities expected to start operation during the four years beginning in 2024. The report reflects 169 updates and nine new fabs/lines projects since its last publication in June 2024. ■

SEMI and IESA Join to Strengthen Semiconductor Ecosystem

In a strategic move to further solidify India's position in the global semiconductor value chain, SEMI®, the global industry association that connects the semiconductor and electronics design and manufacturing value chain, has announced a strategic agreement with the India Electronics and Semiconductor Association (IESA), the leading industry body representing the electronics and semiconductor sectors in India. IESA will become part of the global SEMI family and represent SEMI in India. IESA will continue to use its current brand while beginning to implement SEMI's processes and select initiatives.

The announcement comes at a pivotal time, the start of SEMICON India 2024,

the flagship event aimed at bringing together global leaders, semiconductor industry experts, and key stakeholders under the theme of "Shaping the Semiconductor Future."

This unification is set to bolster India's ambition to become a "Semiconductor Powerhouse" by advancing its design and manufacturing ecosystem. Together, the associations will enhance domestic manufacturing in line with India's "Make in India" initiative, support workforce development, improve global competitiveness, and foster greater technological self-reliance. Additionally, SEMI members will now have direct access to India's growing semiconductor market, tapping into new growth opportunities.

Ajit Manocha, President and CEO, SEMI, expressed his excitement about this milestone, stating, "India holds immense potential in the semiconductor space, and many global companies are already exploring the opportunities within the country's semiconductor industry. This partnership will help SEMI grow a strong presence in this critical emerging market and enable both organizations to identify tangible strategies that leverage our combined strengths to enhance supply chain resilience."

Dr. Veerappan, Chairperson, and Ashok Chandak, President, IESA, emphasized the strategic significance of the partnership, saying, "This milestone is a major

Continued on page 10



DROWNING IN DATA?

VISUAL DATA SCIENCE CAN HELP



www.spotfire.com

Continued from page 4

- tive through economies of scale
- Deliver cutting-edge semiconductor solutions to the U.S. automotive, aerospace, defense, optoelectronics, MEMS, and medical device industries, and
 - Create 160+ new jobs, strengthening Polar's commitment to its community and driving economic growth in the State.

"As a domestic U.S.-owned sensor and advanced power semiconductor merchant foundry, we will support technology and design innovation, protect intellectual property, facilitate onshoring and technology transfers, and provide efficient low- to high-volume manufacturing with world-class quality," said Surya Iyer, President and Chief Operating Officer of Polar Semiconductor. 

Continued from page 8

win for India, SEMI, and IESA. It positions India to become a global semiconductor powerhouse, accelerates economic growth, and fosters innovation. By combining our capabilities with SEMI's global standards, network, and resources, we are fortifying India's ambitions and attracting global partnerships and investments to scale up design, manufacturing, and production capacities."

This agreement will also pave the way for joint policy advocacy efforts, with IESA and SEMI working closely with both Central and State governments to drive incentives for product development and manufacturing, leveraging key programs such as the Production Linked Incentive (PLI) and Design Linked Incentive (DLI) models.

The Semiconductor Executive Forum, held on 10th Sept ahead of the SEMICON India event chaired by Mr. Ashvini Vaishnav, Hon'ble Minister for Railways, Electronics and IT and

Information and Broadcasting, saw participation from over 100 industry leaders from SEMI member companies, with a significant participation of IESA members. Fourteen members (CxOs) from SEMI and IESA engaged in an interactive discussion with the Hon'ble Prime Minister of India, Mr. Narendra Modi, focusing on the fast-track development of the semiconductor ecosystem. Global CxOs

elevated the forum with valuable insights, offering guidance to both the government and industry on how to transform the current industry momentum into sustained business growth. SEMICON India 2024, with 250+ exhibitors, 650+ booths, 100+ global companies and 50+ CxOs in attendance 11-13th Sept 2024, is shaping up to be the largest semiconductor event in India's history. 

NY CREATE\$ Receives \$4.7M NSF Grant to Launch Semiconductor Workforce Development Program

The New York Center for Research, Economic Advancement, Technology, Engineering, and Science (NY CREATE\$) announced it has been awarded a \$4.7 million grant from the National Science Foundation (NSF) to support the establishment of the Education Alliance for Semiconductor Experiential Learning (EASEL) program. This workforce development initiative aims to help address the growing national demand for a skilled workforce in the semiconductor industry, a critical need highlighted by the U.S. CHIPS & Science Act.

The U.S. CHIPS & Science Act, a transformational investment in the nation's semiconductor industry, will help create an estimated 280,000 jobs across the computer chip industry, with nearly half of those positions requiring skilled technicians. EASEL will play a pivotal role in filling these technician positions by providing hands-on, immersive learning experiences for college students from across the U.S. at NY CREATE\$' Albany NanoTech Complex to help them hit the ground

running in semiconductor careers. EASEL will also provide similar experiences to teachers and instructors to better prepare them to educate the nation's semiconductor workforce.

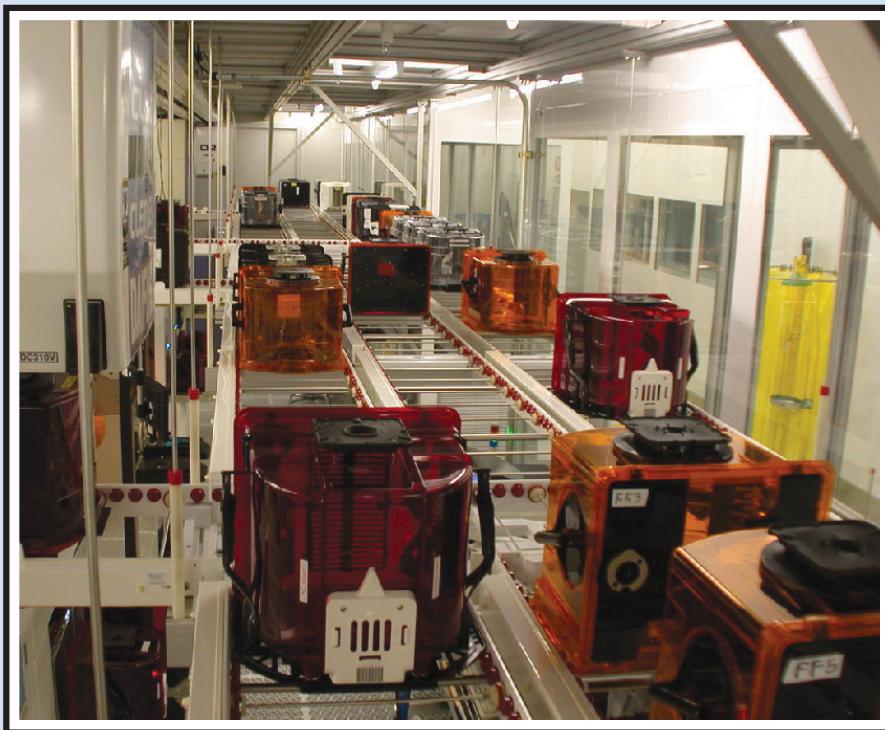
Senate Majority Leader Charles Schumer said, "This \$4.7 million from my CHIPS & Science law will help college students from across America come to Albany NanoTech to get hands-on training and become the next generation of America's semiconductor workforce. It will bring together community colleges, including Onondaga Community College, who are launching chip technician programs now and give them access to the most cutting-edge research facilities to get them ready for good-paying jobs at companies like Micron and GlobalFoundries."

Senator Kirsten Gillibrand said, "This is a long overdue investment in one of the Capital Region's most important bridges. I'm proud to have fought for federal funding for this project and will continue to fight for every dollar necessary to get this restoration done."

"We are thrilled Continued on page 12

AUTOMATION KIND PROMOTES TOOL UTILIZATION

BY ENABLING VEHICLE LINE CAPACITY GROWTH IN THE FIXED TOOL SPACE



INTEGRATES CONVEYORS INTO OHT VEHICLES

- CONFORMS TO SEMI EQUIPMENT INTERFACE
- ADD LOCAL STORAGE WITHOUT FLOOR SPACE
- AUTO SORT AND BUFFER BATCHES ON SITE
- NESTS DYNAMIC BUFFERS INTO EXISTING OHT LINES
- REDUCE AMHS CENTRAL LINE STOCKER USE
- IMPROVES TOOL-SET CYCLE TIMES
- REDUCES MATERIAL HANDLING COMPLEXITY



65 YEARS OF INNOVATION
19 GLOBAL PATENTS

INTEGRATORS/OEMs WELCOMED (APPLY FOR FREE LICENSE)

info@midsx.com
or phone + 1-781-935-8870

Continued from page 10

to receive this grant from the NSF to further train a robust semiconductor-focused workforce," said NY CREATES President Dave Anderson.

"We look forward to engaging with our industry partners, including Micron and Global-Foundries, as well as with our initial cohort of academic institutions to connect students with this program.

Providing them the vital skills required to contribute to this area of research, development, and manufacturing is critically important for New York State and the U.S., especially given the exciting promise of the U.S. CHIPS & Science Act which is already driving industry expansion."

The EASEL program will bring together a coalition of community colleges and leading U.S. semiconductor manufacturers to develop and implement multi-modal experiential learning opportunities. Initially, the alliance will include



four core community colleges—Columbus State Community College, Onondaga Community College, LaGuardia Community College, and Madison Area Technical College—and will expand to include additional institutions across key semiconductor manufacturing regions in the U.S.

Over the course of the four-year project, EASEL is expected to support up to 660 student learners

and faculty participants, providing over 43,000 hours of immersive experiential learning and 4,000 hours of faculty technical development. The project will leverage the unique capabilities of NY CREATES, which operates the largest non-profit 300mm semiconductor R&D facility in North America, offering a complete integrated circuit process flow down to the 5-7nm device node. ■

Jabil Expands Silicon Photonics Capabilities

Jabil Inc. today announced its continued investment in silicon photonics-based products and capabilities to support the increasing demands of hyperscalers and next-wave cloud and AI data center growth. The company is set to roll out additional capabilities at its Ottawa, Canada, site in the fourth calendar-year quarter of 2024 to support customers' advanced photonics packaging new product introductions (NPIs).

The new product introduction (NPI) line will feature innovative capabilities designed to assist photonics customers quickly scale from proof of concept to mass production, such as fluxless flip-chip, fiber attachment, precise die bonding, and

wire bonding. These advancements will support silicon photonics chip packaging, particularly in high-speed connectivity applications such as co-packaged optics (CPO) and high-speed on-board connections. By leveraging Jabil's expertise, customers can benefit from enhanced performance and reliability in their photonics solutions, ultimately driving agility and scalability in their operations.

"The expansion of our Ottawa site is a game-changer for Jabil. This facility will enable us to meet the growing demands for advanced photonics solutions tailored to AI and next-generation data centers. Through our NPI capabilities, we can assist customers in their own product

development journeys, significantly reducing the need for costly trial and error in developing their own solutions from scratch," said Matt Crowley, Executive Vice President, Global Business Units.

Jabil continues to pioneer industry-first "silicon to solutions" manufacturing approaches that improve the scalability of current and next-generation photonics, including 800G and 1.6T. The company also continues to make investments in next-generation silicon photonic technologies beyond 800G and 1.6T to support AI and cloud computing, focusing on optimized performance and reduced power consumption for modern data centers. ■

A New Spin on Inspection

SpinSAM™

Acoustic Inspection



The SpinSAM automated inspection system delivers industry-leading throughput with unparalleled sensitivity for accurately locating defects in wafer based assemblies.

The SpinSAM's innovative spin scanning method efficiently and accurately scans up to 4 (300mm) wafers simultaneously, at 41 wafers per hour with best-in-class defect capture and image quality. With 4 matched waterfall transducers, the SpinSAM was meticulously engineered to attain full wafer scans in less than 6 minutes.

Ideal applications include bonded wafers, Chip-on-Wafer, stacked wafers, MEMS, over-molded wafers and more.

A New Ventilator-on-a-chip Model to Study Lung Damage

In a new study, using a ventilator-on-a-chip model developed at The Ohio State University, researchers found that shear stress from the collapse and reopening of the air sacs is the most injurious type of damage.

This miniature “organ-on-a-chip” model simulates not only lung injury during mechanical ventilation, but also repair and recovery, in human-derived cells in real time, said co-lead author Samir Ghadiali, PhD, professor and chair of biomedical engineering at Ohio State.

“The initial damage is purely physical, but the processes after that are biological in nature — and what we’re doing with this device is coupling the two,” Ghadiali said.

The team hopes the device will also help in the hunt for therapies to address ventilator-induced lung injury.

“This is an important advance in the field that will hopefully allow for a better understanding of how lung injury develops in mechanically ventilated patients and identification of therapeutic targets so that we can give drugs to prevent that kind of injury or treat it when it happens,” said co-lead author Joshua Englert, MD, associate professor of pulmonary, critical care and sleep medicine at The Ohio State University Wexner Medical Center.

The research was published recently in the journal *Lab on a Chip*.

Ventilators save the lives of patients with severe respiratory problems related

to disease or trauma, but it has been known for a long time that the mechanical forces exerted on the lungs also cause injury. The damage at the cellular level can make the barrier between tiny air sacs and capillaries carrying blood become leaky, leading to fluid buildup that interferes with oxygen getting to the lungs.



Of particular value is the ventilator-on-a-chip’s measurement of real-time changes to cells that affect the integrity of that barrier, enabled by an innovative approach: growing human lung cells on a synthetic nanofiber membrane mimicking the complex lung matrix. It’s closer to the authentic ventilated lung microenvironment than any similar lung chip systems to date, the researchers say.

The device measures the effects of three types of mechanical stress on the integrity of the barrier: lung cell stretch from overinflation, increased pressure on lung cells, and cyclical collapse and reopening of air sacs.

Experiments showed that overinflation with a high volume of air and

cyclic collapse and reopening of air sacs both led the barrier to become leaky, but the cells could recover more quickly from overinflation than from the repetitive opening and closing of air sacs.

Englert said the collapse and reopening may be more problematic because it makes fluid in the lungs move, exposing cells to high amounts of shear stress.

“There really hasn’t been a lot of data that could allow for the comparison of those two injurious forces in the same system,” he said. “But now for the first time, we can use the same device with the same cells and induce both types of injury and see what happens. Our data suggests neither one of them is good,

they’re both injurious, but that the collapse and reopening seems to be more severe and makes recovery harder.”

This finding was a demonstration of the model’s sophistication, Ghadiali said.

“We knew for a long time that collapse and reopening is a pretty injurious force, but we never could measure it in real time,” he said. “Now that we know that collapse and reopening injury happens much quicker and takes a long time to recover, we plan to use the ventilator on a chip to figure out how to prevent this injury and/or enhance the repair.”

Next steps involve modeling diseases such as pneumonia and traumatic injuries experienced by ICU patients in combination with mechanical action. ■

Improve OPERATIONAL EFFICIENCY

The semiconductor fab industry has grown rapidly, identifying three drivers for improved operational efficiency:

- 1** Supply chain disruption and chip shortages mean fabs are expanding while needing to become more responsive.
- 2** A trend for regionalization and localized manufacturing has emerged, which can lead to operational challenges.
- 3** An industry competency gap is leading to workforce transformation, which impacts efficiency.

How can we transform the operational efficiency problem into a business opportunity?

Remote expert support

Engaging a remote expert support team can help manage real-time alerts.

This is particularly beneficial during:

- The early stages of a fab's operation when the learning curve is high and numerous alerts, including nuisance alarms, are common.
- Brownfield plants that have new hires or unanticipated or emergency issues, to provide guidance and real-time training.

Integrated, unified operations

The increased processing power and capabilities in the rise of smart chip products present challenges for fabs.

A common digital thread across the entire plant is needed to anticipate and solve complex issues.

Get the whitepaper
and make an

IMPACT

se.com/ww/en/work/solutions/for-business/semiconductor/



Shared practices across fab facilities

Fab utilities can be varied and complex, including:

- | | | | |
|--|-------------------------|--|-----------------|
| | Electrical distribution | | Natural gas |
| | Chilled water | | Chemical supply |
| | Space heating | | |

Top-layer software coordinates teams and pulls processes and procedures together across the facilities management team.



Schneider Electric recommends integrated operations between facility, construction and operations teams.

Life Is On | Schneider
Electric

Record Semiconductor Revenue in 2Q24, Despite Market Weakness

In a new analysis, Omdia reports that total semiconductor revenue reached a record high of \$162.1 billion in 2Q24, marking a 6.7% quarterly growth. This figure surpasses the previous record set in 4Q21 by approximately \$500m. The record growth was largely driven by NVIDIA, the industry's top revenue generator, which now has quarterly semiconductor revenue \$18 billion higher than 4Q21.

While 2Q24 set a new revenue record, not all companies are benefitting. Although revenue for the semiconductor market is \$33 billion higher than a year ago, over 50% of the companies tracked recorded lower semiconductor revenue compared to a year ago. This shows that the market's revenue growth is not being shared by half of the companies. Of the 125 companies tracked in both the record quarters of 4Q21 and 2Q24, more than 70% had lower semiconductor revenue in 2Q24 than in 4Q21.

NVIDIA's revenue is now more than four times greater than it was during the semiconductor industry's previous record in 4Q21. Without NVIDIA, the

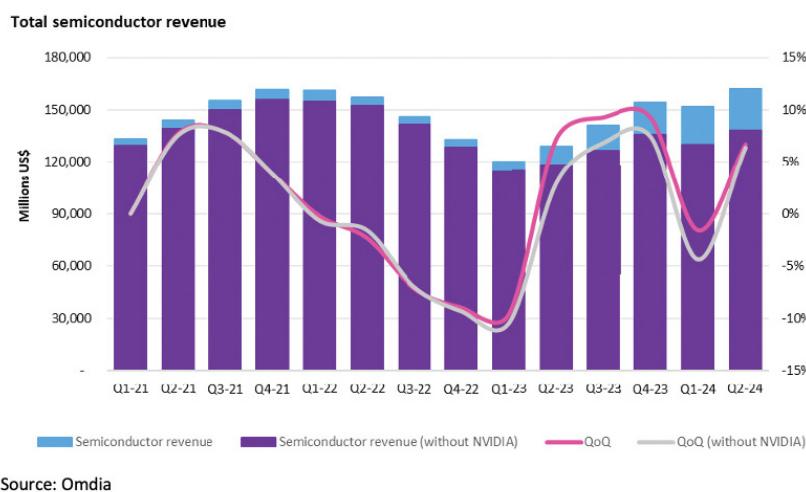
market would be far from reaching a new revenue high. Excluding NVIDIA's revenue, the record remains 4Q21 with total revenue of \$155.8 billion, while

with quarterly revenue now exceeding \$40 billion.

Commenting on the latest industry performance, Cliff Leimbach, Principal Analyst, Omdia stated: "The top semiconductor companies are growing larger. The top ten companies by revenue now account for 64% of the total market in 2Q24, the highest share on record and up seven percentage points over the five-year average of 57%. A comparison to the last record revenue quarter in 4Q21 shows that the market gains are being concentrated

among fewer companies. In 4Q21 the top ten held 57% of the revenue share.

"NVIDIA continues to expand its market share, now representing 14.8% of the semiconductor market by revenue, driven by strong AI demand. Intel, historically either the top or the second largest company remains in third place for the third consecutive quarter. With a 7.5% share in 2Q24, this marks Intel's lowest market share since Omdia began tracking the semiconductor market, in 1Q02," concludes Leimbach. 



Source: Omdia

Total semiconductor revenue

2Q24 revenue stands at \$138.2 billion - over \$17 billion lower.

NVIDIA's dominant position is mainly due to AI demand, though other semiconductor segments are also benefitting from AI growth.

Memory firms are benefitting from AI demand, particularly due to High-Bandwidth Memory (HBM) chips that support AI processors. Additionally, the memory market has seen an improved supply/demand balance, boosting other areas. Following a challenging 2023 the market has recovered,

SWAP Hub Team Awarded Project to Develop High Power, High Frequency Power Converter

The Department of Defense has announced that the Southwest Advanced Prototyping (SWAP) Hub based at Arizona State University (ASU) has been

awarded \$5M in funding by the CHIPS and Science Act for a Multi-MHz, High Density, Ultra-fast RADAR Power Convert project that will advance

radar power systems in critical defense applications.

Researchers at the SWAP Hub are developing a comprehensive suite of

technology innovations to unlock the multi-megahertz promise of gallium nitride (GaN) to achieve ultra-low size and weight, high efficiency and order of magnitude improvements in transient response and power quality of power conversion systems.

The project will specifically develop a multi-megahertz, multi-kilowatt, high-density ultra-fast radar power converter that forms the heart of advanced radar systems. The converters will use GaN-based switching devices and lead to dramatic performance improvements including six times higher power density, 50% lower losses and ultra-fast response times. It is being funded with \$4.97 million from the Department of Defense in its first year.

This is one of five project awards to the SWAP Hub, part of the CHIPS and Science Act-funded Microelectronics Commons, a network of



regional technology hubs. It connects the Southwest — the fastest-growing and largest semiconductor cluster in the United States with more than \$100 billion in private investment — to a growing network of defense and electronics partners across the country. The SWAP Hub is one of eight U.S.

DOD Microelectronics Commons Hubs across the country dedicated to advancing technology for national security.

The radar power converter project is led by ASU and includes partner organizations Lockheed Martin Corp., Sandia National

Continued on page 18

YOUR COMPLETE SUBFAB PARTNER.

Vacuum pumps.
Gas abatement.
Leak detection.
Global service.



From load lock pump down to the harshest processes, Busch provides leading semiconductor Fabs with vacuum pumps and abatement solutions, full SubFab management, and support tailored to your needs.



Contact us today!
Scan to learn more

1-800-USA-PUMP | info@buschusa.com | buschusa.com

U
BUSCH
VACUUM SOLUTIONS

Laboratories, Infineon Technologies Americas Corp., and ThermAvant Technologies.

"This project has potential to enable increased system power within pre-allocated volume and weight constraints, increasing mission capability," said Raja Ayyanar, leader of the project and a professor of electrical, computer and energy engineering at ASU.

In addition to the partner organizations, other collaborators at ASU are Bertan Bakkaloglu, professor of electrical, computer and energy engineering, Mike Ranjram, assistant professor electrical, computer and energy engineering and Ayan Mallik, assistant professor at ASU's Polytechnic School.

Infineon Technologies Americas Corp., will supply state-of-the-art GaN-based power devices which can operate at higher frequencies and higher efficiencies compared to the incumbent silicon-based power devices, says Sameh Khalil, senior principal engineer at Infineon Technologies. "Infineon will also perform accelerated lifetime tests and evaluate device robustness and reliability," he added.

The superior performance characteristics of the GaN devices is a key driver, but the other technologies are critical in enabling the proposed ultra-high switching frequency operation of GaN devices.

Ayyanar said the GaN devices need to be robustly characterized for their critical parasitics and long-term reliability; active gate drive technology and packaging need to be advanced to efficiently drive the GaN devices at multi-megahertz frequencies; circuit topologies and control are needed to support these frequencies, enable fast response and minimize the volume-dominant magnetics; low-loss, high frequency magnetic core materials and planar designs must be advanced; and new thermal management solutions will be critical to alleviate hot spot temperatures and support the proposed extreme power densities of the new devices.

Each partner organization will bring specific, yet complimentary expertise to the project.

- Infineon Technologies Americas Corp.'s roles include providing advanced GaN devices, characterization for multi-MHz operation, reliability testing and techno-economic analysis.
- Sandia's roles include development of advanced magnetic materials and components, heterogenous integration and advanced packaging of power devices.
- Lockheed Martin's roles include defining system specifications, design oversight, simulation, test execution to applicable electrical/environmental conditions and technology transition.

ThermAvant will develop advanced thermal management using its oscillating heat pipe technology.

- ASU's roles include development of advanced circuit topologies, adaptive gate driver, high density planar magnetics, high performance control, converter design, fabrication and integration.

ThermAvant Technologies is the leading oscillating heat pipe provider, primarily for larger-scale aerospace and U.S. defense platforms. Under the proposed workplan, novel small-scale 3-D oscillating heat pipes will be demonstrated to manage the high power-densities and unique packaging requirements being developed by ASU and its partners, explained Joe Boswell, co-founder and CEO of ThermAvant Technologies.

"This is an enormous opportunity for oscillating heat pipes to be packaged within advanced power converters to thermally manage their power-dense components – and do so with minimal size, weight, and cost-or-complexity when integrating into real-world radar systems," Boswell said.

"We are eager to pull together all of the pieces of this project and are excited to get started on it to see where this technology advancement will lead to," Ayyanar added. ■

SEMI Consortium to Develop Cybersecurity Strategy and Roadmap

Seeking to strengthen the semiconductor industry's resilience to cybersecurity threats, the global association SEMI announced the creation of a strategic roadmap for cybersecurity implementation throughout the industry. The SEMI Semiconductor Manufacturing Cybersecurity Consortium (SMCC) has

partnered with the National Institute of Standards and Technology (NIST) to develop a semiconductor manufacturing industry profile for NIST Cybersecurity Framework 2.0 (CSF 2.0) that will serve as the foundation for the aforementioned roadmap. NIST plans to publish the profile in mid-2025.

According to research by the Identity Theft Resource Center, cyberattacks rose by 72 percentage points in 2023 over the previous all-time high in 2021. As semiconductor factories become increasingly connected and autonomous, the industry must respond to the growing security vulnerabilities associated with this next level

of digital reliance and align with broader government efforts to secure the building blocks of technologies vital to society.

"Semiconductors are integral to both national security and the global economy – we need to do everything in our power to protect the industry," said Cherilyn Pascoe, Director of the National Cybersecurity Center of Excellence (NCCoE) at NIST. "NIST is pleased to partner with SEMI SMCC for the development and adoption of a NIST Cybersecurity Framework 2.0 Profile for Semiconductor Manufacturing. This collaboration is important to identify and reduce cybersecurity challenges in semiconductor manufacturing."

"It's important to recognize and address the unique cybersecurity challenges facing the semiconductor industry," said Jennifer Lynn, SMCC Working Group Chair and Semiconductor Cybersecurity Lead at IBM

Research. "This community profile could allow us to better identify and execute a path forward."

In support of the 2023 National Cybersecurity Strategy's strategic objective to secure global supply chains for information, communications and operational technology products and services, the White House Office of the National Cyber Director (ONCD) included a Cybersecurity Framework Profile as part of initiative 5.5.5 in the National Cybersecurity Strategy Implementation Plan Version 2. SMCC recognized the need for a cybersecurity community profile specific to semiconductor manufacturing and worked with the federal government to develop one.

"Unlike air, space, land, and sea, cyberspace is the only battle domain created entirely by human hands," said Anjana Rajan, Assistant National Cyber

Director for Technology Security at ONCD, during the Global Executive Cybersecurity Forum at SEMICON West 2024. "This means we have both the power and the responsibility to shape it. The future of cyberspace where defenders have an inherent advantage over attackers starts with preparation, and that preparation must begin with securing the building blocks."

Prior to completion, the community profile will open for public review and commentary in accordance with NIST's official process. The review period has yet to be announced. The community profile is part of a broader NIST strategy to further standardize cybersecurity protocols for the semiconductor sector, in line with profiles for other industries.

"With the committed resources and support from NIST to support SMCC working groups, we'll be able to accelerate the

Continued on page 50



Technology to Do More.

Big Ideas, The Best Team,
The Right Solutions.

Our lithography and inspection systems bring together the winning combination of over a century of Nikon innovation and the most dedicated employees in the world to deliver the right solutions for our customers.



**Join Our Team!
We're Hiring!**

See us at SEMICON Europa Booth C1359 or visit www.nikonprecision.com

Ion Beam Technology – Enabling the Ever-evolving Mobile Communications Landscape

MANDY GEBHARDT, scia Systems

Ion beam technology ensures that today's mobile networks remain robust and efficient, paving the way for future innovations in the ever-evolving landscape of mobile communications.

MOBILE COMMUNICATION technology has revolutionized how we connect, interact, and conduct business. At the heart of this revolution are frequency filters. These critical components ensure signals' proper transmission and reception by isolating specific frequency bands to minimize interference and improve signal clarity. High-quality filters ensure better signal clarity, reduce interference, and improve overall network reliability.

Among the advanced techniques used to produce high-quality high-frequency filters, ion beam processing technology stands out due to its precision and efficacy. High-frequency filters in mobile communication incorporate many layers of thin films composed of various materials. The uniformity requirements for each film layer are very high. The application of ion beam processing technology for trimming these films to the required dimensions can significantly enhance the performance of mobile communication systems.

Ion beam etching overview

Ion beam etching (IBE) - also known as ion beam milling (IBM) - is ideally suited for precise surface processing. The technology uses a directed beam of high-energy ions to selectively remove

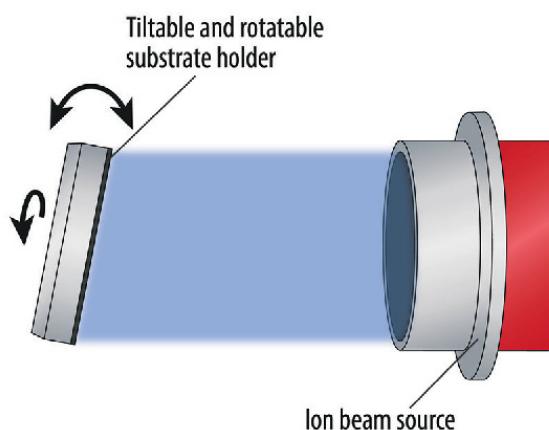


Figure 1. Scheme of an IBE/IBM process that uses a collimated beam of inert gas ions for structuring or material removal.

material from the surface and create specific patterns or structures. The ion beam process combines physical and chemical etching. Physical etching uses the kinetic energy of fast inert ions bombarding the surface to sputter, releasing atoms from the target surface. That process works on all materials facing the ion beam. Chemical etching utilizes a chemical reaction between the reactive ions and the target surface. The reaction products must, therefore, be volatile.

A broad beam of positively charged ions, typically

argon ions, is accelerated onto a substrate (**FIGURE 1**). The ions transfer their kinetic energy to the surface atoms, causing them to be ejected, thus removing the material. The ion beam is typically larger in diameter than the substrate size. That ensures sufficient removal uniformity and throughput. During milling, the wafer substrate can rotate for the best uniformity. Chemically reactive gases can be added to enhance the etch rate.

By varying the angle of incidence and the substrate rotation, material removal can be adjusted precisely to achieve a perfect etching structure with superior homogeneity.

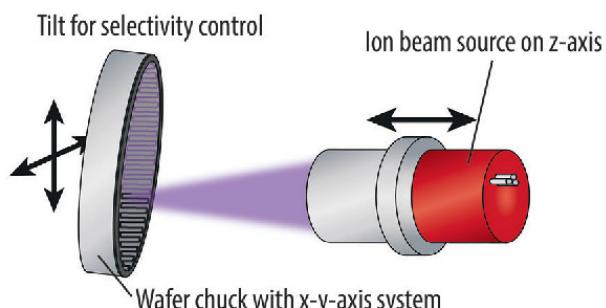
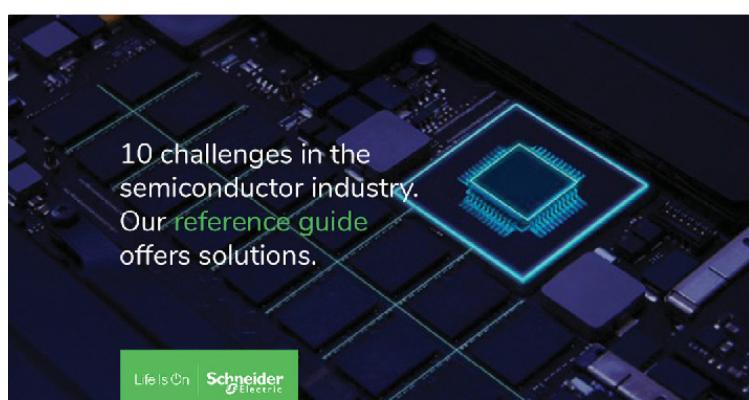
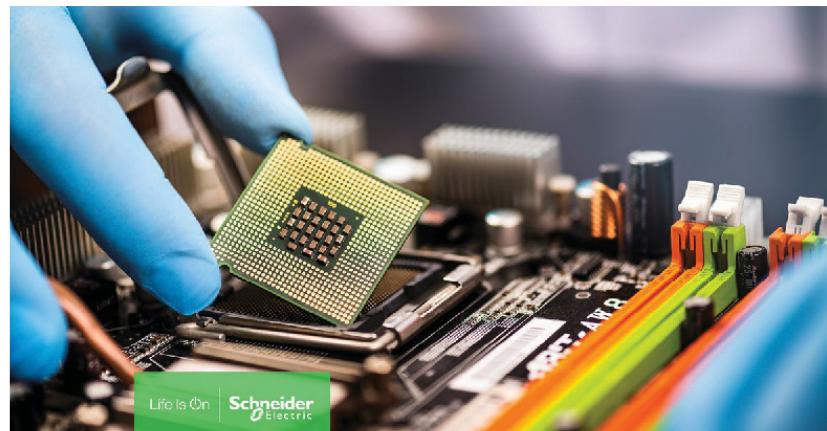


Figure 2. Scheme of an IBT process; a focused broad ion beam raster scans across the wafer. The local material removal is controlled by adjusting the dwell time.

Optimize Fabs for New Business Opportunities

The semiconductor fabrication industry's rapid global growth presents a spectrum of critical business challenges, including sustainability, power reliability, cybersecurity, time-to-market, supply chain, energy efficiency, operational optimization, and workforce management.

Schneider Electric reference guide offers strategies to conquer these challenges and turn them into opportunities. Using specific use cases, it is demonstrated how leading



Scan to download the complete reference guide.



Schneider
Electric™

practices empower semiconductor fabs to enhance their global competitiveness. Each use case in the guide details the driving factors, best practices, and includes a sample case study. Addressing these challenges enables companies to transform industry hurdles into avenues for improved global competitiveness.

Schneider Electric

Website: <https://www.se.com/ww/en/>

Schneider's purpose is to create Impact by empowering all to make the most of our energy and resources, bridging progress and sustainability for all. At Schneider, we call this Life Is On. Our mission is to be the trusted partner in Sustainability and Efficiency. We are a global industrial technology leader bringing world-leading expertise in electrification, automation and digitization to smart industries, resilient infrastructure, future-proof data centers, intelligent buildings, and intuitive homes. Anchored by our deep domain expertise, we provide integrated end-to-end lifecycle AI enabled Industrial IoT solutions with connected products, automation, software and services, delivering digital twins to enable profitable growth for our customers.

DOWNLOAD THE COMPLETE REFERENCE GUIDE NOW!

This allows for the creation of many different geometries in a wide spectrum of processable materials.

Ion beam trimming

Ion beam trimming (IBT) is a particular type of IBE that physically uses a small beam of positively charged ions (e.g., Ar^+) to etch material from a substrate by ion bombardment (**FIGURE 2**). A beam width of typically 8–15 mm (FWHM) ensures a sufficient lateral resolution and a high throughput. During trimming, a focused broad ion beam moves in a meander-shaped pattern across the substrate surface. By altering the local dwell time, it is possible to precisely adjust the material thickness and, hence, device properties like the frequency of acoustic filters. By introducing an additional reactive gas into the ion beam source, a reactive structuring of the surface – the so-called reactive ion beam trimming (RIBT) – is applied.

Advantages of ion beam processes

Ion beam processes offer several advantages. They can be applied to almost all materials. Ion beam machining is always contactless and nondestructive and does not create mechanical stress on the substrate's surface, thus avoiding subsurface damage. The ion beam current, energy, and etching rates can be independently controlled, allowing for precise material removal and excellent uniformity across the etched surface. Furthermore, ion beam processes offer high resolution, making them suitable for detailed, intricate designs and sidewall shaping through simple sample tilting.

These advantages make ion beam

processes powerful tools for precise material processing in various fields, such as semiconductor and MEMS manufacturing, and materials science.

Surface acoustic wave devices

Modern mobile communications depend increasingly on frequency filters since more and more communication standards with often multiple frequency bands have been established. A huge part of these filters is realized using the surface acoustic wave (SAW) mechanism, which transports energy through materials exhibiting elasticity by propagating acoustic waves confined to the surface to a depth of about one wavelength.

SAW filters have remarkable efficiency and strong suppression of frequencies outside the transmission bands. Thus, an extremely high Q factor, meaning the oscillating system, is remarkably under-damped. A SAW filter consists of a piezoelectric substrate, such as quartz, lithium tantalate

An efficient signal transmission only occurs if the signal frequency f matches the resonance criteria

$$f = v_0 / \lambda$$

Thereby, v_0 is the speed of the acoustic surface wave propagation and is twice the distance between the comb structures of an IDT.

Since the available frequency bands used in telecommunications are limited, the 3G, 4G, and 5G standards use carrier aggregation to increase the data rate. That means parallel transmitting on multiple bands. To avoid interference between different bands while using them in parallel, the specifications for bandwidth have become tighter. That requires a growing precision in the manufacturing of SAW filters on wafers and an additional temperature compensation layer, which is realized by a SiO_2 coating on top of the IDT (**FIGURE 4**), which also requires superior uniformity.

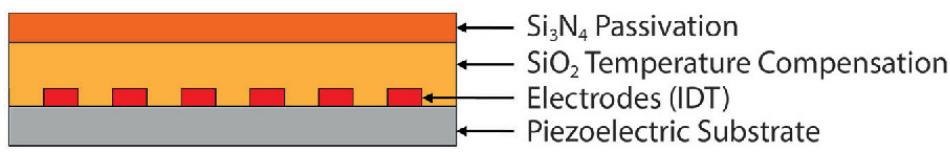


Figure 4. Scheme of a typical TC SAW stack.

(LiTaO_3), or lithium niobate (LiNbO_3), and two sets of interleaved metal electrodes called interdigital transducers (IDTs) on top of the substrate (**FIGURE 3**). Incoming electrical signals at the input transducer generate acoustic waves due to the piezoelectric effect. These waves propagate along the substrate surface and are reconverted at the second transducer.

Thickness trimming for SAW devices

A localized trimming process is necessary to improve the uniformity of SAW devices and maintain a high yield for mass production.

As with all ion beam processes, trimming occurs in a vacuum environment with working pressures from 8×10^{-5} to 8×10^{-4} mbar. A focused broad ion beam of Ar^+ ions physically etches the material from the wafer with ion current densities up to 25 mA/cm^2 . The ion beam diameter is optimized to ensure sufficient lateral resolution and high throughput. The material ablating is done by a meander-shaped pattern

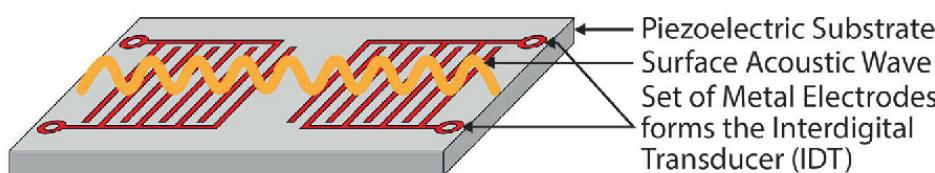


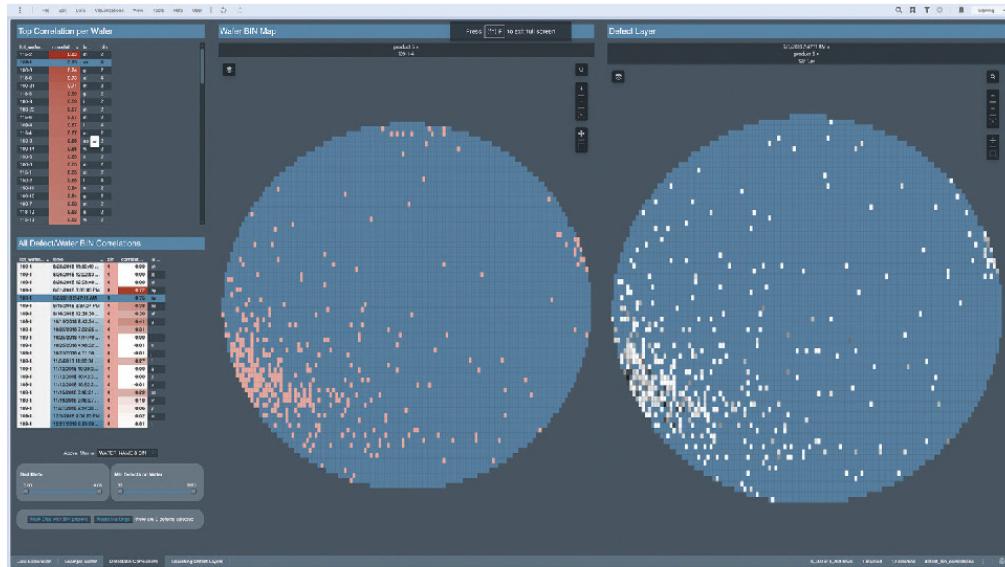
Figure 3. Scheme of a basic SAW filter design.

Unlocking the Power of Visual Data Science in High-Tech Manufacturing

High-tech manufacturing produces vast amounts of complex, heterogeneous data that often goes untapped. Traditional tools struggle to harness this data's full potential, limiting efficiency and innovation. Join our webinar, "Unlocking the Power of Visual Data Science," to discover how Spotfire empowers engineers and management to make data-driven decisions that optimize production, improve quality, and boost profitability.

Through real-world case studies, we'll explore how Spotfire drives proactive problem-solving, democratizes data, and uses AI-powered insights to unlock your manufacturing potential. No data science expertise is required—just a desire to transform operations through the power of visual data science!

Scan to register for the webinar



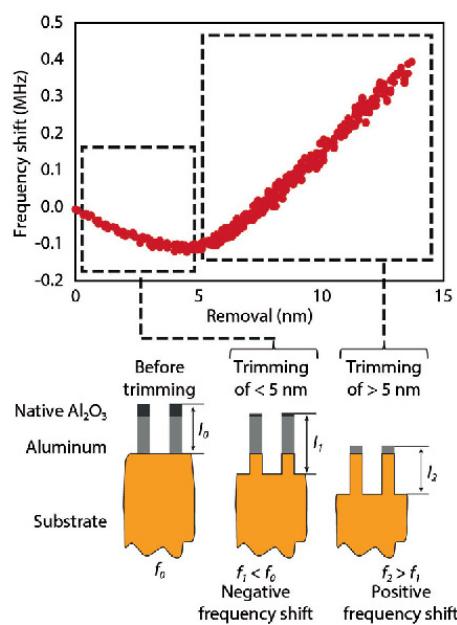


Figure 5. Frequency shift depending on the thickness change by ion beam trimming.

movement across the substrate.

The dependency between frequency shift and removal rate is determined by test etching a wedge on a test wafer. The frequency is then analyzed on the “real” substrates using an external frequency prober. The measurement data is exchanged via files and assigned to the respective substrate via unique wafer IDs. The required surface removal is determined by calculating the necessary

etching removal based on the actual and wanted frequency. The localized correction to the target dimension is carried out using an IBT process by altering the local dwell time.

In general, only an upward frequency shift is possible. Therefore, thicker layers are always applied during the preceding coating process.

Ion beam trimming of a SAW device without temperature compensation causes etching of the metal electrodes and the substrate material. The resulting sensitivity function (**FIGURES 5 and 6**) is non-monotonous, arising from the etch-rate difference of the metal electrode and the substrate. The range for a negative frequency shift can be

Guided SAW devices on POI wafers

With the evolution of the modern communication standard 5G, higher frequencies are used for receiving and sending. RF filters working at such frequencies can be manufactured as a so-called “guided SAW device.” This new class of devices utilizes a bonded piezo layer on a standard silicon wafer, called a piezo on insulator (POI). The filter device uses the same principle known from standard SAW filters.

Building a SAW device on a POI wafer involves guiding the acoustic wave within the piezo layer. This results in a higher coupling factor K2 for larger bandwidth filters and built-in tem-

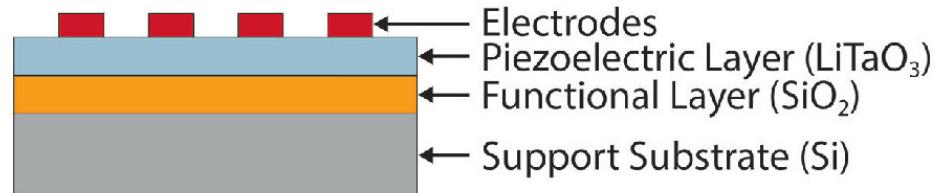


Figure 7. Schematic of a guided SAW device.

extended by adjusting the process parameters. A minimum removal is required to generate higher positive frequency shifts.

perature compensation for high band density.

Typically, POI wafers consist of two or three different functional layers (**FIGURE 7**). Each layer’s thickness must be adjusted to a specific value by keeping the surface as flat as possible. The demand for layer thickness homogeneity and target thickness accuracy becomes stricter than methods like grinding and chemical mechanical polishing (CMP) can deliver. In this case, IBT can drastically improve surface uniformity and desired target thickness accuracy. Removal up to 1 µm is addressed while maintaining low surface roughness.

FIGURE 8 shows the results of a typically trimmed POI wafer. The average thickness of 2450 nm was reduced to a target value of 1600 nm, with the standard deviation improving from 439 nm to 35 nm (13X improvement). The

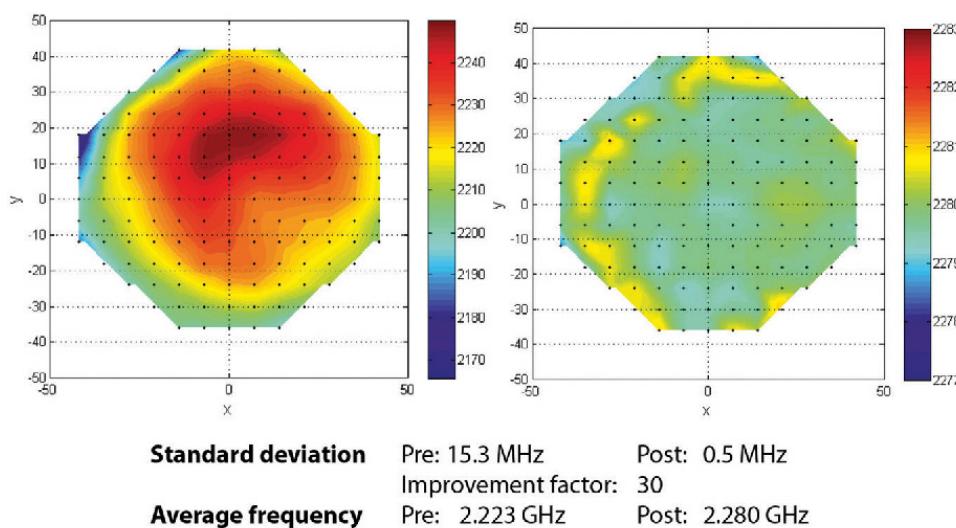


Figure 6. Pre- and post-frequency trimming of a SiO₂ temperature compensation film of a 100 mm wafer. The ion beam trimming process achieves an improvement factor of 30.

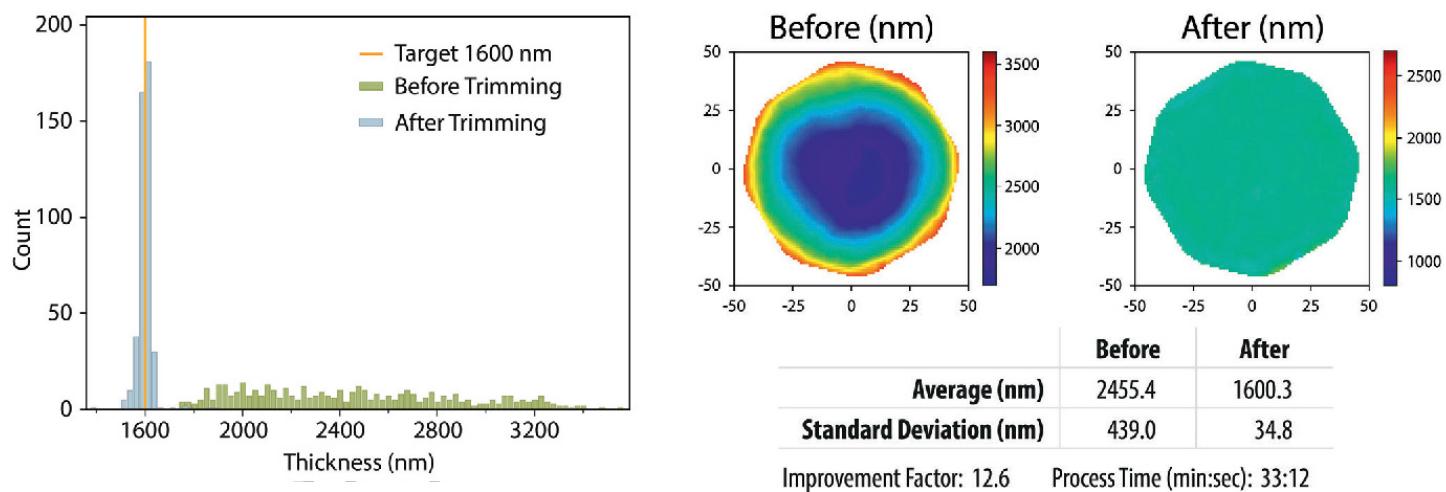


Figure 8. Histogram and height profile of 100 mm POI wafer before and after ion beam trimming. The ion beam trimming process achieves an improvement factor of 13.

thickness distribution after trimming is well centered around the target thickness.

Likewise, AFM images (**FIGURE 9**) of the wafer before and after the trimming process show that the original surface roughness was kept throughout the trimming procedure.

Bulk acoustic wave devices

Since SAW devices are used primarily at long wavelengths and lower frequency ranges of mobile communication, high-frequency filters increasingly apply the bulk acoustic wave (BAW) principle. BAW

becomes advantageous against SAW for frequencies above 2.4 GHz. The devices are tiny and have excellent performance. Furthermore, production costs have been reduced over the last few years.

A BAW filter uses a piezoelectric



REIMAGINE FAB PLANT SAFETY

Protect your most valuable assets with Guardian Equipment's integrated safety shower and pump system. The shower and eyewash deliver a flood of water to rinse away contaminants in the event of an accident. Waste water is fully captured and pumped up to overhead drain piping. The Guardian system is the first turnkey, engineered solution for protecting fab workers and the equipment around them.

Visit us at SEMICON EUROPA HALL C2 STAND 619 to see our system and learn more, visit gesafety.com or contact:

Wesley Day
Vice President | Sales

+1 603.546.8910
wday@gesafety.com



Guardian
INNOVATIVE EYEWASH & SHOWER TECHNOLOGY

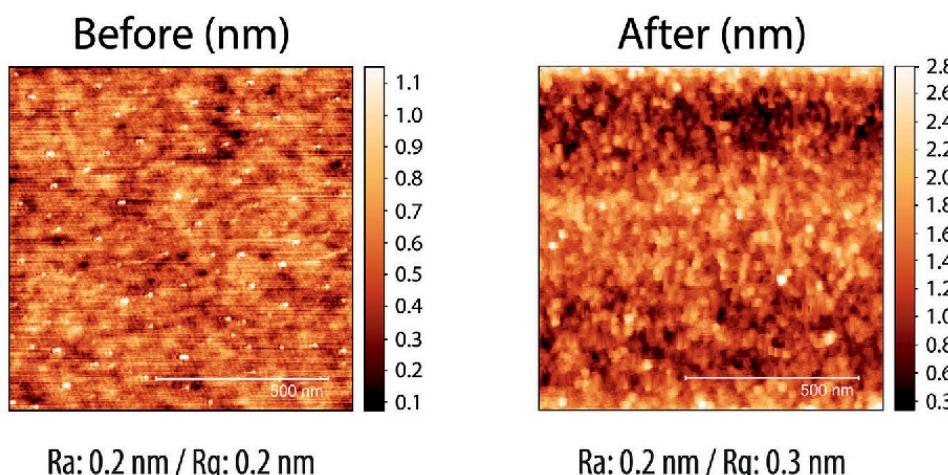


Figure 9. AFM images of a 100 mm POI wafer before and after ion beam trimming.

film commonly made of aluminum nitride, which is contacted by two electrodes. To generate an acoustic resonator, the piezoelectric film's thickness must match $\lambda/2$ of the wavelength of the longitudinal acoustic wave. That means the thickness is defined by the acoustic velocity of the piezo material and the target resonance frequency.

Additionally, the resonator needs to be acoustically isolated from the substrate. There are two different types. Film bulk acoustic resonator (FBAR) devices use a cavity between the substrate and the resonator (**FIGURE 10**). Solidly mounted resonators (SMRs), which are shown in **FIGURE 11**, use an acoustic mirror to achieve isolation from the substrate. The acoustic mirror is made of alternating $\lambda/4$ films with high and low acoustic impedance. With typical materials like silicon dioxide and tungsten, only a few layers are needed to achieve excellent isolation.

The final frequency of each device is adjusted by an additional mass load on top, which is deposited on the top electrode (e.g., silicon nitride).

The requirements for the layer uniformity of each material, especially the aluminum nitride (AlN) piezo layer, are very high. A realistic deposition homogeneity deviation of 0.5% leads to

a final device yield of only 15% to 25%.

Additional tuning steps, such as IBT, can typically improve the layer uniformities by a factor of 10 to 20. Thus, more than 90% of final device yields can be achieved (**FIGURE 12**).

IBT can be applied to each layer in the BAW stack. Thickness adjustments of the AlN piezo layer are most important because its thickness directly defines the resonance

frequency. The oscillator's mass load additionally influences the frequency. Thus, mass load trimming helps to improve yield further (**FIGURE 13**). By trimming the acoustic mirror layers, additional quality factors of the RF device can be optimized.

Trimming of XBAR components

Further device developments no longer establish entirely new functional principles but optimize existing solutions. One example is XBAR components, which are currently under development. The principle corresponds to a freely etched, guided SAW on the back. The fabrication itself is a manageable challenge. Due to the lack of backside support, shear vibrations are now excited in the arrangement. Using this principle, filtering frequencies in higher and higher GHz ranges is now possible.

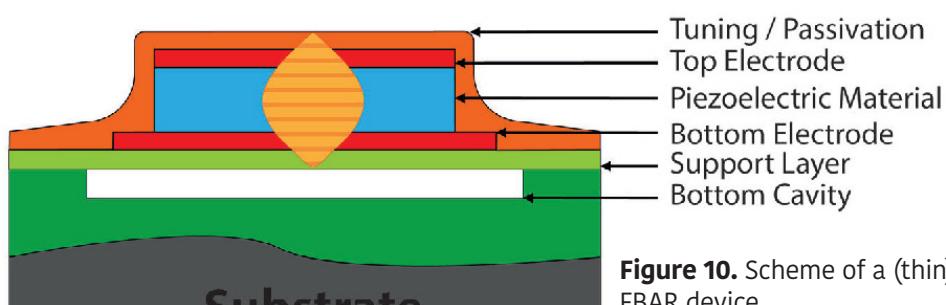


Figure 10. Scheme of a (thin) FBAR device.

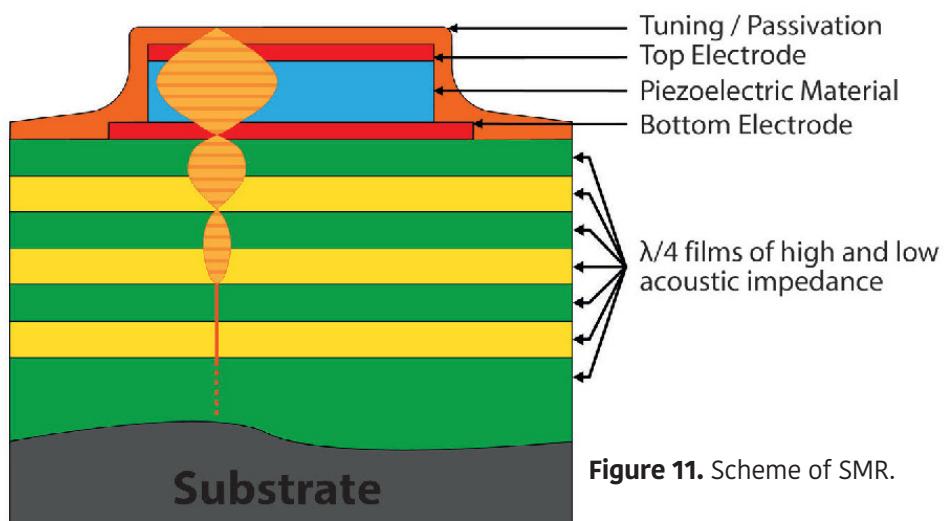


Figure 11. Scheme of SMR.

Conclusion

As mobile networks continue to evolve with the advent of 5G and beyond, the demand for advanced frequency filters will only increase. Ion beam processing technology provides an ideal approach

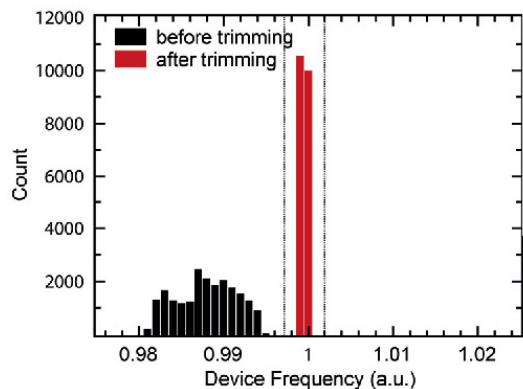


Figure 12. Improved resonance frequency due to IBT. The relative error before trimming was 0.35% and after trimming was 0.02%. This means an improvement factor of 17.

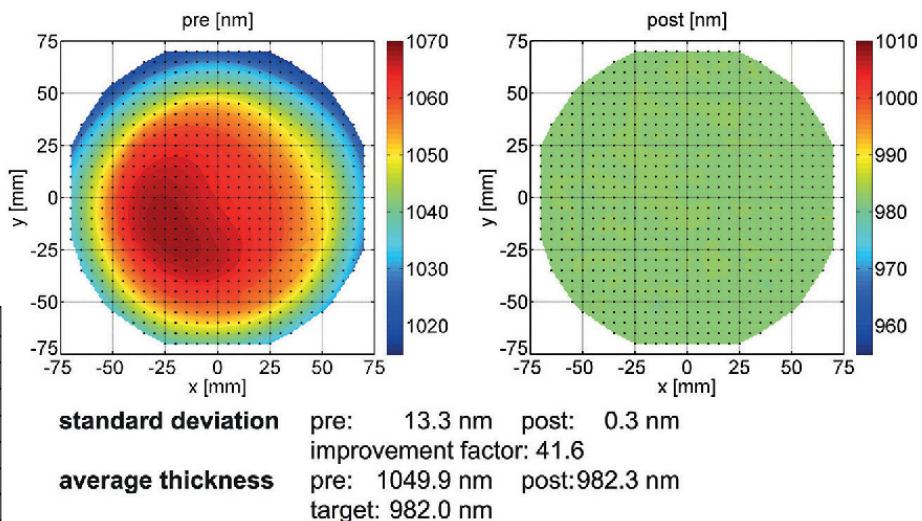


Figure 13. Pre- and post-trim results on an AlN layer for a BAW filter. An improvement factor of 41 could be achieved.

for the manufacture of high-quality high-frequency filters due to its precision and efficacy. As a result, this technology meets the stringent demands of modern communication systems, paving the way for future

innovations in the ever-evolving landscape of mobile communications. ■

About the Author

Mandy Gebhardt is head of marketing at scia Systems GmbH.



OCTOBER 7-9, 2024 | CHÂTEAU-BROMONT HOTEL | QUEBEC, CANADA

SENSORIZATION: ENABLING A NEW INTELLIGENCE

Get a deep dive on the following topics—

- Bio-Medical/MEMS Healthcare
- Generative AI
- Positioning, Navigation, and Timing
- Automotive
- Testing
- Machine Learning ML
- Sustainability (Smart Buildings, Spaces, Cities, and Agriculture)

Interconnects

Semi-damascene Metallization: Inflection Point in Back-end-of-line Processing?

ZSOLT TOKEI, imec fellow, and program director of nano-interconnects at imec

When used in combination with a patternable metal such as Ru, semi-damascene promises to be RC, area, cost and power efficient — offering an interconnect scaling path.

In 1997, THE INTRODUCTION OF CU DUAL-damascene integration schemes in the back-end-of-line (BEOL) of logic and memory chips marked an inflection point in semiconductor history. Chip makers moved away from subtractive Al patterning to wet processes like Cu electroplating and chemical mechanical polishing (CMP). This radical transition was needed to cope with an increasing RC delay in Al-based interconnects, the result of an increasing resistance-capacitance (RC) product. Being cost-effective and applicable to multiple layers of the BEOL stack, Cu dual-damascene was set to enable many subsequent generations of logic and memory technologies.

But in a few years from now, the metal pitches within the most critical BEOL layers will drop below 20nm. When that happens, Cu dual-damascene, in turn, will run out of steam. As shrinking metal line dimensions approach Cu's electron mean free path, the RC delay will increase dramatically. In addition, Cu metallization requires a barrier, a liner and a cap layer to ensure good reliability and prevent Cu from out-diffusing into the dielectric. But these extra layers start to consume a large share of the total available line width, meaning that the precious conductive area cannot be fully utilized by the interconnect metal itself. These issues force the chip industry to investigate alternative metallization

schemes with better figures of merit at tight metal pitches.

After filing an initial patent in 2017, imec presented a new metallization concept to the semiconductor community in 2020 and named it 'semi-damascene' [1]. Just like the Al-based metallization, semi-damascene integration starts with

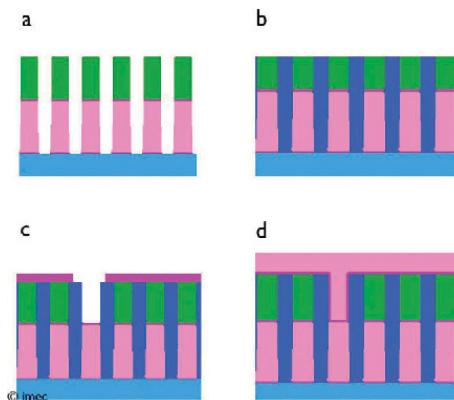


Figure 1. Schematic representation of imec's semi-damascene flow: a) Ru etch (formation of the bottom local interconnect line (M_x)); b) dielectric gap fill or airgap formation; c) via etch; and d) via fill and top line (M_{x+1}) formation (pink = Ru; blue = low-k dielectric; green = hard mask).

the direct patterning (or subtractive metallization) of the first local interconnect metal layer, hence requiring a patternable metal such as W, Mo, Ru, etc. (FIGURE 1). The via that connects with the next interconnect layer is then patterned in a single-damascene fashion: a hole etched into the dielectric is filled with metal and

overfilled – meaning that the metal deposition continues until a layer of metal is formed over the dielectric. This metal layer is subsequently masked and etched to form the second interconnect layer, with lines orthogonal to the first layer.

The value proposition of semi-damascene is promising. It can be regarded as a two-layer metallization module potentially expandable to multiple layers – making it cost effective. The subtractive etch allows for higher metal line aspect ratios (ARs) than conventional Cu interconnects, improving the resistance. As for the dielectric, the metal lines can potentially be combined with airgaps instead of low-k dielectric gap fill. Airgaps offer a lower dielectric constant, leading to smaller intra-level capacitance. Besides being RC efficient, semi-damascene also eliminates the use of metal CMP, simplifying the process flow and resulting in improved line height control. The use of refractory metals also presents benefits. They have the promise to be used without barrier layer, hence providing low via and line resistance. They are also more resistant to electromigration and overall offer lower resistance than Cu at reduced dimensions.

The industry's response: a promising but disruptive technology

Since imec introduced semi-damascene integration, multiple organizations

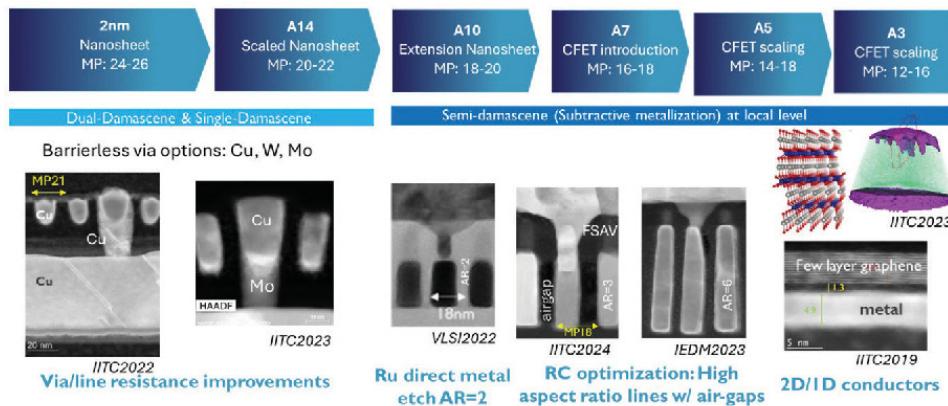


Figure 2. The imec logic roadmap.

started to research similar new schemes, and steady progress has been made through simulations and experiments [2-5]. Today, the very first step of the scheme, i.e., the subtractive etch of the first metal layer, has been successfully demonstrated and reported at conferences by multiple organizations. Experiments have clearly shown that replacing Cu with subtractively etched Ru in the first local interconnect layer can already provide a much-wanted benefit, even at a modest

line AR ~2. For subsequent generations the AR can be increased to 3 or 6 and then combine into multiple local metal layers. R&D evidence is growing that semi-damascene is indeed a valid option, offering an interconnect scaling path.

At the same time, there are question marks. Industry is currently considering moving the first generation of semi-damascene into development, the phase before actual production. As with

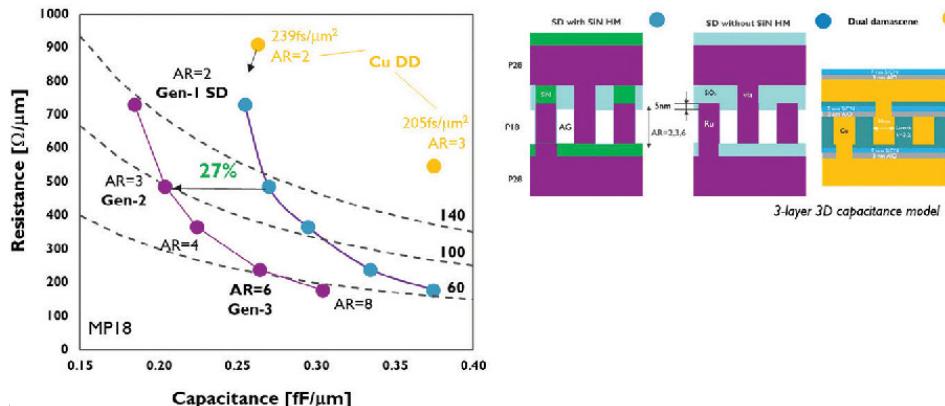


Figure 3. The imec semi-damascene roadmap, introducing subsequent generation of semi-damascene with improved RC (HM = hard mask; DD = dual-damascene; SD = semi-damascene).

SEMICON[®] EUROPA

semi™

NOV 12 – 15, 2024

MUNICH, GERMANY

→ REGISTER NOW

any new technology, industry does not proceed overnight. Semi-damascene integration disrupts the conventional technology for fabricating the BEOL. It requires new tools and materials, and perhaps some of the defect mechanisms are not captured in the research phase. Such investments are of interest only if the technology can span several technology generations. While the first step with only one metal layer is adequately documented, the implementation of a two-layer and even multi-layer integration scheme – where the capabilities and benefits of semi-damascene can be fully exploited – is however less discussed. That's why imec encourages the R&D community to open the discussion, help filling the remaining 'gaps' and share insights on multilayer integration at interconnect technology conferences.

The imec interconnect roadmap: introducing 5 generations of semi-damascene

Imec proposes to gradually introduce subsequent generations of semi-damascene. Insertion of the first generation is envisioned for the imec A10 or A7 logic technology node, where the metal pitch of the most critical interconnects becomes as tight as 18nm (**FIGURE 2**). At that point in time, GAA nanosheet integration is expected to be mainstream and CFETs will not yet be in place. Introducing semi-damascene will therefore be the only major change that chip makers will have to cope with.

Imec proposes to introduce subtractively etched Ru in M0, the first local metal layer that follows the middle of line (MOL). This first generation will come with a metal line AR 2, which is slightly higher than today's typical Cu line AR (~1.6). In combination with the favourable behaviour of barrier-less Ru at tight metal pitches, this approach will already give a resistance and reliability benefit over Cu.

In the second generation, imec aims

to increase the AR of the M0 interconnect line to 3, which will further lower the resistance, and combine the M0 with a barrierless via. As higher ARs tend to increase the intra-level capacitance, this generation needs airgaps instead of low-k dielectric gap fill. Besides offering a lower dielectric constant, working with airgaps also avoids the 'gap fill issue': the challenge of filling narrow trenches with dielectrics in a uniform way.

By adding a via and a second metal layer in semi-damascene fashion, generation three will see true semi-damascene integration of both the M0 and M2 local metal layers – the most critical layers of the BEOL. The fourth generation may see even more layers of semi-damascene. The AR will be gradually ramped up to 4, 5 and even more – depending on what will be feasible. Up to ~AR=6, when combined with airgap, sufficient RC benefit over other options is expected (**FIGURE 3**).

On the longer term, call it generation five, imec envisions alternative metals to enter the semi-damascene roadmap. Think about patternable binary or ternary compounds with better figures of merit than single metals at tight interconnect pitches.

As such, semi-damascene can become the next inflection point for BEOL fabrication. It has an excellent value proposition, not only in terms of resistance, capacitance, and area consumption. Experiments and simulations also point towards lower power consumption and better thermal properties than Cu dual-damascene schemes. At the same time, the stepwise implementation as outlined above will allow to minimize the risks always associated with the introduction of a new technology.

Enabling advanced generations of semi-damascene

While generation one and two are ready to enter the development phase,

more research is needed to demonstrate and mature the next generations of semi-damascene. The main challenges can be grouped around multi-layer semi-damascene integration, increase of the AR, and exploration of new metals for generation five.

Below is a grasp of recent progress reported by imec researchers. The results are not only meant to fill in the remaining gaps. They also aim to trigger the discussion and encourage other research institutions to complement imec's research – to the benefit of the entire ecosystem.

Towards multi-layer integration schemes in advanced interconnect As already mentioned, semi-damascene is in essence a two-metal-layer integration

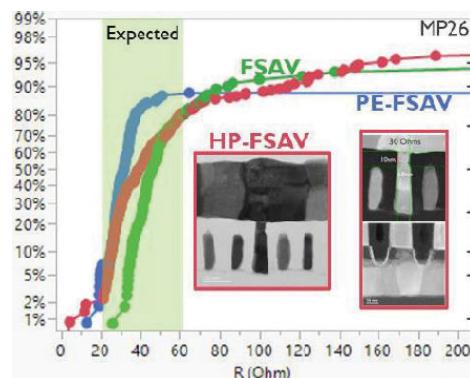


Figure 4. Via resistance distribution and cross-sectional TEMs for the three different FSAV options at 26nm metal pitch.

scheme, potentially expandable to multiple layers. But process optimizations for multilayer schemes are still in their infancy. What is the best way to implement them? Which litho and etch processes, hard masks and resists should be used? And how to integrate the vias that connect the extremely narrow interconnect lines of subsequent BEOL layers?

To address the last question, imec earlier proposed the fully self-aligned via (FSAV) as a key building block to semi-damascene [6]. FSAVs ensure a proper alignment of the lines and via (at both via top and bottom), which is

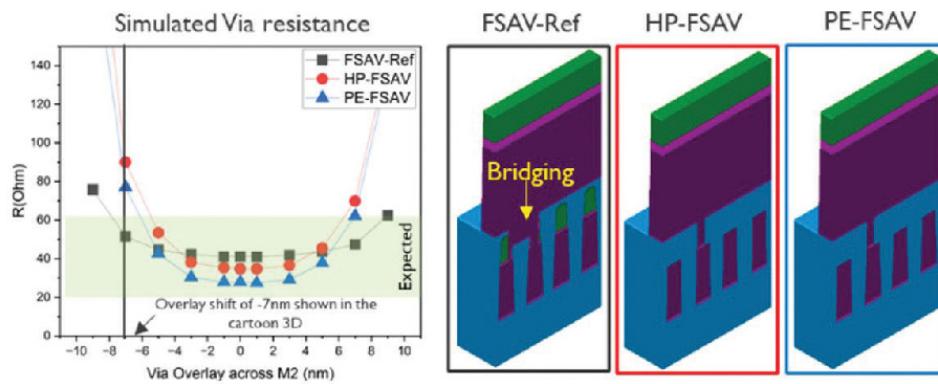


Figure 5. Via resistance distribution for overlay across the MX line, showing overlay margin. In the 3D cartoons, an overlay shift of ~7nm is shown for the three FSAV options.

crucial to enable low via-to-line leakage. So far, several integration schemes for the FSAV have been presented by multiple research organisations, including imec.

At IITC 2024, imec was the first to benchmark different FSAV integration options (**FIGURE 4**), aiming to explore how the FSAV can be best implemented in the 300mm fab [7]. In other words: how can we meet the target via resistance with optimal via-to-line overlay, and at the same time ensure low variability and good reproducibility across the 300mm wafer?

Besides the conventional single-damascene scheme (FSAV) to create the via (meaning that the via is created by etching a hole in a SiO_2 dielectric which is then filled with metal), imec explored two pillar-based FSAV integration schemes (meaning that the via is formed as a pillar by direct etch of a metal layer). The two variants are referred to as ‘hybrid pillar’ (HP-FSAV) and ‘pillar with an etch stop layer’ (PE-FSAV).

The three integration schemes differ in number of process steps, and in patterning and etch processes being used, in hard mask integration and type of resist (e.g., allowing EUV lithography tone inversion for enabling the pillars). But for all three cases, the feasibility of reaching target via resistance and via-to-line overlay margin was showcased (**FIGURE 5**). The most notable difference is related to the resistance uniformity achieved across the wafer. All integration schemes provide sufficient via litho and etch process windows. Therefore, they are compatible with the direct metal etching equipment currently available through our tool suppliers. Other work by imec shows that the self-aligned window also exists for implementing airgaps, which will be needed to continue the capacitance benefit when line ARs increase further [8].

The status today hence proves that technically viable options are available to implement at least two layers of semi-damascene. At the same time the number of wafers

demonstrated is limited. Hence, imec encourages other organizations to complement the puzzle, and let the industry ecosystem ‘decide’ on the best option forward.

Incrementally increasing the aspect ratio of semi-damascene lines: understanding and mitigating the roadblocks

A continued decrease of the resistance of Ru semi-damascene lines is possible by further increasing their AR. In 2022, imec showed first evidence that implementing semi-damascene with AR 6 (**FIGURE**

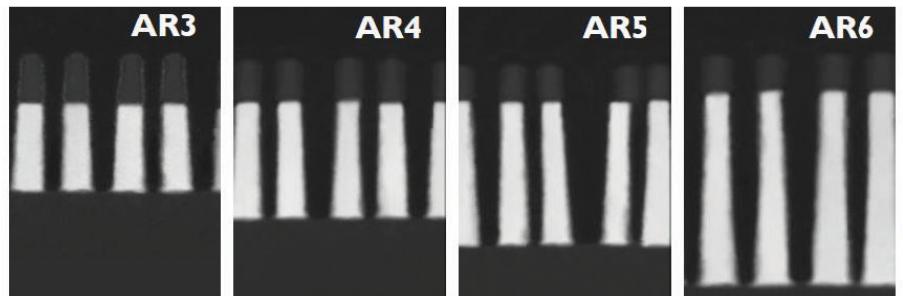


Figure 6. Towards higher AR metal lines.

efficient.

Simple replacement of Kr+ gas laser



TopWave 405 – 1 Watt @ 405 nm

High coherence diode laser for lithography and holography

- Low cost of operation
- 1 Watt @ 405 nm
- Excellent beam quality, typical $M^2 = 1.15$




6) can indeed substantially improve the RC metric over lower AR schemes [9]. Shortly after, initial experiments indicated that high-AR lines are also compatible with multilayer schemes [10].

While the formation of interconnect lines with modest ARs (2 and 3) is relatively well understood, increasing the AR while preserving good line resistance and reliability requires some technical mastery. It has shown to challenge almost every process step – including patterning and etch, cleaning, and defect control. For example, the direct metal etch ‘attacks’ the sidewalls of the Ru lines, leading to line-break defects. And this worsens with increasing AR. Obtaining the lowest possible line resistance necessitates a more fundamental understanding of the high-AR line formation and reliability.

As a first important insight, researchers at imec found that the composition of the stack used to form the high-AR metal lines strongly influences the resistance of the semi-damascene lines. Line break defectivity was shown to be the main contributor to the stack-dependent device performance. Imec, through multiple experiments, found an optimal stack, which starts with depositing 1nm TiN for improved adhesion, followed by physical vapor deposited (PVD) Ru. Compared to other compositions used in the study, this stack offered the lowest resistance over the entire height of the metal line. Second, the study provided a first indication that the line defectivity is influenced by the grain structure and crystal orientation of the Ru metal grains. These morphological parameters strongly depend on the method used for depositing Ru, favoring the use of PVD. [11]

Besides gaining insights in the parameters affecting the Ru line resistance, imec recently came up with a unique approach to further improve the high-AR lines from resistance and uniformity point of view: sandwiching a sub-nm TiN or W layer between two Ru layers. This stack was found to be less prone to

lateral attack and line-break formation during direct metal etch compared to stacks without this extra layer. The key benefit of this ‘defect mitigation layer’ is that it enables low-defectivity lines of high AR and long lengths, which is a promising result towards $\text{AR} \geq 6$ Ru semi-damascene. The results were presented at the 2024 VLSI Symposium [12]. The experimental work showed good reliability behavior of lines down to 24nm pitch (**FIGURE 7**). But, at the same time more work is needed to optimize and extend the results towards 18nm pitch, show compatibility with integrating airgaps and demonstrate sufficient time-dependent dielectric breakdown (TDDB) and mechanical reliability margin.

Advanced interconnects: the quest for alternative conductors The work on semi-damascene integration so far focused on using Ru as the conductor of choice. Several years ago, imec began investigating whether there are other metals with even better prospects. The search expanded from elemental metals towards binary and ternary ordered compounds [13]. After a promising preliminary study, several R&D groups worldwide started to embrace the idea and joined the search for candidate alloys. The community recently gathered at the VLSI 2024 thematic workshop on ‘Novel metals for advanced interconnects’. This workshop was organized by imec to discuss the state of the art and future research directions – from both industrial and academic perspective.

Since the list of potential alloys is enormous, imec started its investigation with setting up a unique methodology for down-selecting and ranking the possible candidates. Two figures of merit were

identified for benchmarking against Cu: the compound’s cohesive energy and the product of the bulk resistivity and the mean free path of the carriers. Ab-initio simulations revealed a sub-list of candidates, including for example intermetallic aluminides, the starting point for further experimental work.

Today, research groups worldwide investigate how the resistivity of these candidate alloys behaves at reduced dimensions. For example, when intermetallic aluminides are deposited in thin films, defect mechanisms involved in thin film formation seem to affect the resistivity behavior (**FIGURE 8**). Understanding that correlation will be key to control the resistance. Imec also identified global and local composition control as an important knob towards minimizing the resistance. [14]

Once ways are found to optimize the resistance of promising binary and ternary alloys, the next step is to implement them in relevant metallization schemes and address the challenges

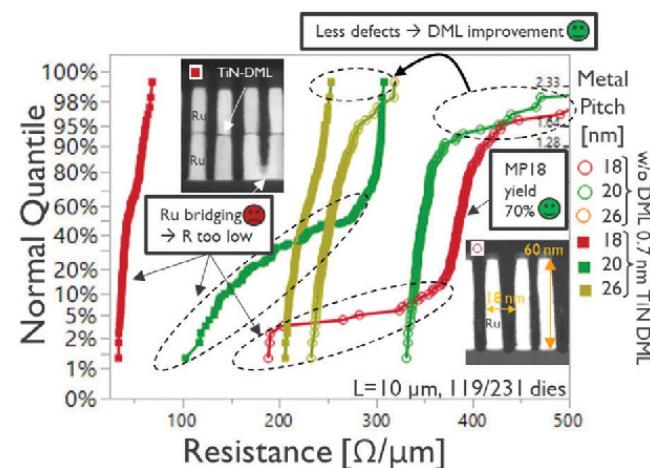


Figure 7. Resistance yield of AR 6 lines at various metal pitches (18–26nm) for cases with and without defect mitigation layer (DML).

related to semi-damascene processing. Imec encourages universities and research groups to collaboratively explore patterning and etch strategies and set up process directions. Although much work remains to be done, research into alternative metals is a promising avenue, and steady progress is being

made. Intense collaborations will yet be needed to eventually introduce them into generation five of semi-damascene integration.

Conclusion

Semi-damascene metallization may become the next inflection point in BEOL fabrication, with industry currently debating about introducing subtractive etch in the first local interconnect layer. Although not even the first generation of semi-damascene is in production today, based on experimental evidence, imec is already looking ahead to newer generations of semi-damascene. The focus is on multiple metal layers and vias, a step-by-step increase of the aspect ratios, and the introduction of new metals. For these next generations to become a reality, joint efforts and more data are needed with strong input from academia and industry. 

REFERENCES

1. 'Semidamascene interconnects for 2nm node and beyond,' G. Murdoch et al., IEEE IITC 2020;
2. 'Subtractive Ru Interconnect Enabled by Novel Patterning Solution for EUV Double Patterning and Top Via with Embedded Airgap Integration for Post Cu Interconnect Scaling,' C. Penny et al., IEDM 2022;
3. 'Airgap Integration on Patterned Metal Lines for Advanced Interconnect Performance Scaling,' H.K. Chang et al., IEEE IITC 2023;
4. 'A Novel Integration Scheme for Self-Aligned Ru Top via as Post-Cu Alternative Metal Interconnects,' K. Motoyama et al., IEEE IITC 2023;
5. 'A Study of Resistivity Control for Subtractive Interconnects Using Ruthenium,' J. Rogers et al., IEEE IITC 2023;
6. 'First demonstration of two metal level semi-damascene interconnects with fully self-aligned vias at 18MP,' G. Murdoch et al., VLSI 2022;
7. 'Redefining 2-level semi-damascene interconnect technology: benchmarking three different fully self-aligned via options,' G. Marti et al., IEEE IITC 2024;
8. 'Airgap integration in MP18 two-level semi-damascene interconnects with fully self-aligned vias,' G. Delie et al., IEEE IITC 2024;
9. 'MP18-26 Ru direct-etch integration development with leakage improvement and increased aspect ratio,' A. Pokhrel et al., IEEE IITC 2022;
10. 'Two-metal-level semi-damascene interconnect at metal pitch 18nm and aspect-ratio 6 routed using fully self-aligned via,' A. Gupta et al., IEDM 2023;
11. 'Impact of Ru deposition method and adhesion layer on electrical performance of semi-damascene interconnects,' G. Delie et al., SSDM 2023;
12. 'Mitigating line-break defectivity with a sandwiched TiN or W layer for metal pitch 18nm aspect ratio 6 semi-damascene interconnects,' A. Gupta et al., VLSI 2024;
13. 'Alternative metals: from ab initio screening to calibrated narrow line model,' C. Adelmann et al., IEEE IITC 2018;
14. 'Optimizations on resistivity of binary compounds for advanced interconnect metallization,' J.-P. Soulié, SSDM 2023.

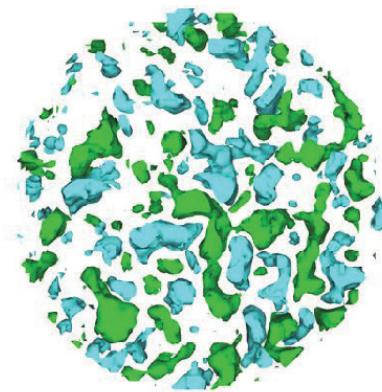
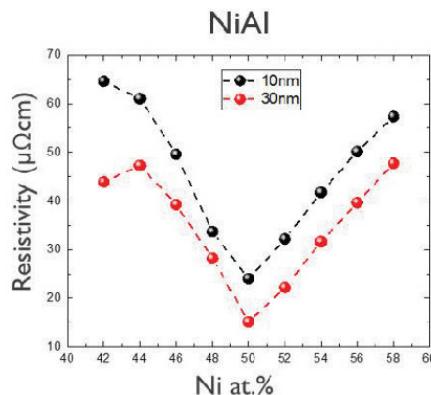


Figure 8. Example of the challenge posed by local composition control in intermetallic aluminides. The atom probe tomography measurement (right) shows local composition fluctuations (blue = Al; green = Ni), affecting the resistivity (left).

About the author

Zsolt Tokei is imec fellow, and program director of nano-interconnects at imec. He joined imec in 1999 and, since then, has held various technical positions in the organization. He is working on a range of interconnect issues, including scaling, metallization, electrical characterization, module integration, reliability, and system aspects.



SEMICONDUCTOR HEATING ELEMENTS

Thermcraft has been supplying high quality diffusion furnace heating elements to the semiconductor industry since 1976. Our high-performance elements are designed for the most demanding processes. Whether used in annealing silicon wafers, silicon doping, or other semiconductor applications, we will provide a custom engineered solution to meet your needs.



How Silicon Carbide Semiconductors Are Conquering E-mobility

Bosch has tailored its semiconductor development to the demands of the automotive industry.

POWER ELECTRONICS ARE AT THE HEART OF many electronic systems in battery-electric vehicles. Here, semiconductors manage the energy and ensure that it is utilized as efficiently as

The semiconductor manufacturer and automotive expert Bosch has an optimistic outlook on the future of silicon carbide.

Silicon carbide belongs to a class of materials known as wide bandgap

can block higher voltages with lower on-state resistances, making them ideal for the high-voltage range. In addition, the improved temperature stability ensures that the semiconductor retains its performance even at temperatures of up to almost 400 degrees Fahrenheit. Another key advantage of SiC is its higher charge carrier mobility, which enables significantly higher switching frequencies compared to conventional silicon-based solutions. Together, these benefits lead to improved overall efficiency.

Why SiC is worthwhile

The main benefits of silicon carbide vary depending on which vehicle components the chips are used in. In electric vehicles, SiC primarily enhances power electronics, especially the inverter, the



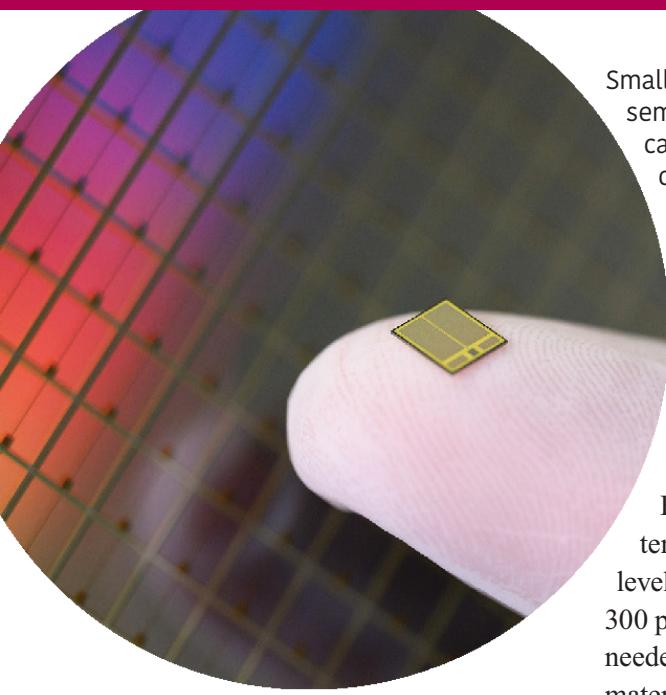
Silicon carbide semiconductors in on-board chargers ensure more efficient charging and lighter systems.

possible. MOSFETs (metal-oxide-semiconductor field-effect transistors) made of silicon carbide (SiC) are renowned for taking electromobility to new levels of efficiency. While semiconductor technology is already widely used in some areas, its application is still in its early stages in certain automotive applications.

semiconductors. This wider bandgap offers several advantages over silicon: thanks to the higher breakdown field strength, these special semiconductors

Bosch is systematically expanding its manufacturing capacity for silicon carbide chips over the next few years.





Small chip with a big impact: semiconductors made of silicon carbide have clear advantages over conventional semiconductors in many applications.

Silicon carbide semiconductors are more expensive than comparable silicon components. The production of silicon carbide boules requires very high temperatures – around 3,600 degrees Fahrenheit – and over ten mask or structure levels with more than 300 process steps are needed before the raw material turns into a chip. As a result, the use of silicon carbide generally follows a careful cost-benefit calculation.

Inverters based on silicon carbide technology are therefore currently found primarily in high-performance vehicles, where the benefits of SiC semiconductors are most obvious. “In smaller

DC/DC converter, and the on-board charger. The use of SiC in the inverter enables higher efficiency, which increases the driving range.

SiC MOSFETs have higher switching transients than Si-IGBTs, allowing for quicker switching speeds. By increasing the switching speed, the overall switching loss is reduced by around 50 percent. Additionally, SiC technology enables higher switching frequencies, reaching up to 24 kHz.

The capability significantly benefits DC/DC converters and on-board chargers by enabling more compact and lightweight systems with improved efficiency. Inverters equipped with SiC semiconductors enhance the overall efficiency of electric drives, reducing electrical consumption (kWh per 100 km) in conjunction with other improvements in the overall system. This increases the range of electric vehicles or, in other words, allows the battery capacity to be optimized based on the vehicle class and application to save costs.

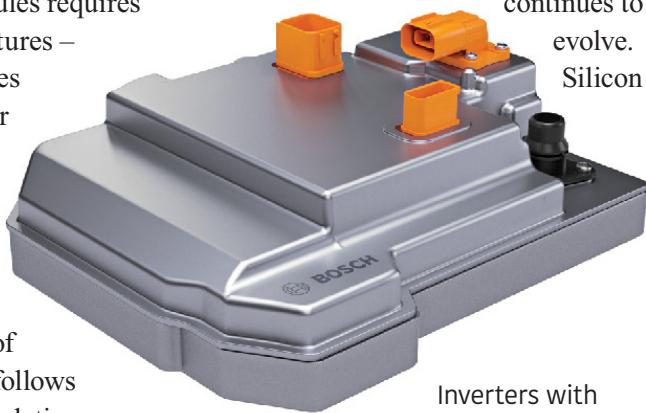
SiC chips are conquering the market

Despite their numerous advantages, not all electric cars currently contain silicon carbide chips. One reason is that SiC

the disadvantages,” explains Anne Bedacht, Head of Product Management for Power Semiconductors at Bosch.

For her, efficient e-mobility is therefore closely linked to SiC: “If you look at the progress made in both SiC and electric vehicles over the last ten to fifteen years, it’s undeniable and

continues to evolve. Silicon

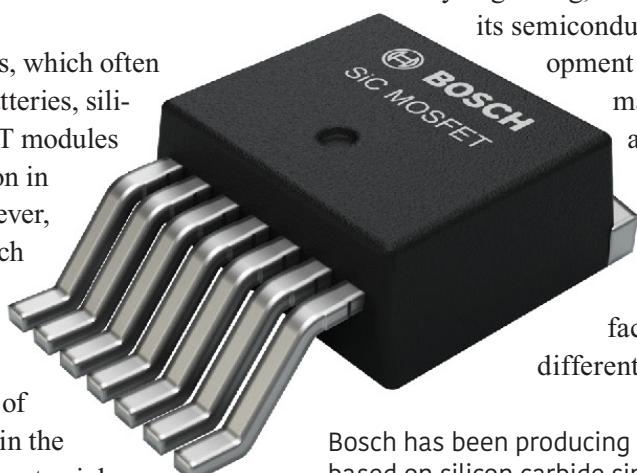


Inverters with silicon carbide semiconductors show their advantages particularly in the high-voltage range.



The Bosch power module with silicon carbide semiconductors offers high power density.

electric vehicles, which often use 400-volt batteries, silicon-based IGBT modules are still common in inverters. However, in vehicles which are based on 800-volt technology, the advantages of silicon carbide in the inverter clearly outweigh



carbide chips have been conquering the market for several years, starting with the most profitable applications. As production scales up, the cost of these chips will eventually decrease – making their use increasingly worthwhile across more vehicle components and models.”

Designed for electric driving

Bosch was an early adopter of SiC technology. The company began developing the first SiC semiconductors in 2001 and had the first MOSFET prototype available by 2011. From the very beginning, Bosch tailored its semiconductor develop-

ment to the demands of the automotive industry.

“Semiconductors in vehicles face entirely different conditions

Bosch has been producing MOSFETs based on silicon carbide since 2001.



Bosch's wafer fab in Roseville, California: starting in 2026, the first silicon carbide chips will be produced in the United States on 200-millimeter wafers.

compared to stationary applications," explains Bedacht. "For example, the temperature fluctuations that a car is exposed to put significant strain on the electronics. In addition, we must deal with higher quality requirements. A car is in use for many years, and the semiconductor's lifespan must keep pace. Our chip designs reflect these demands."

One example is the design of the gate oxide in the trench MOSFET. Bosch has developed its own manufacturing process for SiC chips, adapting Bosch's own trench etching technique. This process, commonly referred to in the industry as the "Bosch process", was originally developed in 1994 for MEMS sensors. It enables high-precision vertical structures to be etched into the wafer material. Unlike the conventional planar structure, the gate is vertical. The insulating oxide not only covers the surface of the chip but also protrudes into it. "This structure ensures higher power density while guaranteeing a long service life. This is important because the component will be exposed to high voltage for many cumulative hours in the vehicle over the years," the semiconductor expert reports.

The future is all about SiC for Bosch

Bosch has positioned itself broadly in the automotive industry and offers SiC MOSFETS in multiple forms. The company sells bare dies and discretes directly to OEMs, to tier 1 and 2 suppliers and to distributors, while also implementing them in its own modules and components. From Bosch's point of view, the two sales channels are by no means contradictory, as Bedacht explains: "On the contrary, both customer groups benefit from our broad experience in the automotive industry. Many customers have long relied on their own designs and systems for greater differentiation, and we aim to support these OEMs and tiers just as much as those who use complete modules and components that include our SiC semiconductors."

For Bosch, the future is clearly centered around SiC. The company is systematically expanding its production capacities – both at its



Anne Bedacht, product manager for silicon carbide semiconductors at Bosch.

existing production facility in Reutlingen, where mass production of SiC chips began in 2021, and at the new wafer fab in Roseville, California, which is currently being converted to silicon carbide. In Reutlingen, Bosch is already producing samples of its first silicon carbide chips on 200-millimeter wafers for customer trials. The delivery volume is expected to increase more than tenfold in the coming years.* With the new fab in Roseville, Bosch will reinforce its global portfolio of SiC chips. Starting in 2026, the first silicon carbide chips will be produced in

the United States on 200-millimeter wafers. "The automotive industry is a key player in driving the technology forward," summarizes Bedacht. "With high production volumes, we will achieve economies of scale, which will reduce costs over time and extend

the benefits of silicon carbide to other applications." sD

**The IPCEI ME/CT project is supported by the German Federal Ministry for Economic Affairs and Climate Action on the basis of a decision by the German Parliament, by the Ministry for Economic Affairs, Labor and Tourism of Baden-Wuerttemberg based on a decision of the State Parliament of Baden-Wuerttemberg, the Free State of Saxony on the basis of the budget adopted by the Saxon State Parliament, the Bavarian State Ministry for Economic Affairs, Regional Development and Energy, and funded by the European Union — NextGenerationEU.*

Factory Integration

Selecting an MES Migration Strategy for Semiconductor Process Optimization

TOM BEDNARZ, Sales Manager Tech Europe, Critical Manufacturing

Migrating to a new MES platform can lower the total cost of ownership of automation and production assets, increase efficiency, revenue, and ultimately, profitability, safety and environmental sustainability.

If you have been running a semiconductor manufacturing execution system (MES) for more than 10 years, you already know well the value of integrated, automated operations. And you likely know also that MES and automation technologies have advanced significantly over the past decade. Maintaining or enhancing those benefits may require migrating to a more modern system. There is, however, more than one way to approach migration, and getting the maximum return on your investment depends on selecting the strategy best suited for your processes, your business and your tolerance for risk. Here are some important things to consider to make your migration a success.

Why migrate?

Migrating to a new MES platform can lower the total cost of ownership of automation and production assets, increase efficiency, revenue, and ultimately, profitability, safety and environmental sustainability.

If your software is at the end of its life and the vendor is phasing out support, you will have little choice but to migrate to a new platform. But even if your ten-year-old system is not on its last legs, there are still major benefits to migrating to a modern system. You can get your legacy functionality in a more

robust, cost-efficient platform while also setting yourself up for valuable new capabilities. Here are just some of the MES-enabling capabilities that have matured within the past decade:

- Integration with plant devices via IIoT

- Streamlined integration with enterprise applications, such as ERP, SCM and PLM.
- Advanced machine learning and AI
- Advanced simulation and modeling, digital twins
- Personalization and customization



Table 1. Tradeoffs in common MES migration strategies

	BIG BANG	PHASED-IN	PARALLEL
RISK	High	Medium	Low
EXECUTION TIME	Fastest	Longest	Medium
COST/EFFORT	Lowest	High	Highest

- Flexibility and scalability
- Advanced user interface
- Automated regulatory compliance
- Cybersecurity

Migration options

Whether you get maximum benefit from your migration depends in part on choosing the migration strategy that is most compatible with your needs. This usually involves making a strategic choice either to migrate everything at once, in phases based on production priorities or in parallel.

Total “big bang” replacement model, often called the big bang or rip-and-replace strategy involves disconnecting the legacy system and replacing it with the new one. After preparation and testing, the migration team switches the old system off and the new one on. During the migration, the new MES and master data GUI will sit alongside the operations GUI. They connect to the ERP, to other applications and to a reporting and analytics dataset. Synchronizing the legacy data will usually require application downtime, file change configurations, and application startup procedures. Application migration and process equipment integration happen after synchronizing the operations data.

Phased in migration strategy

The phased in strategy involves implementing new MES modules by manufacturing operating units, MES functions or lots.

Phasing in by *operating unit* involves introducing functional units slowly, and within this option, there are at least also three approaches: phasing in *area-by-area*, *process step by step*, or *machine by machine*, as needed. Regardless of which strategy you choose, the new and old applications must be able to work interchangeably



with each other so that you can share and exchange data.

Phasing in by *MES function*, such as SPC, recipe management or maintenance management, requires co-existence between the legacy and new MES, but functional responsibilities would never overlap. And phasing in by *lot* might involve upgrading all the modules for the target product, running some on the new platform and some on the old.

Parallel Strategy While the above phased-in approach may have some phases running together, they would not typically run the same operations. In a *parallel* migration strategy, however, both systems would be configured to run simultaneously and completely, with the legacy system running as the master and the new one as the slave. Data sits

in both systems at the same time until the new one passes readiness tests and becomes master, and you switch the legacy system off.

Managing the trade-offs

Each strategy has its tradeoffs though, and which migration approach is best for you depends on how you manage tradeoffs among speed of implementation, cost and risk. If, for example, demand for your products is high, you might optimize for speed-to-market more so than cost control but if you have excess unused production capacity or inventory, cost cutting may be a more strategic immediate priority.

If you are migrating from spreadsheets or from a standalone system that is not heavily integrated with your legacy operations, the big bang approach is likely your best and probably only option. It is also the fastest and lowest cost approach because you don't have to deploy resources to implement the crossovers.

If your legacy MES is integrated into the rest of your enterprise or incorporated into existing automation sequences, and you want to optimize for speed and cost, a big bang approach could be good for you as well, but it does come with high risk. There is, for example, no easy way to test the integration with real production data and rolling back to previous functionality is also challenging.

You can reduce that risk by going with a phased-in or parallel approach. With a phased in approach, confidence and expertise grow steadily as you complete each phase and because each phase is a mini migration unto itself, you have more leeway to roll things back before moving on to the next phase. This is especially true with the parallel strategy, where you have virtually unlimited opportunities to



roll back before switching over to the new systems. But all this learning and rolling back takes time and resources, so these approaches will extend completion time and increase costs.

Planning and implementation

The strategy that best matches your needs, optimizing for cost, speed, and risk reduction, depends on a thorough upfront planning process, where you structure the definition, preparation, execution, and closure of your project.

In the *definition* stage you set the project scope, target and execution strategy, this is where you would commit to a big bang, phased parallel approach. Next, during the *preparation* phase you acquire and install and configure system hardware and other applications and set up development, staging and production environments. This is also where you configure, model and customize the new MES modules, train users, and adapt the related applications and utilities needed to support

the migration.

The *execution* phase then covers all the activities to bring the migration to life. It assumes that you have reconciled downtime with production needs. It includes the roll-out and go live, performance monitoring, phase-in and phase-out of manufacturing processes and ultimately, shutdown and removal of the legacy system. The *closure* phase covers all post-migration close-down activities, such as archiving legacy data and decommissioning unnecessary hardware. It may or may not include activities necessary to activate new functionality from the new MES system.

Adaptable MES

It is quite possible that this may be the last full-scale migration you will ever do. Given the increasing adoption of interoperability standards and software development advancements tailoring to accommodate changing market dynamics could be simply a matter of

swapping out or adding modules.

One note of caution – regardless of which strategy you choose, you may be tempted along the way to add some custom touches maybe to preserve some legacy functionality. This could, however, be a recipe for disaster. Whether you implement it via big bang, phased-in, or parallel, the integrity of the new product must be preserved. You risk not only compatibility issues down the road, but also missing out on new functionality that could optimize your processes in ways you hadn't imagined.

Having taken the time to select the migration strategy that best fits your business strategy, and clearly articulated objectives, however, will help in both the short and the long term.

For more guidelines on planning and implementing your migration see our white paper Guide to Successful MES Replacement. <https://www.criticalmanufacturing.com/insights/white-papers/guide-to-successful-mes-replacement/>

Water Treatment

Maximizing the Value of Wastewater Generated During Semiconductor Fabrication

ZHAOHUI YAN, Global Market Segment Lead for Microelectronics at DuPont Water Solutions

The semiconductor aims to reduce pollutants and freshwater consumption, reuse water, and recycle resources.

WATER IS FUNDAMENTAL IN THE manufacture of microelectronics, with large volumes of water required at every stage of the fabrication process. As one of the world's most water-intensive industries, it is understandable why it is in the

spotlight as water scarcity becomes an increasingly pressing issue. In addition to sustainability considerations, water stress can increase operating costs for foundries as they compete with local communities for local resources, plus it may expose them to reputational,

regulatory, and litigation risks.

"In the midst of increasing regional water scarcity and raw material costs, we're seeing end-users increase their reclamation of wastewater for reuse back into their process streams—and recycling other valuable resources



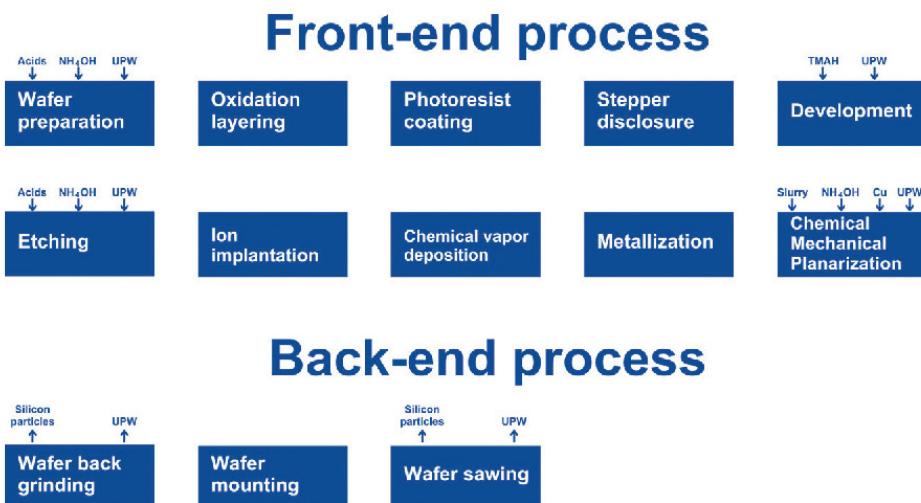


Figure 1.

through minimum or zero liquid discharge strategies,” said Veronica Garcia Molina, Global Marketing Leader, Industrial Water & Energy at DuPont Water Solutions. “We’re seeing a shift from reuse being viewed as aspirational to something that is now necessary.”

The semiconductor industry is undergoing an evolutionary shift from simply striving to meet increasingly stringent regulatory requirements on discharge, to reusing wastewater, and

is now embracing the reclamation of resources from wastewater as part of the treatment processes that enable reuse. This shift reflects the general principle of 3Rs; reducing pollutants and freshwater consumption, reusing water, and recycling resources.

The scale of the challenge

Producing a typical 12-inch wafer will generate around 10 m³ of wastewater containing valuable minerals, including

approximately 3.5 Kg NH4+, 1.0 Kg TMAH, 50 g valuable metals, and 100 g of silicon particles. This wastewater is generated during many different front and back-end process stages, with its composition varying greatly, requiring different treatment approaches for maximum efficiency (**FIGURE 1**).

For example, TSMC classifies its process wastewater [1] into 38 types according to their composition and concentration of specific compounds (**FIGURE 2**). Low-concentration wastewater most suitable for reuse is divided into three categories which directed wastewater streams for treatment by nine recycling systems.

Treatment Technologies: The wide world of membrane filtration and ion exchange resins

Membrane filtration is a flexible and proven method for the concentration of liquids and separation of materials. This technological approach is often faster and easier to manage than energy-intensive centrifugal separation or evaporation solutions. The precise

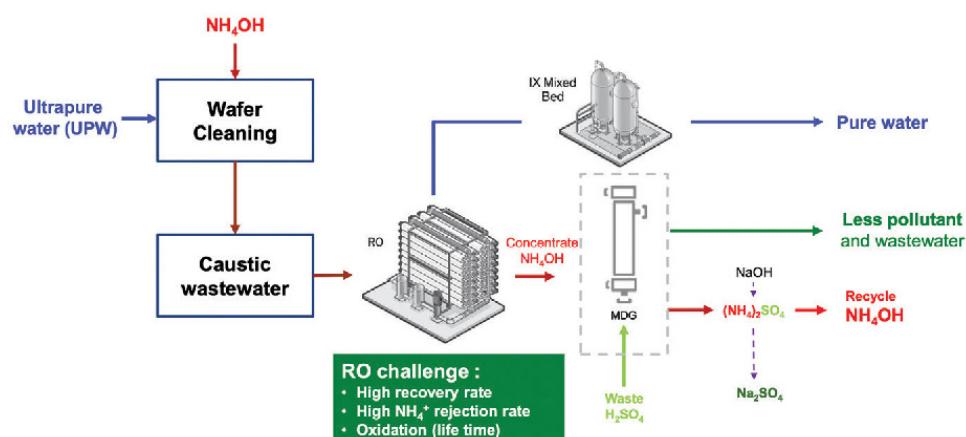
Wastewater Categories

TSMC classifies process wastewater into 38 types according to their composition and concentration of specific compounds. The low-concentration wastewater which can be reused is divided into 3 categories and 9 recycling systems.

Acidic, alkali, and organic wastewater	Deionized Water Ozone-containing deionized water Acidic wastewater (two types)	Ozone-containing acidic wastewater Caustic wastewater (CWD) Ozone-containing caustic wastewater	TMAH wastewater Organic wastewater (two types)
Hydrofluoric (HF) Acid Wastewater	HF acid wastewater (2 types) Ozone-containing HF acid wastewater Manufacturing process scrubbing water (LSD)		
CMP Wastewater	CMP wastewater (2 types) Cu-containing CMP wastewater Co-containing CMP wastewater	Electroplating wastewater	
High-concentration liquid waste	Waste sulfuric acid Waste copper sulfate Co-containing liquid	Other wastewater (16 types)	

Figure 2.

CLASS	PORE SIZE	EXAMPLE APPLICATIONS
Reverse Osmosis (RO)	< 0.001 µm	<ul style="list-style-type: none"> Concentration of NH₄⁺ from the CWD and HFD streams Reduction of total dissolved solids (TDS)
Ultrafiltration (UF)	0.01 – 0.1 µm	<ul style="list-style-type: none"> Recovery of fine silica particles following back-grinding or chemical mechanical polishing Removal of small biological contaminants, including viruses, colloids, proteins, and macromolecules.

**Figure 3.**

nature of the separation is determined by the membrane's chemistry:

- semi-permeable membranes rely on a combination of size exclusion and solution/diffusion permeation to achieve separation.
- microporous membranes can be used to separate targeted components from a feed stream dependent on pressure and the target molecular weight.

It is certainly not a case of one size fits all; there is a huge variety of membranes available on the market, developed for different industries, applications, and treatment approaches. The different grades and properties of these membranes determine not just their efficiency and performance characteristics, but also their resistance to fouling.

There are two different classes of membranes that are commonly used for wastewater treatment and the reclamation of resources in the microelectronics industry (Table 1).

Meanwhile, ion exchange resins (IERs) are polymers with charged functional groups that can be used for the selective removal or exchange of ions in a liquid solution. There are two types

of IER; negatively charged cation resins and positively charged anion resins. These respectively attract and exchange positive and negatively charged ions.

IERs can be used as a pre-treatment to remove hardness traces, protecting and increasing the recovery of downstream RO units, or for the recovery of minerals including tetramethylammonium hydroxide (TMAH) and copper (Cu).

Recycling valuable by-products as part of the wastewater treatment process

Membranes and IERs can be combined in multi-tech solutions for the recovery of various valuable by-products contained within wastewater streams, allowing for their sale to material processors for recycling.

Ammonia A combination of ultrapure water (UPW) and ammonium hydroxide (NH₄OH) is used for wafer cleaning, and the resulting caustic wastewater is unsuitable for discharge without treatment. The concentrated NH₄OH produced after treatment by RO can be combined with other waste

streams to allow for the reclamation of ammonia and associated by-products. Meanwhile, the water purified during the RO process can be demineralized by an IX mixed-bed to produce pre-UPW quality water for reuse (**FIGURE 3**).

Key considerations in specifying RO membranes for this application:

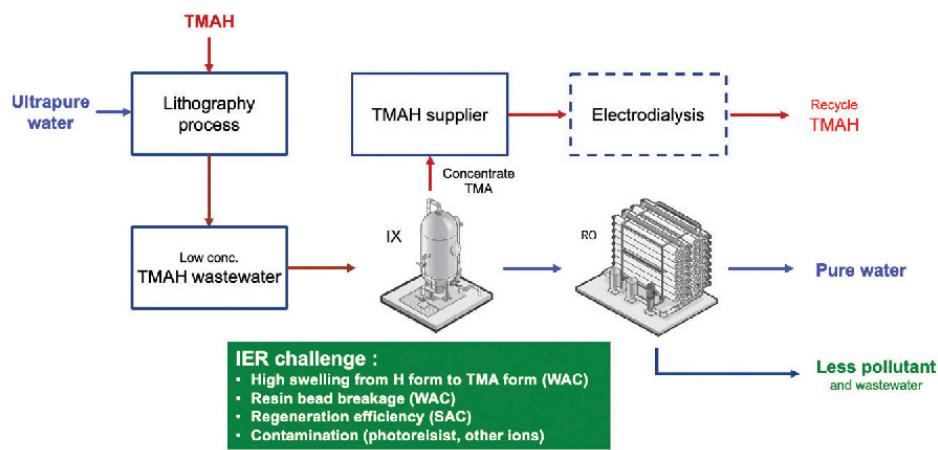
- Requirement for high salt rejection and durable chemical stability to allow for the concentration of ammonia up to 6,000ppm to allow for its subsequent recycling.
- High oxidation tolerance and resistance to H₂O₂ and Fe are needed to reduce fouling and extend membrane service lifetime.

TMAH Used in the lithography process, wastewater streams with low concentration of TMAH can use a combination of technologies to allow for the recovery of this valuable material. Concentrated TMA can be extracted with the aid of cation resins before the remaining wastewater (now TMAH <10ppm) can be treated by RO to produce pure water for reuse. The concentrated TMA can then be recycled into TMAH and other products with the aid of electrodialysis (**FIGURE 4**).

“While reclaiming end of pipe water is critical for future sustainable fab operation, treating discrete wastes like TMAH, copper, and ammonium hydroxide can also harvest valuable raw materials instead of sending them to waste,” said Denise Haukkala, Technical Service Specialist at DuPont Water Solutions.

Key considerations in specifying IERs for this application:

- Due to high TMAH concentration in feed water, high operating capacity

**Figure 4.**

is required to reduce regeneration frequency

- The swelling from H form to TMA form is approximately 160%, requiring resins with high physical strength to reduce breakages

Silicon Silicon particles generated in back grinding are cleaned from wafers using ultra-pure water (UPW). UF membranes can be used to concentrate silicon particles ahead of their recycling for use in the steel industry. Avoiding the use of chemicals for silica extraction, allows for an RO polishing stage to remove any remaining contaminants before the water is ready for reuse (**FIGURE 5**).

This approach was pioneered by TSMC, who launched a back grinding wastewater recycling system in its Advanced Backend Fab 3 in July 2020. 15,000 metric tons of back grinding wastewater had been processed by

January 2021, generating 30 metric tons of industrial-grade silicon products [2].

Key considerations in specifying UF membranes for this application:

- Membranes utilizing PES and PVDF fibers offer fouling resistance which is useful due to the fine silica particles that need to be filtered from the wastewater
- Poor selection could require the use of polymeric coagulants, increasing chemical usage

Multi-tech solutions to reduce energy and cost of MLD or ZLD

Regulators are increasingly requiring industry to minimize discharge volumes, with some authorities even mandating zero liquid discharge (ZLD). Conventional thermal treatment solutions for ZLD are energy-intensive and prove challenging to

adopt alongside complying with other sustainability goals.

A membrane-based wastewater treatment solution can achieve up to a 95% recovery rate – minimal liquid discharge (MLD) – reducing the volume of water that may require additional dewatering via thermal ZLD methods. The water reclaimed through processing can then be reused and this approach is considerably more cost-effective than conventional approaches.

Upgrading existing water reuse solutions

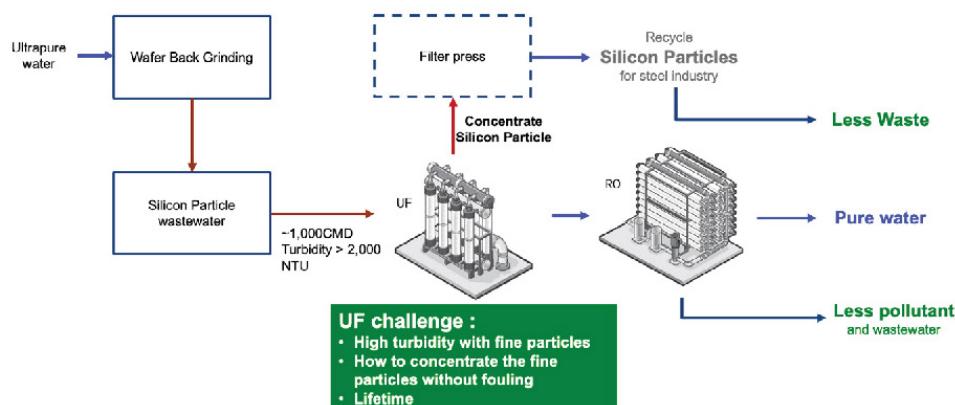
With advancements in water treatment technologies, there are opportunities for existing water reuse systems to be upgraded to deliver improved performance; benefits aren't restricted solely to new facilities. Often there are some quick wins that can be achieved by retrofitting existing infrastructure and with zero or minimal increase in physical footprint.

For example, a foundry was able to retrofit an existing standby RO unit with upgraded membranes to allow RO brine from two existing wastewater reclamation systems to be recycled as makeup water for cooling towers [3]. By selecting low-energy membranes and using feed spacers to reduce energy consumption, the upgraded solution avoided the need for costly and energy-intensive booster pump upgrades.

"Optimizing the RO elements for existing assets or adding energy recovery devices can provide quick gains on reliable operation and achieving sustainability goals for energy," added Denise Haukkala. "Selecting a more optimal reverse osmosis element can help save energy, maintenance costs and increase product lifespan."

REFERENCES

1. https://esg.tsmc.com/en-US/file/public/e-all_2023.pdf#page=116
2. <https://esg.tsmc.com/en-US/articles/29>
3. <https://www.dupont.com/knowledge/water-recycling-at-taiwanese-semiconductor-plant.html>

**Figure 5.**

Workforce Development

Solving the Skilled Tech Talent Gap in the Semiconductor Industry

CRAIG WALTERS, Vice President Business Process Outsourcing, Semiconductor, Kelly

By implementing strategic workforce management and partnering with experienced experts, semiconductor companies can effectively navigate the talent shortage, build a sustainable workforce, and position themselves for long-term success

THE U.S. SEMICONDUCTOR INDUSTRY IS AT a strategic crossroads. Despite being a global technology leader, the U.S. currently manufactures only about 12 percent of the world's semiconductors—not including the most advanced types.

Recognizing the strategic importance of this sector, the U.S. government took decisive action in August 2022 by signing the Creating Helpful Incentives to Produce Semiconductors (CHIPS) and Science Act into law. This legislation allocated more than \$75 billion to revitalize American competitiveness in the industry and to limit the need for foreign suppliers.

While this opens up an amazing potential for U.S. companies to take a larger portion of the highly profitable global semiconductor market (estimated to reach \$1 trillion by 2030) [1], there is a significant shortage of skilled tech talent. The gap between available positions and qualified workers is expected to persist through 2030—threatening to limit growth and innovation.

With nearly 80 years of experience in workforce management and decades of hands-on experience in the semiconductor industry, Kelly® is

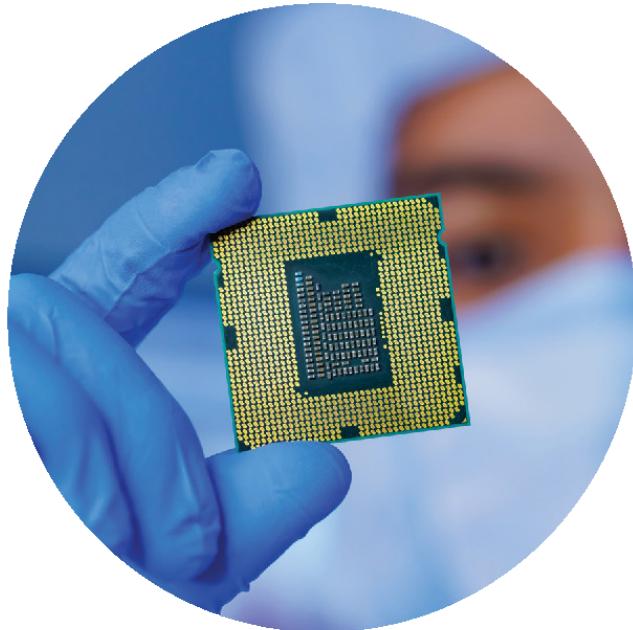
at the forefront of addressing this critical talent gap through our expertly designed, custom business process outsourcing (BPO) solutions.

The semiconductor talent challenge

While the CHIPS and Science Act of 2022 represents a significant step toward revitalizing the U.S. semiconductor industry, it does not mitigate the pressing talent shortage facing the sector. This challenge is rooted in long-term trends and requires a multi-faceted approach.

Decline in domestic manufacturing workforce

According to McKinsey data,



the U.S. domestic semiconductor manufacturing workforce has declined by 43% since its peak in 2000, leaving the industry with a diminished talent pool.

Demanding jobs and lack of clear pathways contribute to attrition The semiconductor industry is known for its demanding work environment—characterized by long hours, high-pressure deadlines, and rapidly evolving technologies. These factors, coupled with a lack of clear career progression pathways in some companies, make the competition





for talent fierce and contribute to employee attrition.

Without well-defined career development plans, employees can feel undervalued and uncertain about their future within the company, leading them to seek opportunities elsewhere.

Massive investments and job

creation Public and private investments aimed at rapidly expanding the U.S. semiconductor industry are projected to exceed \$250 billion by 2032. This influx of capital is expected to create more than 160,000 new jobs in engineering and technician roles, and additional positions in related construction fields.

The growing talent gap The scale of the skilled tech talent shortage becomes apparent when comparing current graduation rates with projected demand.

Engineers:

- Approximately 1,500 engineers join the semiconductor industry annually.
- By 2029, the demand for semiconductor engineers is forecast to reach 88,000 workers.

Technicians:

- Only about 1,000 new technicians enter the field each year.
- By 2029, demand for these workers is expected to rise to 75,000 workers.

According to McKinsey's analysis, the demand for talent is likely to far exceed available labor—even if numerous programs are designed to bridge the gap in supply and achieve their stated aims.

Bridging the semiconductor talent

gap How can the American semiconductor industry fully take advantage of funds provided by the CHIPS and Science Act, with such a considerable skilled tech talent gap? Staffing shortages on this scale put domestic objectives

at risk. They can drive up labor costs and delay or diminish the return on the monumental investments being made in the sector.

Solving this problem requires a significant change from the customary strategies for cultivating, sourcing, and retaining talent.

Outcome-driven workforce

development Rather than waiting for the marketplace to provide skilled workers, companies can take an outcome-driven approach to workforce development. This strategy begins with specific business goals. Management can then work backward from those outcomes to identify clear career pathways to develop workers with targeted skills and training. Using this strategy, businesses circumvent the talent shortage to create a sustainable, competitive talent pool that supports long-term success in a rapidly developing industry.

A semiconductor spotlight on Rhonda

Rhonda, a current Kelly employee, was an underwriter trainer for a mortgage company. After four layoffs, she was in search of a new career path. While entering the semiconductor industry without experience felt intimidating at first, she quickly realized she had transferrable skills that allowed her to thrive and move up in the industry. She started as a level one technician, and has ascended to a supervisor, an operations manager-in-training, an

operations manager, and is currently a senior operations manager. Rhonda has stated that she's invigorated by being at the forefront of cutting-edge technology and by the adventure that each new day at work brings.

Identify entry points with potential for growth This approach includes recognizing the potential of roles that do not require a college degree. These accessible positions can serve as entry points for individuals to be nurtured and developed into more advanced roles over time—creating a pipeline for future skilled workers in the industry.

A semiconductor spotlight on Matt

Matt, a former restaurant chef of 12 years, found his way to a career as a level one semiconductor technician with Kelly. Without an associate or bachelor's degree, he was looking for a foot in the door in a brand-new industry where his finely honed soft skills would translate. In his role with Kelly, he became a bay captain, a shift lead, a supervisor, and an operations manager. After five years, he was hired directly by the semiconductor company—working today as a group leader and a liaison for our on-site talent at the location.

Implement training and development programs Targeted training and development programs are critical to the success of a workforce development strategy. Companies can nurture talent from within, reducing reliance on external hiring for advanced roles. Clear career pathways reduce attrition and increase company loyalty.

A semiconductor spotlight on Dan

Dan immigrated to the U.S. from Israel in 2012, working as a restaurant cook and in retail sales to improve his English language skills. Seeking greater stability and a consistent work schedule, he accepted a level one semiconductor role with Kelly. His commitment to safety and quality, excellent reliability, teamwork, and problem-solving allowed him to advance to a leadership

role. Currently, Dan is an operations manager for Kelly at the semiconductor company, where he enjoys the opportunity to learn and grow daily.

Upskilling: a key strategy for workforce development Upperskilling programs can fundamentally change semiconductor companies' talent equation. The programs proactively enhance employee performance by equipping them with the latest skills and knowledge. They cultivate loyalty through clear career pathways and improve productivity by ensuring employees are engaged and up-to-date in their knowledge.

Common upskilling programs include:

- Training courses
- Mentorship programs
- Tuition reimbursement
- Job rotations
- Technology access

Here are five benefits of using upskilling to strategically and systematically develop existing talent:

1. Training existing employees can be more cost-effective than recruiting and onboarding new hires, especially for specialized roles.
2. By demonstrating their commitment to their workforce, companies reduce attrition and improve job satisfaction.
3. As employees gain new skills, they become more efficient and effective in their roles, enhancing organizational productivity.
4. Upperskilling ensures that the workforce remains current with the latest industry developments.
5. By developing employees' skills, companies can prepare internal candidates for future leadership roles, ensuring smooth transitions and knowledge retention.

By prioritizing upskilling, semiconductor companies can create a more resilient, adaptable, and skilled workforce capable of meeting the industry's evolving challenges.

A semiconductor spotlight on Rich

Rich was working in construction

manufacturing leadership until his company began downsizing. He accepted a role as a level one semiconductor technician with Kelly. Rich stood out due to his unique interest in process improvements and team development, and quickly moved up to a senior operations manager role. Throughout his five-year tenure with Kelly, Rich has had a hand in hiring more than 450 technicians to support the semiconductor company. He currently oversees factory support operations and the startup of a new, remote branch.

Right talent, right jobs, right time In a rapidly evolving and highly competitive industry, ensuring the right talent is in the right roles at the right time can make or break success. However, finding, hiring, onboarding, and upskilling a large staff can be overwhelming for even the best internal HR departments. Time spent on administrative tasks can detract from the strategic workforce planning and development initiatives that are critical for long-term success.

To effectively address the talent shortage, companies need to ensure they have the right talent available. This requires a nuanced understanding of the skillsets required at each job level, from entry-level to highly specialized roles.

Turn to a BPO solution

This is where a business process outsourcing (BPO) solution from Kelly becomes a game-changing advantage. With decades of experience providing workforce solutions, Kelly is the leading provider of skilled tech talent for the semiconductor industry.

Our team has a deep understanding of the skillsets required for each job level—from safety mentors who

partner with skilled technicians during tool installation projects, to field service engineers and supervisors. This unmatched expertise allows us to provide tailored workforce solutions to the industry's most competitive semiconductor organizations—helping them to build a team of skilled workers, well-trained on the company's internal processes.

Comprehensive semiconductor workforce solutions By implementing strategic workforce management and



partnering with experienced experts, semiconductor companies can effectively navigate the talent shortage, build a sustainable workforce, and position themselves for long-term success in this critical industry. The key lies in working with a partner who understands how to identify and manage talent across all levels of technical skills.

Partnering with Kelly delivers established BPO solutions, industry-specific expertise, and a proven track record—allowing semiconductor companies to focus fully on innovation and core business objectives, while ensuring their workforce needs are met with precision and efficiency. 

To learn more, visit www.kellyservices.us/semiconductor-digest/

REFERENCE

1. <https://www.mckinsey.com/industries/semiconductors/our-insights/reimagining-labor-to-close-the-expanding-us-semiconductor-talent-gap>



Navigating the Complexities of Semiconductor Supply Chains

TAMMY MAX, Director of Technical Content at Accuris

THE SEMICONDUCTOR INDUSTRY HAS recently experienced widespread consolidation through merger and acquisition (M&A) activity. Over the past several years, there have been several notable semiconductor acquisitions, including Intel's purchase of Mobileye for \$15.3 billion and Analog Devices' acquisition of Linear Technology for \$14.8 billion.

M&A can benefit companies and investors in many ways, including reduced costs and increased efficiencies, but it can pose significant challenges to the supply chain. In an industry where supply-chain disruptions are already common — mostly due to natural disasters, geopolitical tensions, and factory closures — M&A adds an extra layer of complexity. Electronic products manufacturers, face production delays and shortages due to these industry shifts.

Why does M&A cause supply-chain disruptions?

A product's Bill of Materials (BOM) doesn't change. With M&A part numbers and manufacturer names do change. As a result, semiconductor components impacted by M&A will have multiple identifiers, including their original identity and any subsequent post-acquisition identities.. This can lead to confusion and critical disruptions in a supply chain.

For example, obsolescence and product change notices (PCN) — the documents issued by manufacturers to inform customers about changes to products or manufacturing process

— are usually communicated under their current identifier. The internal dynamics of companies, including their previous M&A history and the use of distributor or legacy part numbers, compound the issue of proper identification.. This confusion may cause production line-down situations or could even force a redesign in the middle of an electronics manufacturer's product lifecycle.

Electronicproduct manufacturers can address these issues with best practices that capture manufacturer and part-number changes over time. For example, it's often beneficial to assign internal part numbers — which allows for more than one manufacturer or part-number identifier for the same part — in internal systems such as PLM(product lifecycle management) platforms and product libraries.

In the past, not tracking part/manufacturer changes over time required significant manual work to assure PCN/EOL notices were not missed due to using legacy part numbers, and often lead to duplication of part numbers and missed opportunities to consolidate volumes for purchasing power.

The good news is that artificial intelligence (AI) technology can help combat these challenges and streamline the process of uncovering identity discrepancies, preventing disruptions.

AI to the rescue

Over the past few years, AI tools have captivated the attention of companies as a way to save time and resources. The

visibility and insights derived from AI empower manufacturers and supply chain professionals to make more informed decisions across their supply chain following M&A activity, pinpointing any deviations and resolving problems before they arise.

By analyzing historical data, schedules and sequences, AI can help design engineers and procurement teams anticipate demand fluctuations and potential supply issues *before* they materialize, leading to proactive problem-solving rather than reactive crisis management. The latest supply-chain AI tools can even help with auto-association of historical identifiers to current identifiers. If a customer uploads a BOM, for example, AI can automatically match the current identifier to the historical identifier, reducing duplication and confusion.

The technology can also be leveraged to track PCN, processes product discontinuance (PDN), and end of life (EOL) issuances from component manufacturers, immediately notifying supply-chain processionalists of any changes, and offering insights on how and when these should be addressed. Through the use of AI, supply chain teams can maintain healthy operations following M&A and other disruptions.

As M&A reshapes the semiconductor industry, supply chains need to adapt. AI offers solutions that streamline operations, manage part duplications, and improve visibility. By leveraging these technologies, companies can navigate challenges more effectively and maintain innovation in a changing market. 



Managing the Impact of Semiconductor Manufacturers' Use of Freshwater

VINCENT PUISOR, Global Business Development Director, Water and Wastewater at Schneider Electric

THE UN PREDICTS THAT BY 2030 THERE will be a 40% gap between global freshwater supply and demand. Amid the escalating decline in freshwater availability, industry still accounts for a staggering 20% of global freshwater withdrawals.

The increased threat of water scarcity, competition for water resources due to a growing global population, and new regulations for wastewater discharge, has highlighted the urgent need to address inefficiencies across all industrial sectors.

The semiconductor industry is no exception, with the chip manufacturing boom increasing water consumption by 20-30% in the last few years. Today, the industry is on average using five times more water for chip production in comparison to ten years ago. In fact, a single semiconductor fabrication plant can use up to 10 million gallons of water per day, which is equivalent to the daily water consumption of a city with a population of 300,000, while an average chip manufacturing facility today can use 10 million gallons of ultrapure water per day—as much water as is used by 33,000 US households every day.

Furthermore, the demand for high-quality ultrapure water (UPW) needed for cleaning and cooling continues to rise, with the average chip manufacturing facility using 10 million gallons of UPW each day.

Producing ultrapure water is typically 60 to 350 times more expensive than producing drinking water, mainly due to the additional purification processes and equipment required to remove virtually all contaminants. This cost is so high because of the energy consumption and chemical usage that is needed for water treatment processes. With water demand showing no signs of slowing down, it is crucial for manufacturers to review operations now to optimize processes and reduce their water consumption.

The operational case for enhanced circularity

According to recent analysis from S&P Global, “water scarcity is a risk in the coming decade for the tech hardware industry, particularly the water-intensive semiconductor subsector. Mishandling of such a risk could hit a chipmaker’s operations and creditworthiness.”

By 2030, 40% of chip production facilities are predicted to be in high- or extremely high-water-risk areas. Already many governments across the globe are increasing investments in domestic semiconductor manufacturing efforts to safeguard supplies while managing ESG concerns and environmental impacts.

Combine this threat with the expanding regulation to include zero liquid discharge (ZLD) treatment

process—which has the capability to reduce plant overall energy consumption by up to 20% and coagulant & flocculant chemical usage by 5- 20%—and it is clear that it is essential that the semiconductor industry focuses efforts on the importance of smarter water use across their operations.

So, what does this look like in practice?

Creating a data-driven circular water economy

Today, data-driven industrial water management technologies are revolutionizing how companies can approach water management and sustainability. Automation coupled with data and AI are playing a crucial role in enabling better management of resources, optimizing treatment processes, and improving operational efficiencies supporting quicker and more precise decision-making than ever before.

This is particularly true for industrial water management solutions that are layered with sensors, data, and cloud-based platforms to optimize physical water systems. The integration of AI, Machine Learning (ML), Data Analytics, Internet of Things (IoT), sensors, and digital twins provides a huge volume of data insights that can be leveraged for quick analysis to measure water quality and make predictions using demand forecasting.

AI models can optimize processes in the semiconductor industry, addressing key challenges such as reducing energy consumption, improving chemical usage efficiency, and extending the lifespan of critical assets. AI models can optimize chemical use in wafer fabrication, reducing waste and ensuring consistent quality. Energy optimization AI models can help semiconductor manufacturers reduce energy consumption by up to 10% by identifying efficiency improvement opportunities. AI-driven predictive maintenance can extend the lifespan of critical assets, such as membranes used in ultrapure water systems, by up to 12 months, reducing replacement costs and minimizing unscheduled downtime.

By leveraging AI-related solutions and process optimization, water producers will benefit from reduced overall process energy consumption, reduced chemical consumption and reduced clean water consumption for CIP process.

Getting started with water circularity models

To maximize ROI for investments in these technologies, semiconductor companies should:

- **Measure water consumption**, beginning with a comprehensive assessment of their manufacturing facility's water footprint and using smart meters and IoT sensors to monitor water usage in real-time. As part of this, establish key performance indicators to track progress and identify areas for improvement, as well as reducing waste and improving water conservation.
- **Educate and train employees** about the importance of water conservation and circularity to foster a collective culture of sustainability. Companies can do this by providing training on best practices for reducing water waste and optimizing water use in

daily activities.

- **Partner with experts** and technology providers to design and implement effective water circularity solutions. Leveraging external expertise can help identify innovative approaches and ensure the integration of new technologies.
- **Continuously improve and innovate**, conducting periodic audits to assess the effectiveness of water circularity initiatives and make necessary adjustments to enhance performance.

Regulatory landscape

The semiconductor industry is also subject to increasingly stringent regulations related to water use and discharge. In the United States, the Environmental Protection Agency (EPA) has established the National Pollutant Discharge Elimination System (NPDES) permit program, which regulates the discharge of pollutants into water bodies. Semiconductor companies must obtain NPDES permits and comply with the specified limits on pollutant discharge.

In addition, some regions have imple-

Semiconductor companies must set clear goals for reducing freshwater consumption by enhancing efficiency and promoting circularity within their operations.

- **Taking collective action**, extending beyond the semiconductor factory boundaries to encourage your supply chain to reduce water impacts, and partner with other actors in water replenishment programs.
- **ESG funding and Green bonds**, which are financial instruments specifically designed to support projects that have a positive environmental impact. Semiconductor manufacturers, with their significant energy consumption and potential environmental footprint, can be eligible for such funding.
- **Water recycling and conservation**: Implementing water recycling systems and reducing water consumption.
- **Renewable energy adoption**: Investing in renewable energy sources to power manufacturing operations. By leveraging ESG funding and green loans, semiconductor manufacturers can accelerate their transition to more sustainable operations while benefiting from financial advantages and improved reputation.

mented more stringent regulations, such as California's State Water Resources Control Board, which has set a goal of reducing water use in the semiconductor industry by 25% by 2025. Companies that fail to comply with these regulations may face significant fines and reputational damage.

Looking ahead

Adopting water circularity practices remains crucial for semiconductor manufacturing to ensure a sustainable future. Implementation of automation alongside advanced digital technologies can help water-intensive industries root out waste, improve operational efficiencies, and reshape operational processes for more sustainable water management.

Ultimately, the cost of doing nothing far outweighs the cost of taking action. Semiconductor companies that prioritize water sustainability will not only contribute to the preservation of this vital resource but also position themselves for long-term success in an increasingly water-constrained world. 

Continued from page 19
 development of this semiconductor manufacturing industry community profile creation," said Brian Korn, Director for SMCC and Staff Technologist focused on Cybersecurity and Automation at Intel Foundry.

SMCC will provide cybersecurity

recommendations for semiconductor manufacturing equipment, information on implementation, and updates on the development of the community profile.

SMCC working groups are engaged with the SEMI Standards program to create a standards-based approach supporting the semiconductor ecosystem

by leveraging the program's 50-year history of industry alignment. SMCC is currently working on developments to two cybersecurity standards:

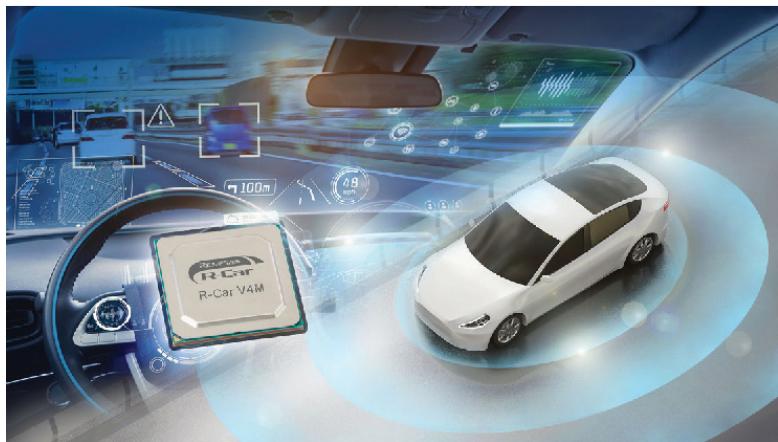
- E187: Specification for Cybersecurity of Fab Equipment
- E188: Specification for Malware-Free Equipment Integration

Renesas Intros 4th-Generation R-Car Automotive SoCs

Renesas Electronics Corporation expanded its R-Car Family of system-on-chips (SoCs) for entry-level Advanced Driver Assistance Systems (ADAS). The new devices, the R-Car V4M series and the expansion of the existing R-Car V4H series, deliver robust AI processing capability and fast CPU performance, while carefully balancing performance and power consumption. Their

exceptional TOPS/W performance and power-optimized features make them ideal for entry-level, cost-sensitive

ADAS applications such as front smart camera systems, surround-view systems, automatic parking and driver monitoring systems.



Based on the same advanced 7-nm manufacturing process technology as the powerful R-Car V4H series, the new R-Car V4M series delivers deep learning performance of up to 17 TOPS and boasts high-speed image processing and precise object recognition using on-board cameras, radar and

AD INDEX

Advertiser	Pg
Bechtel M&T.....	C4
Busch LLC.....	17
Edwards Ltd.	51, C3
Fastmicro B.V.	3
Guardian Equipment.....	25
Hammond Power Solutions.....	5
Levitronix Technologies Inc.....	C2
Middlesex General Industries, Inc.....	11
Nikon Precision, Inc.	19
Nordson Test & Inspection	7, 13
Schneider Electric.....	15, 21
SEMI.....	27, 29
Spotfire	9, 23
Thermcraft, Inc.....	33
TOPTICA Photonics AG	31

SEMICONDUCTOR DIGEST OFFICES

NEWS AND INDUSTRY TRENDS
Gold Flag Media, 58 Summer Street, Andover, MA 01810

ADVERTISING

North America, ROW



Kerry Hoffman

Tel: 978-580-4205

kerryh@semiconductordigest.com

Germany, Austria, Switzerland & E. Europe



Holger Gerisch

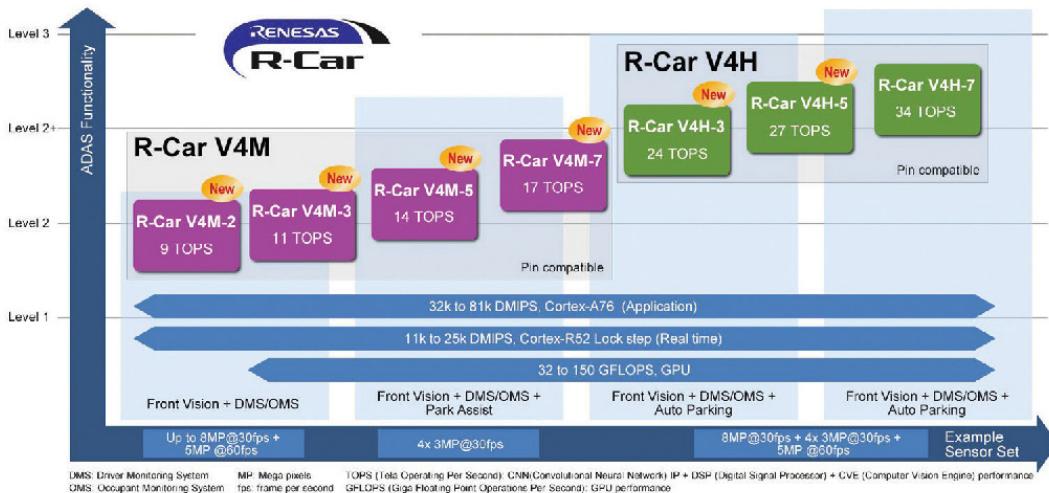
Tel: +49 0 8856 8020228

holger.gerisch@gmx.de

For advertising information,
 please visit www.semiconductordigest.com/advertise.



4th Generation R-Car SoC Lineup for ADAS



LiDAR. With the addition of the new R-Car V4M and R-Car V4H devices, customers can now select the best suited SoC option in Renesas' scalable ADAS portfolio. These devices offer advanced AI technology, performance and power efficiency to meet a diverse array of ADAS application requirements. The new devices maintain pin compatibility within the same series and software compatibility with existing R-Car products, allowing OEMs and Tier-1 suppliers to reuse existing software and reduce engineering costs.

"We are extending our ADAS offerings to meet the increasing demand for Level 1 and Level 2 ADAS solutions for mass-market vehicles," said Aish Dubey, Vice President & General Manager, High Performance Computing SoC Business Division at Renesas. "At the same time, we are developing our new 5th Generation R-Car SoCs, which will further bolster our offerings in ADAS, cockpit, gateway, and infotainment segments. We are committed to offer the broadest range of automotive

embedded processor solutions for all vehicle classes — from entry-level to luxury-class models — all under a single development platform."

The R-Car V4M and R-Car V4H series feature up to four Arm® Cortex®-A76 cores delivering up to 81K DMIPS performance for application processing. It also comes with three Arm Cortex-R52 lockstep cores with up to 25K DMIPS performance for real-time operation. The new devices

are extremely power efficient, providing 9 TOPS/W performance, thanks to their highly integrated design and leading-edge manufacturing process technology. In a typical full-feature smart camera with an 8-megapixel sensor, the R-Car V4M consumes around 5 watts of power – 50 percent less than similar devices on the market. Renesas is sampling the R-Car V4M and R-Car V4H devices to leading automotive manufacturers now, with mass production scheduled in Q1/2026.

SEMICONDUCTOR DIGEST

PRODUCT SHOWCASE

Download The Semi Dig App

Scan the QR code to download the app from Google Play or the App Store.

Google Play App Store

Upgrade efficiency. Downsize emissions.



The new, easy swap out, energy saving iXH1210 dry pump upgrade.
Scan for details.



EDWARDS



Cracking the Chip Code to Meet AI's Growing Demands

MOZ AHMED, Edge & Embedded Technology Solutions Manager at Mobia

AI IS REVOLUTIONISING ENTIRE industries. By next year, it's expected the world will generate over 180 zettabytes of data. As a result, a fundamental shift in computing power is needed to cater for the development of these data-hungry innovations.

In response to this need, one solution that's gaining traction is heterogeneous computing. This enables a single system to have multiple computing sub-systems, such as CPUs, GPUs, DSPs, FPGAs and ASICs. These processors execute core instructions differently, but work in parallel to help increase compute speed and lower the time required to complete a task. The result? A more seamless user experience in instances where vast amounts of data need to be processed and converted — such as AI and machine learning workloads.

A balancing act

For those wishing to push ahead, a heterogeneous system on chip (SoC) is stacked with possibilities. Typically when designing a system, there's some kind of tradeoff between flexibility, performance and cost. For instance, general purpose computing might provide the most flexibility, but loses ground on performance and cost. And because application-specific computing is designed for a particular use case, it impresses when it comes to performance, but this comes at a price and with less flexibility. In contrast, embedded computing is the least flexible, but typically available for the lowest cost.

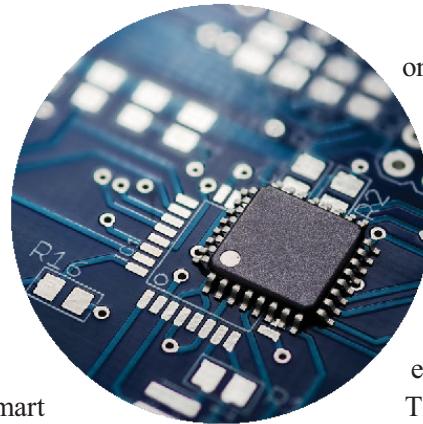
How, then, does a heterogeneous SoC

solve this problem? First, it breaks the link between performance and flexibility. This means a system can scale up to meet increased demands if required. Secondly, by taking advantage of intelligent features like smart scheduling, it breaks the link between flexibility and cost, so as many processors can be employed for as many tasks as possible. Finally, this increased flexibility and scalability results in a more efficient, cost-effective system, which can competently manage multiple tasks.

Opting for custom chip designs

When considering heterogeneous SoCs, there are real gains to be made from custom chip designs or processing blocks in an SoC. These are tailored to specific application requirements, while providing more control when integrating hardware and software.

Custom chip designs can also deliver greater cost efficiencies. Because the chip is designed for a specific use case, fewer inessential features are implemented, reducing design and fabrication costs. In turn, there are fewer functions consuming power, which minimises energy usage, and auxiliary components can be designed with a lower specification on the printed circuit board. A simpler design also means simpler implementation, making the system easier to manage and troubleshoot, which reduces



ongoing maintenance costs. And with fewer functions taking up valuable silicon space, a custom chip not only lowers costs but provides more chips per wafer, improving each wafer's yield too.

The emergence of custom instructions supported by RISC-V also provides an opportunity to further optimise the use of custom processors.

A smarter approach for AI applications

There's no question the demands placed on chips are steadily growing. Heterogeneous computing offers the chance to accelerate computing speed, while reducing the time it takes to complete a task. By delegating different workloads to specialised processors, performance can be optimised and energy efficiency improved. As businesses rush to embrace the opportunities opened up with AI and machine learning, a heterogeneous SoC offers a smarter way to achieve greater performance.

With a long-standing relationship with many of the world's leading vendors in the semiconductor industry, Mobia is well positioned to help them support their customers in maximising the potential of their silicon products.

If you need guidance on how to take advantage of heterogeneous SoCs and custom chip designs, visit www.mobica.com/semiconductor.

find out more



We're about to change the game in the subfab

00.01 | project ganymede 2025

 EDWARDS

Find out how
to increase
predictability
for your next
semiconductor
fab project.

bechtel.com/semi



Extraordinary teams building inspiring projects.

