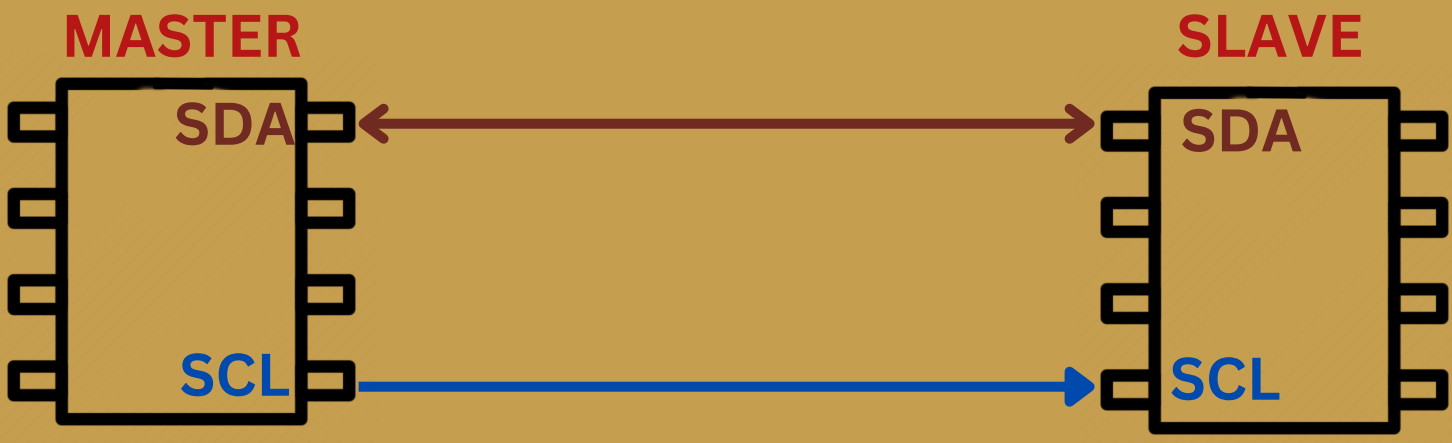
I2C Protocol ?

I2C
(Inter-Integrated Circuit)



- I2C is a serial communication protocol that allows multiple devices to talk to each other using only two wires - a clock (SCL) and a data line (SDA).

Master: The master operates as the primary controller, initiating and managing data transfers with a central role in controlling the communication flow.

Slave: In contrast, the slave devices act as subordinate participants, responding to the master's commands and actively engaging in the communication process.

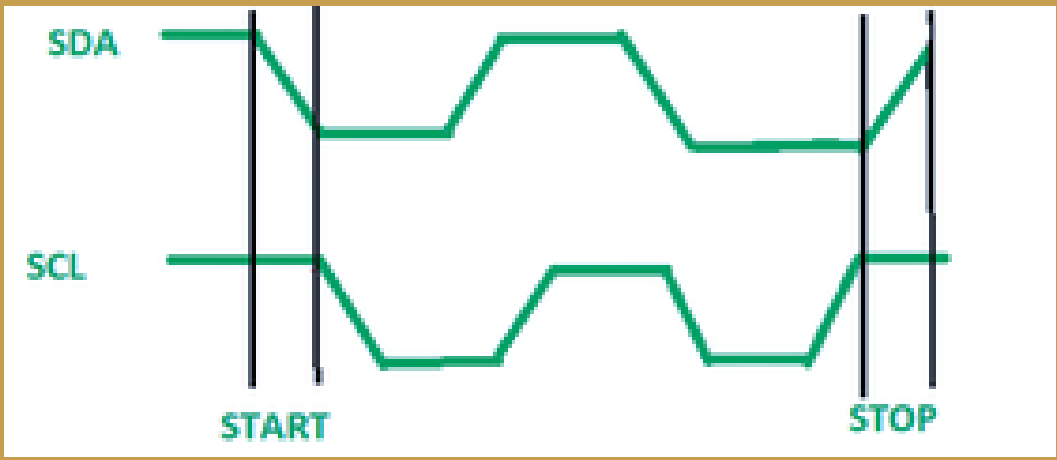
- SDA (Serial Data): Transfer of data takes place through this pin.
- SCL (Serial Clock): It carries the clock signal.

Key Concepts:

Data Line Behavior: In I2C, data changes when the clock is low, remains stable when high. Both lines are open drain, needing pull-up resistors for high levels, as I2C devices often use active-low logic.

Packet Transmission: Data is transmitted in 9-bit packets.

- Start Condition (1 bit)
- Slave Address (8 bits)
- Acknowledgment bit (1 bit)

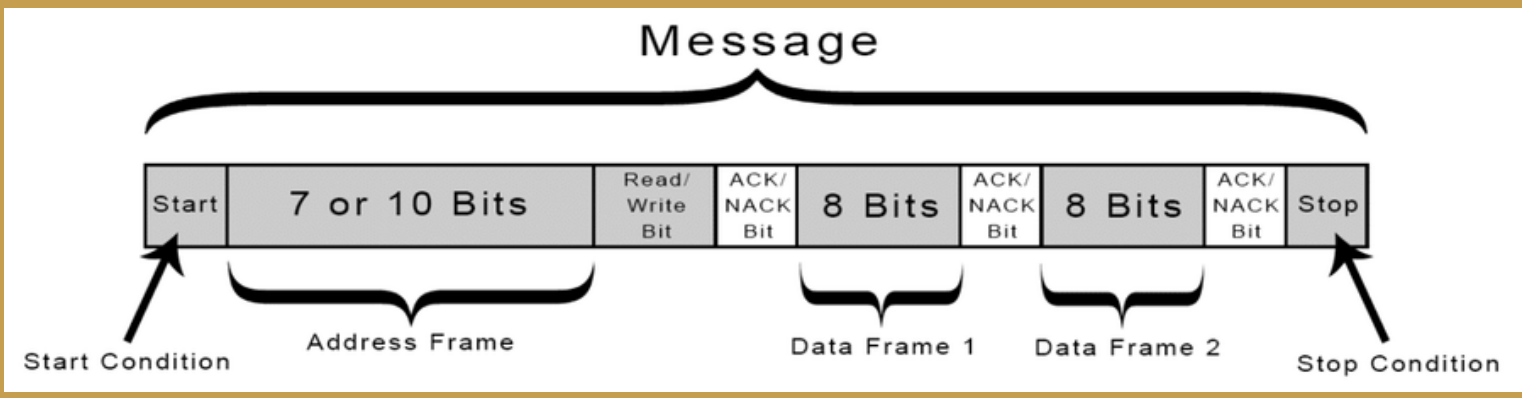


Start and Stop Conditions:

Start Condition: Initiated by transitioning SDA from high to low while keeping SCL high.

Stop Condition: Triggered by transitioning SDA from low to high while keeping SCL high.

Repeated Start Condition: Between each start-stop pair, if the master wants to initiate a new transfer without releasing the bus, it issues a Repeated Start condition.



Addressing: I2C identifies slaves through addressing. The master sends the address frame to all slaves, and the matched slave responds with a low voltage ACK bit.

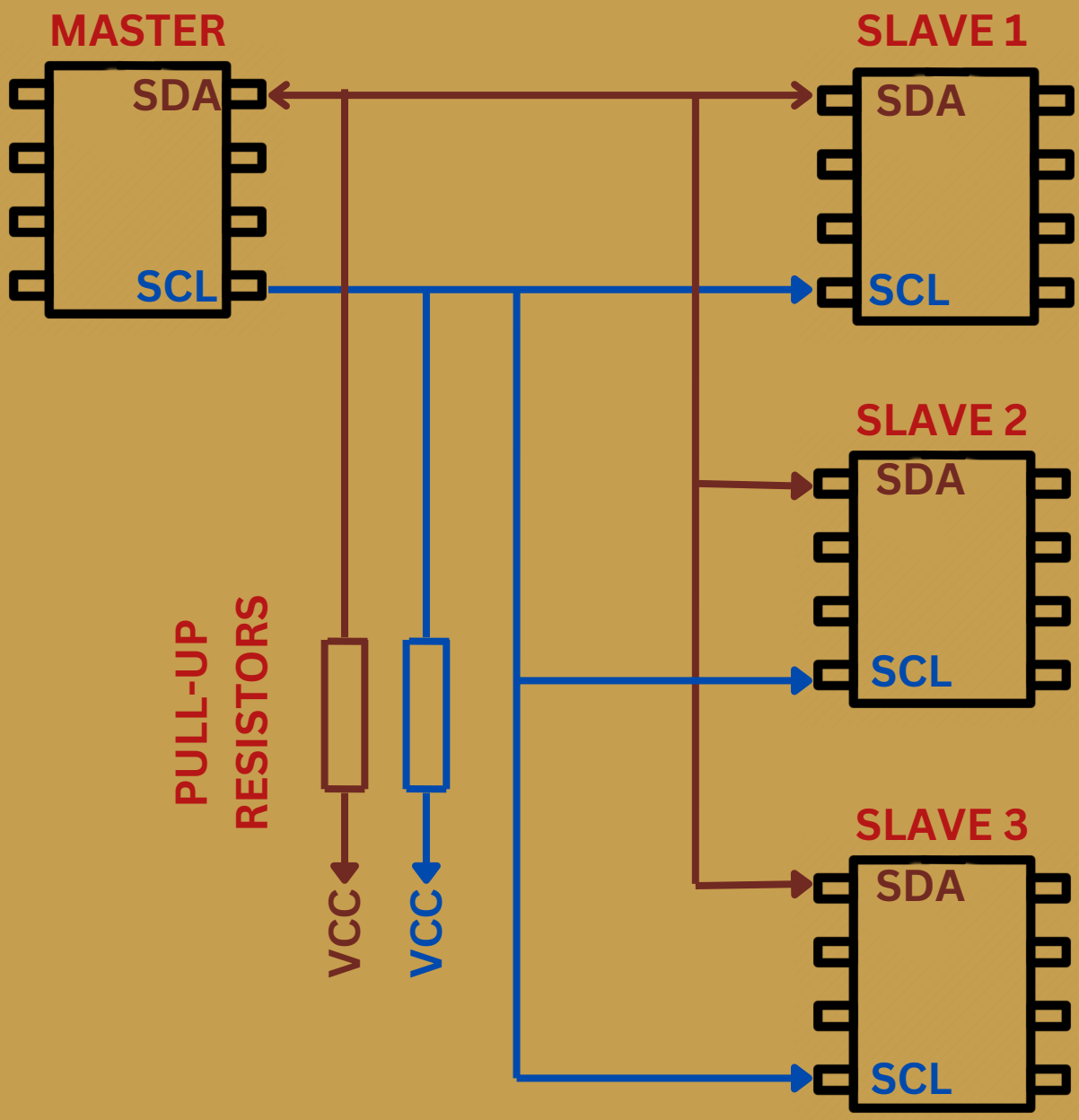
Read/Write Bit: Included in the address frame, a low voltage level signals the master is sending data, while a high level means it's requesting data.

Data Frame: After receiving an ACK bit, the master sends an 8-bit data frame, followed by an ACK/NACK bit. The next frame waits for acknowledgment.

Stop Condition: The master concludes the transmission with a stop condition – a voltage transition from low to high on SDA after a low to high transition on SCL, keeping SCL high.

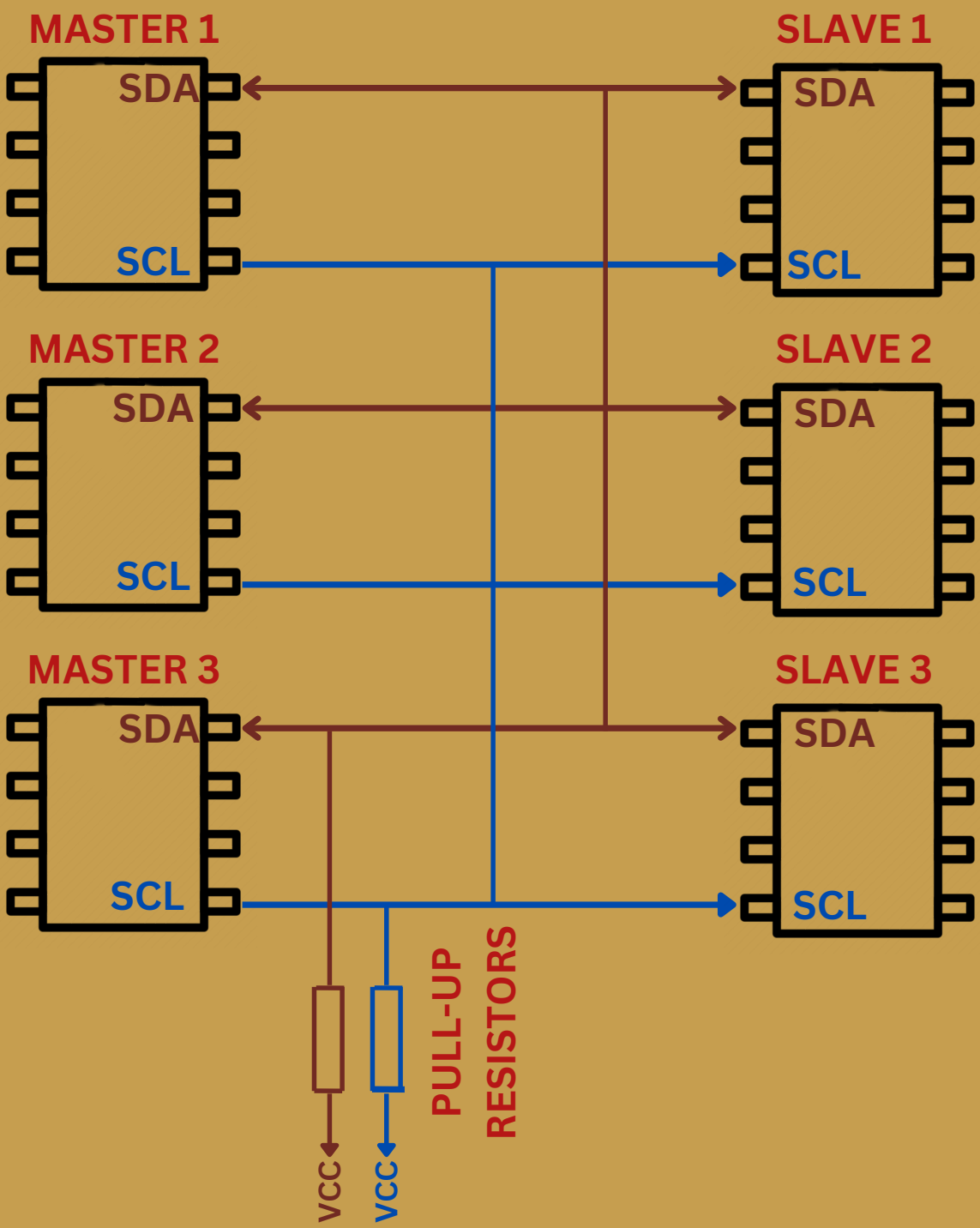
Acknowledge (ACK) and No-Acknowledge (NACK): After each frame, an ACK bit signals successful reception, while a NACK bit indicates an unsuccessful one.

Single Master Controlling Multiple Slaves



In I2C's Single Master, Multiple Slaves setup, one master communicates with several slaves on a shared bus, addressing each for data exchange. This enables efficient management and communication across multiple devices.

Multiple Masters with Multiple Slaves



Multiple Masters, Multiple Slaves in I2C allows several master devices to communicate with multiple slaves on a shared bus. Masters coordinate communication by addressing specific slaves, facilitating efficient interactions across the network.

Key Features of I2C Communication:

Half-duplex Communication: Bi-directional but not simultaneous communication.

Synchronous Transmission: Data is transferred in frames or blocks.

Multi-Master Configuration: Supports multiple masters in the system.

Clock Stretching: Slave can hold the clock low, preventing the master from raising it until ready.

Arbitration: Supports multi-master but only one active master at a time.

Serial Transmission: Utilizes serial transmission for data exchange.

Low-Speed Communication: Primarily designed for low-speed communication

I2C Specifications and Configurations

Maximum Speed:

- Standard Mode (100 kbps)
- Fast Mode (400 kbps)
- High-Speed Mode (3.4 Mbps)
- Ultra-Fast Mode (5 Mbps)

Wires Used:

- Two wires

A (Arbitrary Number of Devices) :

- Unlimited

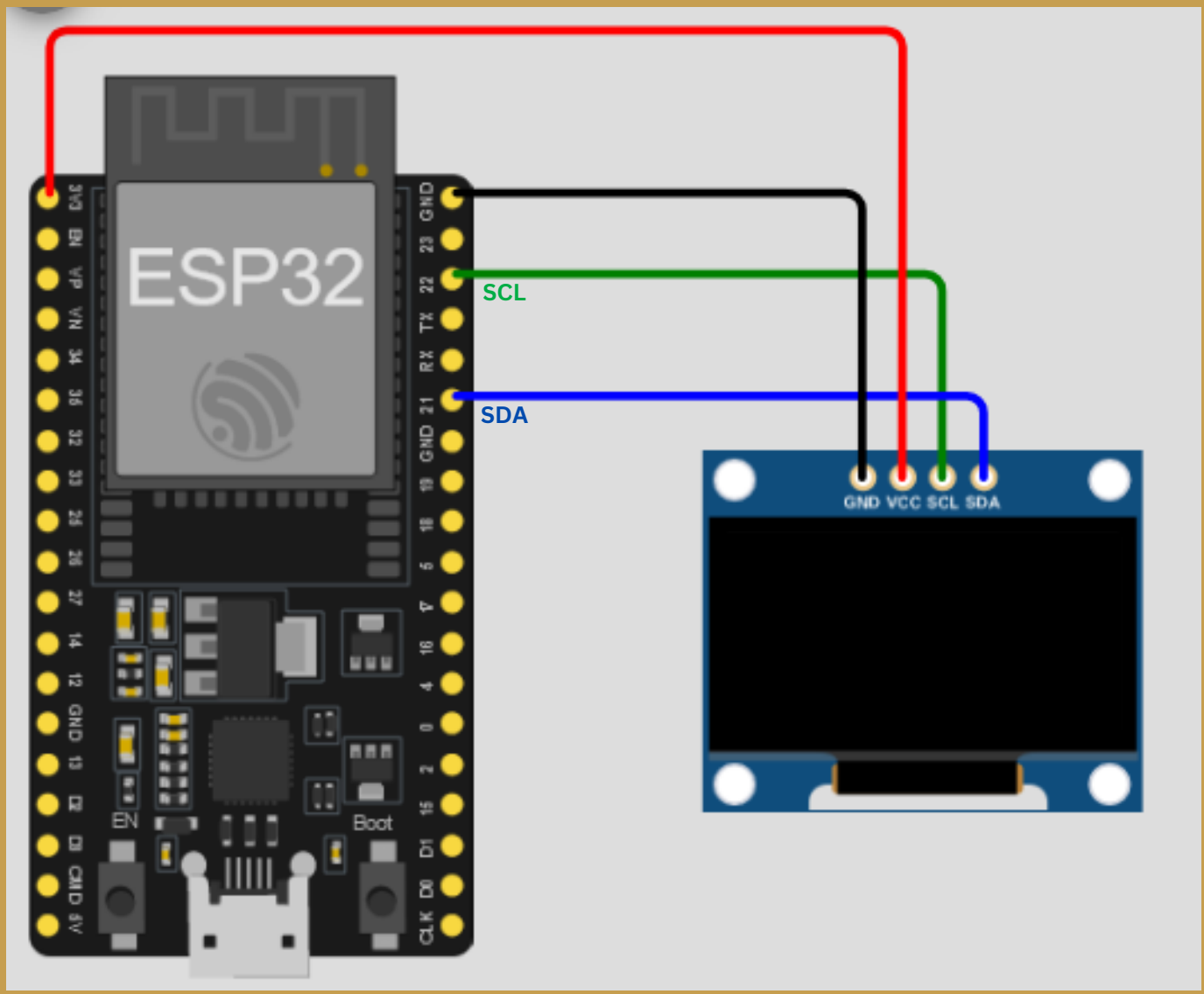
Maximum number of Masters:

- Unlimited (Multiple Masters Supported)

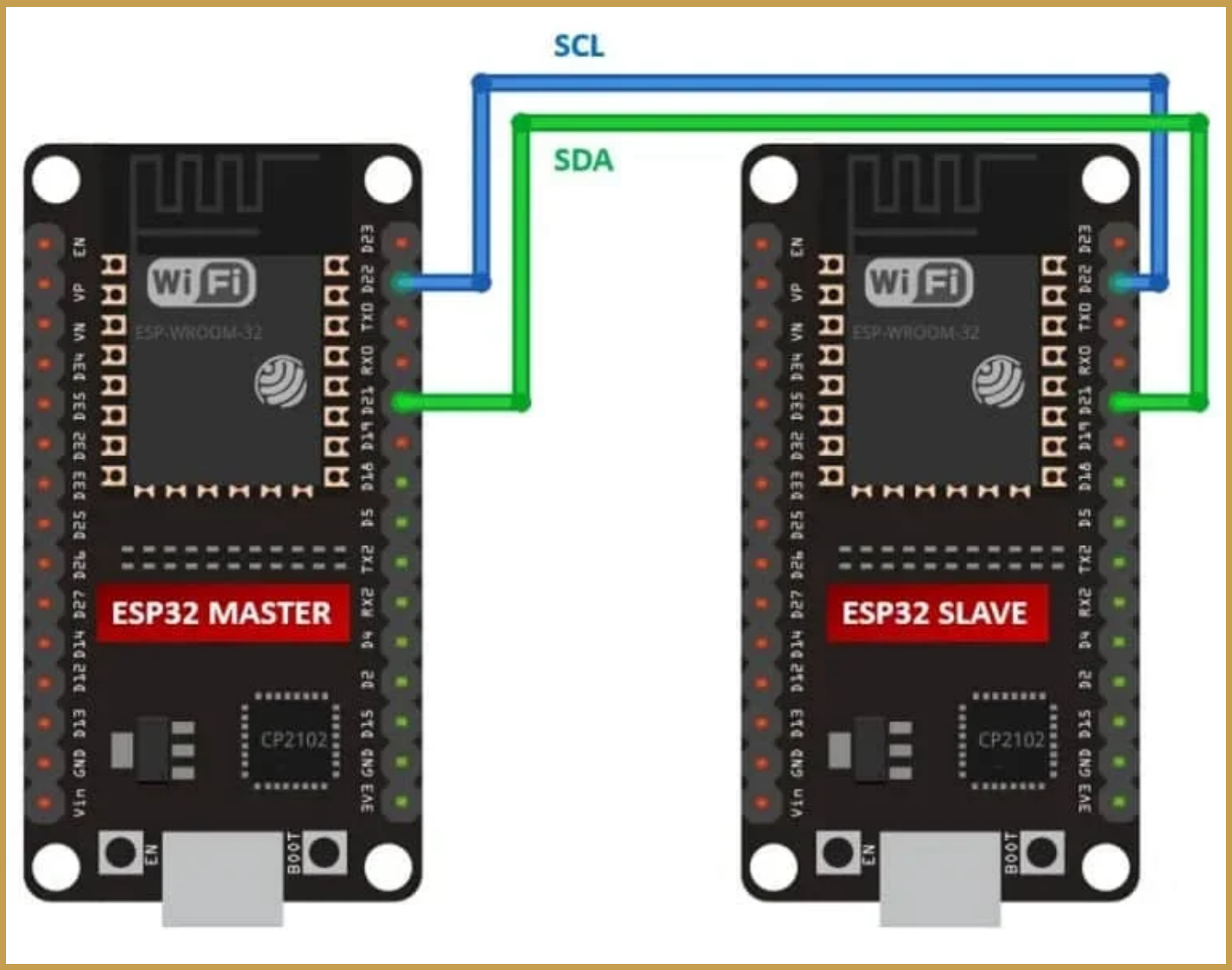
Maximum number of Slaves:

- 1008 (Large Scalability for Peripheral Devices)

Real-Time Example: ESP32 and OLED Display Interfacing via I2C Connection



Real-Time Example: Two ESP32 Devices in I2C Communication



Advantages

- Configurable in multi-master mode.
- Simplicity is achieved with only 2 bi-directional lines.
- Cost-efficient implementation.
- Improved error handling with the ACK/NACK feature.
- Supports multiple masters and slaves.
- Utilizes only two wires.

Limitations

- Slower speed compared to other protocols.
- Half-duplex communication is used.
- Limited data frame size to 8 bits.