Introduction to MOSFET for Analog Circuits

Level 2: Transistor Properties, Basic Equations, and Beginner Design

Executive Summary

This handout is designed for engineers and students transitioning from digital circuit design to analog circuit applications. It provides a practical introduction to MOSFET behavior in analog circuits without requiring deep device physics background. The material focuses on: (1) understanding what makes a MOSFET suitable for analog amplification, (2) learning the key equations that predict device behavior, and (3) applying these equations to basic analog circuit design problems. This level emphasizes hands-on understanding and practical problem-solving rather than theoretical rigor.

Target Audience: Students with basic semiconductor knowledge; digital designers moving to analog; practicing engineers seeking to understand MOSFET-based circuits.

PART I: THE MOSFET AS AN ANALOG DEVICE

Section 1.1: From Digital Switch to Analog Amplifier

1.1.1 The Digital Perspective

In digital circuits, the MOSFET is treated as a switch:

Gate voltage HIGH → Transistor ON → Output LOW (drain pulled to ground)
Gate voltage LOW → Transistor OFF → Output HIGH (drain pulled to supply)

The transistor spends most of its time in one of two extreme states: - **Fully ON (Saturation):** Channel fully conductive, very low impedance - **Fully OFF (Cutoff):** Channel nearly non-existent, very high impedance

This binary behavior is perfect for logic circuits: a signal is either a 0 or a 1 .

1.1.2 The Analog Perspective

In analog circuits, the MOSFET operates very differently :

The transistor spends most of its time **between** these two extremes—partially ON, in the **saturation region** of analog operation .

Here, the MOSFET is neither fully ON nor fully OFF. Instead, it acts as a **voltage-controlled current source**: small changes in gate voltage cause proportional changes in drain current .

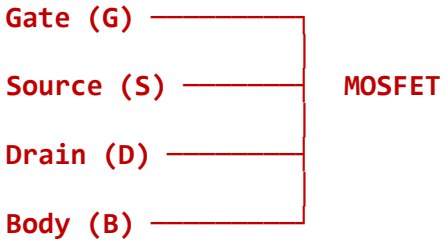
This is the fundamental shift:

Aspect	Digital	Analog
Operating Mode	ON or OFF (two states)	Saturation region (one carefully chosen point)
Gate Signal	Binary (high or low)	Continuous (small variations around DC bias)
Output	Binary (switches between rails)	Amplified signal (proportional to input)
Design Focus	Speed and fanout	Gain, noise, and linearity
Equation Used	Simple threshold model	Differential equations

Key Insight: Analog design begins when you stop thinking of the transistor as ON or OFF, and start thinking of it as a **tunable amplifier** .

Section 1.2: Four Terminal Voltages Control Everything

The MOSFET has four terminals, and every aspect of its behavior is determined by the instantaneous voltages between them :



Four voltages define the device state at any instant:

Voltage	Definition	What It Controls	Typical Range
V_{GS}	Gate to Source	Channel formation; inversion layer	0 to 1.2 V
V_{DS}	Drain to Source	Current magnitude; output behavior	0 to 1.2 V
V_{BS}	Body to Source	Threshold voltage (secondary effect)	0 to ±0.5 V
V_{DG}	Drain to Gate	Determines saturation boundary	0 to 1.2 V

These four voltages are not independent—they are related by circuit topology and design choice.

Understanding these voltages and how they interact is the foundation of analog design .

PART II: THE THREE OPERATING REGIONS

When you apply different gate and drain voltages, the MOSFET operates in three distinct regions, each with different electrical characteristics .

Section 2.1: Cutoff Region – The Transistor is OFF

Condition: $V_{GS} < V_T$

where V_T is the **threshold voltage** (the minimum gate voltage needed to form a conductive channel).

2.1.1 What's Happening Physically

When gate voltage is below threshold, very few charge carriers are attracted to the oxide-silicon interface. There is no continuous conductive path from source to drain .

Current can flow only as **leakage**—a tiny exponential current due to thermally-generated carriers :

$$I_D = I_0 \exp\left(\frac{V_{GS} - V_T}{nV_T}\right)$$

where I_0 is the leakage current (typically picoamperes) .

2.1.2 Electrical Characteristics

- **Current:** Essentially zero (picoampere to nanoampere range)
- **Input Impedance:** Extremely high (transistor is OFF)
- **Output Impedance:** Extremely high (no conductive path)

2.1.3 Use in Analog Circuits

The cutoff region is used for:

- **Switching applications:** MOSFETs can be used as analog switches (multiplexers, sample-and-hold circuits)

- **Power gating:** Turning off entire circuit blocks to save power

Not used for amplification (current is too small).

Section 2.2: Linear (Triode) Region – The Transistor Acts Like a Variable Resistor

Condition: $V_{GS} > V_T$ AND $V_{DS} < (V_{GS} - V_T)$

2.2.1 What's Happening Physically

Above threshold, a conductive inversion layer forms at the oxide-silicon interface, connecting source to drain . This layer acts like a resistor .

The **channel resistance** depends on gate voltage : - Higher gate voltage → thicker channel → lower resistance - Lower gate voltage (but still above V_T) → thinner channel → higher resistance

The drain voltage is small enough that the channel remains approximately uniform along its length .

2.2.2 Current Equation (Linear Region)

The current is:

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

For small V_{DS} (where $V_{DS} \ll (V_{GS} - V_T)$), this simplifies to:

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

where: - μ_n = electron mobility ≈ 400–600 $cm^2/(V \cdot s)$ in silicon - C_{ox} = oxide capacitance per unit area ≈ 1–2 $fF/\mu m^2$ (process-dependent) - W/L = aspect ratio (width divided by length) - $(V_{GS} - V_T)$ = **overdrive voltage** (how much above threshold)

2.2.3 Equivalent Channel Resistance

The channel acts as a voltage-controlled resistor :

$$R_{channel} = \frac{V_{DS}}{I_D} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)}$$

Key observation: Channel resistance is **inversely proportional to overdrive voltage** .

- If $(V_{GS} - V_T) = 0.1$ V: $R_{channel} = \frac{1}{\mu_n C_{ox} (W/L) \times 0.1}$ (relatively high)
- If $(V_{GS} - V_T) = 0.3$ V: $R_{channel} = \frac{1}{\mu_n C_{ox} (W/L) \times 0.3}$ (3× lower)

2.2.4 Electrical Characteristics

- **Current:** Proportional to both V_{GS} and V_{DS}
- **Input Impedance:** Very high (gate is insulated by oxide)
- **Output Impedance:** Low to moderate (channel conducts)
- **Behavior:** Acts like a resistor controlled by gate voltage

2.2.5 Use in Analog Circuits

The linear region is used for: - **Analog switches:** Gate voltage determines ON/OFF and resistance - **Resistive loads:** Replacing passive resistors in precision circuits - **Gain control:** Varying resistance to vary signal path

Not typically used for amplification because current is sensitive to both V_{GS} and V_{DS}—unpredictable behavior .

Section 2.3: Saturation Region – The Transistor Acts Like a Current Source

Condition: $V_{GS} > V_T$ AND $V_{DS} \geq (V_{GS} - V_T)$

This is the **most important region for analog amplifier design** .

2.3.1 What's Happening Physically: Channel Pinch-Off

As drain voltage increases, something surprising happens: the channel doesn't get wider. Instead, it gets narrower .

Why? The potential rises from source to drain. At some point in the channel, the local potential reaches a value where the **local gate-to-channel voltage drops to the threshold voltage** .

At that location, the channel **pinches off**—the conductive layer narrows to nearly zero .

This pinch-off point moves toward the source as V_{DS} increases further .

Result: A **wedge-shaped channel**: thick near the source, tapers to zero at the drain .

2.3.2 Current Equation (Saturation Region)

Once pinched off, the current is determined almost entirely by the gate voltage :

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2$$

Critical observation: I_D depends **only on** V_{GS}, not on V_{DS} (beyond the saturation threshold) .

Doubling V_{DS} does not change the current. Increasing it by a factor of 10 barely affects the current .

This is the **nearly ideal current source behavior** that makes analog amplification possible .

2.3.3 Saturation Voltage Threshold

The boundary between linear and saturation regions occurs when :

$$V_{DS} = V_{GS} - V_T = V_{OV}$$

where V_{OV} is the **overdrive voltage**.

Practical interpretation: To enter saturation, the drain voltage must be at least equal to the overdrive voltage. For a transistor with $V_{GS} = 0.8$ V and $V_T = 0.4$ V:

$$V_{DS,min} = 0.8 - 0.4 = 0.4 \text{ V}$$

2.3.4 Channel Length Modulation (Real Devices)

In an ideal transistor, once in saturation, current would be completely independent of V_{DS} .

In real devices, the pinch-off point shifts slightly, changing the effective channel length L_{eff} .

This is captured by adding a factor :

$$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2[1 + \lambda V_{DS}]$$

where λ (lambda) is the **channel length modulation parameter**: typically 0.01–0.05 V^{-1} in modern processes .

What this means: Current increases slightly with V_{DS}, but the dependence is weak (1–5% per volt) .

For amplifier design: This weak dependence is acceptable, and we often neglect it in first-order calculations .

2.3.5 Electrical Characteristics

- **Current:** Nearly independent of V_{DS}; proportional to $(V_{GS} - V_T)^2$
- **Input Impedance:** Extremely high (gate is insulated)
- **Output Impedance:** Very high (nearly ideal current source)
- **Behavior:** Acts like a current source controlled by gate voltage

2.3.6 Use in Analog Circuits: This is Where Amplification Happens

All analog amplifiers operate in saturation .

Why? Because: 1. The current is nearly independent of output voltage (V_{DS}) 2. The input impedance is extremely high (no loading of previous stage) 3. The output impedance is very high (can drive high impedance loads)

Most critical property: Saturation makes the transistor a **voltage-controlled current source** .

A small change in gate voltage causes a proportional change in drain current:

$$\frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T) = g_m$$

This derivative is **transconductance** g_m—the key to understanding amplifier gain .

PART III: TRANSCONDUCTANCE – THE KEY TO AMPLIFICATION

Section 3.1: What is Transconductance?

Transconductance measures **how strongly the gate voltage controls the drain current** :

$$g_m = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}=\text{constant}}$$

Units: Siemens (S), or more commonly microSiemens (μS) for analog circuits .

Intuitive meaning: If you change the gate voltage by 1 mV, how much does the drain current change?

- If $g_m = 10$ μS: Drain current changes by 0.01 μA
- If $g_m = 100$ μS: Drain current changes by 0.1 μA
- If $g_m = 1000$ μS: Drain current changes by 1 μA

Higher g_m means stronger control—and stronger amplification .

Section 3.2: Calculating Transconductance in Saturation

In the saturation region, the current is:

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2$$

Taking the derivative with respect to V_{GS}:

$$g_m = \frac{\partial I_D}{\partial V_{GS}} = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)$$

This can also be written as:

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

Key insight: Transconductance increases with:

1. **Channel width W:** Wider transistors have more current capacity and higher g_m
2. **Smaller channel length L:** Shorter channels give higher transconductance
3. **Higher bias current I_D:** More current means stronger control
4. **Larger overdrive $(V_{GS} - V_T)$:** Gate voltage further above threshold gives higher g_m

Section 3.3: Transconductance in the Linear Region

In the linear region where $V_{DS} \ll (V_{GS} - V_T)$:

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T) V_{DS}$$

Taking the derivative:

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{DS}$$

Important difference from saturation: In the linear region, g_m depends on V_{DS} .

If you want constant g_m (for linear amplification), you must keep V_{DS} constant—another reason to use saturation operation .

Section 3.4: Transconductance and Amplifier Gain

The voltage gain of a common-source amplifier is directly proportional to transconductance :

$$A_v = -g_m \cdot R_L$$

where R_L is the load resistance .

This is the fundamental equation of analog amplifier design.

Implications:

1. **Higher g_m → Higher gain:** If you double g_m by redesigning the transistor or increasing bias current, gain doubles
2. **Load resistance matters:** A larger load resistor gives higher gain for the same g_m
3. **Gain is linear in g_m:** This is why transconductance is such an important design parameter

PART IV: BASIC MOSFET PARAMETER REVIEW

Section 4.1: Key Device Parameters

When designing with MOSFETs, several device parameters appear repeatedly in equations :

Parameter	Symbol	Typical Value	Unit	Meaning
Electron Mobility	μ_n	400–600	$cm^2/(V \cdot s)$	How fast electrons move in silicon
Oxide Capacitance	C_{ox}	1–3	$fF/\mu m^2$	Capacitive coupling through gate oxide
Threshold Voltage	V_T	0.3–0.5	V	Minimum gate voltage to form channel
Channel Length	L	28 nm–1 μm	μm	Length of conducting channel
Channel Width	W	0.1–100	μm	Width of conducting channel

Aspect Ratio	W/L	0.1–1000	—	Width divided by length (design lever)
Supply Voltage	V_{DD}	1.2–3.3	V	Power supply (process-dependent)

Section 4.2: How Process Technology Affects Parameters

Modern silicon processes come in nodes: 180 nm, 90 nm, 65 nm, 28 nm, 16 nm, 7 nm, 5 nm, etc.

Finer process nodes give:

- **Smaller minimum dimensions:** Smaller L and W
- **Higher C_{ox}:** Thinner oxide increases gate capacitance
- **Lower V_T:** Threshold voltage decreases
- **Lower V_{DD}:** Supply voltage decreases to avoid overstress

Example: 28 nm Process - V_{DD} = 0.9–1.2 V (low power) - μ_n ≈ 200–300 $cm^2/(V \cdot s)$ (reduced by short-channel effects) - C_{ox} ≈ 2–3 $fF/\mu m^2$ (high) - V_T ≈ 0.3–0.4 V (lower)

Design consequence: Smaller processes offer more circuit density but less voltage headroom, making design more challenging .

PART V: PRACTICAL DESIGN EQUATIONS

Section 5.1: The Saturation Current Equation (Most Important)

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2$$

What to use it for: - Calculating drain current for a given gate voltage - Sizing transistors to meet a current specification - Determining bias point for a circuit

Rearranged to solve for aspect ratio:

$$\frac{W}{L} = \frac{2I_D}{\mu_n C_{ox} (V_{GS} - V_T)^2}$$

Use this when you know: - Required drain current I_D - Gate voltage you want to use V_{GS} - And you need to find the transistor width and length ratio

Section 5.2: The Transconductance Equation

In saturation:

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)$$

Or equivalently:

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

Use this to: - Calculate amplifier gain: $A_v = -g_m R_L$ - Determine transconductance for a given operating point - Understand trade-offs between overdrive voltage and current

Section 5.3: The Linear Region Equation

$$I_D = \mu_n C_{ox} \frac{W}{L} \left[(V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} \right]$$

Use this when: - Transistor is used as a switch or variable resistor - You're designing analog multiplexers or sample-and-hold circuits - Linear behavior with small output swing is required

Section 5.4: The Channel Resistance Equation

$$R_{channel} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)}$$

Use this for: - Calculating switch resistance in analog switches - Understanding on-resistance of transmission gates - Designing resistive loads (replacing passive resistors)

PART VI: PRACTICAL EXAMPLE – DESIGNING A SIMPLE AMPLIFIER

Section 6.1: Problem Statement

Design a common-source amplifier with the following specifications:

- **Required voltage gain:** $A_v = -20$ V/V (26 dB)
- **Load resistance:** $R_L = 100$ kΩ
- **Supply voltage:** $V_{DD} = 1.2$ V
- **Power budget:** Max 10 µW
- **Technology:** 28 nm CMOS process

Given process parameters: - $\mu_n C_{ox} = 200$ µA/V^2 (28 nm process) - $V_T = 0.35$ V (typical) - Minimum $L = 30$ nm = 0.03 µm

Section 6.2: Step 1 – Calculate Required Transconductance

From gain equation:

$$g_m = \frac{A_v}{R_L} = \frac{20}{100 \times 10^3} = 0.2 \text{ mS} = 200 \text{ µS}$$

Section 6.3: Step 2 – Calculate Required Bias Current

For saturation region, let's assume reasonable overdrive:

$$V_{GS} - V_T = 0.2 \text{ V}$$

Then:

$$g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)$$

$$200 \times 10^{-6} = 200 \times 10^{-6} \times \frac{W}{L} \times 0.2$$

$$\frac{W}{L} = \frac{200 \times 10^{-6}}{200 \times 10^{-6} \times 0.2} = 5$$

Alternative approach: Use the square-root relationship:

$$g_m = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$$

$$200 \times 10^{-6} = \sqrt{2 \times 200 \times 10^{-6} \times 5 \times I_D}$$

Solving for I_D:

$$I_D = \frac{(200 \times 10^{-6})^2}{2 \times 200 \times 10^{-6} \times 5} = \frac{4 \times 10^{-11}}{2 \times 10^{-3}} = 20 \text{ µA}$$

Section 6.4: Step 3 – Verify Power Budget

Power dissipation:

$$P = I_D \times V_{DD} = 20 \times 10^{-6} \times 1.2 = 24 \text{ µW}$$

This exceeds our 10 µW budget. We must **reduce bias current** and **increase aspect ratio**:

Let's try $I_D = 10$ µA:

$$\frac{W}{L} = \frac{g_m^2}{2\mu_n C_{ox} I_D} = \frac{(200 \times 10^{-6})^2}{2 \times 200 \times 10^{-6} \times 10 \times 10^{-6}} = 10$$

New power:

$$P = 10 \times 10^{-6} \times 1.2 = 12\ \mu\text{W}$$

Still slightly high. Try $I_D = 8$ µA:

$$\frac{W}{L} = \frac{(200 \times 10^{-6})^2}{2 \times 200 \times 10^{-6} \times 8 \times 10^{-6}} = 12.5$$

Power:

$$P = 8 \times 10^{-6} \times 1.2 = 9.6\ \mu\text{W}$$

✓ **Within budget**

Section 6.5: Step 4 – Calculate Gate Voltage

$$I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2$$

$$8 \times 10^{-6} = \frac{200 \times 10^{-6}}{2} \times 12.5 \times (V_{GS} - 0.35)^2$$

$$(V_{GS} - 0.35)^2 = \frac{8 \times 10^{-6} \times 2}{200 \times 10^{-6} \times 12.5} = 0.0064$$

$$V_{GS} - 0.35 = 0.08\ \text{V}$$

$$V_{GS} = 0.43\ \text{V}$$

Section 6.6: Step 5 – Determine Actual Dimensions

With $L = 30$ nm (minimum) and $W/L = 12.5$:

$$W = 12.5 \times 30\ \text{nm} = 375\ \text{nm}$$

Design Summary: - Width: 375 nm - Length: 30 nm (minimum) - V_{GS} = 0.43 V - I_D = 8 µA - g_m = 200 µS - Expected gain: $A_v = -g_m R_L = -200 \times 10^{-6} \times 100 \times 10^3 = -20$ V/V ✓ - Power consumption: 9.6 µW ✓

PART VII: SUMMARY TABLE – EQUATIONS AT A GLANCE

Situation	Equation	When to Use	What You Get
Current in Saturation	$I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2$	Finding current for given voltage	Drain current I_D
Transconductance (Sat.)	$g_m = \mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)$	Finding control strength	Voltage-to-current conversion
Amplifier Gain	$A_v = -g_m R_L$	Finding voltage gain	Amplifier gain in V/V
Sizing (Saturation)	$\frac{W}{L} = \frac{2I_D}{\mu_n C_{ox}(V_{GS} - V_T)^2}$	Finding W/L for required current	Aspect ratio for design
Channel Resistance	$R_{ch} = \frac{1}{\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_T)}$	Finding on-resistance	Switch/resistor value
Current (Linear)	$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_T)V_{DS} - \frac{V_{DS}^2}{2}\right]$	Switch or variable resistor	Triode region current
Power	$P = I_D \times V_{DD}$	Verifying power budget	Total dissipated power

PART VIII: COMMON BEGINNER MISTAKES

Mistake 1: Using Linear Region Equations in Saturation

Wrong: Assuming $I_D = \mu_n C_{ox}\frac{W}{L}V_{DS}$ when transistor is in saturation

Correct: Use $I_D = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_T)^2$ in saturation

Why: In saturation, current is nearly independent of V_{DS}. Linear equation gives incorrect results .

Mistake 2: Forgetting the Threshold Voltage

Wrong: Assuming $V_T = 0$ (then gate voltage of 0.1 V seems large)

Correct: Always subtract V_T (typically 0.3–0.5 V) from V_{GS}

Impact: In 28 nm with $V_T = 0.35$ V and $V_{DD} = 1.2$ V, you only have 0.85 V of "headroom" for analog design—much tighter than 5V processes .

Mistake 3: Confusing Gain Equation Direction

Wrong: Using $A_v = g_m R_L$ for PMOS (gives positive gain)

Correct: Using $A_v = -g_m R_L$ for NMOS (gain is negative, inverted)

Why: NMOS drains current when gate goes high, while load resistor pulls voltage up. This inversion is captured in the negative sign .

Mistake 4: Operating in Linear Region for Amplification

Wrong: Trying to build an amplifier with small V_{DS}

Correct: Always operate in saturation for analog amplification

Why: In linear region, current depends on both V_{GS} and V_{DS}. Output swing changes current, causing distortion .

Mistake 5: Ignoring Body Effect in Circuits

Wrong: Assuming all transistors have the same V_T regardless of substrate voltage

Correct: Recognizing that V_{BS} changes V_T in cascode and other complex topologies

Impact: In differential pairs, $V_{BS} = 0$ for both transistors (matched). In cascode, upper transistor has $V_{BS} \neq 0$ (mismatched) .

PART IX: SUMMARY AND KEY TAKEAWAYS

The MOSFET in Analog Circuits – Core Concepts

1. **The MOSFET is a voltage-controlled current source in saturation**
    - Small changes in gate voltage cause proportional changes in drain current
    - This enables amplification
2. **Three operating regions have different properties**
    - **Cutoff:** OFF, tiny current (leakage only)
    - **Linear:** Acts like variable resistor, current sensitive to output
    - **Saturation:** Acts like current source, current independent of output
3. **Saturation is the region for analog amplifiers**
    - Current depends only on V_{GS}, not V_{DS}
    - Provides gain and signal amplification
4. **Transconductance is the key parameter**
    - $g_m = \partial I_D / \partial V_{GS}$

- Determines amplifier gain: $A_v = -g_m R_L$

5. **Basic equations predict behavior**
   - Saturation current: $I_D = \frac{\mu_n C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2$
   - Transconductance: $g_m = \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_T)$
   - These are surprisingly simple and surprisingly useful
6. **Device parameters vary with process technology**
   - Newer processes have lower V_T, higher C_{ox}, lower V_{DD}
   - Design equations remain the same, but numerical values change
7. **Design is about choosing the operating point**
   - Pick desired gate voltage V_{GS}
   - Calculate required aspect ratio W/L
   - Verify power and other specifications