FLOOR PLAN

1. What checks you do as soon as you get the Netlist before moving the Floor plan?

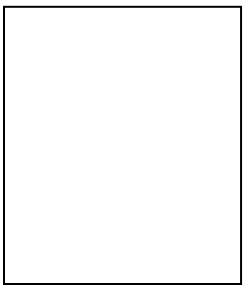
1) Netlist uniqueness
2) Assignment statements
3) Setup timing check
4) SDC constraints (Clock frequency, uncertainty margins, exceptional paths list(false, multi cycle)
5) Multi driven nets
6) No inputs pins/ports/nets should be floating
7) No clock buffers, inverters, hold delay cells
8) Scan stitched
9) All are scan flops
10) No un driven pins
11) No nets connected directly from pads to standard cells
12) Feed through buffers are there or not

2. How the IO pad arrangement will be done

Depending on the

1. Signals coming direction in the board
2. Grouping based on the domain like Analog, Digital
3. Uniform distribution of the power pads based on the ESD and SSO.

3. Red color region shows the routing congestion module inside the chip. What is the reason?



1) Placement density
2) Pin density due to high fan in cells like AOI,OAI
3) Macros/Standard cells might have used the all the metal layers inside and no routing resources.
4) Placement of cells might not have been placed in the logical connectivity order
5) Around this region more number of macros placed
6) Power straps and clock network might have used more routing resources

4. How will you avoid the congestion?

1. Change the floor plan (macros placement, macros spacing and **pin orientation**) such that cells will be distributed uniformly

2. Introduce the placement density screens and placement blockage (block halos)
3. Logic optimization if possible
4. Module constraints like fence, region and guide.
5. Increase the number of metal layers, core area

5. What is the die size if standard cell are is $3mm^2$ and macro are is $2mm^2$?

First decide whether it is pad limited or core limited design.

1) Pad limited ,

Width, Height = pad width x Number of pads on each side + Pitch x (Number pads on each side-1)

2) Core limited,

Core area = (Macro area+ standard cell area)/Target cell utilization
Get H, W from aspect ratio.
Chip Width, Height = Core Width, height + Core ring width

6. On what basis will you place the macros?

1. IP guide lines
a. Sensitive blocks (PLL,ADC,DAC, touch screen) should be placed far from high frequency blocks and high frequency IOs
b. High power consumption(HOT) IPs (DCDC (*domain controller*-to-*domain controller),LDO(load drop out) regulator) placed far from sensitive blocks*
2. IO pads arrangement (to decrease RLC, Noise, IR drop)
3. Connectivity (macro to IO, macro to macro, macro to standard cells, critical paths)
4. Macro alignment and orientation is correct, and pins are on the edges that you expect. Make sure pins get connected with the **default routing** direction directly without vias
5. All macros are placed in the core area.
6. Macros do not overlap, or have very little overlap between them.
7. Macros match the module locations, or they are physically located with similar macros to minimize connectivity.
8. Macro grouping is correct.
9. There is enough spacing between macros to avoid congestion.
Note: You might want to restrict logic cells from being placed between macros to avoid routing congestion, but still allow nets to be buffered using this area.
10. Guides have the correct relative locations.
Note: Designer knowledge should always take precedence over any recommended guidelines.

Macro to Macro spacing deciding factors:

1. Pin density
2. Number of metal layers
3. Routing pitch

7. What are constraints you consider for floor planning of Standard Cells?

Generally standard cells will not be floor planned but can be shaped and placed as required with fence, region and boundary constraints along with target/effective utilization factor.

8. What parameters (or aspects) differentiate Chip Design & Block level design??

1. IO pads
2. Meeting the timing at block as well as at chip for block level design. Correlation depends on the timing budget accuracy.
3. Getting the afresh time budget SDC at particular stages like Floor plan, post placement, post CTS and post routing.
4. Making sure block power nets and IO pins match while hierarchy assembling (by providing LEF).
5. Providing the .lib, Clock Macro model for assembly.
6. Need to do any fix (timing/non timing) in block level.
7. Gate count

9. Differentiate between a Hierarchical Design and flat design?

Hier

- No effective optimization at boundaries
- Effective High gate count chips
- Design reuse
- Tools can handle design complexity easily

10. Flip Chip I/O

Flip Chip, the direct electrical connection of face down (hence "flipped") electronic components onto the substrate, with benefits in comparison with the non-CUP wire bond as follows:

• Reduce the required board area.

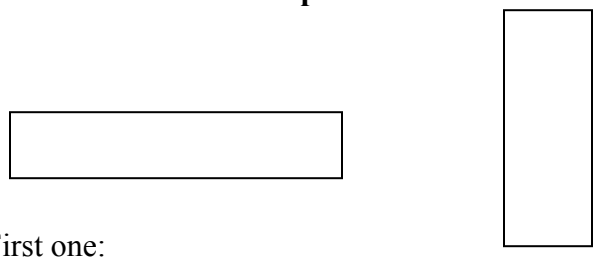
• Reduce the inductance and capacitance of connections and shortens the path, greatly improving the accuracy of impedance control.

• Provide excellent heat dissipating channel by using bumps.

11. What Floor plan checks do you do to freeze?

1. IO timing
2. Macro to macro timing
3. Macro to standard cell timing with margin. How much margin
4. IR drop analysis ,how much margin

12. In which metal do you prefer the Io pins for block? How many metal layers (HVH) will you select for the below shaped blocks?



First one:

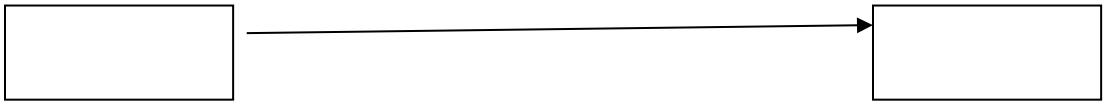
M1-M5 because we will have 3 horizontal metal layers.

Second one

M1-M6 because we will have 3 vertical metal layers.
North and south pins should be in vertical metal layers (M2,4,6).
East and west pins should be horizontal metal layers (M1,3,5)

13. How much space/area do you take while doing floor plan if 8x32 bit bus talking from one macro to another macro?

5 M, Horizontal= M1, M3, M5
Vertical= M2, M4
M2 pitch= 0.28
Cell Height =0.54



Routing space =8X32x0.28/2

"2" is because 2 layers can used on average of out of 3 layers. M1 mostly will be used in standard cells and M5 used for global connects.

Interconnect lengths are more. So, need to add buff/inv .If 2 cells per net,

Total cells= 8x32x2= 512 cells
Area = 512x(3x0.28)x0.54 ,extrapolated this value because buffers are not used all at the same location.

Placement

1. How do you calculate the core ring width?

1. Core current requirement

2. Current carrying capability/maximum current density (Jmax) of the metal

2. How you deal with the congestion after placement? When will you ignore and What basis? Is trail rout will try to route with the shortest path?

0.5% and 1.0% of Congestion for okay for 3 M and 5M correspondingly.

3.**What are the advantages and disadvantage of Dcap cells?**

Advantages

1) Stable voltage (acts as a local source) between power and ground when signal nets switch.

2) This can reduce IR drop for power nets and limit bouncing on ground nets.

Disadvantages:

1) Consumes chip area as they are big in size

2) Leakage power consumption

3) Performance degradation in terms of timing

<u>IR Drop:</u>

- IR drop is a signal integrity effect caused by wire resistance and current draw off of the power and ground grids. If the wire resistance is too high or the cell current larger than predicted, an unacceptable voltage drop may occur.
- This voltage drop causes the supply voltage to the affected cells to be lower than required, leading to larger gate and signal delays that can consequently cause timing degradation in the signal paths as well as clock skew.

- Lowered power supply current due to IR voltage drop also reduces the noise margins and compromises the signal integrity of the design.

4. What are the general power margins?

5 % of both VDD and GND

5. How will you decrease the voltage drop?

Dynamic

1. De caps
2. Clock gating
3. Gate level power optimization (cell sizing, buffer insertion instead of high drive strength)
4. voltage scaling
5. Multi VDD
6. Frequency scaling, Reducing the frequency of operation using pipelining
7. Async design techniques
8. Reducing number of transitions, eg. using grey coding

Static

1. Multi Vt Cells
2. Power gating
3. By applying a reverse bias voltage to the sub- strate, it is possible to reduce the value of the term (VGS-VT), effectively increasing VT. This approach can reduce the standby leakage by up to three orders of magnitude. However, VTCMOS (variable threshold CMOS) adds complexity to the library and requires two additional power networks to separately control the voltage applied to the wells. Unfortunately, the effectiveness of reverse body bias has been shown to be decreasing with scaling technology.
4. High K gate oxide
5. The Stack Effect, or self-reverse bias, can help to reduce sub-threshold leakage when more than one transistor in the stack is turned off. This is primarily because the small amount of sub-threshold leakage causes the intermediate nodes between the stacked transistors to float away from the power/ground rail. The reduced body-source potential results in a slightly negative gate- source drain voltage. Thus, it reduces the value of the term (VGS-VT), effec- tively increasing VT and reducing the sub-threshold leakage
6. Long channel devices but low dynamic current leads to reduced performance

6. During power analysis, if you are facing IR drop problem, then how did u avoid?

Dynamic IR drop:

a. By adding Decap Cells

Static IR drop:

1. Increase the width of power straps
2. Do the routing in the top metal layers
3. Increase the number of power pads
4. Place more power consuming macros near to the IO power pad

7. IR Drop effects:

1. Delay performances due to less slew rate
2. Noise margins will decrease
3. More susceptible to noise

8. During power analysis, if you are facing IR drop problem, then how did you avoid?

1. Increase power metal layer width.
2. Go for higher metal layer.
3. Spread macros or standard cells.
4. Provide more straps.

9. How to reduce the power /ground Bounce?

1. Wide width metal
2. Top metal layers (low resistivity)
3. Multi cut Vias
4. Placing near power pads
5. Decap cells

10. How you fix the EM violations?

1. Widen the metal
2. Metal slotting

Some Steps to Minimize Electromigration :

- Wider Wire Decreases current density and hence decreases electromigration.
- Length of the wire less then “BLECH LENGTH” decreases electromigration.
- Vias should be organized such that the current flow is uniformly distributed.

- Bends of interconnects should be avoided at 90 degrees because the current density is more at 90 degrees than at oblique angles.
  Use the taper circuits than high drive strength cells

11. Clock gating:

On using false path on enable I will say be very careful and this is fine for global on/off signal for which you don't care when they occur, for thing that need to be cycled accurate (typically controlling write to config register, internal memories, ...) this is the best way to end up with gate level simulation not matching your functional simulation despite the fact that your formal equivalency pass!! Ever been beaten by that one due to the clock latency making your enable being seen one cycle too late?

12. If in your design has reset pin, then it'll affect input pin or output pin or both?

Output pin**.**

14. Why order of filling is form more width filler cells to low width filler cells?

It forms the wide metal due to continuous placement of low width filler cells. Creates Metal slotting rule violation.

The CMP damascene process also introduces undesirable side effects, including dielectric erosion and metal dishing.

Please always insert fat fillers first and then thin fillers afterwards. To avoid the metal-slot-rule violation, please do not only use thin filler cells to fill large I/O spacing. For example, use one 20um pitch filler cell (PFILLER20) and one 10um pitch filler cell (PFILLER10) instead of using 6 "5um pitch" filler cells (PFILLER5) to fill 30um spacing. In addition, if spacing is larger than one cell pitch, please first insert core power cell PVDD1DGZ/CDG and I/O power cell PVDD2DGZ/CDG. Then insert filler cells to fill up the rest of spacing for ESD robustness.

15. Why filler cell are uesd? Why we need fill in descending order of filler cell size?

To have well, substrate continuity.

16. What is Amoeba placement? What its use?

The amoeba view to see the placement of modules and blocks. We can analyze module boundaries and whether the cell placed closed or not. So that we can refine the placement as pet the requirement.

17. Why is power planning done and how? Which metal should we use for power and ground ring & strips and why?

1. Provide the foundation for hooking up each cell to a power source.
2. To supply sufficient current/power/voltage to the chip
    1. To have less IR drop
3. To avoid the EM

Top metal layers because of the low Rs.

18. How to do Congestion optimization?

1. Change the floor plan (macros placement, macros spacing and **pin orientation**) such that cells will be distributed uniformly
2. Introduce the placement density screens and placement blockage (block halos)
3. Logic optimization if possible
4. Module constraints like fence, region and guide.

19. Can I add Spare cells instead of filler cells? So that we can have many for ECO.

No because

(1) More static power consumption of the spare cells compared to filler cells

(2) Spare cells are not available in all sizes.

20. Can I use number of FILL1 cells where I can use FILL32/64?

No because

i) Metal slot problems will come.

ii) Dishing

iii) Erosion

21. 1 high drive strength cell equal to 5 buffers. Which one will you choose?

5 buffers because taper circuit is effective in terms of delay but may not be the area/power effective circuit.
It is essential to not to use single input high drive strength cell by itself. It would potentially cause a large current and cause critical EM failure. Designer can remove ‘don’t use’ attribute to drive high fan out from LIB if they are careful enough to avoid EM issues.

22. What is the difference between the prototype and timing driven placement?

23. Could you place the standard cells in Core to IO region?

NO because

1. Need to create the core rows to place, extend the follow pins
2. DRC violations occurs (Nwell connectivity)
3. Need filler cells
4. Will be very near to IO pads which will should be away from the high frequency and ESD

24. Why standard cell width is integer multiples of M2 pitch?

To get maximum metal routing tracks on top of standard cell. Standard cell pins are aligned to the M2 routing grid.

25. Why to fix DRVs ? How you fix DRVs ?

We need to fix DRV even though the timing met because the cell characteristics will be unpredictable with DRV violations.
Max transition violations will be fixed –By adding the repeater which

1. Boosts the signal strength
2. Increases the slew rate

Max cap will be fixed by cloning, adding buffer

26. How much placement density allowed at floor plan stage-

65 to 75% is allowed. Some cases I worked on the chip which had 75% at Floor plan and 85% at the end.

CLOCK TREE SYNTHESIS

1. Generally in which stage will you find the clock gating violations? Why in that stage?

Post CTS stage because skew control between the clock gated and no clock gated cells is difficult.
Clock gated path takes more path delay compared to no clock gated path.
CGC type depends on the pos edge/neg edge triggered flip flop.

Advantages:

1. Less Power dissipation
2. Decrease in area overhead compared to synchronous clock enable methodology

2. Drawbacks of clock gating technique

1. You could get some glitches in the gated clock if clock gating was not done properly. Which could cause severe problems
2. Synchronization (skew balancing). In fact gated and not gated circuits are not clocked at the same time because of the delay overhead introduced by the circuit responsible of gating the clock.
3. Overhead in design, verification and silicon area.

3. What are the synchronous and asynchronous clocks?

Synchronous clocks: Same source or constant phase difference (main clocks and generated clocks)
Async'hronous clocks: Different clock sources or no constant phase difference
A clock domain is defined as that part of the design driven by either a single clock or clocks that have constant phase relationships. A clock and its inverted clock or its derived divide-by-two clocks are considered a clock domain (synchronous).
Conversely, domains that have clocks with variable phase and time relationships are considered different clock domains.

4. How the clock uncertainty will be considered as a skew in ctstch file? What are the components and source of uncertainty?

The clock uncertainty include/components: jitter (PLL), clock skew (before CTS), OCV (before post-routing), guard margin.

Sources:

1. PLL or clock generator
2. Process variations
3. Load mismatch
4. Different width and length clock nets
5. Coupling capacitance/Cross talk
6. Power supply Variations

Post CTS: Uncertainty will be decreased in SDC. Clock skew (including the OCV) target will be given in ctstch.eg:
A 1 ns clock with a 100 ps clock uncertainty means that the next clock tick will arrive in 1 ns plus or minus 50 ps.

Setup uncertainty should include all of them (capture clock and launch clock are different) but we can ignore PLL jitter in hold uncertainty (capture clock and launch clock are same), and OCV uncertainty for hold can be less than setup.

5. Why are we not checking the hold before CTS?

Setup violations are checked before CTS, while hold violations are checked after CTS. This is because positive clock skew helps setup. So if setup is cleared before CTS with an estimated skew, then mostly setup will be clear with the actual value of skew calculated after CTS. However, in hold analysis, skew increases the minimum logic delay required in the path. Since it works against hold, hold analysis is performed after CTS when an accurate value of skew is known.
Fixing hold is easy compared to setup. Cell density (Unnecessarily data paths) may increase if we keep fixing from pre CTS stage itself.

6. What is the difference between through pin, leaf pin and exclude pin?

The clock tracing stops at
A clock pin/sink pink
An asynchronous set/reset pin
An input pin without any timing arc to an output pin
A user-specified leaf pins or excluded pin
CTS does not trace through gates, because NoGating rising is specified, but the skew is balanced

7. What are the inputs given while CTS and which are important in order?

1. Well floor planned and Placed design
2. Module Placement Utilization (which contains the clock nets is set to 5–7 percent less than the desired final chip utilization (placement density). This provides placement resources for adding clock buffers during CTS)
3. Clock Designs with Tight Area, use the Specify Cell Padding form (Place – Specify – Cell Padding) to create placement resources near clocked flip-flop cell types.
4. Balancing Pins for Macro Models CTS can balance a pin of a macro model. These macro models are user specified. CTS balance the phase delay of all leaf pins in the clock tree, including leaf pins of macro models. The timing models for macro models are defined in the clock tree specification file Macro Model statement.
5. Timing Model Requirement for Cells Make sure that all cells have a timing model. If a cell does not have a timing model, CTS will not trace through the gate, and may set the gate's input pin as a leaf pin.

6. Delay Variation and OCV (setAnalysisMode and setTimingDerate commands).
7. Cts tch file
    a. Non Default Rules (NDR) (extra spacing, shielding)
    b. Routing layers
    c. Clock root pins
    d. Max/Min delay (clock latencies)
    e. Skew
    f. Sink/Buffer transition
    g. Cells to be used while doing CTS
    h. Routing while CTS
    i. Leaf pins, exclude pins, through pins
    j. Clock grouping
    k. Macro models

8. Can we have latency/ insertion delay more than clock period?

We cannot because the data will be missed without capturing.

9. Why clock buffers and inverts should have equal rise and fall times?

1. To maintain minimum clock pulse width
2. To have timing margin for the both negative and positive edge triggered flip flops i.e for half cycle paths
3. They have higher max_cap value

Disadvantages:

1. Occupies more area
2. More power consumption
3. More delay compared the normal buffers

9. How CPPR will analyze for half Cycle paths?

CPPR /CRPR will not depend on half /full cycle path.

10. In which paths mainly will you see the violations at post CTS stage?

Paths related to IO like Input to Reg , Reg to output and in to out (if max_delay is not used).

12. Why scan re ordering is required?

1. To save the routing resources
2. Easy timing closure for setup time
3. IR drop/power consumption can be decreased

13. What are the changes between the pre CTS and post CTS?

1. Clock propagation
2. Uncertainty values
3. IO delays
4. Disable timing constraints, False paths if timing violations occurs

14. How to decrease the clock skew and insertion delay?

To minimize the clock skew and clock latency, designers may find the following recommendations helpful. It must be noted that these recommendations are not hard and fast rules. Designers often resort to using a mixture of techniques to solve the clocking issues.

15. How will you decrease the latency and skew?

Latency:

1) Use the minimum clock level with balanced clock branches
2) Widen the wire width from the source to first clock buf/Inv
3) Use high drive strength cells
4) Use Inverters instead buffers
5) Library study- cells which have minimum delay ex: use cells which have less delay for rising signals for positive edge triggered flops
6) By grouping the flops in the same domain

Skew:

1) Balanced clock tree by cloning
2) By clock grouping
3) Mix of drive strength cells
4) Ability to trap from any level (clock gating vs not clock gating)
5) By synthesizing the separate clock tree for the generated clocks
6) Widen the wire

Discussed elaborately below:

1. Use a balanced clock tree structure with minimum number of levels possible. Try not to go overboard with the number of levels. The more the levels, the greater the clock latency.

2. Use high drive strength buffers in large clock trees. This also helps in reducing the number of levels.
3. In order to reduce clock skew between different clock domains, try balancing the number of levels and types of gates used in each clock tree.For instance, if one clock is driving 50 flops while the other clock is driving 500 flops, then use low drive strength gates in the clock tree of the first clock, and high drive strength gates for the other. The ideas here is to speed-up the clock driving 500 flops, and slow down the clock that is driving 50 flops, in order to match the delay between the two clock trees.
4. If your library contains balanced rise and fall buffers, you may prefer to use these instead. Remember, in general it is not always true that the balanced rise and fall buffers, are faster (less cell delay) than the normal buffers. Some libraries provide buffers that have lower cell delays for rise times of signals, as compared to the fall times. For designs utilizing the positive edge trigger flops, these buffers may be an ideal choice. The idea is to study the library and choose the most appropriate gate available. Past experience also comes in handy.
5. To reduce clock latency, you may try to use high drive inverters for two levels. This is because, logically a single buffer cell consists of two inverters connected together, and therefore has an cell delay of two inverters. Using two separate inverters (two levels) will achieve the same function, but will result in reduced overall cell delay – since you are not using another buffer (2 more inverters) for the second level. Use this approach, only for designs that do not contain gated clocks. The reason for this explained later (point h).
6. Do not restrict yourself to using the same type and drive strength gate for CTS. Current layout tools allow you to mix and match.
7. For a balanced clock tree (e.g., 3 levels), the first level is generally a single buffer driven by the Pad. In order to reduce clock skew, the first level buffer is placed near the center of the chip, so that it can connect to the next level of buffers, through equal interconnect wires. This creates a ring like structure with the first buffer in the center, with the second set of buffers (second level) surrounding it, and the last stage surrounding the second level. Thus, the distance between the first, second and the third level are kept at minimum. However, although a good arrangement, it does result in the first level buffer being placed farthest from the source (Pad). If a minimum size wire is used to route the clock network from the Pad source to the first buffer, it will result in a large RC delay that will affect the clock latency. Therefore, it is necessary to size-up (widen) this wire from the Pad source to the input of the buffer (first level), in order to reduce the resistance of the wire, thereby reducing the overall latency.Depending upon the size of your design and the number of levels, you may also need to perform this operation on other levels.
8. In order to minimize the skew, the layout tool should have the ability to tap the clock signal, from any level of the clock tree. This is especially important for designs that contain gated clocks. If the same clock is used for other ungated flops, then it results in additional delay, hence the skew.If the clock tree ended at the gate, the additional delay will cause a large skew between the gated-clock flop and the ungated-clock flop as shownin Figure 9-1 (a). Therefore it is necessary to tap the clock source from a level up for the gated-clock flop, while maintaining the full clock tree for the ungated clock flop, as illustrated in Figure 9-1 (b).

However, if inverters are used in the clock tree (point e), then the above approach breaks down. In this case, do not use inverters as part of the clock tree.

- Clock skew can be minimized by proper routing of clock signal (clock distribution tree) or putting variable delay buffer so that all clock inputs arrive at the same time

  - Local skew.
  - Clock skew occurring between two adjacent clock storage elements.
  - Global skew.
  - Maximal difference between two clock signals reaching any of two storage elements on the chip.

16 .How you control the OCV in clock paths

Try to have the more common path than individual path from the divergence clock tree point. So that CPPR/CRPR will decrease the OCV effect.

17. What is the advantage of the clock mesh structure?

1) used for high frequency clocks
2) less than 1ps skew can be achieved

18. Will you use the buffers or inverters for CTS and why?

Inverter:

1. Less area
2. Less power (dynamic as well as leakage current)
3. Less prone to OCV (process variation) due to less number transistors
4. Less delay, skew reduction because on less insertion delay because of the less inverter delay compared to buffer delay
5. Clock phase corrections can also be achieved by buffers
6. Inverts in the Buffer will see the different loads. First inverter sees the load of only 2d Inverter but 2nd inverter sees the load of receiver and interconnect.

19. What are the NDR (Non Default Rules) used for the clock tree?

1. Double spacing or extra spacing
2. Shielding

20. Which metal did you use for the clock tree routing?

Next lower layer to the top two metal layers (global routing layers).
Because it has less resistance hence less RC delay.
Cobra : (5M)
Top Preferred Layer 5
Bottom Preferred Layer 2
Crinmson: (7M2T) Top Preferred Layer 4
Bottom Preferred Layer 3

21. What CTS Specifications contains?

Skew Balancing:

1. Give tight skew constraint
2. Relax latency
3. Place the clock source in the centre if possible
4. Synthesize the separate clock tree for the generated clocks
5. Balance the load by cloning/buffering
6. For lengthy nets add buffers and increase the drive strength of the driver
7. Use clock buffers and inverts which has symmetrical rise and fall times
8. Use more inverters
9. Clock grouping for inter clock domain crossing

22. What are the pros & cons of switch "RouteClkNet"?

When we generate the cts spec file. There is a option in each clock root called Routeclknet. If you click Routeclknet option – yes
Clock routing has been done on that specific clock during CTS stage using nanoroute. Its Important to have a proper clock sequence so that critical clock will route first so that it will get the complete routing resource.
If you click Routeclknet option – No
Routing of the clock net will be done along with the data path routing.

23. Does order of clocks in CTS clock specification file affect quality of results?

yes

24. User is running CTS to synthesize multiple clock trees. Does quality of results depend on the order in which the clocks are defined in the specification file?

Solution

The quality of results depends on the flow being used to synthesize the clock trees

Flow1:
=====

If user builds clock trees in a serial manner using multiple clock specification files, then the sequence in which the clocks are built does affect quality of results.

This is because after the first clock is built, the buffers and flip-flops which are part of this first clock tree are marked as "FIXED". Hence when the refinePlace step is run as part of the second clock synthesis run, it cannot move the buffers and flip-flops which were added as part of the first clock tree.

So when clock trees are built in a serial fashion, the sequence at which the trees are build does affect results.

Flow2:
=====

If the multiple clocks are part of one CTS specification file, CTS determines the clock topology one clock at a time and builds the clock tree in a serial manner. This may result in overlaps between the buffers added for the different clock trees and the flip-flops.

To resolve these overlaps, CTS calls refinePlace at the end to legalize the placement. This step uses some weighting when determining where to move the cells so as to remove the overlaps.

So if multiple clocks are part of the same specification file, the order in which the clocks are defined does not affect results.

However there is an exception if crossover clocks are involved.

If there are cross-over clocks, it is recommended to have the cross-over clocks be specified in the specification file in order of increasing skew.

For example, if the specification file contains 3 clocks, ClkA, ClkB and ClkC, with ClkA and ClkB being crossover clocks, and the skew constraints being 200ps 300ps and 100ps respectively, then the order in the clock specification file should be:

ClkC

ClkA # Cross-over clock ClkA should be specified before ClkB

ClkB

Summary:

=======

The recommendation when building multiple clock trees is to use Flow #2. However if a design contains multiple clocks where the zones of the clock trees overlap, and one particular clock is very critical, it may help to first synthesize the critical clock by itself. The remaining clocks can then be synthesized next using Flow #2.

29. What is a difference between Clock Tree & Reset Tree?

There is a major difference between Clock Tree & Reset Tree - in regards to correct design practices.

1. Clock Tree must always be 'Skew Balanced' to avoid synchronous skips & races.
2. Reset Trees - especially for those cases where the Reset is Asynchrounous - MAY not be 'Skew Balanced' (in most of the times).
3. Reset Tree can be MORE loaded than Clock Tree - e.g. - a relaxed DRC rule cab be set for Reset Tree - since Flip-Flops unstable behavior is less sensitive for slow slew rates in the Reset input (while the Clock input is).
4. Some ppl consider synchronizing the Reset input signal with the main System Clock. While this is a correct practice to avoid Metastability at the trailing edge of Reset, some skew problems may arise. For those cases, carefull STA must be run to alert the designer.

Clock skew is related to chip speed while reset is not. Clock tree may set to 300ps skew with 500 ps transition time while reset may only require 1000/1000.
You need a Reset Tree to reduce heavy load. But Skew requirements for reset trees are almost non-existent for Asynchronous Resets!

30. What is Static and Dynamic Clock Uncertainties?

Clock uncertainties can be classified as static or dynamic. Static uncertainty does not vary or varies very slowly with time. Process variation induced clock uncertainty, clock skew is such an example. On the other hand, dynamic uncertainty varies with time. Dynamic power supply induced delay variation, clock jitter is an example of a dynamic uncertainty.

Sources of static clock uncertainties are:
1. Intentional or unintentional design mismatches
2. On-die process variations
3. Loading variations (mismatch) at the intermediate or final stage of the clock distribution

Clock uncertainties Sources

Static (skew)
Intentional or unintentional design mismatches
On-die process variations
Final or intermediate loading variations

Dynamic (jitter)
Voltage droop and dynamic voltage variations
Temperature gradient due to activity variations

31. what is Hold Time Skew

The big difference between the setup and hold time case is that the hold time skew refers to the same clock edge. In this case, the PLL jitter and the common path delays will be removed from the skew calculation. This is valid for both random and systematic components since they will have just one value at a given time, and can be removed from the skew as common path delay components. In the case of setup time skew, these components may vary from cycle-to-cycle and, therefore, cannot be removed as common path delays.

32. what is Half-Cycle Setup Skew

In this case, the source uses the rising clock edge and the receiver uses the falling edge. The skew in a half-cycle path will be the same as for the single-cycle skew with the addition of the PLL duty cycle variation in the RSS component.

In the multiple-cycle paths case, the skew will be similar to the single-cycle one. The main difference is the potential extra voltage and temperature variation that may occur during the longer multiple-cycle path.

33. Design has no setup and hold violations but skew target was not met. Can we tape out?

Yes we can but

1. Power consumption will be more

2. Area over head because of more number of cells (buffers/inv) in clock path due to which we might had the congestion

34. How to decrease the skew manually

Cloning to balance the load
Minimizing the clock levels with high drive strength cell
Widen the metal
Delay of large drive strength can be decreased by taper circuit

35. Which Vt cells will you use in the CTS

Standard Vt cells because of
The delay and leakage power compromise
The less process variations compared to LVT and HVT

36. How will you calculate the latency value of the main clock and generated clock?

Insertion delay value need to be decreased a lot for the generated clock if you break because latency already exists till the generation point.
Get the main clock latency from the first iteration.

37. When will you break the generated clocks? When you give as a through pins

When there are no paths talking between the main clock and generated clock. Define as through pins if paths are talking between the domains.
Use clock grouping to balance the skew between the generated clocks/synchronous clocks.

38. What are the types of clock tree structures available?

H tree, Binary, Star, mesh structure, Fish bone

39. **How will you decide the clock skew value while CTS?**

Generally it will be 100-200ps.It needs to more hold buffers/inv as the skew increases. Better to keep as less as possible.

Uncertainty values for setup and hold after CTS will be generally given by foundry .uncertainty value depends on the PLL. Setup uncertainty can be avoided if you could not close the timing but not hold uncertainty. Setup timing issues can be addressed by decreasing the clock frequency but no fix for hold after manufacturing.

Hold sometimes can be fixed by decreasing the voltage vale.

40. What is Advantages and disadvantages of virtual clocks and Real clock

- Advantages of Virtual Clocks:

1. Directly we can change the clock latency after CTS, No need to change the input delay (insertion delay addition) and output delay (insertion delay subtraction)

Disadvantage:

2. Need to give the false paths exceptions for clock domain crossings

Advantages of Real Clocks:

1. No need to give the false paths exceptions for clock domain crossings

Disadvantage

2. Input delay & output delay has to be changed. These will be changed based on the clock latency of boundary flops
3. CTS does not trace through gates, because No Gating rising is specified, but the skew is balanced.

41. How delay will be decreased due to repeater?

Delay proportional to quadratic function of length of the interconnect (Elmore delay equation). So, repeater breaks interconnect and decreases the delay value.

42. Why IO delays change post CTS? Did you consider the clock latency upfront?

IO delays should be defined by considering the latencies upfront

39. Which design you prefer among 0PS and 100PS clock skew.

100 ps because 0ps will consume the power at time because of the simultaneous switching of the clock at all the sinks

40. What is Current density equation?

J = I/Unit Are ,Unit Area = Metal Width X Thickness

41. What might be the reason for more Insertion delay in the design?

i) Clock source might be far from the sinks

ii) Low drive strength at the source point

iii) More resistance (due to small width routing)of the Clock network

iv) More number of clock levels

v) Flops in the same domain might have sprinkled in the design instead of grouping.

vi) E.g. 1 Macro and 3000 number of flops might be there. Paths might be talking from the Macro to the flops. Generally macro will have more delay. So, keeps the high insertion delay to balance the skew between the macro and the flops

42. What ate the asynchronous checks you do? What is meant by them?

I do check for the Recovery and Removal timings.

Recovery - The time period for the reset to de - assert before the active clock edge.
Removal -The time period for the reset to de-assert after the active clock edge

43.How can we make sure all the flops got the clock?

check_timing
[-pins pin_list]
[-type type_list]
[-verbose]
[-sort {pin | warning}]
[-exclude_warning warning_list]
[-include_warning warning_list]
[-early | -late]
[-old]
[{> | >> } file_name | -tcl_list]
Performs a variety of consistency and completeness checks on the timing constraints specified for a design. Valid types are: clocks, clock_clipping,constant_collision, endpoints, input, multiple_clocks and loops.

ROUTING

1. Why spare cells inputs to be tied to logic low/high when output pins are left floating?

Floating outputs can create the interference to the nearby nets like floating inputs picking up the nearby interference and propagating down the network.
Inputs are critical because they are directly connected to the gate .So gate oxide can be damaged easily by the unnecessary charges like ESD/process antenna violations.
Outputs are taken from either drain/source which is immune to ESD.

2. What is the difference between global and detailed routing?

Global routing: just you can see the lines with out vias.
Detailed Routing: Physical nets with vias

3. What are the output files after physical Design?

1. Enc.dat consists of below files.
   cobra_top.conf
   cobra_top.fp
   cobra_top.marker.gz
   cobra_top_physical.vg
   cobra_top.v
   cobra_top.ctstch
   cobra_top.fp.spr
   cobra_top.mode
   cobra_top.place.gz
   enc.pref.tcl
   cobra_top.def
   cobra_top.globals
   cobra_top.opconds
   cobra_top.route.gz
   siFix.option
2. DEF
3. GDSII
4. Physical verilog netlist
5. Sdf, spef

4. Why HVH routing is used generally?

Since logic cell interconnect usually blocks most of the area on the m1 layer.
HVH is efficient if you have standard cells in the row fashion because the M2 vertical layer useful to connect the cell pins of the different rows

5. What is the difference between the global and detailed routing?

Global Route (G Cells)
    Channel assignment
    Metal layer assignment
Detailed Route (S Box)

Track assignment
Via creation

6. Tool could not able to start routing. What might be the problem?

1) Pitch -Specifies the required routing pitch for the layer. Pitch is used to generate the routing grid (the DEF TRACKS).
2) Metal Width
3) Offset value might have not mentioned in the tech LEF. Offset is main thing to be specified and it should be an integer multiple of manufacturing grid.

Specifies the offset for the routing grid for the layer. This value is used to align routing tracks with standard cell boundaries, which helps routers get good on-grid access to the cell pin shapes. For the best routing results, most standard cells have a 1/2 pitch offset between the MACRO SIZE boundary and the center of cell pins that should be aligned with the routing grid. If some other offset is required to get more pins to align, specify an OFFSET value. Generally, it is best for all of the horizontal layers to have the same offset and all of the vertical layers to have the same offset, so that routing grids on different layers align with each other. Higher layers can have a larger pitch, but for best results, they should still align with a lower layer routing grid every few track.
Default: Half the routing pitch for the layer.

PHYSICAL VERIFICATION

1. How the Ntap and Ptap are mentioned in the rule deck?

NTAP = NSRC AND NWELL
PTAP = PSRC AND PSUB

2. How will resolve the power shorts/opens?

LVS ISOLATE YES, text marks.

3. What is the implementation difference between the 130nm and 90nm?

Well Taps, Macro rotation,3x3 via pattern

4. What is the Connect errors and how those will be solved logically and physically?

Shorting of two power domains through the high resistive substrate leads to SConnect errors. This leads to substrate noise by which analog macros get affected.

Logical solution is by adding the PSUB2 layer around the analog macro/different power domain.

Physical Solution to mitigate substrate noise

1. Splitting power will reduce substrate noise
2. Backside Grounding has little effect on substrate noise reduction for high frequency ic.
3. Extending the N-Well under the compensation devices may improve noise immunity by upto 50%
    a. -- to isolates resistors from substrate.
    b. -- to isolated bottom plate from substrate.
    c. -- Nwell rings and p diffusion substrate contacts to reduce noise.
4. P+ ring around the cells may increase noise immunity by about 80%
5. Add multiple rows of contacts
6. the substrate thickness and doping concentrations – *Lightly doped substrate has more noise immunity.*
7. the physical separation between noise aggressors and victims

5. Why float output are ignored but not float gate inputs?

Float gate inputs may pickup any value. So

1. Both the transistors may form the conduction path and short circuit VDD&VSS. Power dissipation increases.
2. ESD signals directly enter the gate and destroy the gate oxide.
3. Inputs may pick up the unnecessary signals from the by side nets and destroy the functionality of the down the stage circuits
4. To avoid these problems we connect the spare gate inputs either to 1/0.

Floating output s

- Connected to the drain & source and is not a problem to the device structure.

6. What are the inputs to and out puts from the power analysis?

Power Meter inputs:

1. Power grid views of the std cells and macros
2. DEF
3. Power and ground voltage values
4. Power consumption of all cells (.lib and customized instance power file if any ex:1T-SRAm)
5. Operating frequency, duty cycle, Input activity factor
6. SDC
7. TWF
8. SPEF

Output: Instance power file

Voltage storm inputs:

1. Power grid views of the std cells and macros
2. DEF
3. Power and ground voltage values & Allowed voltage drop
4. Temperature
5. Metal maximum current density and thickness
6. Power pads location
7. Instance Power file

Outputs:

1) IR drop analysis report
2) EM analysis report and current density report

12. What are the inputs to the SI analysis tool?

- CDB,UDN
- power supply

- verilog netlist
- process
- SPEF
- TWF

Output:

- Noise reports
- SDF
- max delay according to threshold value
- min delay

13. What is purpose of seal ring? What it consists of? How it works (absorbing the stress, protecting the die)?

It is guard fence of the die to protect from the pressure or stress caused while dicing with diamond saw. It consists of all the base layers and metal layers.
It absorbs heat and avoids warping of the die by limiting the heat -affected zone. Stress will be more at corner because it goes twice for cutting.CSR (Chip stress relief) pattern inside the corner pads absorbs more stress.

14. What is the LVS process?

1. V2LVS,spice file editing
2. Merge the GDS,
3. Run flat/Hier

15. How will you solve the LVS short connection with out RVE?

LVS SHORT ISOLATE YES

16. Name few tools which you used for physical verification?

Calibre

17. Electrical-Rule Checkers

Geometrical design rules ensure that the circuit will be manufactured correctly by checking the relative position, or syntax, of the final layout. However, there is nothing to ensure that this circuit will work. Correct functionality is left to the simulators and verifiers that manipulate circuit activity and behavior. Nevertheless, there is a middle ground between simple layout syntax and complex behavioral analysis, and it is the domain of **electrical-rule checkers**, or **ERC**.

Electrical rules are those properties of a circuit that can be determined from the geometry and connectivity without understanding the behavior. For example, the estimated power consumption of a circuit can be determined by evaluating the requirements of each device and trying to figure out how many of the devices will be active at one time. From this information, the power-carrying lines can be checked to see whether they have adequate capacity. In addition to **power estimation**, there are electrical rules to detect incorrect transistor ratios, short-circuits, and isolated or badly connected parts of a circuit. All these checks examine the network and look for inconsistencies. Thus, whereas design-rule checking does syntax analysis on the layout, electrical-rule checking does syntax analysis on the network.

ERC includes following checks

Logical Layer Definition
Tap/Gate/SD Connection Floating Gate/Substrate/Metals
Soft Connection
Valid Device Voltages
Voltage Dependent Channel Length Checks

Whether jogging to be done through lower or top metal layer?
Top metal layer because the deionization will be done after each metal process from M1 to M Top.

14. What is Slot error?

The slot error occurs due to long & high width metals. Can be rectified by creating metal slots.

Signal Integrity

1. What are the effects of cross talk? Why is the cross talk happening? What are the ways to prevent the crosstalk?

Effects are cross talk noise and delay.

Formation of capacitance between the nets will create problem by charge transfer from one net to another net.

Sol:

1. More Space
2. Shielding
3. Order the nets such that timing dependent/timing window overlap nets are far from each other
4. Increase drive strength of the victim net

2. Will you consider the Xtalk effect on the below red color net?

No if and gate connected 2nd input tied to 1.

3. Simultaneous switching of the signal on victim net in the same direction will cause the---- violation?

HOLD

4. Simultaneous switching of the signal on victim net in the same direction will cause the---- violation?

HOLD

5. Simultaneous switching of the signal on victim net in the same direction will cause the---- violation?

HOLD

6. what is cross talk and its causes

Cross Talk : With the scaling of the horizontal dimensions of wires, the aspect ratio of the horizontal to vertical dimensions is reduced, resulting in increased ratios of coupling capacitance to substrate capacitances.

When the signals in the neighboring wires switch, the coupling capacitors cause transfer of charge between them. Depending on the relative rate of switching (rise and fall times of the signals) and the amount of mutual capacitance, there can be significant crosstalk noise.

Cross Talk Causes: Cross talk noise and Cross Talk delay.

Case 1: Victim net switching in same direction

-Shorter switching times on clock path (Setup Violation)

- Shorter Switching times on data path (Hold Violation)

Case 2: Victim net switching in opposite direction

- Longer switching times on clock path (Hold violation)
- Longer switching times on data path (Setup Violation)

Cross talk occurs because of cross-coupling capacitance between interconnects

It is measure of CC / Cs
CC - Lateral coupling capacitance between interconnects of the same layer
CS - Capacitance due to overlapping of interconnect between diff. layers
Solution - Keep problematic nets apart

Crosstalk Noise

- When the signals in the neighboring wires switch, the coupling capacitors cause transfer of charge between them. Depending on the relative rate of switching (rise and fall times of the signals) and the amount of mutual capacitance, there can be significant crosstalk noise.
- Crosstalk noise between neighboring signal wires can cause two major problems that affect the operational integrity of IC designs:
  Crosstalk delay and Crosstalk glitch

Crosstalk Delay

- Crosstalk delay changes the signal propagation on some of the nets, reducing achievable clock speed
  Crosstalk Glitch
- Crosstalk glitch causes voltage spikes on some nets, resulting in false logic states being captured in the registers.

OCV

1. What is OCV and why it occurs?

Characteristic variations of the cells/nets on the chip are called On Chip variations. It occurs due to

1. Process variations
2. Voltage variations due to IR drop
3. Temperature variations due to non uniform power dissipations due to non uniform frequency of operation

2. What is the difference between the signal transition and signal drive strength?

Signal transition is the time taken by the signal from 10% to 90% of final value.

The maximum current the drier can drive is called signal/cell drive strength.

3. Why the resistivity of the top metal layers will be low compared to the lower metal layers eve though you use the same metal for all the layers?

Theoretically, one would want to have all metal layers with low resistance. Practically, there are limitations - cost and technology - that lead to finite metal resistance .All metal layers can be made of copper, and copper has much lower resistance than aluminum (~1.7e-6 Ohm*cm vs ~2.7e-6 Ohm*cm). However copper technology is more expensive than aluminum technology, so there is a cost-performance trade-off.

From technology viewpoint, you can make a metal layer very thick (to make sheet rho value lower), but then you can't make metal line very narrow (lateral coupling capacitance increases and results the cross talk) .So if you want to achieve very fine metal pitch (to provide high integration density - i.e. number of devices per unit area), the metal thickness can't be made very large. The solution is to use thinner (and thus more resistive) metal layers for low layers (i.e. M1, M2 ...) and for local routing, and thicker (less resistive) layers with larger width and spacing for long-range routing on the higher levels.

4. How will you decrease the project cycle time If a similar design is given to you

1. Anticipating the similar problems and coming up with quick fix solutions
2. Scripting the methodology/patches
3. Making sure the SDC available is complete and correct in terms of exceptional paths, and timing values
4. Implementing the sanity checks (data inputs like verilog,lib, lef,IPs ,rule decks , GDSII, CDB,tech files and cdl files extensively with respect to the design
5. Stick to the time schedule of inter dependency deliverables

5. How Latch up is taken care in the ASIC flow?

1. Guard rings
2. Body biasing (Nmos to ground, Pmos to VDD)

6. What is Antenna effect and antenna ratio? How to eliminate this?

Antenna ratio = Total area of the metal connected to the gate / Gate area

Eliminate By:-

1. Metal jogging to top metal layer
2. Antenna diodes
3. Decrease the ratio in lef file and do routing

4. Insert the buffers

7. What is the difference between the Antenna check at Encounter and calibre?

Open nets are the antenna at encounter and Process antenna is the antenna violations at calibre.

8. What is the difference between a process antenna violation and a geometry antenna violation?

Solution:
In the documentation and user interface for FE you may find that the word 'antenna' is used to describe two different routing situations: process antennas and geometry antennas. This has caused some confusion and the following explanation will help to explain the difference.

Process antenna effect is a standard concept in physical design and the one most users refer to when seeing the word 'antenna'. Process antenna effect is when charge builds up on metal routing during planarization that can damage gates.
The FE command Verify Antenna refers to process antennas and will report input pins that exceed the allowed antenna ratio as defined in the LEF.

Users will also see the word 'antenna' used when referring to dangling nets that do not terminate at a pin or wire. This is a lesser known use of the word 'antenna' which the documentation and UI will refer to in the future as dangling nets. Verify Geometry will flag 'geometry antennas' by indicating a **violation** at the end of the dangling net.

10. Which type of Antenna diode? How it works? What are the disadvantages compared to metal jogging? (

Once the chip is fabricated, this cannot happen, since every net has at least some source/drain implant connected to it. The source/drain implant forms a diode, which breaks down at a lower voltage than the oxide (either forward diode conduction, or reverse breakdown), and does so non-destructively. This protects the gate oxide.
Taking a small metal jump to the higher level is the first step that should be tried, rather than adding antenna diodes which leads to reverse bias leakages (and especially on the switching nodes).
Disadvantages:
The extra capacitance of the antenna diode makes the circuit

a) Slower

b) More power hungry.

11. Same buffer name has been used in the analog block as well as in the digital domain. How you solve the LVS issue?

Rename the buffer in the analog macro. Buffers used in the analog macro have the different width and lengths compared to digital domain buffers

12. What are the DRC errors you encountered rather than spacing

1. Well spacing
2. Min width
3. Enclosure
4. Metal slotting due to wide width metal
5. Metal/AP/Poly density

13. What is the tap less and tap cells. What is the advantage of tap less? What care should be taken for tap less cells?

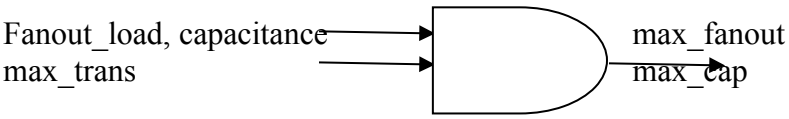
Tap less cell does not have Substrate/bulk connections to connect to VDD/VSS. Tap less standard cell should connect to tap cells through filler cells to have the well continuity. We can control the substrate/body biasing to decrease the sub threshold current by increasing the threshold voltag

TIMING CLOSURE

1. Can I have the infinity load if I can maintain the required transition?

No because drive max_fanout would be finite value. Max_cap and max_fanout also should be considered.

2. Why max_cap and max_fanout checks?



Fanout load for input and max_ fanout for output are unit less constraints
Capacitance for input and max _cap for output are another set of constraints.
We cannot predict the behavior of the cell once you violate the DRVs. We can confirm by simulation for few nets but not for hundreds of nets.

3. What is the recommended procedure for the designers to help close on hold time fixing?

Here are some pointers for the designer that should help them close on hold time fixing:

1. Don't wait until after fixing setup to check for hold.
Even though we recommend fixing the hold time violations after fixing the setup Violations in post route stage, it still makes sense to run timing analysis after CTS to see how bad the hold problems really are. It may require going back to Floor planning and placement to fix them, so if there are a lot of hold time Violations post CTS, do some analysis.

2. Check your Clock Skew
Reg2reg Hold time is caused by excessive clock skew between clock inputs to the registers. Thus prior to running "optDesign -hold -postRoute", you should run "timedesign -hold -postRoute" to check for hold time violations after the setup fixing. If there are more then 50% of the paths that are violating, you should do some analysis of the clock skew and clock uncertainty to see if there is a systematic problem. While it is true that routing may fixed some of the smaller violations because of detouring of the routes, it will not have a big impact on larger violations.

3. Placement considerations
If design has gated clock, then be sure to run placeDesign after reading cts spec and set placeDesign to be clock gate aware:

```
setPlaceMode  -clkGateAware 1
```

If the design has several blocks, try to not have small slivers of placable area where registers can be placed between the block and make balancing the clock very difficult. Use block halos and soft placement screens to force placement into the biggest areas. The placement screens should be soft, so during optimization, the area can be used for buffering.

5. SDC constraints should not have clock uncertainty too large for postRoute
The SDC may have a clock uncertainty for hold that includes an estimate of the clock skew. After the design has had the clock synthesized and routed, the clock uncertainty should be reduced to remove skew estimates and fudging for routing delays, since both are now known in the post route design with extraction and delay calculation.

Also there some good pointers are:
1) Do timing analysis prior to each stage optimization. This will help identify constraints related issues up ahead. Otherwise, the tool will be inserting too many buffers or un-needed up-sizing etc. to fix violations that may be false.

2) Post clock tree analysis and tweaks in terms of clock balancing or clock tree ECO building will enable you to meet timing without too much buffer addition, etc.

3) It's good to "ANALYZE" setup and hold post CTS so you can make quick iterations.

4. What methods do you follow to close the timing when the design is critical?

Set up Time: Cloning, High drive strength driver, adding repeater to break the long net.

5. How to do timing analysis when the data path coming from slow domain to fast domain?

False can be used if synchronizer used between the domains else Multi cycle path, taking worst of all path delay to define in SDC file.

Analyze

1) Data from fast domain to slow domain

2) Data from slow domain to fast domain

6. Is worth doing zero RC delay for the synthesized netlist for DSM designs?

No because the Net delay > Cell Delay

7. Will you go ahead if you have 10-20ps negative slack for the synthesized netlist?

1) Depending on the uncertainty margin for setup slack
2) Clock frequency margin
3) Wire models, can not go ahead if you use accurate WLM instead of pessimistic WLM.

8. What will you do if you have 500ps slack for synthesized netlist?

1) Check the uncertainty margin
2) Check the clock frequency
3) Check the WLM whether they are accurate/pessimistic
4) RTL change
5) Re synthesize

9. How will you solve if you have -1ns after place IPO? What might be the reason?

According to the reason

1) Check the paths and confirm whether valid/false or multi cycle paths
2) Change the floor plan
3) Change the placement of standard cells ,whether they placed around the macro
4) Check can you provide the other flavor of standard cells
5) Logical change/RTL change (pipe line)

10. What timing checks did you do?

Setup
Hold
DRV - max_cap,max__tran,max_fanout
Clock gating check
Clock Min pulse width
Max timing borrow check
Clock transition

11. Will all the flops have same setup and hold value?

No

12. What is negative temperature inversion?

Delay is directly proportional to temperature at lower voltage for the lower geometries

13. How do we eliminate slack if it occurs during First optimization stage (trial routing)?

1. Check the SDC consistency
2. IPO
3. Check placement and routing

14. Which is more complicated when u have a 48 MHz and 500 MHz clock design?

500MHZ because we will have tight skew margins compared 48MHZ.

15. What are the 3 fundamental operating conditions that determine the delay characteristics of gate? How operating conditions affect gate delay?

- Process
- Voltage
- Temperature

16. In a system with insufficient hold time, will slowing down the clock frequency help?

- No.
- Making data path slower can help hold time but it may result in setup violation.

17. In a system with insufficient setup time, will slowing down the clock frequency help?

- Yes.
- Making data path faster can also help setup time but it may result in hold violation

18. A very good interview question... What is difference between setup and hold time. The interviewer was looking for one specific reason, and its really a good answer too. The hint is hold time doesn't depend on clock, why is it so...?

Setup violations are related to two edges of clock, i mean you can vary the clock frequency to correct setup violation. But for hold time, you are only concerned with one edge and does not basically depend on clock frequency

19. What is Static Timing Analysis ?

It is the method of computing the expected timing of a digital circuit without actual simulation

20. Why Static timing Analysis:
Gate-level simulations are time consuming and resource-intensive GLS exhaustiveness is limited to the test cases

21. Four Valid Timing Paths are:
1. Reg to Reg
2. Input to Register
3. Register to output
4. Input to output.

22. What is Setup Time?
The amount of time for which data has to be stable before the active edge of the clock.
- Tclk period >= Tclk□q(max) + Tcombo(max) + Tsetup of ff2
- Setup □ Arrival Time(AT) < Required Time(RT)
  A.T □ Tclk□q + Tcombo +Tsetup + Tskew
  R.T □ Tclk
- If not setup is violating

REMEDY:
1. Fasten the data path
2. Delay the clock path

23. What is Hold Time ?
The amount of time the data has to be stable after the active edge of the clock.
- Tclk□q(min) + Tcombo(min) >= Thold + Tskew
- HOLD : Arrival Time > Required Time

A.T □ Tclk□q + Tcombo
R.T □ Thold + Tskew

REMEDY: Slow down the data path

24. Problem statement:
In the report generated by timeDesign, the overall total negative slack (TNS) and number of violating paths of a design does not equal to the total of the TNS and violating paths of the individul path groups.How can this be possible
Solution:
It is possible for the overall total negative slack (TNS) and number of **violating** paths of a design to not be equal to the total of the TNS and **violating** paths of the individual path groups.

This is because the TNS and number of **violating** paths are based on end-point of the path and is not path based.

For example, consider a simple design comprising of 2 flip-flops and some combinational logic. For this design, assume the following:

-There is a constrained path from the first flip-flop to the data pin of the second flip-flop (reg2reg path group) which **violates** the setup constraint by .03ns.

-There is a constrained path from the input port of this design to the data pin of the second flip-flop (in2reg path group) which **violates** the setup constraint by .25ns

Shown below is the report generated by timeDesign for this design:

```
------------------------------------------------------------
         timeDesign Summary
------------------------------------------------------------

+--------------------+---------+---------+---------+---------+---------+--------
-+
|    Setup mode      |   all   | reg2reg | in2reg  | reg2out | in2out  | clkgate
 |
+--------------------+---------+---------+---------+---------+---------+--------
-+
|          WNS (ns):| -0.250  | -0.030  | -0.250  |   N/A   |   N/A   |   N/A
 |
|          TNS (ns):| -0.250  | -0.030  | -0.250  |   N/A   |   N/A   |   N/A
 |
|   Violating Paths:|    1    |    1    |    1    |   N/A   |   N/A   |   N/A
 |
|         All Paths:|    2    |    1    |    2    |   N/A   |   N/A   |   N/A
 |
+--------------------+---------+---------+---------+---------+---------+---------+
```

As can be seen in the above report, the overall TNS (-.25ns) does not equal the total TNS of the individual path groups (.25 + .03) = -.28ns
Also the total number of **violating** paths in the overall report (1 **violating** path), does not equal the sum of **violating** paths in each individual path group (1 + 1) = 2 **violating** paths.

This is because timeDesign is end-point based. In the contrived example, both **violations** were on the data pin of the second flip-flop.

The overall number reported by timeDesign reports the worst **violation** at each end point, and hence reports only one **violation** of -.25ns, while the individual path group sections report the worst violators in each path group.

The same holds true when reporting number of **violating** paths. Since both **violations** were at the data pin of the second flip-flop, the overall report being end-point based Just counts this as one **violating** path.

26. What is the setup and hold time of latch?

That will defined at the end of active edge

27. Can setup and hold be there for a same path? How fix the hold time violation if no setup margin exists and vice versa?

It can be between the same end points but not for the same path.
Setup:
Upsize the driver cell before the divergence point.
Hold:
Add the delay cell at the path end point.
Try logic optimization when no margins exist.
Split the logic by inserting the Flop and do the pie lining.

28. What is the correlation factor for the PT and encounter?

Generally greater than 1

SPEF correlation (QRC vs native detailed extraction) using ostrich and perl script (spefCapCmp.pl) in both worst and best case for DSHR block.
Capacitance scaling factors are here.

	WC	BC
Ostrich:	**1.021**	**1.1058**
Perl script:	**1.0163**	**1.0973**

I got resistance scaling factors as 1.0435 for WC and 1.0019 for BC by using Ostrich

29. In how many corners did you close the timing? How did you decide upon the corners and de rating factors? What is MMMC?

Depends on the fab guide lines because many DSM effects like Temperature inversion comes into the picture.

Crimson:
Set up MMMC analysis views
Create RC Corners

```
create_rc_corner -name RCMAX_timi_woSI -cap_table
/projects/cmos090_7M2T_M2V_Worst.captbl -detailed_cap_factor 1.03 -
default_cap_factor 1.0 -res_factor 1.0 -xcap_factor 1.0
create_rc_corner -name RCMIN_timi_woSI -cap_table
/projects/cmos090_7M2T_M2V_Best.captbl  -detailed_cap_factor 1.03 -default_cap_factor
1.0 -res_factor 1.0 -xcap_factor 1.0
# Create RC/Lib corners
create_delay_corner -name RCMAX_timi_woSI_max -library_set default_libs_max -
rc_corner RCMAX_timi_woSI
create_delay_corner -name RCMAX_timi_woSI_min -library_set default_libs_min -
rc_corner RCMAX_timi_woSI
create_delay_corner -name RCMIN_timi_woSI_max -library_set default_libs_max -
rc_corner RCMIN_timi_woSI
create_delay_corner -name RCMIN_timi_woSI_min -library_set default_libs_min -
rc_corner RCMIN_timi_woSI
# Set up 10% OCV and clock reconvergence pessimism removal
set_timing_derate -delay_corner RCMAX_timi_woSI_max -early 1.0 -late 1.0
set_timing_derate -delay_corner RCMAX_timi_woSI_min -early 1.0 -late 1.0
set_timing_derate -delay_corner RCMIN_timi_woSI_max -early 1.0 -late 1.0
set_timing_derate -delay_corner RCMIN_timi_woSI_min -early 1.0 -late 1.1
setAnalysisMode -cppr true
# Create operating modes
create_constraint_mode -name mission_timi_woSI -sdc_files {/design.constr.pt}
create_constraint_mode -name scan_timi_woSI -sdc_files {/design.constr.pt}
# Establish MMMC analysis views
create_analysis_view -name mission_RCMAX_timi_woSI_max -delay_corner
RCMAX_timi_woSI_max -constraint_mode mission_timi_woSI
create_analysis_view -name mission_RCMAX_timi_woSI_min -delay_corner
RCMAX_timi_woSI_min -constraint_mode mission_timi_woSI
create_analysis_view -name mission_RCMIN_timi_woSI_max -delay_corner
RCMIN_timi_woSI_max -constraint_mode mission_timi_woSI
create_analysis_view -name mission_RCMIN_timi_woSI_min -delay_corner
RCMIN_timi_woSI_min -constraint_mode mission_timi_woSI
create_analysis_view -name scan_RCMAX_timi_woSI_max -delay_corner
RCMAX_timi_woSI_max -constraint_mode scan_timi_woSI
create_analysis_view -name scan_RCMAX_timi_woSI_min -delay_corner
RCMAX_timi_woSI_min -constraint_mode scan_timi_woSI
create_analysis_view -name scan_RCMIN_timi_woSI_max -delay_corner
RCMIN_timi_woSI_max -constraint_mode scan_timi_woSI
create_analysis_view -name scan_RCMIN_timi_woSI_min -delay_corner
RCMIN_timi_woSI_min -constraint_mode scan_timi_woSI
# Set analysis views
```

```
set missionList_timi_woSI [list  \
      mission_RCMAX_timi_woSI_max \
      mission_RCMAX_timi_woSI_min \
      mission_RCMIN_timi_woSI_max \
      mission_RCMIN_timi_woSI_min \
      ]
set scanList_timi_woSI [list  \
      scan_RCMAX_timi_woSI_max \
      scan_RCMAX_timi_woSI_min \
      scan_RCMIN_timi_woSI_max \
      scan_RCMIN_timi_woSI_min \
      ]
set_analysis_view -setup $missionList_timi_woSI -hold [ concat $missionList_timi_woSI
$scanList_timi_woSI ]
```

30. What is Timing challenges faced

Fixing the setup and hold violations.

For setup: Back tracing the path and decreasing the delay by

- Upsize the drive
- Insert Buffer
- Useful skew by considering the net stage hold margin
- Pipe lining

For Hold: Adding the delay buffers at the end point.

1. Input max transition - 25% clock period for data,10% for clock paths

Depends previous project experience we can say typically for faster clocks at 55 nm clock transition is 250 ps and data transition is 500 ps for slower clocks data transition limit is 800 ps to 1 ns and for clocks is around 500 ps all these numbers are in 55nm chip.For higher technologies like 130nm these values can be higher.
For 180nm cobra we used 1.8ns =1800ps on signal pins, 400ps for clock pins T = 4ns.
I think even from library we can decide our max trans and max trans value

2. Clock uncertainty for

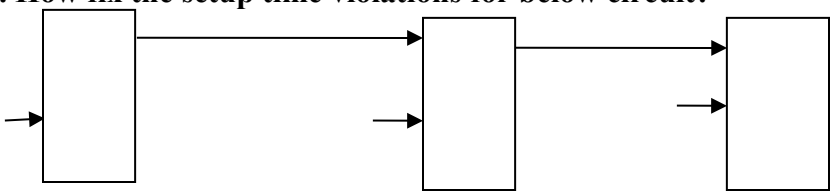
Setup: 10-15% clock period
Hold: 5 – 7 % clock period

31. Which stages will you check the timing .How much margin will you give at each stage?

Synthesized netlist
Post Floor plan
Post placement
Post CTS

Post Route

32. How fix the setup time violations for below circuit?



1) Decrease the clock frequency
2) Skew the capture clock –useful skew. Skew value will be defined based on the hold margin available in next stage

This type of scenarios mainly occurs with the macro/memories write cycle mode. These will be solved on the (TEFS) Total endpoints failing slack.
This approach isolates the macro_3 path group for optimization and determines whether the TEFS can be reduced. The optimizer will stop when the worst path cannot be improved so the critical paths 2 to 51 of this path group have not yet been optimized. After optimization, if the TEFS are significantly reduced, then possibly there is only a minor issue with that path group.

However, if the slack is not significantly reduced, isolating the clock network to the RAM and using useful skew is probably the only strategy that will work. Alternatively, you could re-place the design with regions or net weights bt this can be a major setback for large blocks where the placement and optimization times are long.
To determine if this is a possibility, you need to know the slack margin of the RAM. In other words, you need to determine the worst case timing to and from the RAM. If all the critical timing is to the RAM and there is enough margin on the paths from the RAM, then slowing down the clock to the RAM will help. If all the critical timing is from the RAM and there is enough margin on the paths to the RAM, then the clock to the RAM must be sped up or the clock to the critical registers being driven by the RAM must be slowed down. This is a much more difficult process and might require rebuilding clock trees instead of simply running clock tree optimization.

33 How hold analysis done for the multi cycle paths?

By default it checks one cycle before the setup cycle check but we need guide the tool to check for the restrictive edge. For more information refer STA for Nanometer Designs.

34. How the R, C of the net modeled for the delay calculation?

Equal segments of the net will have the R, C values. Distributed capacitance and resistance of the net used for the delay calculations. Arnold delay model is accurate than Elmore.

35. How capacitance modeled for the nets on different layers?

Nets on different layers will have below components

1. Overlap (bottom and top) capacitance
2. Fringe capacitance
3. Lateral capacitance

36. How to fix the hold violations at post silicon stage 1) Decrease the voltage (results in slow slew

which may fix the hold violations) .This type of products undergo binning which work with low frequencies and low voltages.

37. Synchronous vs. Asynchronous Reset
Synchronous Reset
1. Is easy to synthesize.
2. Requires a free-running clock for reset to occur.
3. For VHDL, the synchronous reset does not have to be in the process sensitivity list.

a. VHDL- Flip Flop with synchronous Reset

```
process (clock)
begin
if (clock'event and clock = '1') then
if (reset_n = '0') then
data_out <= '0';
else
data_out <= data_in;
end if;
end if;
end process;
```

b. Verilog- Flip Flop with synchronous Reset

```
always @ (posedge clock)
begin
if (reset)
data_out <= 1'b0;
else
data_out <= data_in;
end
```

Asynchronous Reset

1. Does not require a free-running clock for a reset to occur
2. An asynchronous reset is harder to implement because it is a special signal like a clock. Usually, a tree of buffers is inserted at place and route.
3. Must be synchronously de-asserted in order to ensure that all flops exit the reset condition on the same clock. Otherwise, state machines can reset into invalid states.
4. For both VHDL and Verilog, the asynchronous signal must be in the process and always sensitivity list.

a. VHDL- Flip Flop with asynchronous Reset

```
process (clock, reset_n)
begin
if (reset_n = '0') then
data_out <= '0';
elsif (clock'event and clock = '1') then
data_out <= data_in;
end if;
end process;
```

b. Verilog- Flip Flop with asynchronous Reset

```
always @ (posedge clock or negedge reset_n)
begin
if (!reset)
data_out <= 1'b0;
else
data_out <= data_in;
end
```

38. Whether setup time of the flop depends on the output load?

No, it depends on the data transition (intrinsic rise or intrinsic fall). It is modeled for a rising edge triggered Flip flop as below.

```
timing () {
timing_type : setup_rising ;
intrinsic_rise : 1.5 ;
intrinsic_fall : 1.5 ;
related_pin : "Clock" ;
}
```

39. How you avoid the noise problem?

1. Shielding
2. Spacing
3. Re ordering
4. Metal layer change
5. Buffer insertion
6. Decrease the distance between the source and sink. So, interconnect will not be effected by the aggressor.