

# Introduction to Memory

Reviewed 2026



© 2020-2026 Micron Technology, Inc. All rights reserved. Information, products, and/or specifications are subject to change without notice. All information is provided on an "AS IS" basis without warranties of any kind. Statements regarding products, including statements regarding product features, availability, functionality, or compatibility, are provided for informational purposes only and do not modify the warranty, if any, applicable to any product. Drawings may not be to scale. Micron, the Micron logo, and other Micron trademarks are the property of Micron Technology, Inc. All other trademarks are the property of their respective owners.

# How to cite sources from the Micron Educator Hub

- Micron is committed to collaborate with educators to make semiconductor memory education resources available through the Micron Educator Hub
- The content in the Micron Educator Hub has been identified by Micron as current and relevant to our company
- Please refer to the table on the right for proper citation

Use case	How to cite sources
<b>Whole slide deck or whole document</b>  Description: User uses the whole slide deck or whole document AS IS, without any modification	No additional citation required
<b>Full slide or full page</b>  Description: User incorporates a full slide or a full page into their own slide deck or document	“© 2020-2026 Micron Technology, Inc. All Rights Reserved. Used with permission.”
<b>Portion of a slide or portion of a page</b>  Description: User copies a portion of a slide or a portion of a page into a new slide or page	This is not allowed

# Table of Contents

- 1 Goal, Objectives and Target Audience**
- 2 Introduction to Semiconductor Memory**
- 3 Semiconductor Devices Overview**
- 4 Introduction to DRAM**
- 5 Introduction to Flash**
- 6 Key Terminology/Glossary**
- 7 Document Updates**

# Introduction to Memory - Goal and Objectives

Participants will be able to understand basic concepts of semiconductor memory technologies.

## Objectives:

1. Explain what is Semiconductor Memory
2. Describe some of the fundamental semiconductor devices used in memory (resistor, diode, capacitor, transistor)
3. Describe the basic structure and operation of a MOSFET transistor
4. Describe the basic structure and operation of DRAM memory
5. Describe the basic structure and operation of Flash memories

# Target Audience

- This Introduction to Memory module covers the basic structure and operation of DRAM and Flash memory
- Interns, NCGs (New College Grads), and new employees in technical roles need to understand these concepts
- Examples of critical target audience roles at Micron that utilize these concepts:
  - Process Technicians
  - Design Engineer
  - Product Engineer
  - Verification Engineer
  - Process Engineer
  - Process Integration Engineer
  - Test Engineer
  - Probe Engineer
  - Characterization Engineer
  - Reliability Engineer
  - Signal Integrity Engineer
  - Quality Engineer

## Pro tip

Everyone interviewing at Micron can use this presentation to prepare for the interview by learning foundational information about memory. Check out the candidate guides for Engineering, Technician and Business roles.

- [Micron engineering candidate guide](#)
- [Micron technician candidate guide](#)
- [Micron business candidate guide](#)

## 2. Introduction to Semiconductor Memory

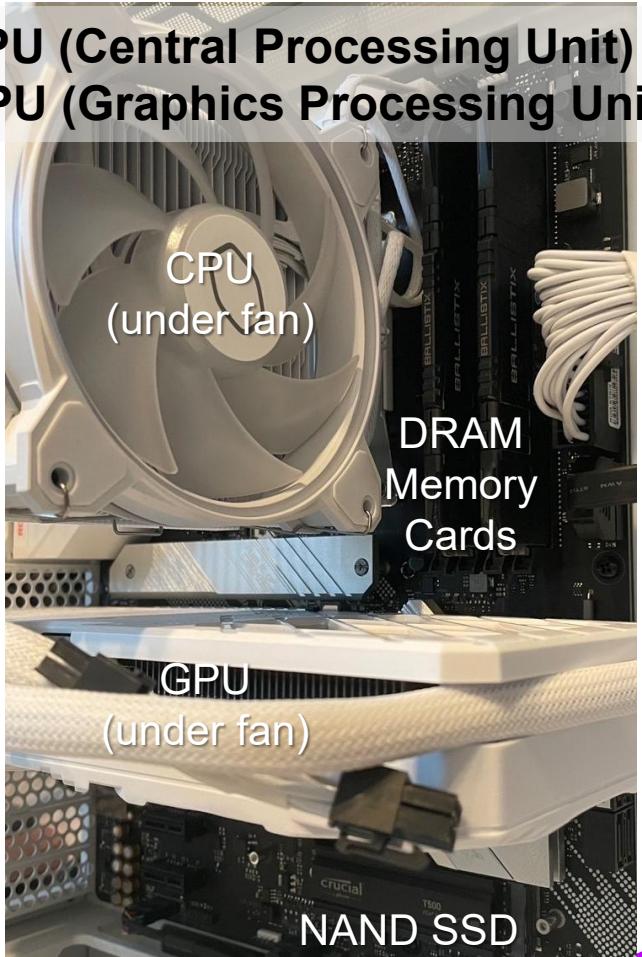
micron



# Types of Semiconductor Devices

## LOGIC DEVICES

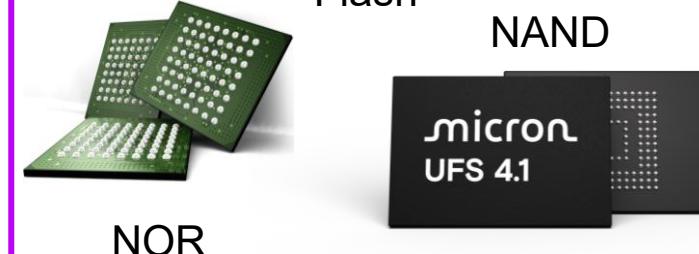
**CPU (Central Processing Unit)**  
**GPU (Graphics Processing Unit)**



## MEMORY DEVICES



DRAM



**MICRON Products**

## SPECIALTY DEVICES



CMOS Image Sensors



LEDs

# Logic vs Memory

## LOGIC

- A **logic chip** performs a function on given data
- A processor or controller chip
- Logic implies "processing"
  - a fixed operation is performed
  - a set of instructions is executed that may vary

## MEMORY

- A **memory chip** allows you to store & retrieve data
- A chip that holds programs and data (temporarily or permanently)
  - DRAMs are for temporary workspace
  - Flash memory is used like a disk drive (permanent until erased)

# Basic Memory Operations

## WRITE OR PROGRAM



WRITE or PROGRAM or store information (1s and 0s) in the memory

Example: Snap a picture with a phone. The picture is “written/programmed” in memory.

## READ



READ information from the memory

Example: You look at a picture you took yesterday. You are “reading” it from the memory.

## ERASE



ERASE or delete information from the memory

Example: You don’t like the picture, so you “erase” it from the memory!

# How Memory Works – Binary language

- Electronic systems store information using digital technology
- Digital technology uses **BITS** and **BYTEs** to encode information (1 BYTE = 8 BITS)
  - Each BIT is a single piece of information that can have one of two values: 0 or 1
  - Groups of BITS are used to represent whole pieces of information, such as a letter, a number, or a color
  - 1 BYTE of information is required to represent a letter
  - The name Micron is represented by six BYTEs as follows

M

01001101

i

01101001

c

01100011

r

01110010

o

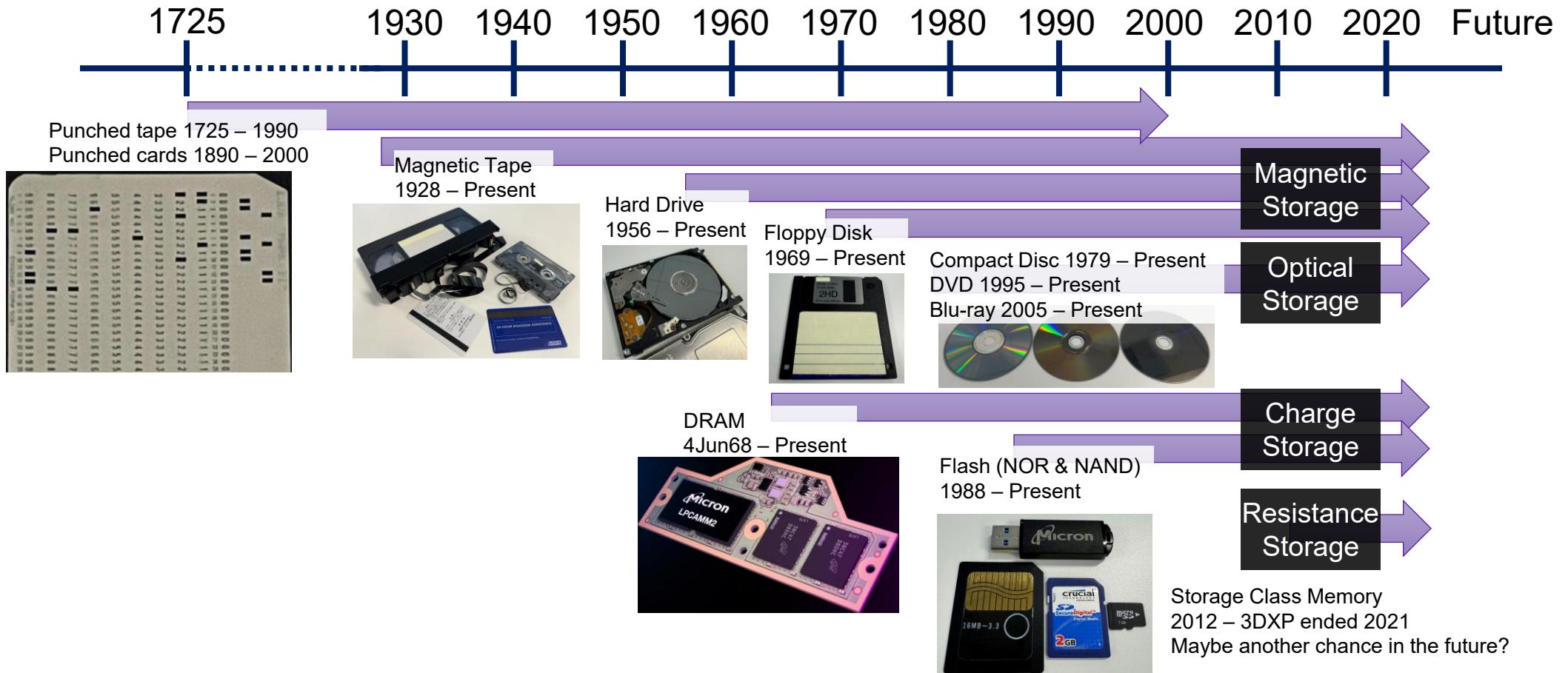
01101111

n

01101110

# Memory Storage

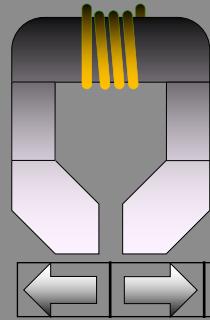
- Memory (data) storage is not a modern invention.
- Over the years many different approaches have been used to store information...



# Memory Storage Methods

Magnetic

Hard Disk Drive



1 0 1 1 0 1 0 1

← → ← → → ← ← →

Optical

Charge

Resistance

Read head senses changes in direction of domains within the thin magnetic film: change = 1, no change = 0

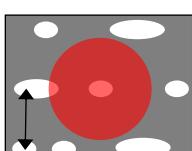
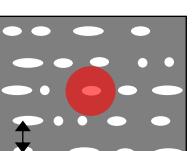
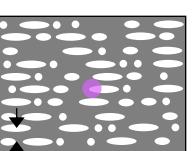
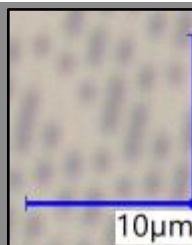
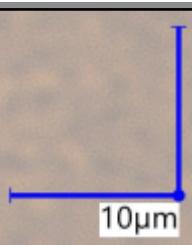
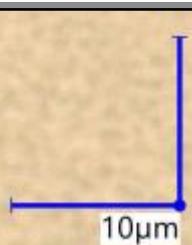
(binary code for “μ”)



# Memory Storage Methods

Magnetic      Optical      Charge      Resistance

CD ROM, DVD, Blu-Ray

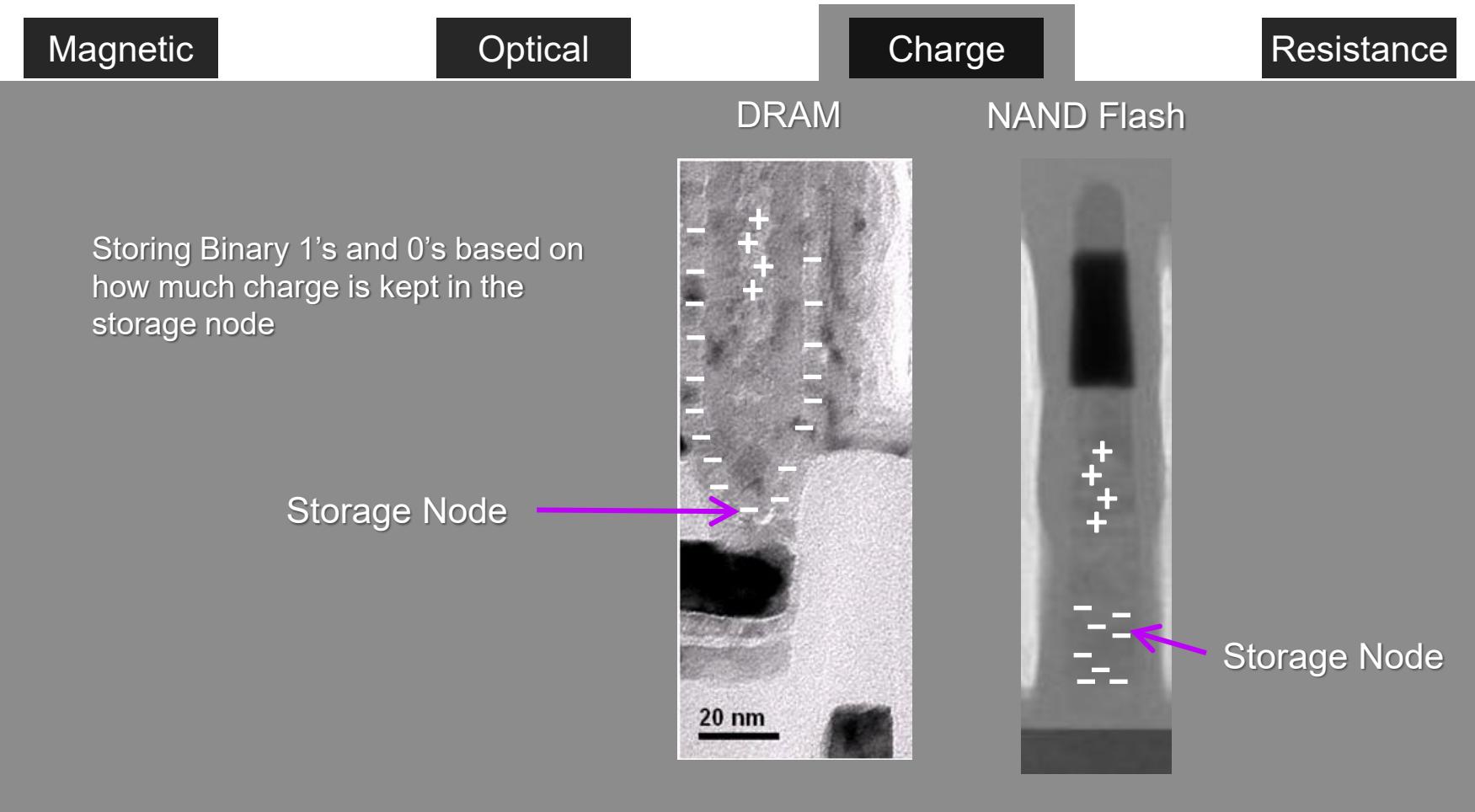
Compact Disc	Digital Video Disc	Blu-Ray Disc
780nm Red Laser	650nm Red Laser	405nm Blue Laser
		
Track pitch 1.6µm	Track pitch 0.74µm	Track pitch 0.30µm
		
Optical microscope photos		



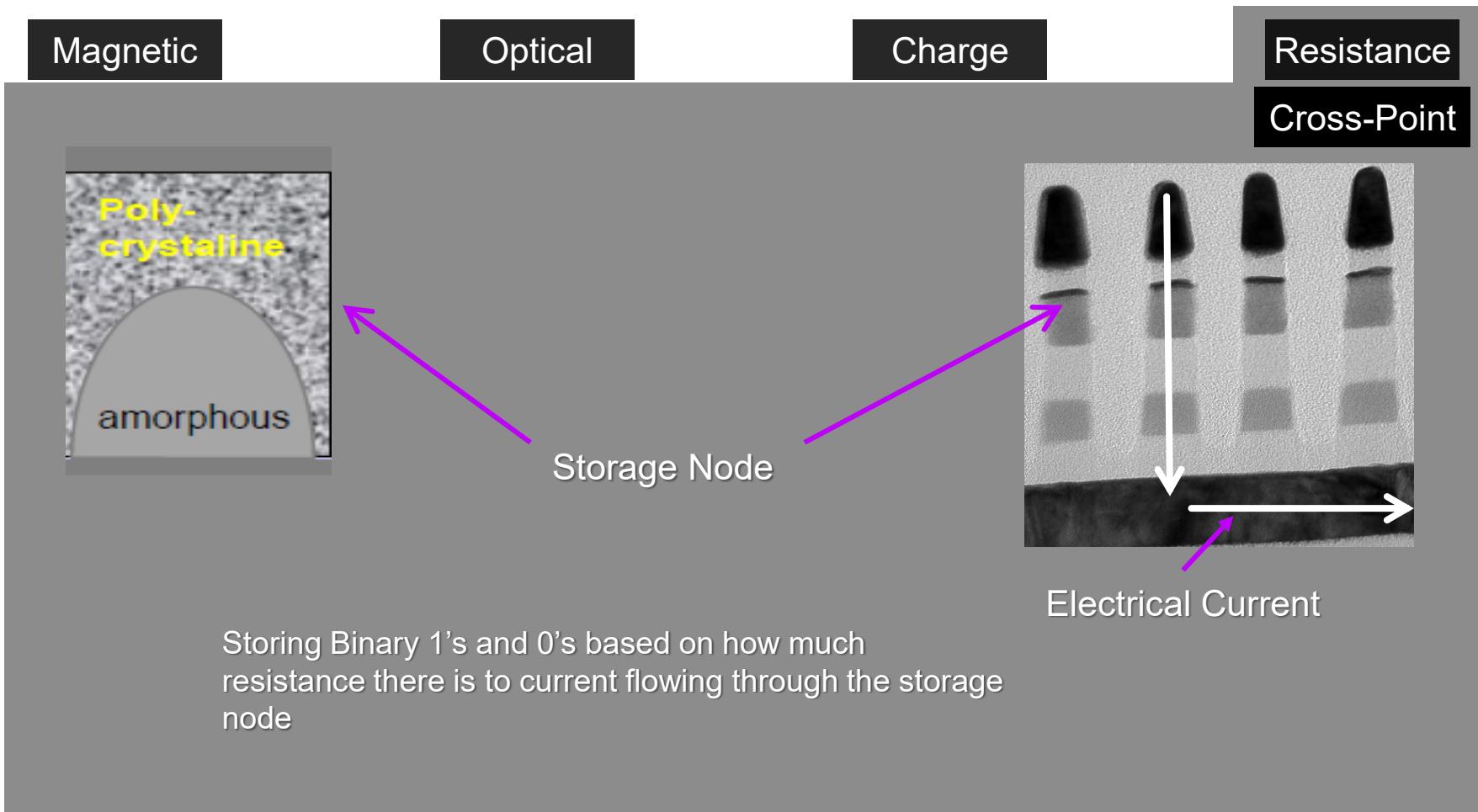
Storing Binary 1's and 0's with indentations in a metallic film

Storage Capacity:  
 $750\text{MB} \times 6 = 4.5\text{GB} \times 5.6 = 25\text{GB}$

# Memory Storage Methods



# Memory Storage Methods



# Major Types of Memory

- Memory can be classified as **Volatile** or **Non-Volatile**
- **Volatile** (example: DRAM)
  - Memory that will lose stored information when power is removed from the part
- **Non-Volatile** (example: NOR Flash & NAND Flash)
  - Memory that will retain stored information even when power is removed from the part



Quiz: What type of memory (volatile or non-volatile) do you want for the memory that stores the pictures you take in a smart phone?

# Summary of Silicon-Based Memory Technologies

Short Name	Full Name	Description	Type	Speed	Density	Primary Applications
SRAM	Static Random Access Memory	Data is stored as the state of a digital flip-flop. Does not require refresh.	Volatile	Very Fast Read and Write	Low	Cache between CPU and other memory types.
DRAM	Dynamic Random Access Memory	Data is stored as charge on a capacitor. Charge is quickly lost and must be constantly “refreshed”.	Volatile	Fast Read and Write	High	“Scratch Pad” for a CPU. Computers, servers, laptops, tablets, PDA's, cell phones, AI applications, etc.
NAND	NAND Flash Memory	Data is stored by “trapping” charge in a film. Data can be stored for up to 10 years without need for refresh.	Non-Volatile	Slow Read, Very Slow Write	Very High	Long term storage: digital cameras, cell phones, MP3s, memory sticks, SSDs, etc.
NOR	NOR Flash Memory	Similar to NAND Flash, but the array is configured for faster read/write.	Non-Volatile	Faster access time than NAND	Medium	Applications that require fast access time like code execution. Example: OS (Operative System)

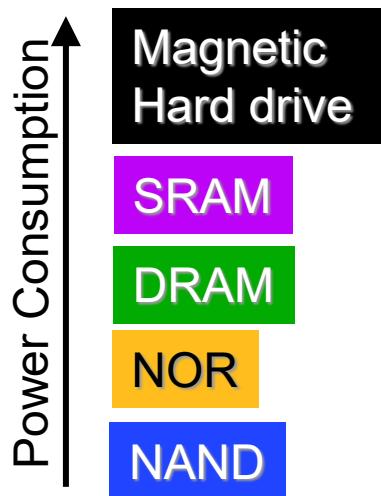
NAND/NOR are not acronyms:

NAND refers to the series arrangement of memory cells similar to NAND (Not AND) digital logic

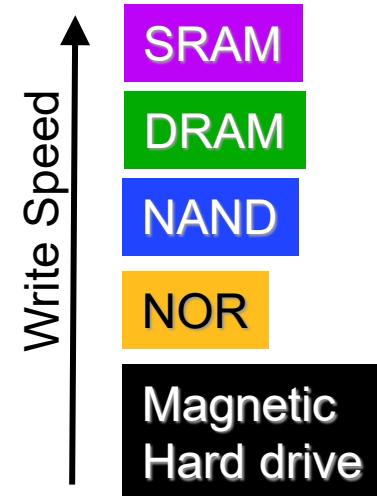
NOR memory cells are arranged in parallel like NOR (Not OR) digital logic

# Comparison of Memory Types

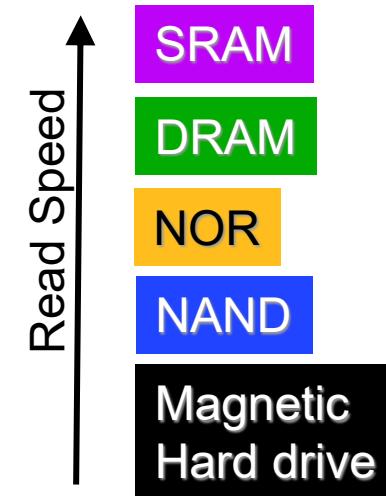
Power Consumption



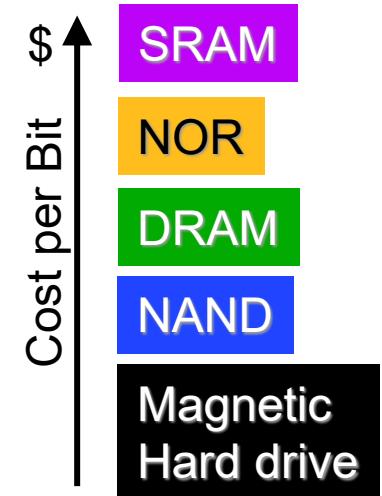
Write Speed



Read Speed



Cost per Bit



Lower is better  
to extend battery charge  
in mobile devices and reduce  
operating costs in data centers

Higher is better  
for faster operation

Higher is better  
for faster operation

Lower is better  
for higher density  
at similar price point

DRAM = Dynamic Random Access Memory  
DDR = Double Data Rate  
LPDDR = Low Power Double Data Rate  
GDDR = Graphics Double Data Rate  
HBM = High Bandwidth Memory

# DRAM (DDR, LPDDR, GDDR & HBM)

Smartphone

Automotive  
ADAS

Data Center

Personal  
Computing

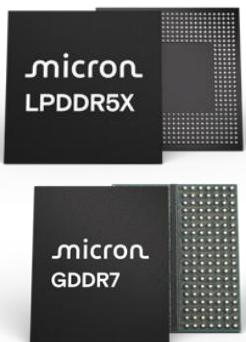
PC Gaming

Game Console

Content  
Creation



Smart factory &  
Robotics



- High-performance volatile memory
- Modules & components
- Low power consumption
- High-bandwidth
- System level solutions

Industrial IoT  
Applications

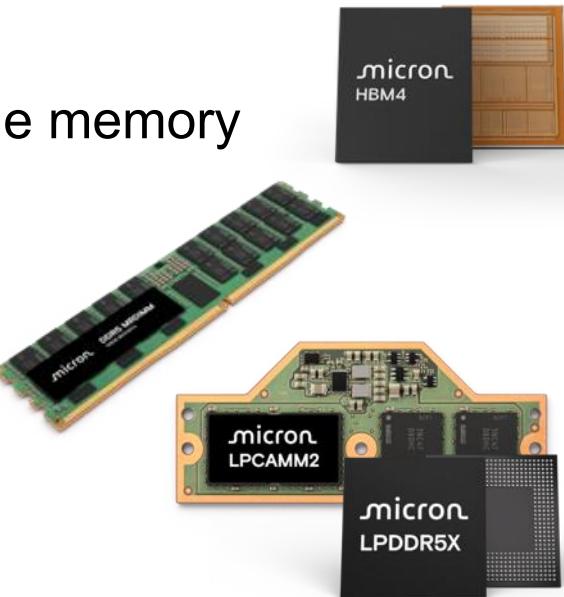
Telco & Edge

Aerospace and  
Defense

Database/  
Hypervisor

Generative AI

Medical  
Equipment



AR/VR  
Applications

Work from  
Anywhere

ADAS = Advanced Driver Assistance Systems  
AI = Artificial Intelligence  
AR = Augmented Reality  
IoT = Internet of Things  
VR = Virtual Reality

# Flash Memory (NAND and NOR)

Smartphone

Automotive  
ADAS

Data Center

Personal  
Computing

Portable  
Storage

Game Console

Video  
Surveillance



- Long-term memory storage
- Security Protection
- Low Power Consumption
- Reprogrammable
- Booting Software

Smart factory &  
Robotics



Industrial IoT  
Applications

Networking

Aerospace and  
Defense

Energy

Drones and  
Transport

Medical  
Equipment



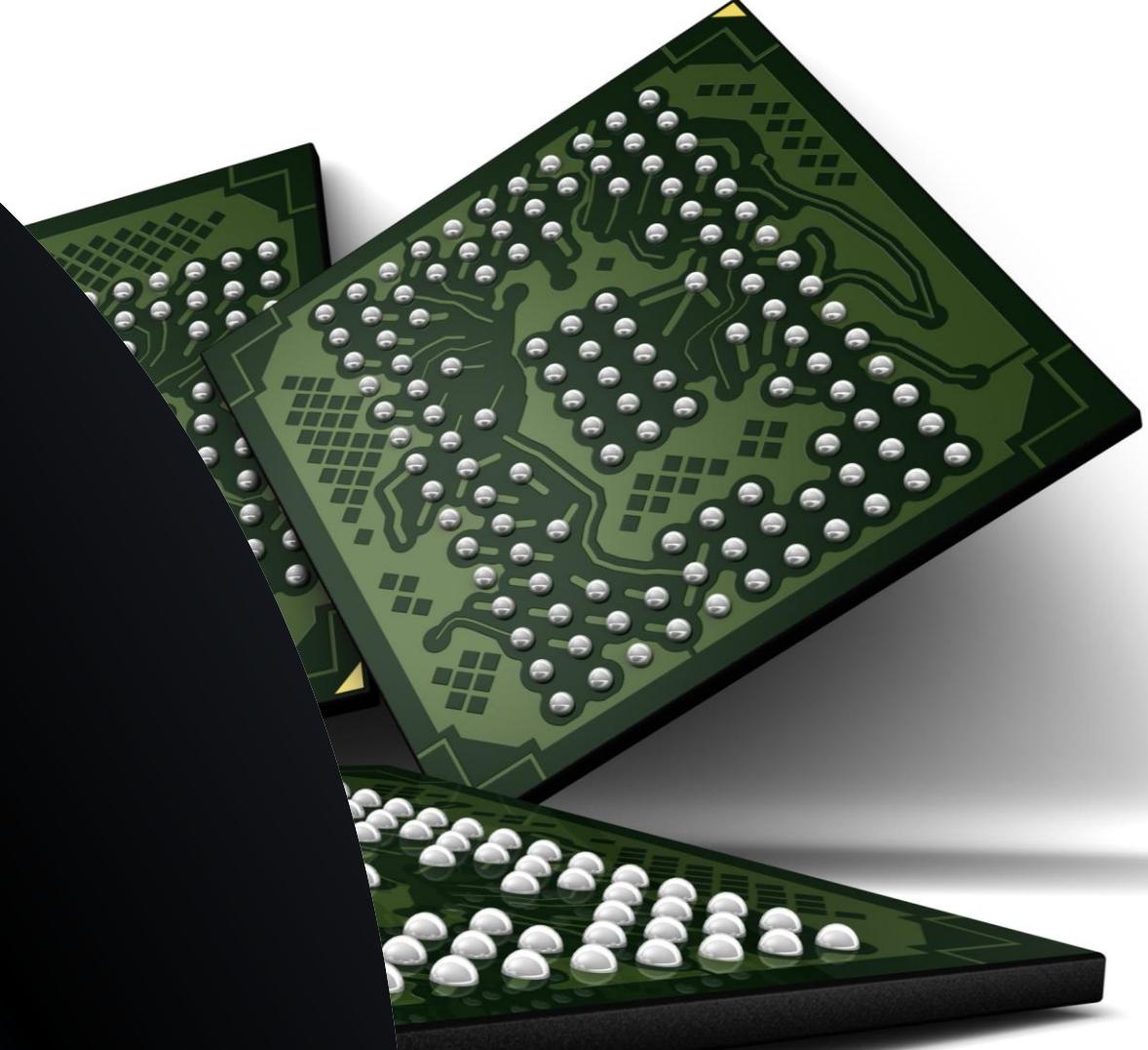
AR/VR  
Applications

Point of Sales /  
Wearable

# 3. Semiconductor Devices Overview

Fundamentals | Capacitors | Transistors

micron



# Conductors, Insulators & Semiconductor Materials

## Conductors

- Allow electrical current to flow easily
- Conductors used in integrated circuits are mostly metals: Aluminum, Tungsten and Copper

## Insulators

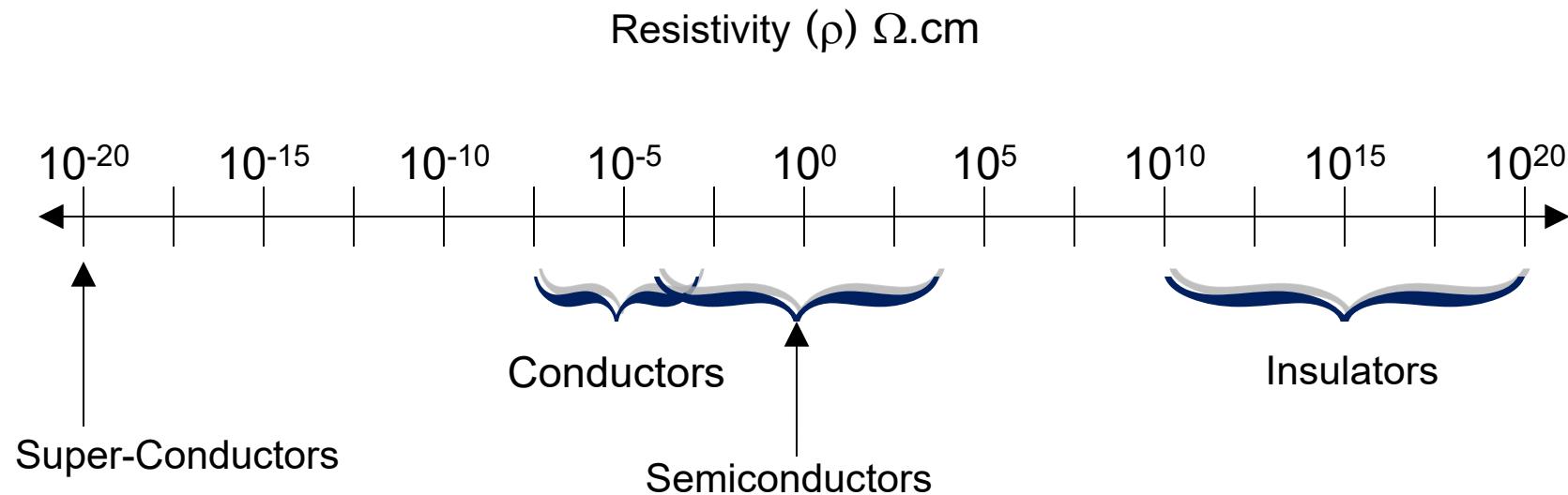
- Very resistive to electrical current flow
- Used to electrically isolate one part of the circuit from another
- Some insulators used in integrated circuits: Silicon dioxide and Silicon nitride

## Semiconductors

- Between conductors and insulators on the resistivity scale
- The semiconductor used in Micron is Silicon
- Silicon resistivity can be changed via “doping” (see upcoming slide)

# Resistivity Scale

- Electrical resistivity is a measure of how strongly a material opposes the flow of electric current.
- Low resistivity indicates a material that readily allows the movement of electrical charge.



# Semiconductor Doping

## Intrinsic (pure) Silicon

- Very resistive to electrical current flow
- Intrinsic silicon has very few applications in memory chips
- Silicon has 4 valence electrons (in outer shell)

## Doped Silicon

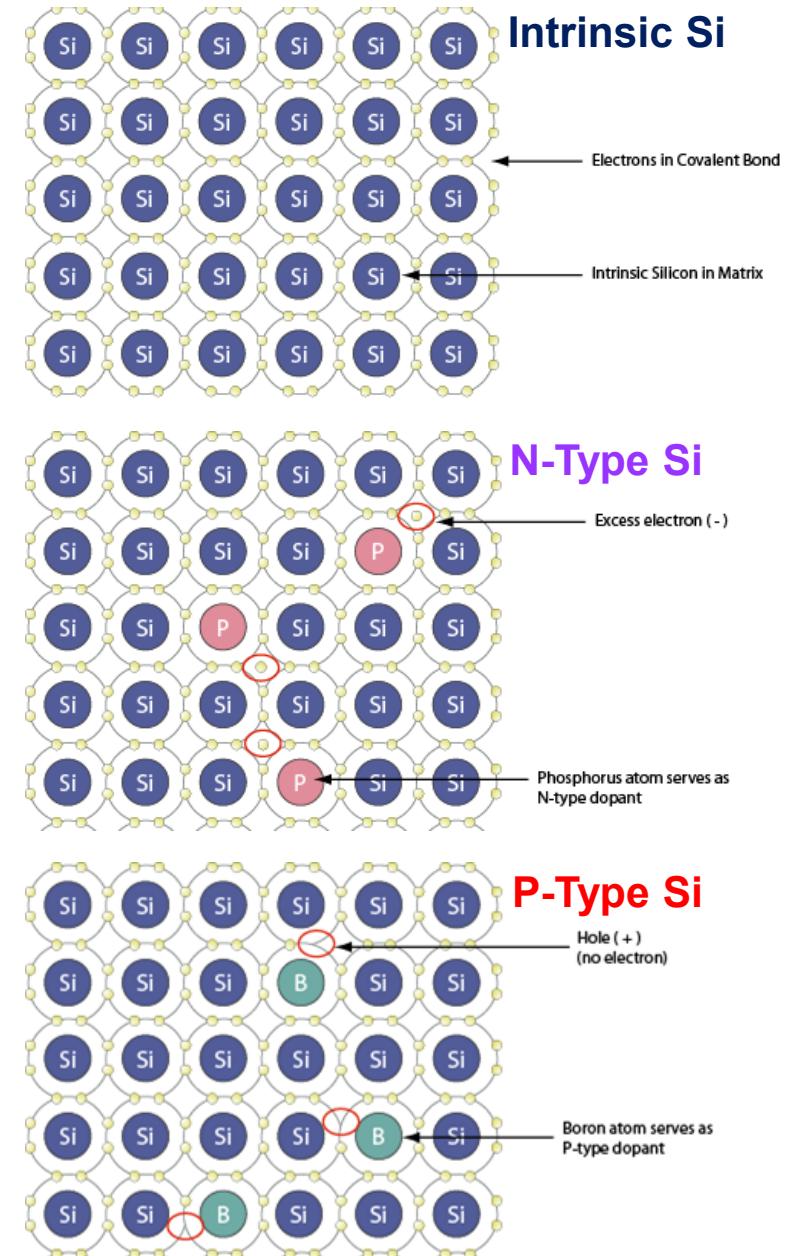
- A small percentage of impurities (“dopants”) are added to the silicon
- Dopants reduce the resistance of the silicon
- Dopants can be “N-type” or P-type”

## N-Type Silicon

- Most common N-Type Dopants are Arsenic (As) or Phosphorous (P)
- Current is carried by electrons that have a negative charge (N-Type)
- Phosphorous and Arsenic have 5 valence electrons (in outer shell)

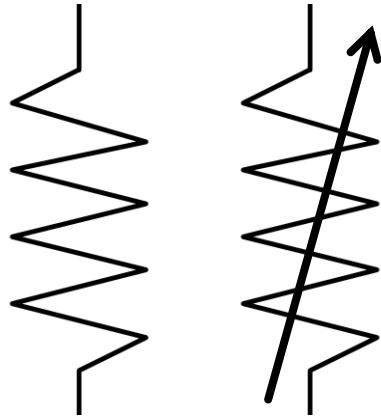
## P-Type Silicon

- Most common P-Type Dopants is Boron (B)
- Current is carried by “holes” that have a positive charge (P-Type)
- Boron has 3 valence electrons (in outer shell)



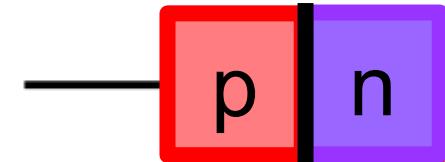
# Important Semiconductor Components

Resistors



- Reduces or limits current flow

Diodes



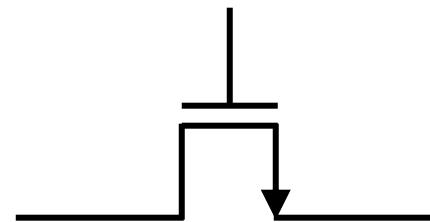
- Allows current to flow in one direction
- Can be used to electrically isolate adjacent devices from each other

Capacitors



- Stores an electrical charge
- Has two conductive plates separated by an insulator

Transistors

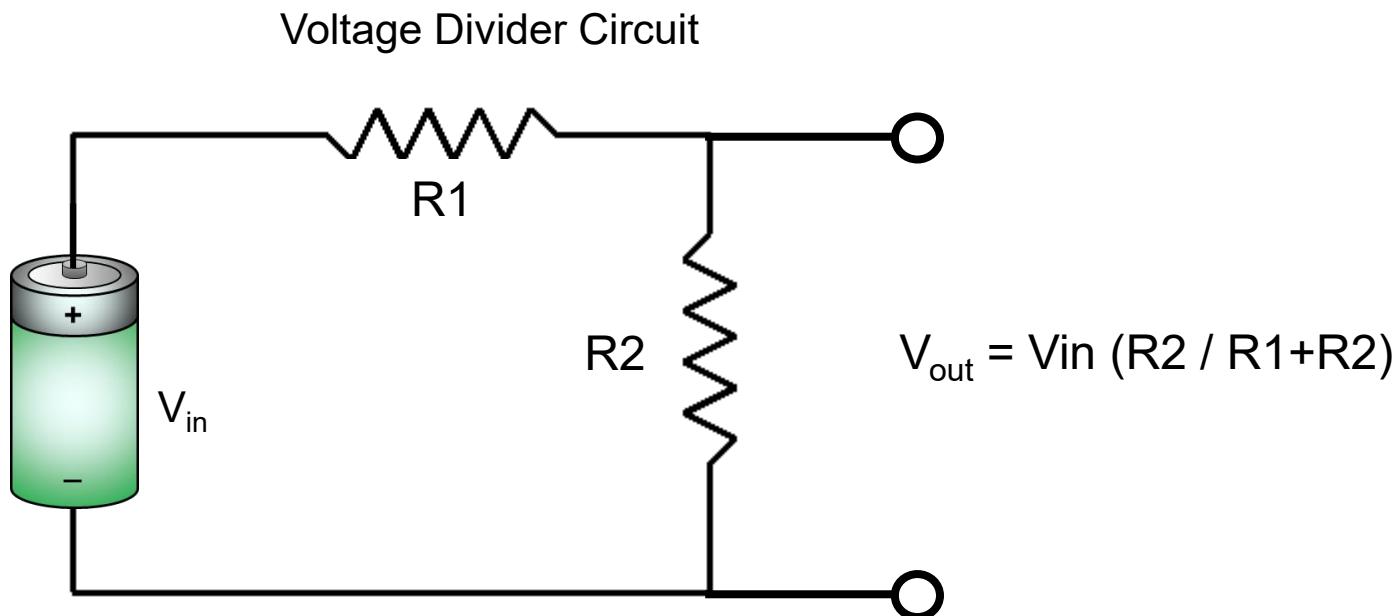


- Controls current flow
- Can function like a switch or valve

# Resistors

**Definition:** A device that reduces or limits current flow

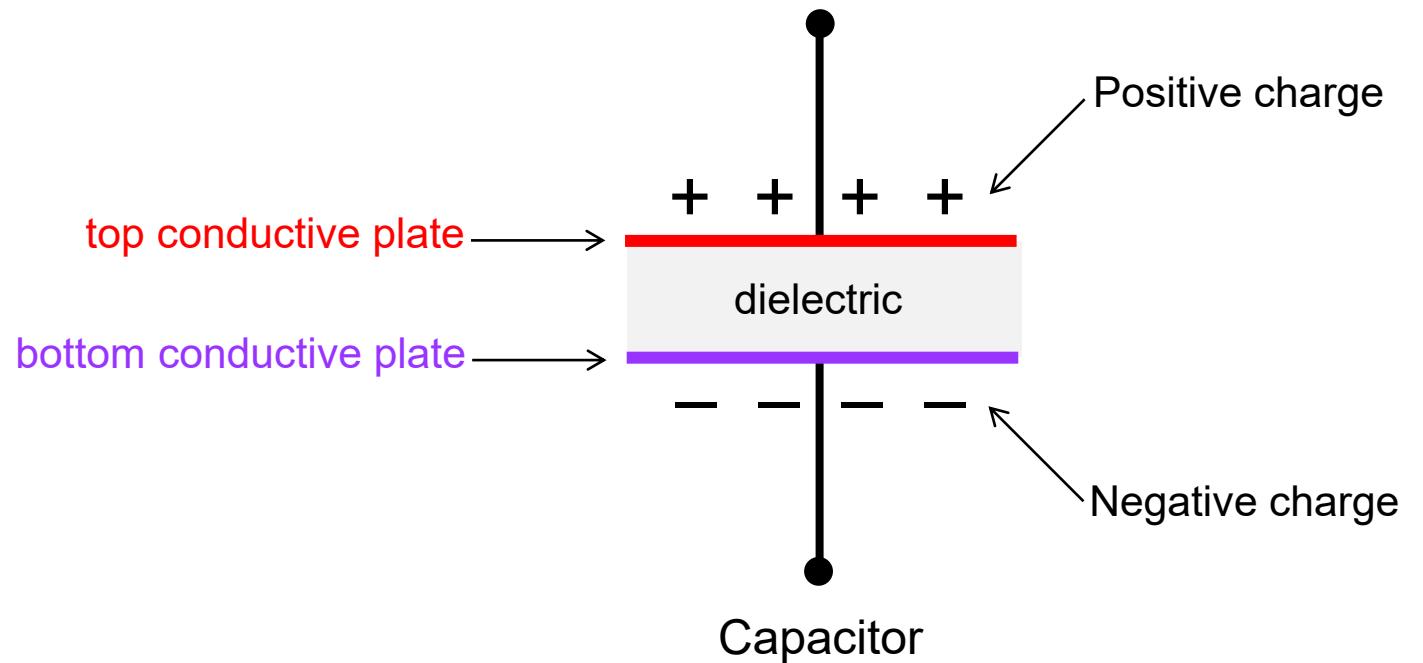
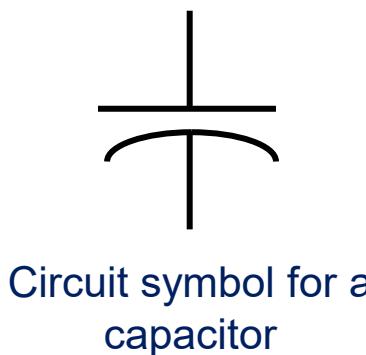
- A resistor is created by using a material less conductive (more resistive) anywhere along the path of current flow
- Resistors can have a fixed  or variable  resistance value



# Capacitors

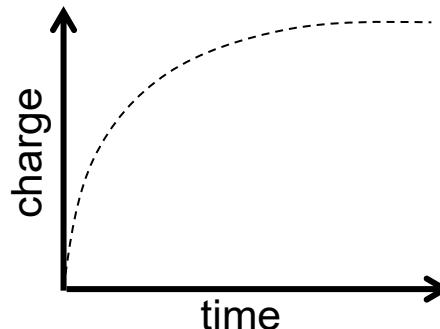
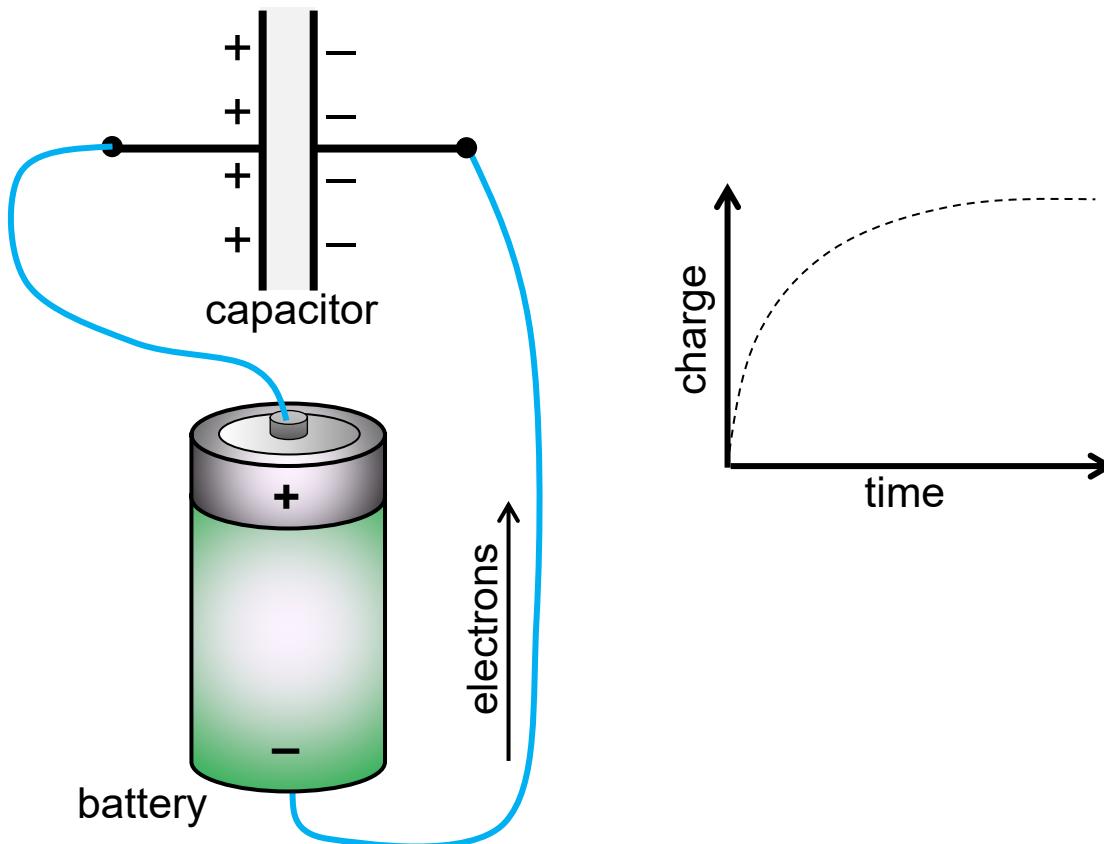
**Definition:** An electronic device used to store electric charge

- A capacitor consists of:
  - Two conductive “plates” – we arbitrarily call them “top” and “bottom” plates
  - An insulating layer known as a “dielectric” that electrically separates the two plates
- Opposite charges on the plates are held in place by their mutual attraction, but they cannot cross the dielectric layer



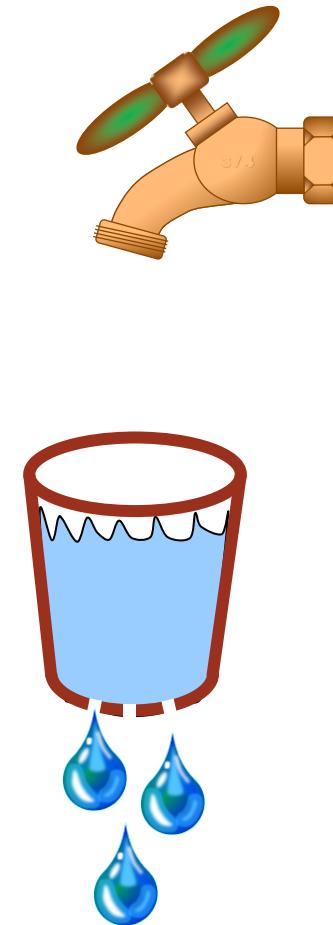
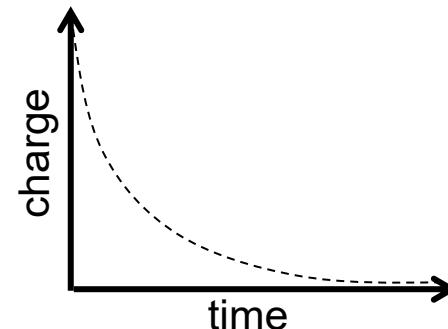
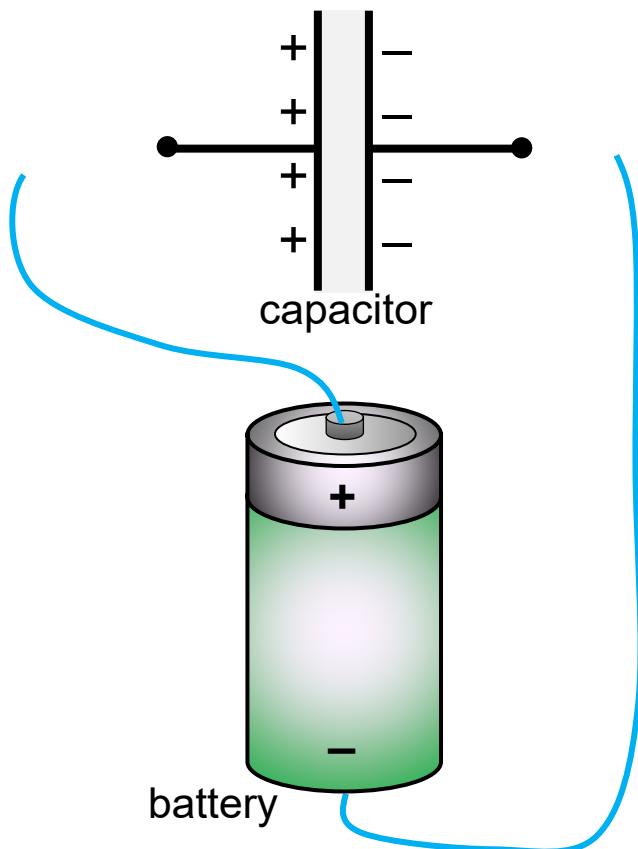
# Capacitors

- If a capacitor is hooked up to a power source, such as a battery, the capacitor will “charge up” until it can hold no more charge
- Analogy: This is like filling a bucket with water until it can hold no more water



# Capacitors

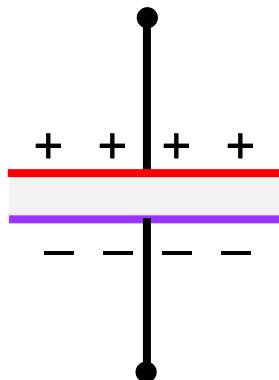
- When the battery is disconnected, the capacitor will gradually begin to lose the charge. This is known as “discharging”.
- Analogy: This is like water slowly leaking out of small holes in a bucket



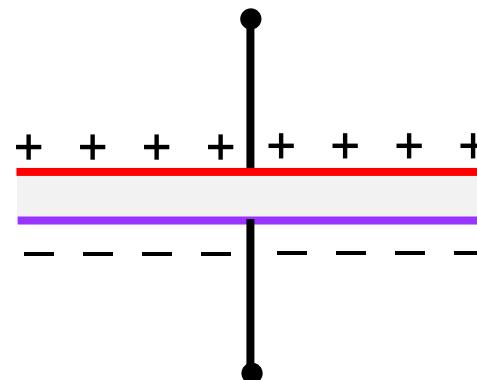
# Capacitors

How much charge (Q) can a capacitor hold?

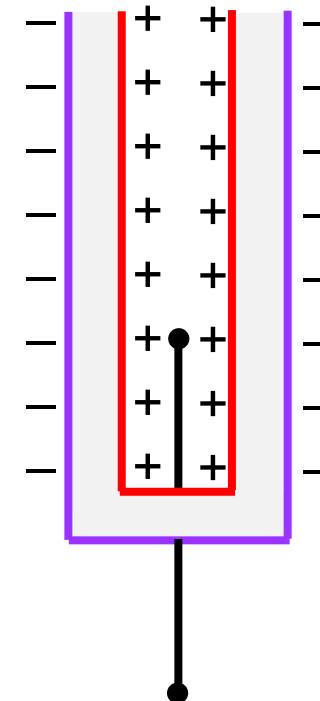
- As the surface area of the conductive plates is increased, the capacitor can hold more charge.
- Note: The plates do not have to be flat!
- The charge (Q) stored in a capacitor, under a given voltage (V), is called the “capacitance.”



Small flat plates →  
less charge can be  
stored



Large flat plates →  
more charge can be stored but  
require more X x Y area on  
wafer surface



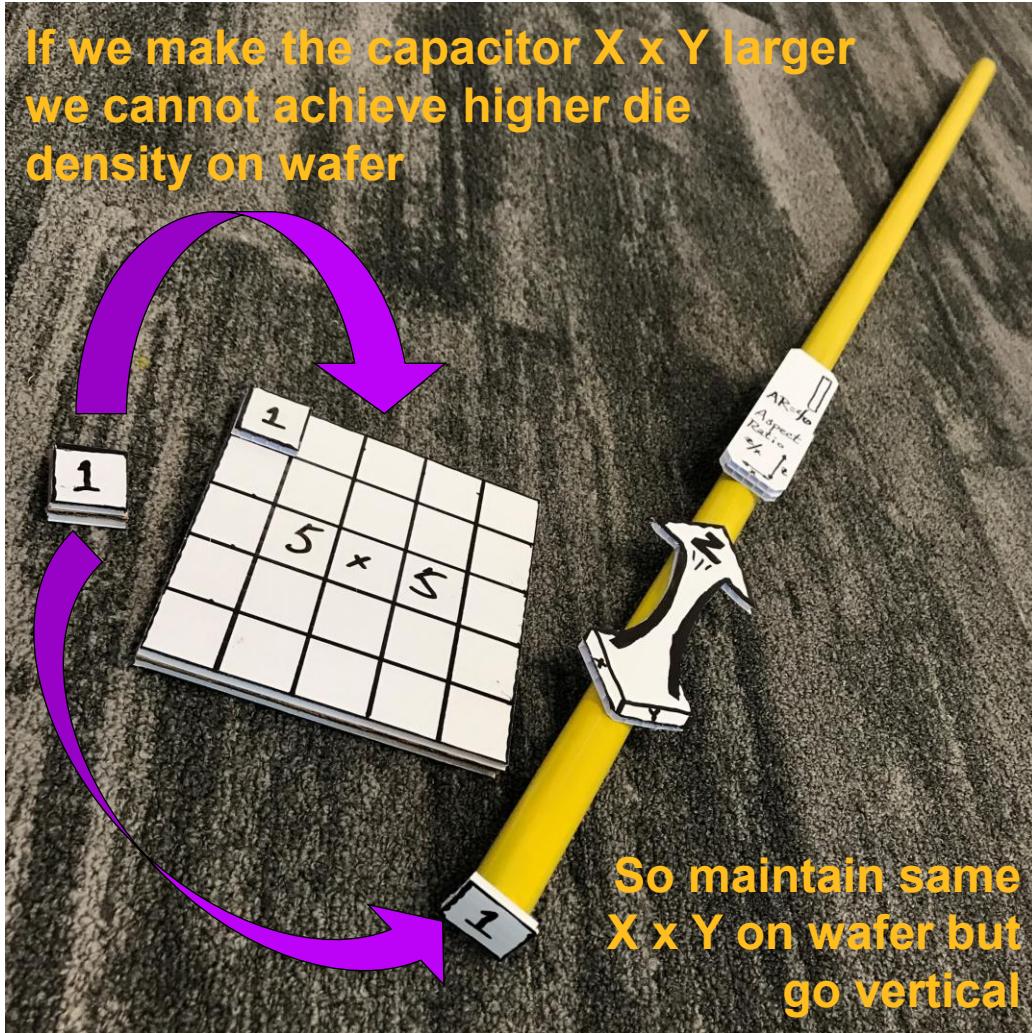
Large cylindrical plates →  
even more charge can be  
stored with less area on the  
wafer!

$$Q = \text{Capacitance} \times \text{Applied Voltage}$$

$$Q = C \times V$$

$$C \approx k \times \text{plate area} / \text{spacing}$$

# Into the Z Dimension!

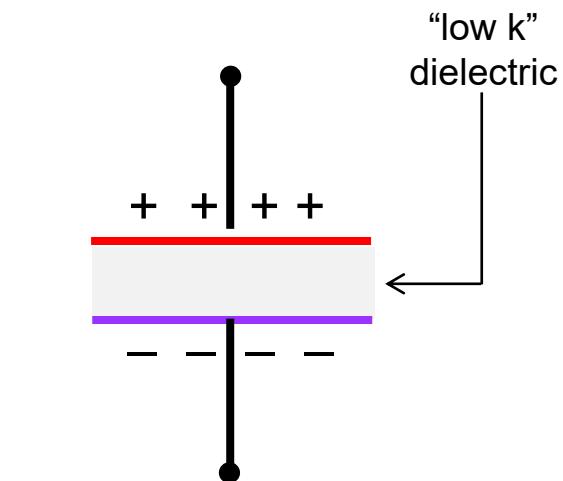


# Capacitors

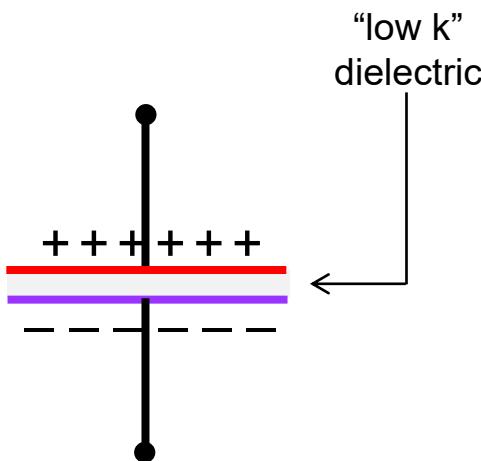
How much charge can a capacitor hold?

$$C \approx k \times \text{plate area} / \text{spacing}$$

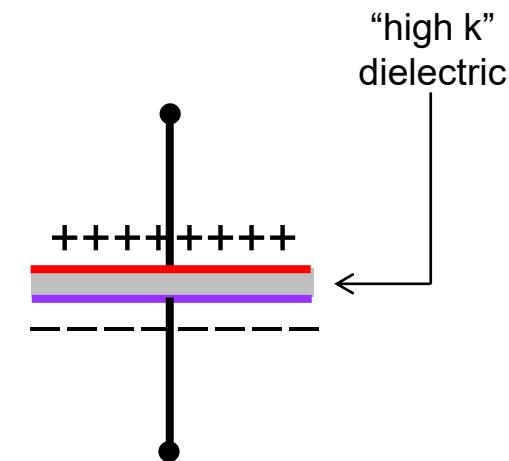
- As the spacing between the plates decreases, the capacitor can hold more charge. This spacing can also be thought as the dielectric thickness.
- The choice of dielectric material can also increase the amount of charge that can be stored.
  - “High k” dielectric materials can store more charge.



Wide space between plates → less charge can be stored



Narrow space between plates → more charge can be stored



Narrow space, with special dielectric → even more charge can be stored

<u>Dielectric Constant k</u>	
$\text{SiO}_2$	3.9
$\text{Si}_3\text{N}_4$	7.5
$\text{Ta}_2\text{O}_5$	22
$\text{HfO}_2$	25
$\text{ZrO}_2$	25
$\text{TiO}_2$	80

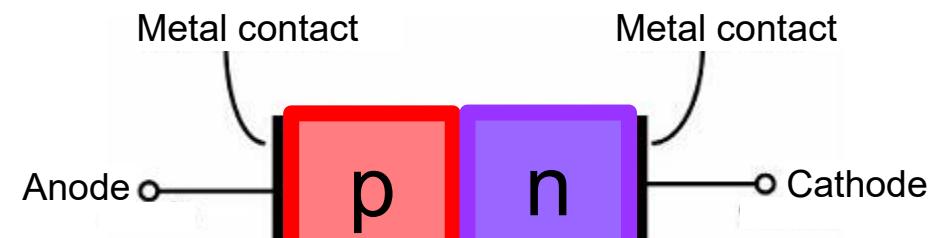
# Diodes

**Definition:** An electronic device that allows current to flow in one direction only

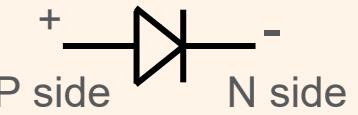
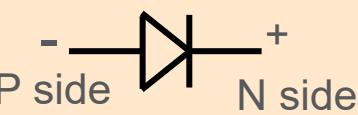
- Formed by connecting a P-type material with an N-type material



Schematic symbol for a diode

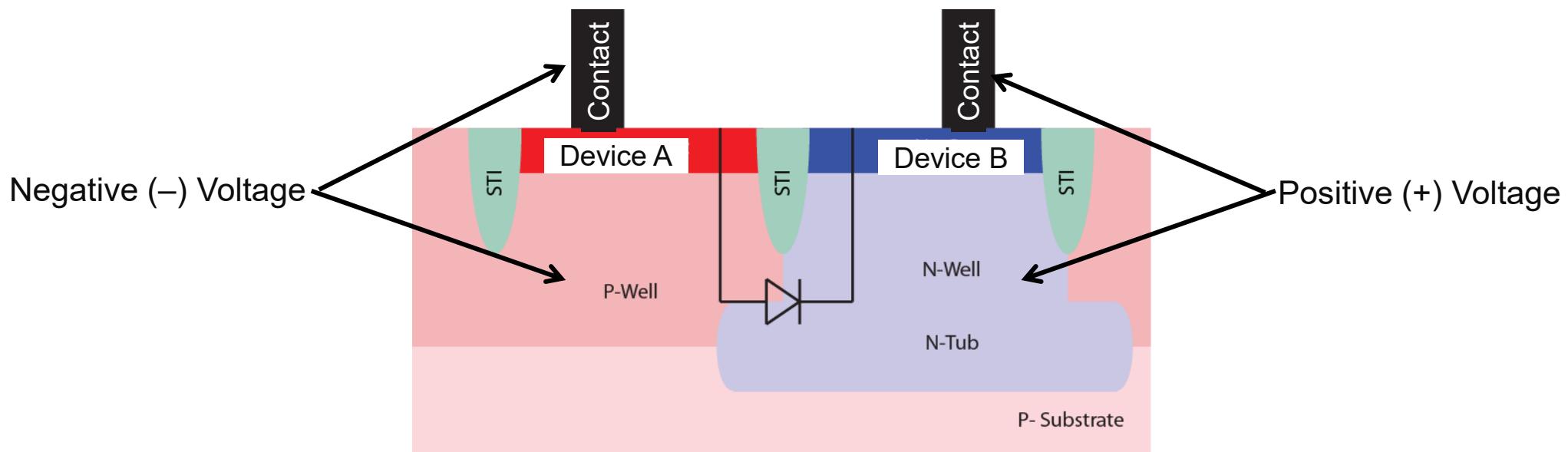


Simplified physical structure of a diode

Diodes	Forward biased:		Current flows
	Reverse biased:		Negligible current flows

# Diodes

- Diodes can be used to electrically isolate adjacent devices from each other
  - In the example below, the P-Well and N-Well form a diode where they meet
  - By applying a negative voltage to the P-Well and a positive voltage to the N-Well, the diode is reverse-biased, and current cannot flow between devices A and B

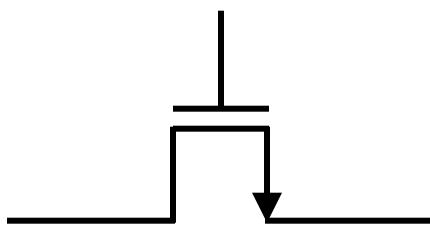


Key:  
STI: shallow trench isolation

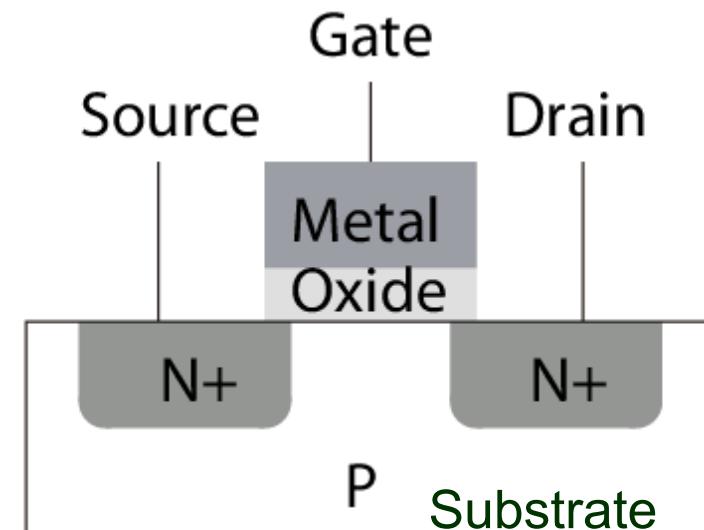
# Transistors

**Definition:** An electronic device that can control the current running through it – like an On/Off switch

- The most common type is the *Field Effect Transistor* (FET)
  - Used in digital applications
  - Low-power device
  - Still being scaled below 10 nm



Circuit symbol of a MOSFET Transistor



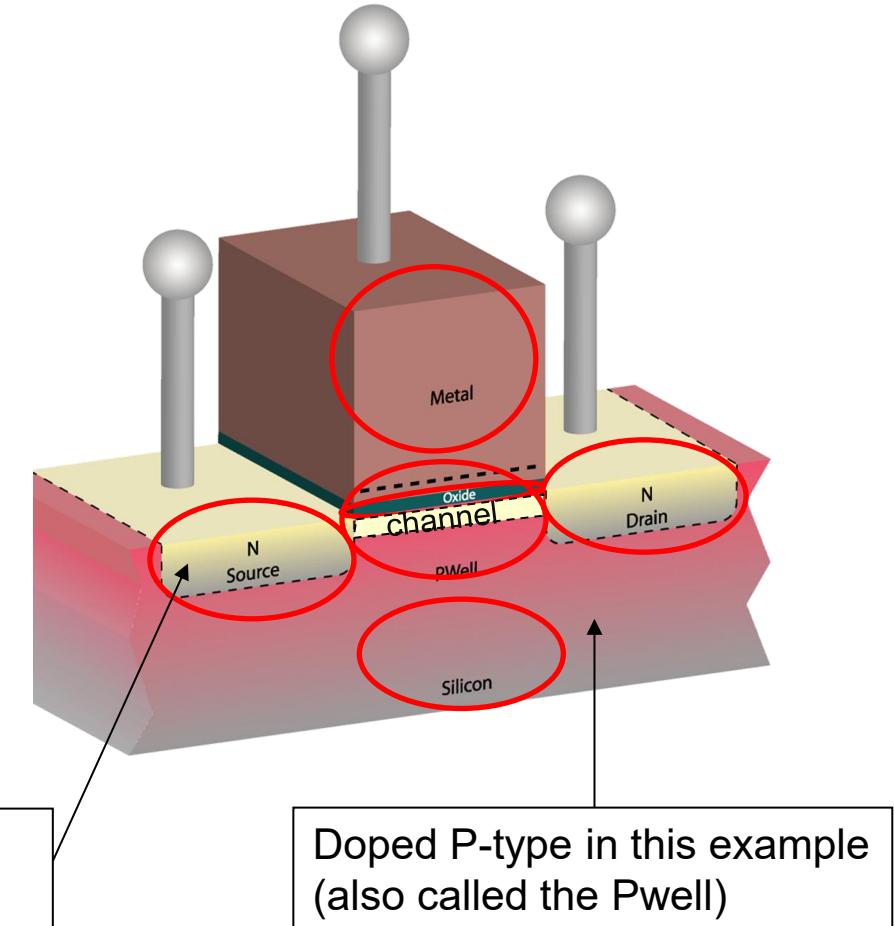
Structure of a MOSFET Transistor

MOSFET: Metal Oxide Semiconductor Field Effect Transistor

# MOSFET Overview

## Structure of a MOSFET

- Doped semiconductor (silicon) substrate
- Doped source and drain regions (oppositely doped from substrate)
- Insulating gate oxide
- Metal control gate on top of oxide is used to apply voltages that turn the transistor ON or OFF
- The “channel” is the region beneath the gate where electrons will flow from source to drain under the right conditions

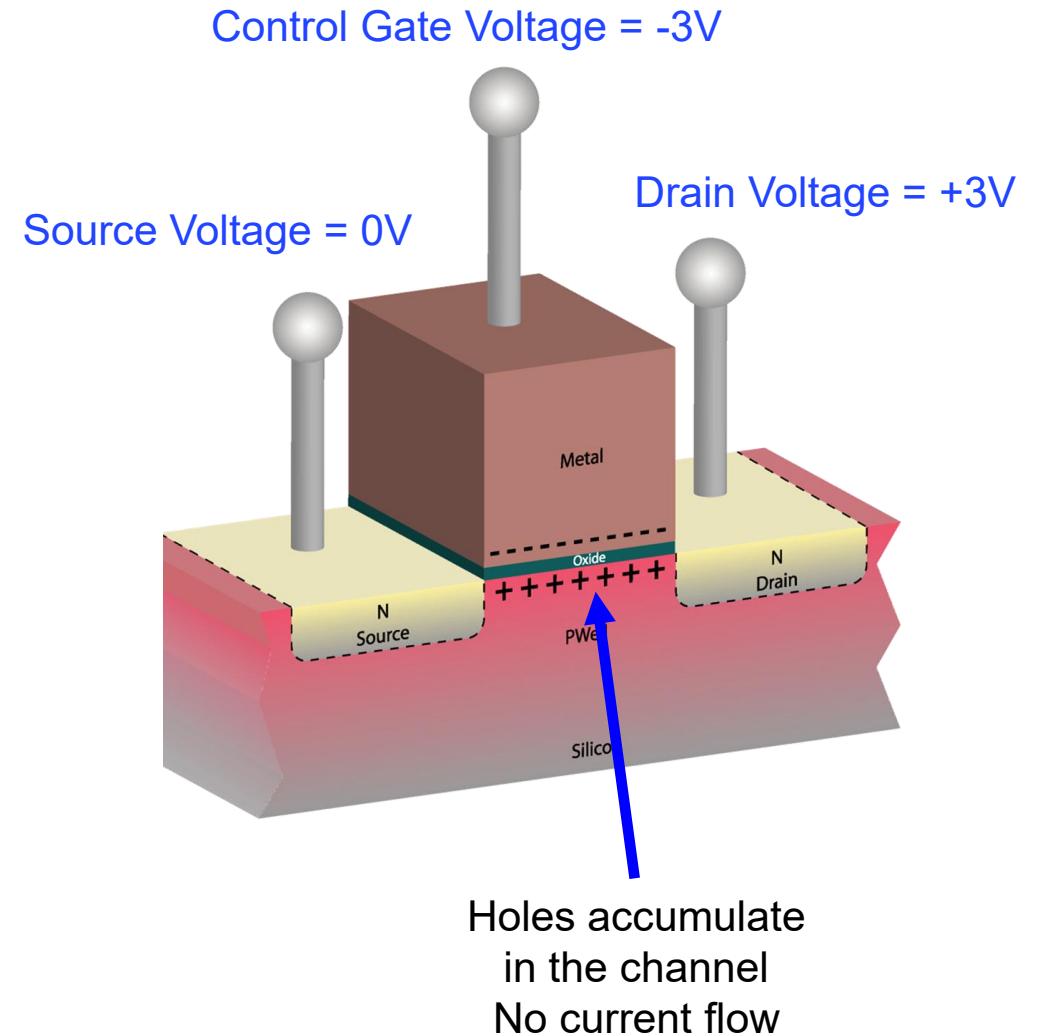


MOSFET: Metal Oxide Semiconductor Field Effect Transistor

# MOSFET Overview

## OFF STATE

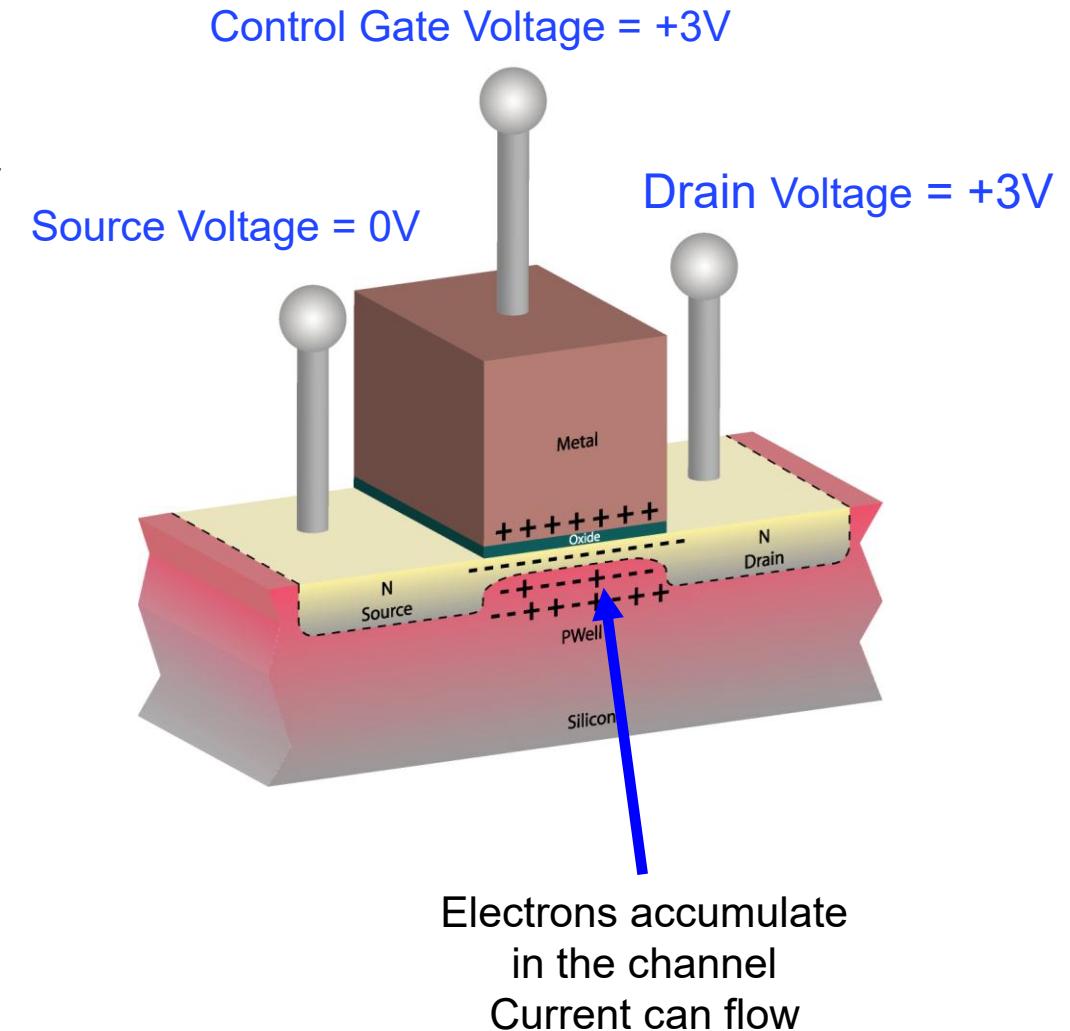
- Drain voltage is higher than source voltage, creating a voltage drop. Current could flow through the device under these conditions if the gate allows.
- Negative voltage applied to the control gate attracts positive charges (“holes”) into the channel region
- The holes in the channel act as a barrier so current cannot flow between the Source and Drain
- The transistor is OFF



# MOSFET Overview

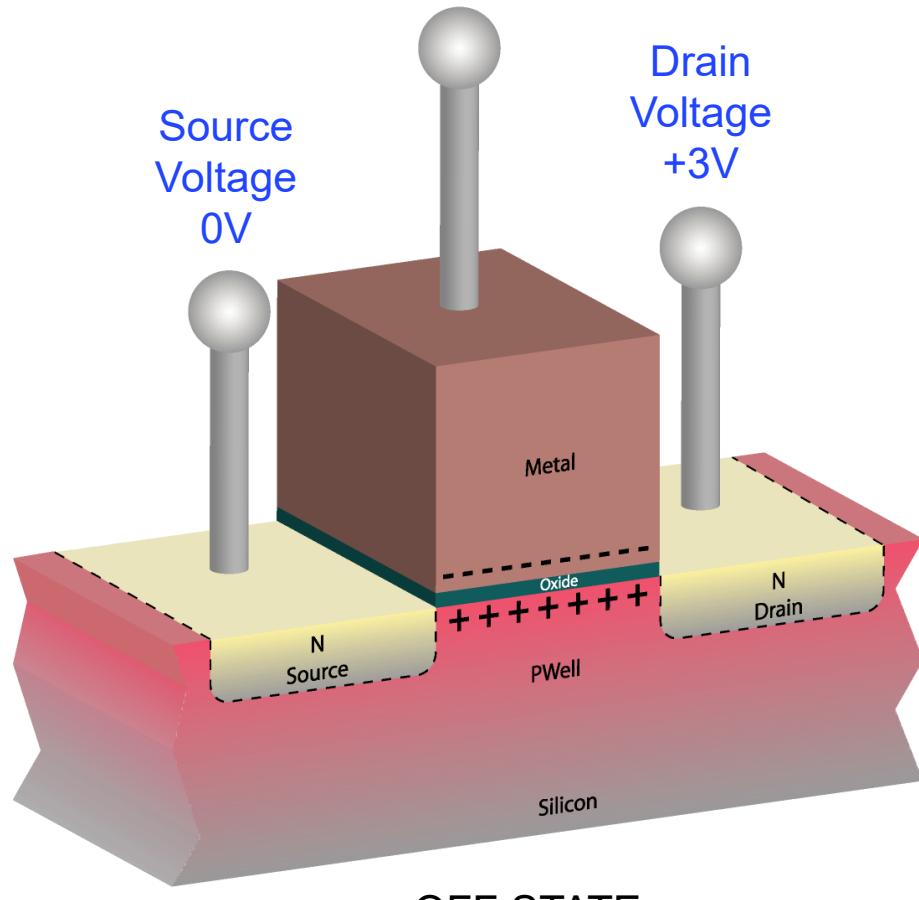
## ON STATE

- Drain voltage is higher than source voltage, creating a voltage drop. Current could flow through the device under these conditions if the gate allows.
- Positive voltage applied to the control gate attracts negative charges (electrons) into the channel region
- Electrons in the channel create an electrical connection between the Source and Drain, allowing current to flow
- The transistor is ON



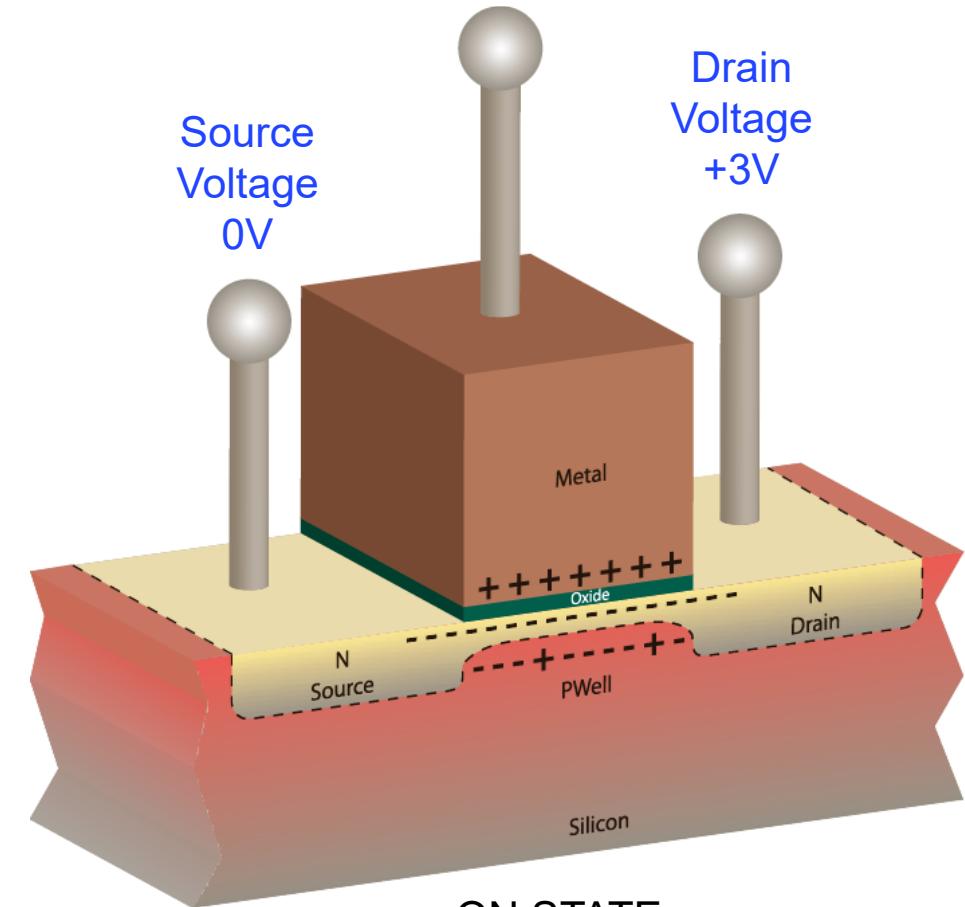
# MOSFET States: OFF and ON Summary

Control Gate Voltage = -3V



OFF STATE

Control Gate Voltage = +3V

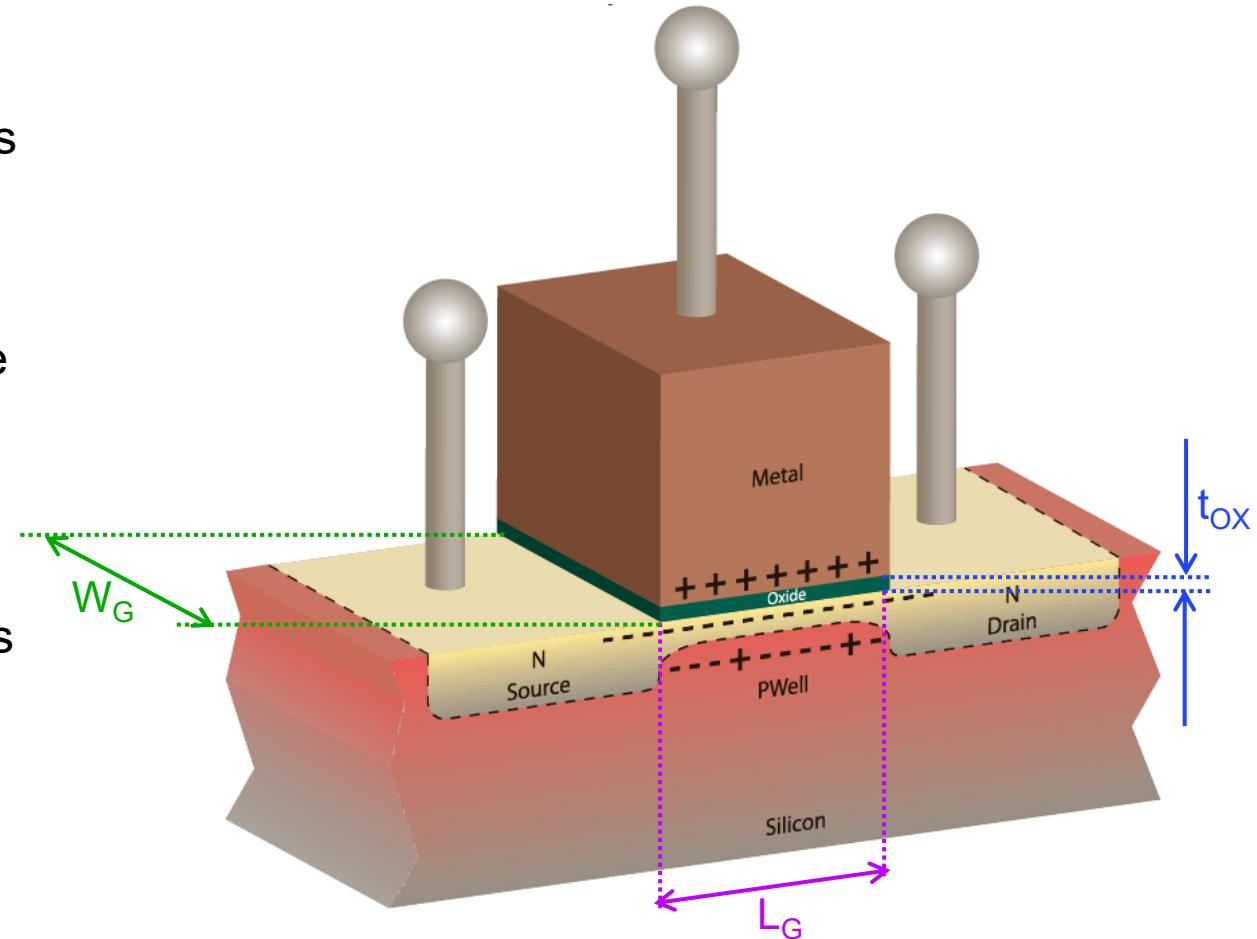


ON STATE

# MOSFET Transistor Dimensions

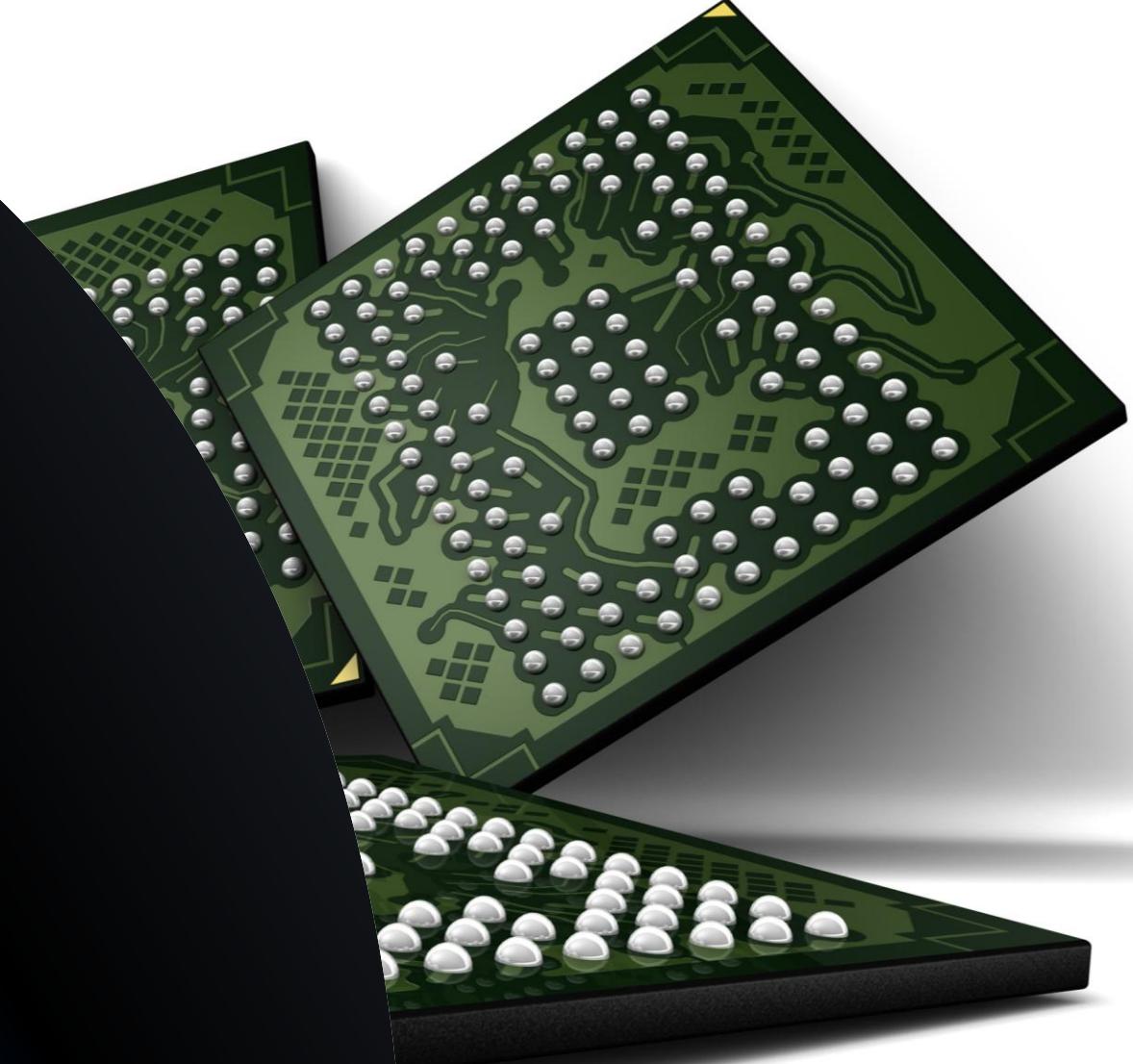
## Three Important Dimensions (but many others!):

- Gate Length ( $L_G$ ): As the gate length (channel) gets shorter, the device can switch faster. The tradeoff is an increase of leakage current in the off-state.
- Gate Width ( $W_G$ ): As the gate gets wider, more current can flow from drain to source in the on-state which improves circuit speed. The tradeoff is that more silicon area is needed.
- Gate Oxide Thickness ( $t_{ox}$ ): As the gate oxide gets thinner, the device can switch faster. The tradeoff is an increase of leakage current through the gate.



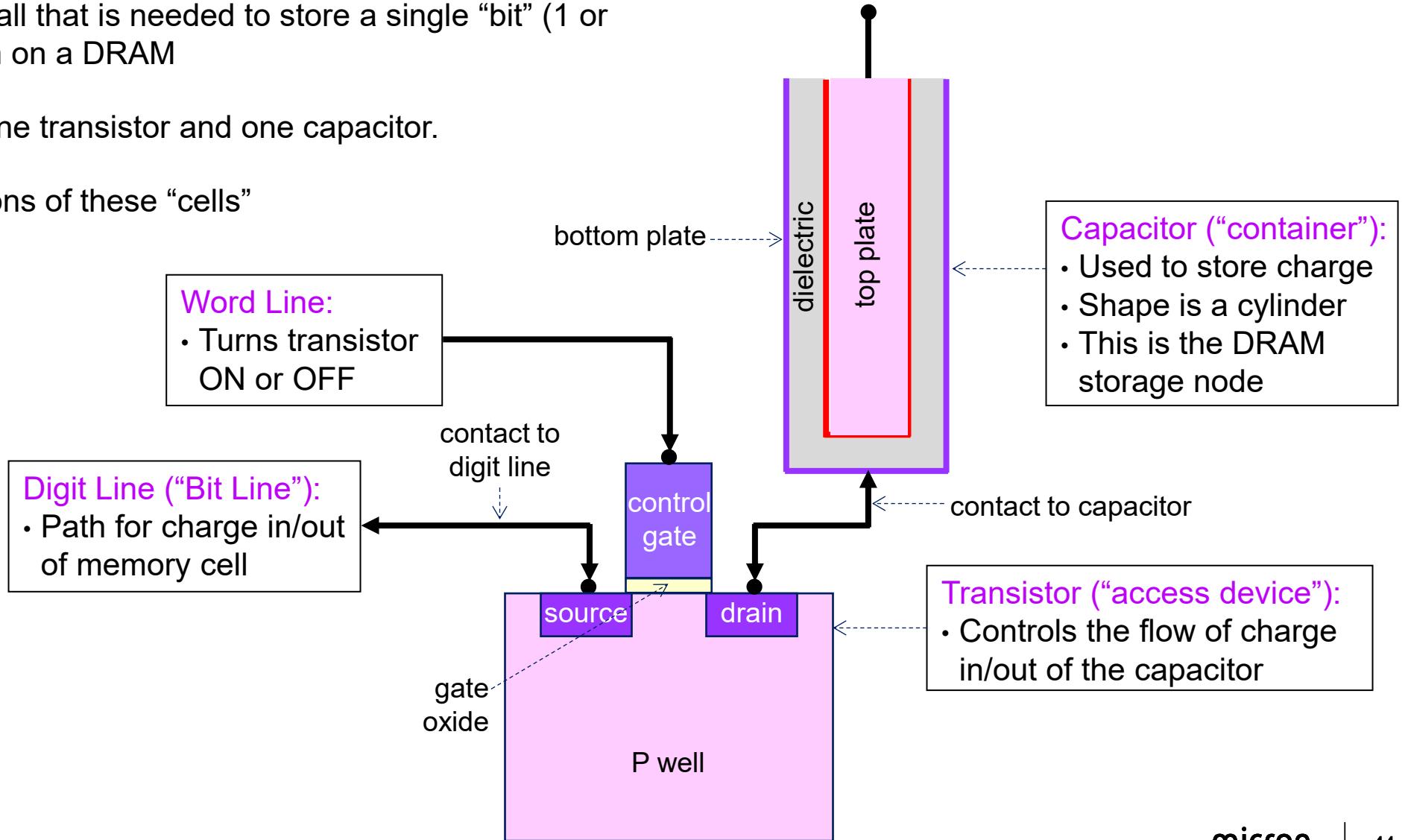
## 4. Introduction to DRAM

micron



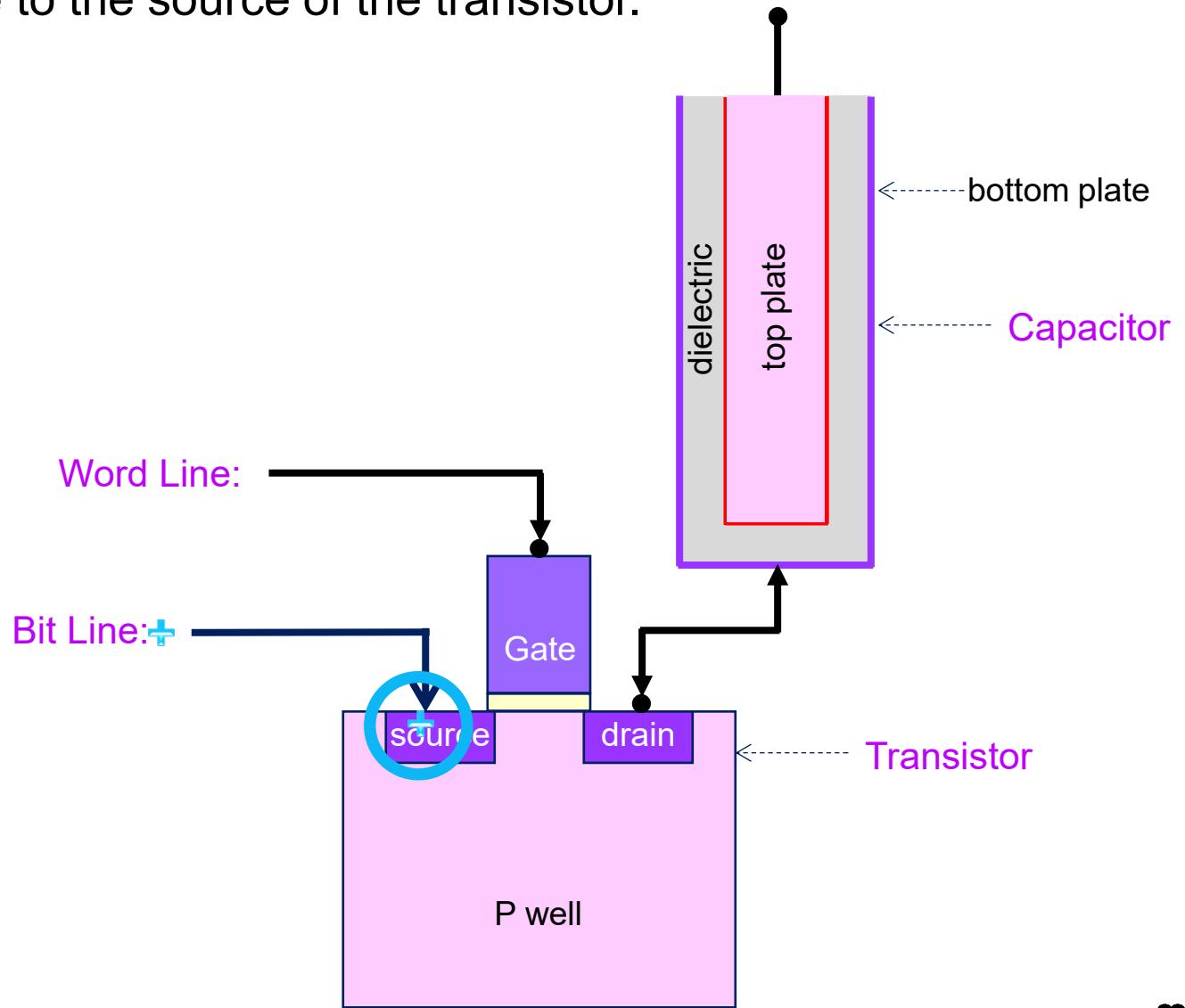
# Basic DRAM Memory Cell

- Shown on this slide is all that is needed to store a single “bit” (1 or 0) of digital information on a DRAM
- Each cell consists of one transistor and one capacitor.
- A DRAM chip has billions of these “cells”



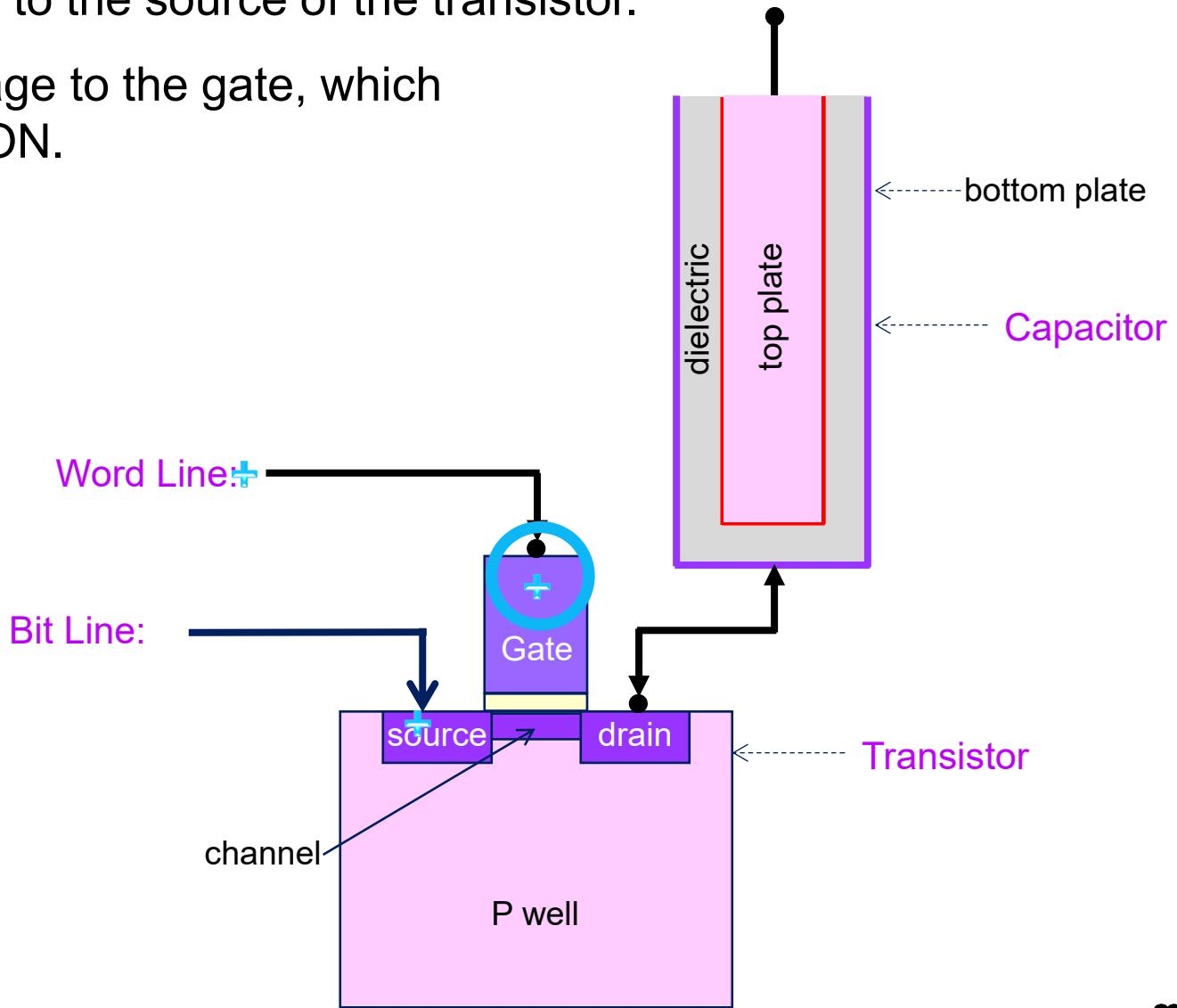
# DRAM Operation – Write

1. Bit Line delivers positive voltage to the source of the transistor.



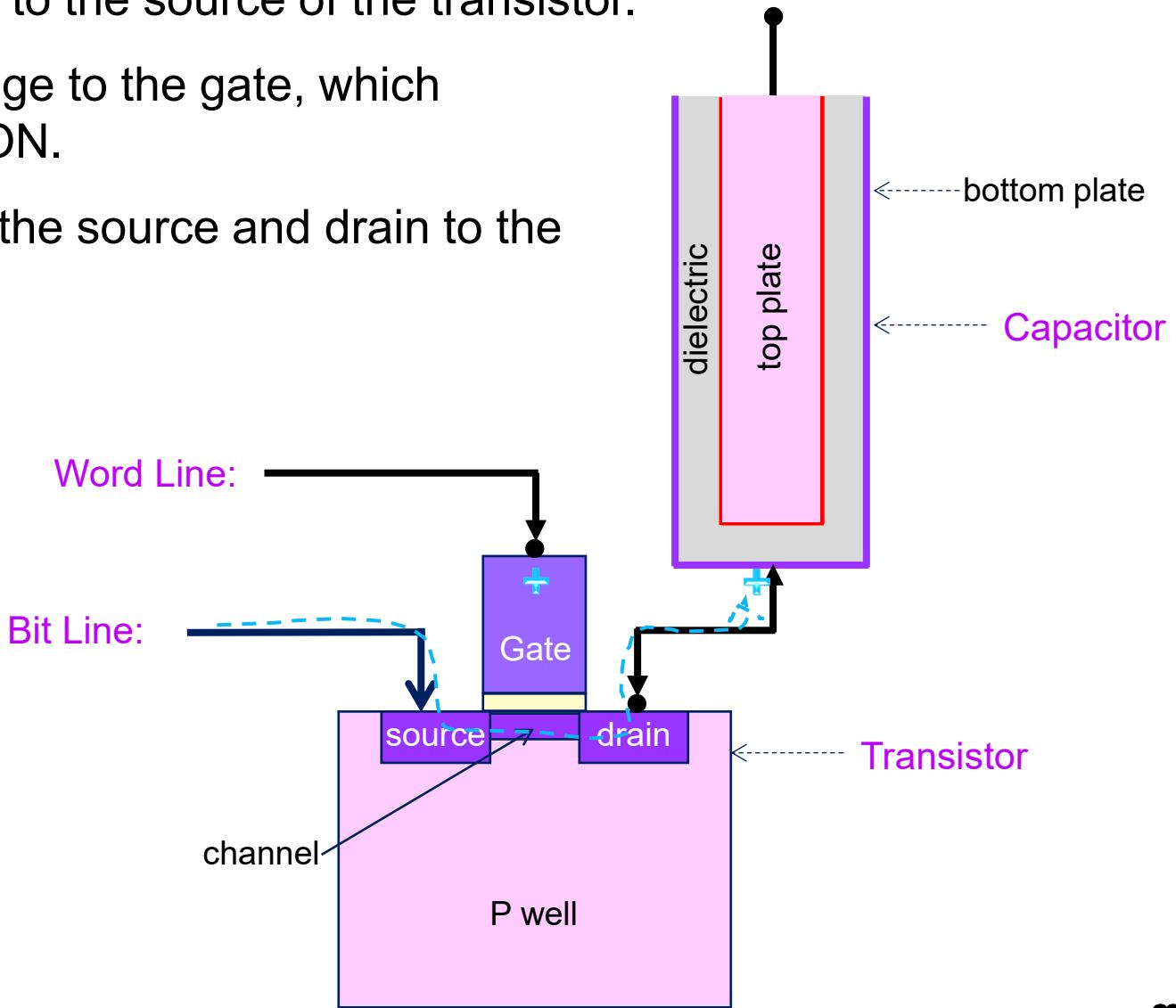
# DRAM Operation – Write

1. Bit Line delivers positive voltage to the source of the transistor.
2. Word Line delivers positive voltage to the gate, which creates the channel and turns it ON.



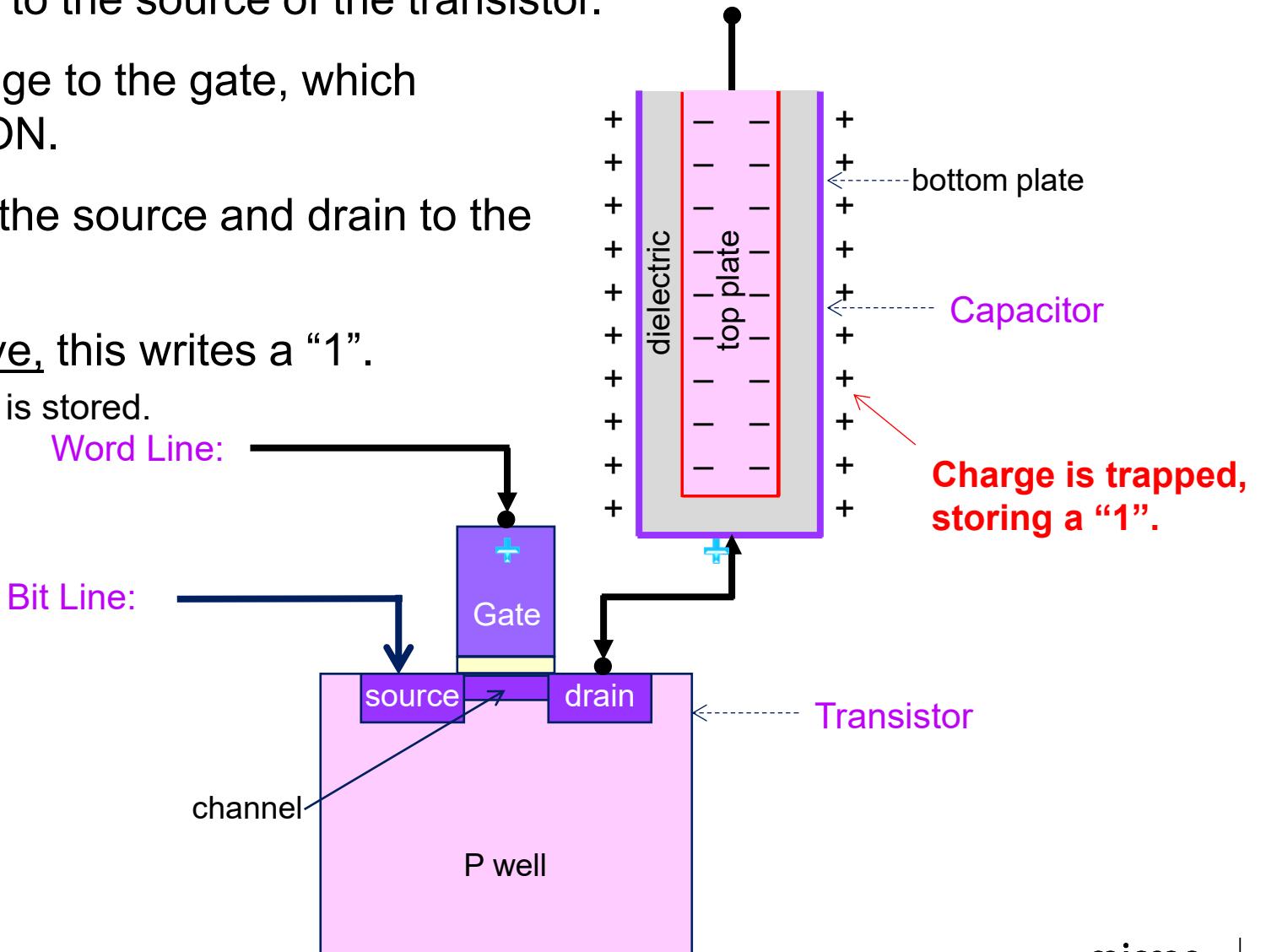
# DRAM Operation – Write

1. Bit Line delivers positive voltage to the source of the transistor.
2. Word Line delivers positive voltage to the gate, which creates the channel and turns it ON.
3. Bit Line voltage passes through the source and drain to the capacitor.



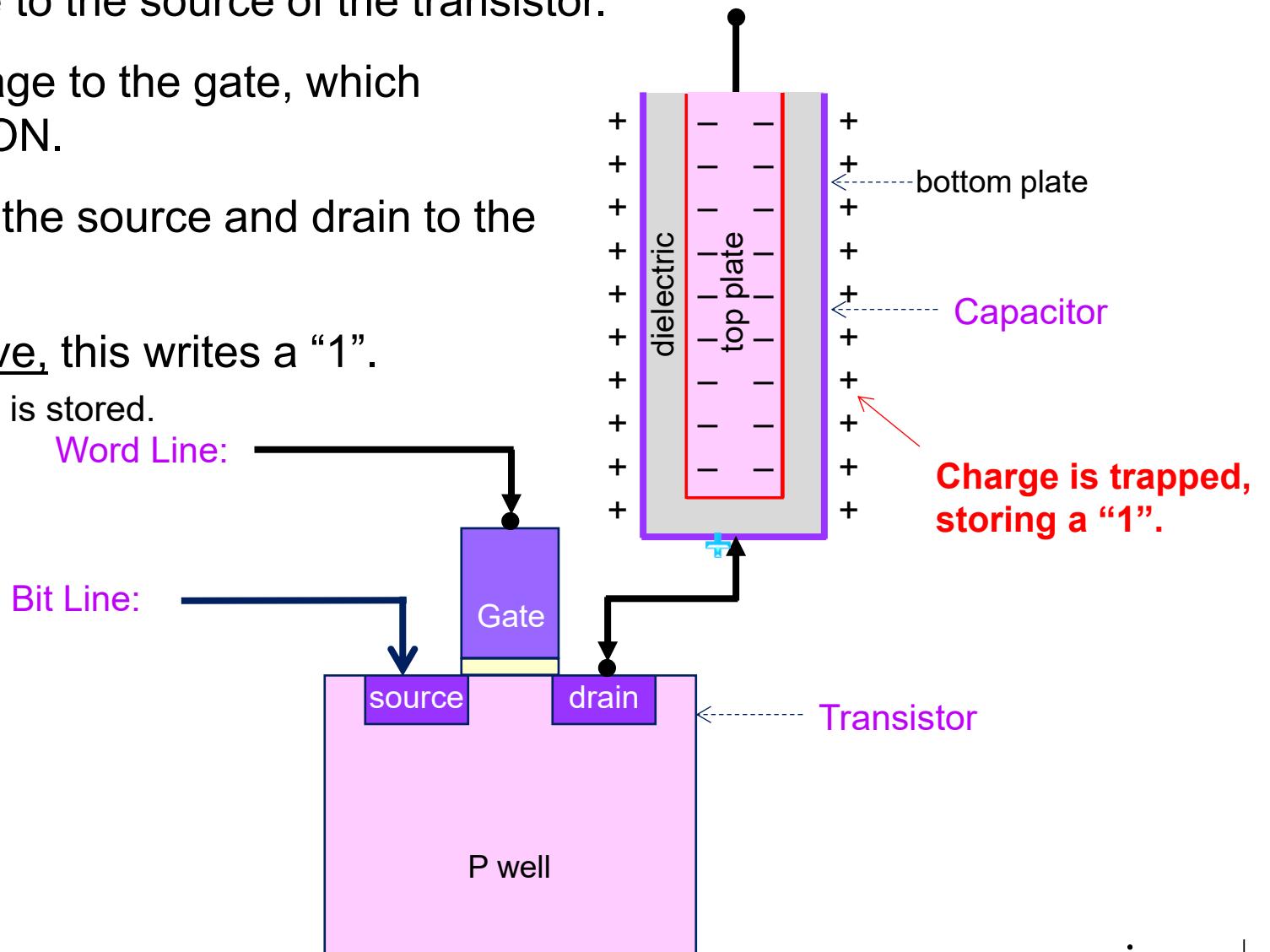
# DRAM Operation – Write

1. Bit Line delivers positive voltage to the source of the transistor.
2. Word Line delivers positive voltage to the gate, which creates the channel and turns it ON.
3. Bit Line voltage passes through the source and drain to the capacitor.
4. The bottom plate charges positive, this writes a “1”.
  - If bottom plate charges negative, a “0” is stored.



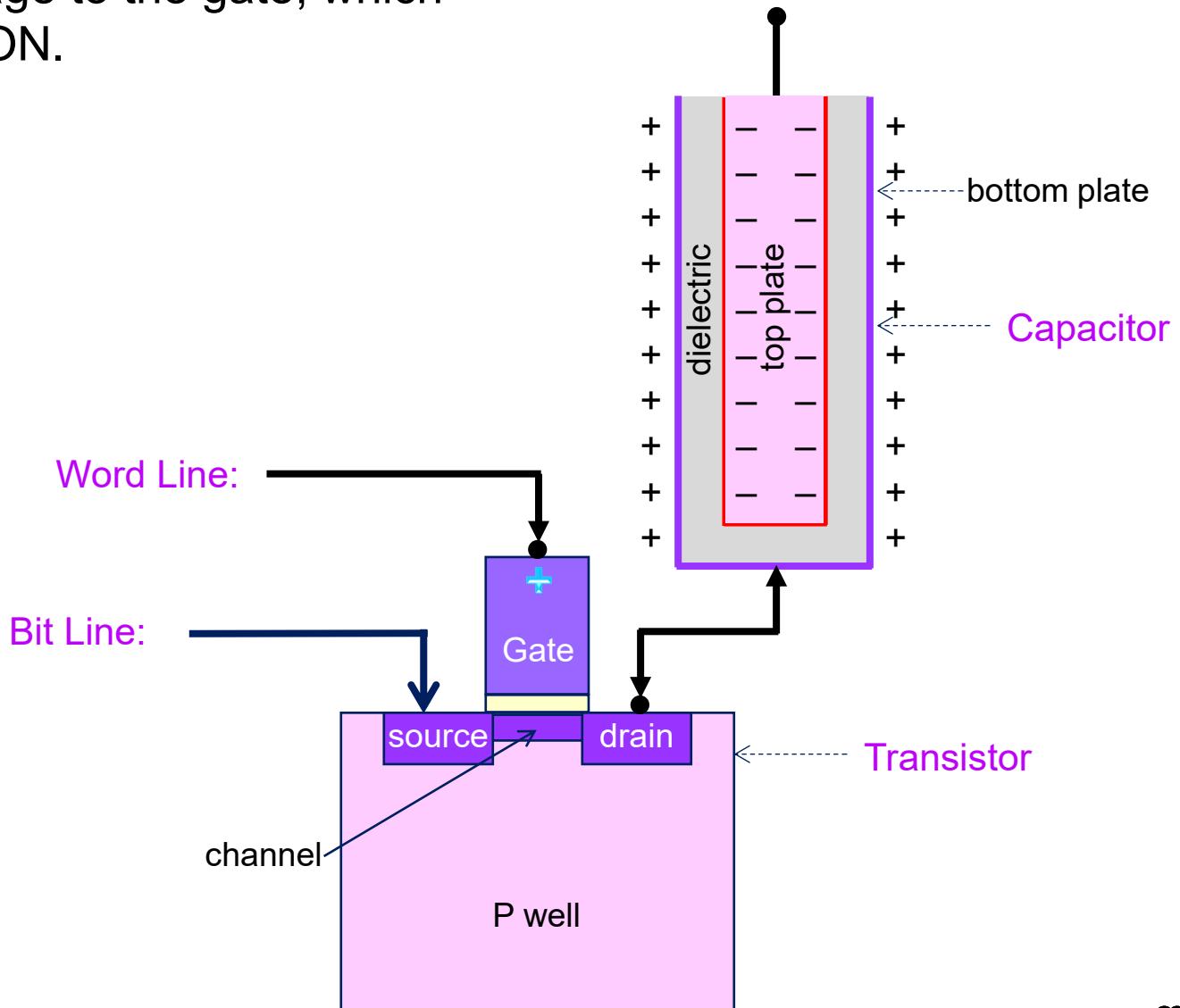
# DRAM Operation – Write

1. Bit Line delivers positive voltage to the source of the transistor.
2. Word Line delivers positive voltage to the gate, which creates the channel and turns it ON.
3. Bit Line voltage passes through the source and drain to the capacitor.
4. The bottom plate charges positive, this writes a “1”.
  - If bottom plate charges negative, a “0” is stored.
5. Word Line turns off transistor, “trapping” the charge on the capacitor.



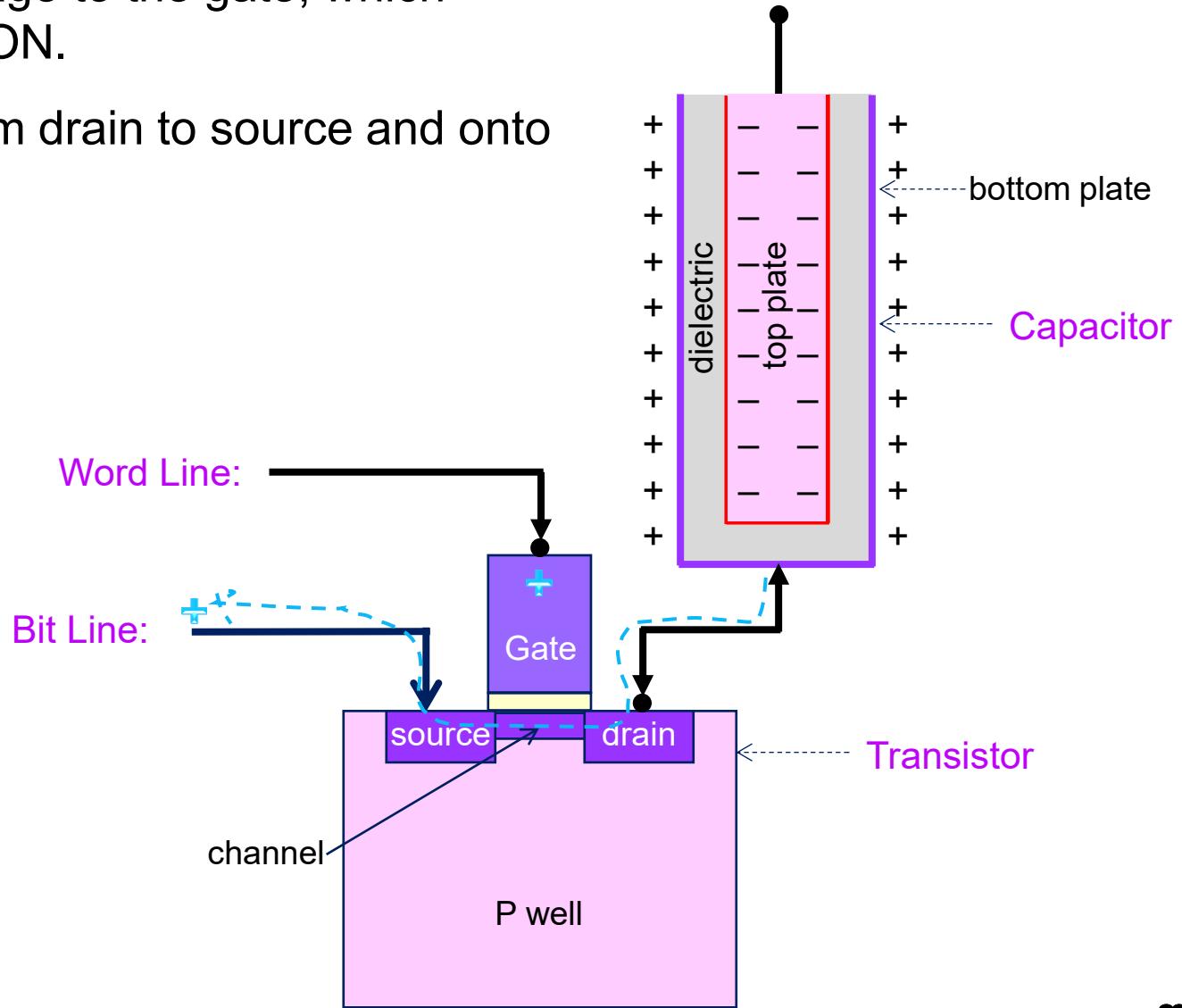
# DRAM Operation – Read

1. Word Line delivers positive voltage to the gate, which creates the channel and turns it ON.



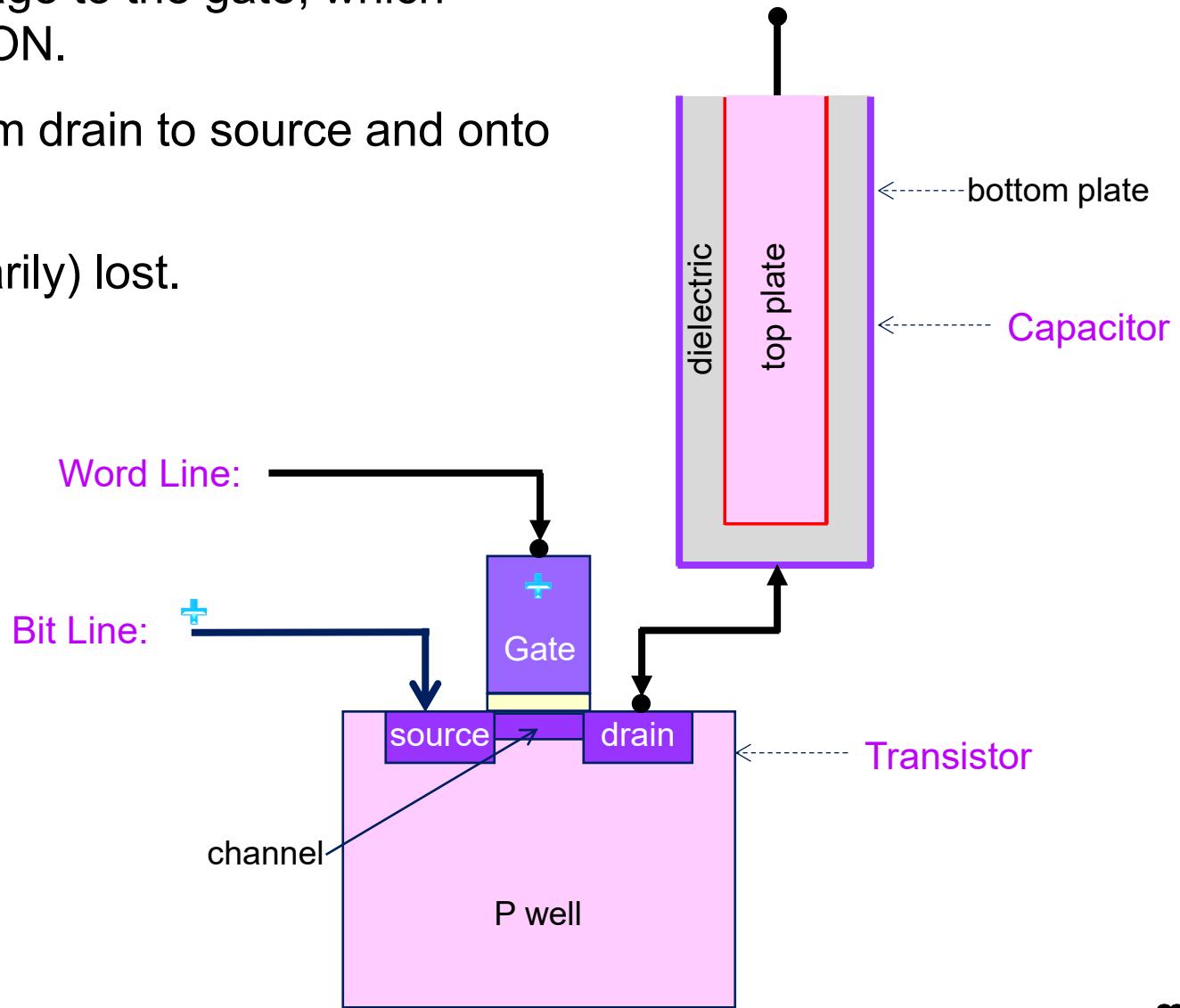
# DRAM Operation – Read

1. Word Line delivers positive voltage to the gate, which creates the channel and turns it ON.
2. Charge on capacitor passes from drain to source and onto the Bit Line.



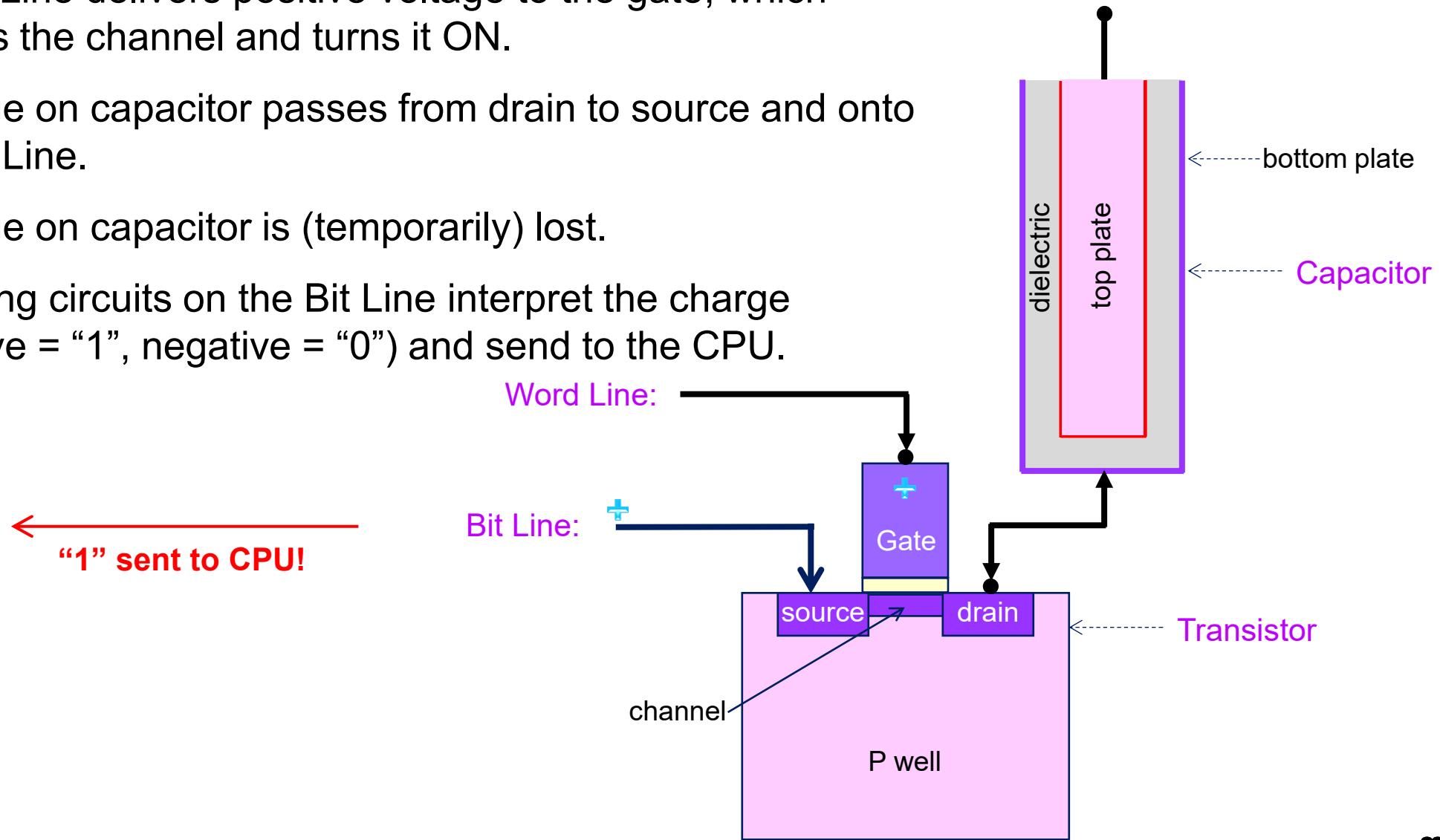
# DRAM Operation – Read

1. Word Line delivers positive voltage to the gate, which creates the channel and turns it ON.
2. Charge on capacitor passes from drain to source and onto the Bit Line.
3. Charge on capacitor is (temporarily) lost.



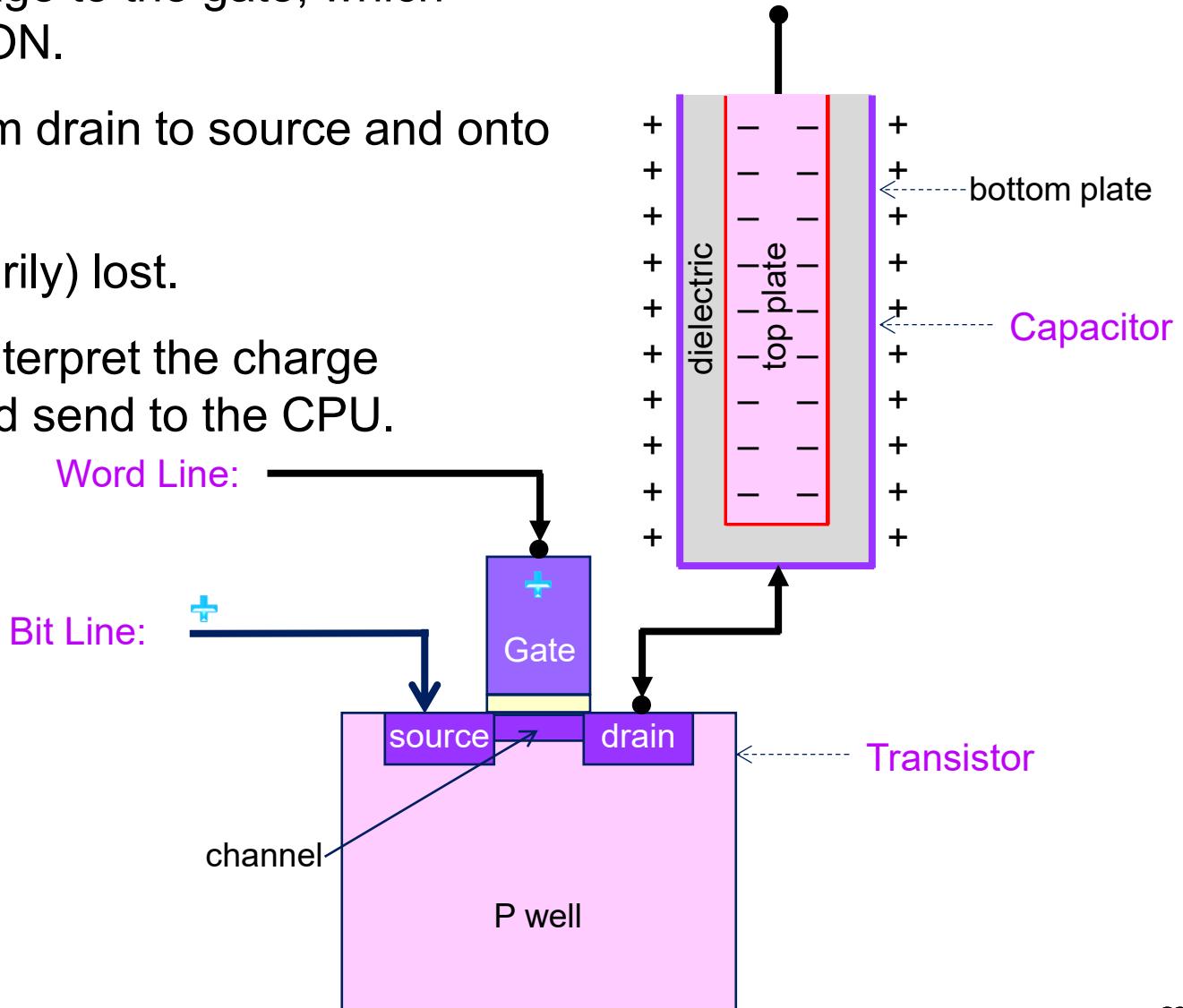
# DRAM Operation – Read

1. Word Line delivers positive voltage to the gate, which creates the channel and turns it ON.
2. Charge on capacitor passes from drain to source and onto the Bit Line.
3. Charge on capacitor is (temporarily) lost.
4. Sensing circuits on the Bit Line interpret the charge (positive = “1”, negative = “0”) and send to the CPU.

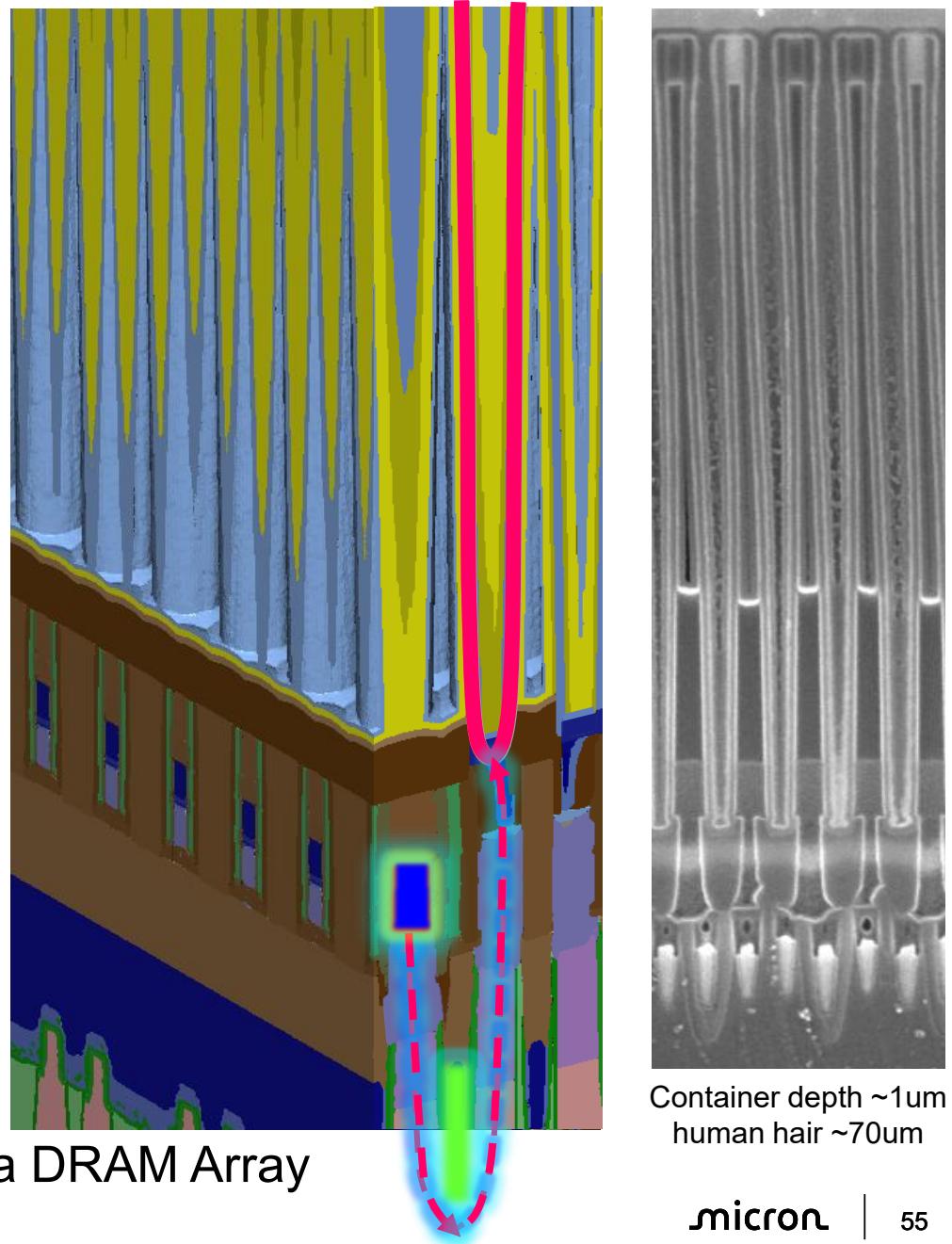
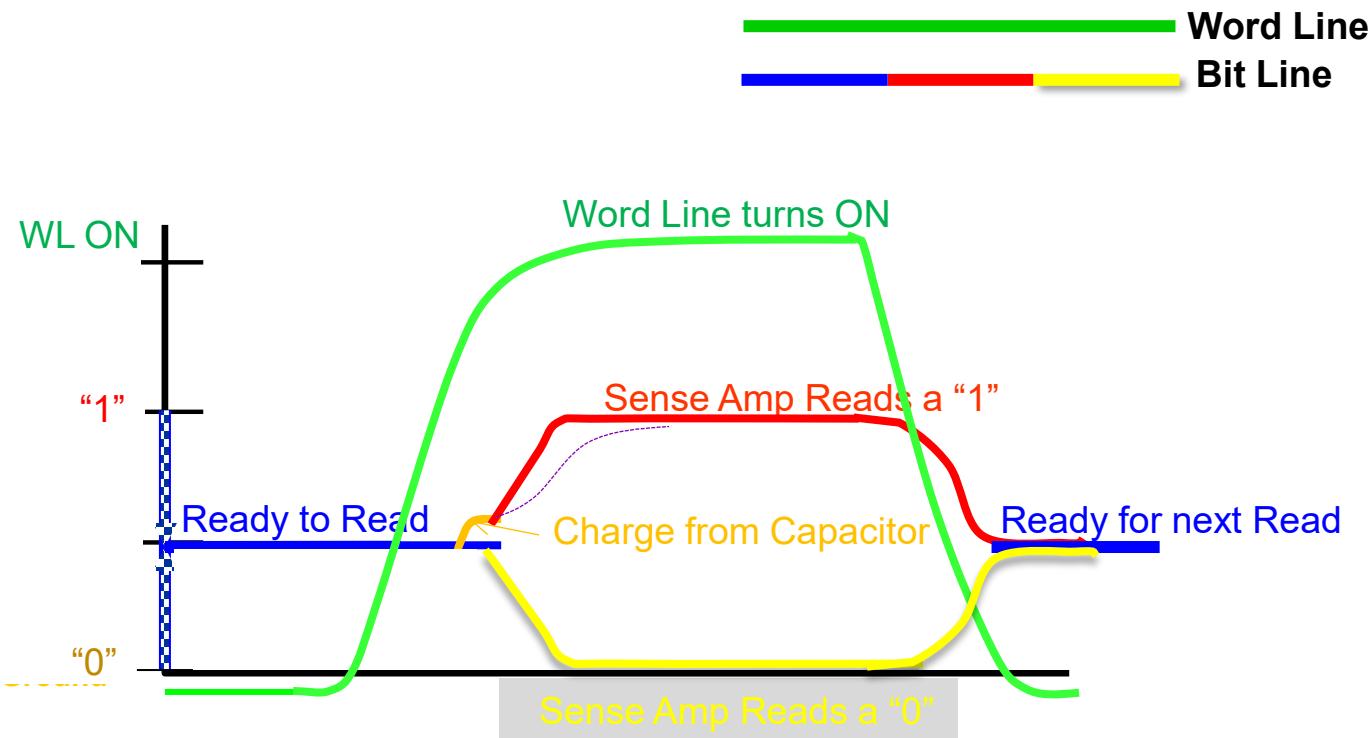


# DRAM Operation – Read

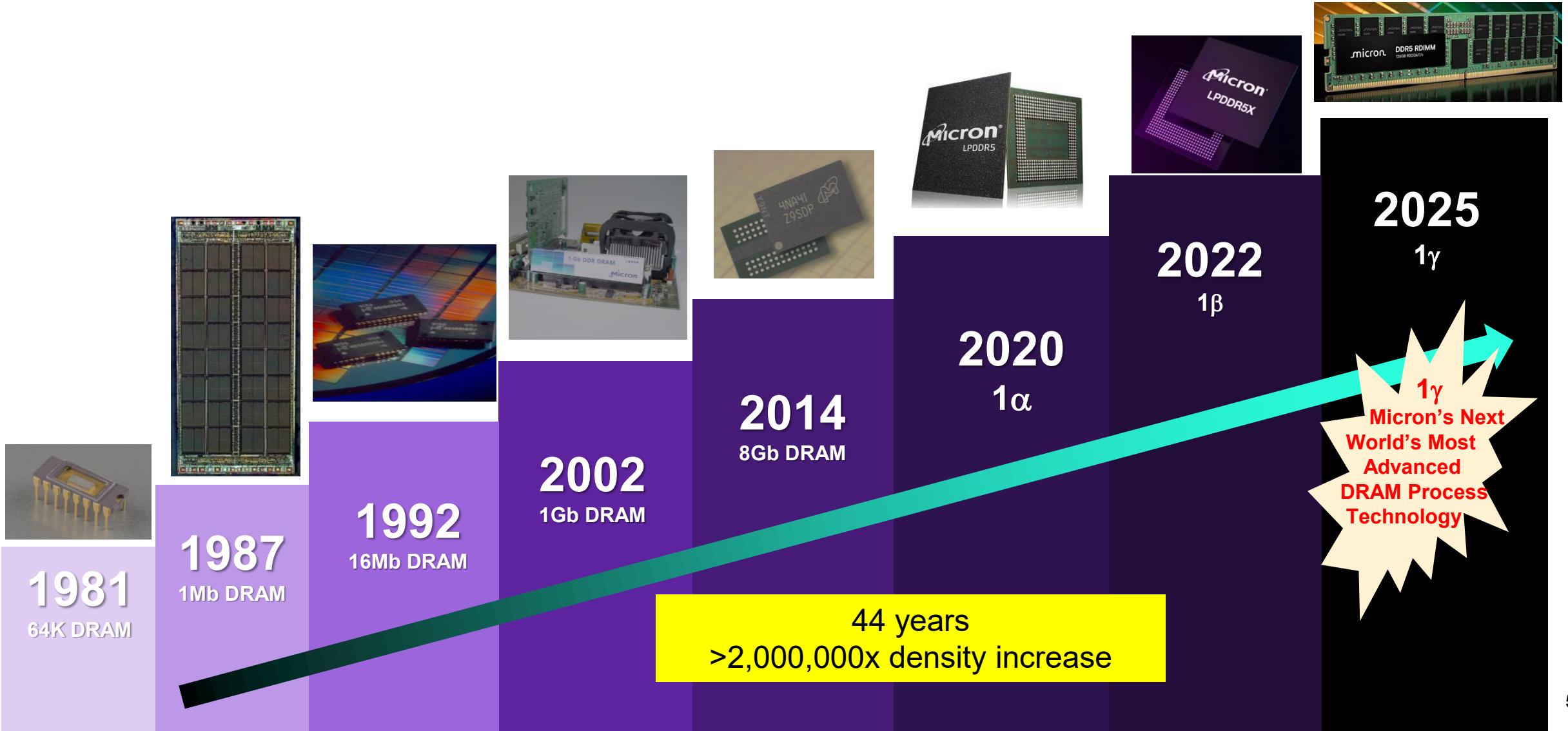
1. Word Line delivers positive voltage to the gate, which creates the channel and turns it ON.
2. Charge on capacitor passes from drain to source and onto the Bit Line.
3. Charge on capacitor is (temporarily) lost.
4. Sensing circuits on the bit line interpret the charge (positive = “1”, negative = “0”) and send to the CPU.
5. Lost charge on the capacitor must be “refreshed” (same as write operation).



# Read (& Refresh)

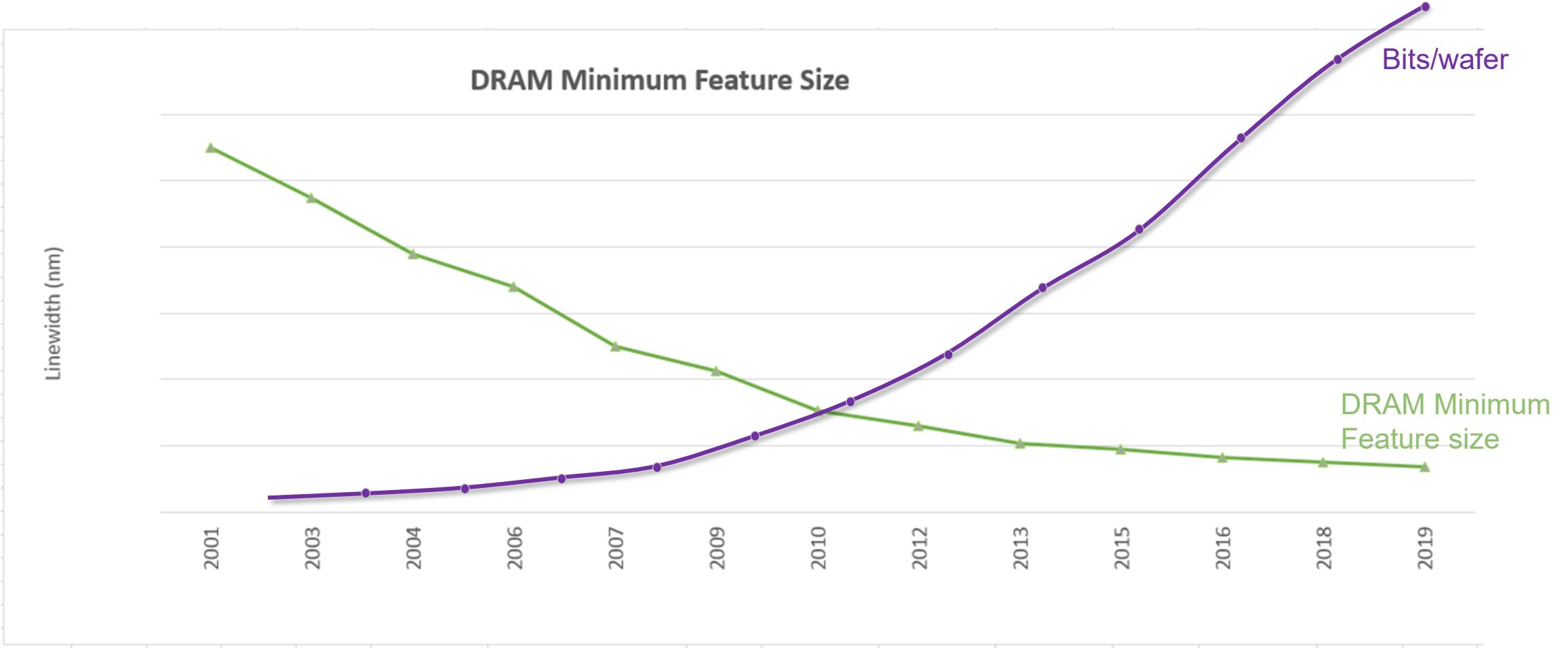


# Evolution of DRAM



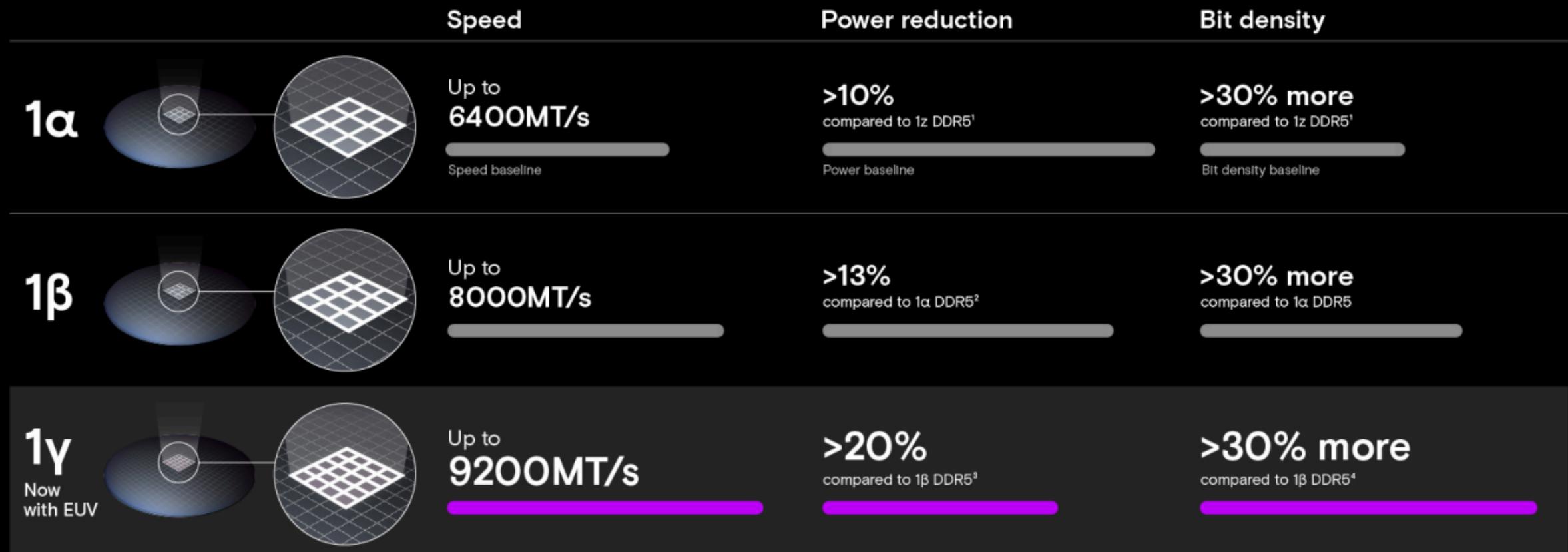
# DRAM Scaling Trend

With each generation, by reducing the feature sizes of our memory cells on each die we can increase density, achieve higher bits per wafer, and lower cost per bit.



# Gen-over-gen DRAM technology leadership

Micron continues to lead the industry, advancing from 1 $\alpha$  (1-alpha) and 1 $\beta$  (1-beta) to 1 $\gamma$  (1-gamma) technology



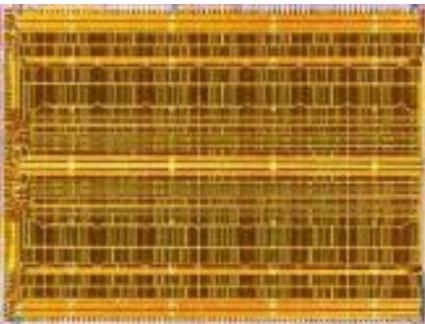
(1) 1z is the previous version of DRAM technology before 1 $\alpha$ . (2) Based on calculations comparing 24Gb density DDR5. (3) Based on calculations comparing 16Gb density DDR5.

(4) Calculated based on overall bits per wafer comparing 1 $\beta$  and 1 $\gamma$  process.

# DRAM technology leadership

Innovation and  
execution for sustained  
leadership

## DRAM



**1 $\beta$**

First to market with  
next-generation  
process node

**1 $\gamma$**

First to ship 6<sup>th</sup>  
generation process  
node-based  
memory

**1 $\gamma$**

- Leverages EUV lithography and next-generation HKMG\* CMOS technology. Results in greater than 30% more bits-per-wafer output over 1 $\beta$  node
- 1 $\gamma$ -based DDR5 for data center and client, delivering up to a 15% speed increase and over 20% power reduction\*\*
- The world's first 1 $\gamma$ -based LPDDR5X for mobile, offering a 10.7 Gbps speed grade and up to 20% power savings\*\*
- Deployed on computing platforms, from the cloud to edge AI devices

\*High-K metal gate

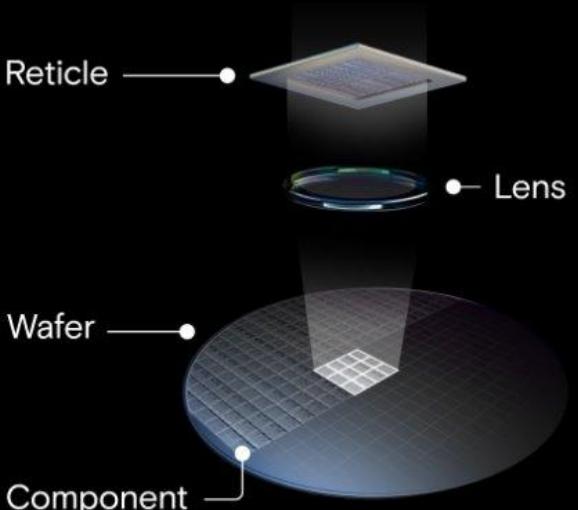
\*\* Compared to the previous generation

# 1γ: The world's most advanced DRAM

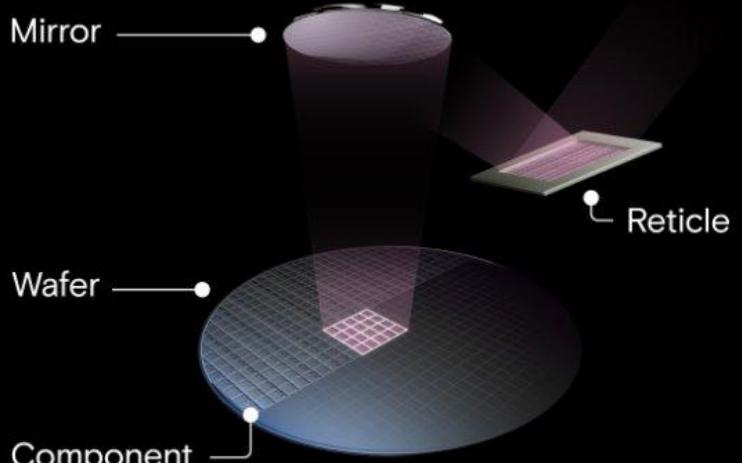
First in the industry to ship samples of 1γ (1-gamma), sixth-generation DRAM node-based DDR5 and LPDDR5X memory

- Builds on Micron's previous 1α (1-alpha) and 1β (1-beta) DRAM node leadership
- Leverages EUV lithography and next-generation HKMG and CMOS technology
- Deployed on computing platforms from the cloud to edge AI devices like AI PCs, smartphones and automobiles
- Features advanced power, performance and bit density

## Previous process node



## 1γ (1-gamma) process node



\*High-K metal gate

\*\* Compared to the previous generation

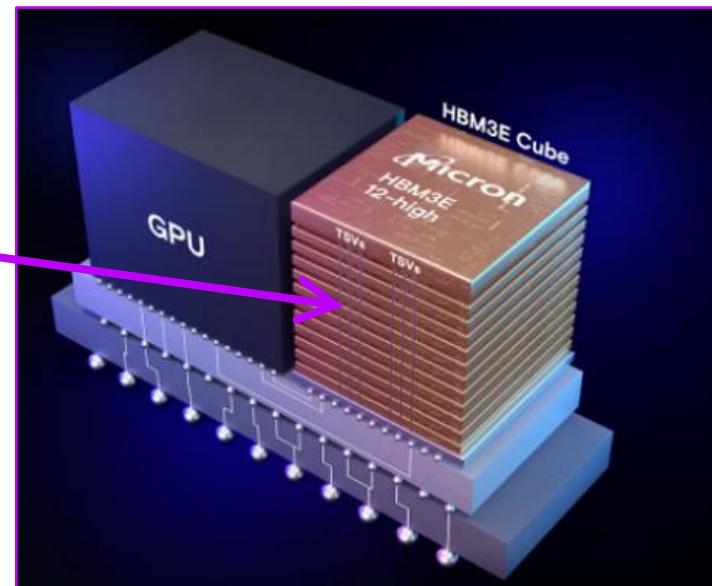
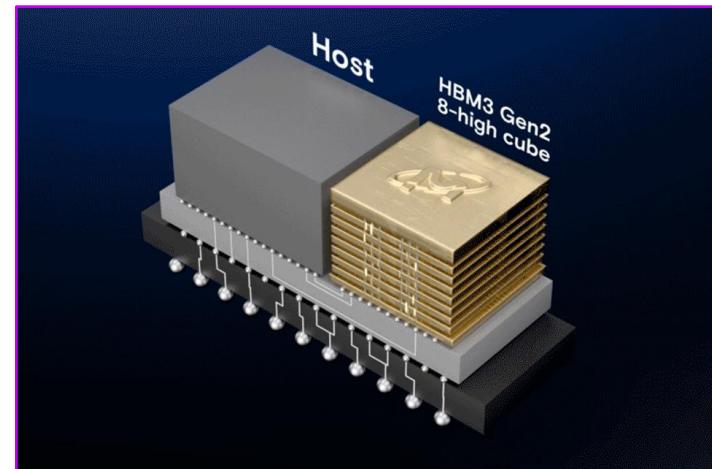
# Micron Delivers Industry's Fastest, Highest-Capacity HBM to Advance Generative AI Innovation

First in industry to launch 8-high 24GB HBM3 Gen2 with bandwidth over 1.2TB/s and superior power efficiency enabled by advanced 1β process node

BOISE, Idaho, July 26, 2023 (GLOBE NEWSWIRE) -- Micron Technology, Inc. (Nasdaq: MU) today announced it has begun sampling the industry's first 8-high 24GB HBM3 Gen2 memory with bandwidth greater than 1.2TB/s and pin speed over 9.2Gb/s, which is up to a 50% improvement over currently shipping HBM3 solutions. With a 2.5 times performance per watt improvement over previous generations, Micron's HBM3 Gen2 offering sets new records for the critical artificial intelligence (AI) data center metrics of performance, capacity and power efficiency. These Micron improvements reduce training times of large language models like GPT-4 and beyond, deliver efficient infrastructure use for AI inference and provide superior total cost of ownership (TCO).

The foundation of Micron's high-bandwidth memory (HBM) solution is Micron's industry-leading 1β (1-beta) DRAM process node, which allows a 24Gb DRAM die to be assembled into an 8-high cube within an industry-standard package dimension. Moreover, Micron's 12-high stack with 36GB capacity will begin sampling in the first quarter of calendar 2024. Micron provides 50% more capacity for a given stack height compared to existing competitive solutions. Micron's HBM3 Gen2 performance-to-power ratio and pin speed improvements are critical for managing the extreme power demands of today's AI data centers. The improved power efficiency is possible because of Micron advancements such as doubling of the through-silicon vias (TSVs) over competitive HBM3 offerings, thermal impedance reduction through a five-time increase in metal density, and an energy-efficient data path design.

This 24GB HBM3 Gen2 contains 8 of the leading-edge 1Beta 24Gbit DRAM die! Those HBM3-specific die are interconnected vertically by Thru-Silicon Vias (TSVs) that are formed in the wafer during in-fab processing

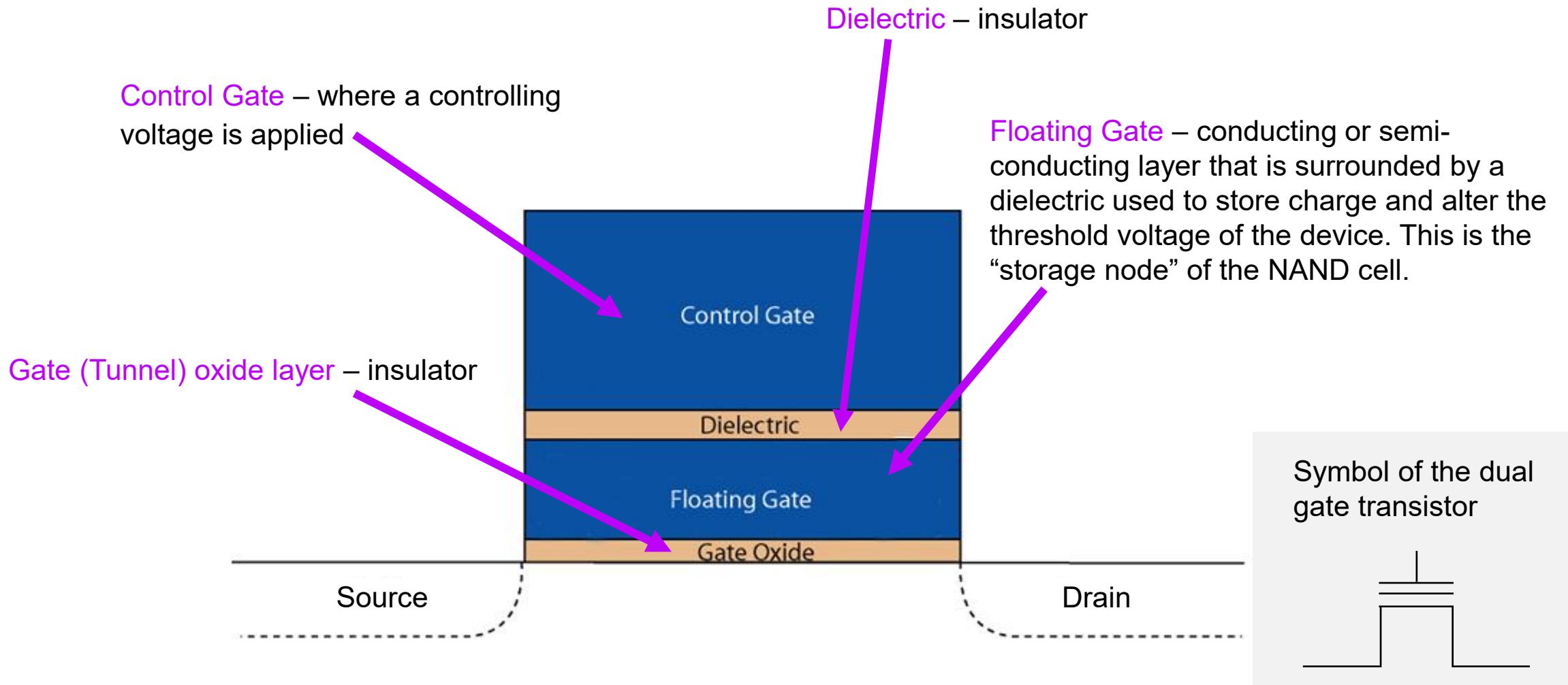


# 5. Introduction to Flash

micron

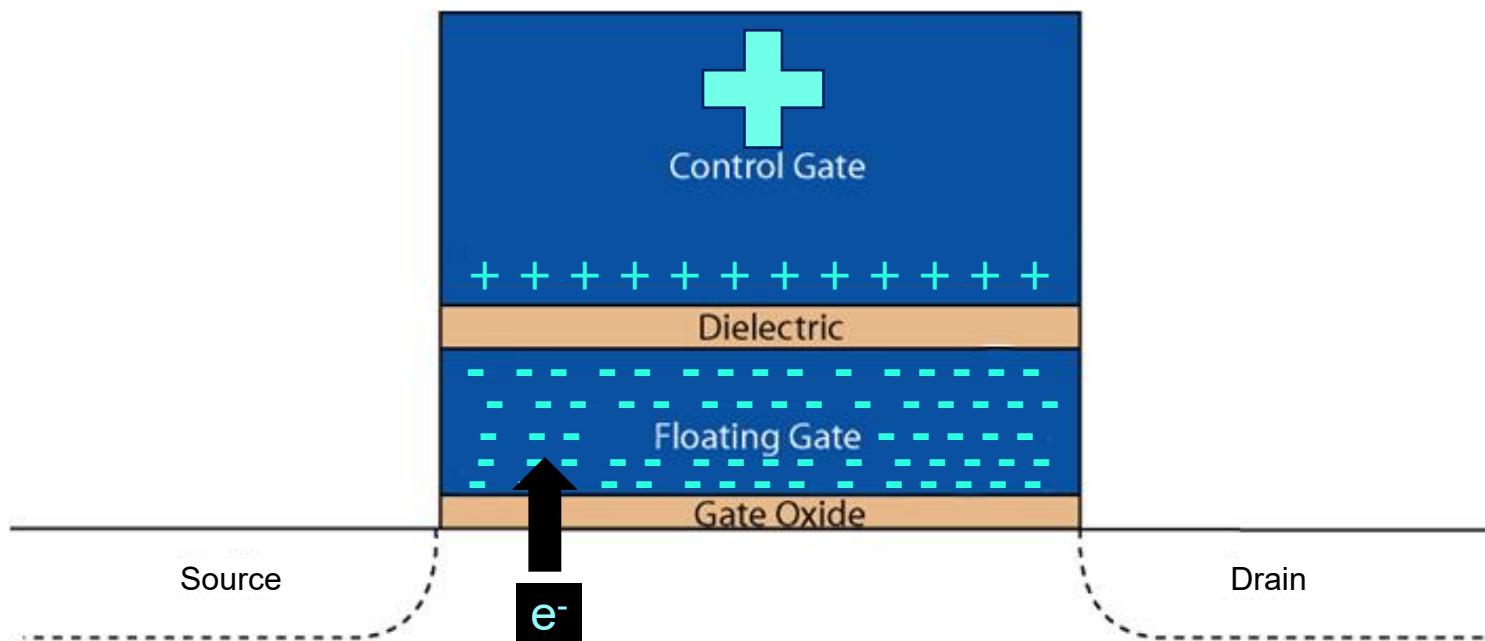


# Structure of a Basic Flash Cell



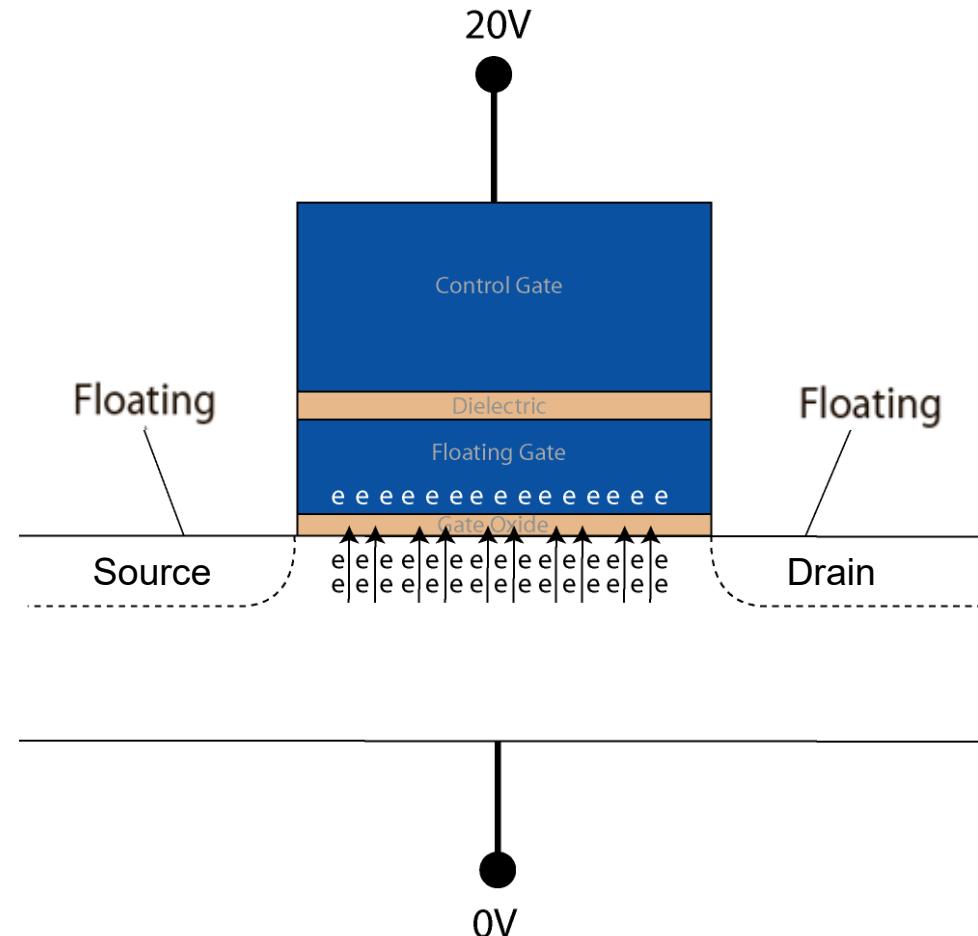
# NAND Function

- High voltage on the Control Gate causes electrons to tunnel through the gate oxide and get trapped within the Floating Gate



# Programming / Writing a NAND Cell

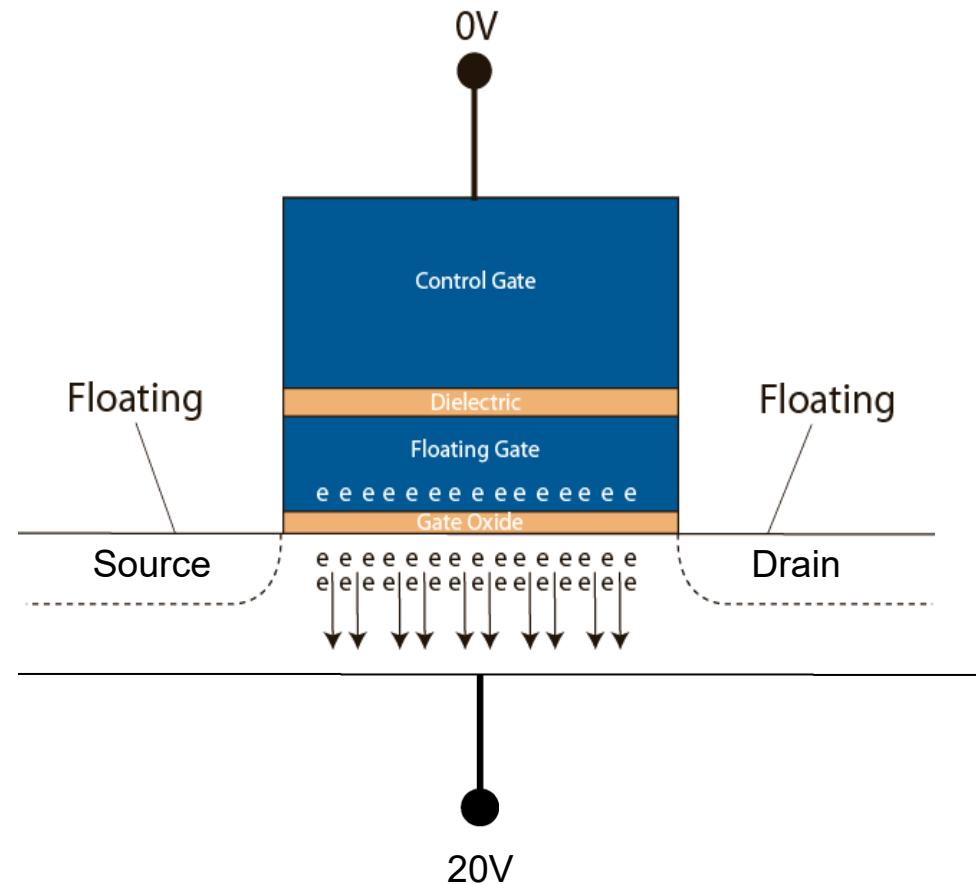
- Ground the substrate
- Apply ~+20V to the control gate
- Electrons in the substrate tunnel through the gate oxide and relocate in the floating gate
- When voltage is released, electrons are trapped in the floating gate making NAND Flash a non-volatile memory
- For some of our parts, data is guaranteed for 10 years



Note: cell design and voltage values have evolved from technology node to technology node. Design and values shown here for educational purpose.

# Erasing a NAND Cell

- Ground the control gate
- Apply  $\sim 20V$  to the substrate
- Electrons trapped within the floating gate tunnel back through the gate oxide into the substrate

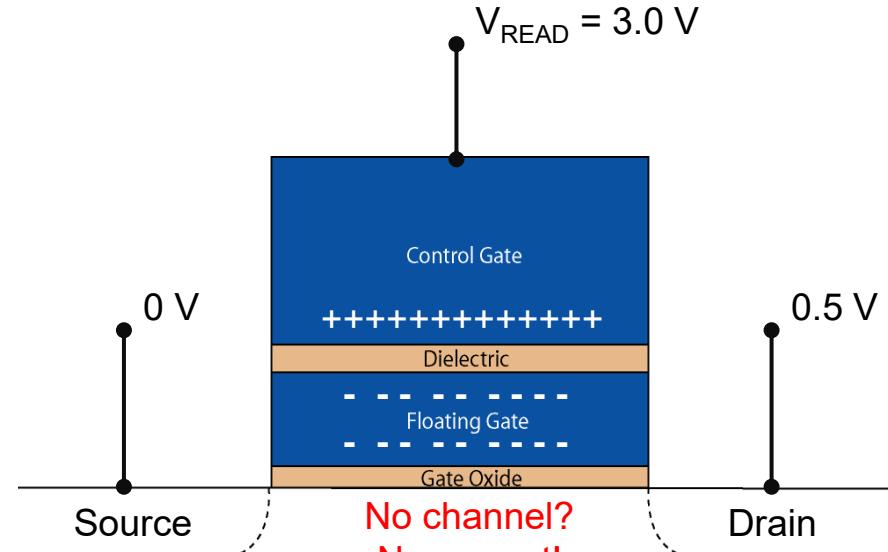


Note: cell design and voltage values have evolved from technology node to technology node. Design and values shown here for educational purpose.

# Reading a NAND Cell

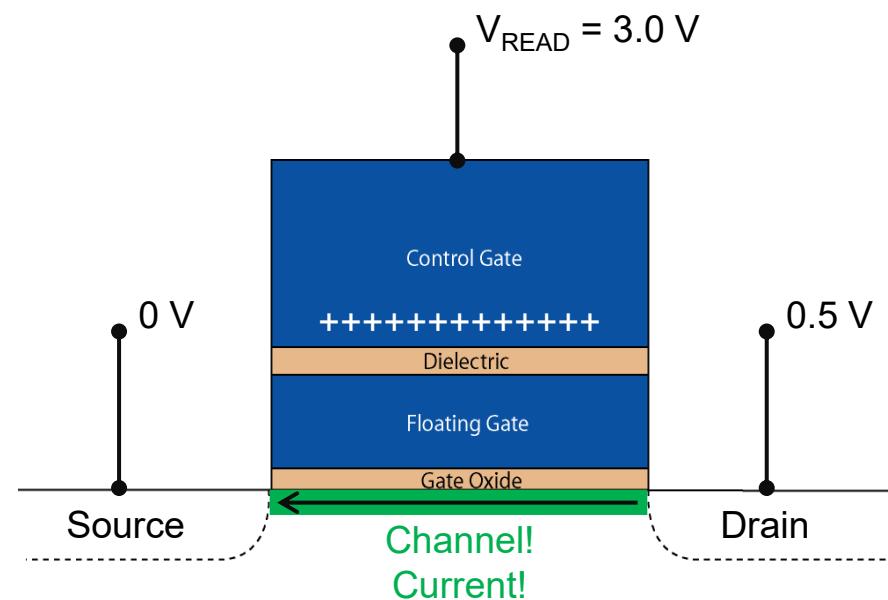
## Reading a Programmed Cell:

- 0.5V on drain, 0V on source create a voltage drop
- $V_{READ} = 3.0V$  on the control gate attempts to create a channel to turn transistor ON
- Electrons trapped in the floating gate prevent the channel from forming so transistor remains OFF ( $V_{READ}$  not sufficient to form channel)
- No current flows between source and drain so a logic "0" is read



## Reading an Erased Cell:

- 0.5V on drain, 0V on source create a voltage drop
- $V_{READ} = 3.0V$  on the gate attempts to create a channel to turn transistor ON
- With no electrons trapped in the floating gate, the channel is formed, and transistor turns ON
- Current flows between source and drain so a logic "1" is read



Note: cell design and voltage values have evolved from technology node to technology node. Design and values shown here for educational purpose.

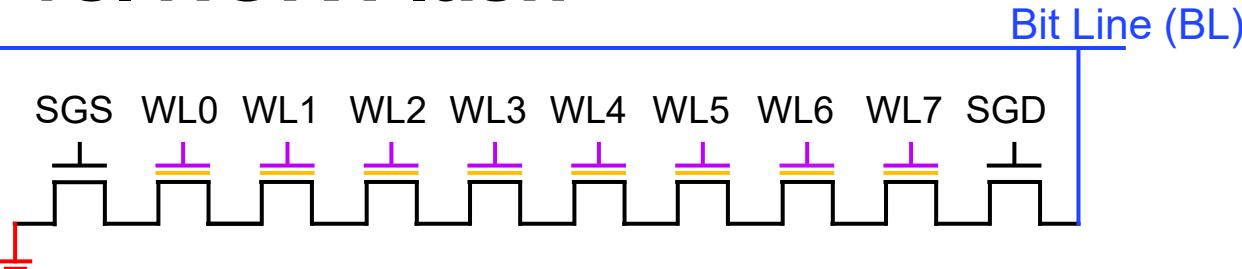
# Flash Function: Logic States

# of e <sup>-</sup> Trapped in Floating Gate	Cell Threshold Voltage	State of the Cell	Current in Channel	Logic State
Low	Low	Not Programmed	Yes	1
High	High	Programmed	No	0

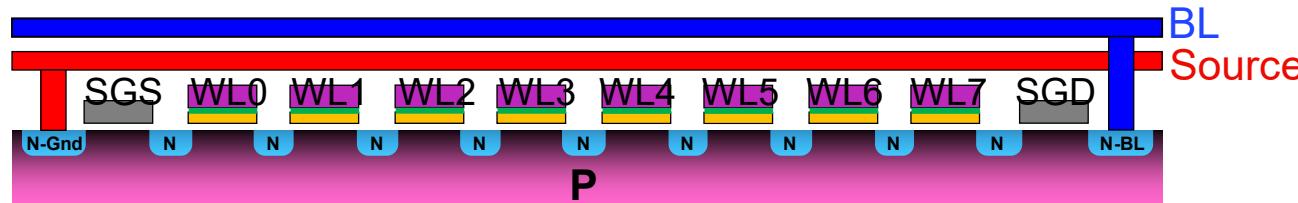
# NAND Flash vs. NOR Flash

## NAND

- Higher Density but Slower

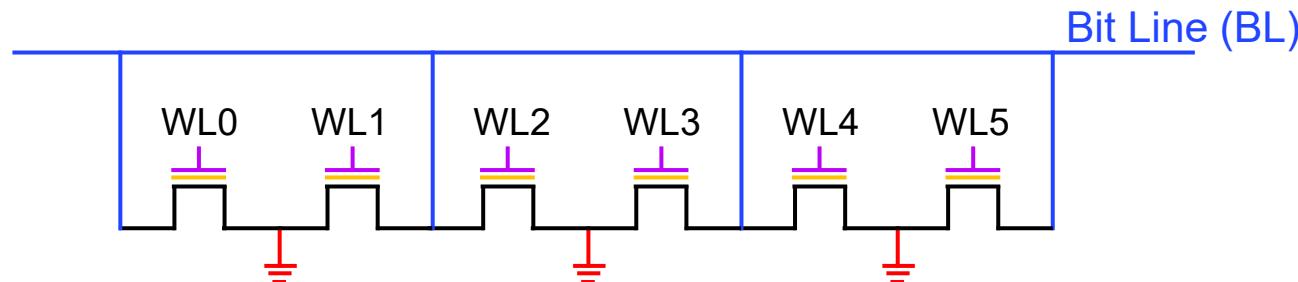


Shared Select Gate Source (SGS) and Bit Line connections for a string of NAND Flash Memory Cells

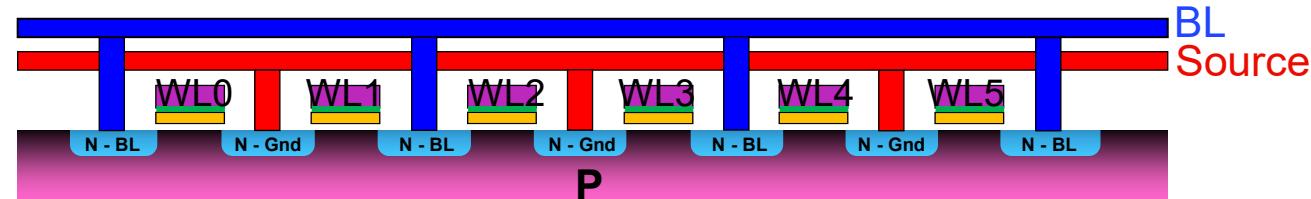


## NOR

- Lower Density but Faster



Individual Bit Line connections for each NOR Flash Memory Cell



### Key

BL: Bit Line

SGS: Select Gate Source Transistor

SGD: Select Gate Drain Transistor

WL: Word Line

# Multi Level Cell (MLC) Technology

- So far we have seen a NAND cell that can store 1 bit per cell where the cell is in one of two possible states:
  - Programmed (Logic 0) or cup is full
  - Erased (Logic 1) or cup is empty
- Continuous innovations in NAND technology now allow us to store more than 1 bit per cell.
- Micron has NAND parts that can store 2, 3, or 4 bits in each cell.
  - SLC: 1 bit per cell (Single level Cell)



Erased  
Logic 1

Programmed  
Logic 0

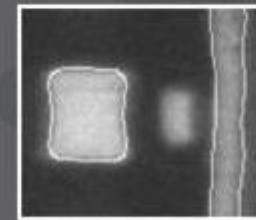
# Multi Level Cell (MLC) Technology

- So far we have seen a NAND cell that can store 1 bit per cell where the cell is in one of two possible states:
  - Programmed (Logic 0) or cup is full
  - Erased (Logic 1) or cup is empty
- Continuous innovations in NAND technology now allow us to store more than 1 bit per cell.
- Micron has NAND parts that can store 2, 3, or 4 bits in each cell.
  - SLC: 1 bit per cell (Single level Cell)
  - MLC: 2 bits per cell (Multi Level Cell)
  - TLC: 3 bits per cell (Triple Level Cell)
  - QLC: 4 bits per cell (Quad Level Cell)
- These new cells are allowed to have “partially full” states
- Consider this MLC example →

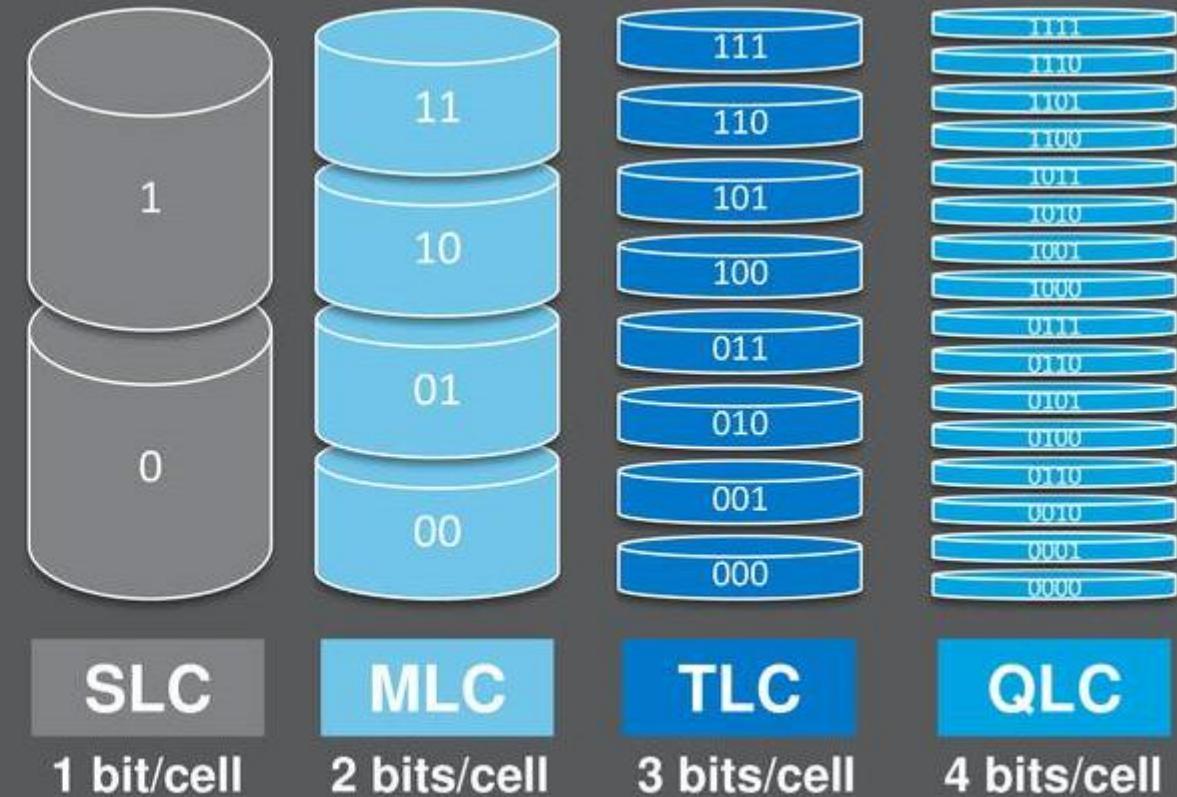


# NAND: Leading the Industry in 4 Bits per Cell (QLC)

- First 64 Layer QLC (4 bits/cell) SSD solution
- Industry's first 1Tb die
- Achieves 33% density increase over TLC



Single NAND Cell



MLC = Multi Level Cell (2 bits per cell)

QLC = Quad Level Cell (4 bits per cell)

SLC = Single Level Cell (1 bit per cell)

SSD = Solid State Drive

Tb = Terabit (one trillion bits or 1,000 gigabits)

TLC = Triple Level Cell (3 bits per cell)

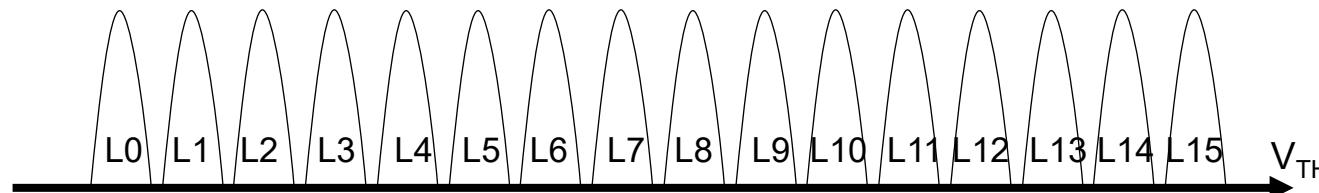
# Charge States in NAND SLC/MLC/TLC/QLC Memory

QLC - Quad Level Cell

**16 Charge States:**

1 Erased + 15 Programmed

**4 Bits** per cell

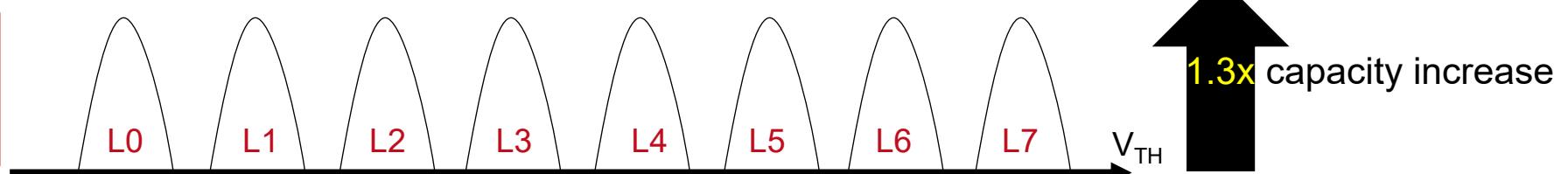


TLC - Triple Level Cell

**8 Charge States:**

1 Erased + 7 Programmed

**3 Bits** per cell

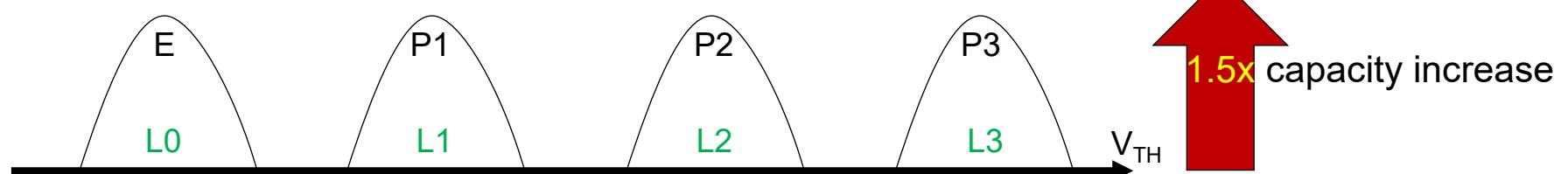


MLC - Multi-Level Cell

**4 Charge States:**

1 Erased + 3 Programmed

**2 Bits** per cell

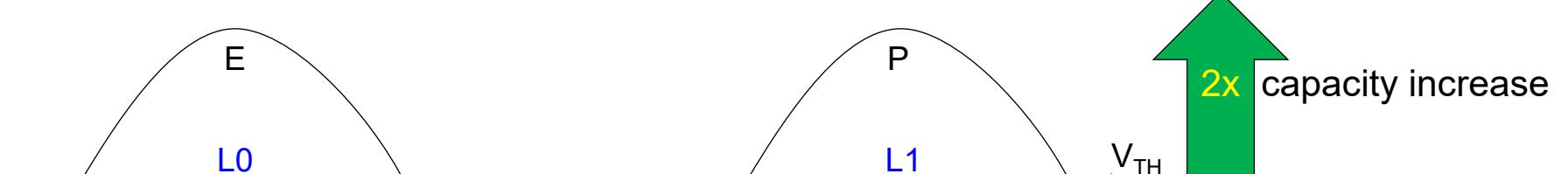


SLC - Single Level Cell

**2 Charge States:**

1 Erased + 1 Programmed

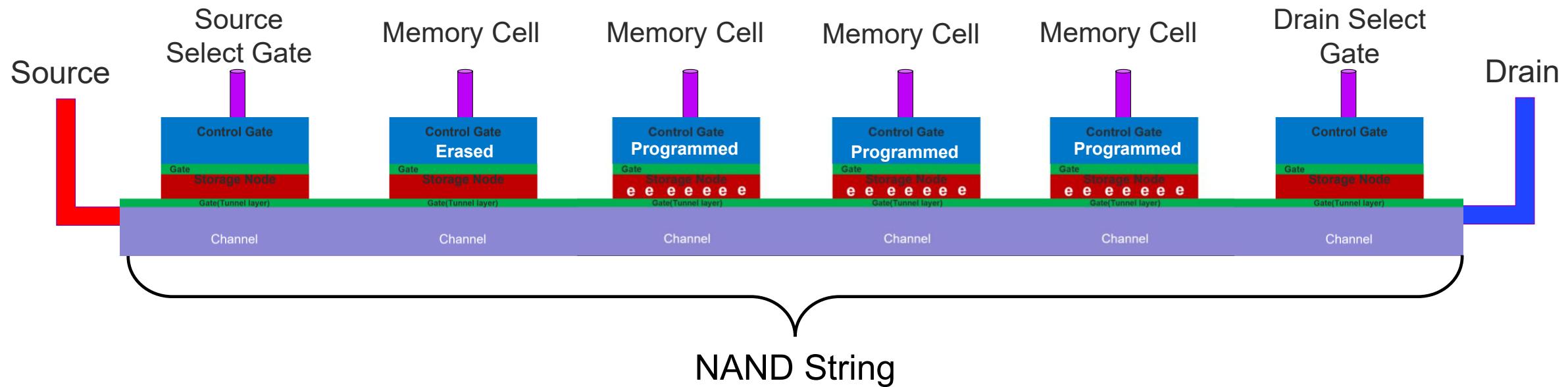
**1 Bit** per cell



Graphic is in arbitrary x/y scale

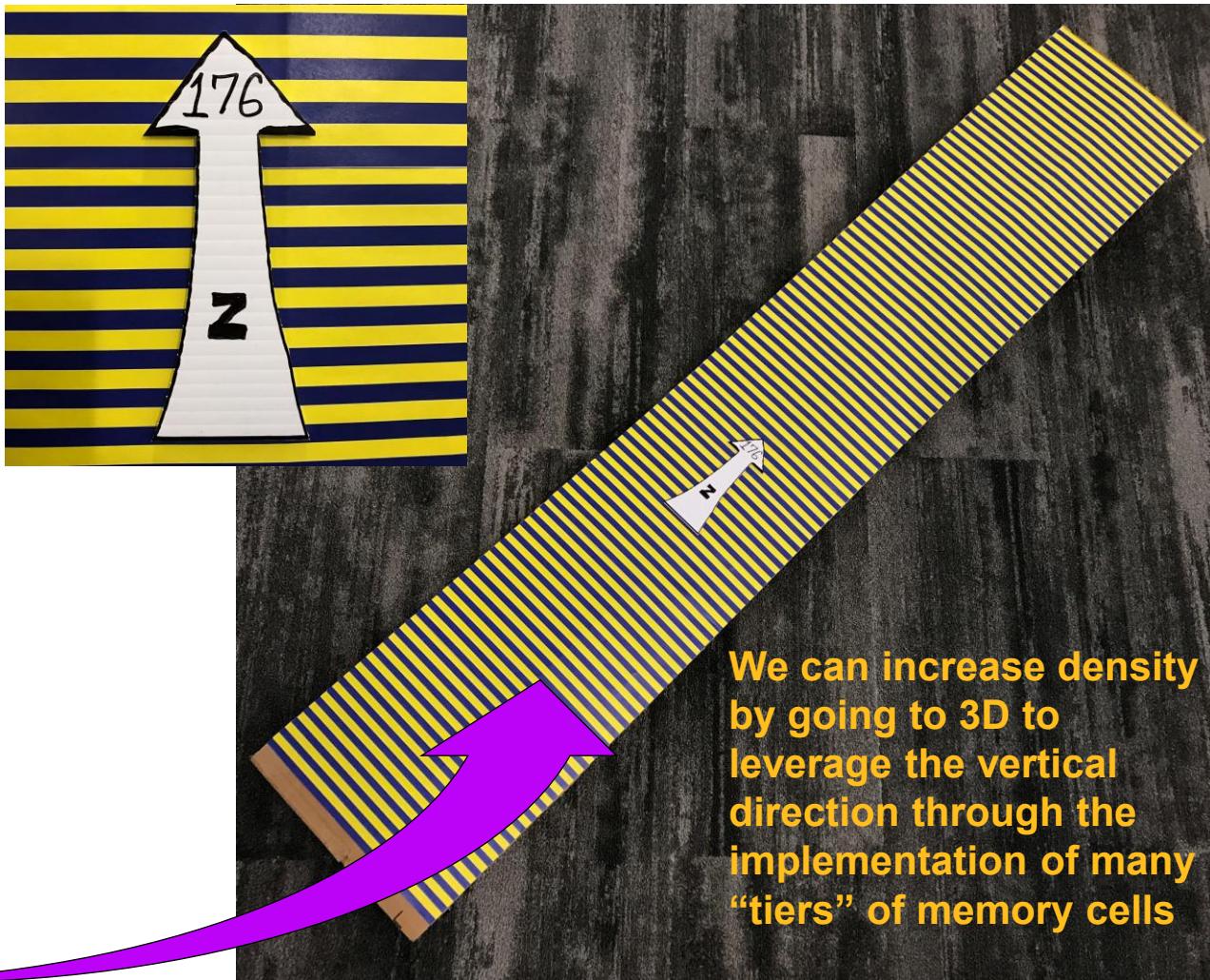
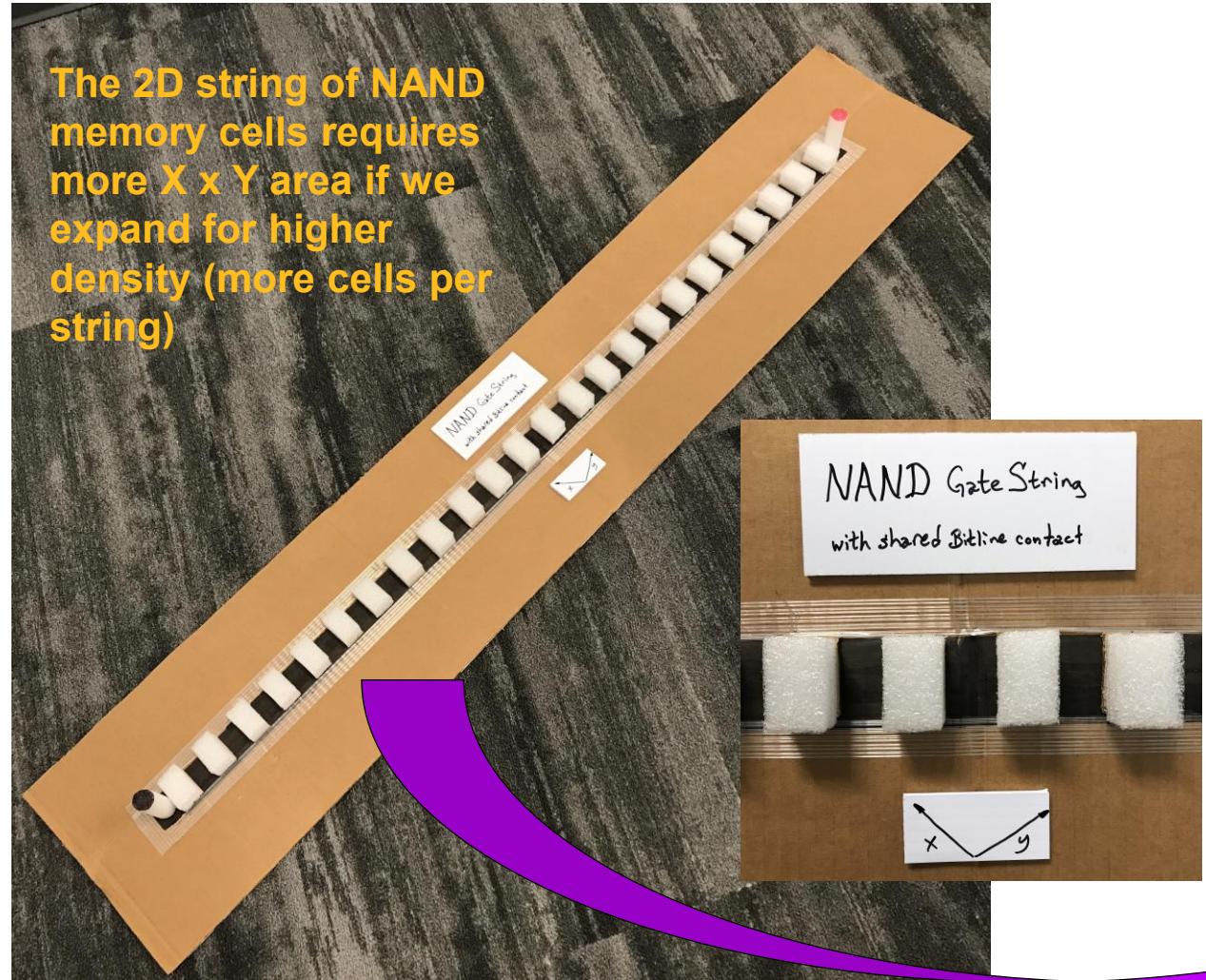
# 2D NAND of Years Past

- Early NAND generations arranged the cells horizontally



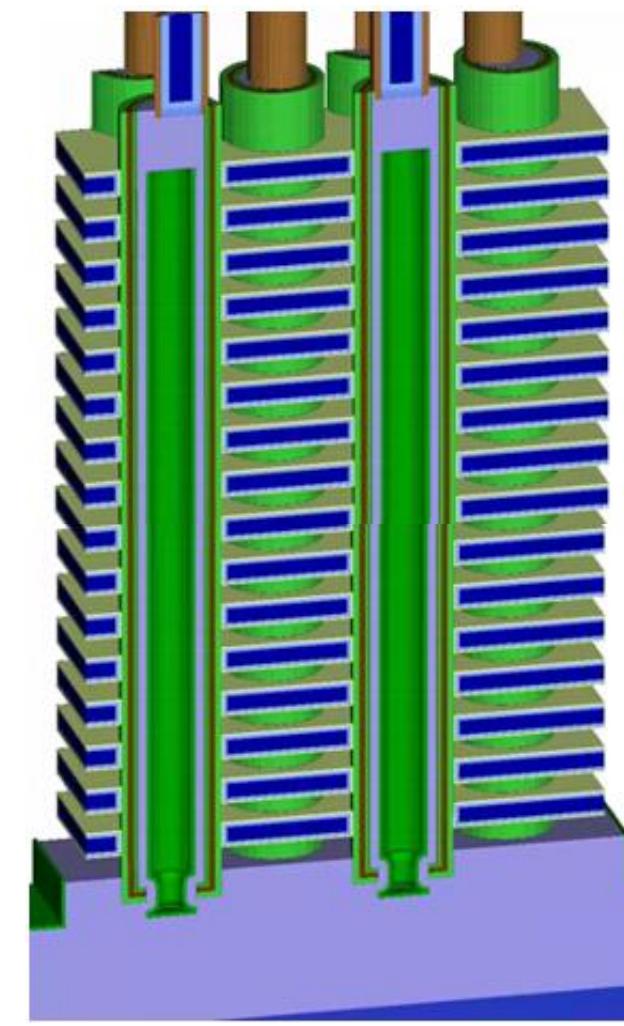
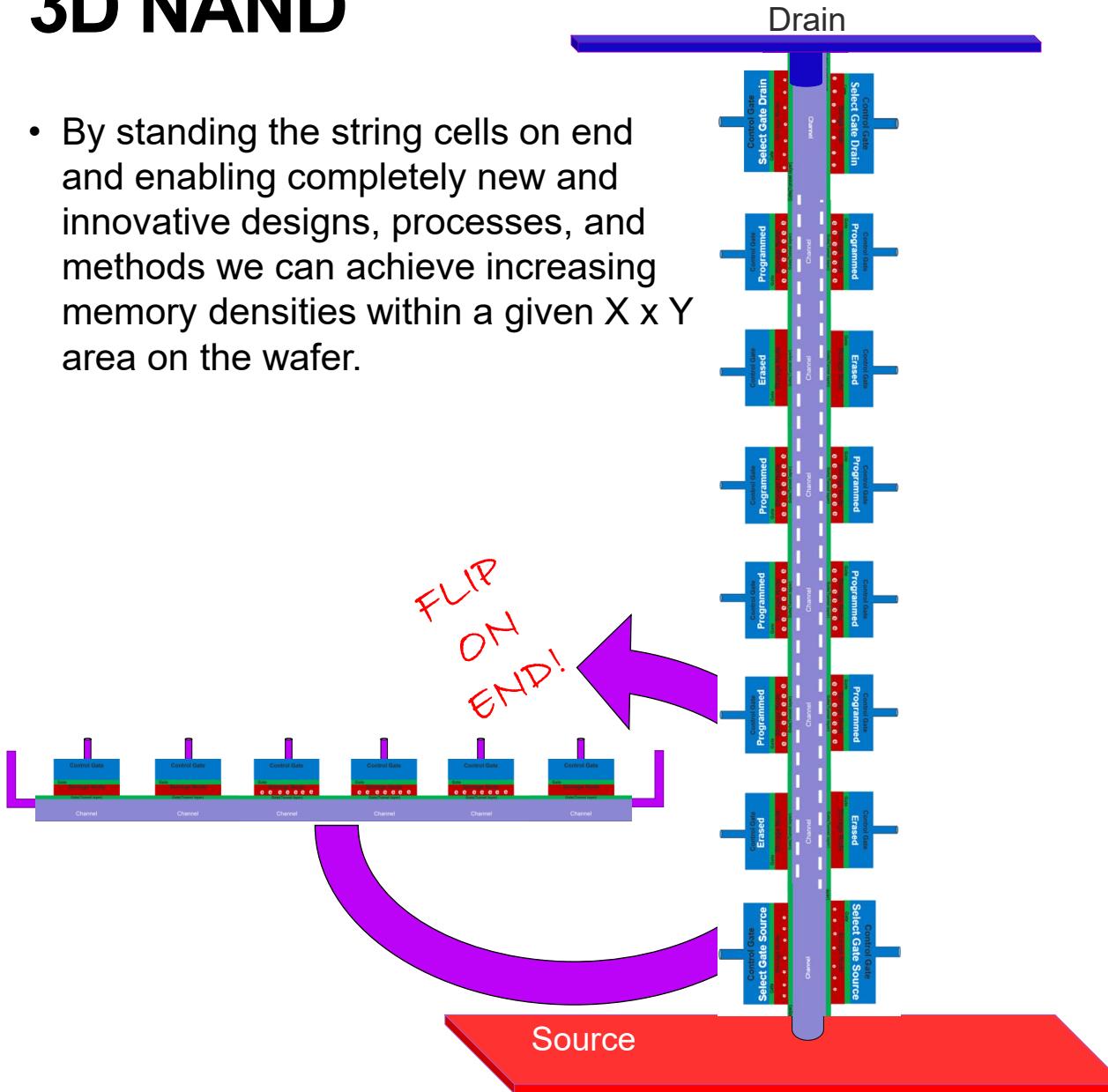
# Into the Z Dimension!

The 2D string of NAND memory cells requires more X x Y area if we expand for higher density (more cells per string)

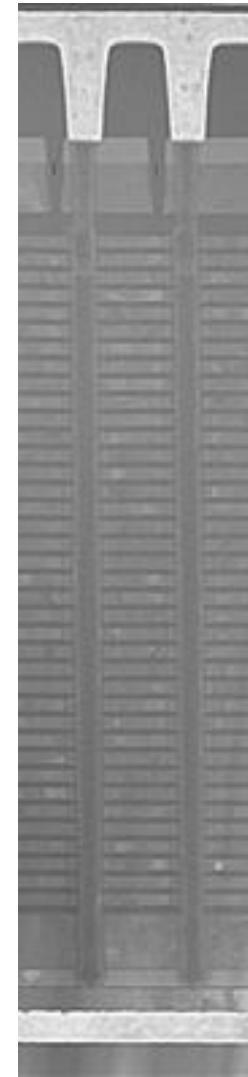


# 3D NAND

- By standing the string cells on end and enabling completely new and innovative designs, processes, and methods we can achieve increasing memory densities within a given X x Y area on the wafer.



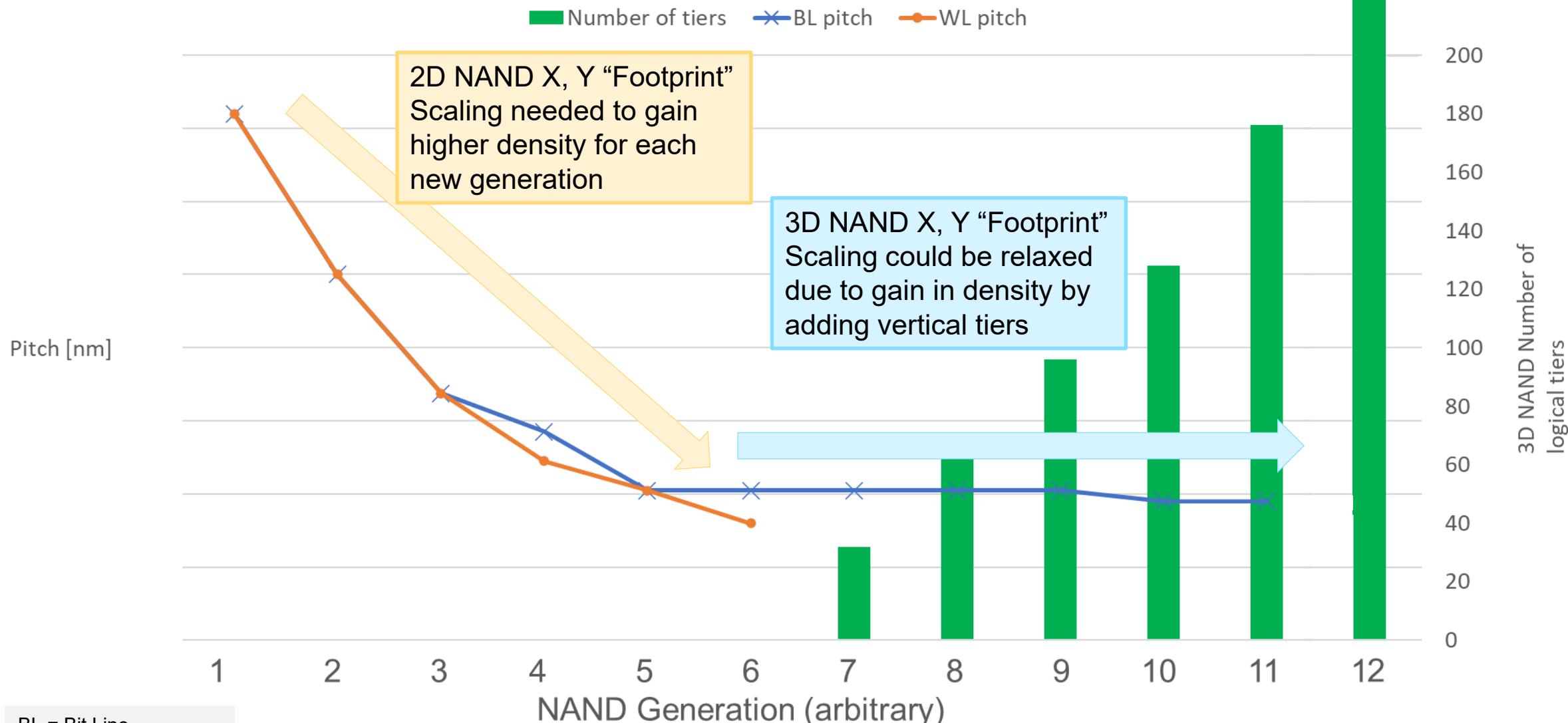
3D Model of a 3D NAND Array



Stacked tiers ~10um  
human hair ~70um

SEM = Scanning Electro Microscope

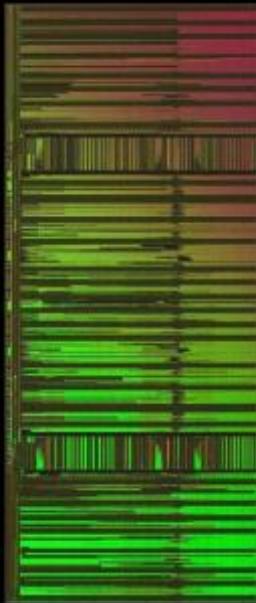
# NAND Scaling Trend



BL = Bit Line  
Gb = Gigabits  
WL = Word Line

# 232-layer: The world's most advanced NAND

Industry leadership sustained – starting ramp in late CY22



1Tb TLC NAND

- Extending CuA and 2 array stack process architecture
- Optimized for leadership in managed NAND and SSD
- Combination of external and optimized internal controllers
- Increased density, power and bandwidth node-over-node



232 Layer, 2 stack,  
CuA\* NAND

\*CuA – CMOS Under Array - another Micron innovation – by locating all support circuitry underneath the memory cell tiers, the die size can be further minimized, thereby gaining even higher bit density (like all supporting utilities and parking garage installed beneath a skyscraper!)

CuA = CMOS Under Array

CY = Calendar Year

SSD = Solid State Drive

Tb = Terabit

TLC = Triple Level Cell (3 bits per cell)

# The world's fastest TLC NAND<sup>1</sup>

Micron is now the first to ship the industry's 9th-generation (G9) 3D NAND in an SSD, and for the third-generation in a row<sup>2</sup>



Advanced building block for cutting-edge storage

Design flexibility with ultra-compact, ultra-dense storage

High performance for devices from your PC to the edge and into the AI-enabled cloud

## Sources

<sup>1</sup> Competitors are identified as SK Hynix, Solidigm, Kioxia, WD and Samsung Semiconductor. The comparisons of I/O speed and design are based on the specifications detailed in the datasheets for NAND shipped in an SSD at the time of Micron's G9 NAND product announcement. The evaluations of read/write bandwidth performance and density are derived from tests conducted in Micron's laboratories, utilizing NAND that was commercially available.

<sup>2</sup> Micron announced shipment of 9th-generation NAND (G9) in the Micron 2650 NVMe, a first for industry 9th-generation NAND. Micron was previously first to announce the industry's 7th- and 8th-generation NAND shipping in an SSD in 2020 and 2022, respectively, and now is first to ship again per footnote 1. See <https://Investors.micron.com/news-releases/news-release-details/micron-ships-worlds-first-176-layer-nand-delivering-breakthrough> and <https://Investors.micron.com/news-releases/news-release-details/micron-ships-worlds-first-232-layer-nand-extends-technology>.



© 2024 Micron Technology, Inc. Micron, the Micron logo, the M logo, Intelligence Accelerated™, and other Micron trademarks are the property of Micron Technology, Inc. All other trademarks are the property of their respective owners.

Peak performance.<sup>1</sup>  
Density dominance.<sup>1</sup>

**3.6 GB/s**  
performance<sup>1</sup>

Up to  
**99%**  
better read<sup>1</sup>

Up to  
**88%**  
better write<sup>1</sup>

**World's densest NAND is now shipping in the Micron 2650 SSD<sup>1</sup>**

Up to  
**73%**  
denser NAND<sup>1</sup>

Up to  
**28%**  
more space efficient<sup>1</sup>

Ideal for the most demanding high performance and data intensive workloads



Data center



Client



Mobile



Automotive and embedded

Learn more at [micron.com/G9](https://micron.com/G9)

# NAND technology leadership

Innovation and  
execution for sustained  
leadership

## NAND



### G8

First to market with  
industry's most advanced  
NAND in volume production

### G9

First to market with  
industry's fastest NAND  
in volume production

### G9

- Best-in-class performance and density compared to competitors
- The industry's highest transfer speed of 3.6 GB/s
- High performance for devices from PC to edge and into AI-enabled cloud
- First to ship G9 TLC NAND in an SSD — Micron 2600 SSD
- Enables award-winning PCIe Gen5 performance — Micron 4600 SSD
- First PCIe Gen6 SSD for high-performance AI workloads — Micron 9650 SSD
- Lowest latency PCIe Gen5 mainstream performance SSD — Micron 7600 SSD
- Industry-leading storage density — Micron 6600 ION SSD

# Summary – DRAM vs. NAND

- DRAM (Dynamic Random Access Memory) and NAND are two common memory or storage options with different designs and working principles.
- DRAM is a volatile memory, meaning data stored in it is lost when there is a power failure or when you shut down your system. It is a type of semiconductor memory used to temporarily store the program code or data required by the computer's processor. DRAM is typically used in personal computers, servers, workstations, processors, graphics cards, video gaming consoles, and other gaming devices.
- NAND, is a non-volatile storage technology that does not need any power to hold the data stored in it. It is a common type of flash memory that is usually used in different types of storage devices such as Solid State Drives (SSDs), Secure Digital (SD) cards, and Universal Serial Bus (USB) flash drives.
- In terms of memory cell construction, a DRAM is made up of a transistor and a capacitor, while NAND uses a dual-gate transistor.
- DRAM has fast read/write speed and high performance, making it widely used in computer memory. NAND, however, has a larger storage capacity and better data persistence, making it widely used in storage media.

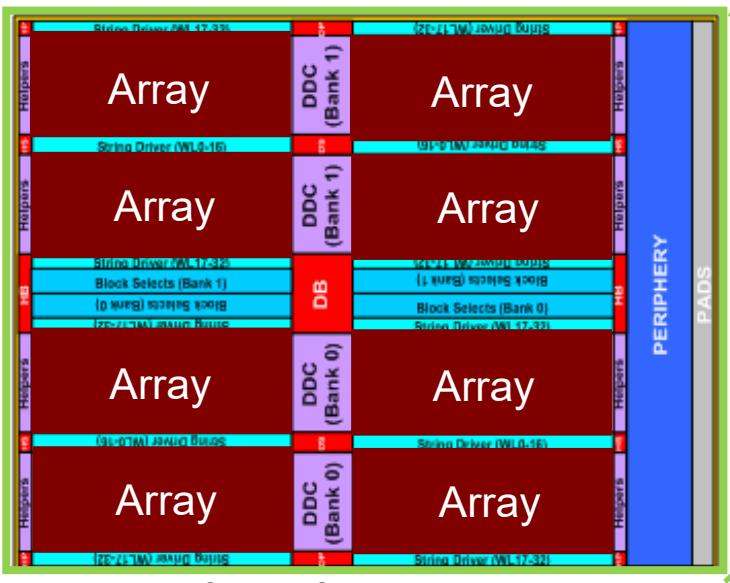
# 6. Key Terminology/ Glossary

micron

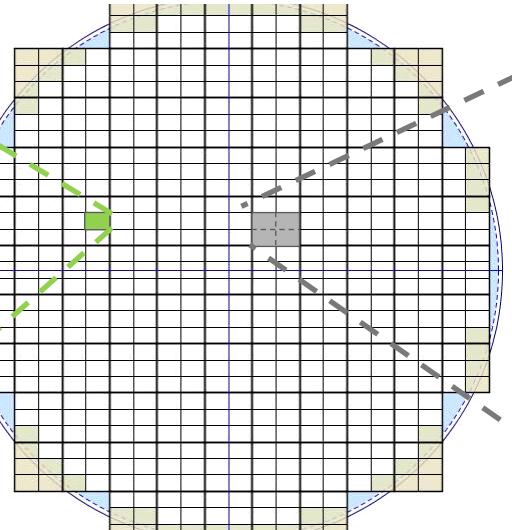


# Terminology: wafer, die, array, periphery, scribe

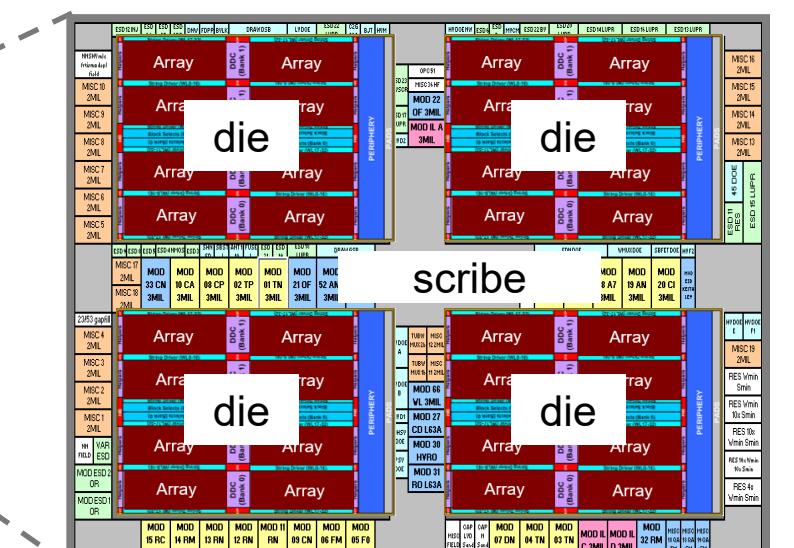
- Memory is fabricated on a 300 mm diameter silicon **wafer**. We try to maximize our die per wafer.
- A **die** is the memory chip which has a memory **array** and a **periphery**
  - The **array** (DRAM cells or NAND cells) stores information
  - The **periphery** has many circuits that operate with the array (pumps, regulators, IO (Input/Output), ESD, etc.)
- The **scribe** or **frame** is the region between die. It contains hundreds of alignment and metrology structures and electrical test circuits to enable in-line measurements and electrical testing. Die gets cut apart through the die singulation process for packaging.



Example of a die floorplan. Array is the dark red. Periphery shown in other colors.



Wafer



Example of scribe circuits around die  
(not to scale)

# Glossary

Term or acronym	Definition/description
Array	The die has a memory array and a periphery. The memory array is where the data (1s and 0s) is stored.
Capacitor	An electronic device used to store electric charge. A capacitor consists of two conductive “plates” and an insulating layer known as a “dielectric” that electrically separates the two plates.
Conductor	A material that allows electrical current to flow easily. Examples of conductors used in integrated circuits are metals like aluminum, tungsten and copper.
CuA	CMOS Under Array - a Micron innovation. An architecture that consists on locating all support circuitry (periphery) underneath the memory cell array. CuA allows the die size to be further minimized, thereby gaining higher bit density (like all supporting utilities and parking garage installed beneath a skyscraper!)
Die	A memory die is a semiconductor memory chip in its state before it is packaged. At Micron, memory die are fabricated on a silicon substrate. Hundreds of memory die are built on the wafer, and after fabrication is completed, each memory die gets cut apart through the die singulation process. Individual memory die are very delicate, so they next go through the Packaging process.
Diode	An electronic device that allows current to flow in one direction only. Formed by connecting a P-type material with an N-type material. Diodes can be used to electrically isolate adjacent devices from each other
DRAM	Dynamic Random Access Memory. This is one of the types of semiconductor memory that Micron designs and fabricates. In DRAM memory data is stored as electrical charge on a capacitor. Charge is quickly lost though, so data must be constantly “refreshed”. DRAM is one of the fastest memories and provides both fast read and write operations. DRAM can be found in applications like computers, servers, laptops, tablets, cell phones, AI applications, etc.
Frame	The frame or scribe is the region of the wafer that separates one die from another die. The frame contains hundreds of alignment and metrology structures to enable in-line measurements, and electrical test circuits to enable electrical testing. These structures are sacrificial as they are cut apart through the die singulation process as each die needs to be cut apart before packaging.
Insulator	A material that is very resistive to electrical current flow. Examples of insulators used in integrated circuits are silicon dioxide ( $\text{SiO}_2$ ) and silicon nitride ( $\text{Si}_3\text{N}_4$ ).
MLC	Multi Level Cell. it refers to a NAND architecture that allows to program 2 bits per memory cell.

# Glossary

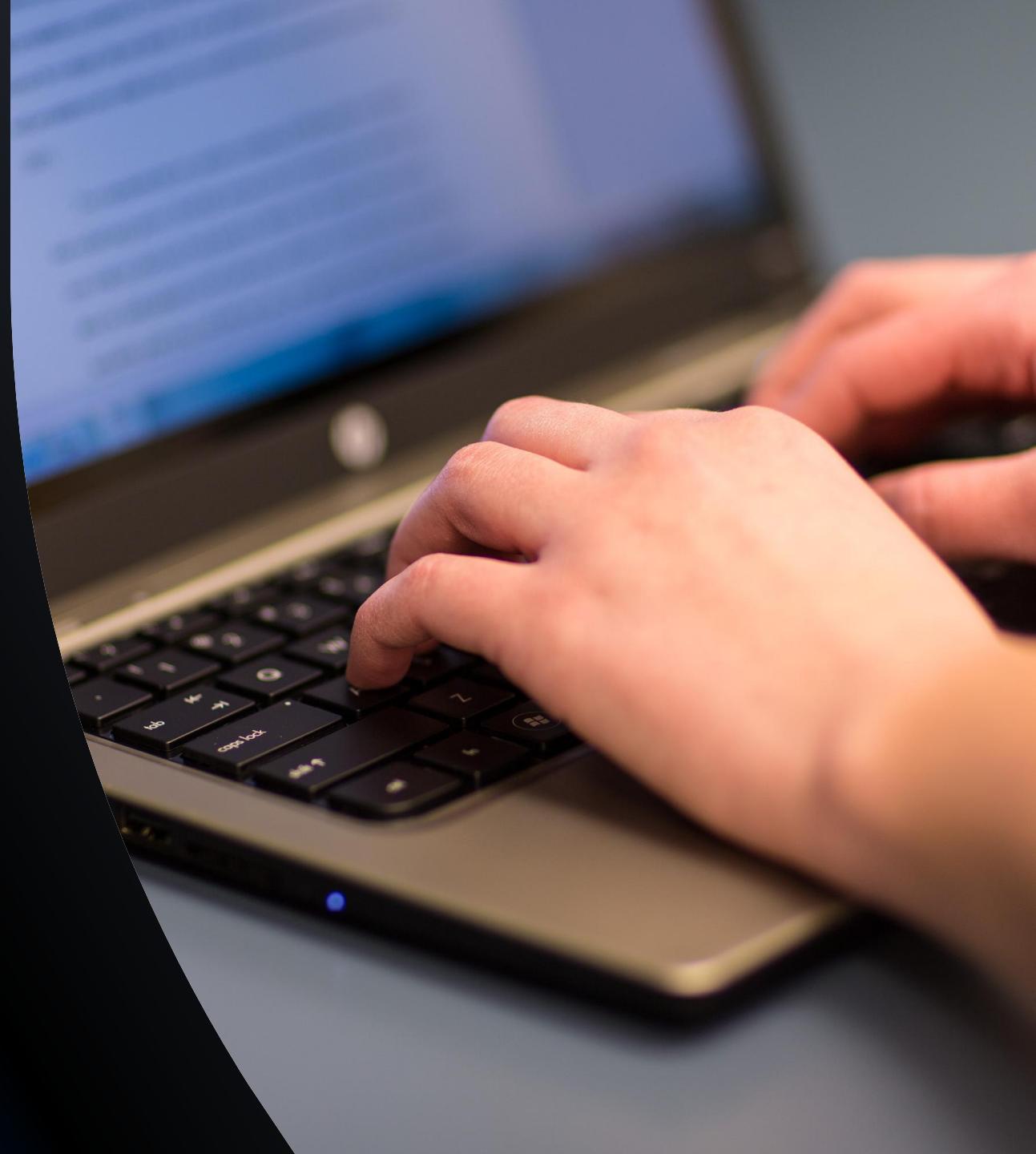
Term or acronym	Definition/description
MOSFET	Metal Oxide Semiconductor Field Effect Transistor. A low-power electronic transistor device used in digital applications.
NAND	This is one of the types of semiconductor Flash memory that Micron designs and fabricates. In NAND memory data is stored by “trapping” charge in a film. Data can be stored for up to 10 years without need for refresh. While NAND has a slower read and write than other memory types like DRAM, this memory is a good fit for many non-volatile high-density applications that require large amounts of storage like cellphones, SSDs, etc. NAND is not an acronym; NAND refers to the series arrangement of memory cells similar to the NAND (Not AND) digital logic.
Non-volatile	Refers to the type of semiconductor memory that will retain stored information even when power is removed from the part. Examples of non-volatile memory are NAND Flash and NOR Flash.
NOR	This is one of the types of semiconductor Flash memory that Micron designs and fabricates. Similar to NAND, in NOR the memory data is stored by “trapping” charge in a film. But unlike NAND, the NOR architecture is designed for faster read/write operations. While NOR is slower than DRAM memory, this memory is a good fit for many non-volatile applications and it is used for applications that require fast access time like code execution, for example for storing and booting the Operative System (OS). NOR is not an acronym; NOR refers to memory cells arranged in parallel like a NOR (Not OR) digital logic.
Periphery	A memory die is a memory chip in its state before it is packaged. The die has a memory array and a periphery. The periphery is the region of the die that has the many circuits that allow to operate on the memory array. Some of the periphery circuits are pumps, regulators, IO (Input/Output), ESD (electrostatic discharge circuits), etc.
QLC	Quad Level Cell. It refers to a NAND architecture that allows to program 4 bits per memory cell.
Resistivity	Electrical resistivity is a measure of how strongly a material opposes the flow of electrical current. Resistivity is represented by the Greek letter $\rho$ . Low resistivity indicated a material that readily allows movement of electrical charge.
Resistor	A device that reduces or limits current flow. A resistor is created by using a material less conductive (more resistive) anywhere along the path of current flow.
Scribe	See Frame
Semiconductor	A material that is between conductors and insulators on the resistivity scale. The semiconductor material used at Micron is silicon.

# Glossary

Term or acronym	Definition/description
SLC	Single Level Cell. In NAND Flash, it refers to a NAND architecture that allows to program only 1 bit per memory cell.
Silicon, doped	A small percentage of controlled impurities or dopants are added to the silicon to reduce its resistance.
Silicon, intrinsic	Intrinsic Silicon is pure silicon. This material has 4 valence electrons and is very resistive. Intrinsic silicon has very few applications in memory chip manufacturing.
Silicon, n-type	An n-type dopant is an element that is added to the silicon that has more valence electrons than the silicon. The most common n-type dopants used at Micron are arsenic (As) and phosphorous (P), both with 5 valence electrons. In the regions of the die where the silicon has been doped n-type there is an excess of electrons so current is carried by electrons.
Silicon, p-type	An p-type dopant is an element that is added to the silicon that has less valence electrons than the silicon. The most common p-type dopant used at Micron is boron (B) with 3 valence electrons. In the regions of the die where the silicon has been doped p-type there is an excess of "holes" so current is thought as carried by "holes" that have a positive charge.
TLC	Triple Level Cell. In NAND Flash, it refers to a NAND architecture that allows to program 3 bits per memory cell.
Transistor	An electronic device that can control the current running through it – like an On/Off switch.
Volatile	Refers to the type of semiconductor memory that will lose stored information when power is removed from the part. Examples of volatile memory are DRAM and SRAM.

# 7. Document Updates

micron



# Document Updates

Date	Description
January 2025	<ul style="list-style-type: none"><li>• Added goals, objectives and target audience</li><li>• Added several new images</li><li>• Added acronym legends</li><li>• Added glossary section</li></ul>
April 2025	<ul style="list-style-type: none"><li>• Slide 57: Added DRAM 1<math>\gamma</math> technology – Micron's newest DRAM technology</li><li>• Slide 58: New slide comparing DRAM 1<math>\alpha</math>, 1<math>\beta</math>, and 1<math>\gamma</math> technologies</li><li>• Slide 79: Added summary slide DRAM vs. NAND</li></ul>
January 2026	<ul style="list-style-type: none"><li>• Slides 7, 8, 20, 21, 62: replaced images with newer Micron products</li><li>• Slide 59: new slide</li><li>• Slide 60: new slide</li><li>• Slide 81: new slide</li></ul>

# Educator Hub

micron

© 2020–2026 Micron Technology, Inc. All rights reserved. Information, products, and/or specifications are subject to change without notice. All information is provided on an “AS IS” basis without warranties of any kind. Statements regarding products, including statements regarding product features, availability, functionality, or compatibility, are provided for informational purposes only and do not modify the warranty, if any, applicable to any product. Drawings may not be to scale. Micron, the Micron logo, and other Micron trademarks are the property of Micron Technology, Inc. All other trademarks are the property of their respective owners.