Enabling Technologies for Scalable Superconducting Quantum Computing

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Experiments with superconducting quantum processors have successfully demonstrated the basic functions needed for quantum computation and evidence of utility, albeit without a sizable array of error-corrected qubits. The realization of the full potential of quantum computing centers on achieving large scale fault-tolerant quantum computers. Science, engineering and industry advances are needed to robustly generate, sustain, and efficiently manipulate an exponentially large computational (Hilbert) space as well as supply the number and quality components needed for such a scaled system. In this article, we suggest critical areas of quantum system and ecosystem development, with respect to the handling and transmission of quantum information within and out of a cryogenic environment, that would accelerate the development of quantum computers based on superconducting circuits.

I. INTRODUCTION

Nearly a century after the mathematical and philosophical foundations of quantum physics were laid, we are now embarking on the challenge of producing technologies that leverage uniquely quantum phenomena to execute information processing tasks that are beyond the reach of conventional classical hardware. The basic functional elements needed for universal quantum computation have been demonstrated in proof-of-concept experiments. Evidence of utility is also emerging.

More qubits with a higher degree of coherence than currently available is a common goal to move towards the full promise of large scale fault-tolerant quantum computation (FTQC). Significantly larger machines are anticipated than in quantum computers that exist today. Supporting the pursuit of improved qubits in a scaled environment, advances and ecosystem development is sought for an entire suite of technologies that provide the capability to efficiently shuttle signals and information on and off a quantum processor.

In this article, we focus on superconducting qubits and consider technologies that would accelerate scaling to a significantly larger number of qubits for future large scale fault-tolerant quantum error corrected systems greater than 100-1000 physical qubits. In this discussion we focus on the interface with a QPU rather than on the materials science and quantum electrical engineering needed to produce an array of highly-coherent, highly-entangled qubits. We first examine some motivations for modular architectures; we then explore the cryogenic back-plane where a QPU is placed; the need for cryogenic electronics; the classical controls needed to operate a quantum computer; and finally the classical computing resources that need to be paired with a quantum computer. This report is the outcome of discussions that began among participants of the Roadmap Workshop on Developing the Complementary Technologies to Enable Quantum Computing, hosted by the CIFAR Quantum Information Science program.

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II. MODULAR QUANTUM PROCESSORS

A. Defining a Module

Increasing the number of superconducting qubits on a single substrate die heightens challenges related to qubit yield (including performance uniformity), qubit frequency collisions, and wiring complexity. There are, therefore, advantages to considering modular qubit architectures, which can range from attaching multiple qubit dies ("chiplets") to an interconnect substrate providing control and readout wiring as well as inter-die connectivity, to placing qubit dies in connectorized packages and using cabling to provide the needed inter-die connections. Similar modular designs can be used for the control and readout stacks between the qubit modules and the room-temperature end of the cryostat, simplifying the complexity of each module-specific stack, while retaining quantum-coherent communication linkages between the qubit modules. If these linkages are maintained at sufficiently low cryogenic temperatures, these can use microwave signals to achieve and maintain quantum coherent connectivity [83]; this approach, however, is not conceptually distinct from simply building a larger cryostat to accommodate larger circuit designs. If, instead, room temperature linkages are needed, for instance to link modules in distant cryostats, quantum coherent transduction between microwave and optical frequencies would be required.

B. Engineering/Implementation Considerations

Different versions of these levels of modularity have been explored, including dies mounted on a substrate [48], qubits connected by on-chip waveguides [126], packaged qubit circuits connected to one another with moderate-length cabling [126], qubits linked by a 64 m long cable within a conventional cryostat [100], to qubits with completely separate control, readout and cryogenic stacks linked by a 30 m cryogenic link used to demonstrate a loophole-free Bell inequality violation [109]. We note that in this context, different link lengths lead to different communication modalities: Very short links, with lengths less than a few wavelengths at the qubit commu-

(a) On-Chip Waveguides (<1 cm)

(c) Linked Cryopackages (~10 cm)

(d) Distant Modules (>1000 cm)
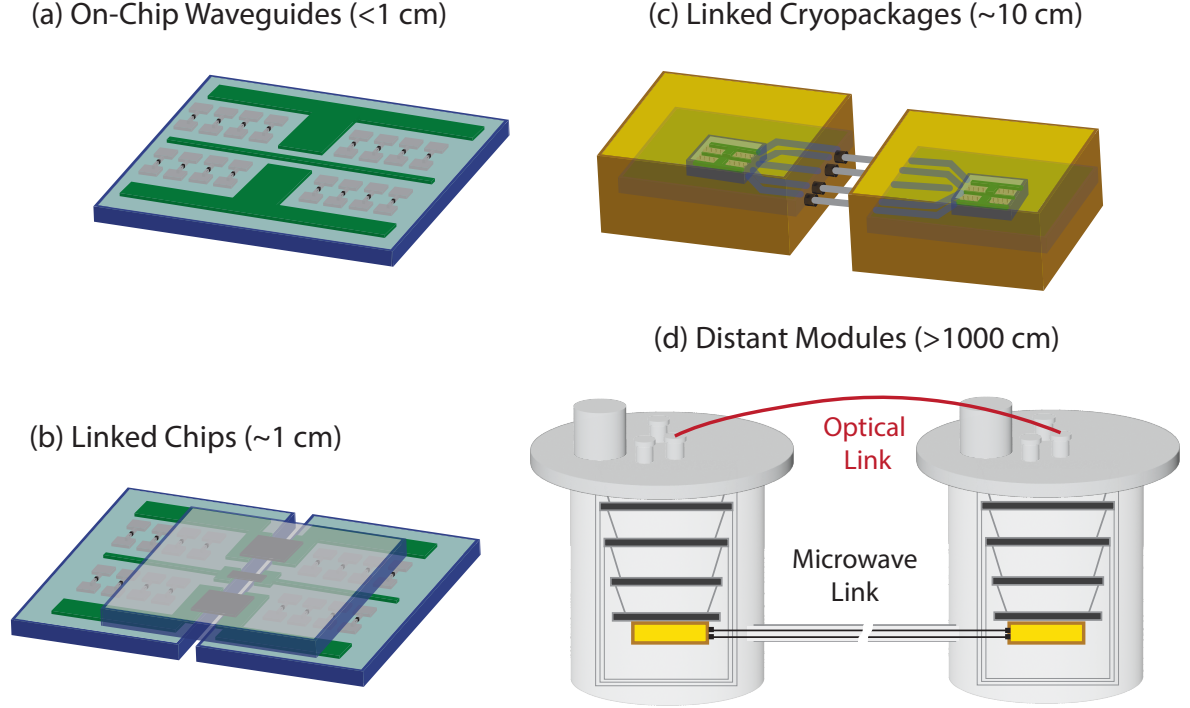
(b) Linked Chips (~1 cm)

Optical Link

Microwave Link

FIG. 1. Modular QPU Approaches: (a) Interconnected processing units linked by on-chip microwave transmission lines, (b) separate QPU chips connected by a linker chip, (c) independently packaged QPUs connected by cabling in an single cryostat, and (d) independent QPUs linked by either native microwave frequency links of approximately one or more meters, or via conversion to itinerant optical photons in different cryostats for greater than 1000 cm.

nication frequency allow direct qubit-qubit swaps, while for longer cable links, swaps via resonant cable modes or shaped envelopes for itinerant (mobile) photon signals are preferred. While swaps using "dark modes" can sidestep losses associated with low quality-factor cabling [79], these tend to be slower than direct "bright mode" swaps or itinerant signals. "Bright mode" swaps or itinerant signals, however, require very high quality factor cables and cable-module connections [96, 126], which present challenges for longer-range direct coupling.

An important future consideration for longer cable links will also be the development of 'hot swap' cable-connect configurations (e.g. at 4K or mK) that would allow isolated fridge modules to be brought down for maintenance without stopping the entire system.

For longer connections outside a cryostat, optical fibers or free-space transmission of optical signals are highly appealing approaches. However, using these for quantum-coherent communication will require a means of transducing between microwave signals generated by superconducting qubits and optical signals for transmission, for which there are a number of approaches being pursued, mostly based on methods of generating microwave-frequency sidebands on an optical carrier using optomechanical or electrooptic methods [39, 58, 66, 76, 91, 104, 119, 125]. How such communication channels will be used will depend on the available fidelities and data rates,

which will also determine whether these links can serve to extend a quantum computation over large distances, such as using teleported gates [5], or if instead these are a means to securely communicate private information [47]. We note that most optical communication schemes rely on good long-term memories at the endpoints [47], for instance provided by sufficiently error-protected logical qubits.

C. Quantum Error Correction and Modularity

While qubit modularity offers relaxed requirements for qubit uniformity and module wiring, it can significantly complicate the picture when considering quantum error correction. This leads to research questions of optimal distribution of logical capability and communication. Multiple modules, with possibly separate control and readout stacks might, for example, provide a backbone of quantum memory [15, 43, 93], whose size scales with the number of modules, while other logical functionality might be distributed to its own modules or integrated in some fashion with the memory modules. Regardless of the architecture choices, arranging for fault-tolerant operations across modules introduces challenges and a complex trade space. The module-to-module interconnects ideally need to extend the warp and

weft of the code fabric used within each module, in line with and uninterrupted by the module boundaries. The inter-module interconnect densities and fidelities would also need to be sufficient to maintain the effective code distance and functionality introducing performance and yield challenges for hardware and architectural choices. Furthermore, control and readout electronics, error decoding software, and the algorithmic compilation software, would all have to be designed and operated to account for these module boundaries.

One way to reduce the challenge is to reduce the number of modules and interfaces through reducing the number of qubits per logical qubit. Such a direction also reduces qubit yield requirements. Recent work on high code rate quantum low-density parity-check (qLDPC) codes has recently identified more hardware implementable choices [15, 118]. Complementing other architecture works relying on more orthodox code choices like surface code, a modular universal fault-tolerant qLDPC architecture has been described and numerically benchmarked [120].

III. CRYOGENIC SYSTEMS

A. Optimized Temperatures and Cooling Powers for Cryostat Stages

Many proposals for long-term fault-tolerant quantum computing require qubit numbers that are orders of magnitude greater than the capacity of available fridges, even when accounting for densification of components and reduction of thermal loads per qubit. One approach to extend fridges is to monolithically increase the size of the fridge. There are, however, challenges to increasing the size of a single volume. Practical concerns include limits of the facility capacities, for example, sizes of building entry points and load-bearing floor limits in typical data centers, while cost reduction per qubit is also critical and reduction of cost for equivalently scaled measures such as cooling power or working volumes have not yet been shown to improve through monolithic increase of fridge size.

Modular fridge architectures, coupling unit fridges through tunnels [83], for example, has been demonstrated in custom cases and represent an alternative path towards extensibility. Notionally, modular units that could be connected according to demand would allow growth of cryogenic environments according to need, while keeping cost per cooling power and volume at least relatively constant, while numbers of qubits per fridge might be scaled up (i.e., reducing cost per qubit), Fig. 2. Striving for minimum distances between adjacent modular fridge quantum processor payloads will also be desirable to maximize high-fidelity long-range coupling (l-coupling) [14].

A sense of standardization, for example, of plate spacings and port sizes would also behoove the community,

Stage	Temperature (K)	Cooling power (W)
PT1	≤ 50	25
elec. cntrl	$\sim 4\text{-}20$	25-50
PT2	$\sim 3.6\text{-}4.5$	$\sim 2\text{-}3$
still	≤ 1.2	$\sim 4\text{-}5 \times 10^{-3}$
CP	≤ 0.2	$\sim 1\text{-}2 \times 10^{-4}$
MXC	≤ 0.02	$\sim 2\text{-}3 \times 10^{-5}$

TABLE I. Approximate magnitudes of available cooling powers needed for temperature stages of a modular fridge unit, see Fig. 2, assuming roughly 2 PT and 'large' fridge dilution unit cooling capacity assigned to all the stages other than the elec. cntrl. stage [10, 87, 98, 128]. Some additional allowance on the higher end of the ranges is indicated for example for the PT2 stage to accommodate expected additional load of LNAs.

allowing fridge companies to focus on competitive advantage in cooling performance and cost while not being hampered by customization of retrofitting mechanical interfaces for componentry (e.g., cable and connector dimensions). Viewed from the perspective of the QC integrator, there are non-trivial time and cost barriers to retrofit a QC system to different mechanical configurations. To date, no fridge vendor offers a truly incrementally extensible modular solution.

B. Power

There are a number of dilution refrigerator vendors which offer similar 'large' cooling power that have become workhorse units for QC integrators. These can be representative of a fridge module. Their capabilities center on a combination of 2-3 pulse tubes (PT) and dilution unit capability providing $\sim 20\text{-}30$ μW of cooling power at 20 mK. Temperature zones generally breakdown into a PT1, PT2, still, cold plate (CP) and mixing chamber (MXC) stages, see Table I. We also assume that there will be an electronics control (elec. cntrl.) stage that supports cryoelectronics control (e.g., cryoCMOS) and that could operate at an intermediate temperature between 4-20 K. Assuming of the order 1,000 qubits per fridge unit at ~ 1 mW per channel (i.e., 3-4 channels per qubit [6, 15]), the necessary cooling power for such a control electronics plate would be $\sim 30\text{-}40$ W. Two pulse tubes applied to support a "large" fridge configuration is common and provides approximate power needs for the dilution system, radiative load, and passive wire cooling (see wiring section). A third PT or some other cooling power source would be necessary to supplying the tens of Watts for the electronics control, if the system design calls for moving a large fraction of control electronics into the fridge module. Coarse estimates of cooling powers for the different stages can be estimated from these order of magnitude considerations, see Table I.

Wall power of scaled FTQC systems could grow to as large as GW scale and therefore become a relevant
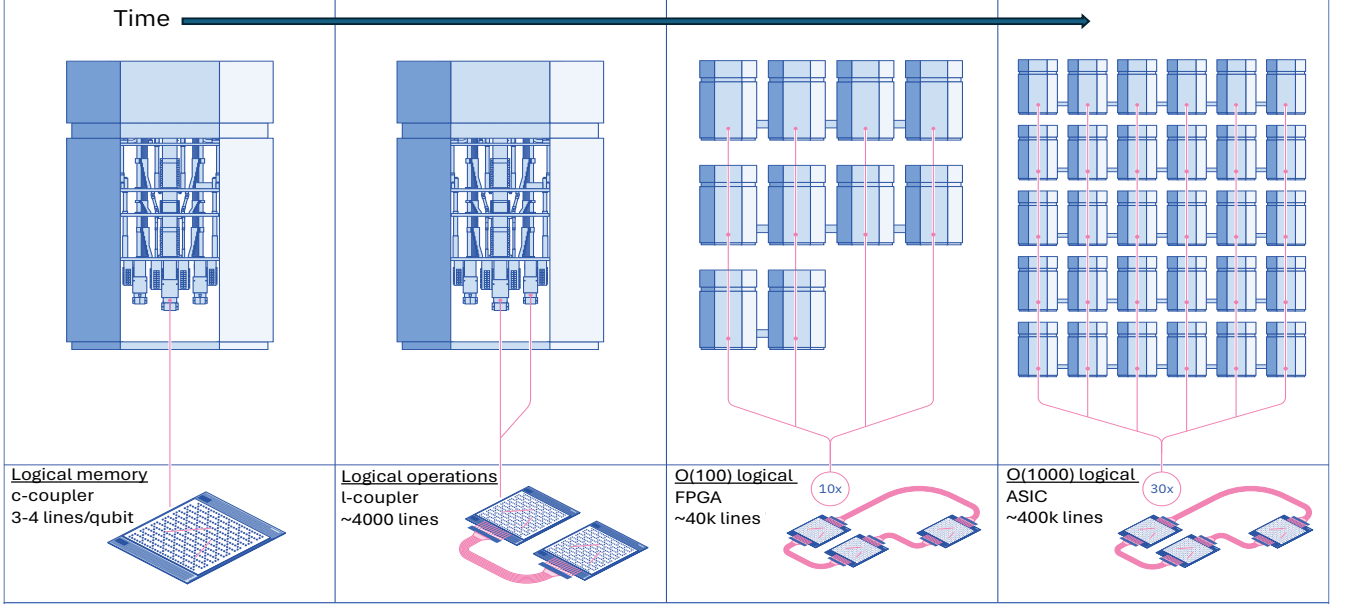
FIG. 2. Example evolution of fridge extensibility to data center size. A contiguous volume is established through connection of fridge modules. Quantum processing chips are also modular connected using l-couplers as defined in Bravyi et al.[14]. Commercial systems consisting of two dilution units, $\mathcal{O}(25~\mu\text{W})$ cooling power at the mixing chamber, and two to three pulse tubes has become a commonly used size and is a conceptual starting point for practical fridge module cooling powers, volume, weight, and cost. A third PT or some other source of cooling power would be needed for the elec. cntrl. stage.

focus of design and innovation to minimize marginal run/compute cost. The fridge system wall plug power represents a large fraction of that power and alone could grow to comparable magnitudes as classic data centers when scaled to fault-tolerant error-corrected sizes. Pulse tubes are a dominant wall plug power demand, ∼10-15 kW with cooling power efficiencies of ∼1:1500, cooling power at the lowest temperature PT stage to wall plug power. The efficiency is sensitive to factors such as the operation temperature choice and optimization of thermal coupling between stage and PT (e.g., copper braid). Inclusion of cryogenic CMOS for control will further increase cooling power demands within the fridge with possibly ∼25 W to source ∼1000 of qubits and might suggest operation of stages at intermediate temperatures between ∼3.6 K and ∼50 K. As systems are scaled orders of magnitude, alternate higher efficiency cooling approaches will be desirable to provide 'greener' and thereby cheaper computing. Efficiency can be expected to improve at higher temperature stages from simple arguments based on Carnot efficiency. Judicious placement of supporting componentry such as low-noise amplifiers (LNAs) and other electronics at as high a temperature as possible will be desirable. Cooling at higher temperatures furthermore provides more design space for alternative cooling technologies. There are also precedents of high ∼10 kW cooling using liquid helium cryoplants that for example provide efficiencies of ∼1:220 for ∼4.5 K [29]. However,

there are nontrivial practical challenges for implementation including overcoming efficiency losses related to distribution and service-ability of future very large systems. In the context of National Laboratory experience in large scale cryogenic cooling, this may be an area of fruitful public-private collaboration.

C. Rare resource utilization: ^{3}He volume per qubit

Dilution refrigerator technology is the predominant approach for cooling of continuous operation multi-qubit devices. Keeping the qubits as close to the achievable base operating temperature of these systems (e.g., targeting ≤20 mK), will become increasingly critical to minimize deleterious thermal excitations across increasingly large qubit numbers to achieve uniformly high-fidelity qubit operations and low leakage. Present mixtures of ^{3}He/^{4}He are central to their operation. The ^{3}He is extremely rare and has historically been dominantly supplied from the 12.3 year tritium half-life decay. The tritium supply is a byproduct of U.S. and Russian nuclear weapons stockpile stewardship.

In the United States, the cost of ^{3}He has been subsidized and is supplied through programs like isotopes.gov, which have mostly been sufficient for demand excepting historical demand spikes [107]. Notably, 'at cost' production is estimated to be substantially higher particu-

larly for alternate approaches like trace source extraction [107]. The U.S. and world production of ^{3}He was for many years, $\mathcal{O}(10^4$ liters/year). The majority of its use has been for purposes other than cryogenics related to quantum computing [107]. To address recent and anticipated greater future demand compared to supply, some companies (e.g., Air Liquide) have started to supply some of their ^{3}He from niche stocks at commercial heavy-water electric generation reactors [56]. These reactors can capture and accumulate ^{3}He. A source in Canada, for example, has been leveraged as a temporary buffer in response to demand and scarcity challenges.

Scaling of mixing chamber power has relied primarily on incrementally adding dilution units to a fridge. Recently, IBM has shown that a 1000 qubit system ~25 qubits/liter [30] is possible relying on dilution units that require ~20 liters per unit. Systems of 100k qubits would demand large fractions of the yearly world production based on naive linear scaling. Planning for success, a combination of continued reduction of mixing chamber heat load per qubit, increased supply, and perhaps improvements in cooling power per liter ^{3}He, will optimize the dilution refrigerator architecture with respect to cooling power vs temperature. There is a quadratic cooling power dependence on temperature for a dilution unit, and utilizing this effect when scaling the system has the promise of reducing the amount of ^{3}He per qubit. Advances in alternative cooling approaches (e.g., continuous adiabatic demagnetization refrigeration) could complement ^{3}He based cooling to avoid ^{3}He becoming both a dominant cost per qubit and a potential supply bottleneck.

IV. CRYOGENIC ELECTRONICS

A. Testbeds for Cryogenic Electronics and Components, and Standardization Considerations

In Ref. [11], Boiko et al. explain that: "one of the limitations hindering a reliable QC supply chain is the ability for companies to provide microwave components that have been tested and qualified at cryogenic temperatures. However, the domains of cryogenics and microwave electronics are two highly specialized and rarely overlapping disciplines. The rapid increase in QC scaling drives the present need for dedicated test protocols and infrastructure for QC component testing..."

A new product family typically requires several design-fabricate-test cycles to reach market readiness. Currently, component manufacturers are equipped to develop and qualify their components in the standard temperature range of -40 °C to 85 °C. The cost of establishing cryogenic testing capability and the naturally longer test cycles prevent component manufacturers from fully qualifying their products for the QC market. Thus, the ability to perform economical cryogenic component testing is critical as QC systems scale and are commercialized.

Why doesn't this capability exist today? Two reasons stand out as most notable. First, there has not been significant business incentive from QC system integrators (i.e., those entities driving the scale and development of QC technologies) for commercially available test infrastructure, due in large part to the small-scale research nature of QC to date. Second, investment into the unique skill set and infrastructure is too costly for most companies.

Given the above, it would reduce barriers if Test as a Service (TaaS) could be incentivized to foster a healthy QC market ecosystem. Failing to establish this capability will result in several consequences that can impact the ability of the quantum industry to mature. For example, some of the standard temperature component manufacturers will find it prohibitively difficult to enter the QC market given their lack of ability to develop and test components that meet the requirements of system integrators. This will result in the component ecosystem being supported by only a small number of specialized component manufacturers. The absence of a competitive marketplace stymies both the innovations and the competitive labor market required to rapidly advance and scale cryogenic component technologies for QC. Volume testing will furthermore remain difficult and burdensome while standard methodologies are not available to unify the market or ensure accurate and repeatable product specifications. Traceable and certifiable testing at scale of components is also necessary to reach quality and reliability for production environments.

Example microwave components to be tested in a testbed include passive components such as RF wiring, connectors, qubit shielding, attenuators, filters, directional couplers, circulators and isolators, and active components such as LNAs, quantum-limited amplifiers (QLAs) and microwave switches. Characterization items differ slightly depending on the component and the level of integration. Required capabilities of a testbed are measurements of S-parameters, qubit performance, materials characteristics, failure in time (FIT) rates, thermal cycling reliability, etc. Scaling systems to $\mathcal{O}(100k)$ qubits introduces a greater importance on reliability and FIT, particularly for components within the fridge, when considering the relatively high time overhead to warm and open the fridge environment to access and replace components.

There are a number of challenges to overcome in scaling the system to $\mathcal{O}(100k)$ qubits, but one the first priorities will be to minimize the volume and weight of microwave passive components that incorporate permanent magnets, such as circulators and isolators, which are essential for routing the microwave pulse signals required to control and read out the qubits. For example, it has been reported that it is possible to reduce the volume to one-third and the weight to one-fifth compared to conventional isolators while maintaining high isolation characteristics over a wide frequency range. Approaches based on Josephson junctions are an appealing but speculative

alternative worth further investigation as well. It seems, regardless, extremely challenging to pursue the plan illustrated in Fig. 1 without solving this problem (i.e., reducing volume and weight). If the microwave passive components are first miniaturized, the valuable large volume of the lowest temperature region of the dilution refrigerator can be effectively utilized to achieve quantum connections between modular processors as described in Bravyi et al. [14].

Test components are placed inside a cryogenic refrigerator such as a dilution fridge, and the component is characterized, for example, the S-parameters are measured by a vector network analyzer. To increase throughput, multi-channel switches are a common feature allowing switching between multiple components within the fridge and smaller and faster switches are of interest. Further innovations providing faster cycle times and throughput of components are of great interest.

For the material characteristics, measurements such as thermal conductivity, resistance, etc. and their temperature dependencies are performed. Characterization approaches depend critically on the type of component to be probed. Qubit performance tests include a wide variety of experiments to determine qubit device parameters, such as coherence times, gate errors, measurement errors, and error per layered gate (EPLG) experiments [90]. Whether one performs all or some of these experiments depends on whether the control and readout chain includes the component under test. For components on the readout line, for example, insertion loss and thermal isolation due to the component can be estimated from the impact on the readout SNR and qubit decoherence time (e.g., T_2), respectively. The component to be probed and a reference are arranged in parallel and switched with the multi-channel switch. Overall, qubit architecture specific measurements can be more challenging to provide as a service because of the level of customization and barriers to sharing of company information.

The need for a testbed to drive efficiency in the evaluation of, and to support standardization of cryogenic components is also a challenge facing the quantum design community in the context of deriving learning for custom CMOS designs (especially cryo-CMOS designs). It is a challenge to establish a representative testing context meaningful to test cryo-CMOS and it demands that researchers implement not only exploratory circuits, but also qubit test structures, connectivity solutions and a system framework. The development of one or more reference testbeds that (1) enable connection of exploratory circuit designs both to target qubit test payloads and to a system infrastructure that provides a wrapper to support qubit calibration and gate execution, and (2) support a means to compare to best-of-breed qubit interface electronics solutions would bring great value to the broader community.

In an attempt to meet this demand, for example, several testbeds for QC components are being planned in Japan by the National Institute of Advanced Industrial Science and Technology (G-QuAT) and Osaka University. Also, the University of Tokyo, in collaboration with IBM Quantum, has begun collaborating with Japanese companies to develop critical QC components that can function at dilution refrigerator temperatures, using testbeds installed at their Quantum Hardware Test Center.

B. Cryogenic Wiring, Integration and Technology Foundries

The i/o of signal between qubit and control electronics is a central bottleneck to scaling. Cost, thermal load and space must be scaled along with the number of qubits given a fixed fridge unit (i.e., fixed fridge volume, escape port sizes and cooling power) [42, 75, 85, 101]. Approaches to this challenge include multiplexing (e.g., readout and control), densification of the wiring (e.g., flex), introduction of control within the fridge (e.g., cryoCMOS) and alternative signal distribution approaches to modify bandwidth of channels and/or footprint (e.g., RF over fiber).

Flex is a promising path to substantially reducing cost, thermal load and space, while still obtaining sufficient performance (e.g., attenuation and crosstalk). Flex has been investigated for quantum computing [1, 2, 111] but is, for QC, still at a relatively custom design and fabrication stage. There are furthermore few standards for quantum system integrators (e.g., lengths, thermal conductivity, attenuation, cross talk or connectorization choice) and the rapid need to scale drives rapidly changing specifications for a spectrum of quantum integrator custom solutions including the possibility that solutions will be eliminated in relatively short times as discrete elements are integrated into more compact and cost effective subsystems [3, 32]. This makes it extremely challenging for vendors to design their own solutions and intersect with quantum integrators because of challenges with cost of paying vendor margins for small market components, moving targets, timely communication and short lived solutions.

A model of integrator design ownership (e.g., foundry model) is an alternative functional model that provides more agile response, while reducing risk for the manufacturer who can sell to multiple integrators avoiding custom in-house design costs and intersection challenges for what is a relatively small market. A need for vendors that can respond to both superconducting and normal metal flex fabrication is needed. Normal metal wiring will likely be a sustained need for at least the purpose of power supplies and some signaling even if other control electronics (e.g., cryoCMOS) is introduced at cold stages close to the quantum processor. There are fewer options to dislodge the need for superconducing wiring and therefore superconducting flex represents a continuing opportunity for both research and development of foundry-like options as improved materials and processing capability is needed.

To further illustrate the parameter space, returning to

the modular fridge model and superconducting wiring as an example. QC integrators will be driven towards 1000s of qubits per fridge-module due to drivers such as cost per qubit and practical use of space. Available space, exit port area, and cooling power of fridges can be roughly estimated at an order of magnitude as they are not very agile in view of practical challenges of cost to change, risk, and lead time to make significant changes to fridges. In this context, order of magnitude wiring density and thermal requirements can be made. If one assumes a high-degree qubit coupling architecture (e.g., $\sim$4 signals per qubit assuming tunable coupling [6, 15]) and a limited number of ISO100-like line-of-sight ports connecting to the superconducting lines, roughly $\sim$4-5 per fridge-module, densification of wiring might be assumed to push towards cabling line densities of $\geq$ 1 line/mm. This estimated density is driven in part due to an assumption of some minimum spacing between flex cables, limited due to practical considerations such as cable-to-cable connectorization limits leading to only space for $\mathcal{O}(10)$ stacked cables of width $\mathcal{O}(100)$ mm wide that pass the ISO100-like port or common side loading bay assembly sizes. Passive heat load management will further demand of the order 1 μW-cm/K assuming a length separation of $\sim$500 mm between a $\sim$4 K stage and the QPU. In contrast, estimates for signal performance requirements like bandwidths or tolerable crosstalk and loss are more challenging because of the qubit architecture specificity needed.

In the context of QC integrators exploring many qubit architectures, the choice of cabling materials, stack-up and connectorization to simultaneously satisfy, mechanical, thermal, electrical and cost performance will likely continue to remain custom. In this light, having foundry capabilities for the flex technologies that can respond to custom requests appears to have a great deal of merit.

Foundry capabilities apply well beyond the flex example. One might anticipate that CMOS foundries will play an ever greater role as ASIC solutions are developed (see later section), for example, including the displacement of present discrete components such as HEMT based LNAs by more integrated multi-channel and lower cost biCMOS or CMOS solutions [8]. In some qubit architectures, tolerance to lower measurement fidelity may allow performance to be traded for reductions in cost, size, weight and power (CSWaP).

We also note a gap in superconducting foundry options that support development and commercialization of componentry that could significantly reduce CSWaP, such as, multi-channnel integrated isolators (e.g., non-ferrite approaches [3]), quantum-limited amplifiers and more speculatively low-power control electronics (e.g., DACs). CSWaP reduction or complete circumvention of readout components [97], for example novel approaches to reduce isolator sizes [84], remain an active parallel and competing area of research and development.

We now turn to a notable emerging research and development thrust in superconducting cabling, which is driven by modular concepts entailing entanglement between separate chips within a shared cryogenic environment [83, 96]. The need for ultra-low-loss connectivity will introduce a need for specialized high-Q superconducting wiring with photon loss comparable to that of optical long haul fiber (e.g, order of 0.1-0.4 dB/km [96]) as well as the development of complementary low-loss connectorization to the QPU. The best results have been observed in Al cables with low density teflon dielectric. It will be of interest to identify other materials motivated by the desire to widen engineering options (e.g., bonding, cable handling) and this may introduce a need for improved basic understanding with respect to engineering RF loss in dielectrics and superconductors at the single excitation level in these cable/connector geometries including extending the communities understanding of defects and two level systems within the skin depth of the metals and within the cable dilectrics. The refinement of plating processess may be a fruitful direction. In the near term discrete cable connectivity will be sufficient, but longer term research and development of higher density scaled solutions to produce more seamless connection between remote chips will be also likely be needed.

Another direction of interest is increasing bandwidth. More disruptive approaches such as RF over fiber [78] are of academic interest in the context that they are high-risk high-reward paths. In the case of RF over fiber, it is unlikely that such solutions will reach the MXC and still be viable from a cooling power perspective. However, the substantial bandwidth and low thermal conductivity of fiber are tantalizing and might offer important options for spatial transposition of control electronics (i.e., further away from the fridge), while providing delivery of signal to higher temperature stages combined with perhaps fewer active components in the fridge than cryoCMOS. Space around the fridge for electronics is increasingly a scaling constraint as qubit number is scaled for a unit fridge footprint for which RF over fiber could be useful. However, whatever alternative solution is identified, reliability, thermal load and cost relative to relying on brute force wiring still need to be shown.

V. CONTROL HARDWARE

A. Functionality and Reliability

Electronics solutions are needed to realize multiple functions in an error-corrected quantum computing system. These functions comprise RF control pulse generation, flux gate control signal generation, pump tone generation for quantum-limited amplifiers, RF readout pulse generation, low-noise amplification, readout discrimination, syndrome decoding, and system control and coordination. Electronics solutions must also be compatible with an end-to-end system design, software stack, and compiler infrastructure that enables appropriate abstraction to support efficient customer engagement with such
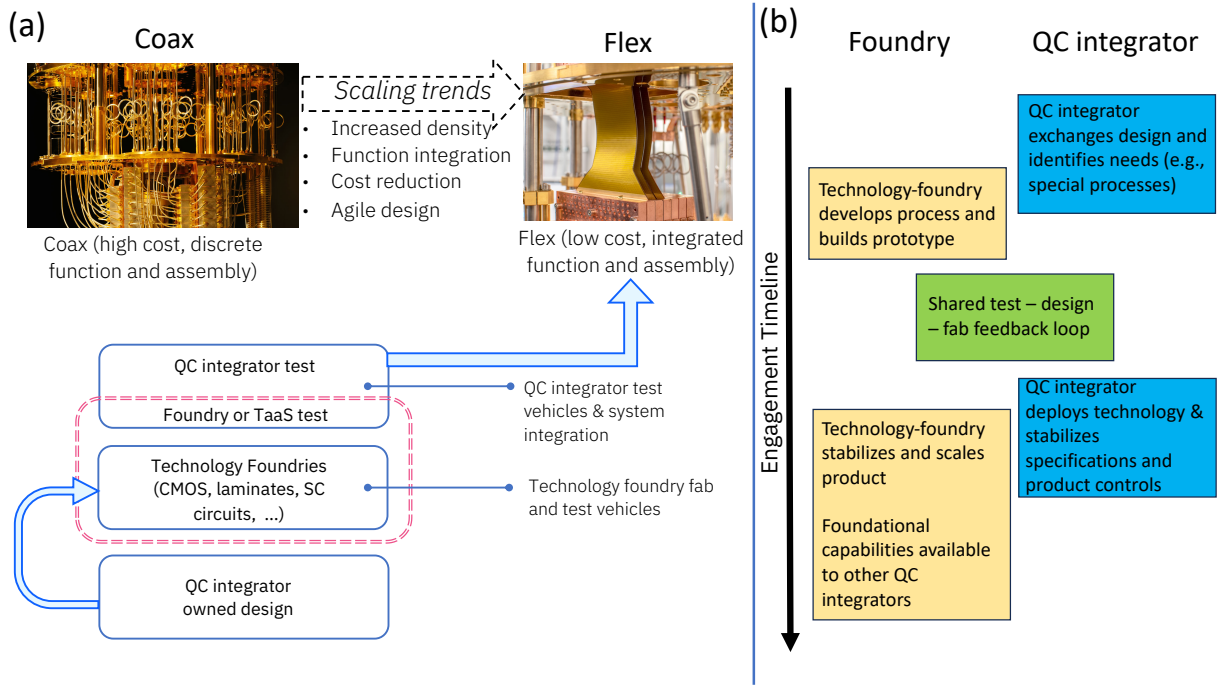
FIG. 3. (a) Functional relationship and (b) conceptual engagement timeline of technology foundries, QC integrators and test services.

systems. As systems increase in size and complexity, cryogenic electronic solutions may be needed to reduce signal travel times as well as wiring density. Current modalities envisioned for such control include cryogenic CMOS technology as well as electronic based on digital superconducting electronics.

As systems scale, robustness and reliability grow in importance. FIT rate analysis for the components used in quantum computing systems is therefore necessary. For system elements that do or will operate at room temperature, FIT data exists or can be generated using well-understood methodologies. For the elements of systems operating at cryogenic temperatures, however, FIT data does not exist and the appropriate conditions under which to acquire data and then develop associated models has not been defined. To address this gap, it is first necessary to identify intended use case classes for system components, including, for example, projected frequency of temperature cycling and target overall lifetimes. Establishing standard approaches, for example, to assess failure rates for cryogenic CMOS elements across multiple techonologies would also be valuable, as would the development of standardized approaches to evaluate failure rates for connectors, solder joins, flex cables, amplifiers, non-reciprocal elements, and other cryogenic system components. The creation of a test facility and an associated set of failure analysis methodologies that would drive clarity in the generation of failure rate performance would be very valuable in this context, see section IV A.

As described in more detail below, the choice of cryogenic CMOS versus room temperature CMOS for qubit interface electronics drives significant considerations regarding reliability, availability, serviceability, and performance. As noted below, cryogenic CMOS usage promises to reduce connector count and wiring density into the dilution refrigerator, which could improve reliability and assembly, but introduces what is today a question mark, namely the relative reliability of CMOS and associated packaging at cryogenic temperatures. The reliability of cryogenic CMOS and associated packaging will also be a significant contributor to serviceability and availability for future systems. Unlike systems that use room-temperature electronics for qubit interface control, systems that use cryogenic CMOS will require warm-up and cool-down if component replacement is required, making the need for a service strategy more critical, undoubtedly making servicing more challenging, and (comparatively) negatively impacting system availability. Key investments that would bring greater clarity to this space include reliability evaluation of cryogenic CMOS approaches and other cryogenic components as noted above. As systems scale, even independent of specific reliability concerns associated with any one component, efforts to develop redundancy solutions that extend all the way to the qubit plane and/or error correction approaches that tolerate isolated hard failure of connections to a subset of system qubits would bring value. From a performance perspective, as described in greater detail below, the use of cryogenic elements imposes a stricter power budget but offers potential for reduced noise and wiring complexity reduction; it also offers a path to support highly local feedback loops for branching operations, although the

compelling value of such a capability versus loops closed through room temperature solutions is not presently obvious.

B. Technology Implementation

Reduction of cost, size, weight and power is vital to achieving commerically viable systems. The path to further driving cost reduction necessarily demands the use of electronics solutions featuring levels of integration and customization (e.g., ASIC solutions) that are beyond those deployed in current known solutions. For each electronic component, it is necessary to consider the physical placement in the system, both from a thermal environment perspective, and, for room temperature elements, with respect to the location of refrigerator electrical ports.

As noted in the cost discussion below, per-qubit electronics cost is a significant challenge that must be met as a necessary condition for the realization of quantum computing systems at scales envisioned to support quantum error correction. Current approaches [123] that rely on racks of custom boards built from commercially available electronic components are viable for systems with even up to 1000 qubits. Such approaches, however, do not appear to support a path to the cost take-down needed for future systems as they scale toward qubit counts of order 100k and beyond. Integrated CMOS solutions operating at room temperature, within the cryostat, or in hybrid combinations are promising that would involve the exchange of a more significant up front non-recurring engineering cost and reduction in flexibility for a dramatic reduction in per-qubit bill-of-materials electronics cost. Extensive multiplexing has been proposed as a means to drive further cost reduction [99], but challenges are foreseen in effective support of quantum error correction in a highly multiplexed environment [45]. As a room temperature alternative to a full room temperature ASIC implementation, the use of FPGAs (operating at room temperature) with integrated multi-channel DACs and ADCs as primary qubit interface electronics is worth exploration, but this approach appears unlikely to support electronics cost reduction to the degree needed for future scaled systems. Note, however, that in scaled quantum computing systems, FPGA usage as an element that provides a customizable interface to CMOS ASICs and supports critical computation tasks (e.g. syndrome matching) is a near certainty.

A room temperature ASIC approach offers multiple advantages over a cryogenic CMOS approach. Power consumption limits are significantly less stringent for a room temperature design than for a cryogenic design, opening up the design space and helping to mitigate traditional power/performance tradeoffs. Design for serviceability is also more straightforward as replacing a board housing a room temperature ASIC is unlikely to demand thermal cycling of the quantum computer's dilution refrigerator.

Such an ASIC would also be designed within the supported temperature range for models and digital libraries associated with the vast majority of CMOS technology offerings of today. Such an approach also presents significant challenges compared to those associated with a cryogenic CMOS approach, however. Wiring density connecting elements at a cryogenic (e.g., 4K) stage of the dilution refrigerator to those at room temperature will be dramatically reduced if cryogenic CMOS is used. Similarly, connectorization challenges and connector density will be reduced in this case. Operating at lower temperature may further provide an opportunity for performance benefit in the cryogenic CMOS case, through reduction in thermal noise and improvement in other properties of CMOS technology at cryogenic temperatures. If superconducting flex can be used to link cryogenic CMOS elements to the qubit plane, an effective path to bypassing the signal quality/thermal conductivity trade space can be explored.

While cryogenic CMOS is promising approach, technical investment on the part of the broader community in a number of areas would be highly beneficial to accelerating progress. Achieving required performance while meeting cooling power constraints, especially if pulse tube coolers are used, is an area in which the research community has begun to make investments [25, 70, 121], but significant further effort is required. An additional high-level domain where investment is needed is in the area of CMOS technology and associated modeling. Enabling advanced node reduced supply operation—-including for SRAM—-will drive better optimization and improved power efficiency for cryogenic operation. Device, interconnect, and library modeling reflecting below 20 K behavior critical to enabling improved design, both to accurately predict design performance and to accurately predict design power consumption. Improved thermal modeling and thermal solutions will let us better estimate and optimize controller temperature. Understanding and mitigating stress effects for chip-package interactions at cryogenic temperatures will also be important. Reliability modeling for CMOS and other electronic components at cryogenic temperatures is needed to make scaled systems viable. Standardized approaches to enable serviceability of cryogenic CMOS will also be highly valuable. For both cryogenic and room temperature approaches, supporting investment in fully custom electronic designs despite the low volume nature of the current electronics for quantum computing market is a further imperative.

C. Cost/Budget

In the early days of the quantum program, quantum computing electronics were implemented primarily using off-the-shelf commercial instruments, resulting in an effective $\sim\$50,000$ per qubit for electronics cost alone. Some efforts at companies such as IBM have implemented custom discrete electronics-based solutions, which have

targeted both dramatic densification of the electronics solution while also achieving a substantial improvement in cost per qubit (e.g., perhaps an order of magnitude). While addressing electronics cost is necessary to achieve an acceptable cost point for scaled quantum computing systems, it is not sufficient. Major fixed cost contributions to the cost per qubit roughly break down into the categories of electronics, wiring and cryogenic environment. Approaches to reduction of cost in these areas are noted in the sections above.

A general challenge that the community faces is that quantum computing is presently a low volume application. Any consideration of the implementation trade space must strongly reflect non-recurring engineering cost in addition to unit cost and cost of operation. Physical footprint at the system level may have significant capital infrastructure implications, especially as cryogenic environment sizes grow (i.e., multi-fridge-module systems). The physical footprint of elements to be placed at room temperature but ideally near refrigeration units is also significant in that floor space is intrinsically expensive, as is the cabling needed to connect electronics to fridge ports while meeting required signal integrity specifications. Finally, for cryogenic elements, the volume within the refrigerator is a constrained resource and is therefore drives cost considerations.

It is also important to consider how use-case requirements will impact system cost. Current system designs are typically developed with flexibility and the need to support research in mind, the latter including not only qubit payload and gate exploration but also different means of implementing required control, filtering, and qubit interface functions. Scaled systems may eventually abandon the generality of today's research-focused designs in favor of more per-qubit cost-efficient and focused design points. This type of transition is important to enable the introduction of custom electronic designs into future quantum computing implementations, as ASICs typically will not deliver the same flexibility as will FPGAs or test equipment. Analysis and validation in the system-level and application context are critical to studying whether and under what circumstances lower performance, lower flexibility and lower cost elements might be appropriate to replace high performance, more expensive elements. One near term example might be, for example, determining alternatives to the high performance ultra low-noise amplifiers that are typically used in today's systems but for which readout performance might be sacrificed for certain qubit architectures and error correction choices.

VI. QPU TUNE-UP AND OPERATION

At the highest level of the computational stack, one step up from the classical control hardware layer, we now identify challenges around QPU operation, including pulse-design, periodic re-calibration, error minimization

strategies including error suppression, error mitigaton and error correction, algorithm implementation requirements, and ultimately, efficient validation of the quantum output for quality assurance. All of these tasks involve significant complexity and some require significant resources. Below we summarize current best approaches and address critical needs where appropriate, which broadly points to mitigate the challenging scope of low-latency, high-performance classical compute that is required for many of these tasks.

A major component of this section is various approaches to error minimization and performance validation, which are critical to optimize and verify the correctness of the QPU output. As described below, there are a wide variety of error minimization strategies with distinct capabilities and requirements. At the lowest level there are passive run-time strategies such as dynamical decoupling and randomized compiling. At the next level of complexity there are error mitigation strategies requiring an expanded family of circuits as well as preparatory benchmarking experiments, verification & validation of noise models and resource-intensive post-processing of data. Going forward fault-tolerant error correction will be adopted increasingly in the work loads. The computational load of these tasks of course depends on the details of the quantum algorithm, the error management strategy including architectural decisions of how to handle integration with high performance computing resources [67].

A. QPU Pulse-design, Tune-Up and Calibration

Preparing a quantum processor to execute an algorithm requires many parameters to be set precisely to allow high-fidelity gate execution (e.g., operation fidelities > 0.999) with minimal cross-talk. Typical errors that must be minimized include information/coherence loss to the environment via, e.g., materials imperfections, such as drift and fluctuations, in the classical control fields used to operate the QPU. Achieving this aim requires procedures for pulse-design and calibration, as well as routinely scheduled (ideally at lower-cost) recalibration and tune-up procedures. As the system size grows, the number of measurements/calibrations associated with these tasks grows rapidly, highlighting the critical need for robust, automated and resource-efficient solutions for these tasks. These tasks include low-level error diagnostic routines, for example, to assess and reduce infidelities of gate and measurement operations, cross-talk and drift-compensation. Most of these techniques are well-established and standardized and require minimal classical compute resources. At the other end of the spectrum there are the more recently developed high-level, high-resource cost characterization methods, such as Pauli error reconstruction, which can characterize QPU clock cycles (parallel instruction sets) across very large arrays of qubits and identify cross-talk and corre-

lations in multi-qubit error models. These methods have proven useful to characterize error models for large blocks of operations that are tremendously useful for error mitigation methods. They may also help optimize and inform decoding for quantum error correction, with the cost of requiring a significant fraction of QPU cycles and wall-clock time. A considerable amount of classical compute is needed even at current system sizes.

The more well-tested and well-established methods at the level of individual qubits and elementary operations include:

- Determination of the individual qubit frequencies and drive parameters for single and two-qubit gates via standard methods.

- Determination of the many-body cross-couplings in a given quantum processor graph via standard methods.

- Optimizing and benchmarking fidelities of a given pulse-design for sets of primitive gate operations is typically performed via randomized benchmarking (RB) [35] with random Clifford gates [31, 80, 81] or cross-entropy benchmarking [12], while estimating the fidelity of individual entangling gates is generally achieved via cycle benchmarking (CB) [38] with random Pauli for Clifford gates or dihedral gates [19] for T-gates.

- More detailed (Pauli) error learning for quantum operations on small numbers of qubits is possible with slightly more resource-intensive approaches such as gate-set tomography [95] or cycle error reconstruction [22], which combines the Pauli error learning ideas from [36] and the Pauli error amplification approach of CB [38]. However, when the errors are quasi-local, they can be learned efficiently [112] and self-consistently [26, 28] by adding constrained to the learning algorithm.

- Optimizing and benchmarking fidelities of mid-circuit measurement and dynamic circuit operations using RB methods [51, 62, 108], which are important for QEC and other circuit applications [16, 17, 23, 69]

- Older approaches to randomized benchmarking for elementary gates that are now less common include single qubit RB using a subset of the single Clifford gates [74], which has been shown to produce a biased estimator [13], randomized benchmarking with Haar random unitaries [35] which becomes inefficient for large numbers of qubits, and interleaved randomized benchmarking [82] with random Clifford twirls which shows significant bias due to systematic uncertainties in the presence of coherent errors [20, 21, 105].

- For more details, the reader is referred to the general theoretical framework for randomized benchmarking developed in [57].

Methods for characterizing errors on large (parallel) sets of quantum operations, e.g., cycles, layers or large circuit blocks, have been less widely adopted, and can be resource intensive, both in terms of QPU time and classical post-processing. These methods include:

- Optimizing fidelity for layers or cycles of quantum gates across n-qubits, i.e., parallel instruction sets, in a manner that detects all cross-talk and context-dependent errors, can be achieved via cycle benchmarking (CB) [38], with a resource requirement that is constant in the number of qubits but also requires high-fidelity high-weight Pauli measurements which proves challenging in many platforms. Alternate methods such as simultaneous RB [88], as simultaneous direct RB (i.e., layer fidelity (LF)) [89], avoid measuring high-weight Pauli operators and have different resource requirements than CB with the drawback that although LF is a lower bound and often, to good approximation the fidelity, it is not exact in the presence of inter-gate cross-talk, see e.g. [89]. All of these approaches become more resource-efficient if low-latency, single-shot randomization is available in the control hardware [46].

- Diagnosing multi-qubit error rates, including cross-talk and context-dependent errors, is known to be possible in principle even across large number of qubits via Pauli error channel estimation techniques [36] and more scalable RB approaches [60]. Moreover the Pauli error rates can even be learned to multiplicative precision, for example, via the amplification approach of cycle error reconstruction (CER) [22, 27, 38, 40, 53], which has been extended to include mid-circuit measurements [59, 124**?**]. In practice, the high QPU-time and classical post-processing required by Pauli error channel estimation imposes a limitation on how much information can be learned (there is afterall an exponential amount of information available). There is some evidence that estimation of even a small fraction of Pauli error rates can predict logical error rates and even improve decoder performance [40, 63]. Clifford benchmarking is also sufficient for some noise model classes [92]. Average circuit eigenvalue sampling [61] is an alternative scheme for Pauli error learning that is restricted to Clifford circuits, such as syndrome extraction circuits, but is known to give inaccurate results in the presence of inter-gate cross-talk. All of these schemes can have very high-resource costs and, as discussed below, more resource-efficient methods, based on validated error model assumptions, remain an important need and area for further research. These methods also benefit significantly from low-latency single-shot randomization [46]. This is especially true in the context of frequent, periodic recalibration.

- For more details, the reader is referred to a recent

review article [54].

While many of the above optimization tasks are resource intensive when performed comprehensively (i.e., without strong assumptions on the unknown error model), there is an important need to identify short-cut methods to be used during the fequent, periodic recalibrations required during operation. As noted above, these short-cut methods may require additional, strong and system-specific assumptions on the error model, ideally validated by prior, more comprehensive error diagnostics, to reduce the scope of error learning [52]. Because all of the best-known methods for Pauli error learning require some form of twirling/randomization to induce a stochastic (Pauli) error channel, the efficiency in terms of wall-clock time will certainly benefit greatly from low-latency single-shot randomization [46]. These short-cut methods could also benefit from using stronger twirling groups, such as single qubit or multi-qubit Cliffords instead of Pauli twirling [36]. Stronger twirls generally induce coarse-grained degeneracies in the learnable errors [36] and increase systematic uncertainty [20, 21], so less information is learned and it is learned less accurately, but such methods can hope to learn these coarse-grained error properties much more efficiently.

Some other outstanding challenges include:

- All of the above "established" methods make the standing assumption that non-Markovian errors are negligible. These effects can be important and so characterization of temporal fluctuations and drift is needed. While many of these effects show up as a deviation from an exponential decay in an RB experiment [24, 81, 116], the classification of relevant non-Markovian effects and methods for their characterization remains an important open problem.

- There is an outstanding question as to whether the above methods will remain practical in the context of logical operations on logical (error-corrected) qubits, in particular whether the standing Markovianity assumption will remain valid for such "highly-engineered" qubits and gate operations.

- Optimizing / cross-layer compilation, and compiling to the actual implemented gates vs target gates, can provide significant advantages [44, 65] and requires further exploration.

- Optimizing selection of reduced instruction sets, by balancing trade-offs between calibration costs and compilation efficiency is also an opportunity, where the analysis of these trade-offs is application-specific and the possibility of a general framework remains an open question. An example implementation is described in [65]).

B. Error Suppression Methods During Operation

This is a broad category of strategies designed to suppress or correct errors arising in the course of QPU operation. These errors can include coherent errors due to the finite precision and fluctuations/drift in the classical control fields and the decoherence errors due the environment.

The family of solutions includes passive error suppression strategies such as dynamical decoupling (DD) [114], Pauli frame randomization (PFR) [73] for Clifford circuits, and randomized compiling (RC) [115] for universal circuits.

Dynamical decoupling applies when errors are preferentially aligned along the quantization axis and requires inserting additional gates to reduce/cancel these errors by leveraging the known (directional) bias in the error model [114]. Pauli-frame randomization (PFR) and the equivalent but less well-known proposal known as PAREC [71], which both require Pauli frame tracking (PFT) [73, 117], are designed to suppress unknown (but otherwise generic) coherent errors but are limited to the restricted setting of Clifford circuits due to the exponential cost of Pauli frame tracking through universal circuits.

Because of the limitation of DD to single-axis error, and restriction of PFR to Clifford circuits, error suppression for universal circuits can be achieved via randomized compiling (RC) [115], a randomization method that leverages a locally corrected twirl and does not require Pauli frame tracking through the circuit. RC utilizes either Pauli or dihedral twirls [19], depending on the how the T-gate is implemented. As a result, RC can be applied efficiently in the more general setting of universal circuits to suppress fidelity loss due to coherent errors [53, 113, 115]. Randomized compiling also aligns the actual error model in applications, whether NISQ or logical level algorithms, with the error model that can be learned via Pauli error estimation methods discussed above [22, 115].

Randomized compiling is highly resource efficient. In terms of demands on QPU time, only 20 randomized circuits are required for significant suppression of coherent errors in many use-cases [53, 113, 115]. It should be noted that this form of error suppression method does not require additional qubits nor access to low-latency high-performance compute, as is required by quantum error correction. It also does not require the exponential overhead of implementing a family of increasingly longer depth circuits, as is required for error mitigation. Both of these issues are discussed below. However, for optimal resource-efficiency (in terms of wall-clock time) for suppression of (residual) coherent errors, RC works best by randomizing the single qubits gate in a circuit as frequently as possible. The randomization of the circuit should be achieved with zero or negligible latency, and the ideal limit is a fresh randomization with every new shot, which is already the current state of the art [46].

C.   Error Correction Methods During Operation

Reaching the very low error rates required for many applications requires the implementation of fault-tolerance-quantum error correction (FT-QEC) strategies [49, 50], where the overhead of (many) additional qubits is leveraged to deliver lower error rates at the level of logical qubits. This overhead is expected to take us to a performance regime where QPUs can deliver widespread quantum advantage. In typical implementations, FT-QEC requires encoding a small number of logical qubits into a much larger number of physical qubits, and repeated measurement of error syndromes, for example as often as once per clock cycle. With each measured syndrome, the challenge is to quickly compute and implementing the most likely recovery operation — this is a highly intensive task both in terms of repeated measurements, low-latency and high performance classical compute for the decoding of the measured syndromes — and finally implementation of the computed recovery operation in the subsequent clock cycle. The qubit overheads for the best FT-QEC schemes are daunting, and the implementation of decoding on the time-scale of the quantum gates (clock cycle) remains an open challenge in many leading hardware platforms. The performance and threshold of most FT-QEC is only well understood in the limit of stochastic error channels, such as the overly-simplistic depolarizing channel or in some cases the more general setting of Pauli error channels which can of course be realized via randomized compiling [115] as noted above and demonstrated experimentally in multiple platforms [40, 53].

Specific areas where significant advances are needed include:

- Control with very low latency i/o to the fpga/control hardware to deliver pre-computed randomized circuits, or else computing the randomizations on the fly at the fpga level [46], to tailor generic errors into stochastic Pauli errors [115] in the limit of single-shot randomization to minimize QPU wall-clock time. This is required also for Pauli error learing to predict and inform decoder performance.

- The implementation of FT-QEC requires developing new, architecture-friendly, low-overhead codes admitting fast and efficient decoders to avoid the extremely high qubit overheads demanded by, for example, the surface code. Recent progress on qLDPC codes [15] suggests more research is needed to develop good qLDPC decoders in light of some promising recent results [94, 103] and in parallel the community needs to explore the development of novel codes with desirable properties. Solutions are needed also to address the non-triviality of logical operations on logical qubits with codes such as qLDPC [55], that address the time overhead of the logical operations [120] and fault-tolerant circuits that permit reduced connectivity [106] or defects [7]. Codes should be tested not just for memory, but also for logical operations.

- Low-latency and high-performance classical compute, eg at the FPGA or ASIC level, is required to implement decoding on platform with fast gates [9, 86].

- Advancing error diagnostic methods to guide and inform code selection and decoder optimizations [22, 40, 61, 64].

- Developing new error diagnostic methods relevant to the specific constraints of modular architectures.

- Evaluating performance trade-offs and achievable physical and logical limits of error reduction through dynamical decoupling and randomized compiling

- Exploring decreased overheads in code design and decoder efficiencies that can be leveraged by qudit systems.

D.   Error Mitigation via Expanded Circuits, Post-processing and Extrapolation

In recent years there has been significant interest in error mitigation methods that require executing an expanded family of (non-equivalent) circuits and post processing [18]. It is now increasingly accepted that these techniques could enable accurate observable estimation at qubit counts exceeding brute-force classical simulation, and with circuit volumes of few thousands of two-qubit gates, enabling initial demonstrations of quantum advantage [4, 34, 127]. Furthermore, these techniques are also expected to be relevant even as error corrected processors become a reality. For example, extrapolation based methods, use circuits of increasing depth [33] or gate time [68] to artificially increase the noise, and then perform an extrapolation to the zero-noise limit to estimate the ideal output [110]. More controlled ways to perform extrapolation employ the use of a noise model. Such an approach requires measuring the error model for each cycle, eg via cycle error reconstruction, and post-processing leading to evidence of utility [72]. While error extrapolation techniques can retain a bias, given an accurate noise model, it is possible alternatively, to obtain an unbiased estimate for observables using Probabilistic Error Cancellation [112]. Generally, these approaches require exponential sampling overhead on the QPU, but in the limit of low error rates, the base of this exponential is very close to 1 and one can obtain unbiased observable estimates on circuits with gate counts (5000-10000) that could be challenging for classical simulation [34, 38].

Some key challenges include:

- While cycle benchmarking provides an efficient method to bound the overhead cost for some error mitigation methods, limitations to the effectiveness of cycle benchmarking for this task include limitations under high measurement error rates, which needs to be overcome.

- Recent error mitigation methods, such as noiseless output extrapolation, suggest that lower overhead post-processing methods of error mitigation may be achievable [41].

- While error mitigation can lower the impact of the infidelity of the physical qubits, enabling more powerful computations in the near-term, the synergies between error mitigation and quantum error correction require further exploration.

- Heuristic error mitigation methods can be useful but typically do not provide rigorous bounds on the mitigated results. The use of methods with tight, rigorous bounds is particularly crucial, for placing trust in error mitigated quantum computation, at scales where a classical solution does not exist [77].

E.   Algorithm Implementation

At the most basic level, classical data has to be uploaded to the QPU and outputs have to retrieved and analyzed. This already imposes a constraint on any algorithms where this basic i/o can require a significant, if not exponential cost.

Many quantum algorithms require leveraging complementary compute requirements, for example, quantum-classical hybrid-algorithms. These algorithms often require low latency high-performance compute in parallel with the implementation of the quantum circuits.

With many recent advances both in machine learning and in different hardware architectures (eg. graphical and tensor processing units), some QPU-related tasks may be well aligned with specific classical tools, and may also form the basis of future quantum-classical co-design of such data interfaces. Research into the utility of quantum-classical hybrid algorithms is ongoing [102, 122].

F.   Output Validation

For many quantum applications and use-cases where an exponential advantage is expected, for example, quantum dynamical simulation, quantum chemistry, drug discovery and so on, the correctness of the (candidate) quantum solution, obtained on imperfect and noisy quantum hardware, cannot be verified classically. In particular, the exponentially large number of unquantified residual physical errors create a problem where the precision or accuracy of the quantum solutions are unknown and can not be efficiently measured or efficiently computed.

While it is well understood that this creates a validation problem for NISQ implementations of algorithms, because the presence of residual physical level errors lead to incorrect solutions, the persistence of this problem at the logical level is less well appreciated. It is important to recognize that fault-tolerant quantum computation is not actually "tolerant of all faults" and will always suffer from the same challenge. For example, the distance of the code guarantees only that a subset of (low-weight) errors are detectable and correctable, however, it is still possible to have larger weight errors go undetected or result in decoding errors (such as predicting the wrong recovery operation).

Thus, it is important to develop highly-scalable, resource-efficient verification and validation methods to characterize the effective error rates under all of the layers/cycles of universal circuit for large-scale processors, both for current NISQ processors and in the long-run of fault-tolerant architectures. This in turn provides a bound on the output accuracy under the entire algorithm when executed on given hardware. A promising solution in this direction consists in leveraging cycle benchmarking [38] to measure the cycle infidelities for each of the distinct/layers of a quantum algorithm, then, thanks to the recent fidelity bound on compositions of cycles [20], this enables a rigorous and accurate 'circuit benchmarking' [37] prediction of the circuit fidelity, even for universal circuits, and this circuit fidelity in turn bounds the total variation distance on the output. This approach assumes that the errors are stochastic, and this assumption can easily be enforced by implementing the circuit via randomized compiling.

Going forward, some specific tasks and questions include:

- Development of scalable verification and validation methods that can be applied at the logical level to herald or bound logical faults occurring due to code-distance limitations and decoding failures, such as the circuit benchmarking method. Determine how to related these bounds on fidelity and total variation distance to the observables of interest for quantum algorithms.

- Can ideas from machine learning proved improved ways to learn noise/error models to ease scale-up?

VII.   CONCLUDING REMARKS

Quantum information science and technology is a field that continues to grow at a rapid pace, and holds the promise of many new revolutionary technologies. To achieve the full potential of fault-tolerant quantum error corrected quantum computing, it will be vital to continue to improve the quality of individual qubits, produce

Research Focus Area	Desired Outcomes	Enabling Near-Term Research Directions
Modular Quantum Processors	Distribute computation to increase fabrication yield & to reduce classical control stack complexity	Quantum coherent transduction between microwave and itinerant optical photons
		Distributed quantum error correction codes
		On-chip ineterconnects and multi-chip modules
		Interconnected cryopackages
		Remote entanglement
Cryogenic Systems	Extend cooling capacity of cryogenic sysems to accommodate large qubit counts needed for fault-tolerant operation	High-density components to reduce space, cost & thermal load
		Interconnected fridge modules capable of asynchronous operation
		Standardized wiring interfaces (plate spacings & port form factors)
		Hybrid refrigeration schemes to provide additional cooling power for cryogenic control circuitry, and to soften wall power scaling of conventional pulse tube coolers
		Reduce 3He need per qubit / increase 3He production
Cryogenic Electronics	Develop robust cryogenic electronics and interconnects	Testbed facilities for economical cryogenic component testing (eg. wiring, shielding, passive and active components, cryopackages, etc.)
		Perfomance standards, traceability, and certification including microwave characteristics, failure-in-time rates, materials characteristics, and thermal cycle reliability.
		Reduced volume/weight of passive components requriing permanent magnets
		Multi-user enabling foundries, multiplexed and densified cryogenic wiring (eg. flex) with standardized physical characteristics
		CMOS and superconducting control electronics with standardized interface protocols
		Fiber-based microwave signal transmission
Room Temperature Control Electronics	Develop resoruce-efficient, robust, and scalable solutions for RF pulse generation	Detailed failure rates needed for computing at scale
		Integrated and customized controls such as ASIC-bsaed controls for >> 1000 qubits
		Integrated FPGA controls to form a customizable interface for ASIC-based architectures & critical computation tasks
Classical High Performace Computing Resrouces	Develop resource-efficient solutions for low-latency classical compute tasks for QPU operation	Dynamic pulse-deisgn and recurring calibration employing error diagnostics to minimize cross-talk, compensate for drift, optmize fidelities, etc.
		Error minimization and mitigation using quantum algorithms supported by conventional data processing
		Quantum error correction with new architecture-friendly, low-overhead codes and custom FGPA/ASIC classical compute for decoding
		Algorithm implementation leveraging quantum/classical co-design for computational advantage
		Resource-efficient quantum verification & validation methods to characterize effective error rates under full circuits

FIG. 4. Summary of major recommendations

quantum processors capable of generating long-lived entanglement, and develop robust, scalable strategies to address a QPU and interface it with a classical user. In this article, we have enumerated a list of several critical areas where advancements in the last category are needed for sustained future progress.

We note that this progression is integrally connected with the establishment of a quantum ecosystem where many players in the commercial and academic domains can jointly develop quantum-tailored engineering solutions that require both fundamental science advances and industrial precision. At the heart of this environment is a quantum-literate workforce, and its cultivation cannot be understated. We envision this document as the first installment of a technology idea map, assembled by a collection of authors from across the ecosystem, for superconducting qubit technologies that is intended to help focus emerging technology partnerships. It will no doubt rapidly evolve with new developments in the field and should form the basis of a future living document.

A. Acknowledgements

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