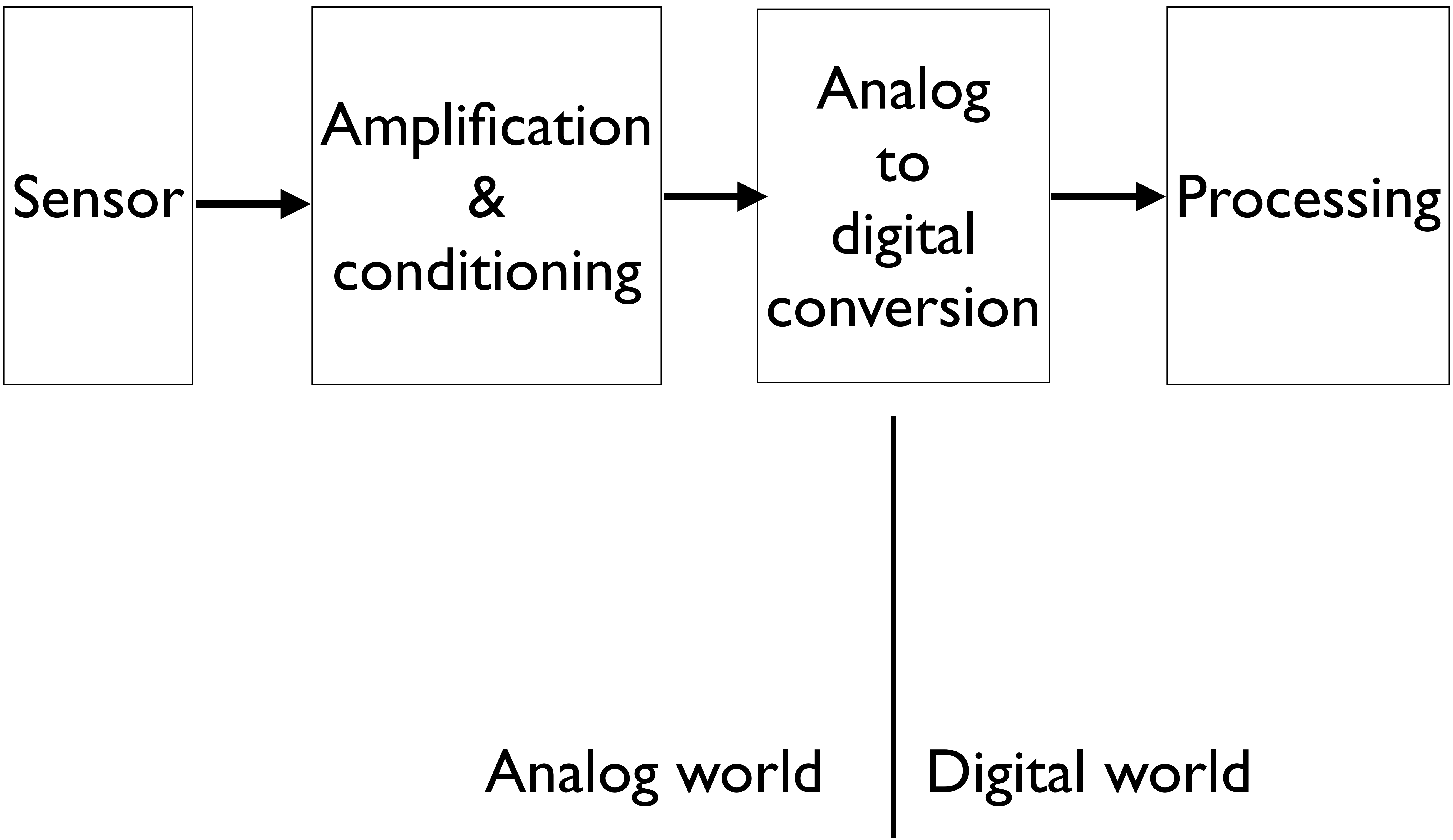
AE3B38SME

Lecture 1

-Sampling and quantization
-AD converters
-Digital oscilloscope

The measurement chain



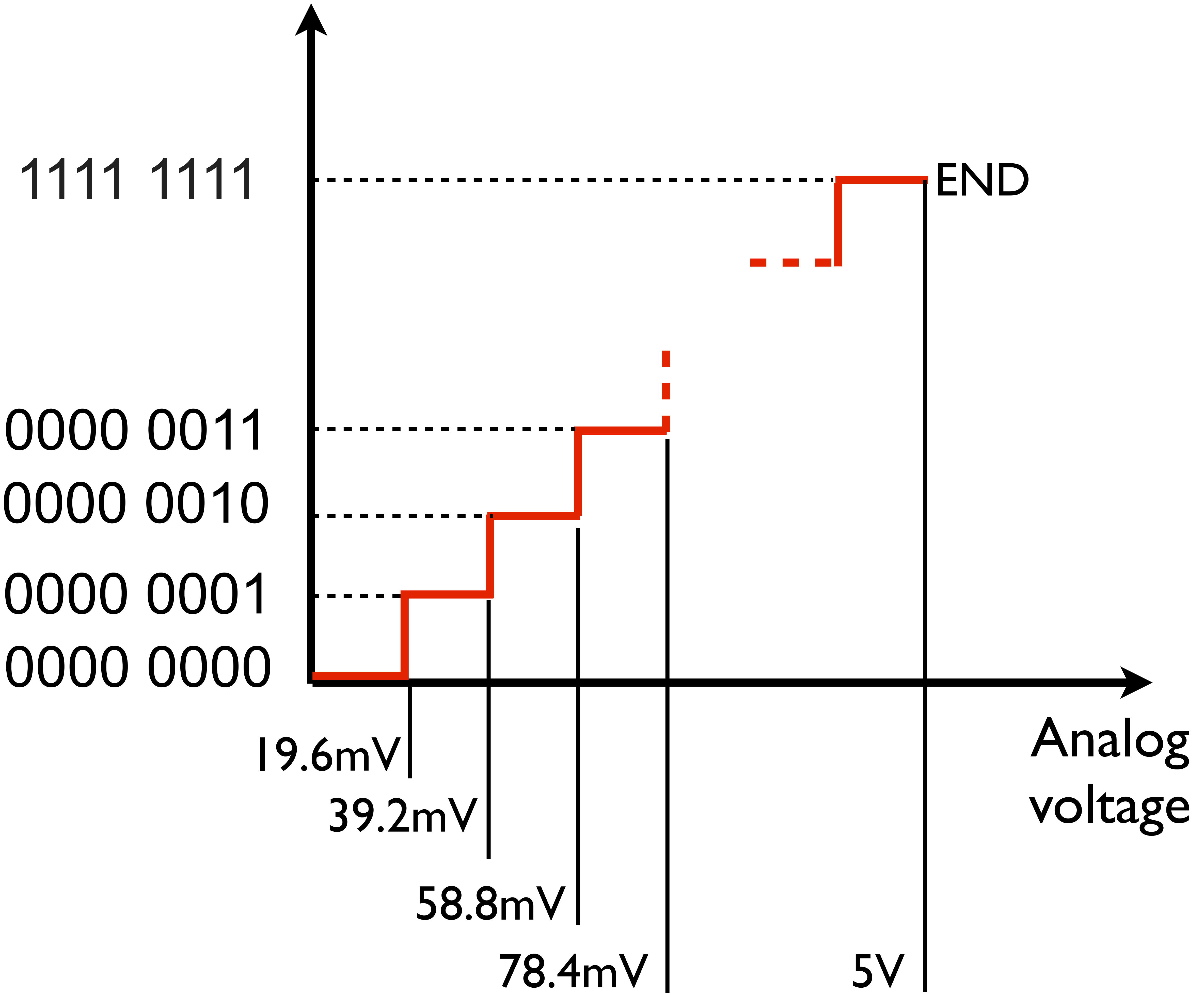
What's the difference between analog and digital data?

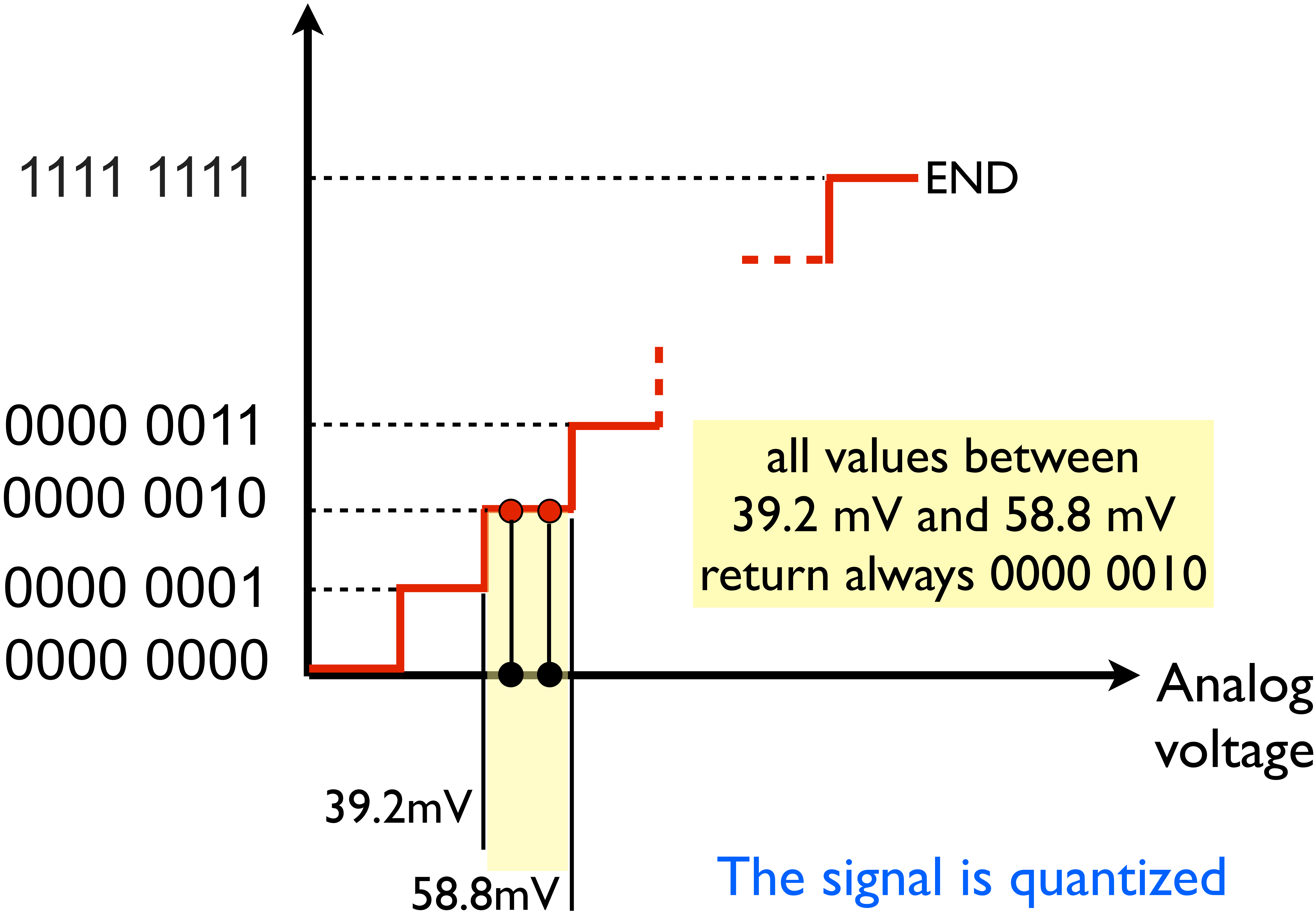
1 - Amplitude

Analog voltage s		Digital code c	
0 V	$\longrightarrow$	0	0000 000
⋮		⋮	
5 V	$\longrightarrow$	255	1111 1111

ANALOG TO DIGITAL CONVERSION

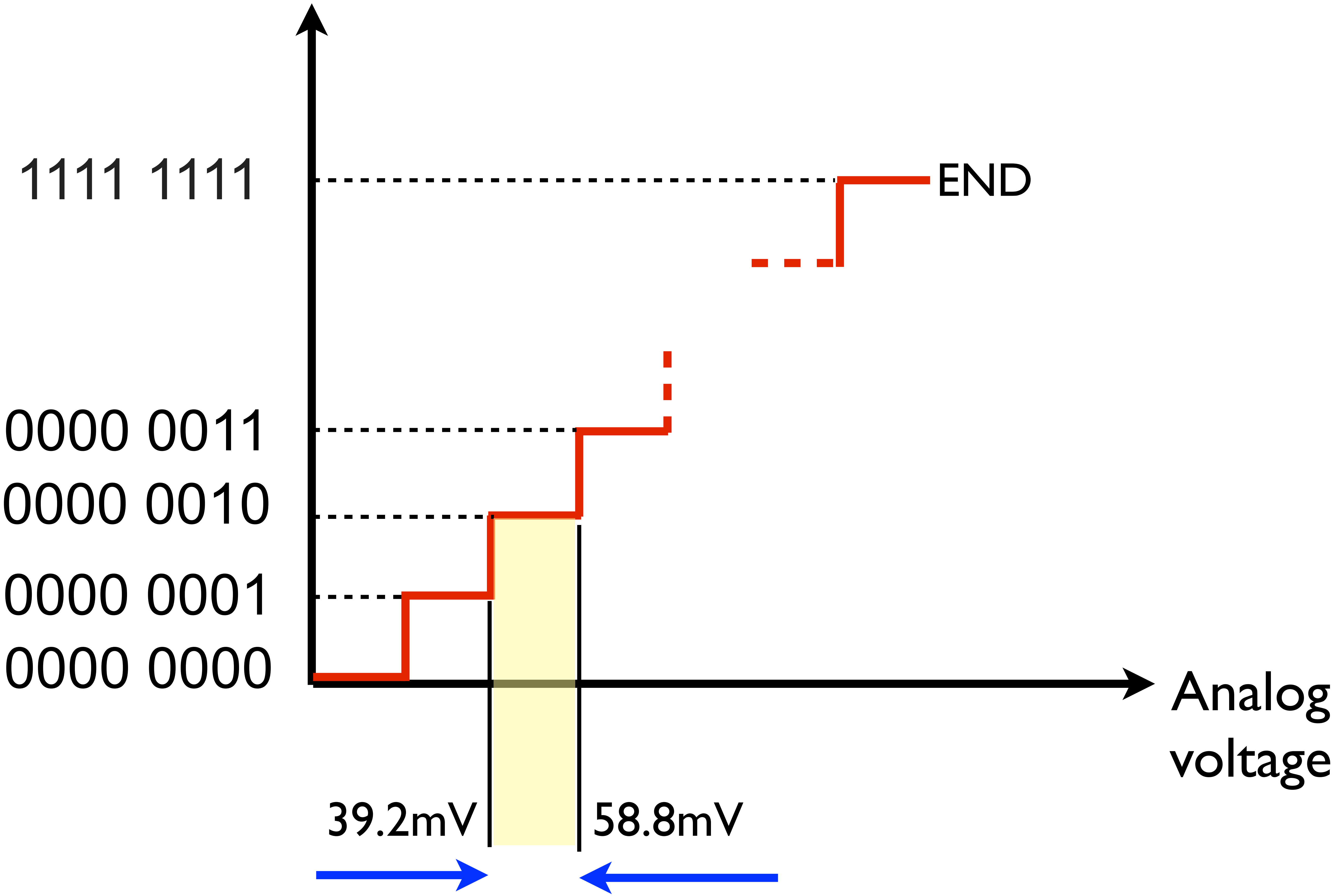
Analog voltage		Digital code	
s		*c*	
0 V	→	0	0000 0000
0.84V	→	43	0010 1011
5 V	→	255	1111 1111


1111 1111
END
0000 0011
0000 0010
0000 0001
0000 0000
19.6mV
39.2mV
58.8mV
78.4mV
5V
Analog voltage

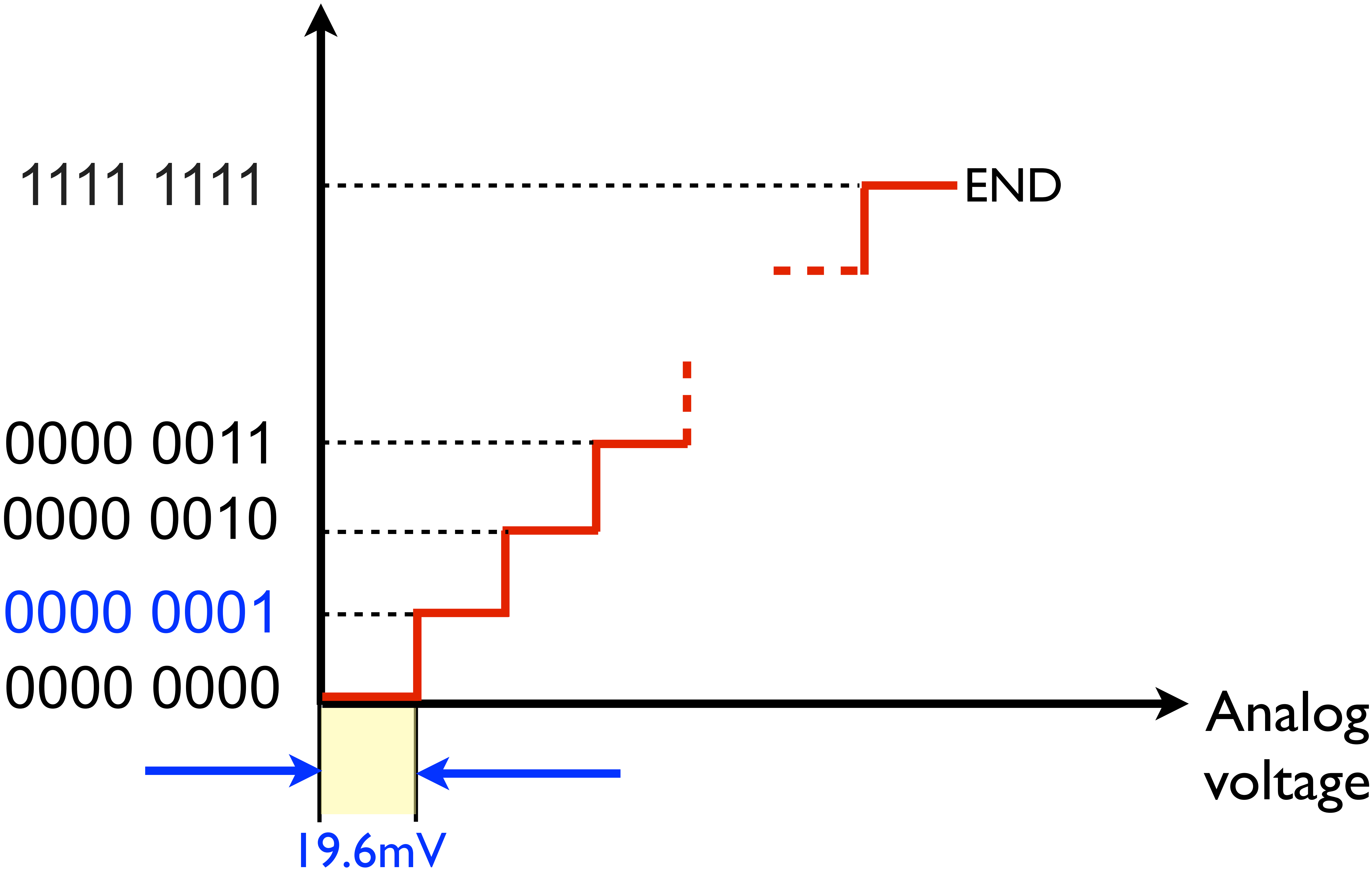


all values between
39.2 mV and 58.8 mV
return always 0000 0010

The signal is quantized



minimum voltage we can discriminate 58.8-39.2= 19.6 mV



LSB = least significant bit

from http://www.maximintegrated.com

Top ⌃ Total Parts: 452	Resolution (bits) ADC	Input Chan.	Conv. Rate (ksps) max	Data Bus	Diff/S.E. Input	Internal V_{REF} (V) nominal	External V_{REF} (V) min	External V_{REF} (V) max
MAX11166 NEW! 16-Bit 500ksps ±5V SAR ADC with Internal/External Reference in 3mm x 3mm Package	16	1	500	SPI	Both	4.096	2.5	5
MAX11167 NEW! 16-Bit 250ksps ±5V SAR ADC with Internal/External Reference in 3mm x 3mm Package	16	1	250	SPI	Both	4.096	2.5	5
MAX11120 1Msps 4 channel 8 bit Analog-to-Digital Converter with SampleSet	8	4	1000	SPI	Both	-	1	3.6
MAX11121 1Msps 4 channel 10 bit Analog-to-Digital Converter with SampleSet	10	4	1000	SPI	Both	-	1	3.6
MAX11122 1Msps 4 channel 12bit Analog-to-Digital Converter with SampleSet	12	4	1000	SPI	Both	-	1	3.6
MAX11123 1Msps 8 channel 8 bit Analog-to-Digital Converter with SampleSet	8	8	1000	SPI	Both	-	1	3.6

number of bits (resolution)

full scale voltage Vfs (= V_{REF})

0000 0000 0000
⋮
1111 1111 1111

from 0 to 4095 = 2^{12}-1

0000 0000
⋮
1111 1111

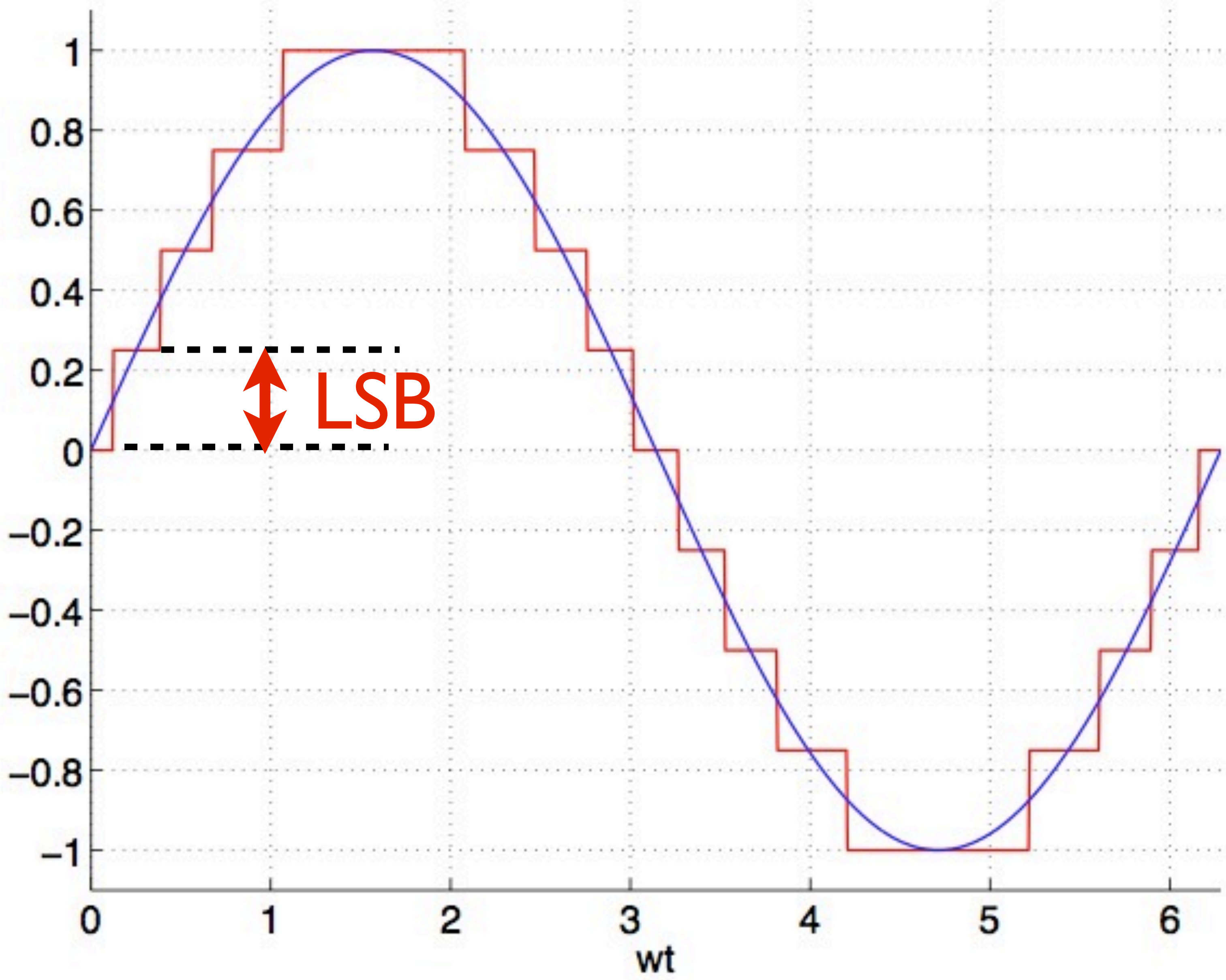
from 0 to 255 = 2^{8}-1

n = number of bits

V_{fs} = full scale voltage

$$LSB = \frac{V_{fs}}{2^n}$$

How does LSB affect the digital signal?



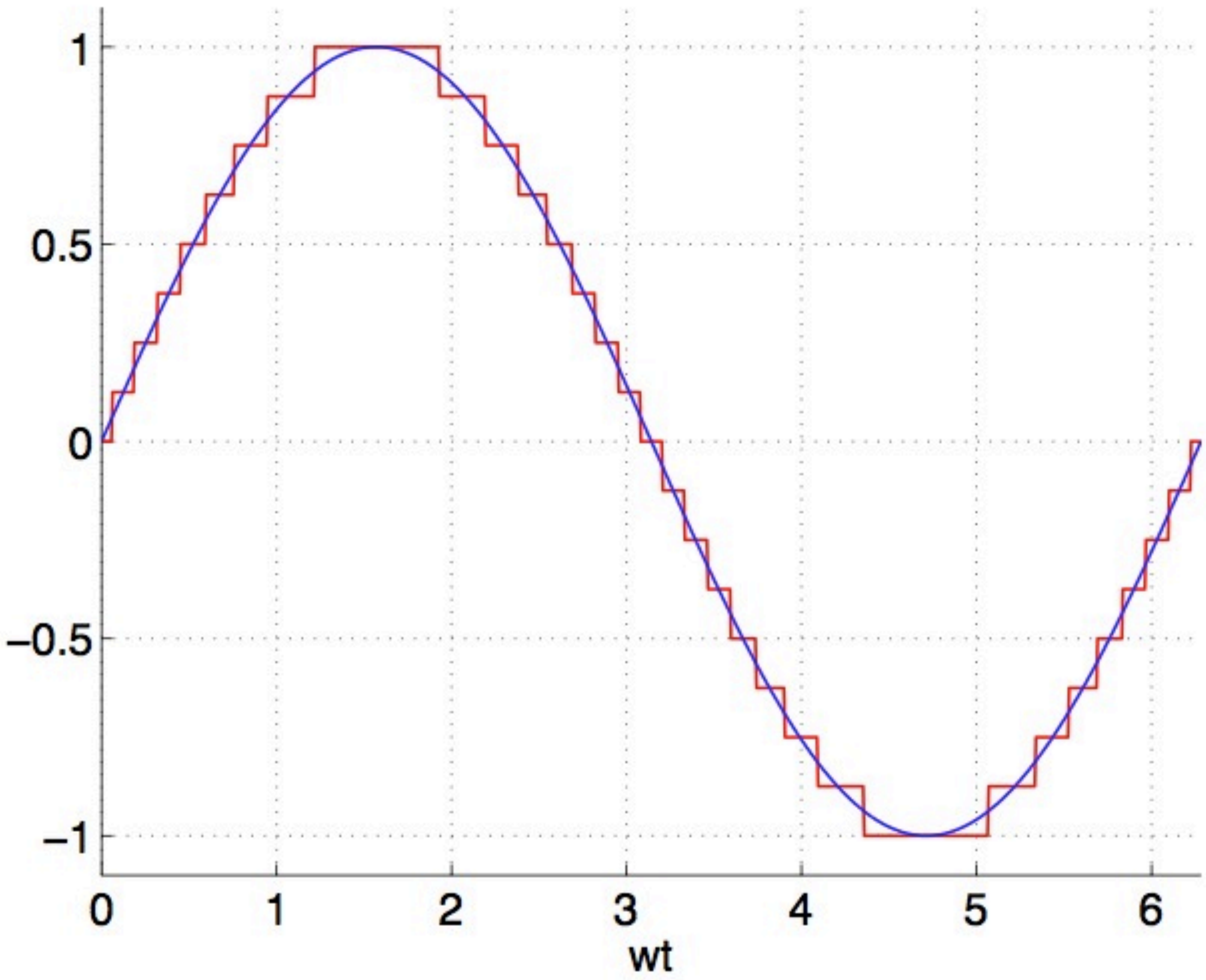
3 bits ADC

$2^3=8$

Maximum voltage range 2V

LSB = 2V/8 = 0.25 V

How does LSB affect the digital signal?

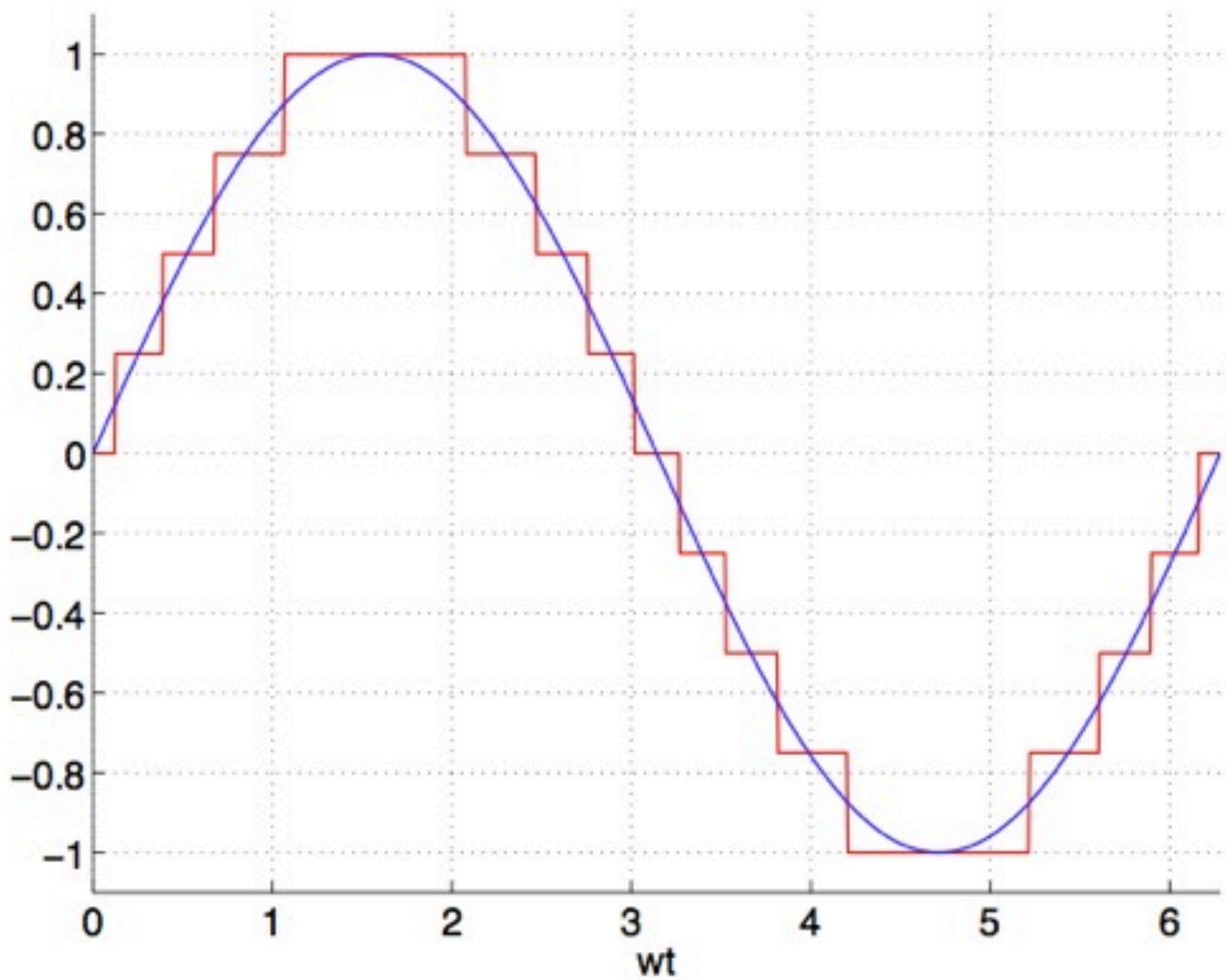


4 bits ADC

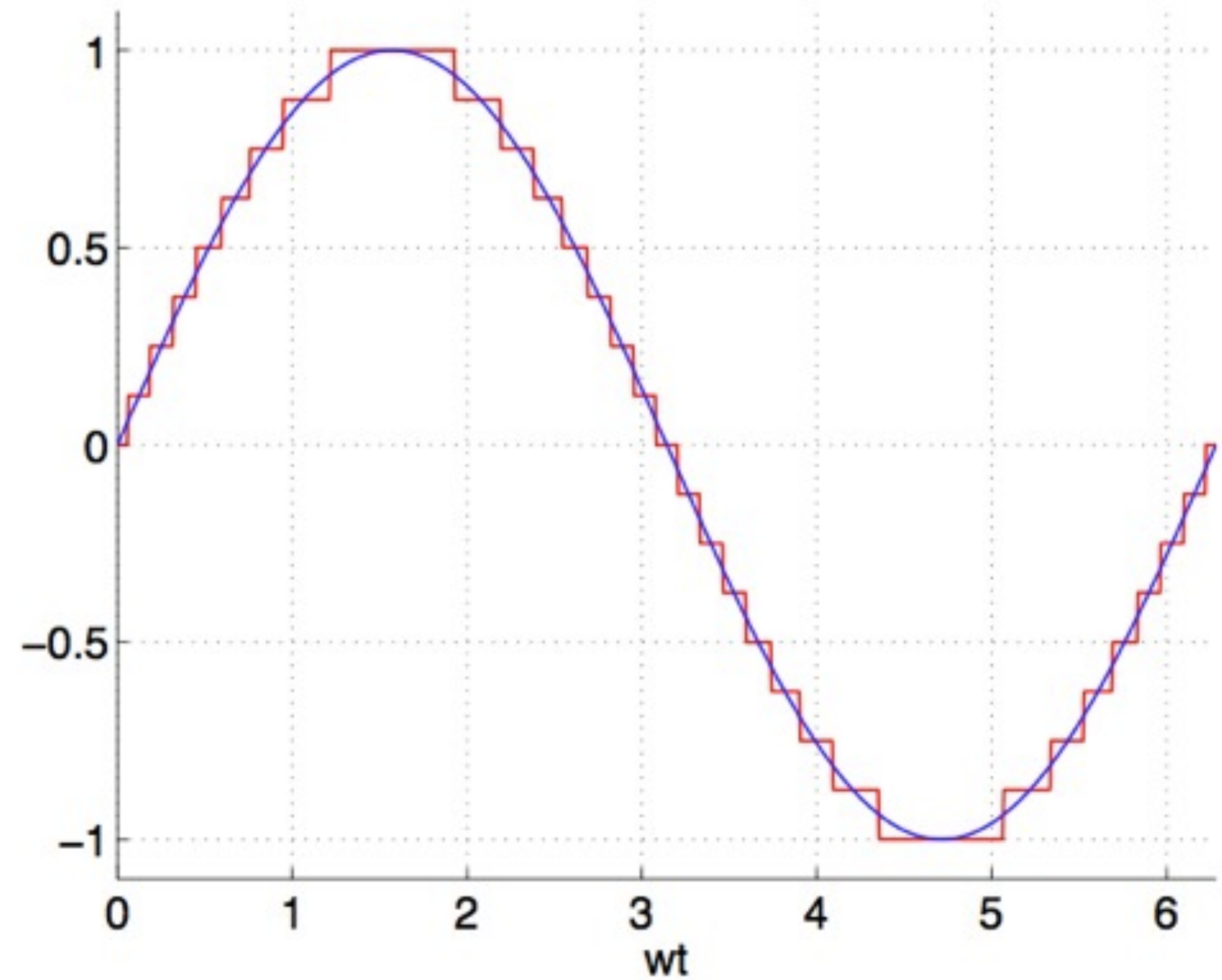
$2^4=16$

LSB = 2V/16 = 0.125 V

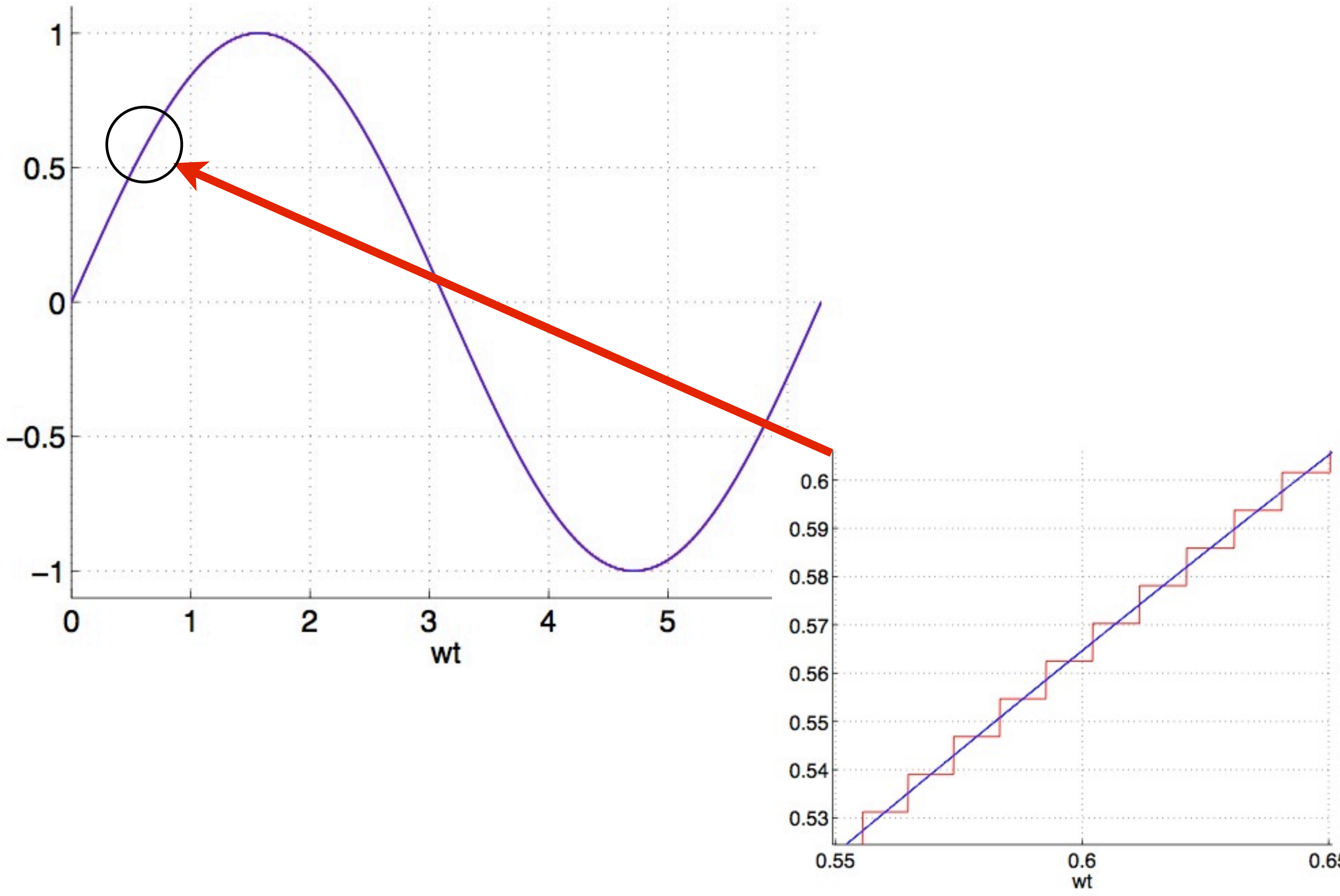
3 bits ADC



4 bits ADC

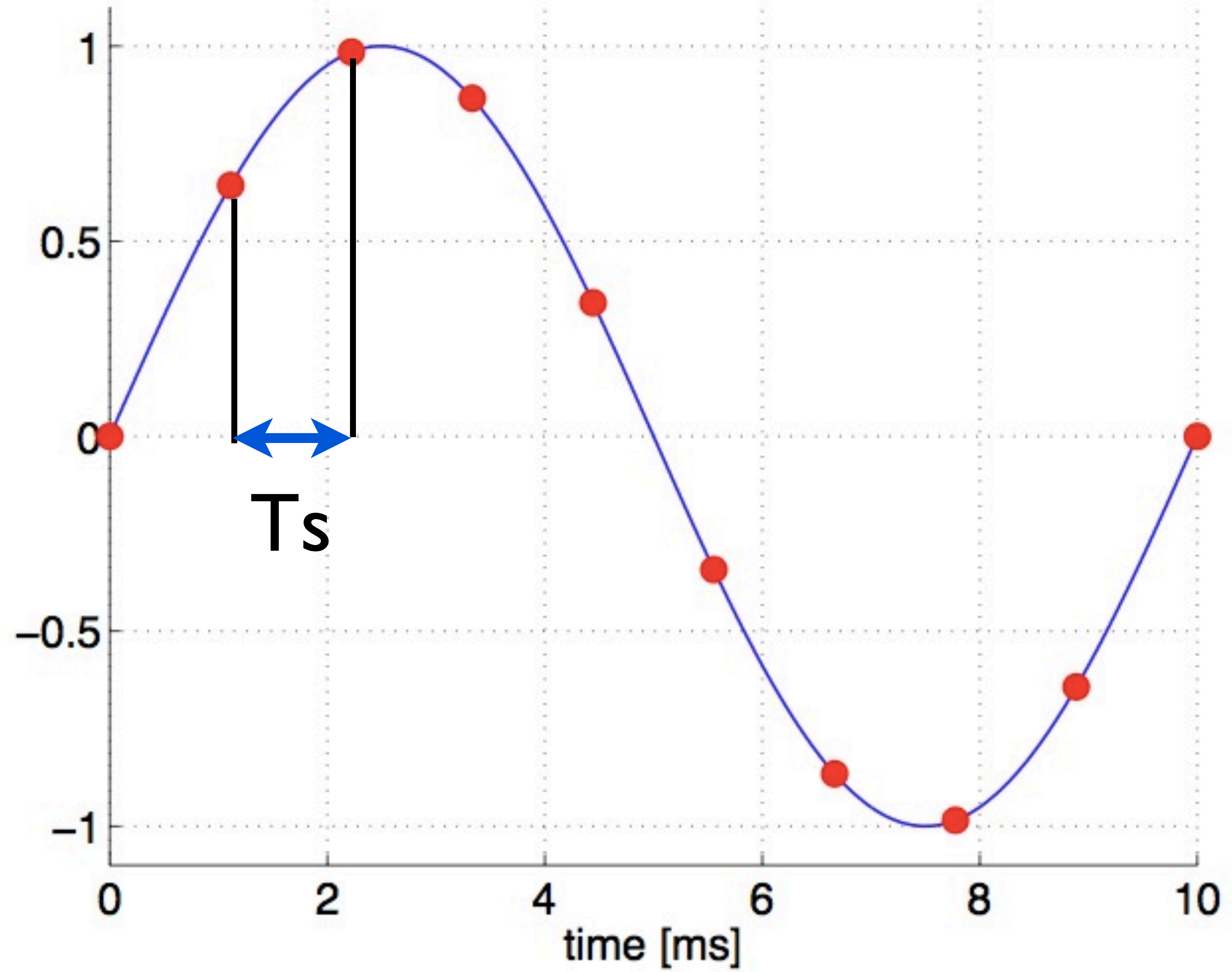


8 bits ADC



What's the difference between analog and digital data?

1 - Amplitude
2 - Time



Quantization on time

DEFINITIONS

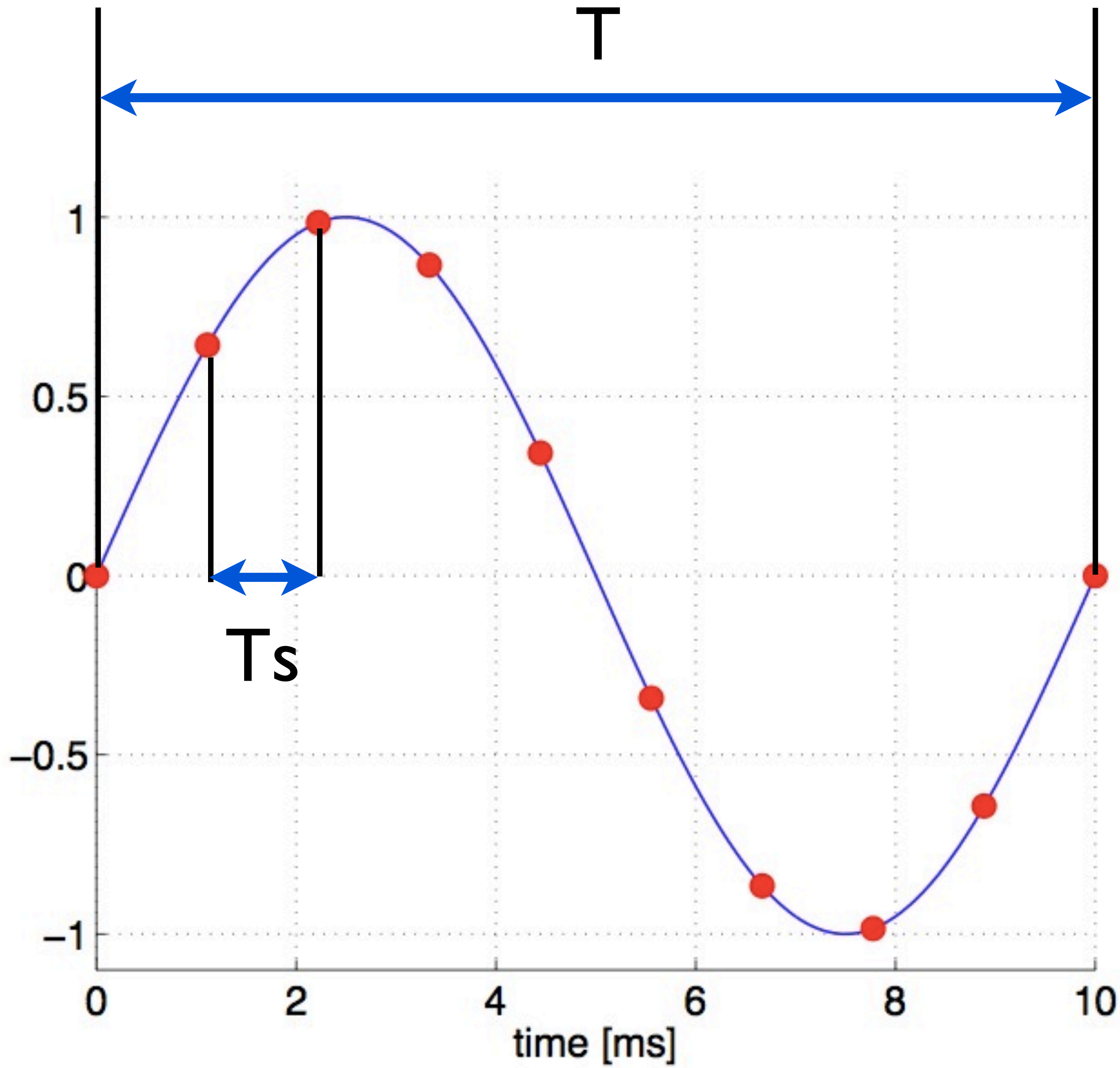
T= 10 ms
period of the signal

f=100 Hz
frequency of the signal

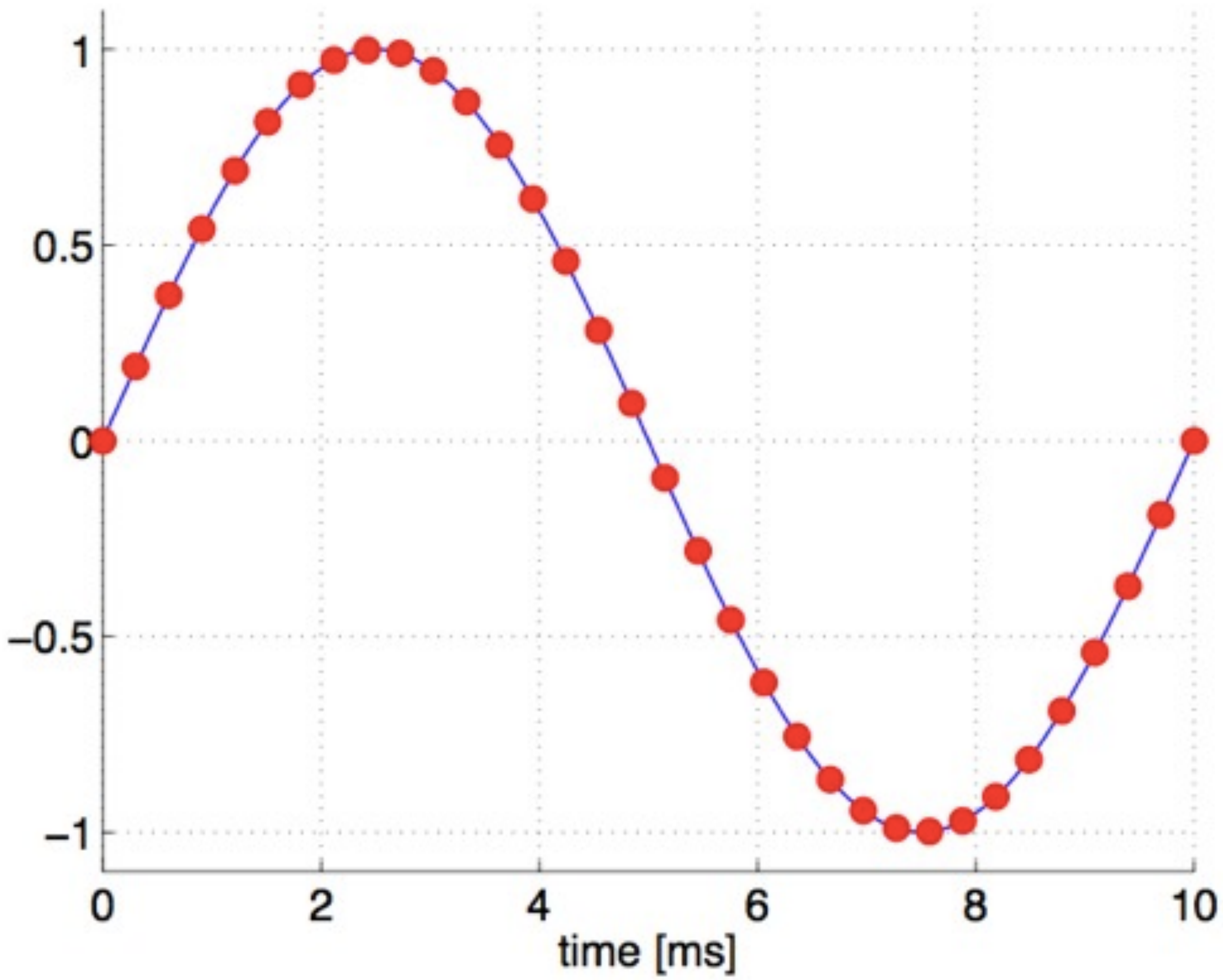
n= 9
number of samples per period

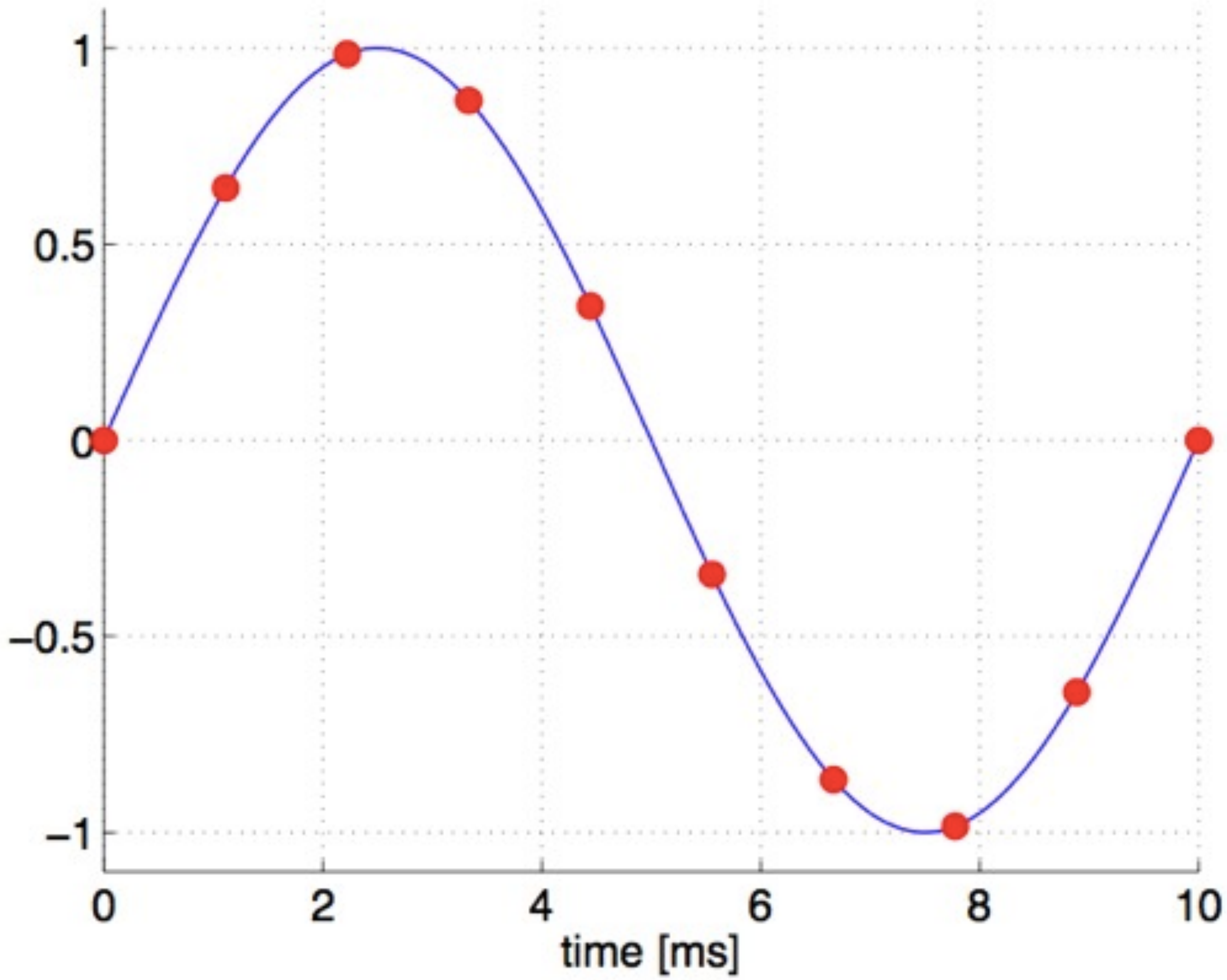
Ts = T / n = 10 ms / 9
sampling time

fs =1/Ts
samplig frequency



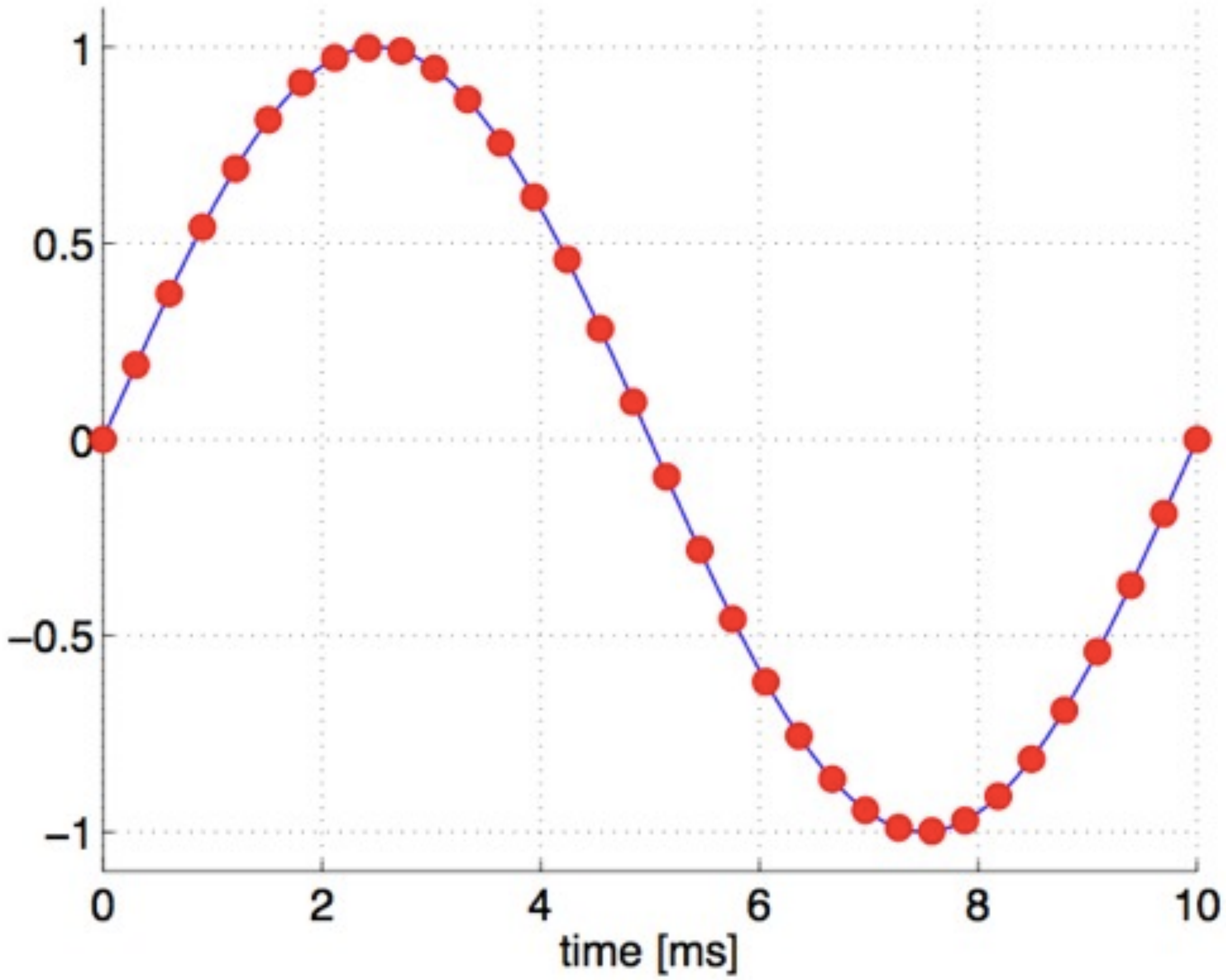
Which is better?



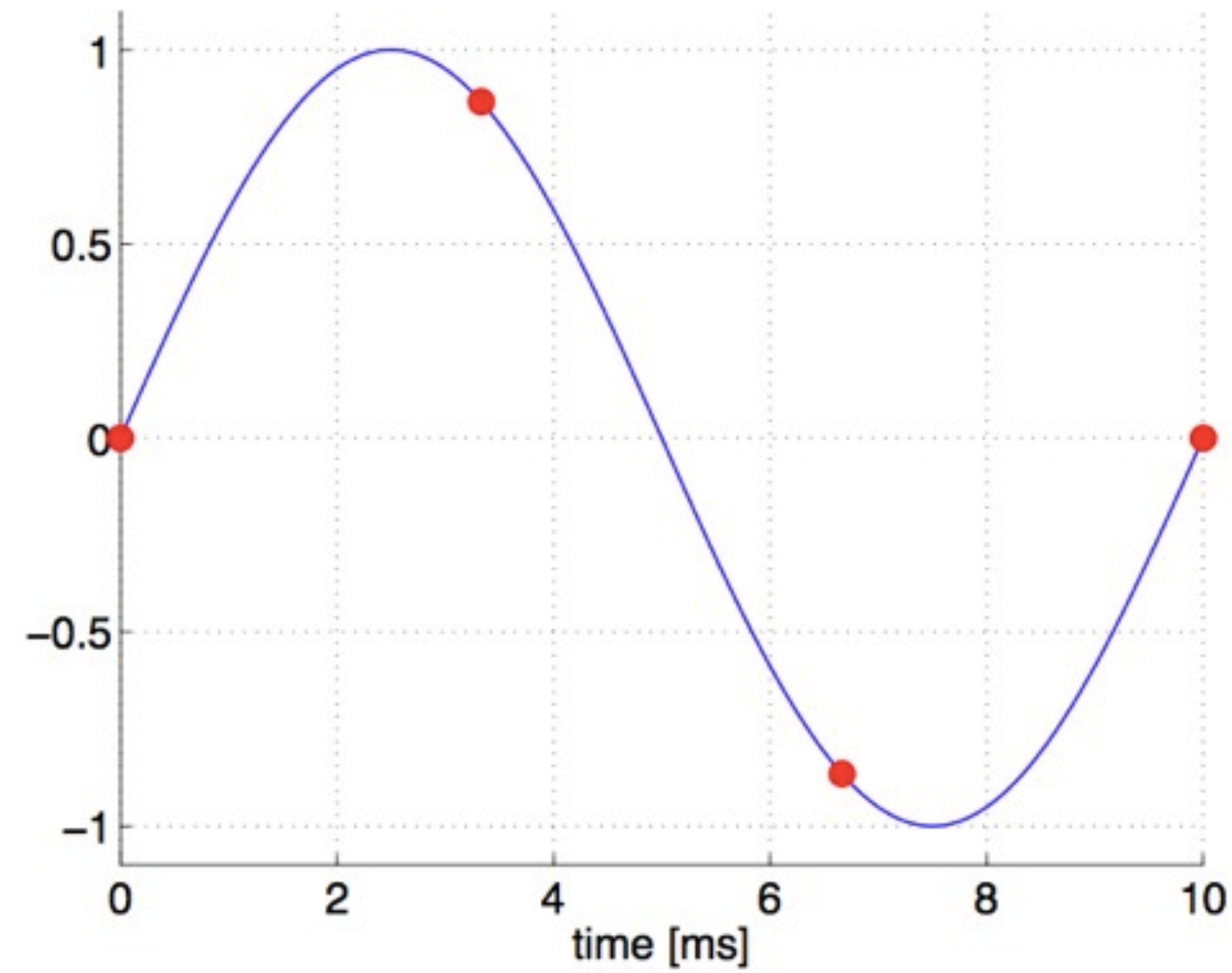


n=34

n=10



n=33



n=3

In fact, 3 points are enough...

$$s = A\sin(\omega t + \varphi) + k$$

3 unknowns

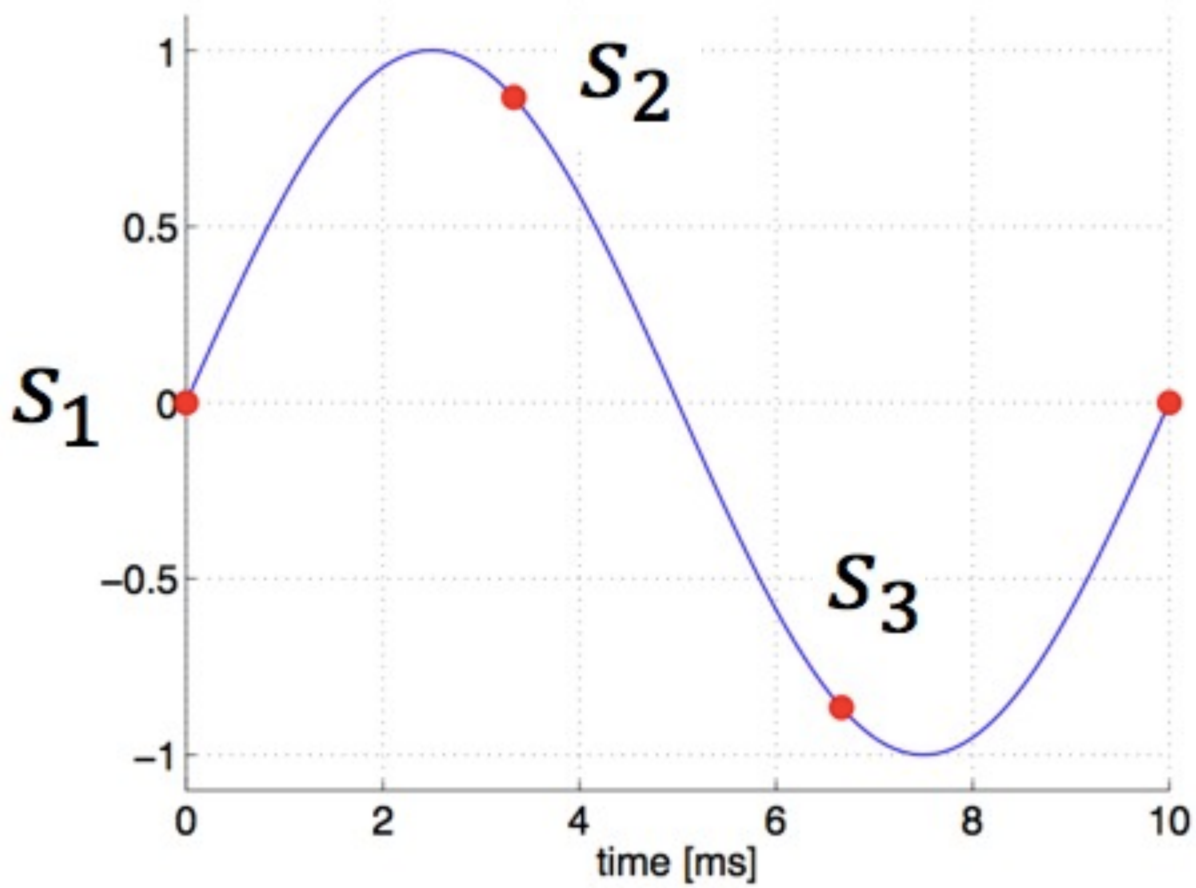
- A: amplitude
- φ: phase
- k: offset

3 equations

$$s_1 = s(t_1) = A\sin(\omega t_1 + \varphi) + k$$

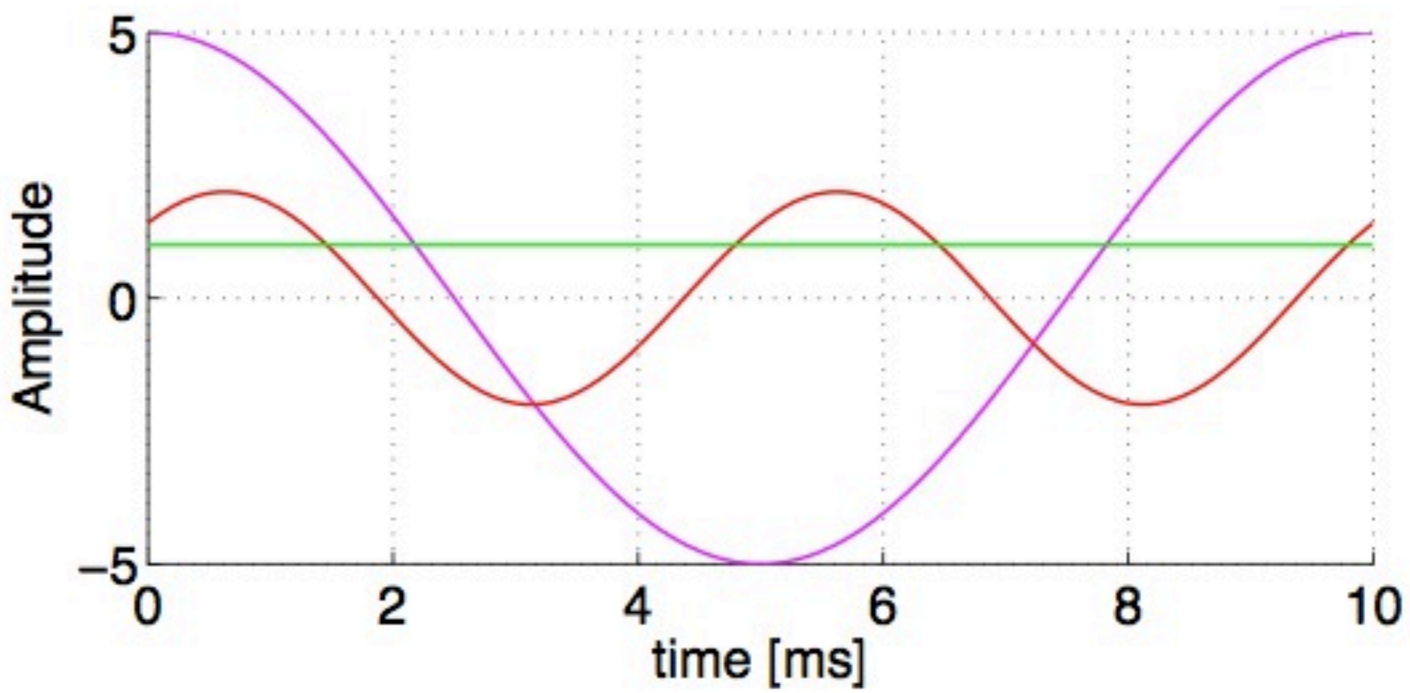
$$s_2 = s(t_2) = A\sin(\omega t_2 + \varphi) + k$$

$$s_3 = s(t_3) = A\sin(\omega t_3 + \varphi) + k$$



What if we have multiple harmonics?

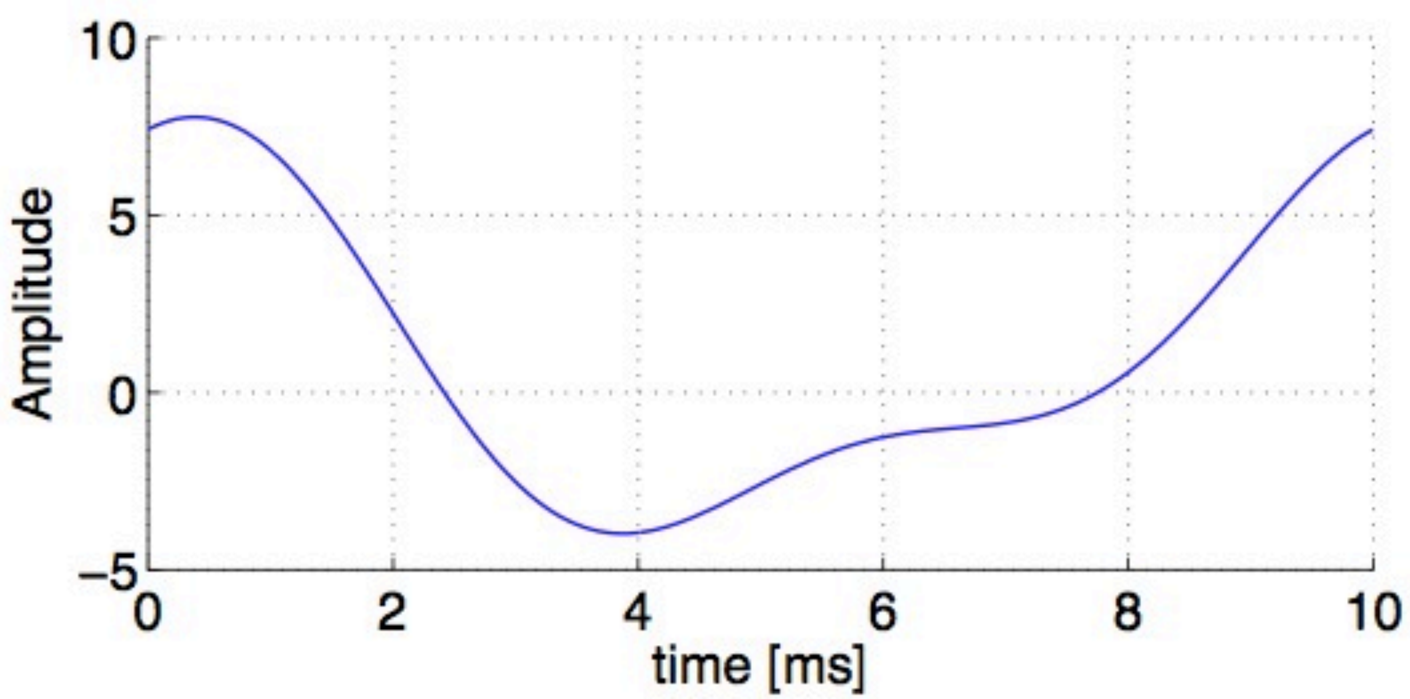
$$s = 5\cos(1\omega t + 0) + 2\cos\left(2\omega t - \frac{\pi}{2}\right) + 1$$



first harmonic

second harmonic

dc value



total

What if we have multiple harmonics?

$$s = 5\cos(1\omega t + 0) + 2\cos\left(2\omega t - \frac{\pi}{2}\right) + 1$$

$$s = A_1 \cos(1\omega t + \varphi_1) + A_2 \cos(2\omega t + \varphi_2) + k$$

dc value: k

1^{st} harmonic: A_1 φ_1

2^{nd} harmonic: A_2 φ_2

....

N^{th} harmonic: A_N φ_N

If the signal has
N harmonics
we need

n=2N+1 samples

If the signal has N harmonics we need

$n=2N+1$ samples per period T

Sampling period: $T_s = T/(2N+1)$

Sampling frequency: $f_s = 1/T_s = (2N+1)/T$

but $1/T = f$ frequency of the signal

so

$$f_s = (2N+1)\,f$$

If the signal has N harmonics we need

n=2N+1 samples per period T

$$fs = (2N+1)\, f$$

fs = 2N f is NOT enough
because we would get 2N sample, and we need 2N+1

Therefore

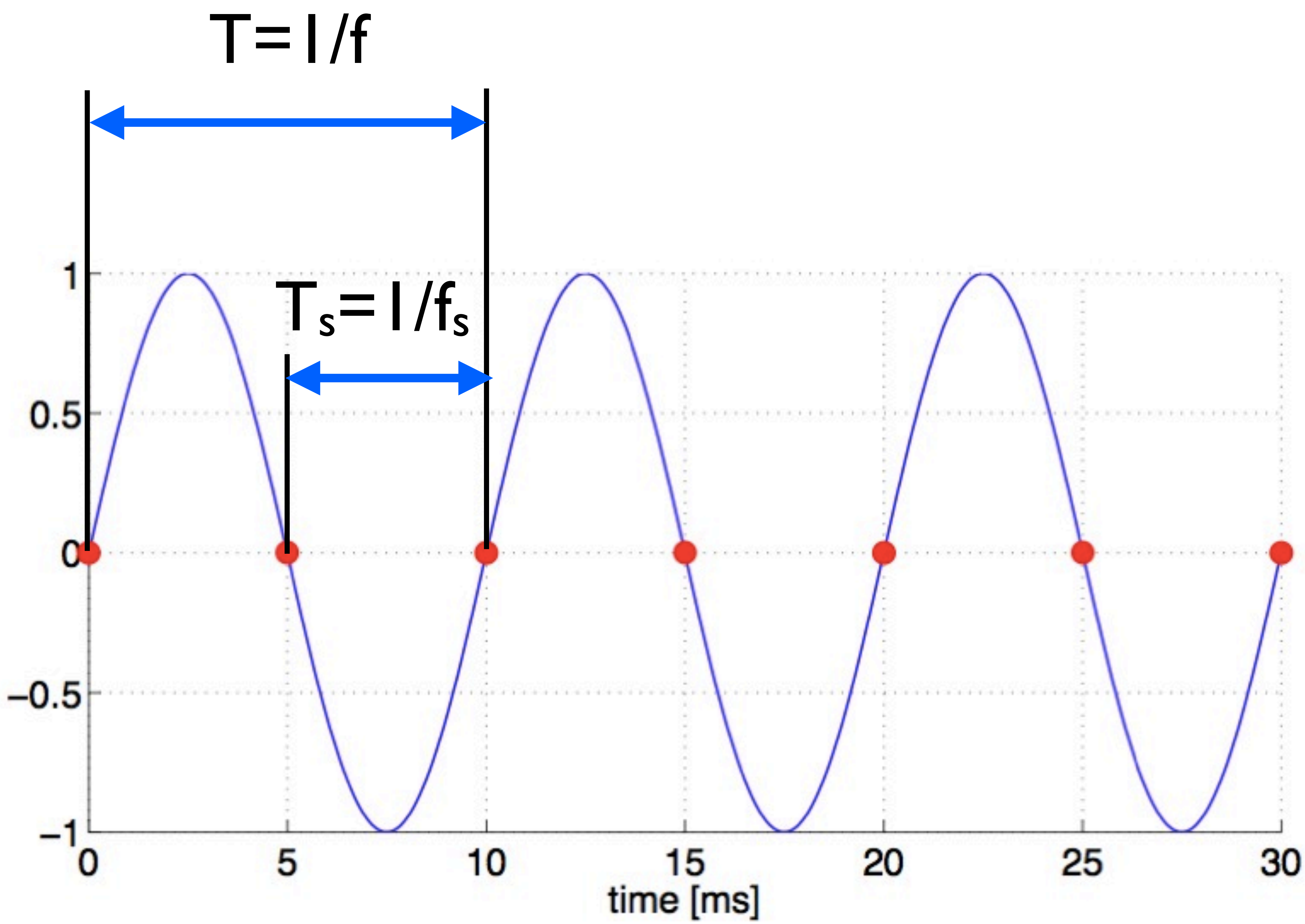
$$fs > 2N\, f$$

that is

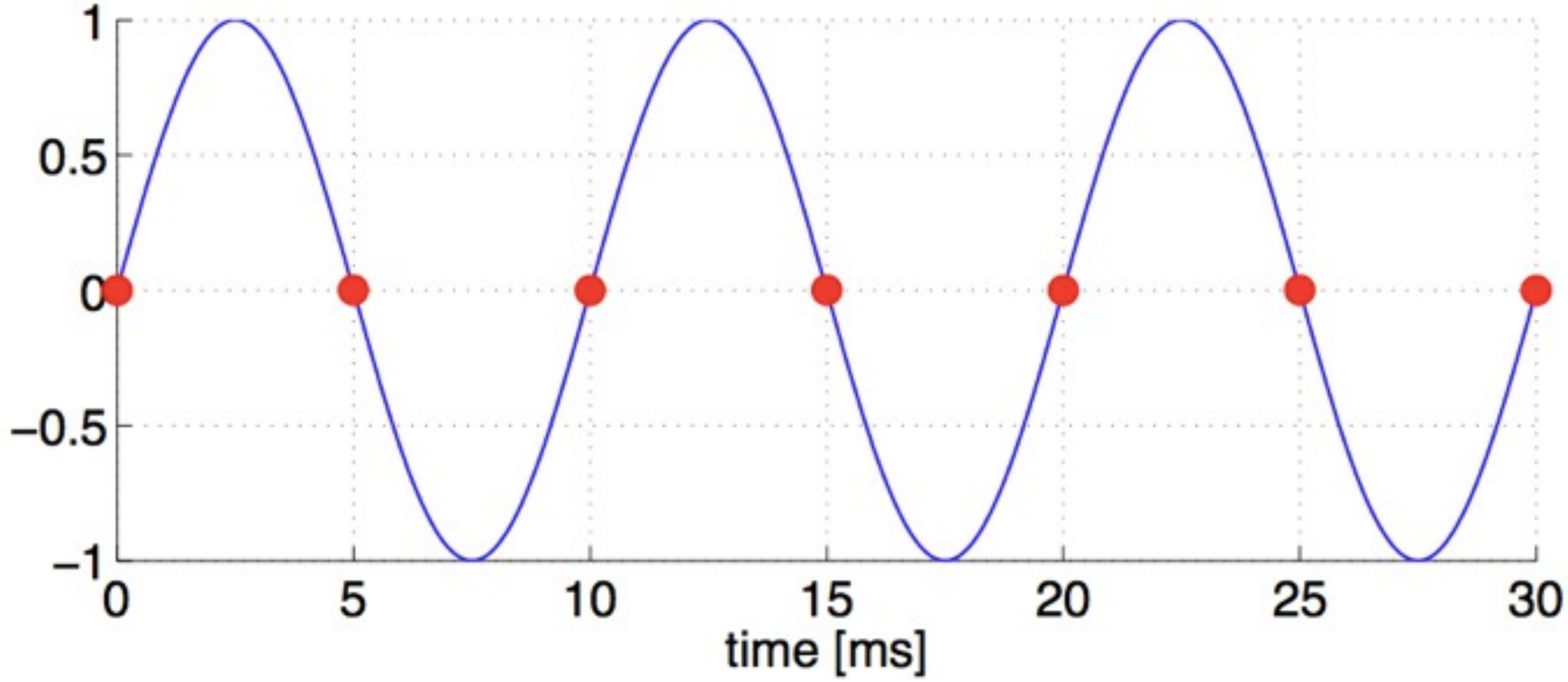
$$fs > 2\, f_N$$

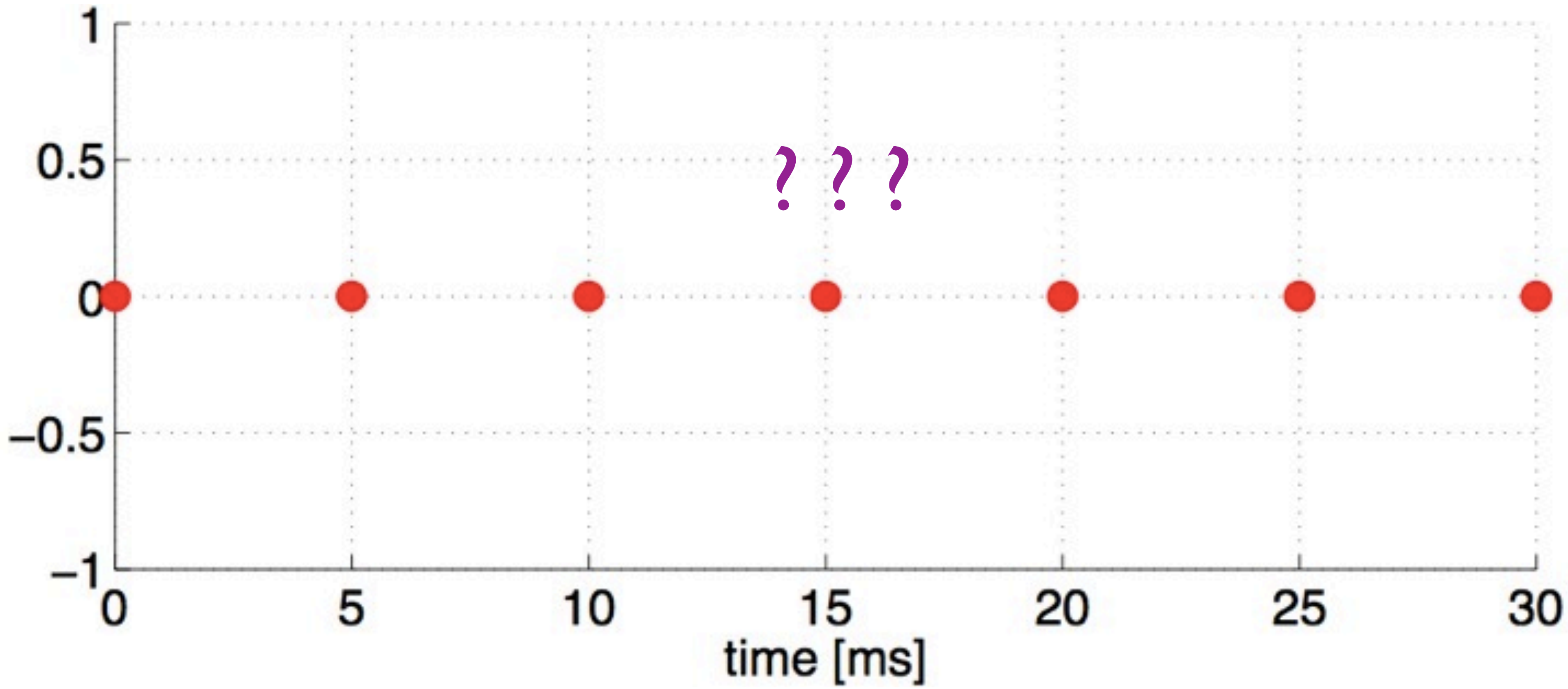
$f_N = N f$ is the maximum harmonic in the signal

What happens if $f_s=2f$

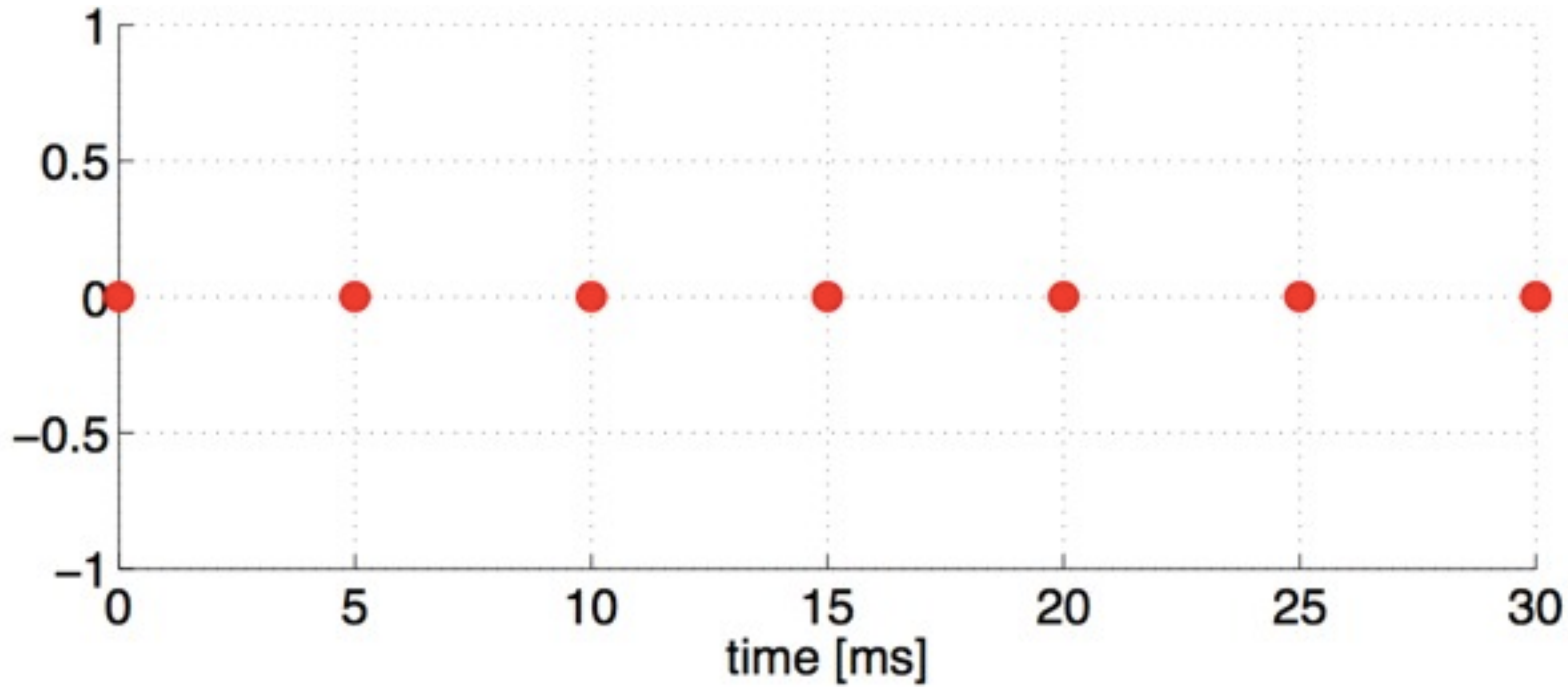


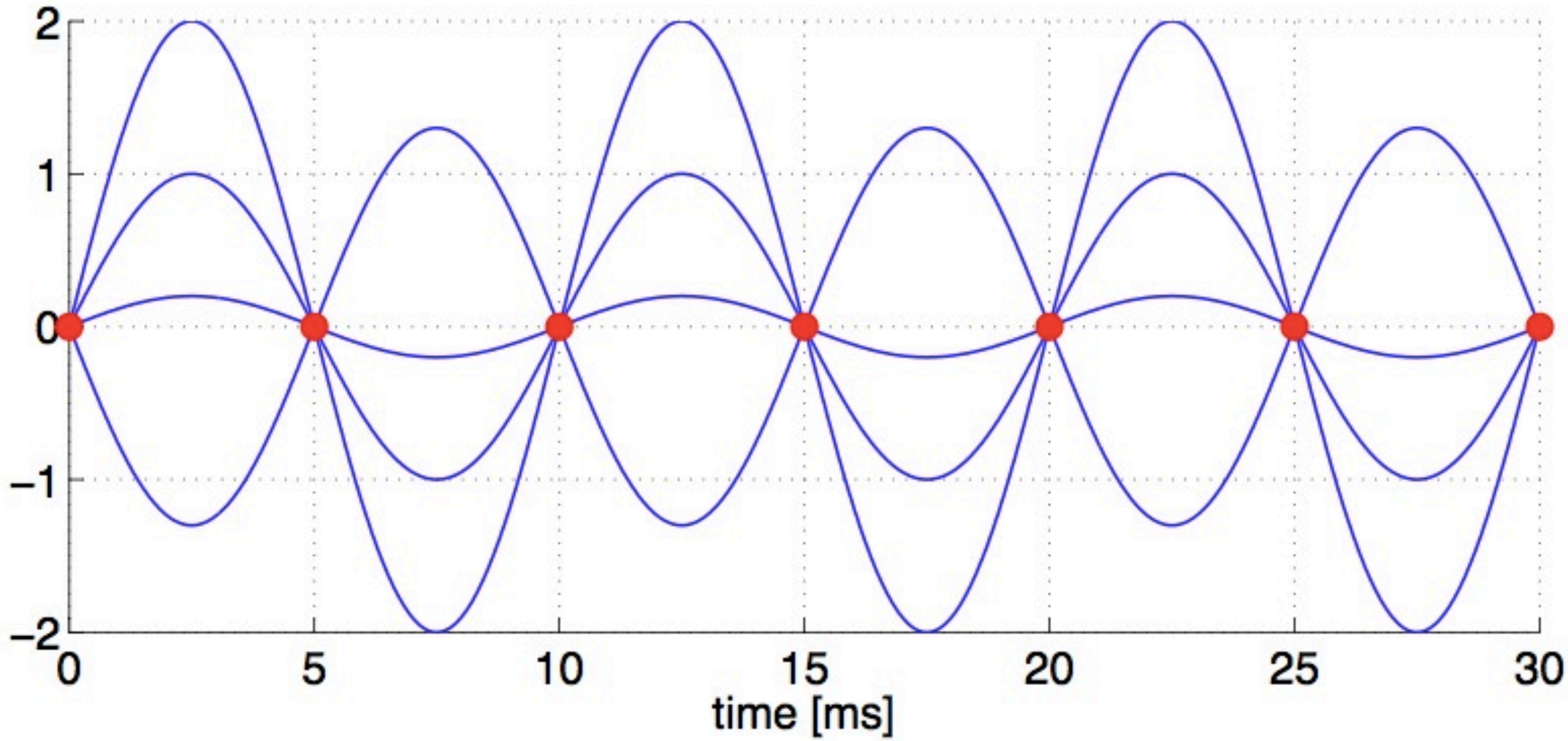
What happens if fs=f



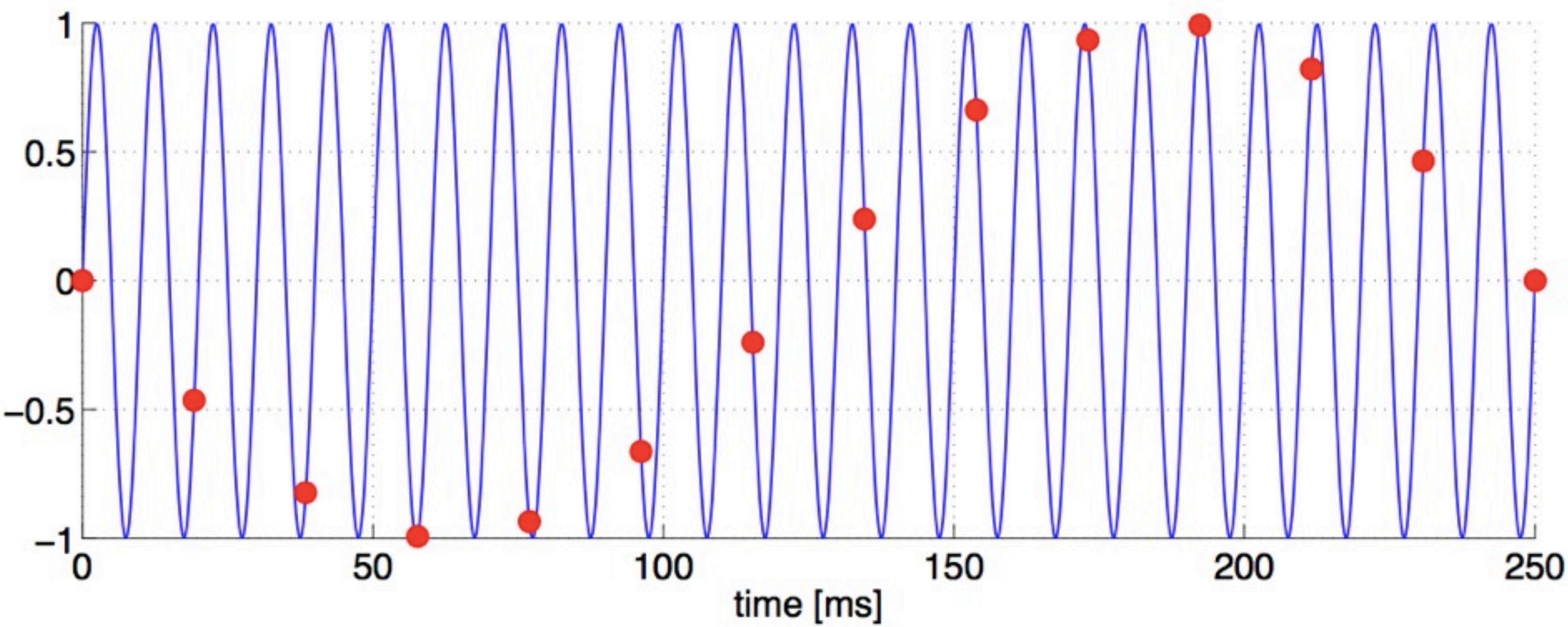


What happens if fs=f



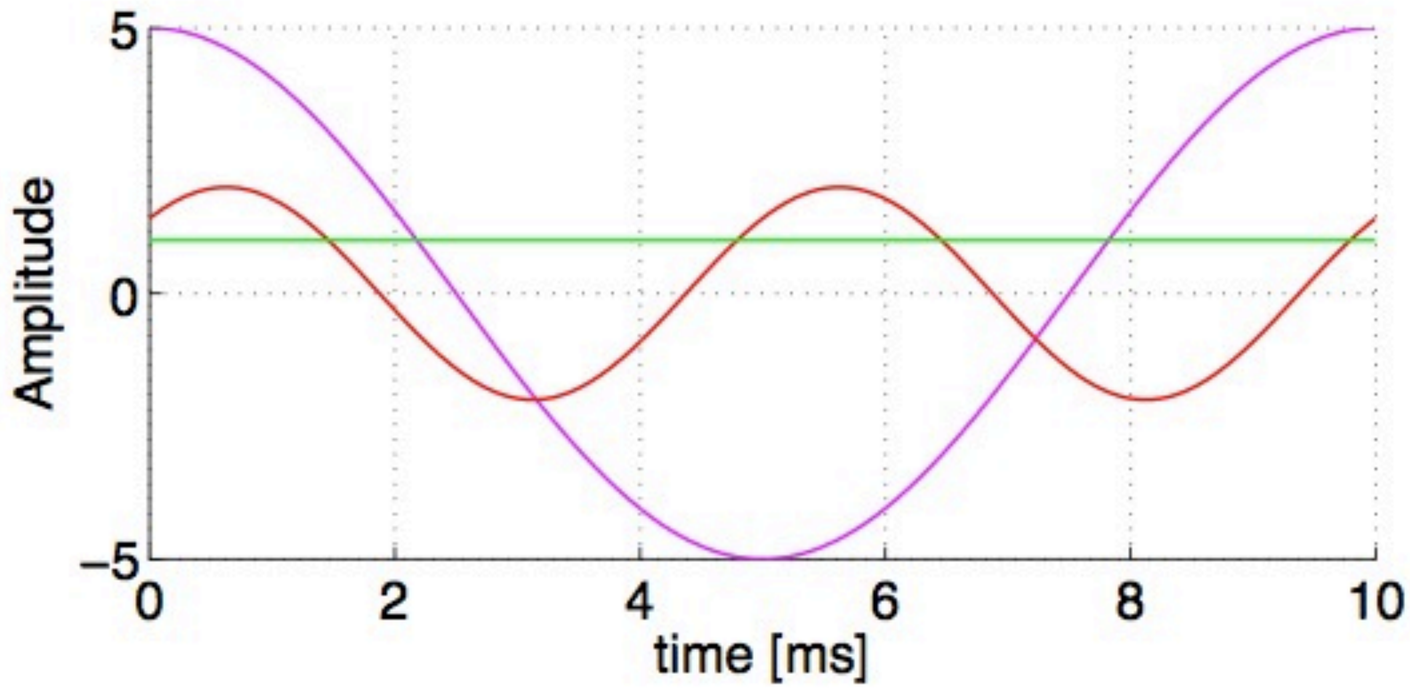


What might happen if fs is very low



ALIASING

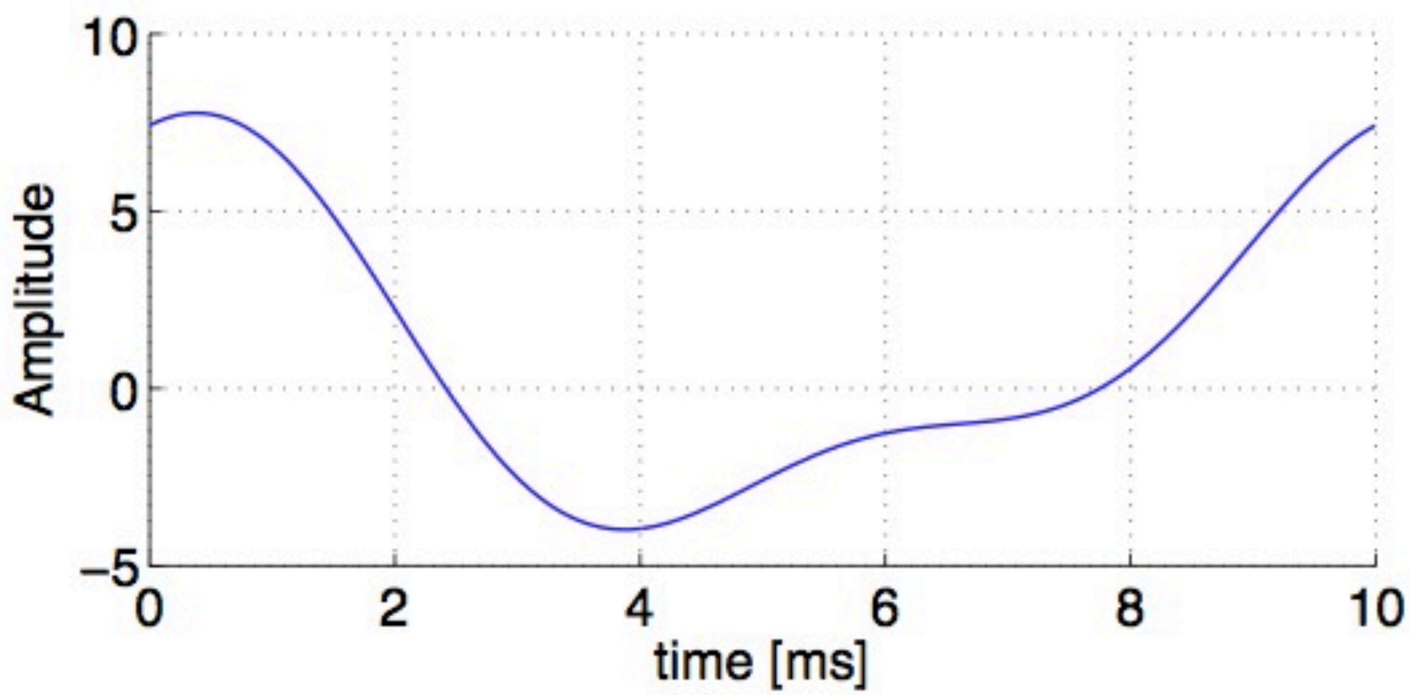
$$s = 5\cos(1\omega t + 0) + 2\cos\left(2\omega t - \frac{\pi}{2}\right) + 1$$



first harmonic

second harmonic

dc value



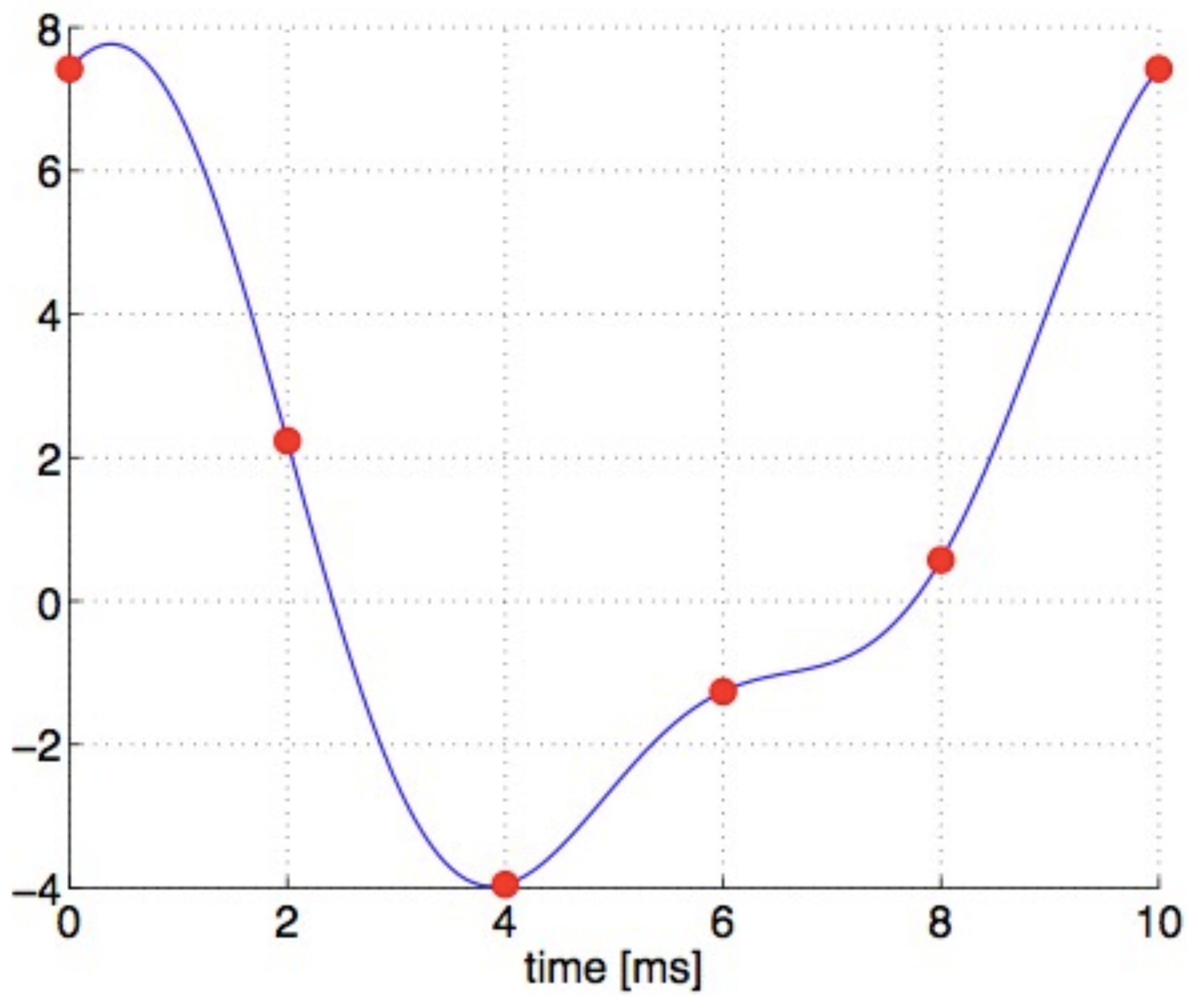
total

N=2

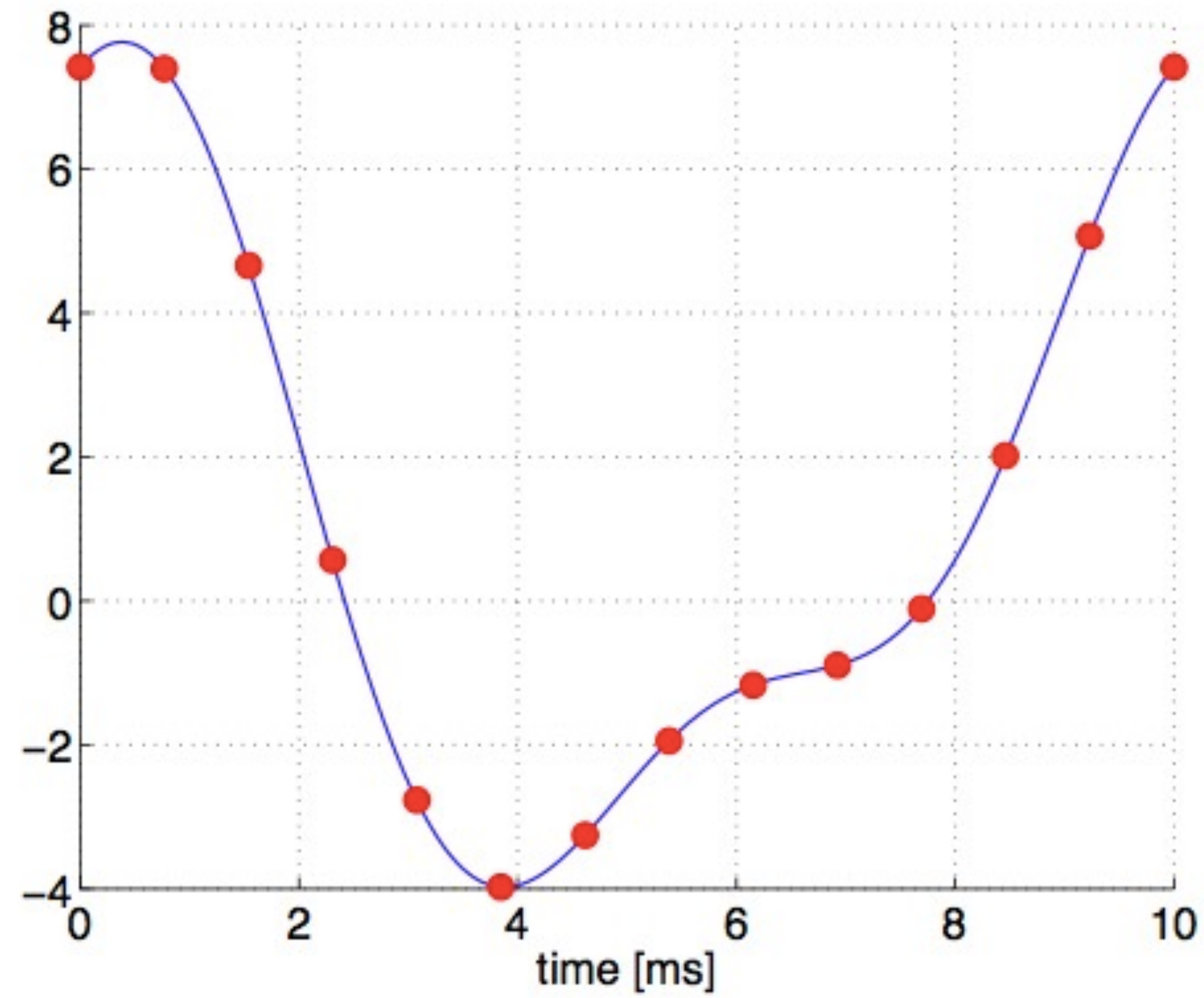
n=2N+1 = 5

We need at least 5 samples per period

Oversampling

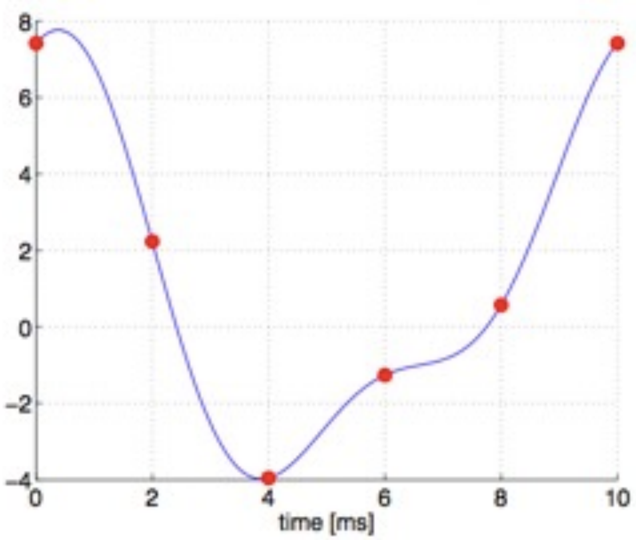


n=5

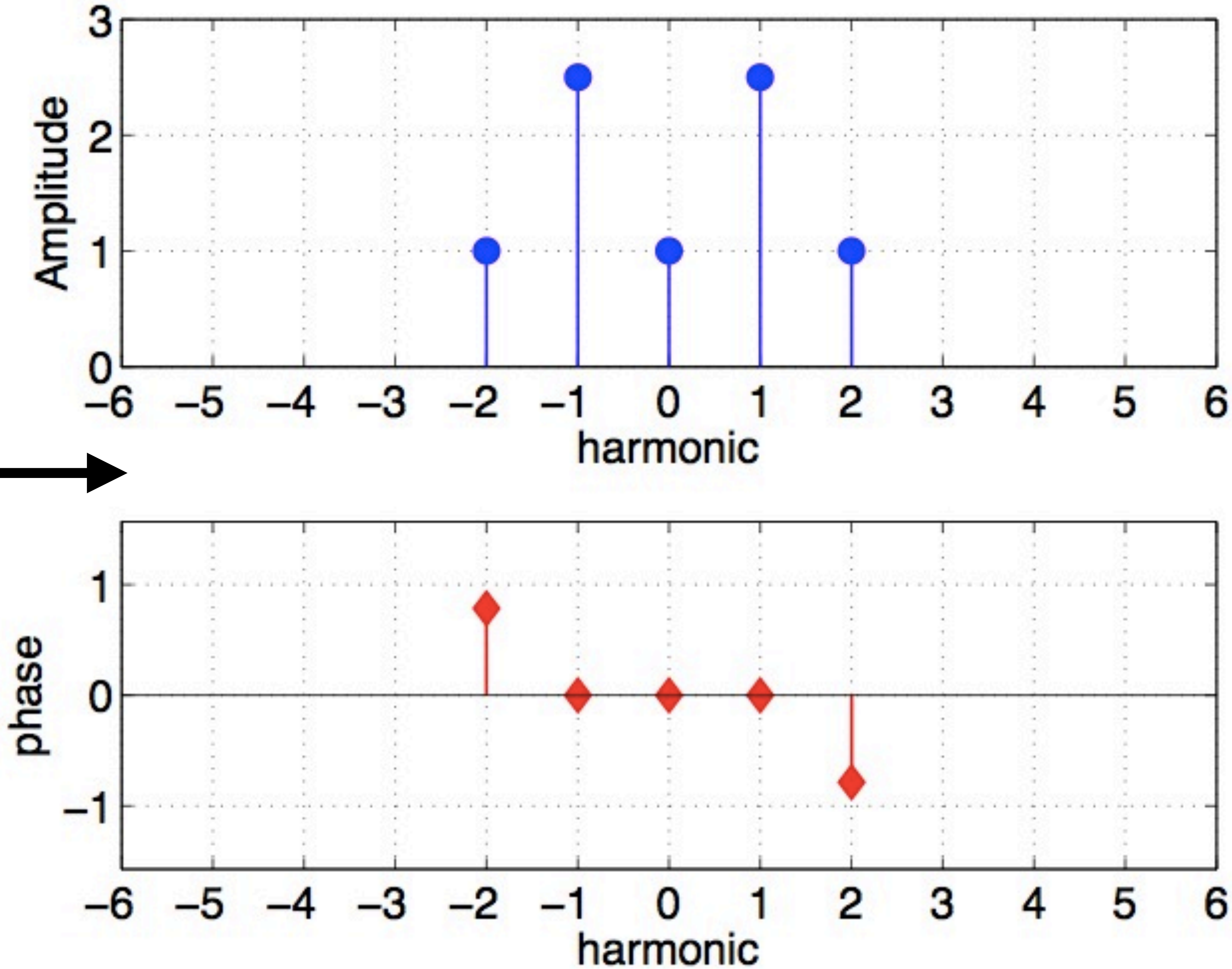


n=13

n=5

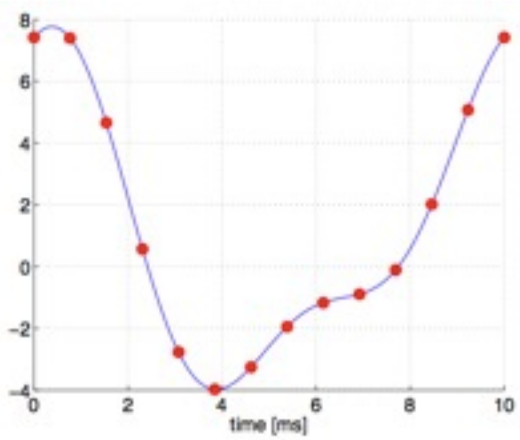


DFT

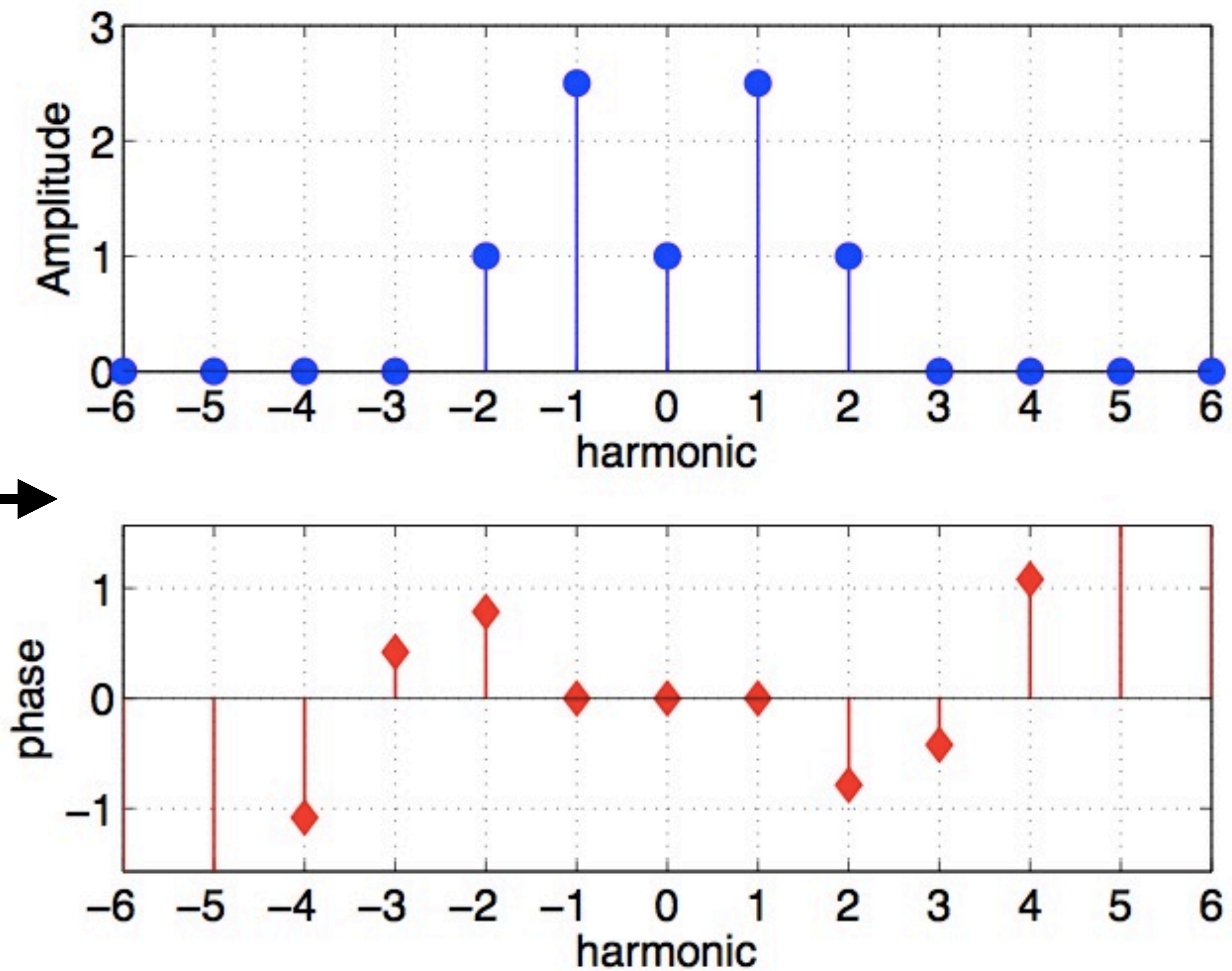


$$s = 5\cos(1\omega t + 0) + 2\cos\left(2\omega t - \frac{\pi}{2}\right) + 1$$

n=13

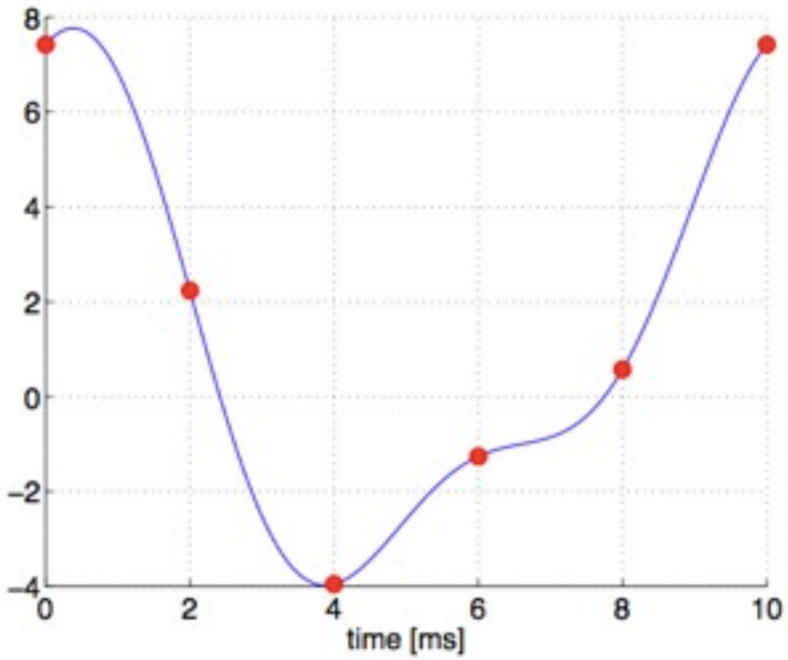


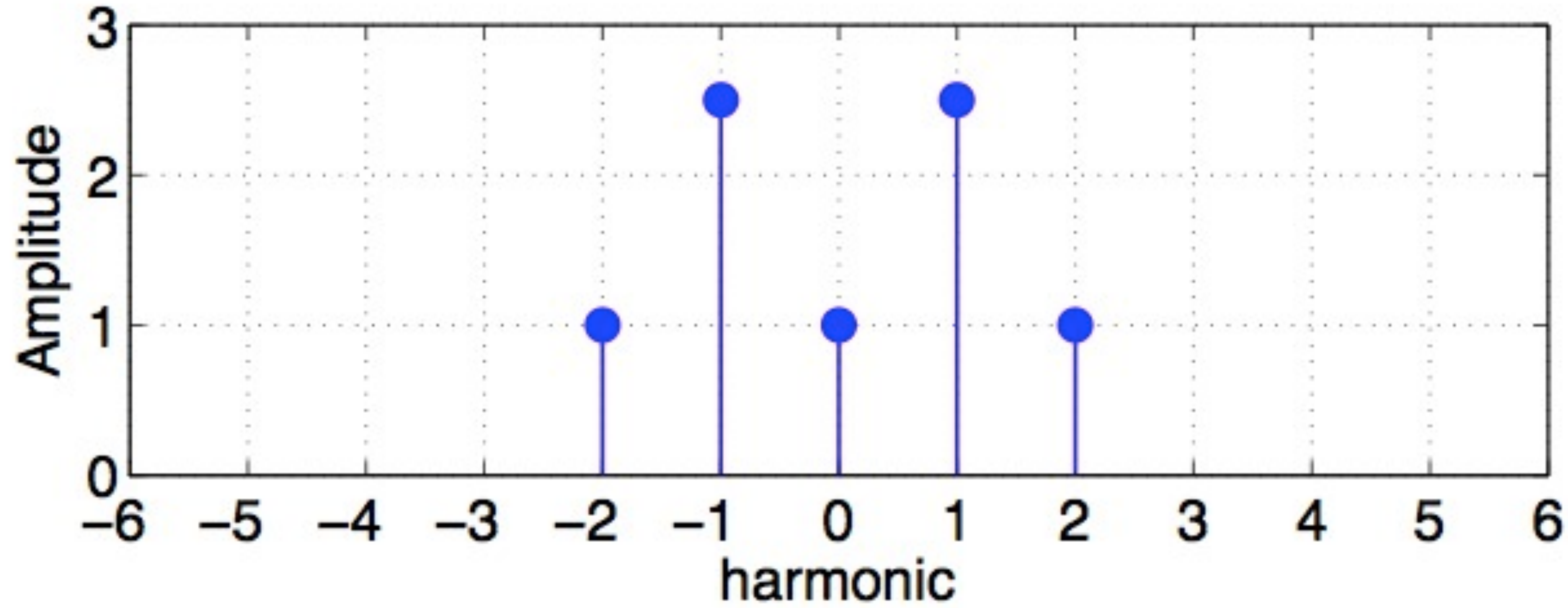
DFT



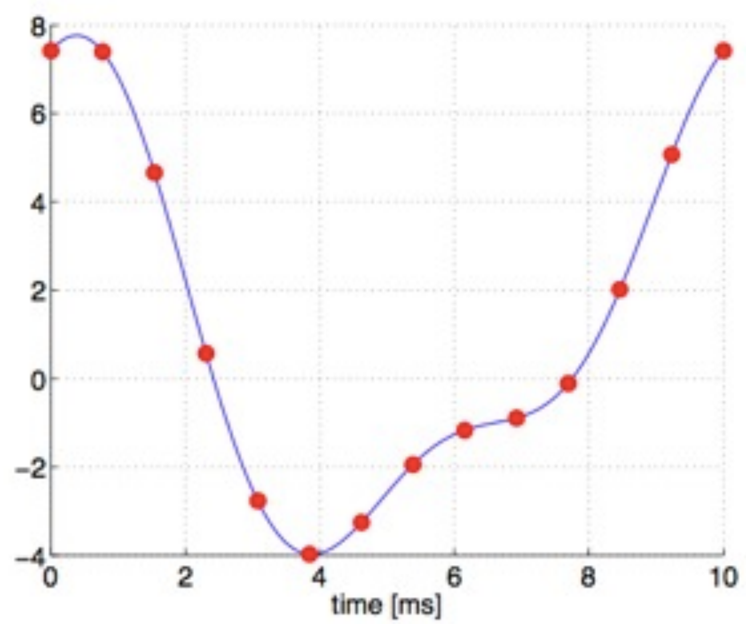
$$s = 5\cos(1\omega t + 0) + 2\cos\left(2\omega t - \frac{\pi}{2}\right) + 1$$

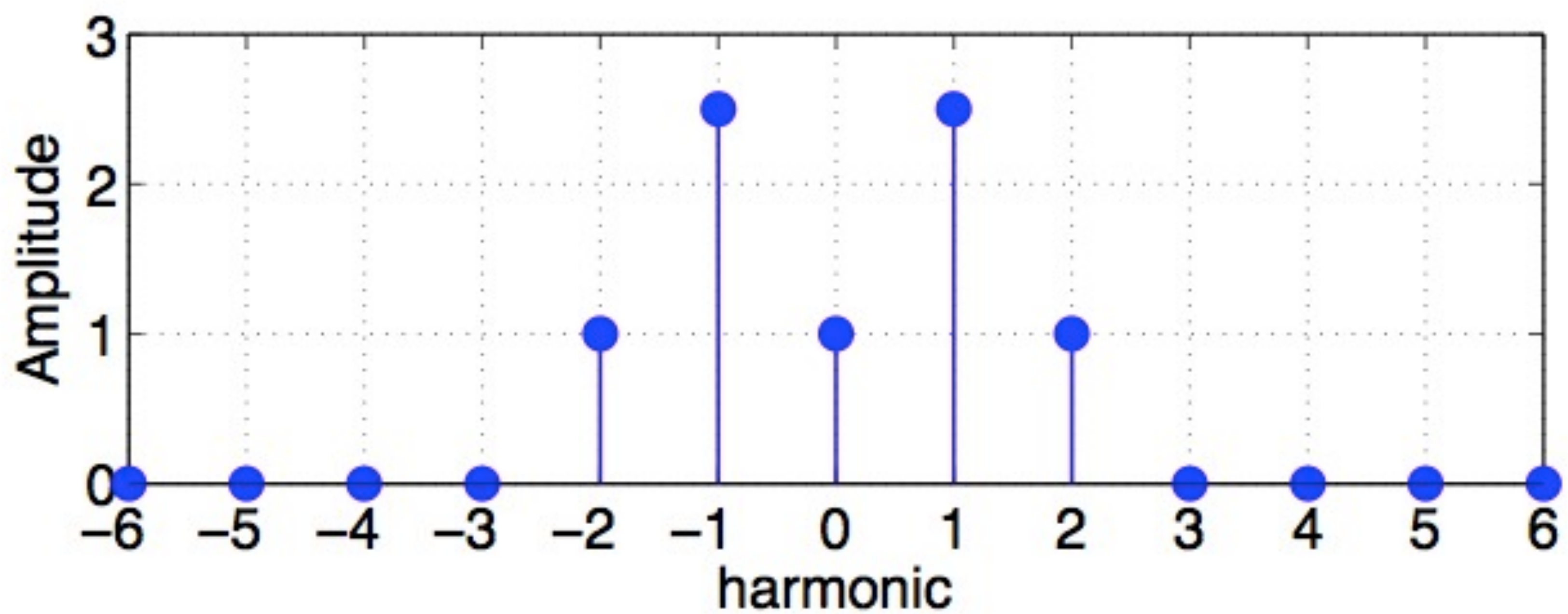
n=5



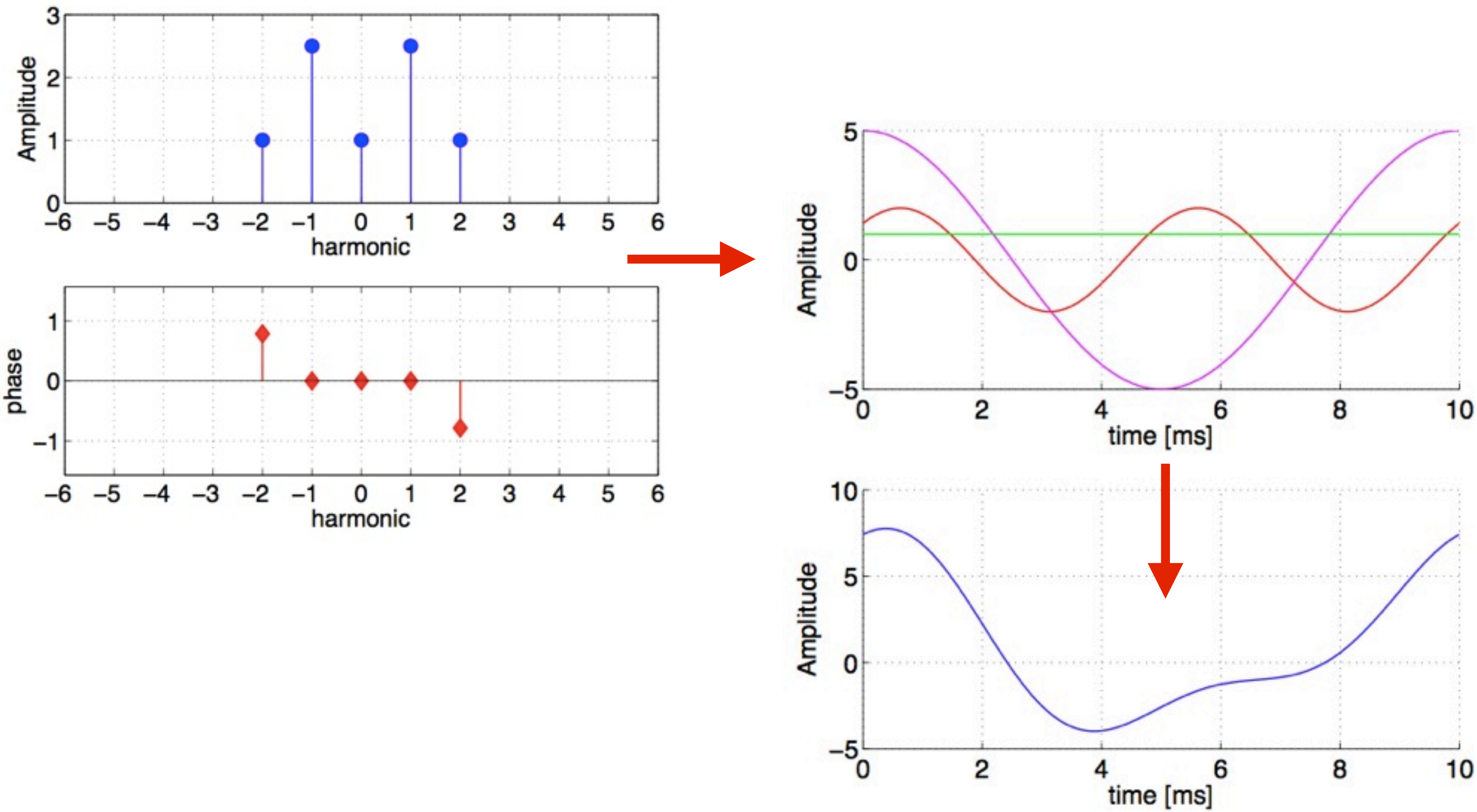


n=13



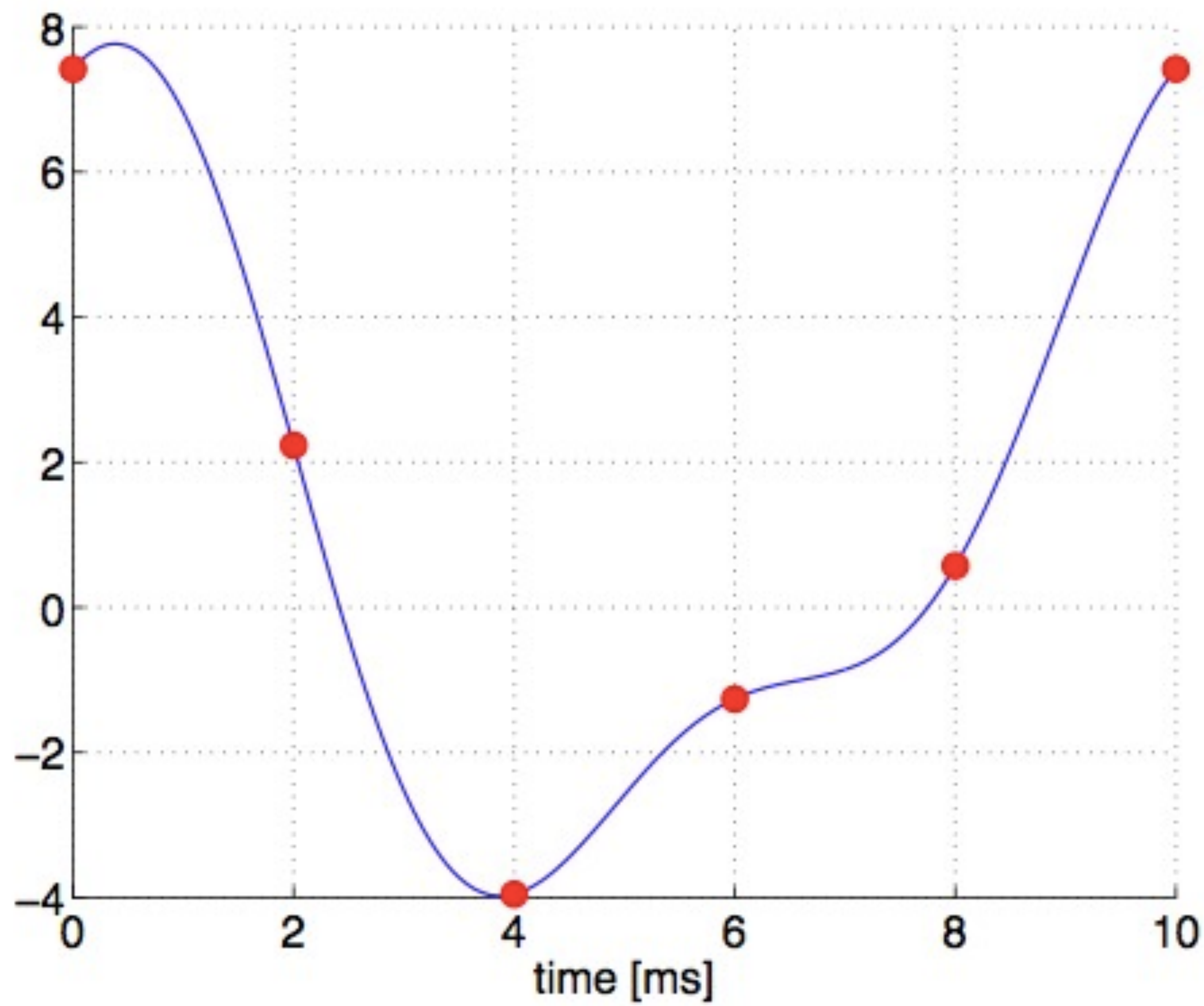


Reconstruction of the signal

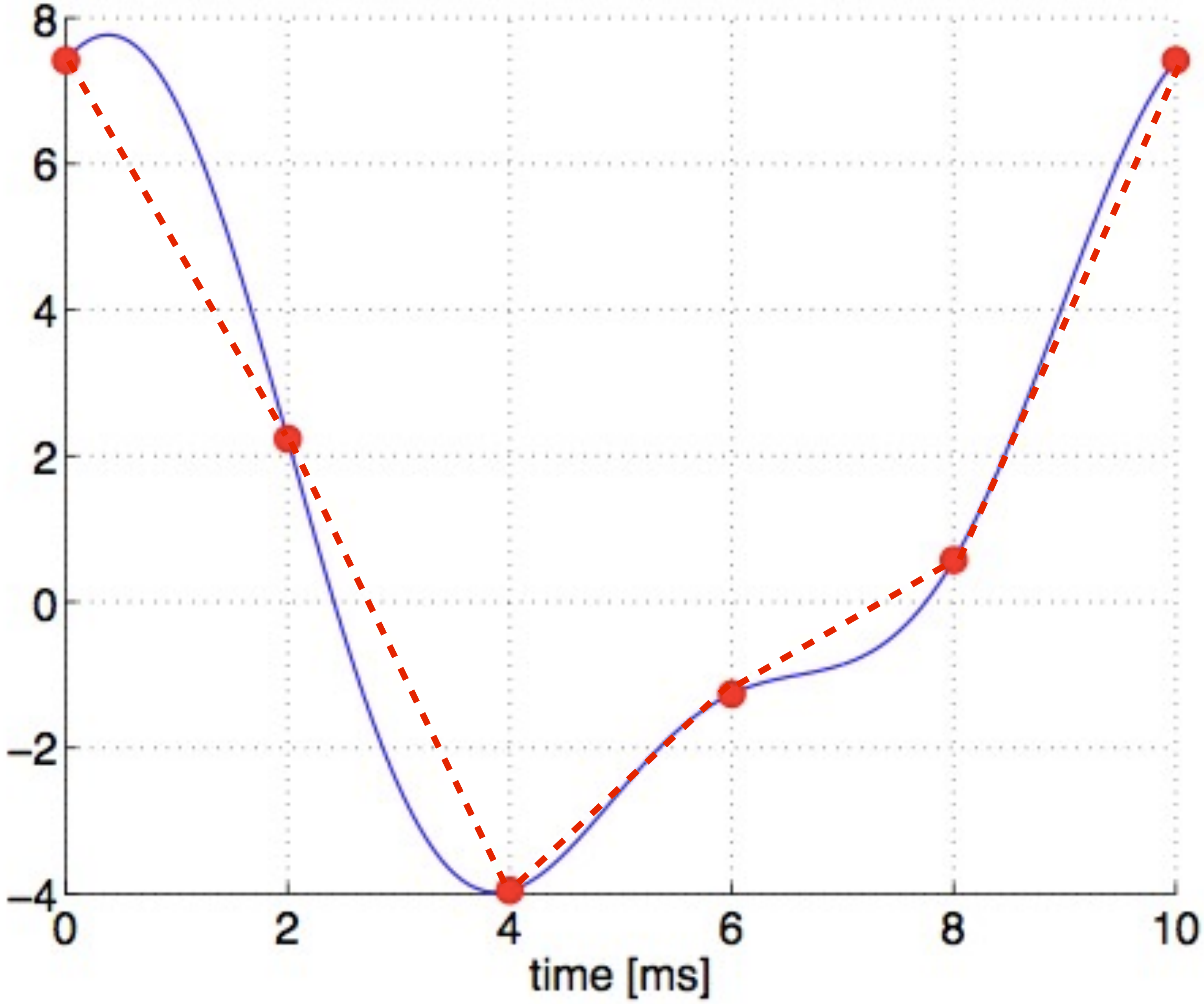


Reconstruction of the signal

1. Sampling
2. samples
3. DFT
4. spectrum
5. amplitude and phase of the harmonics
6. $s(t) = \sum_{i=1}^{N} A_i \cos(i\omega t + \varphi_i) + k$
7. we can calculate s(t) at any value of t

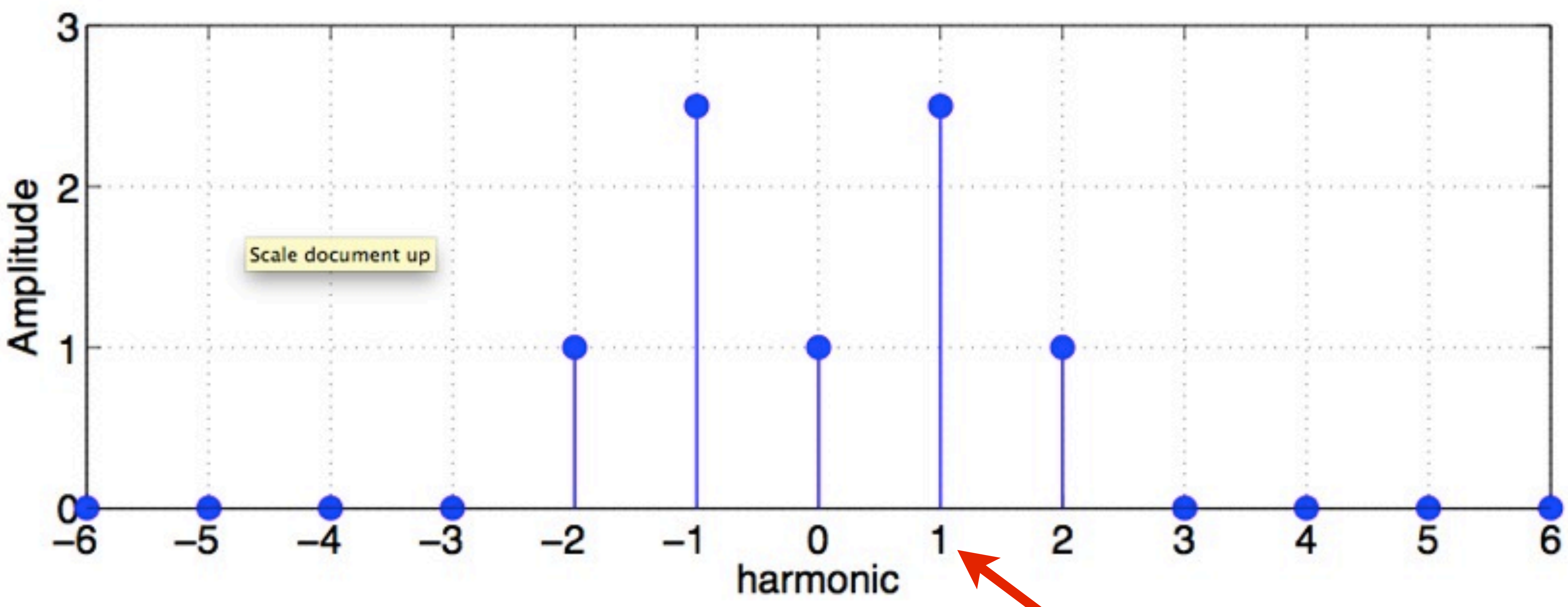


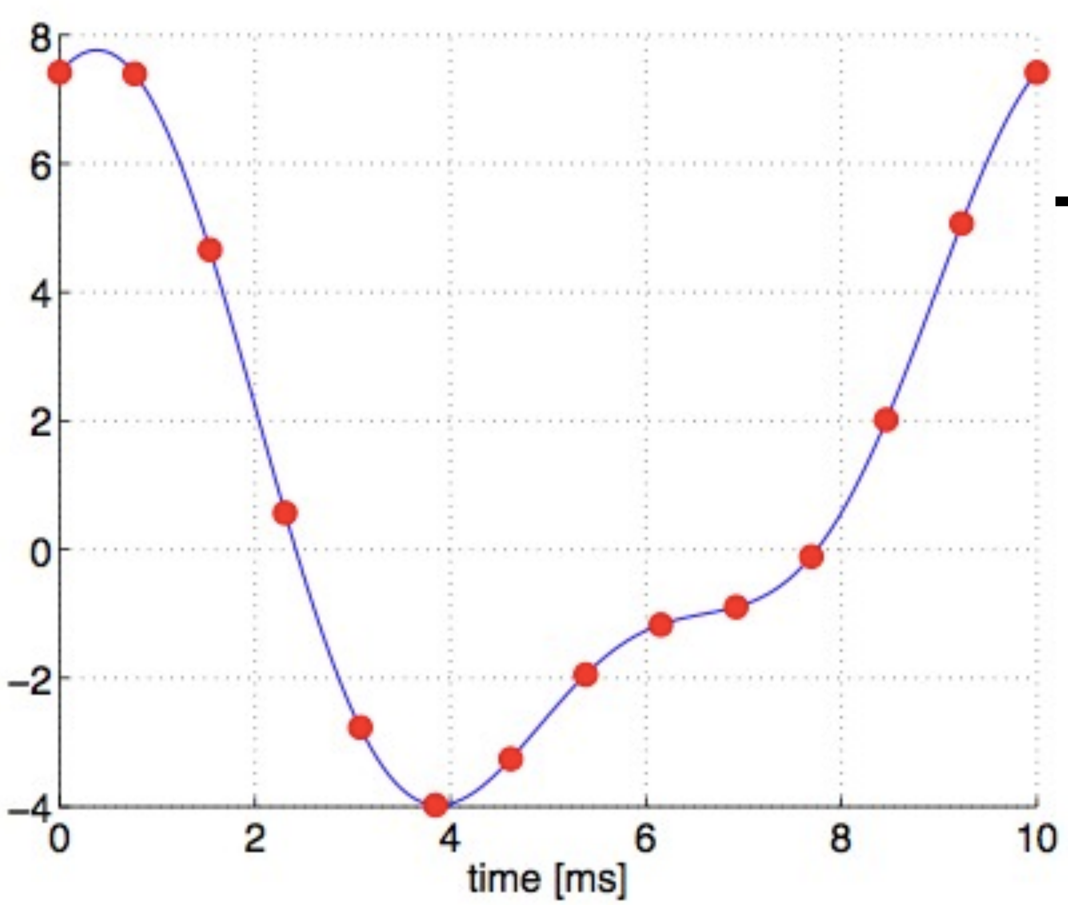
Reconstruction of the signal is NOT interpolation



Reconstruction of the signal can calculate perfectly any point of the signal, interpolation cannot

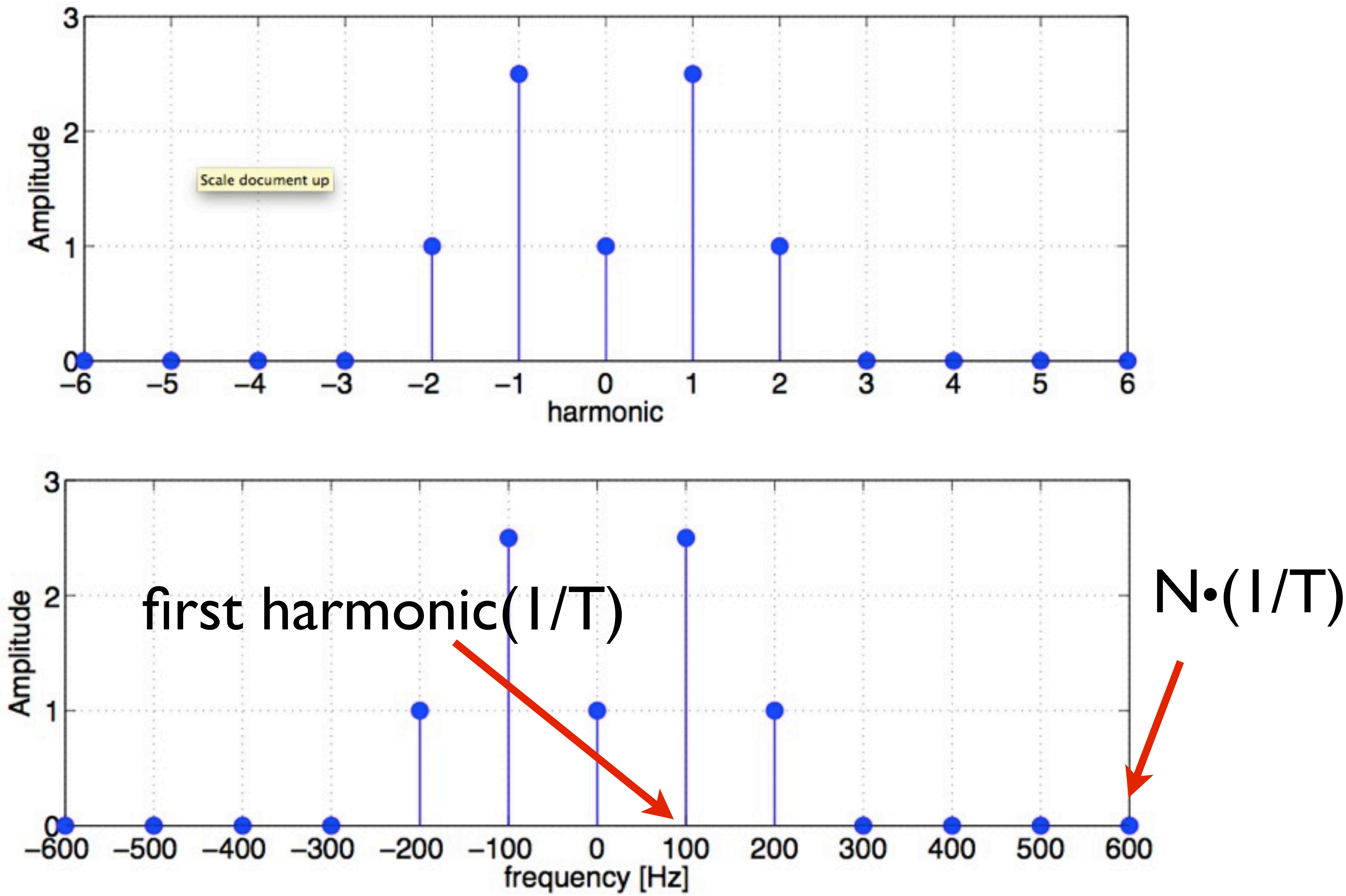
Let's watch the spectrum closer





T= 10 ms → f=100 Hz

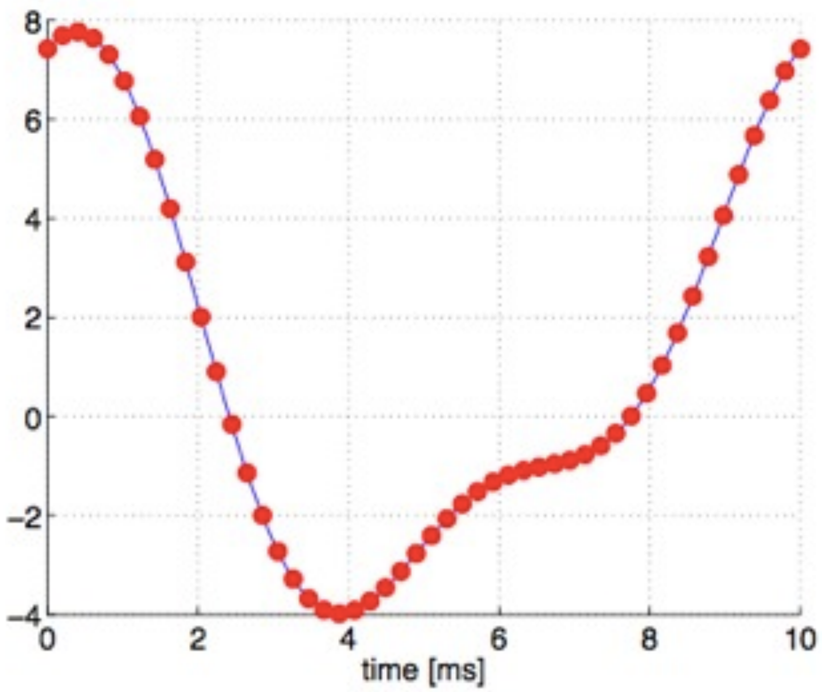
n=2N+1=13 → N=6

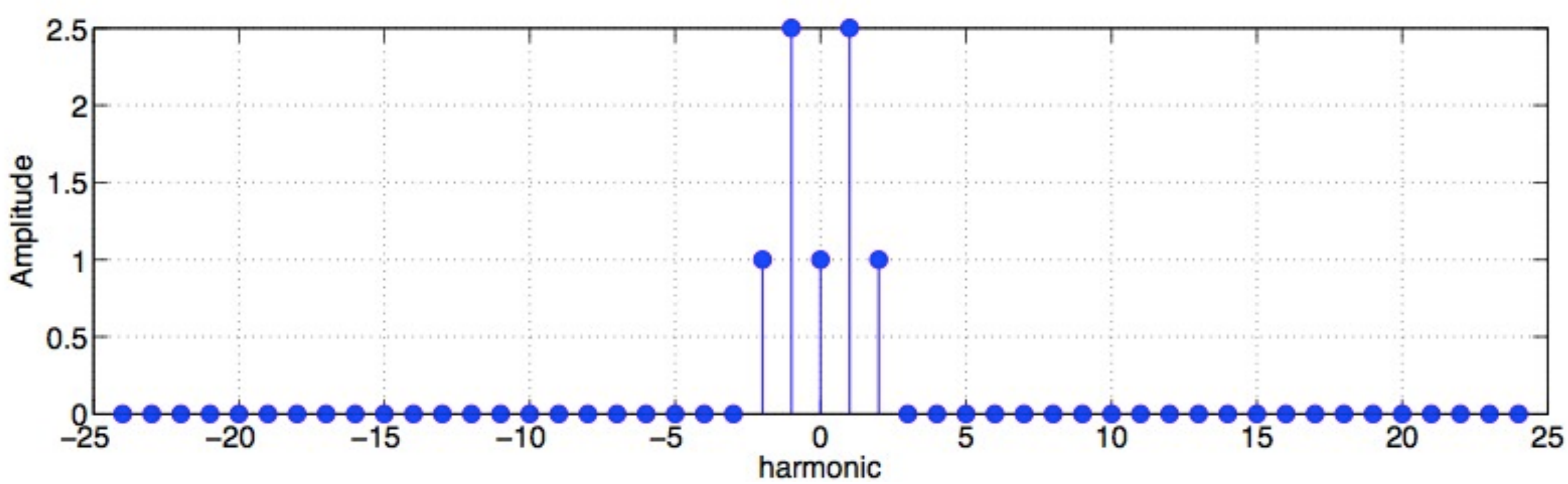

Amplitude
harmonic
Scale document up
Amplitude
frequency [Hz]
first harmonic(1/T)
N•(1/T)

What happens if...

we increase the sampling frequency fs

fs ↑ Ts ↓ n=2N+1 ↑ N ↑

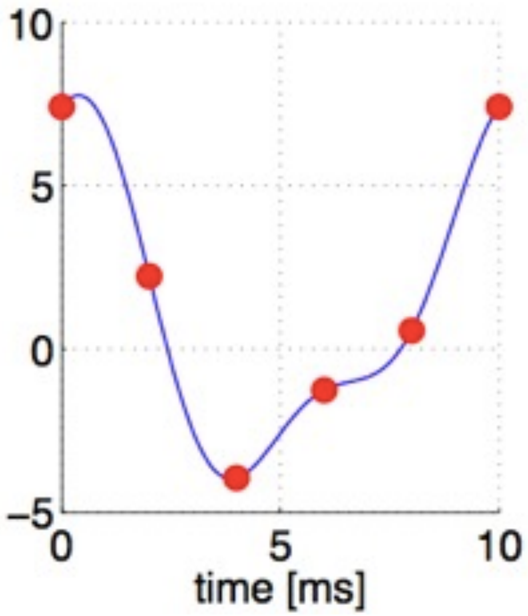


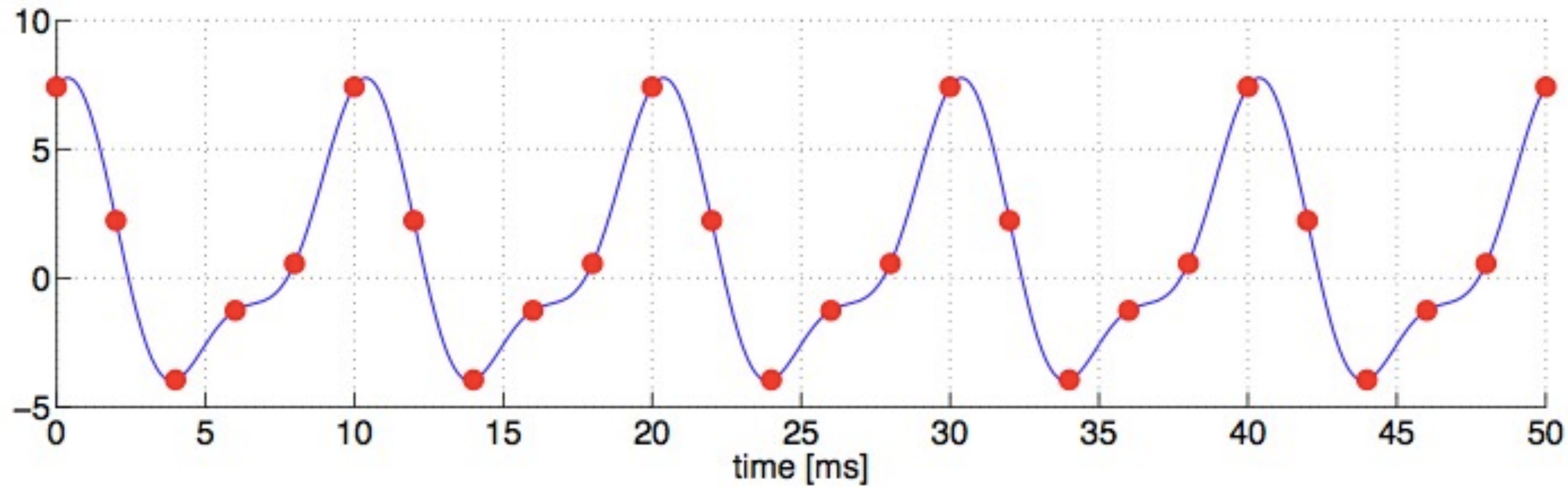


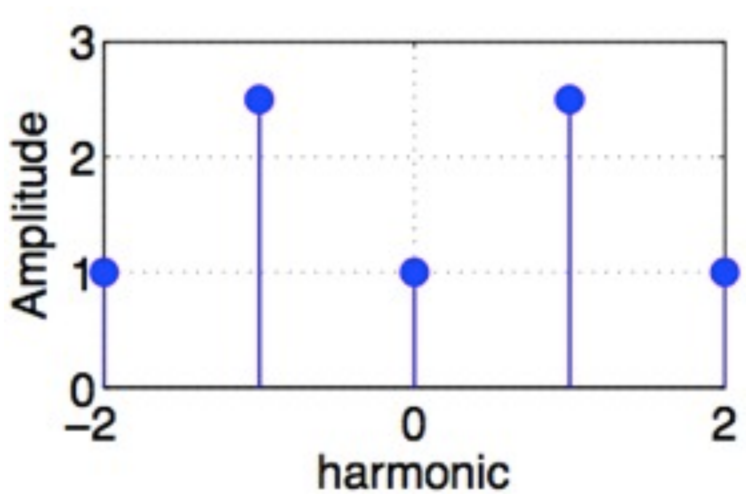
What happens if...

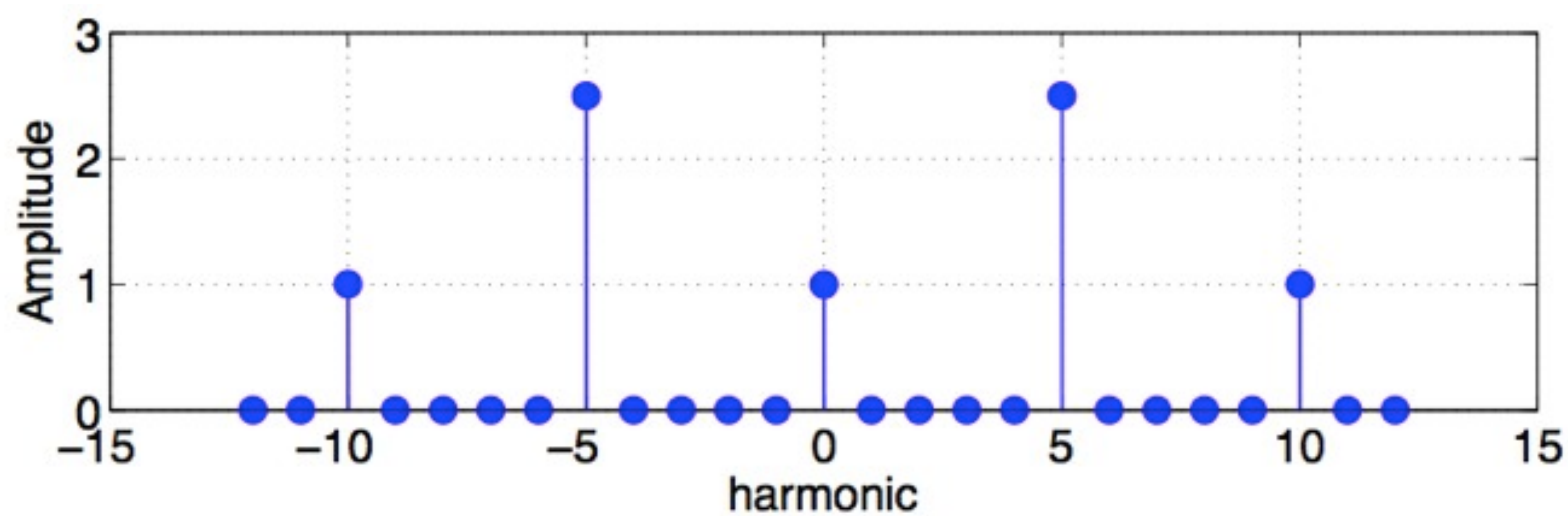
we increase the acquiring time

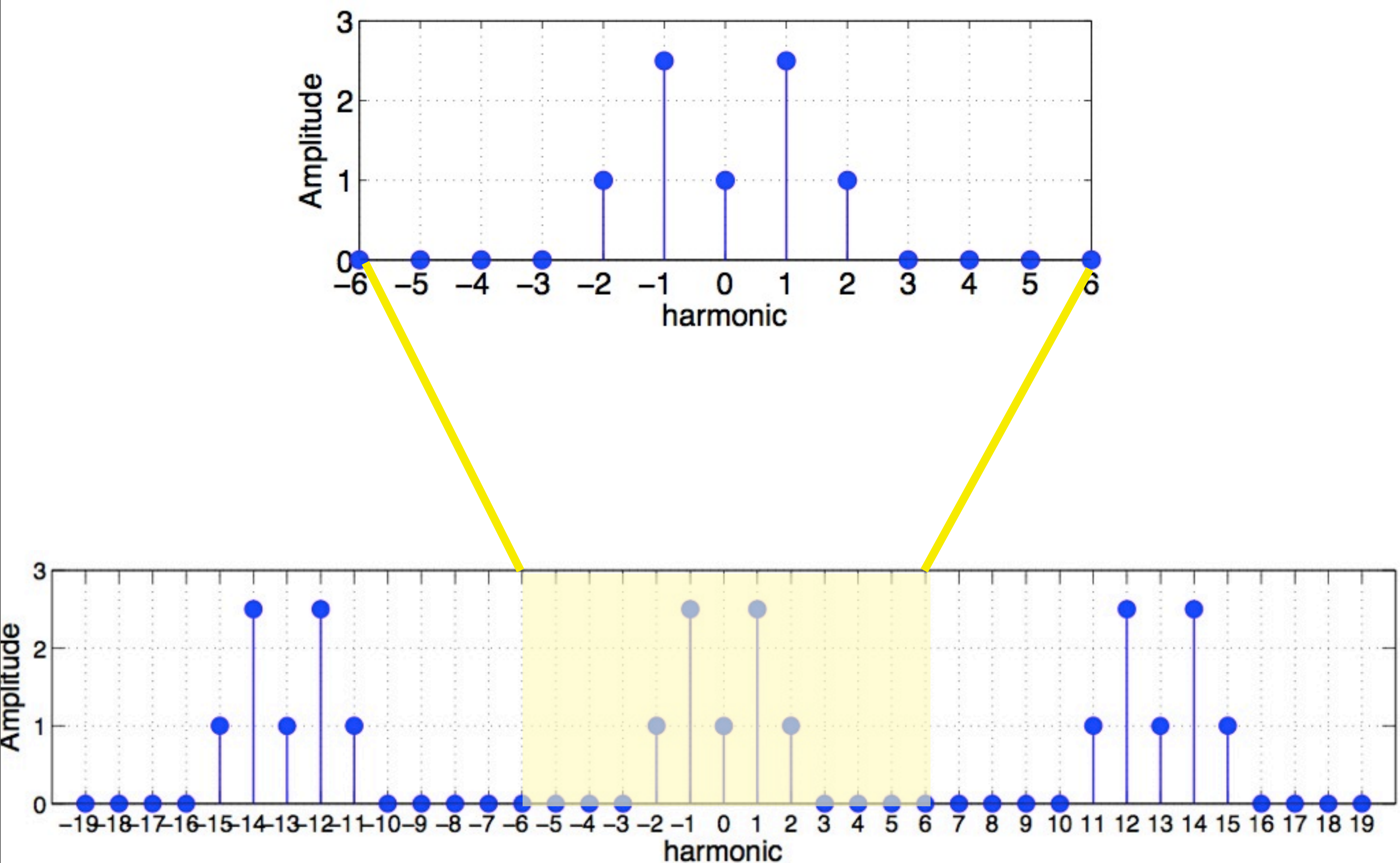
and fs does not change



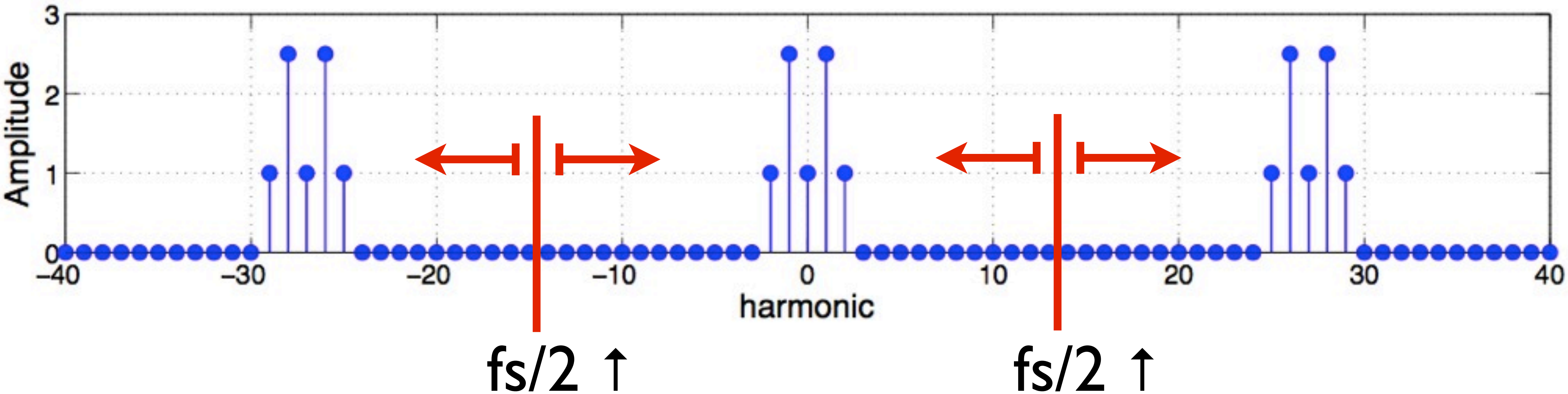




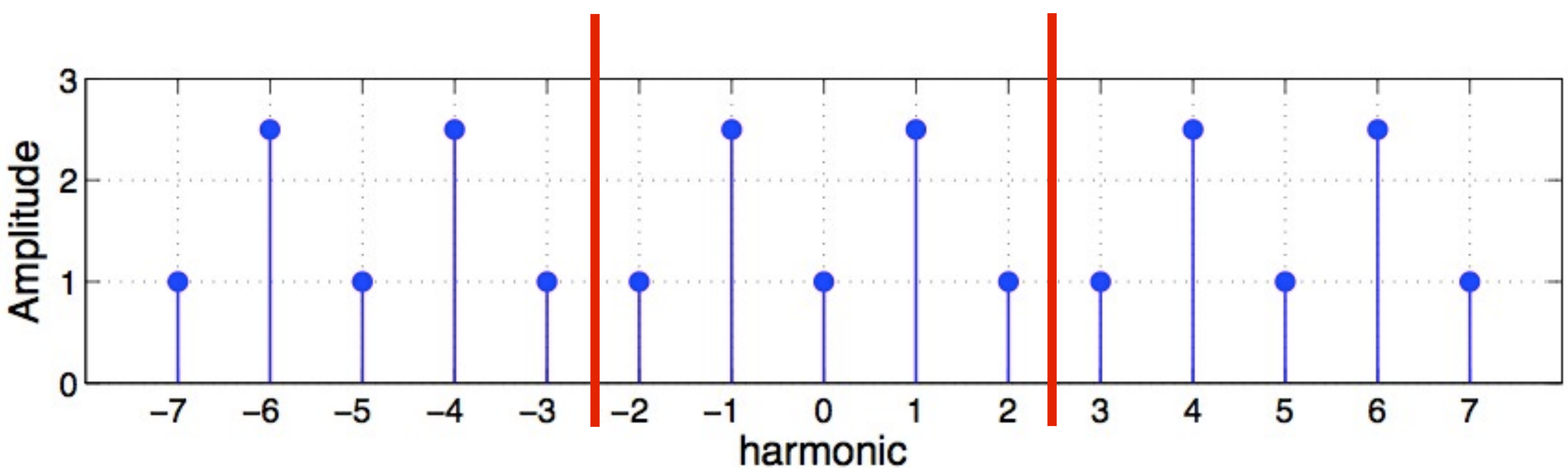



3
2
1
0
Amplitude
−6 −5 −4 −3 −2 −1 0 1 2 3 4 5 6
harmonic
3
2
1
0
Amplitude
−19 −18 −17 −16 −15 −14 −13 −12 −11 −10 −9 −8 −7 −6 −5 −4 −3 −2 −1 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
harmonic

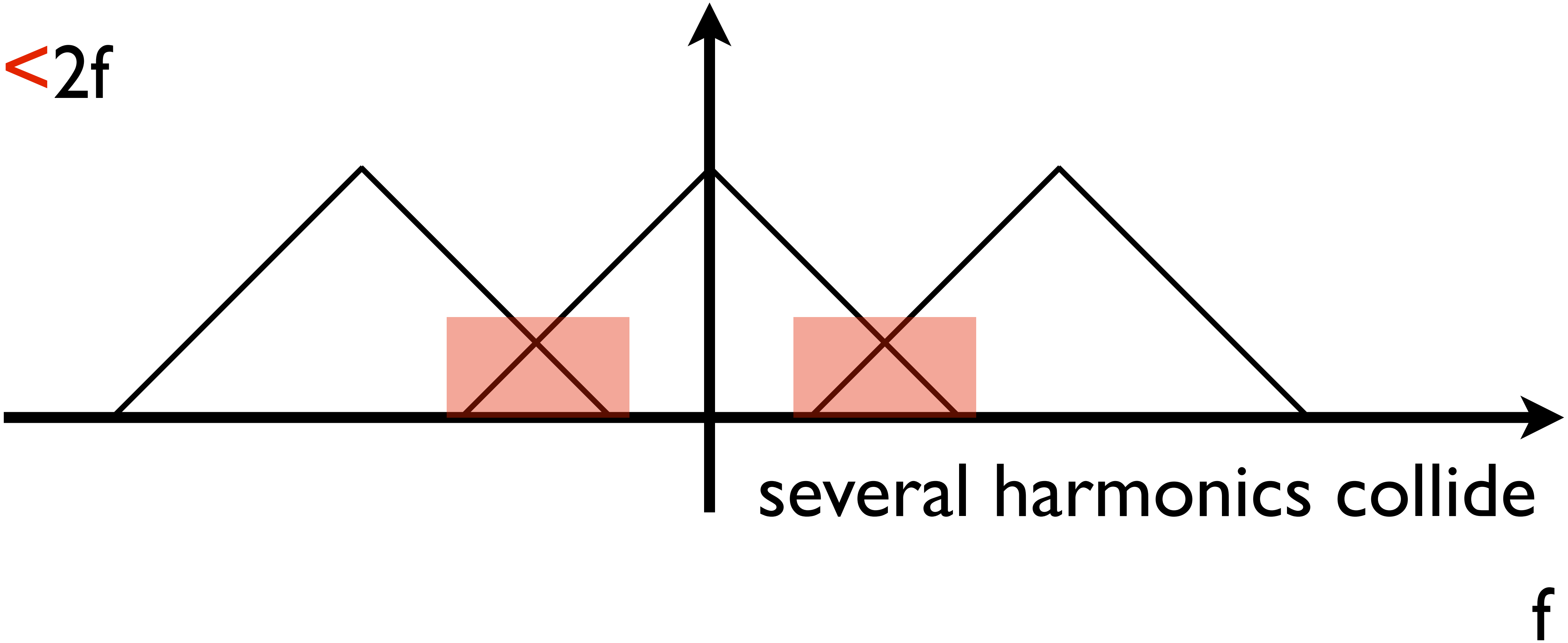
Large sampling frequency pushes the spectra apart



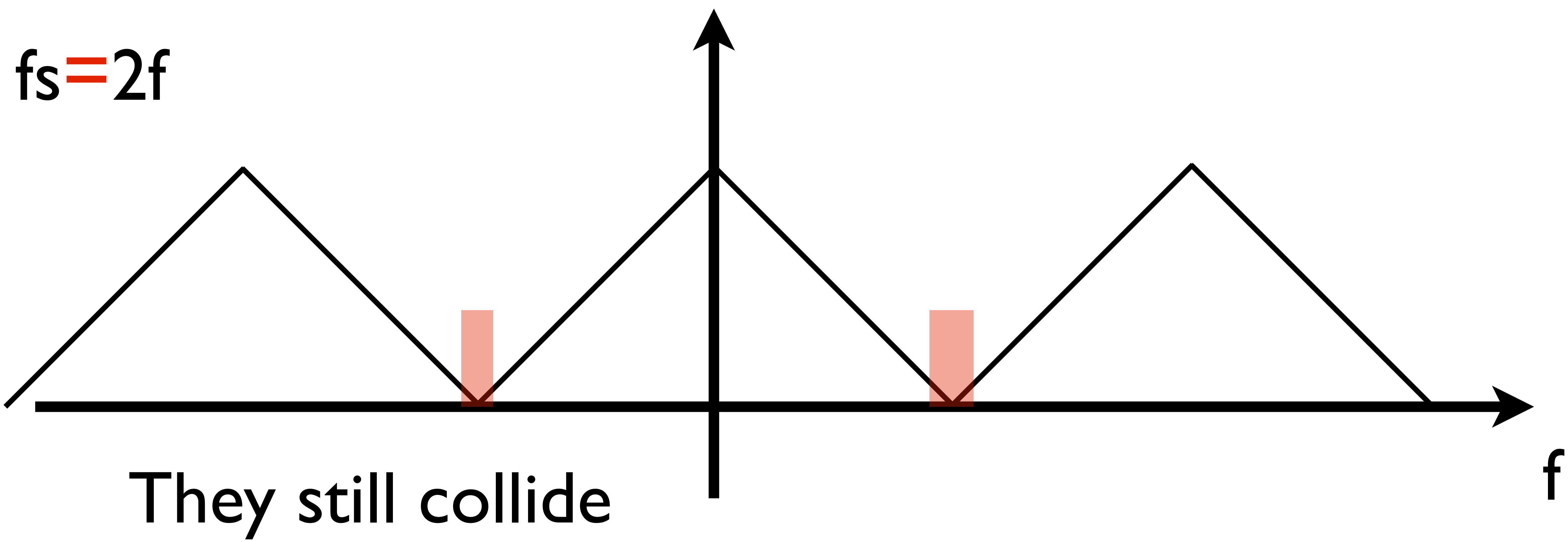
The minimum fs to avoid "collision" of spectra is fs>2f



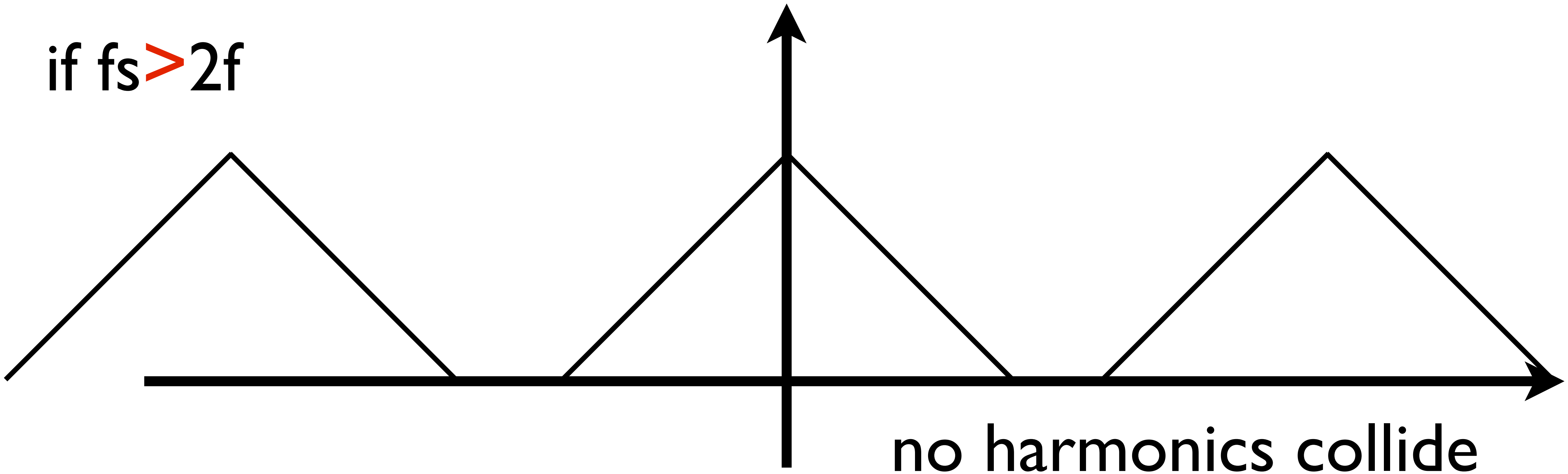
if fs<2f



if fs=2f



if fs>2f



no harmonics collide

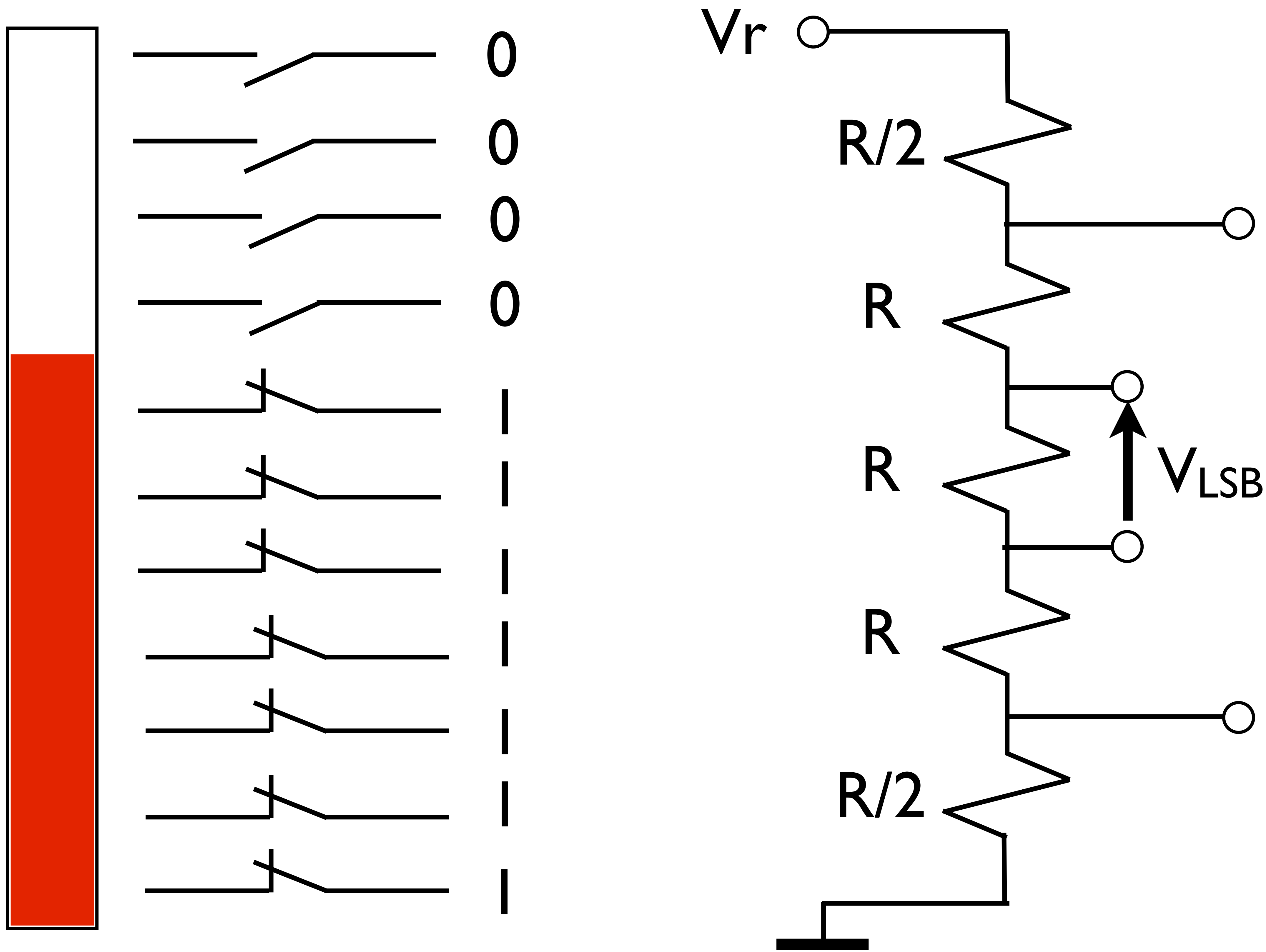
f

ANALOG TO DIGITAL CONVERTERS

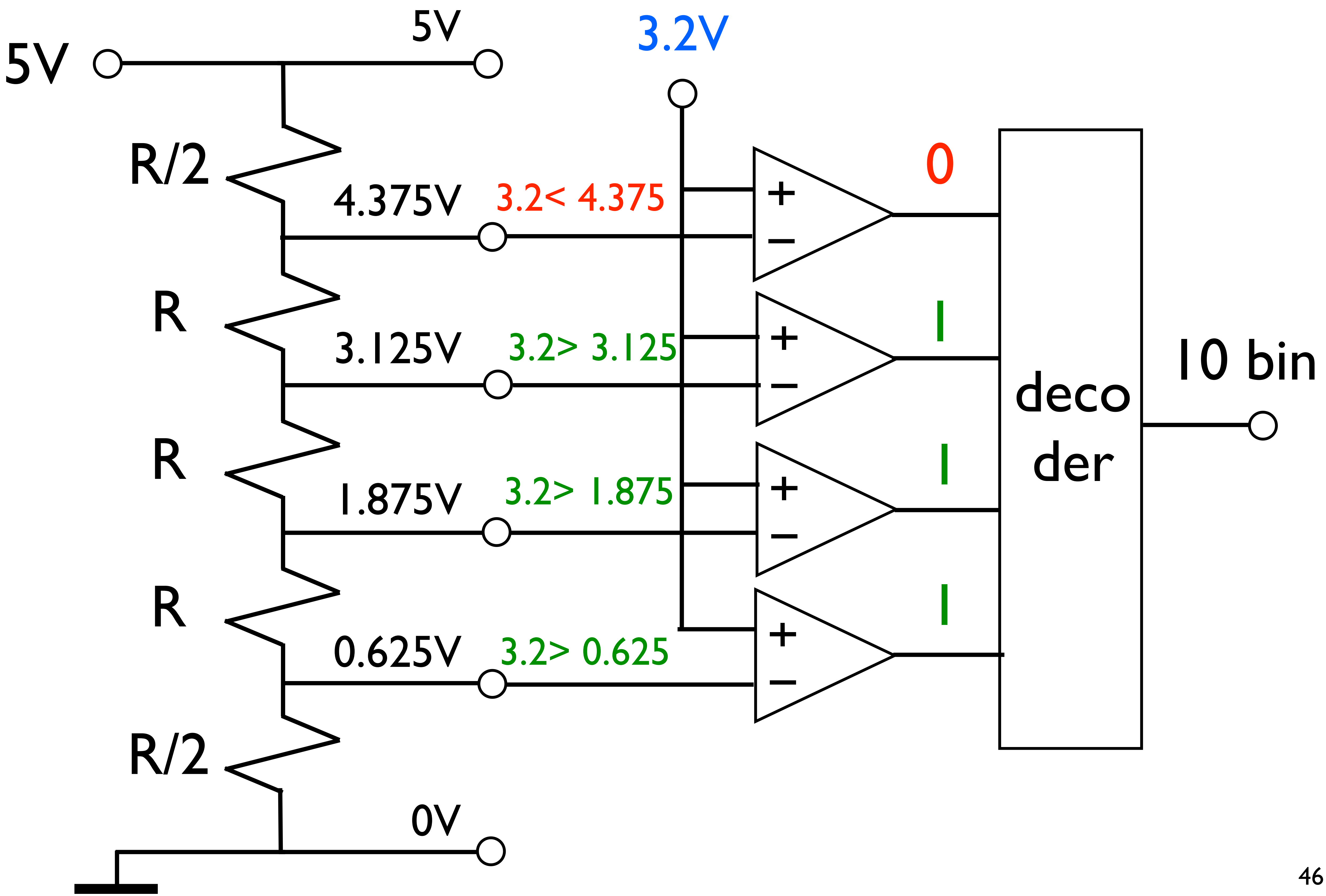
Two main parameters:
- resolution (number of bits)
- sampling frequency

FLASH
Successive approximation
Dual slope integration
Sigma delta

FLASH



FLASH



5V
5V
3.2V
R/2
4.375V
3.2< 4.375
0
+
−
R
3.125V
3.2> 3.125
1
R
1.875V
3.2> 1.875
1
R
0.625V
3.2> 0.625
1
R/2
0V
deco
der
10 bin

FLASH

- Very high speed (even 1 GHz)
- Poor resolution (6 to 8 bits)

SUCCESSIVE APPROXIMATIONS

Principle

V_{ref}=8 V
Resolution 6 bits

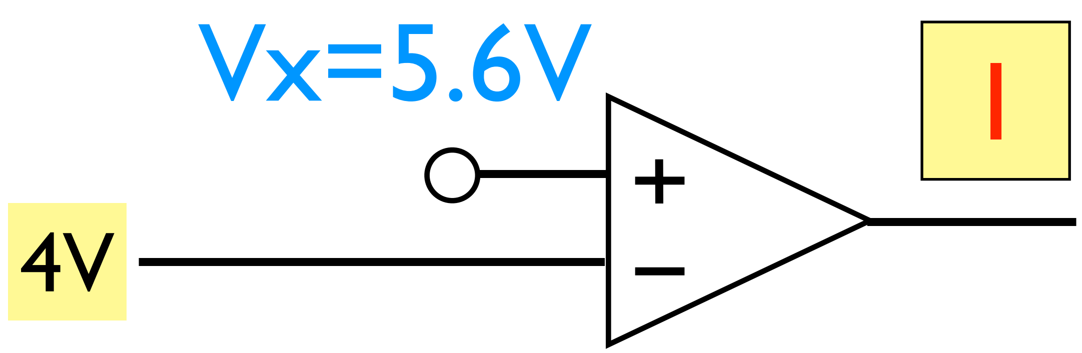
MSB					LSB
1	1	1	1	1	1
4V	2V	1V	0.5V	0.25V	0.125V

SUCCESSIVE APPROXIMATIONS

MSB					LSB
?	?	?	?	?	?
4V	2V	1V	0.5V	0.25V	0.125V

I want to convert Vx=5.6V

STEP 1

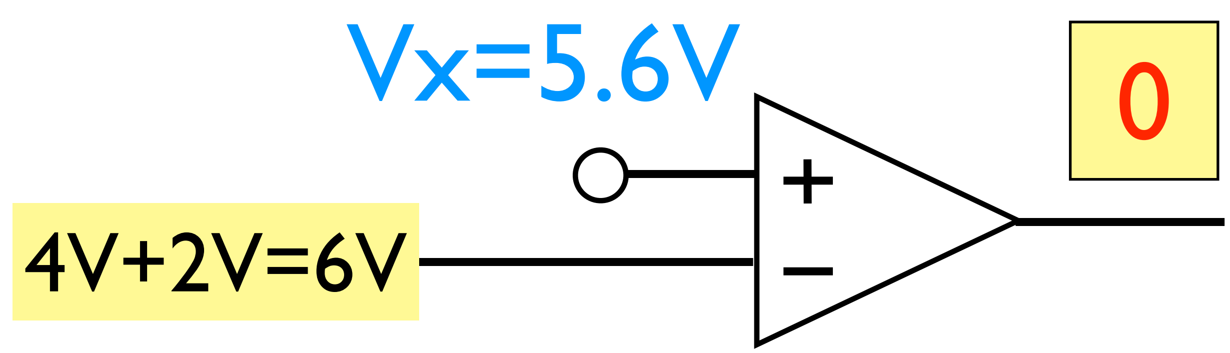


MSB					LSB
1	?	?	?	?	?
4V	2V	1V	0.5V	0.25V	0.125V

SUCCESSIVE APPROXIMATIONS

MSB					LSB
1	?	?	?	?	?
4V	2V	1V	0.5V	0.25V	0.125V

STEP 2

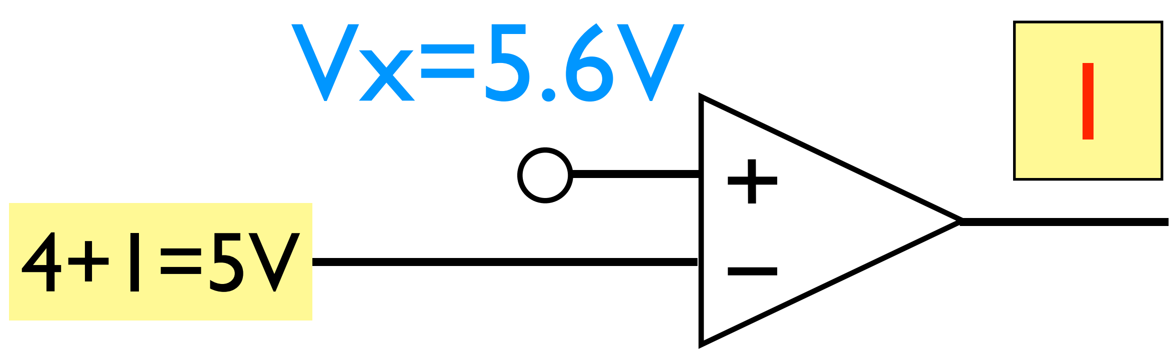


MSB					LSB
1	0	?	?	?	?
4V	2V	1V	0.5V	0.25V	0.125V

SUCCESSIVE APPROXIMATIONS

MSB					LSB
1	0	?	?	?	?
4V	2V	1V	0.5V	0.25V	0.125V

STEP 3

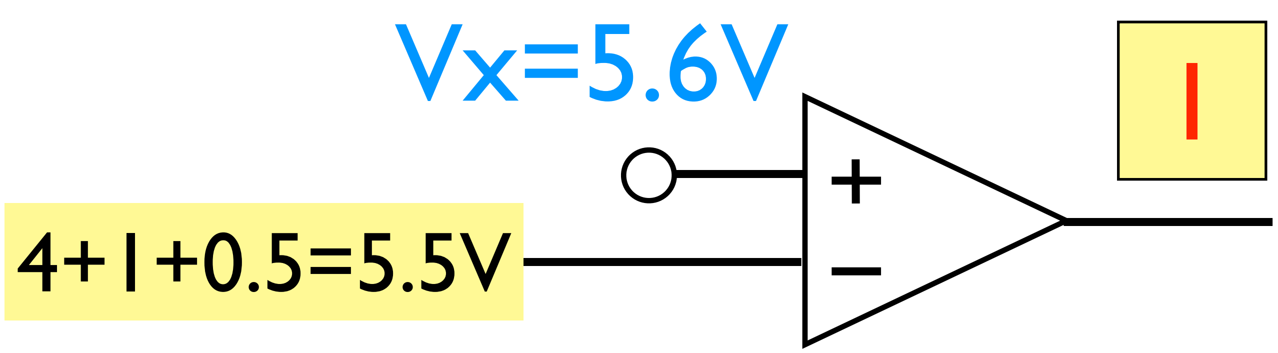


MSB					LSB
1	0	1	?	?	?
4V	2V	1V	0.5V	0.25V	0.125V

SUCCESSIVE APPROXIMATIONS

MSB					LSB
1	0	1	?	?	?
4V	2V	1V	0.5V	0.25V	0.125V

STEP 4

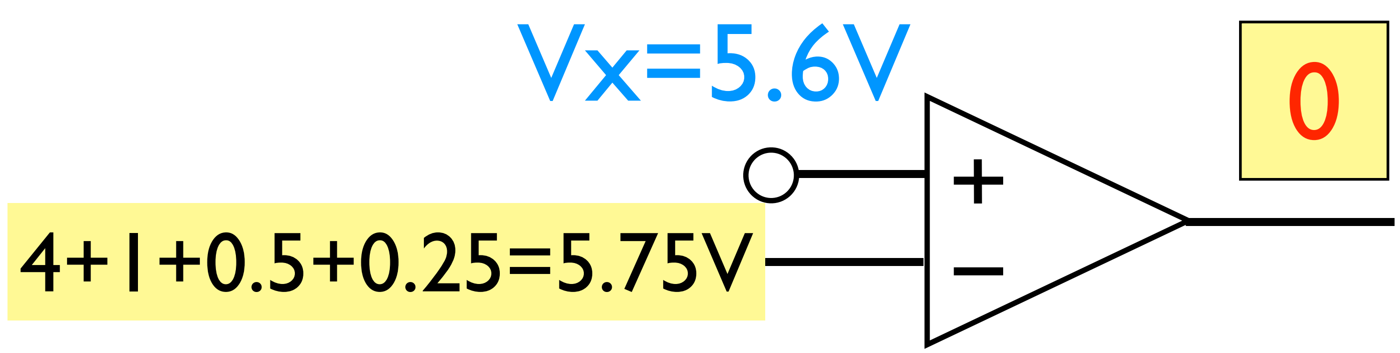


MSB					LSB
1	0	1	1	?	?
4V	2V	1V	0.5V	0.25V	0.125V

SUCCESSIVE APPROXIMATIONS

MSB					LSB
1	0	1	1	?	?
4V	2V	1V	0.5V	0.25V	0.125V

STEP 5



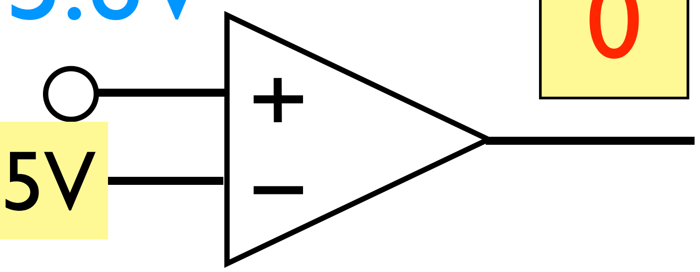
MSB					LSB
1	0	1	1	0	?
4V	2V	1V	0.5V	0.25V	0.125V

SUCCESSIVE APPROXIMATIONS

MSB					LSB
1	0	1	1	0	?
4V	2V	1V	0.5V	0.25V	0.125V

STEP 6

Vx=5.6V

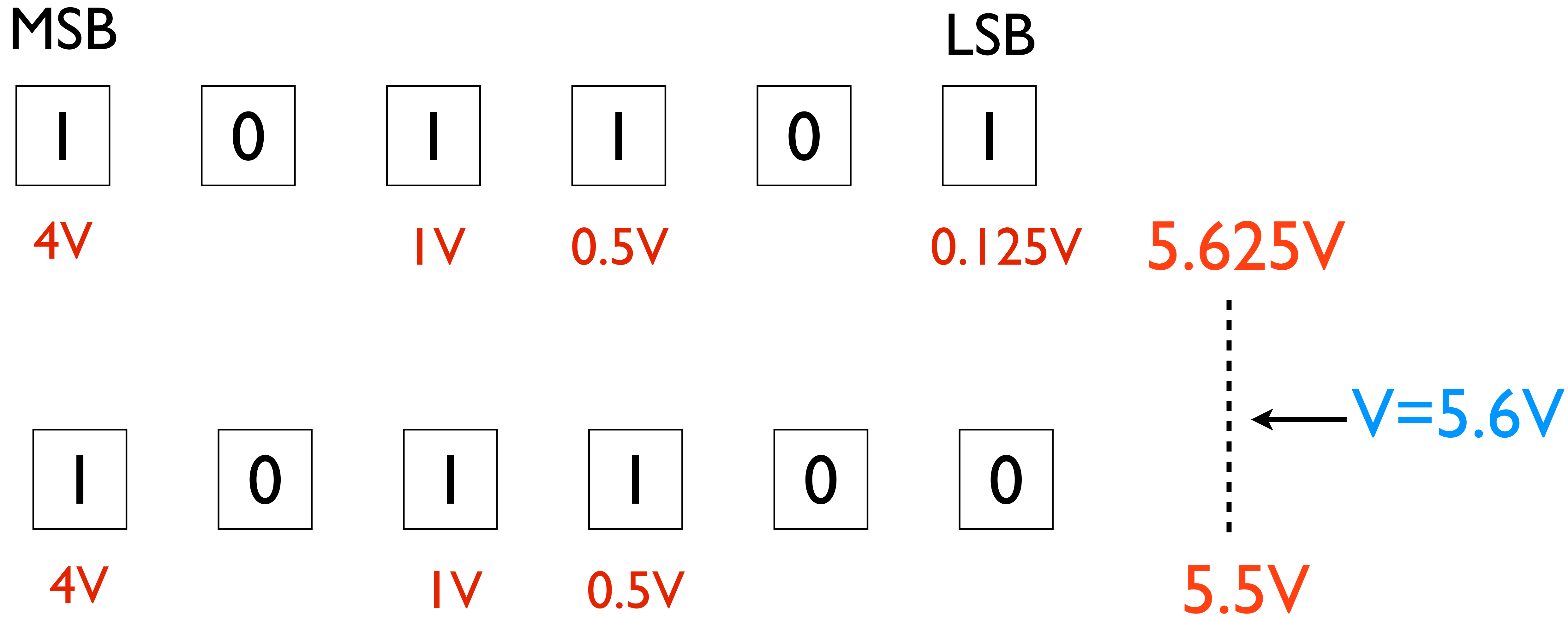


0

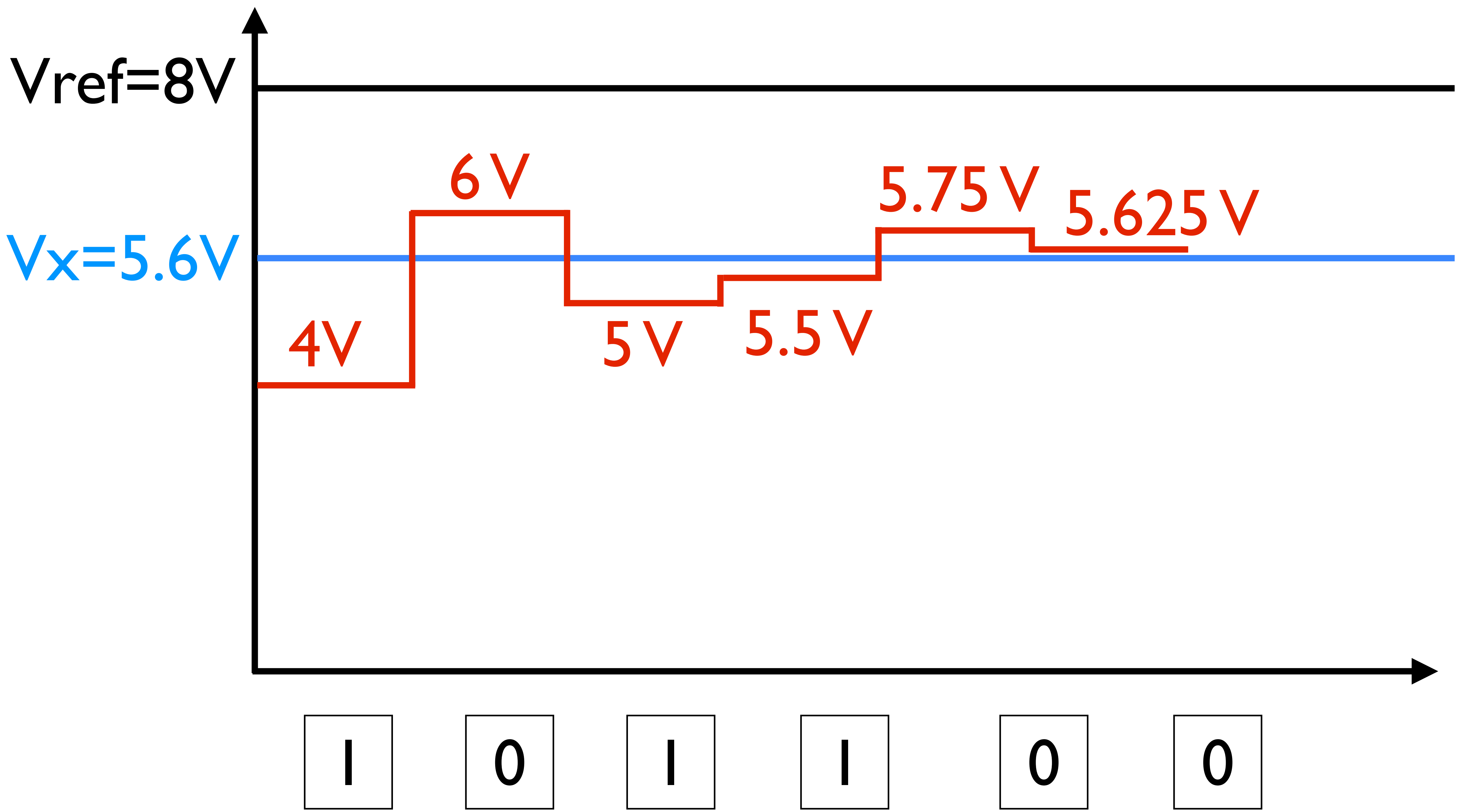
4+1+0.5+0.125=5.625V

MSB					LSB
1	0	1	1	0	0
4V	2V	1V	0.5V	0.25V	0.125V

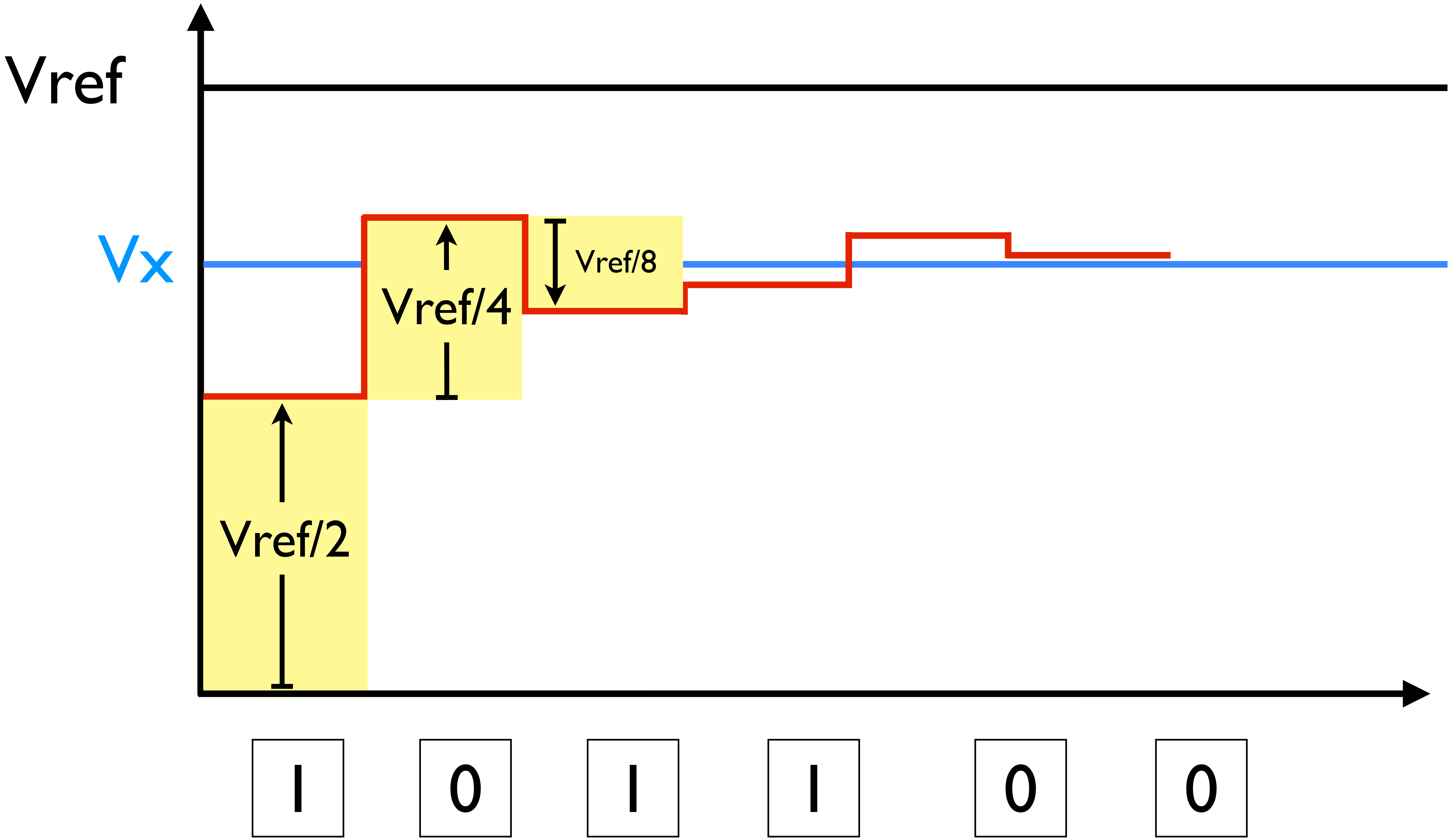
SUCCESSIVE APPROXIMATIONS



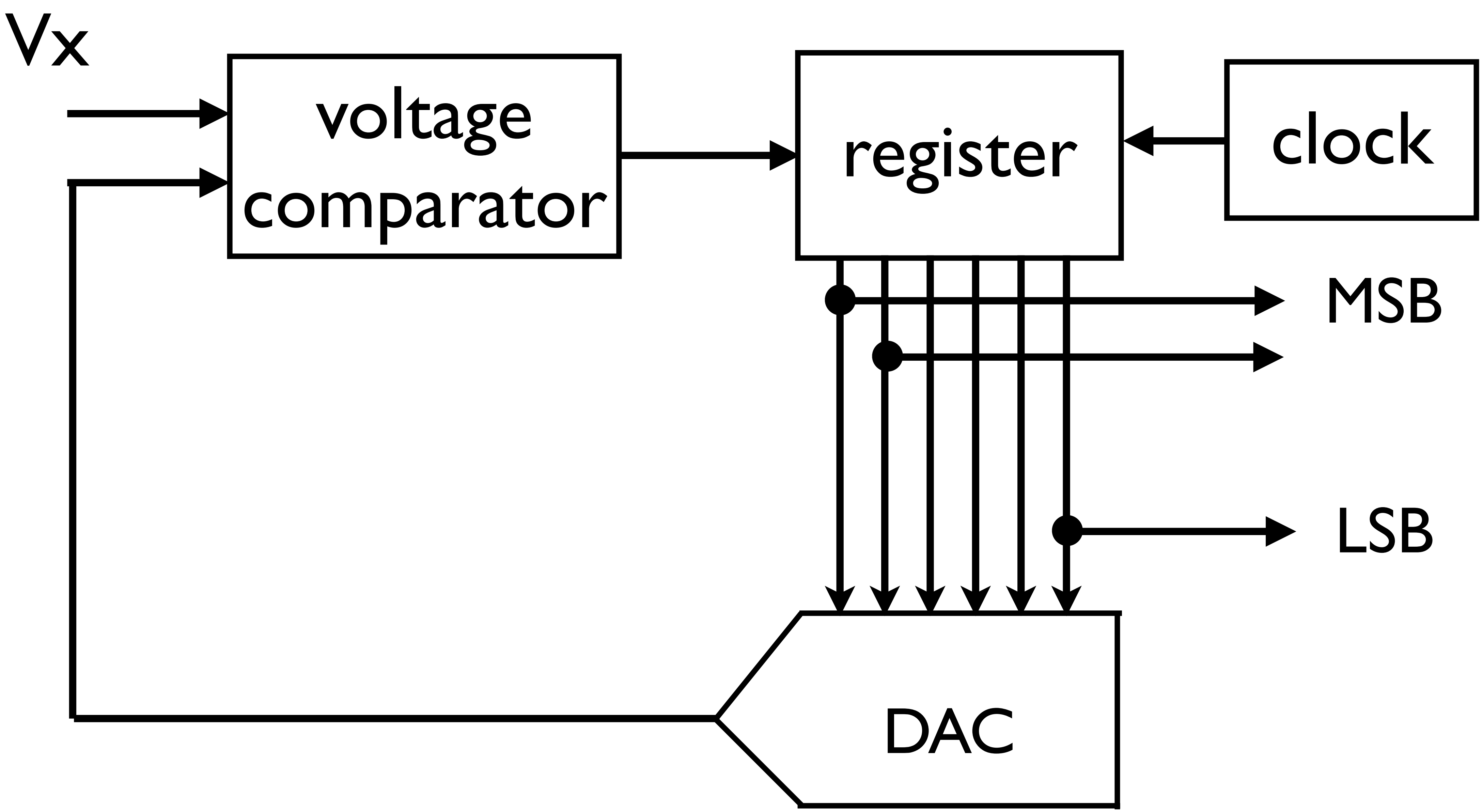
SUCCESSIVE APPROXIMATIONS



SUCCESSIVE APPROXIMATIONS

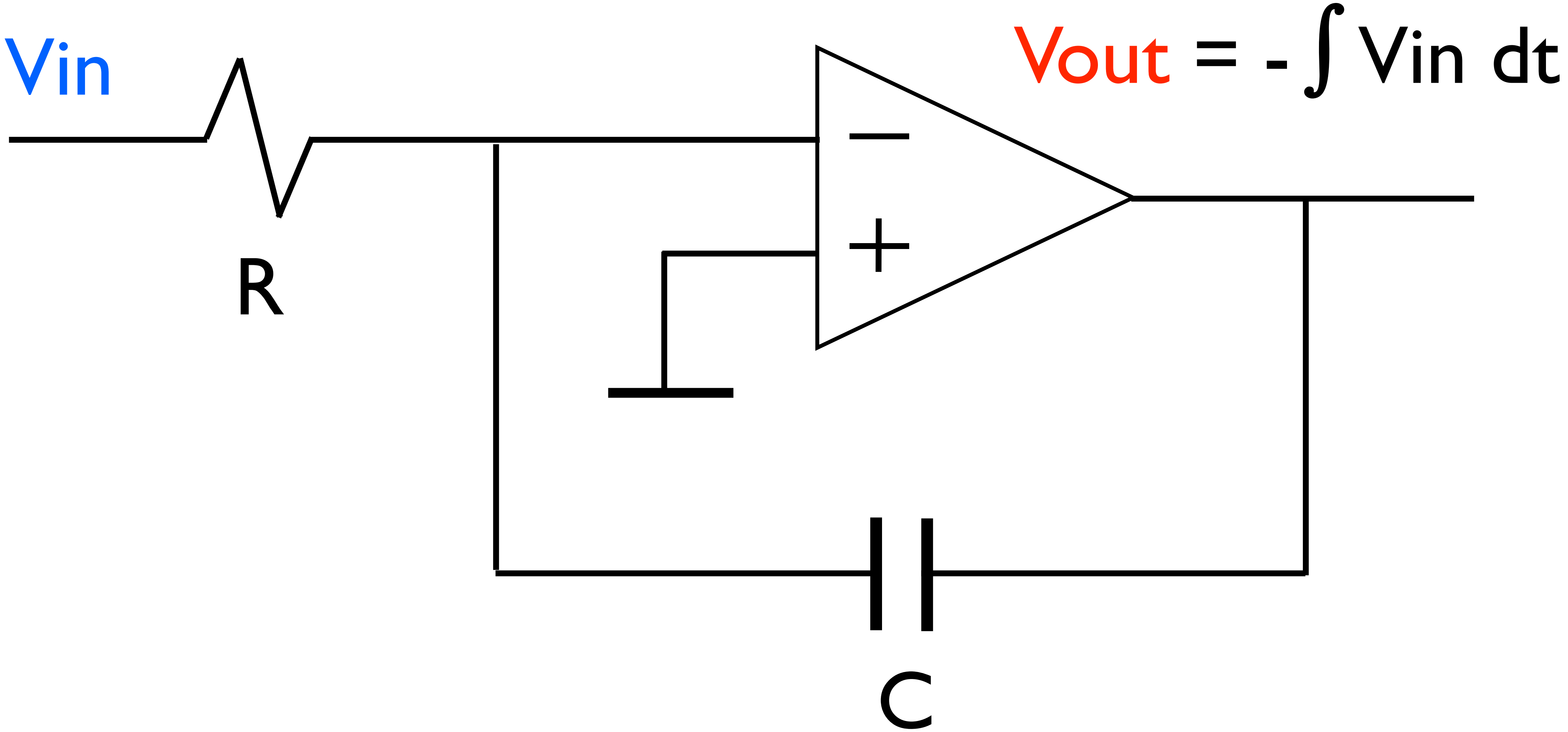


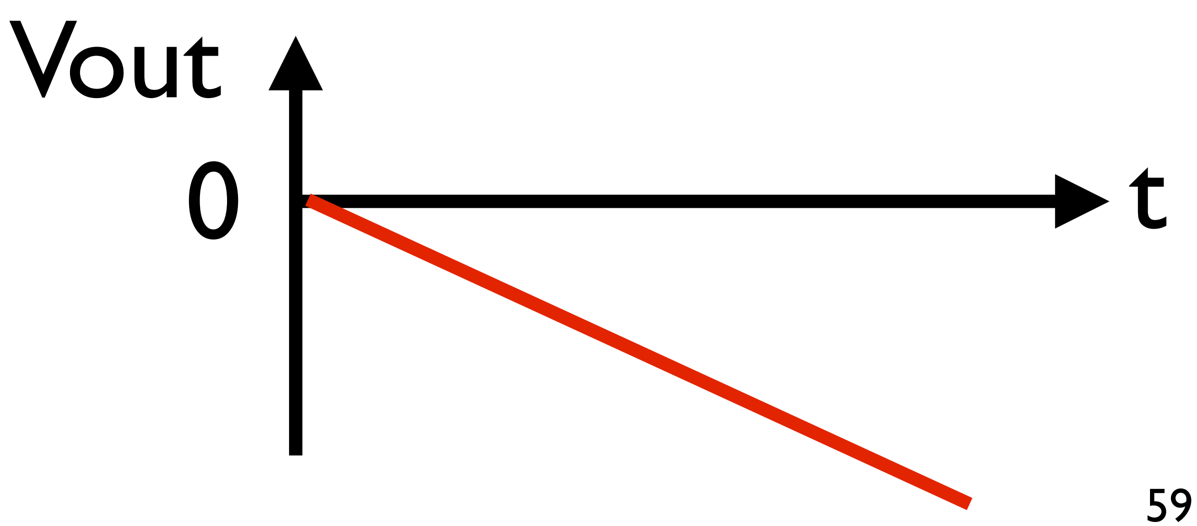
SUCCESSIVE APPROXIMATIONS



Intermediate speed (1 to 10 MHz)
Intermediate resolution (8-16 bits)

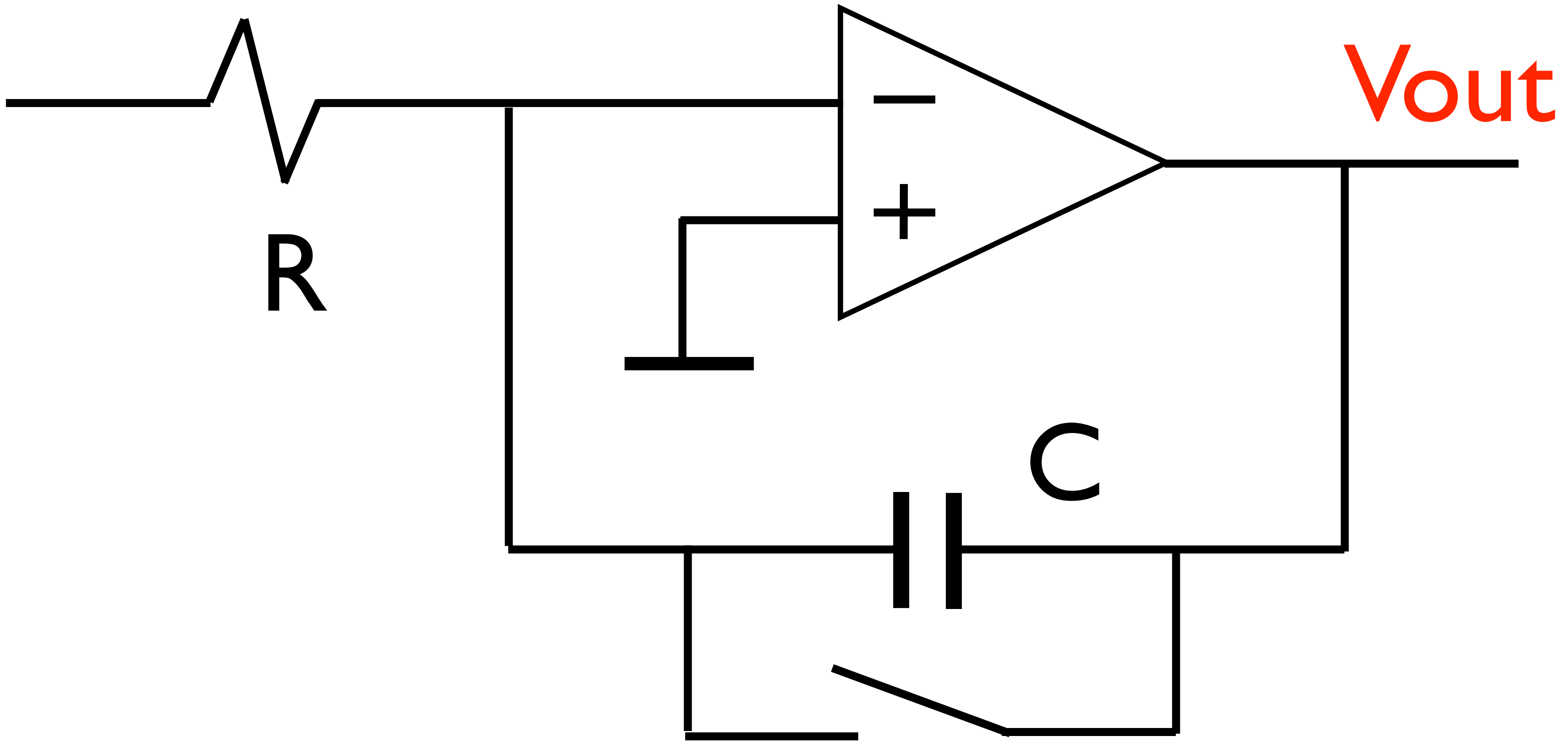
DUAL SLOPE INTEGRATION ADC

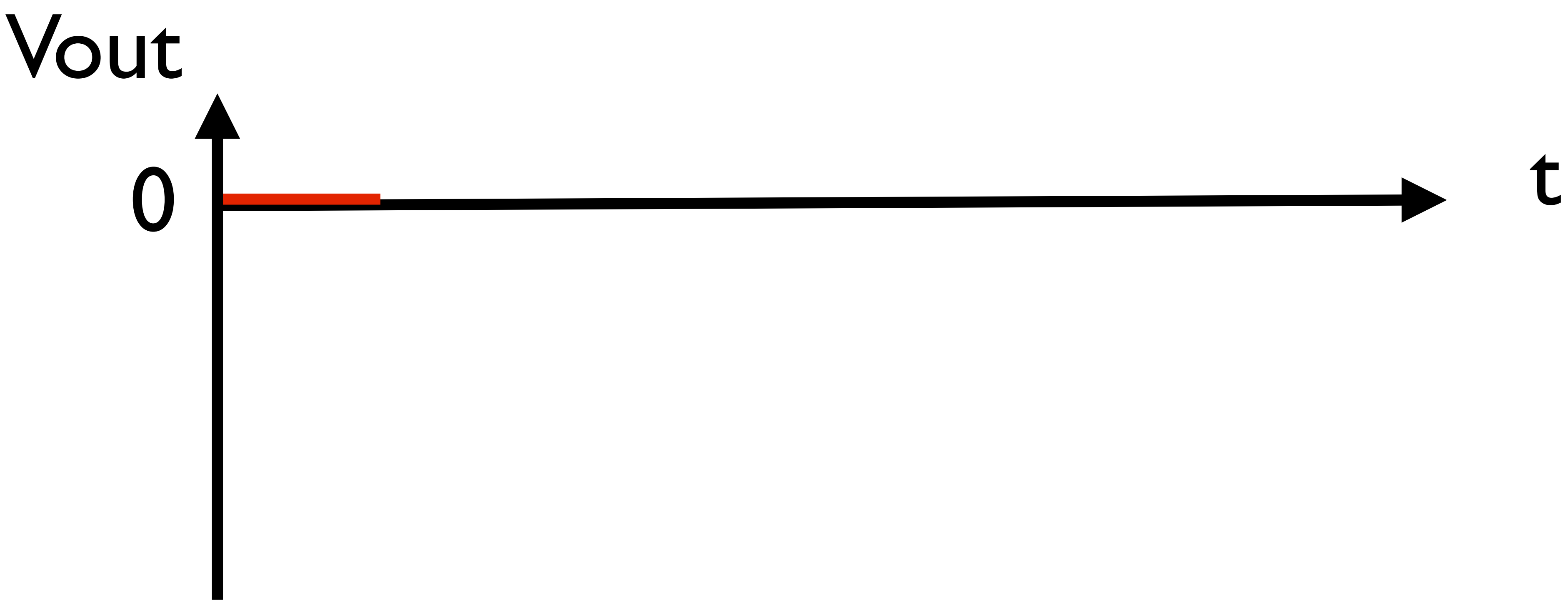




DUAL SLOPE INTEGRATION ADC

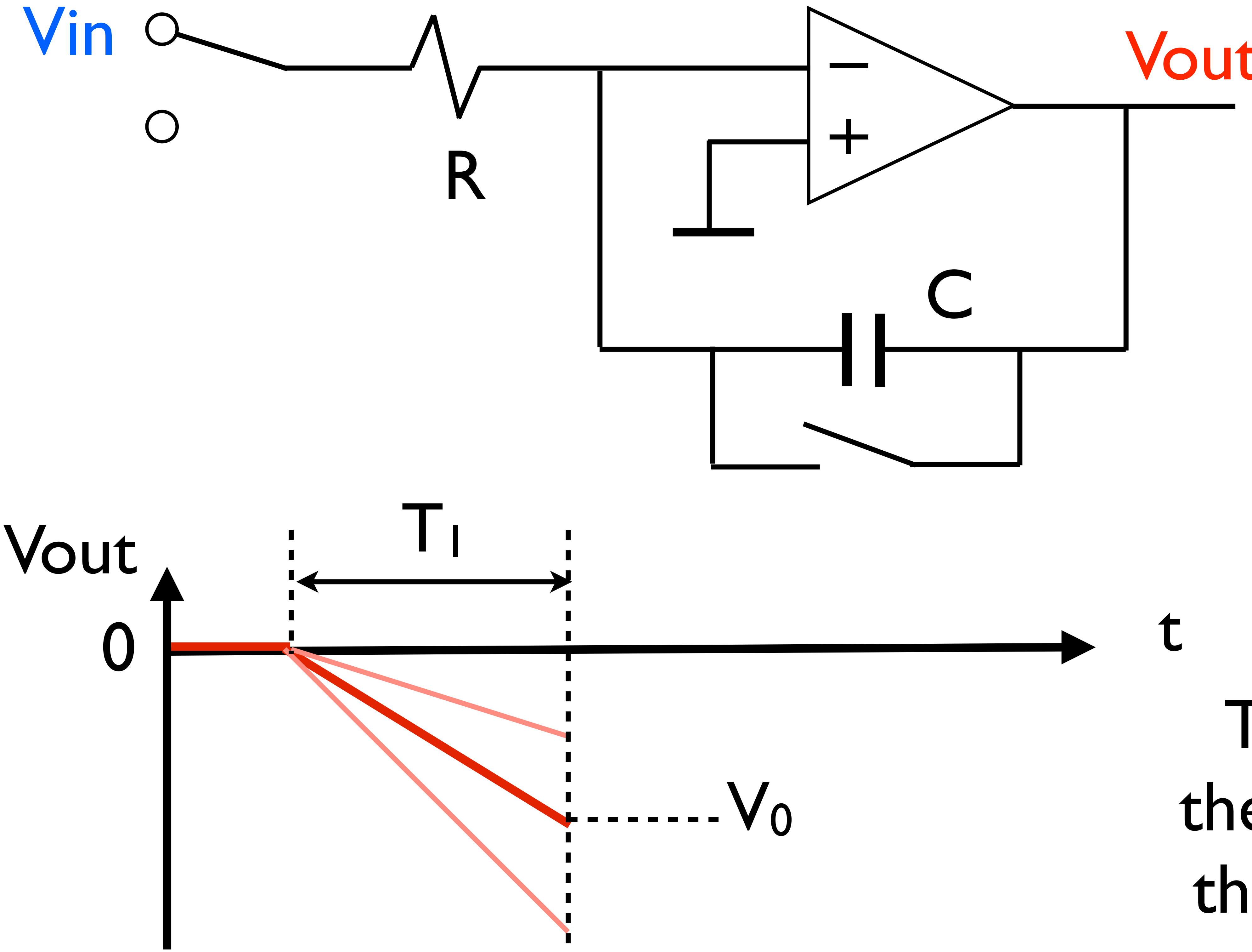
STEP 0





DUAL SLOPE INTEGRATION ADC

STEP 1



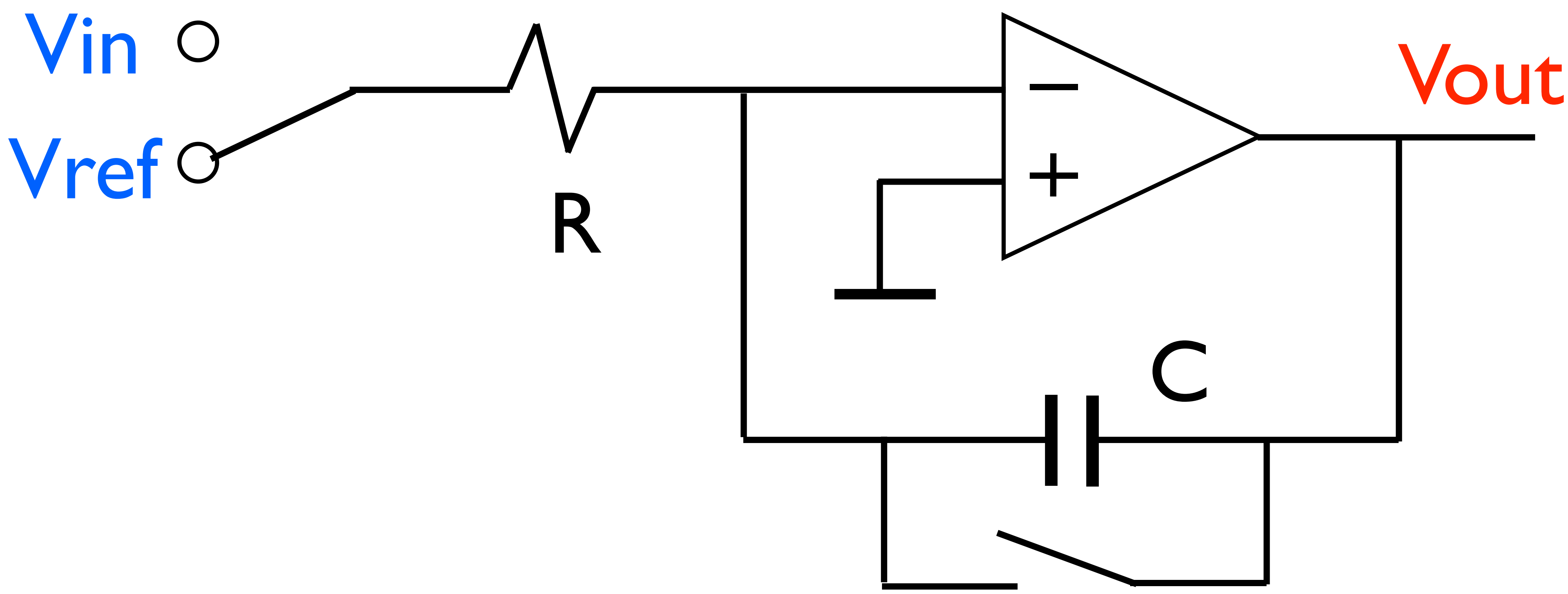
T_1 is constant

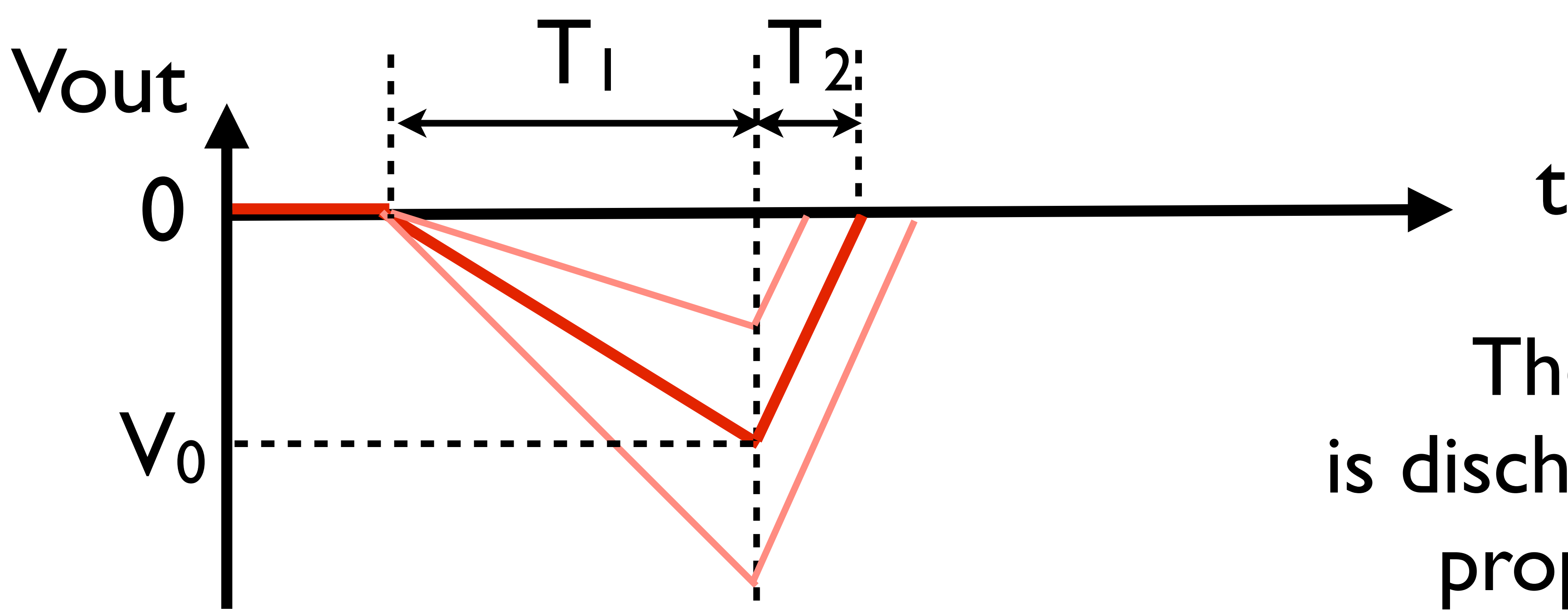
the higher is Vin

the higher is V_0

DUAL SLOPE INTEGRATION ADC

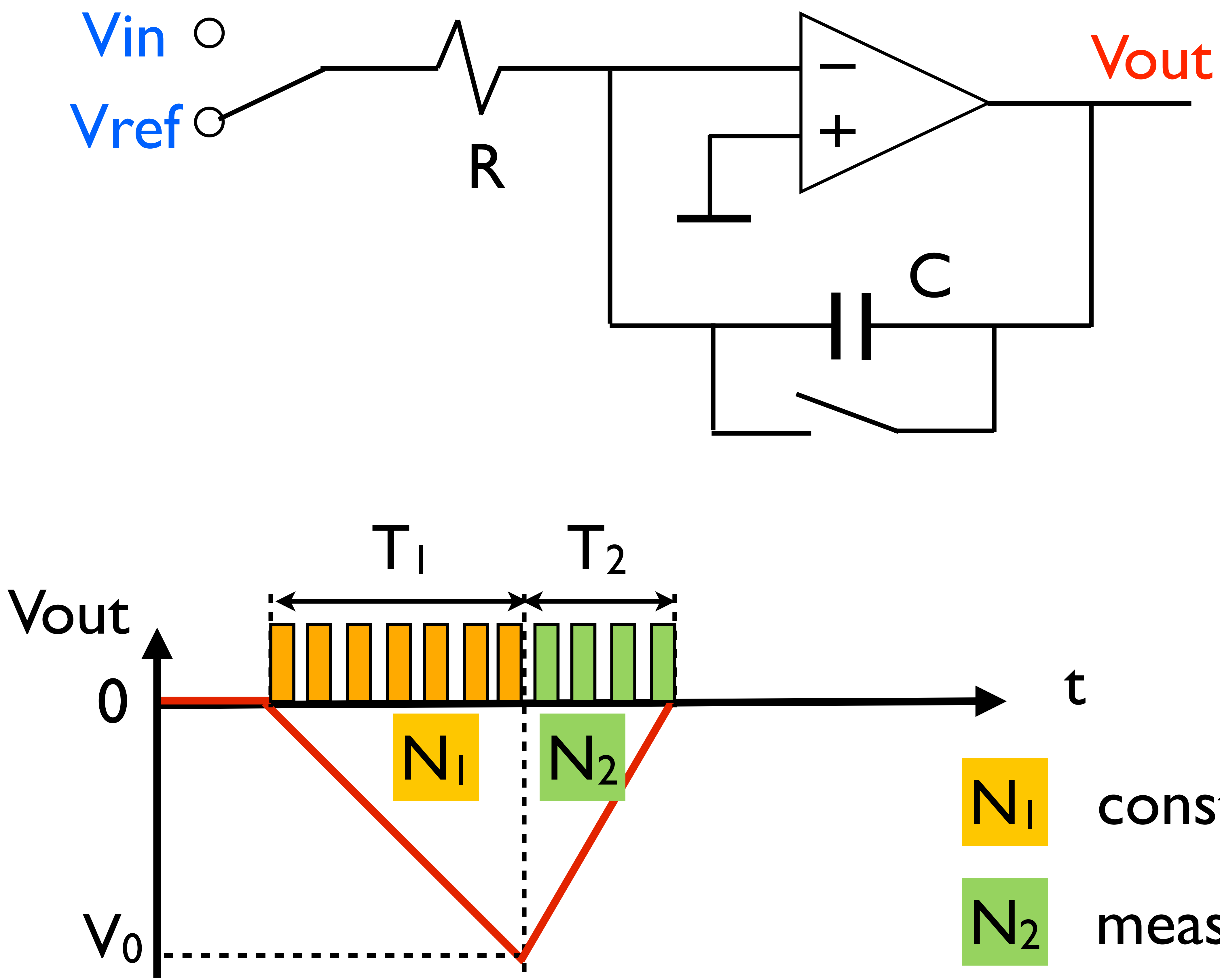
STEP 1





The capacitor C
is discharged in a time T_2
proportional to V_0

DUAL SLOPE INTEGRATION ADC

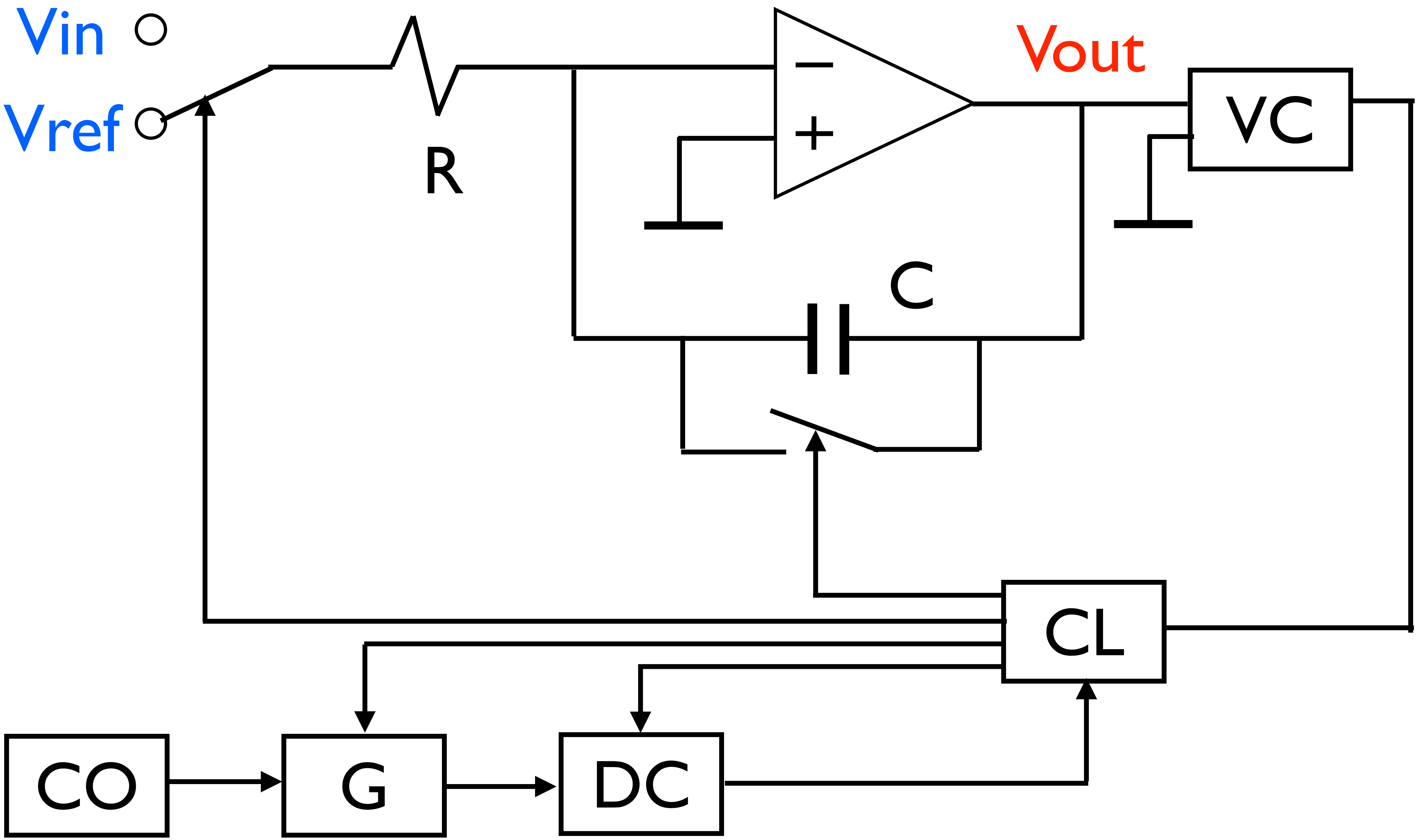


N_1 constant

N_2 measures Vin

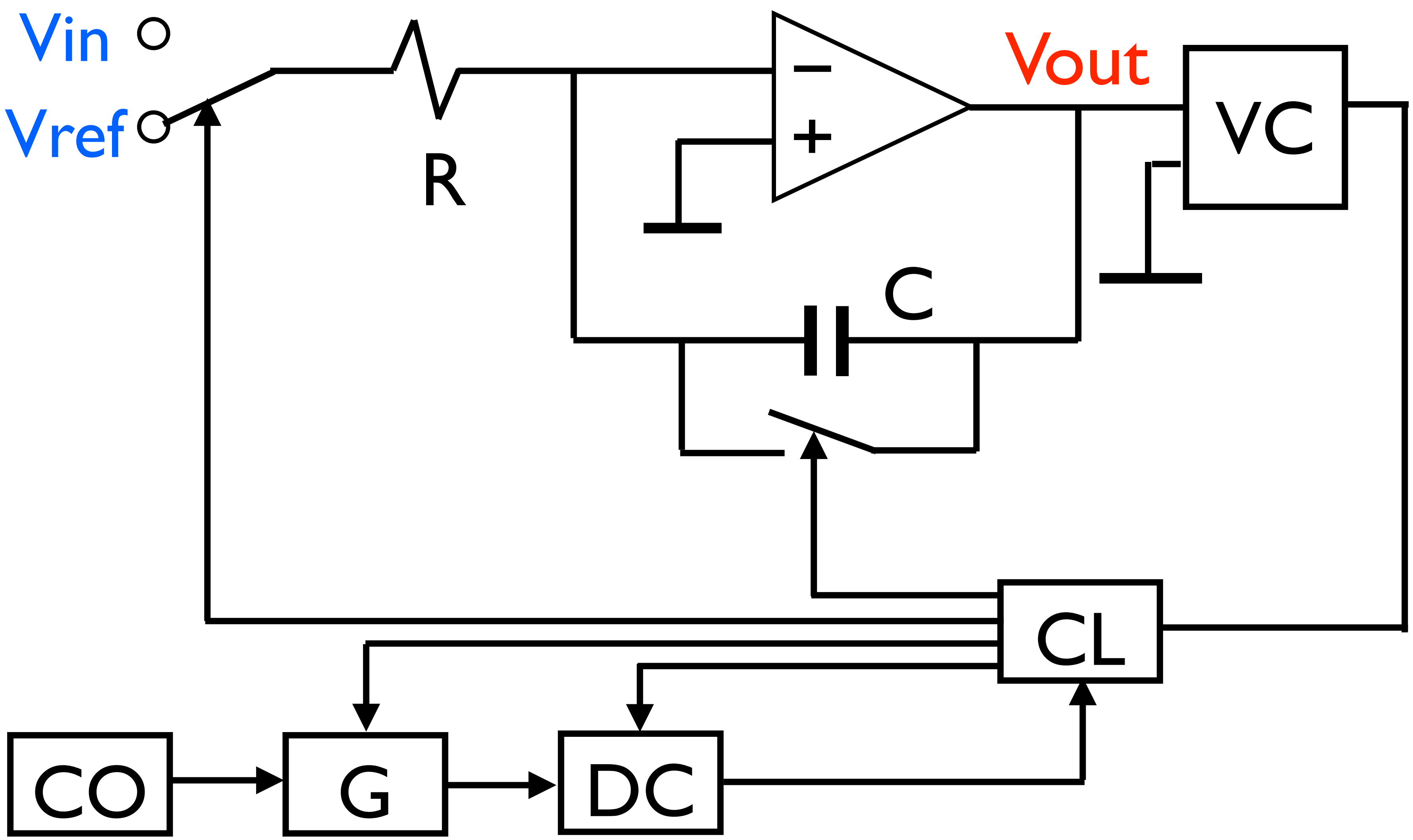
DUAL SLOPE INTEGRATION ADC

Detailed structure



CO= crystal oscillator; G=gate; DC=decimal counter;
CL=control logic; VC=voltage comparator

DUAL SLOPE INTEGRATION ADC



Very precise, but also very slow
Used in multimeters

SIGMA DELTA

Basic idea:

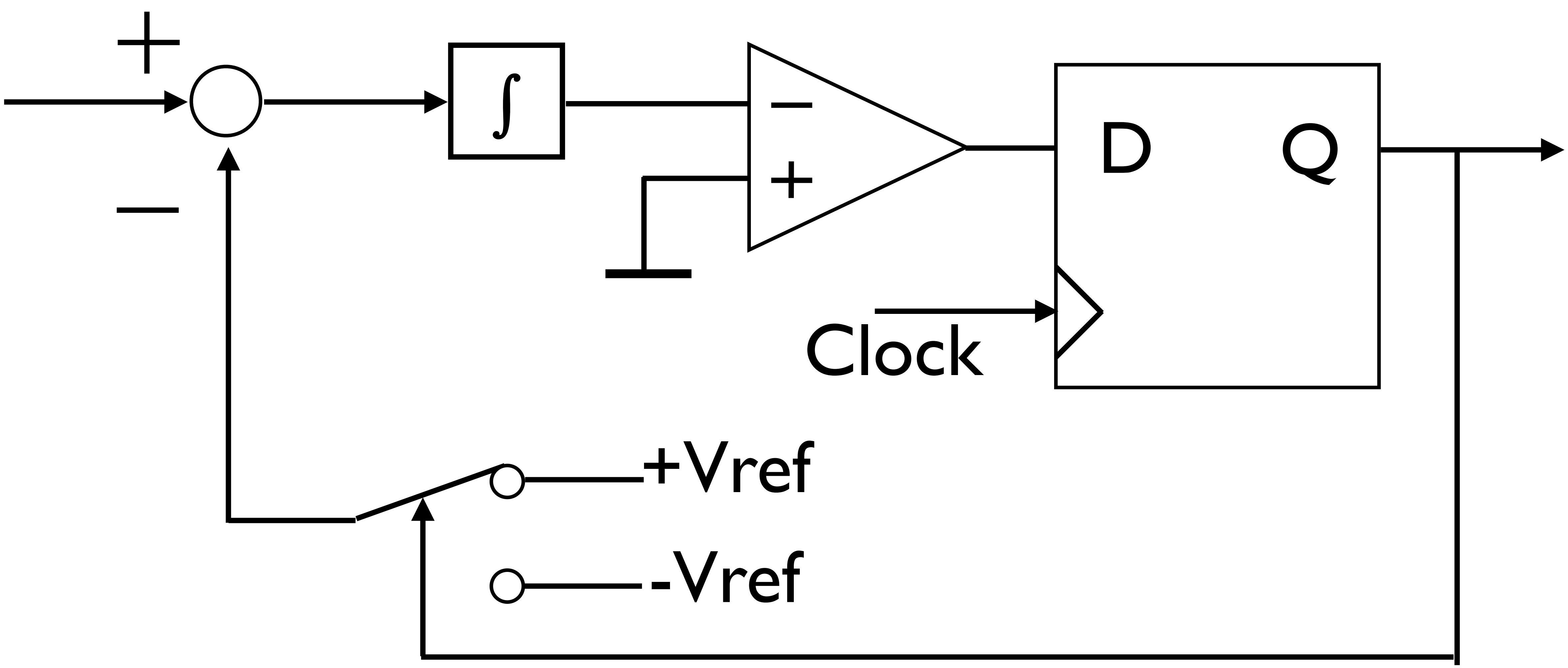
sample the signal with
low resolution
and high sampling frequency

then you can work on the data and obtain
high resolution
with low sampling frequency

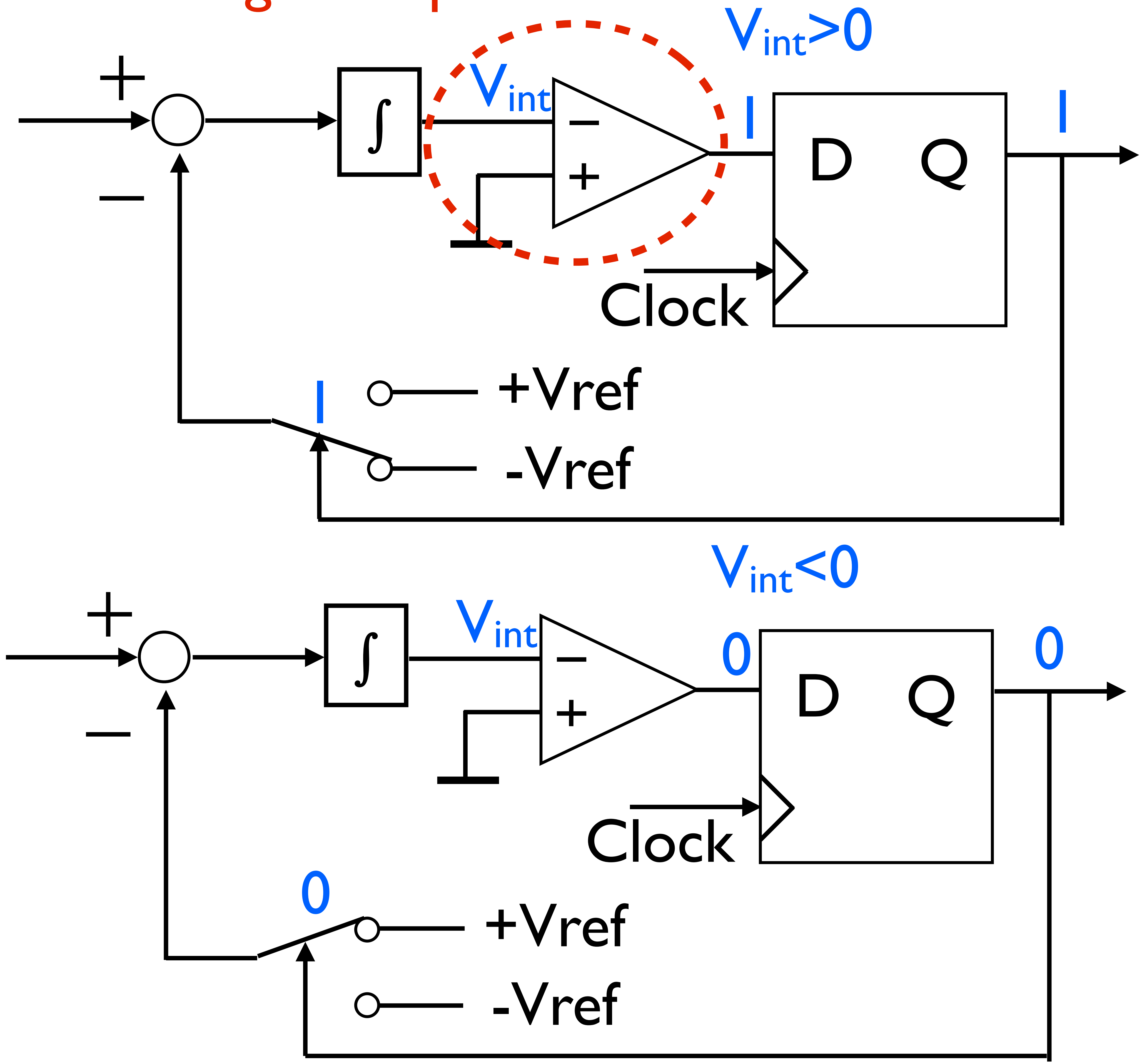
SIGMA DELTA

One bit sampling with ultra high sampling frequency

Structure



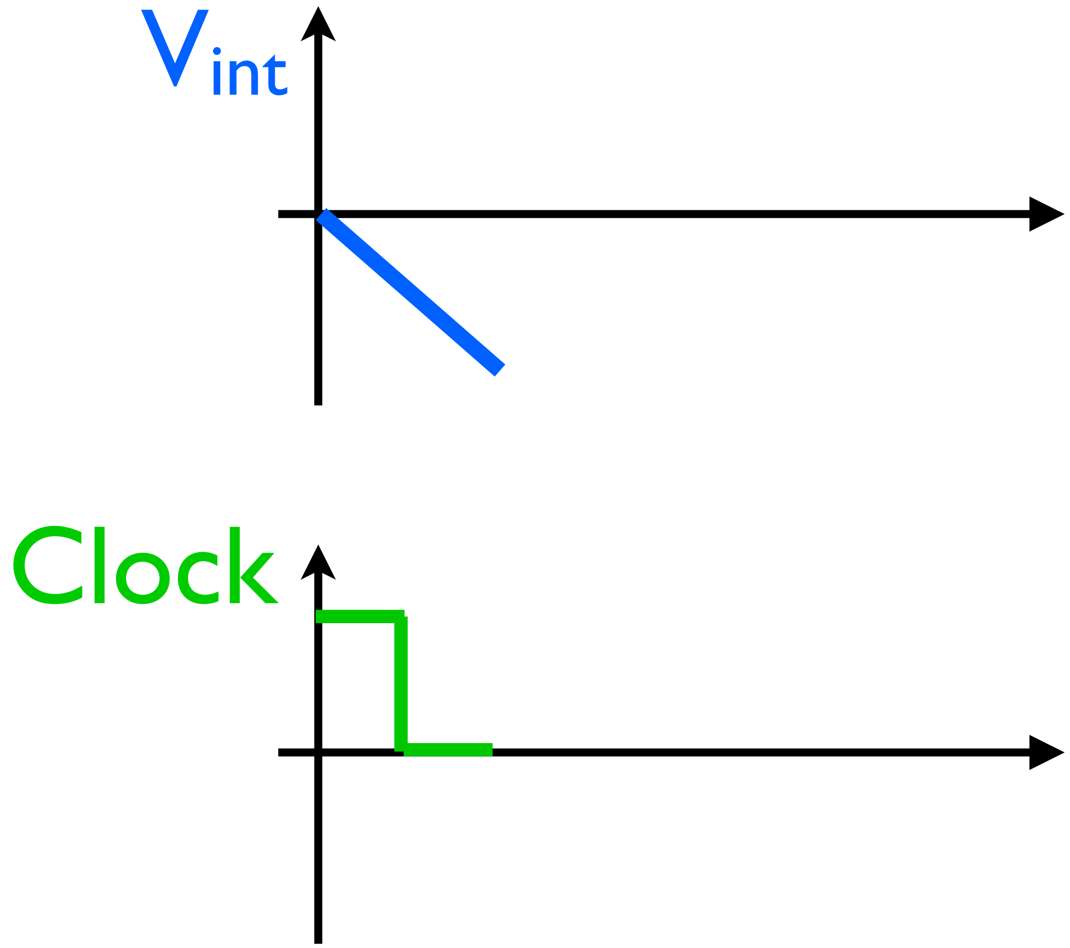
Voltage comparator

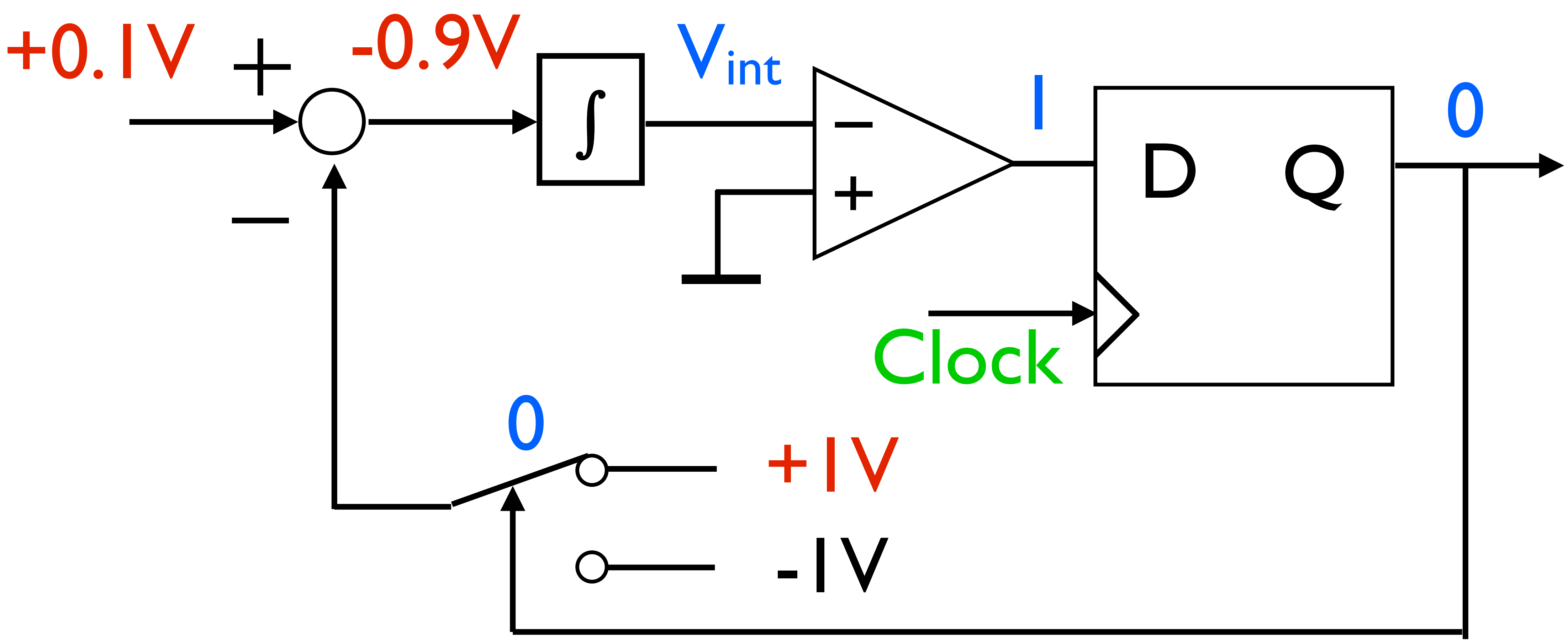


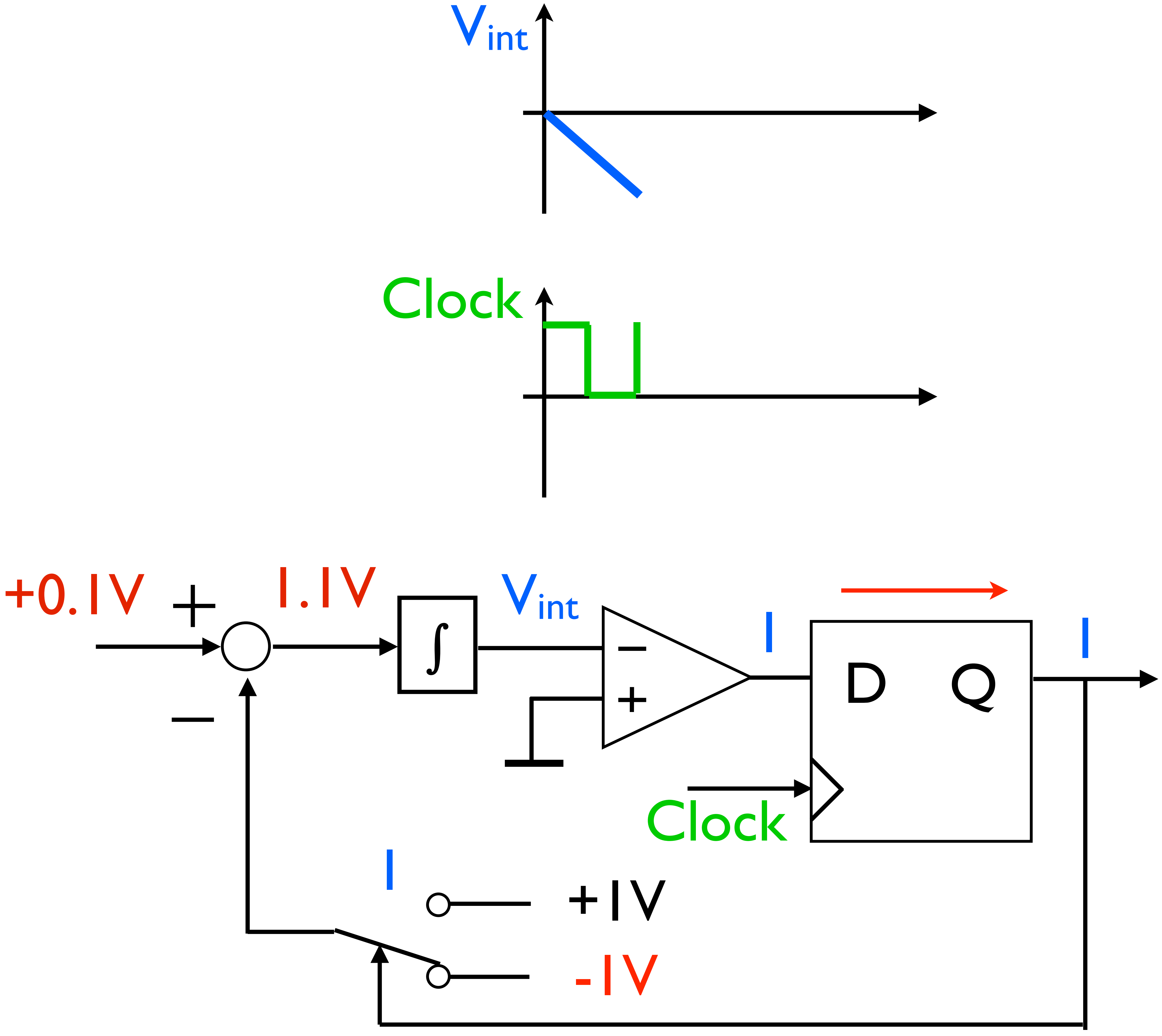
Initial condition:

integrator=0

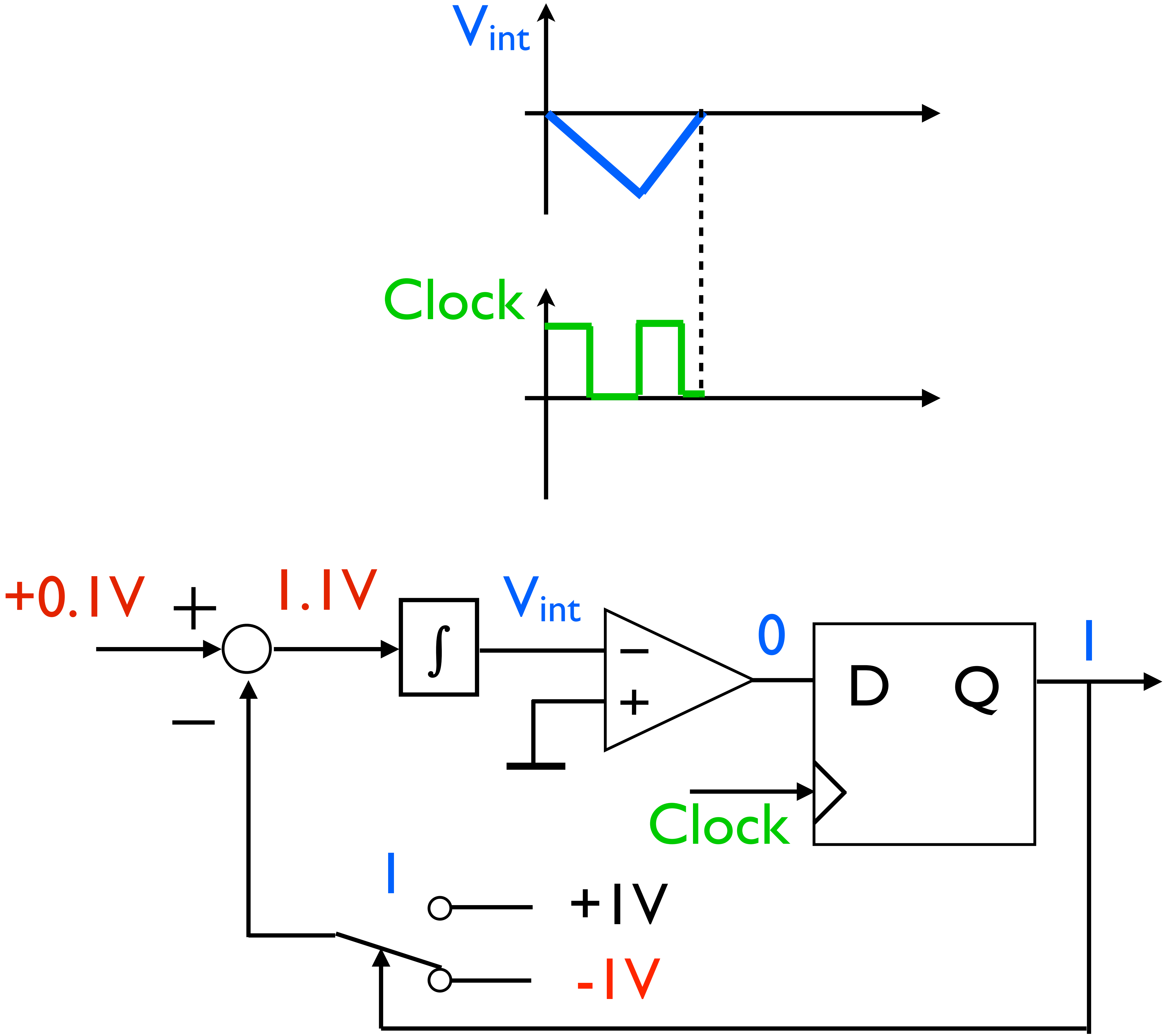
Q=0

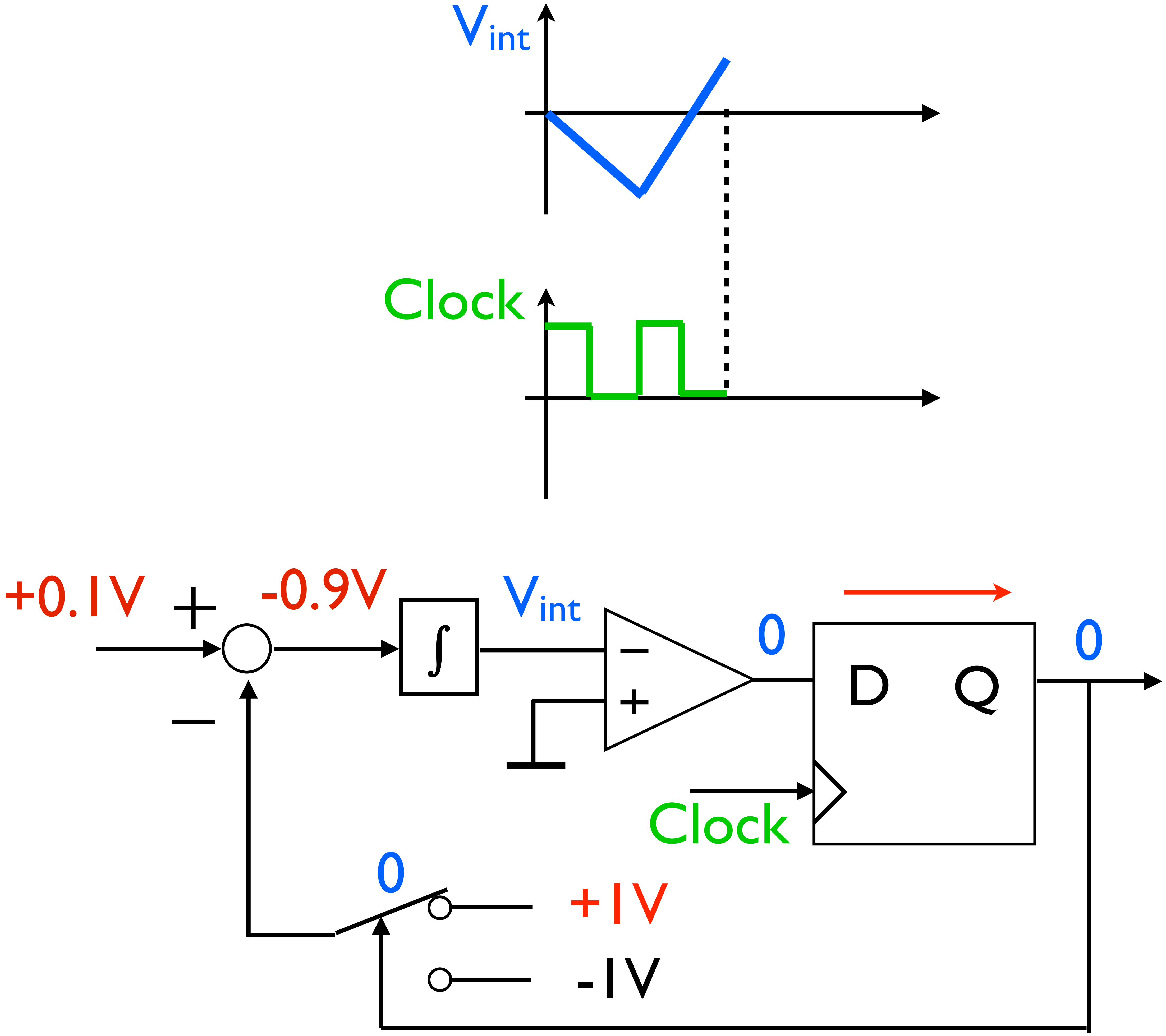


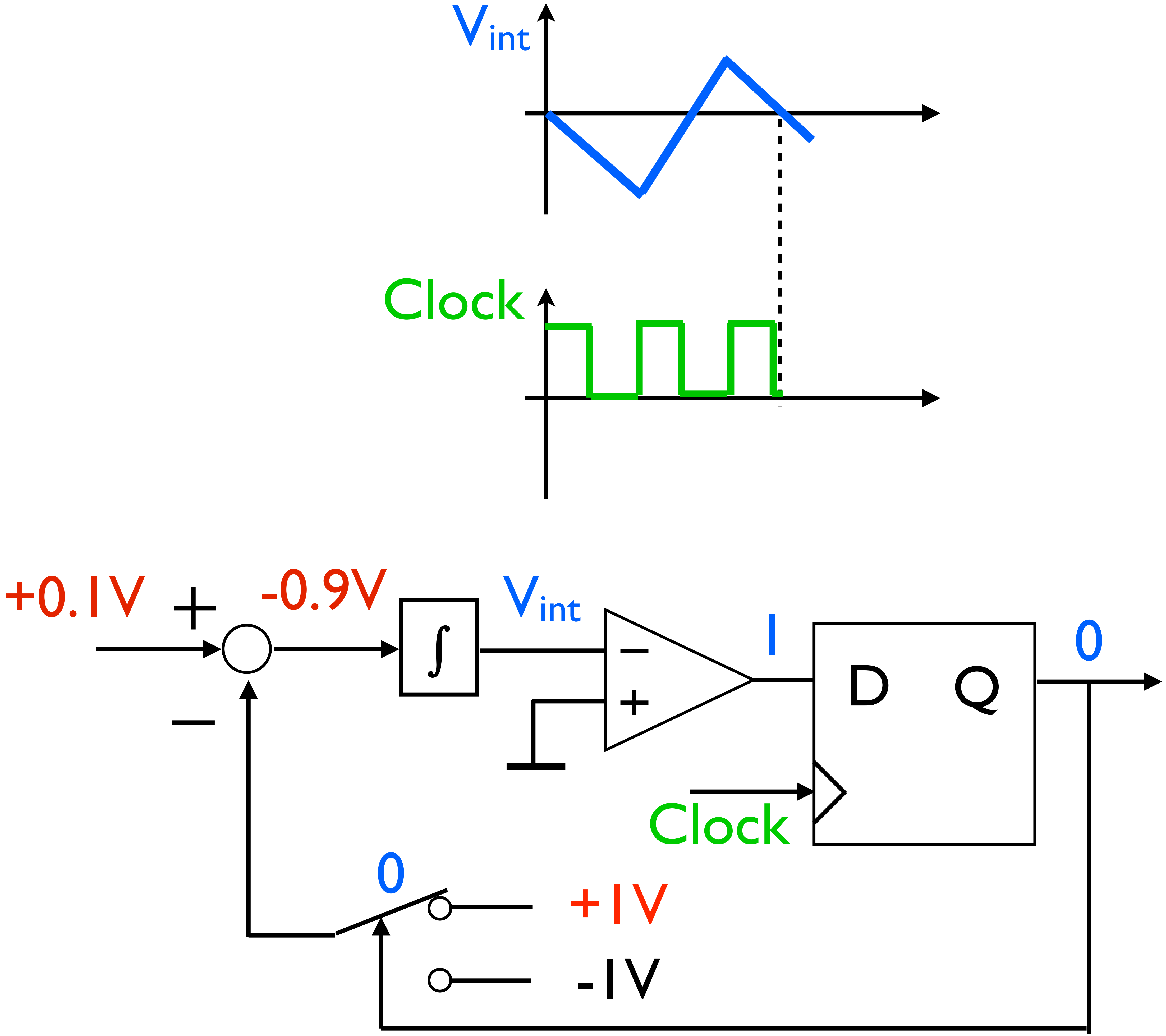




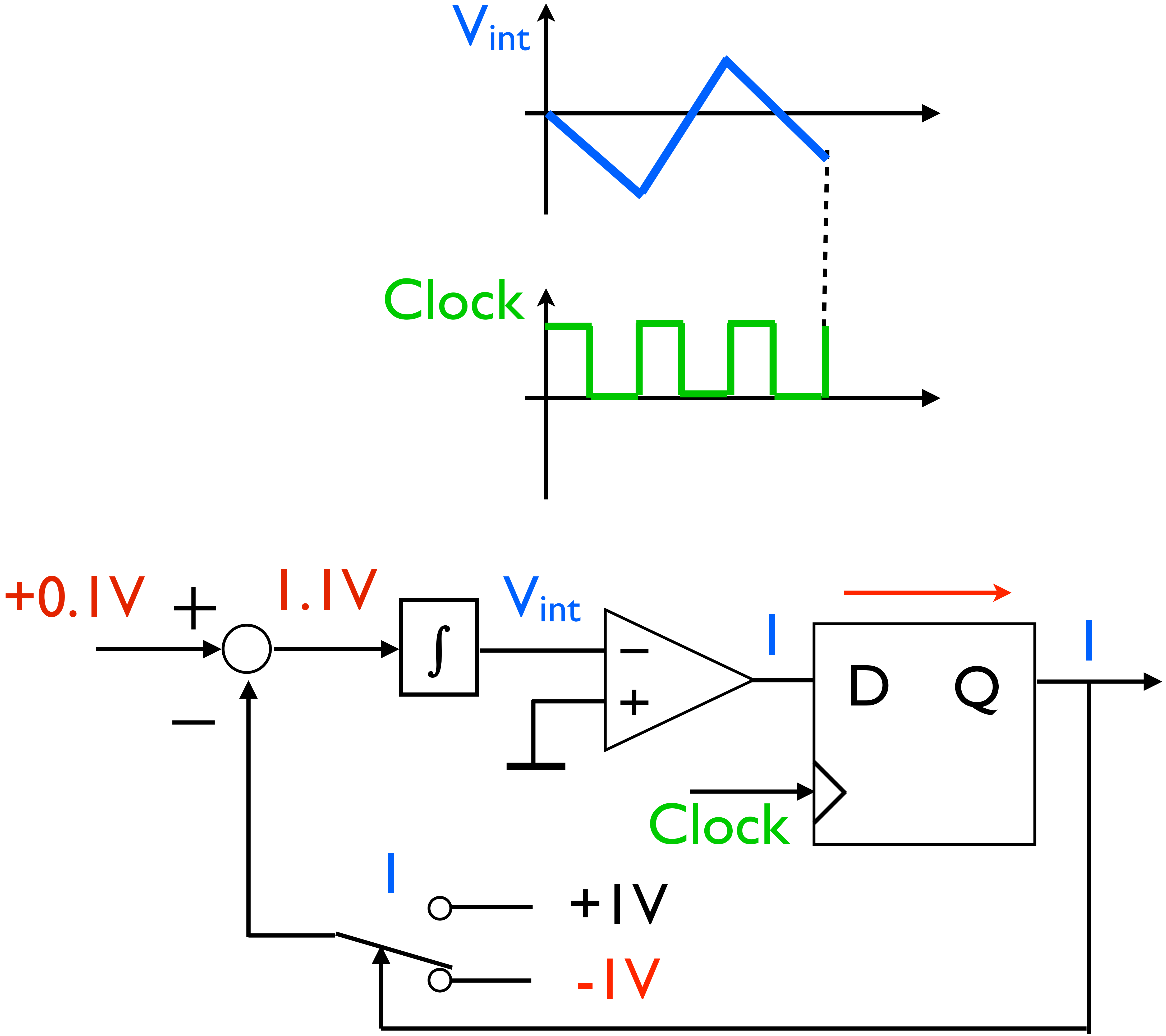
Vint
Clock
+0.1V
+
1.1V
–
∫
Vint
–
+
1
D
Q
1
Clock
1
+1V
-1V


V_int
Clock
+0.1V
+
−
1.1V
∫
V_int
−
+
0
D
Q
1
Clock
1
+1V
-1V

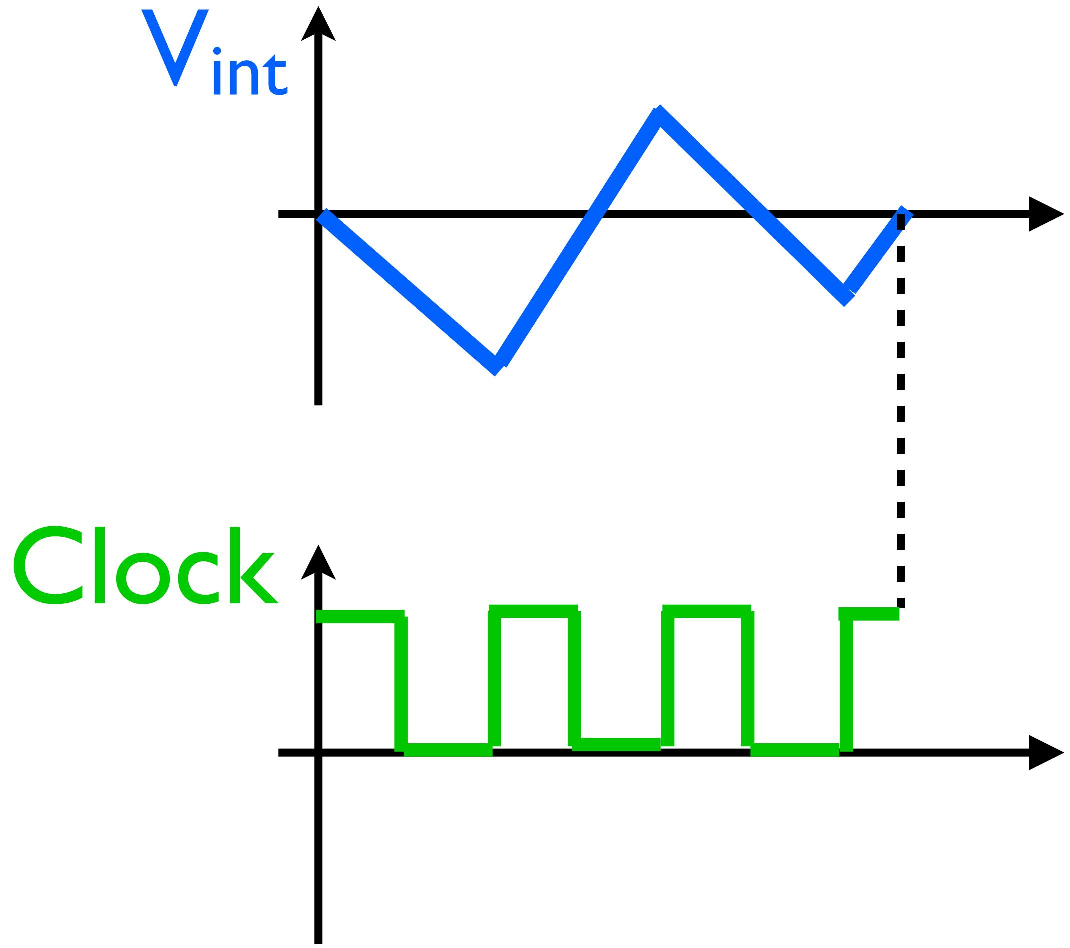

V_{int}
Clock
+0.1V
+
-0.9V
∫
V_{int}
−
+
0
D
Q
0
−
Clock
0
+1V
-1V

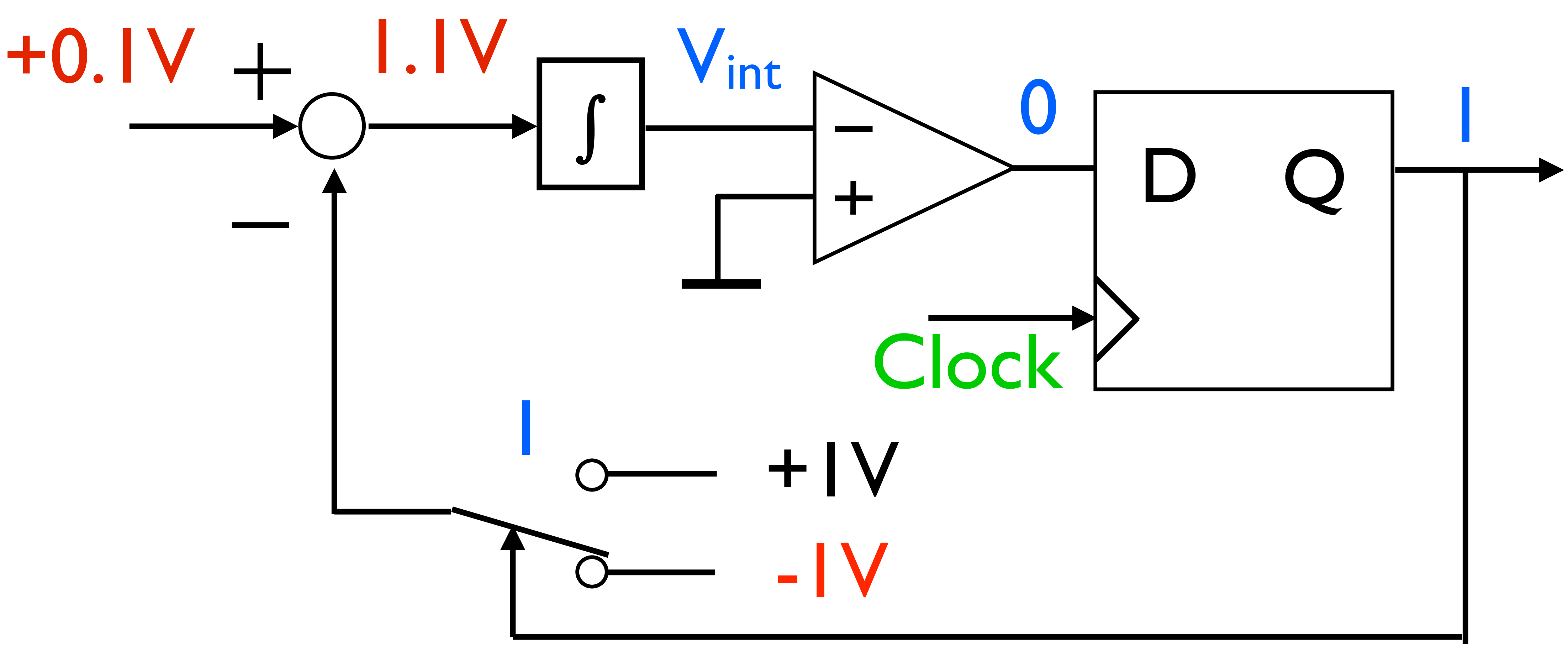


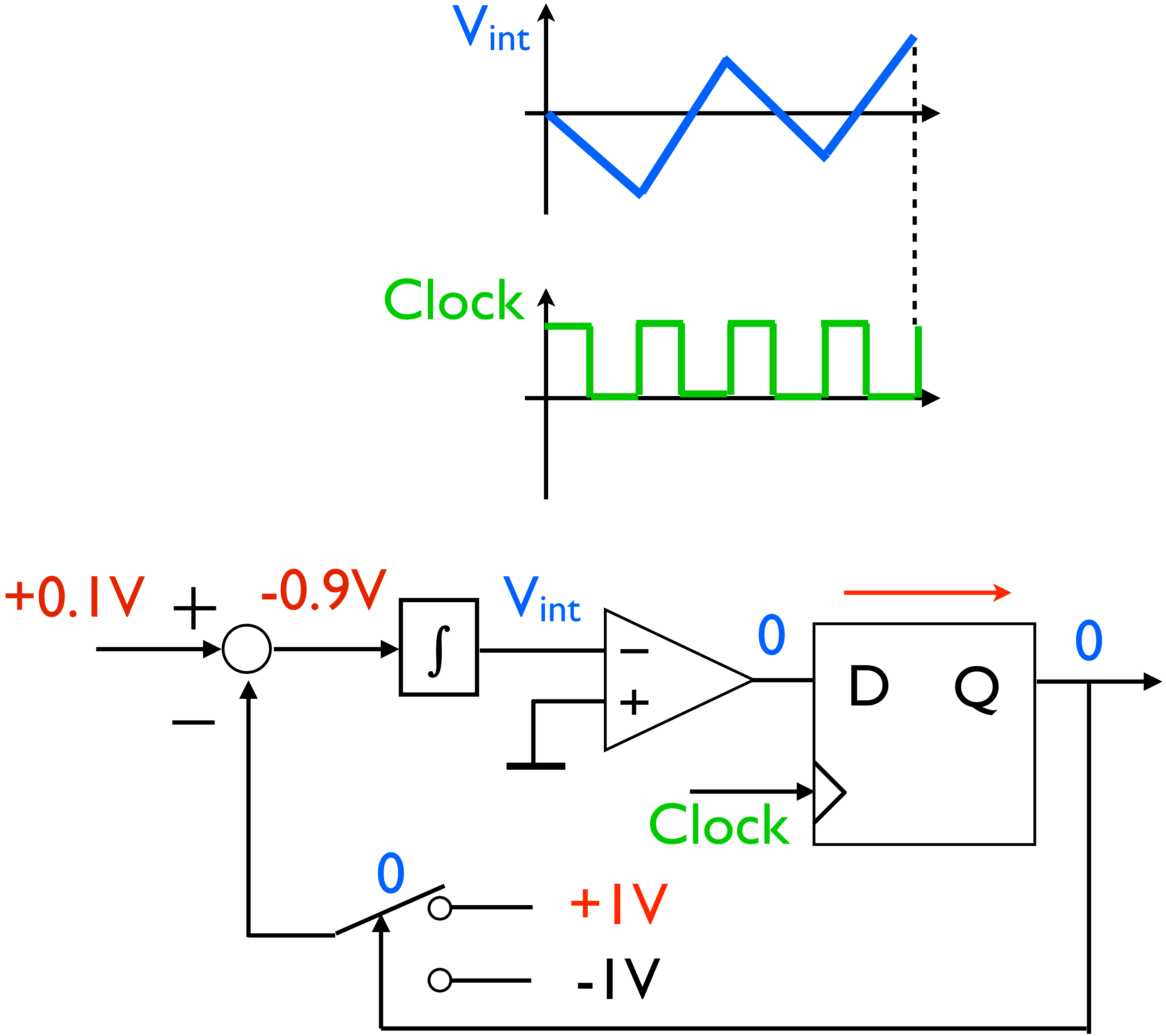
Vint
Clock
+0.1V
+
-0.9V
Vint
1
D
Q
0
–
Clock
0
+1V
-1V

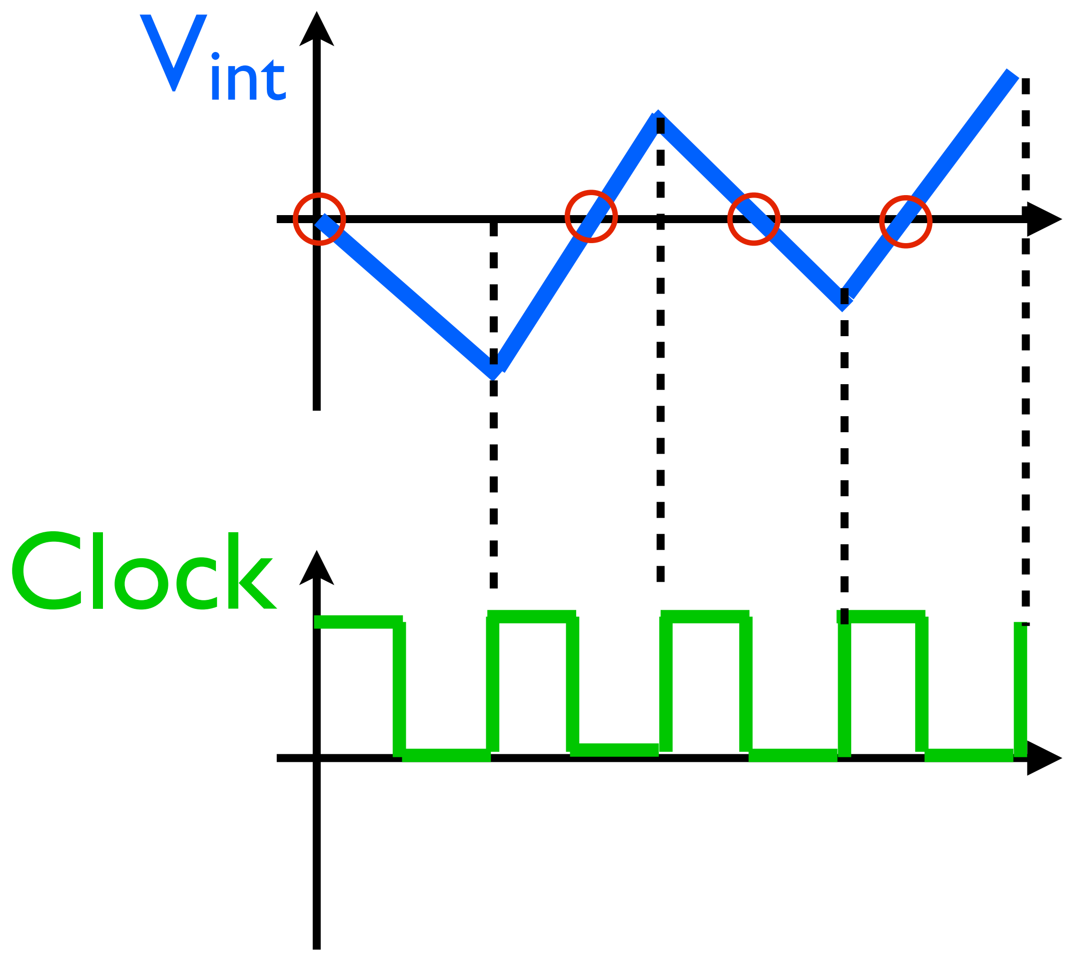


Vint
Clock
+0.1V
+
1.1V
−
Vint
−
+
1
D
Q
1
Clock
1
+1V
-1V

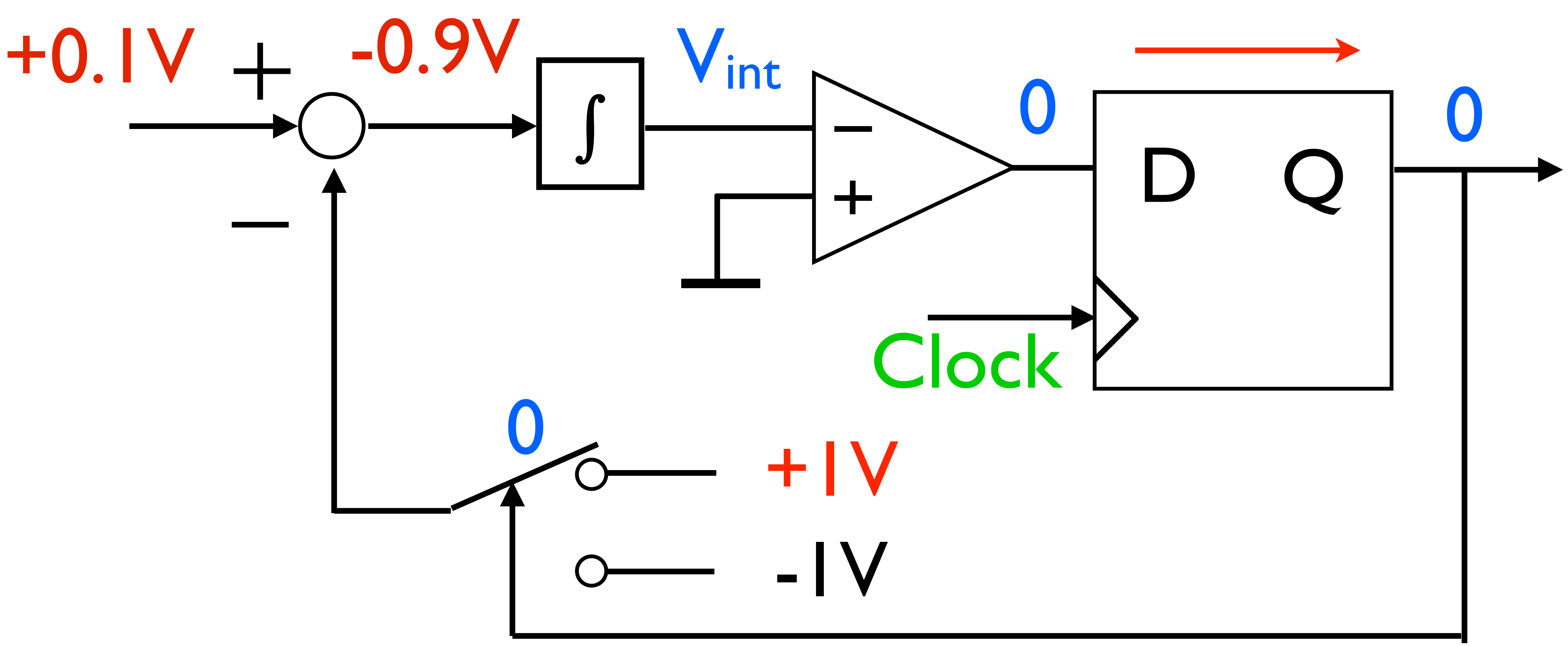

V_{int}
Clock


+0.1V
+
−
1.1V
V_{int}
∫
−
+
0
D
Q
1
Clock
1
+1V
-1V


V_int
Clock
+0.1V
+
-0.9V
∫
V_int
0
D
Q
0
−
−
+
Clock
0
+1V
-1V



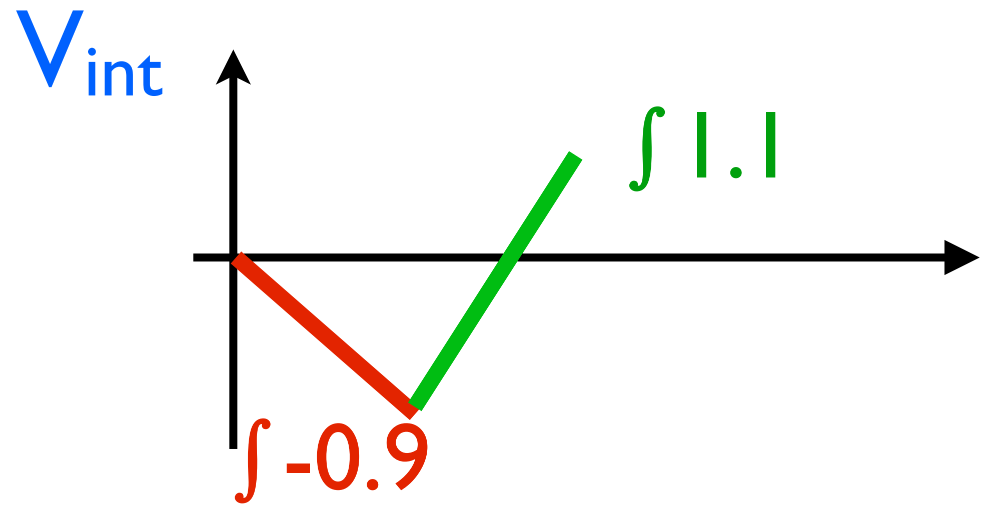
Q inverts its status at every rising edge following a change of sign of Vint



Ex. Vref=1V

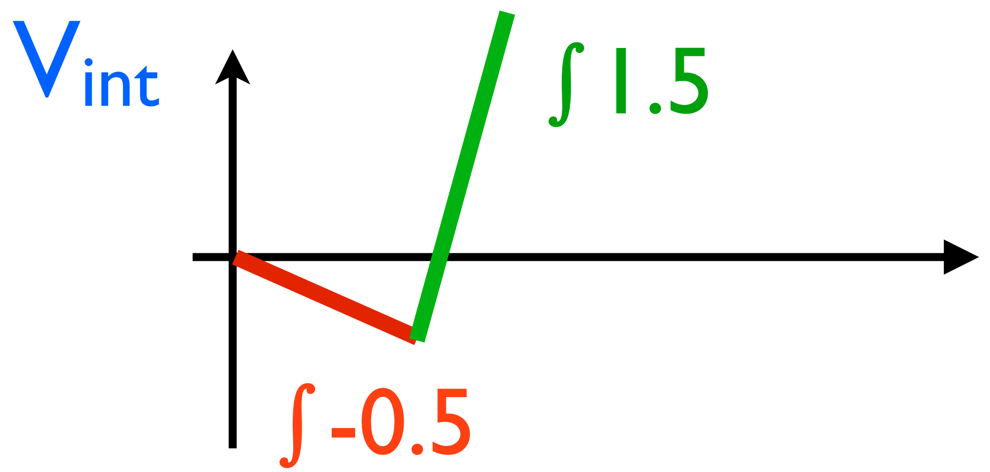
Vi=0.1V

Vdiff=1.1
Vdiff=-0.9



Vi=0.5V

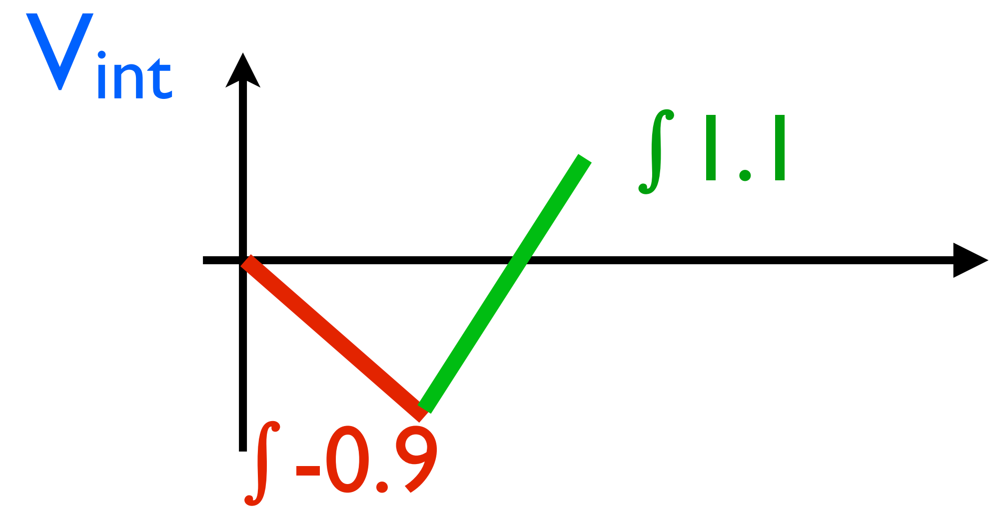
Vdiff=1.5
Vdiff=-0.5

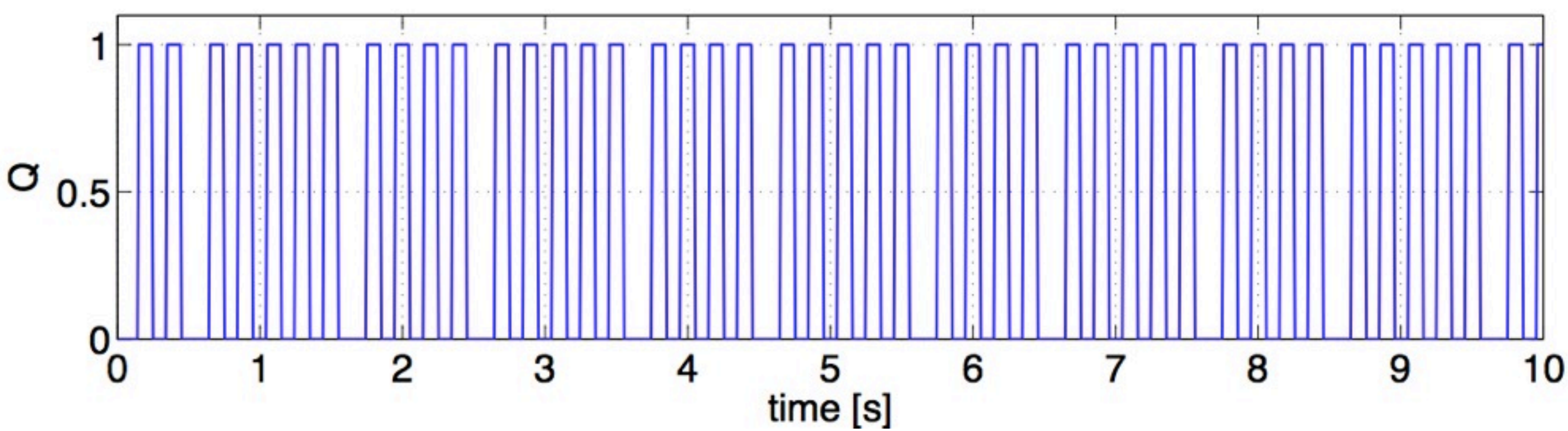


Vi=0.1V

Vdiff=1.1

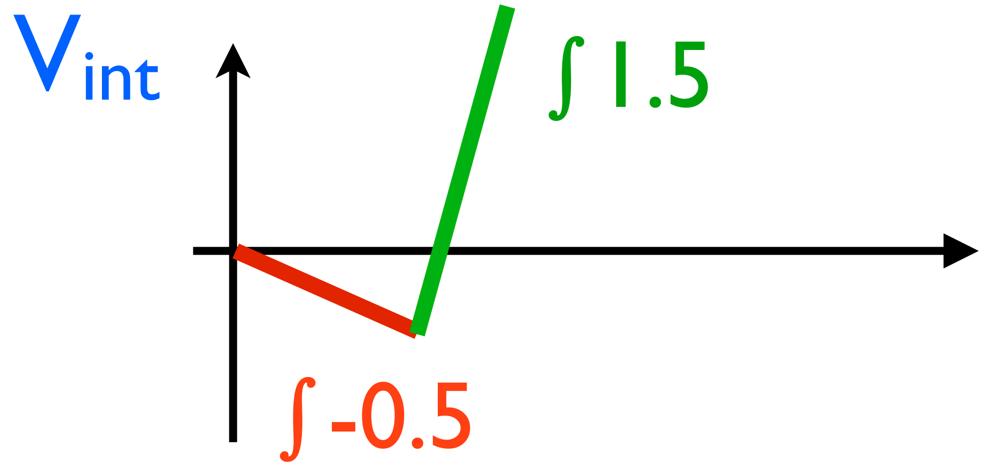
Vdiff=-0.9

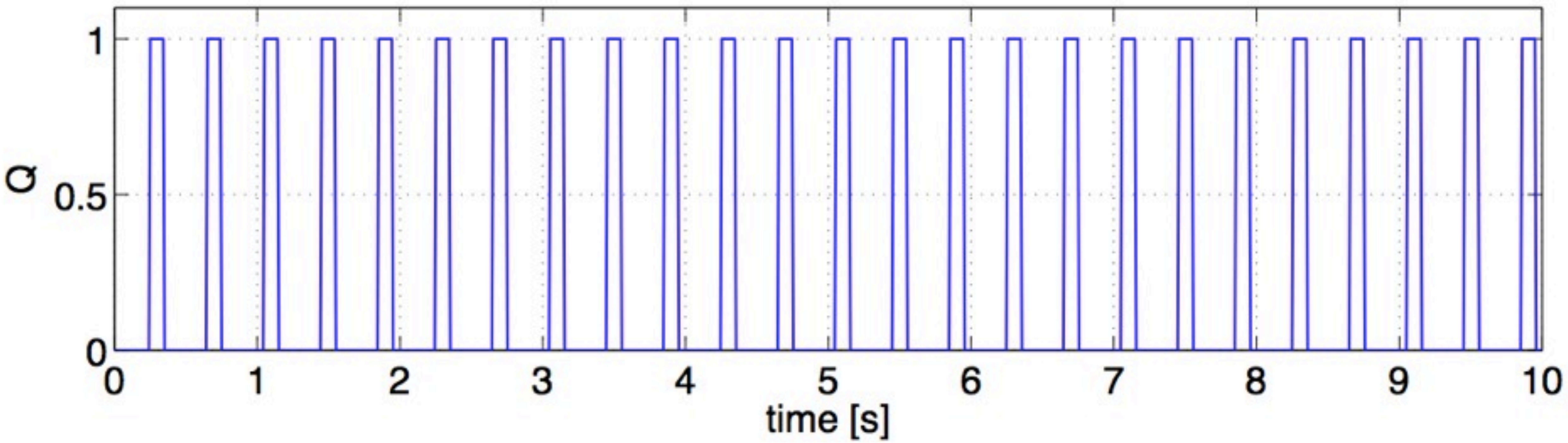




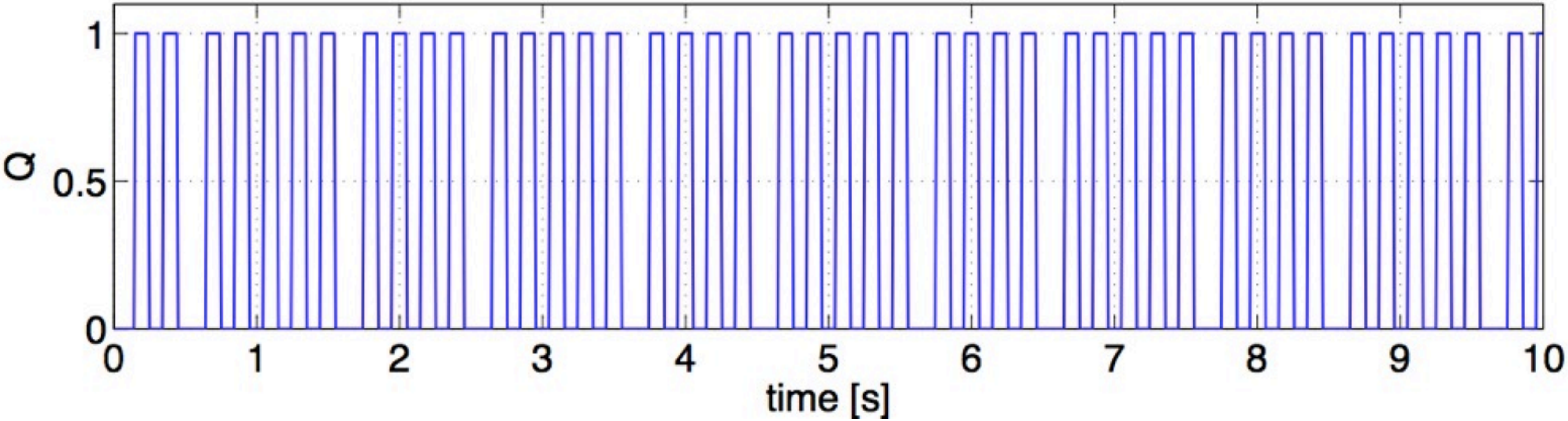
Vi=0.5V

Vdiff=1.5
Vdiff=-0.5

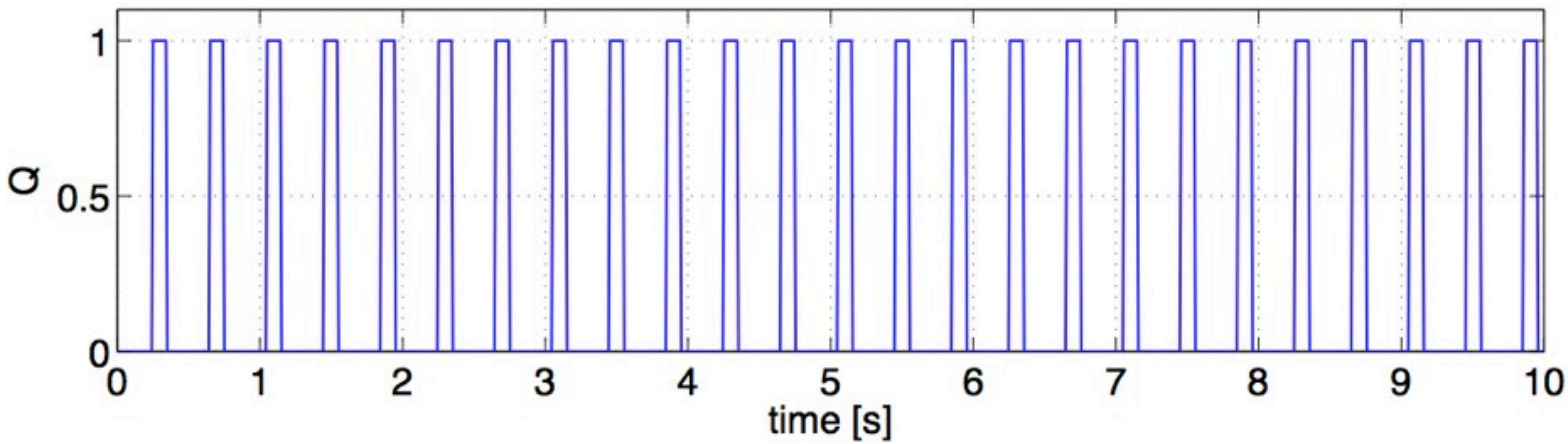




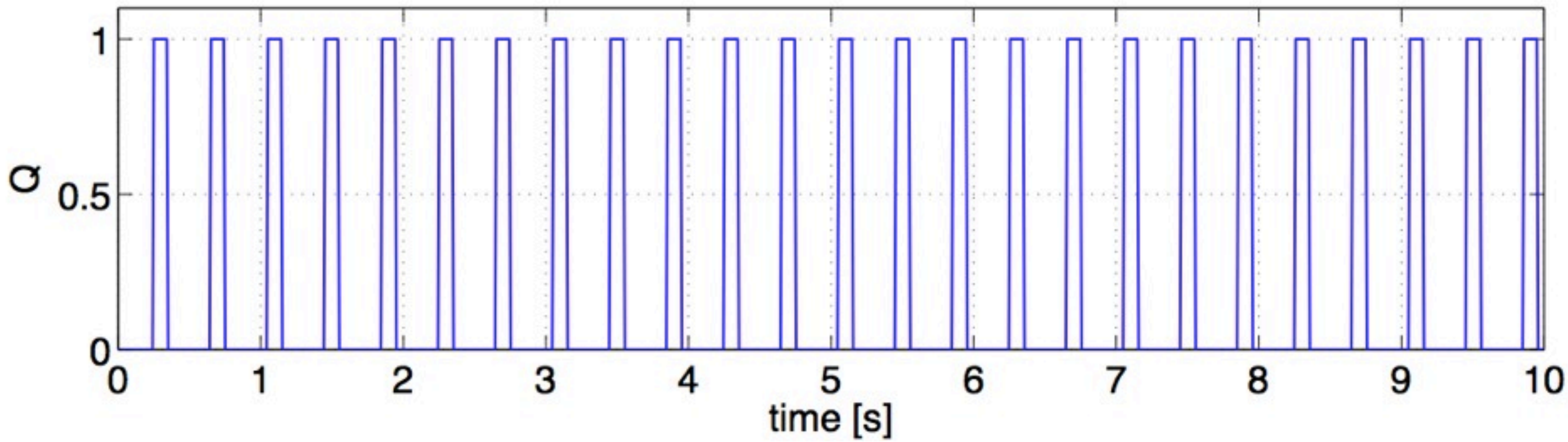
Vi=0.1V



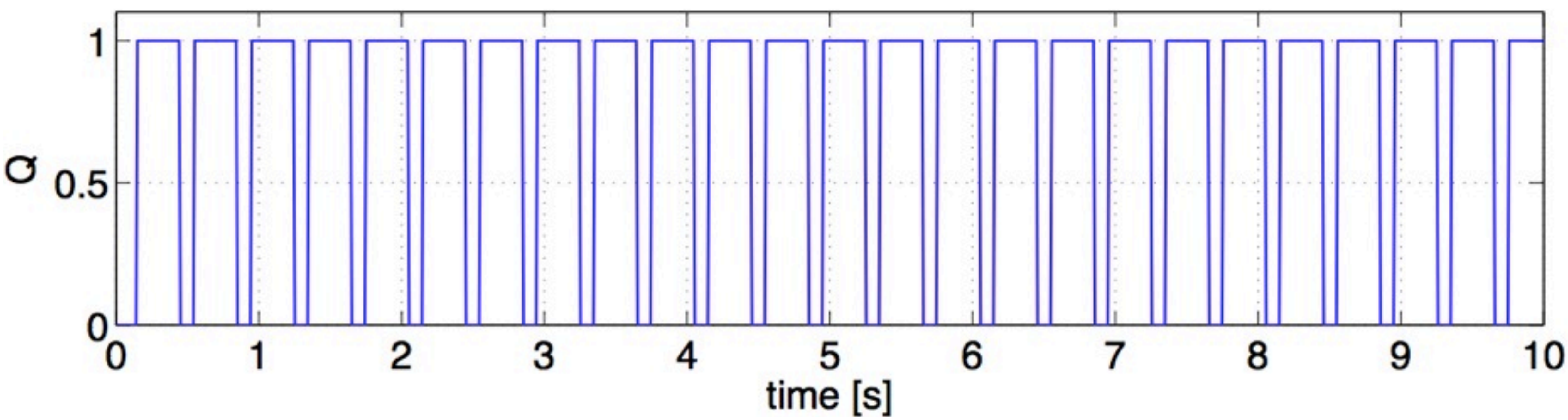
Vi=0.5V



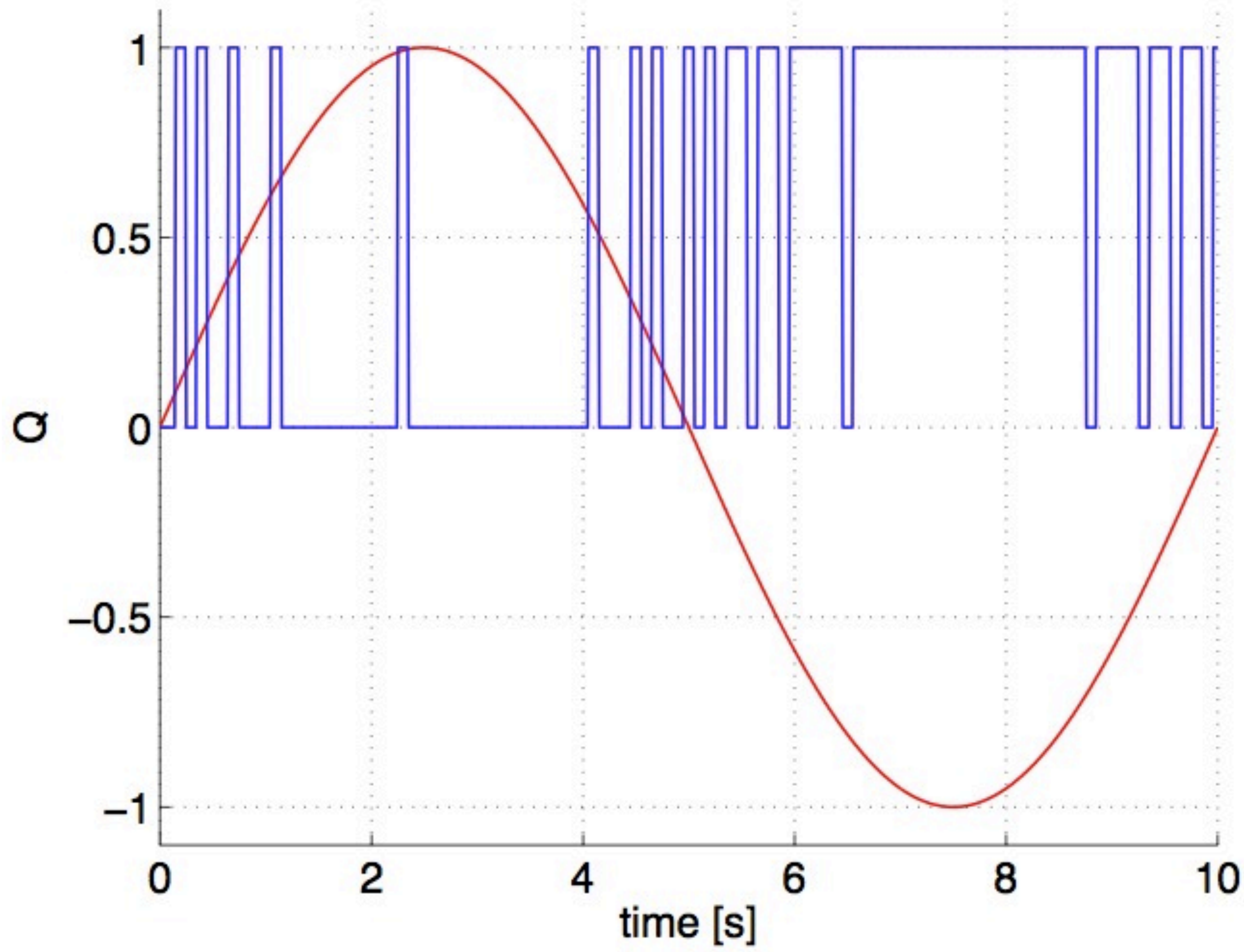
Vi=0.5V



Vi=-0.5V

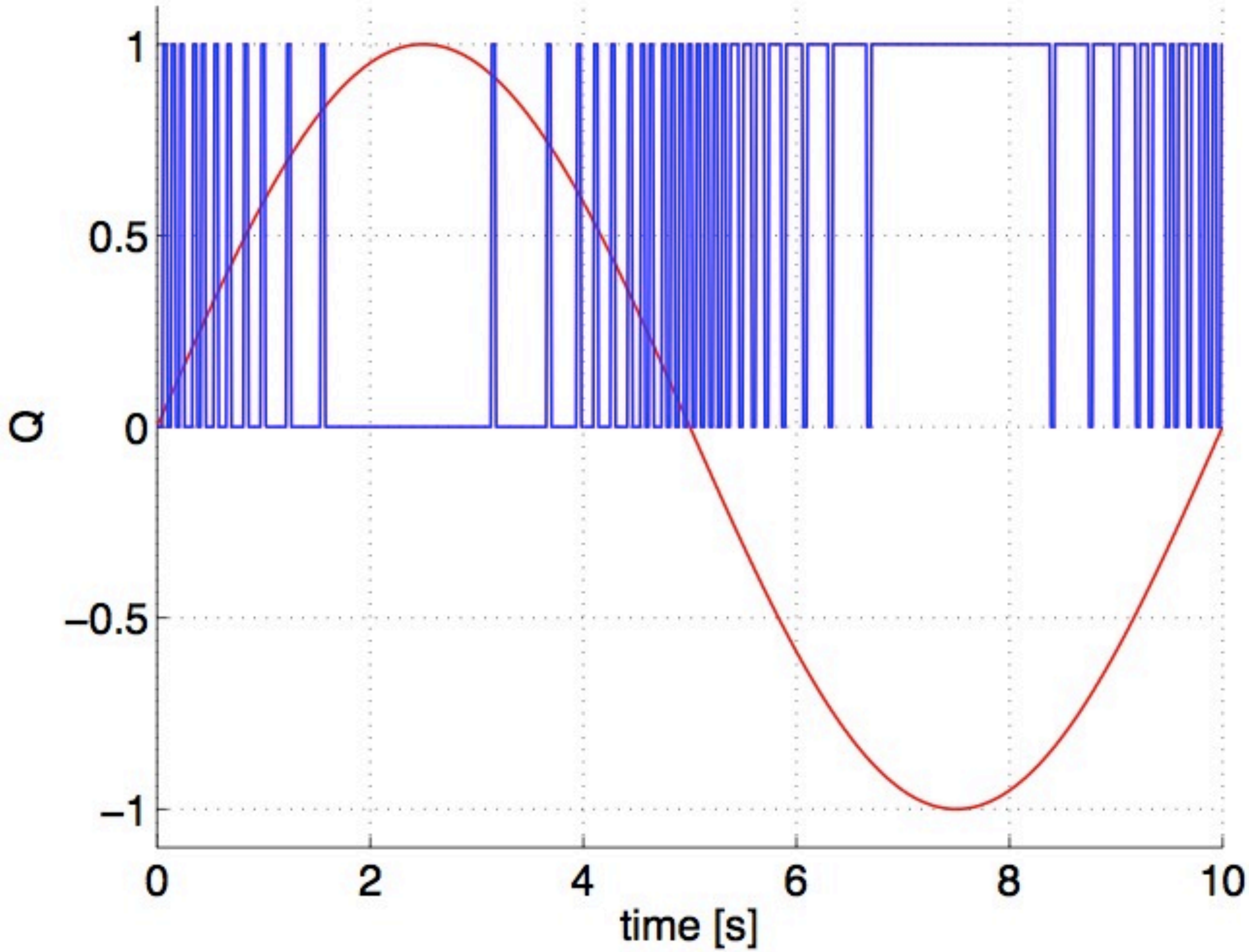


Converting a Sine wave



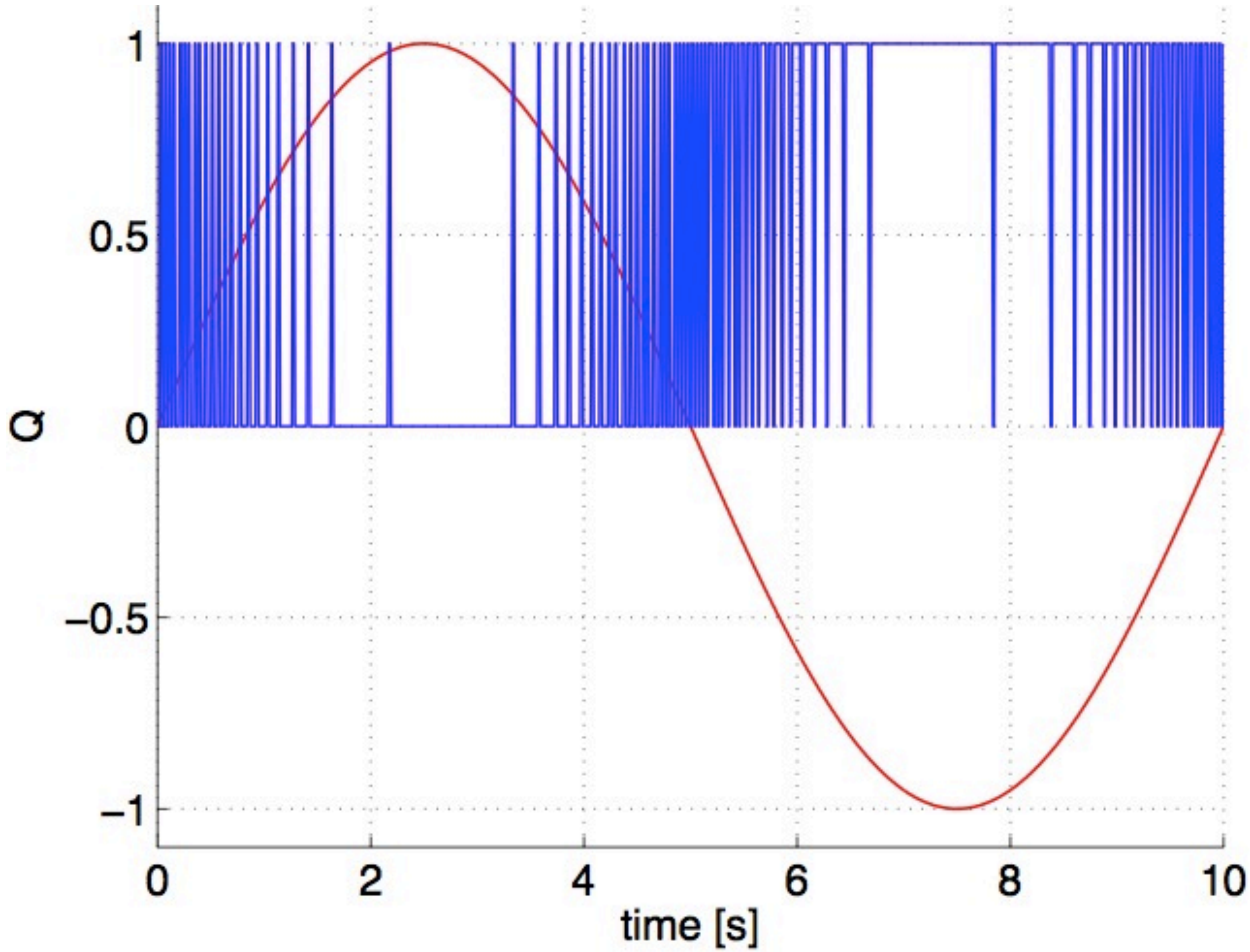
Converting a Sine wave

higher clock rate



Converting a Sine wave

even higher clock rate



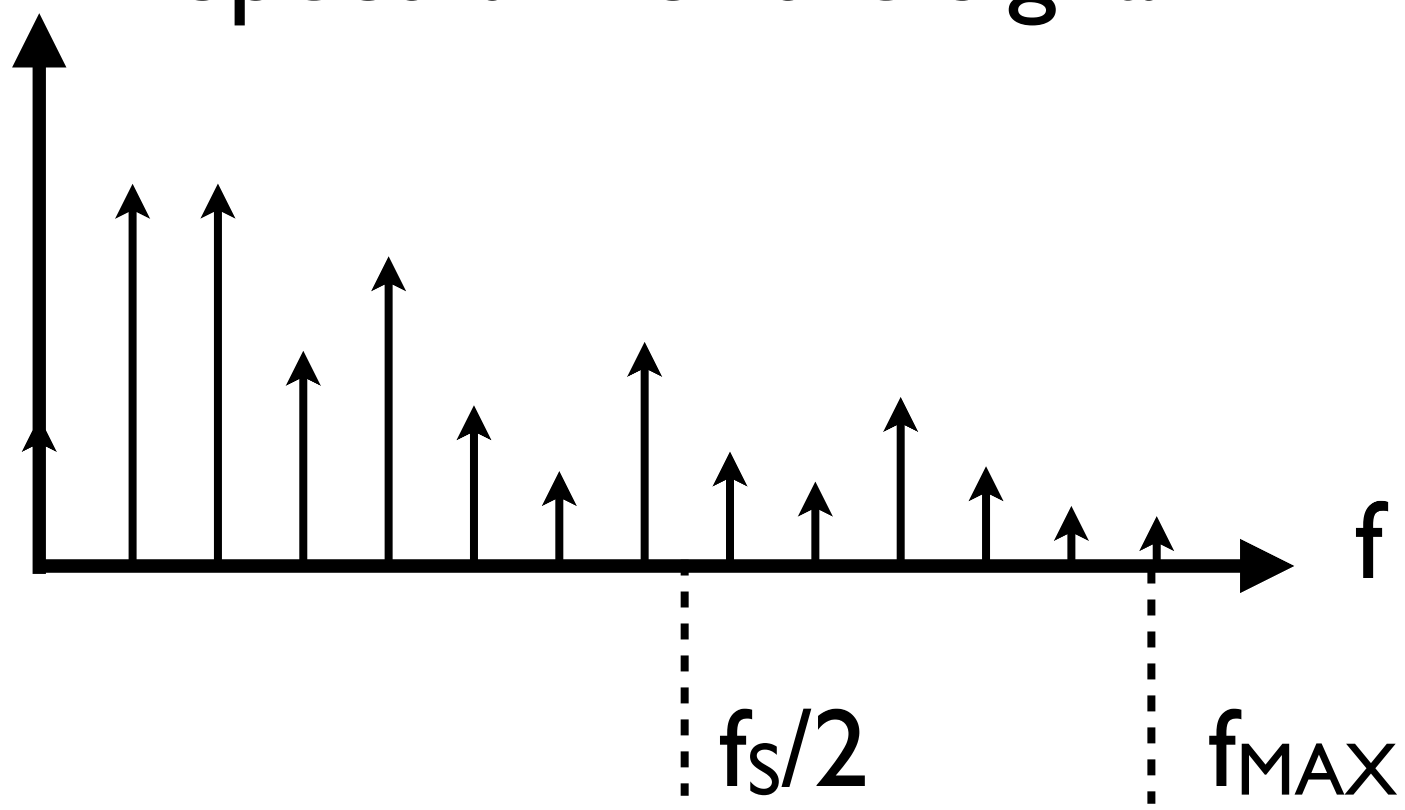
SIGMA DELTA

One bit sampling with ultra high sampling frequency
High speed is transformed into high resolution

Top Total Parts: 452	Resolution (bits)	Input Chan.	Conv. Rate (ksps)	Budgetary Price
Matching Parts: 5	ADC		max	*See Notes*
Current Selections:	= 24	-	-	-
MAX11200 24-bit, 1-channel, Ultra-Low Power Delta Sigma ADC	24	1	0.48	$2.65 @1k
MAX11201 24-bit, 1-channel, Ultra-Low Power Delta Sigma ADC	24	1	0.12	$2.55 @1k
MAX11202 24-bit, 1-channel, Ultra-Low Power Delta Sigma ADC	24	1	0.12	$2.45 @1k
MAX11210 24-bit, 1-channel, Ultra-Low Power Delta Sigma ADC with Programmable Gain	24	1	0.48	$2.85 @1k

What if the sampling frequency of the ADC is NOT high enough?

Spectrum of the signal



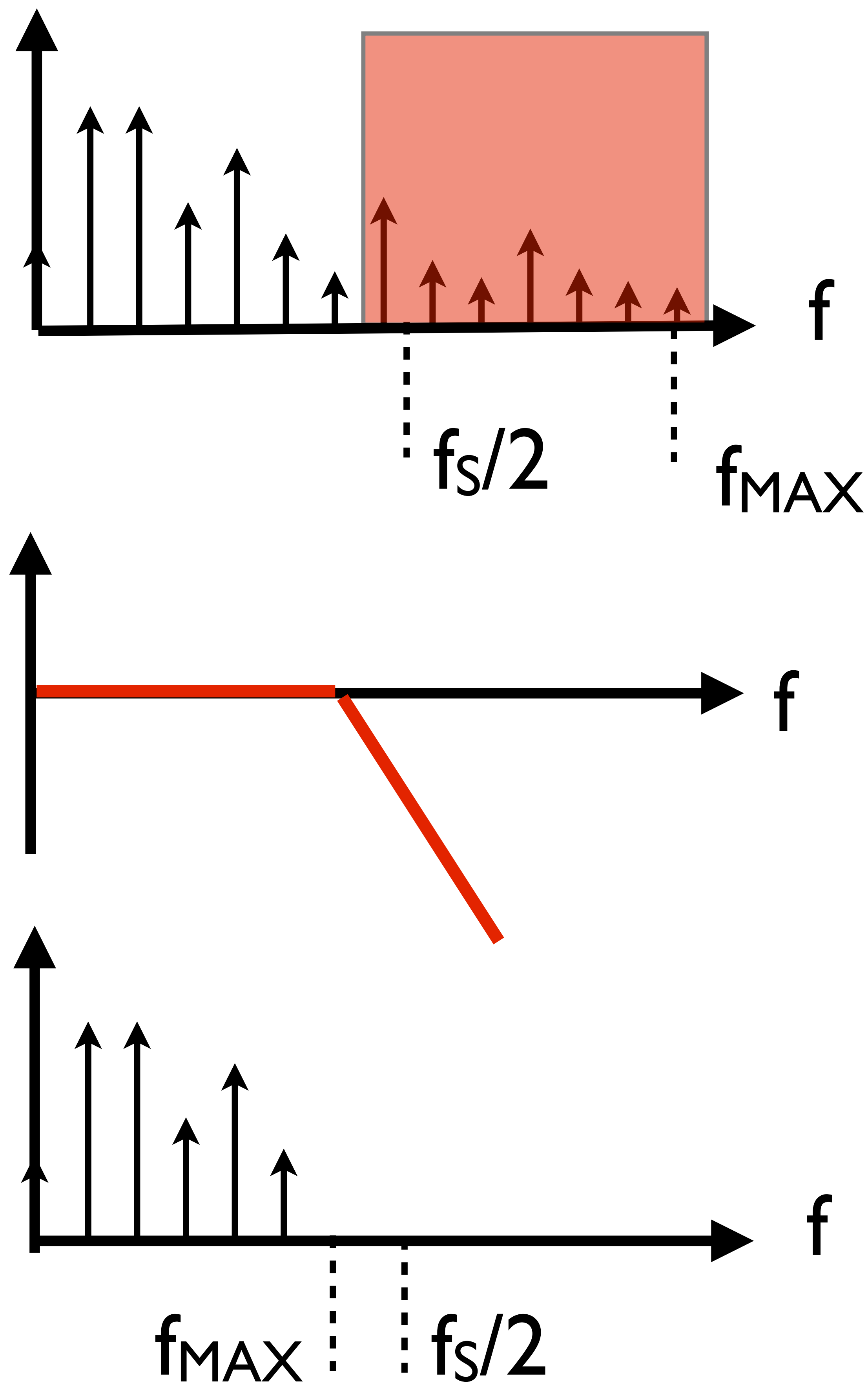
It should be $f_S/2 > f_{MAX}$ but it is $f_S/2 < f_{MAX}$

ANTI-ALIASING FILTER

Spectrum of the signal

low pass filter

Spectrum to



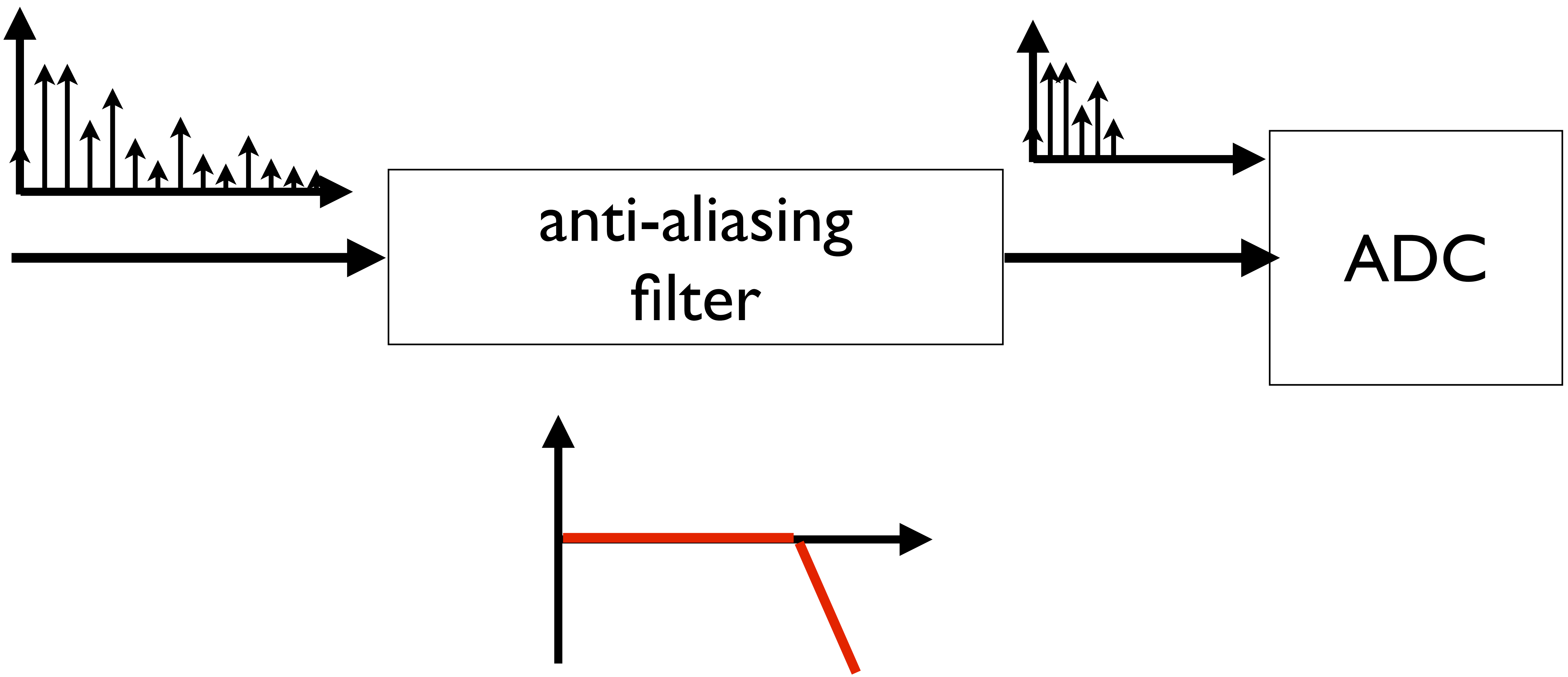
$f_S/2 < f_{MAX}$

BAD

$f_S/2 > f_{MAX}$

GOOD

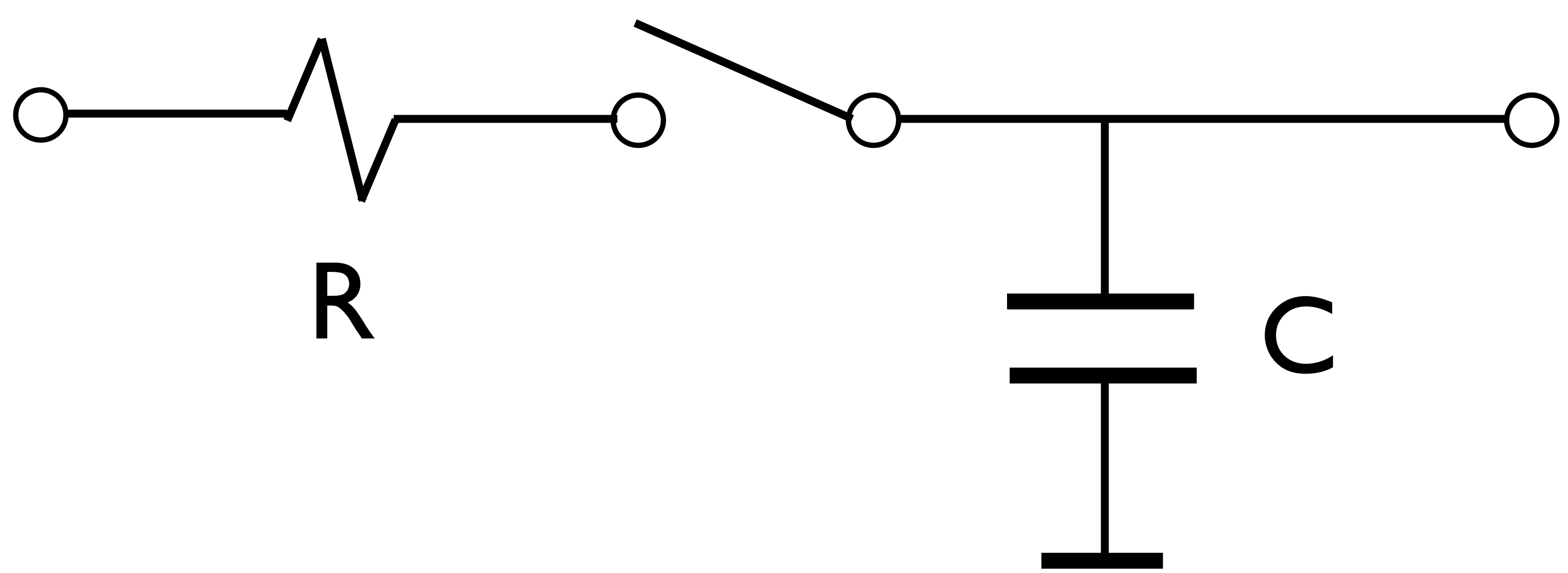
ANTI-ALIASING FILTER



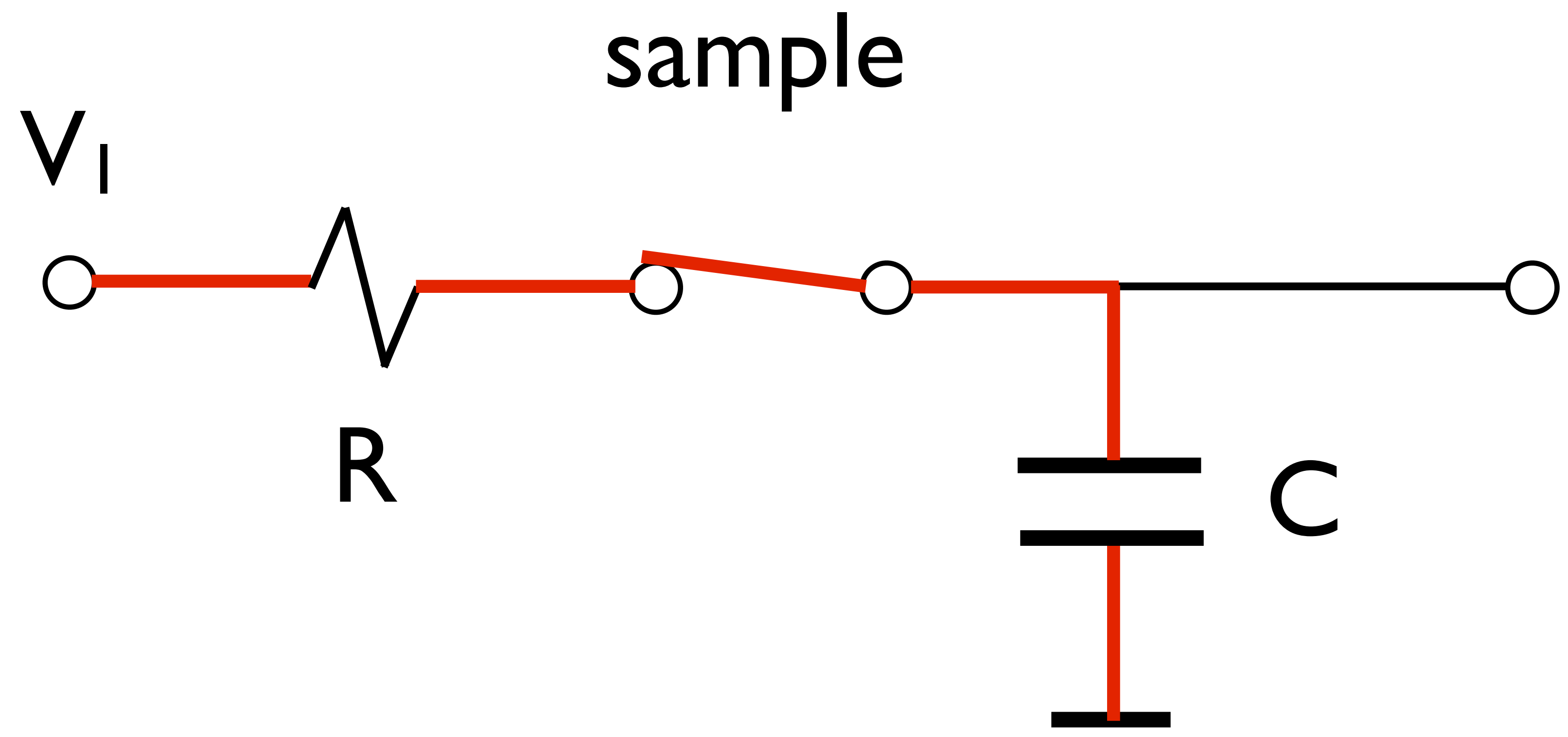
SAMPLE & HOLD

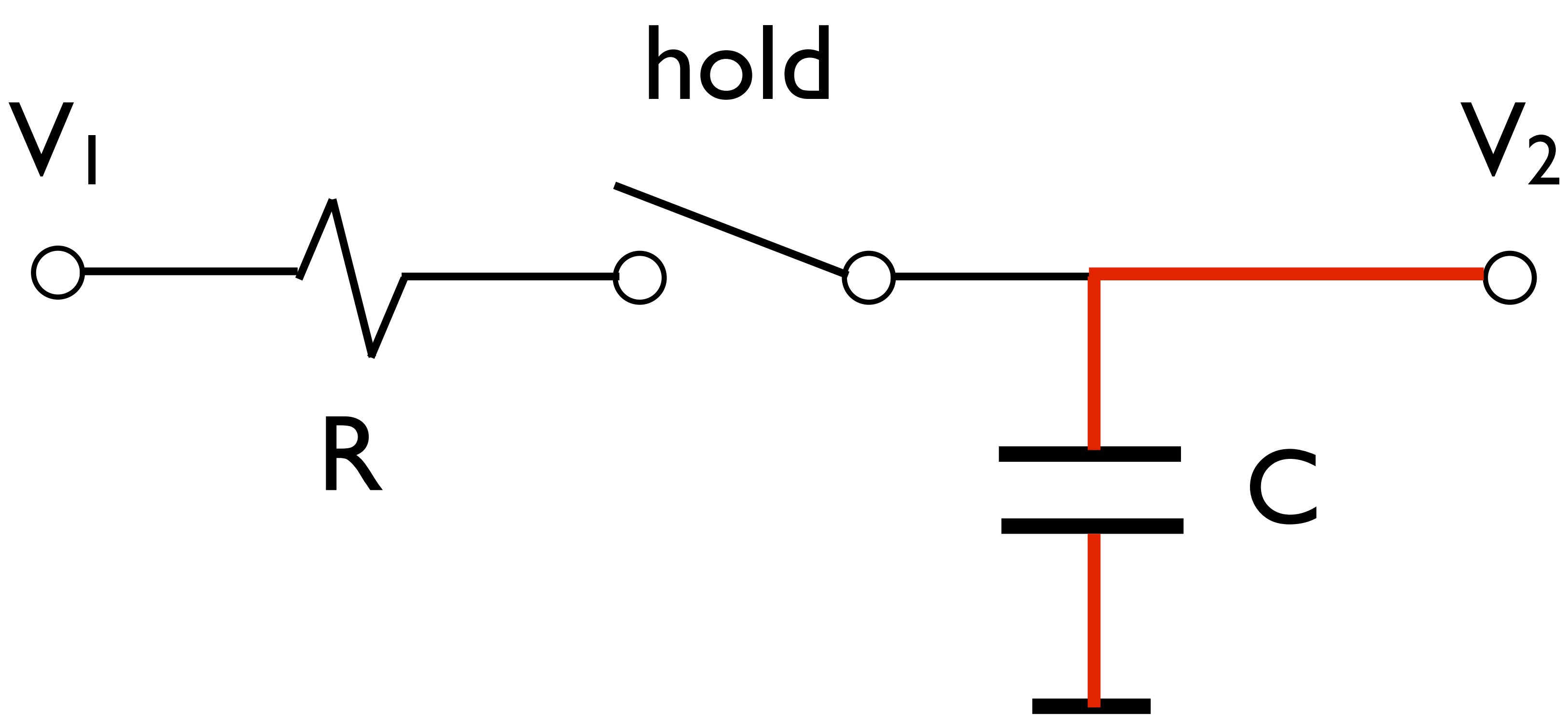
We need to keep the voltage constant during the conversion time

Basic idea



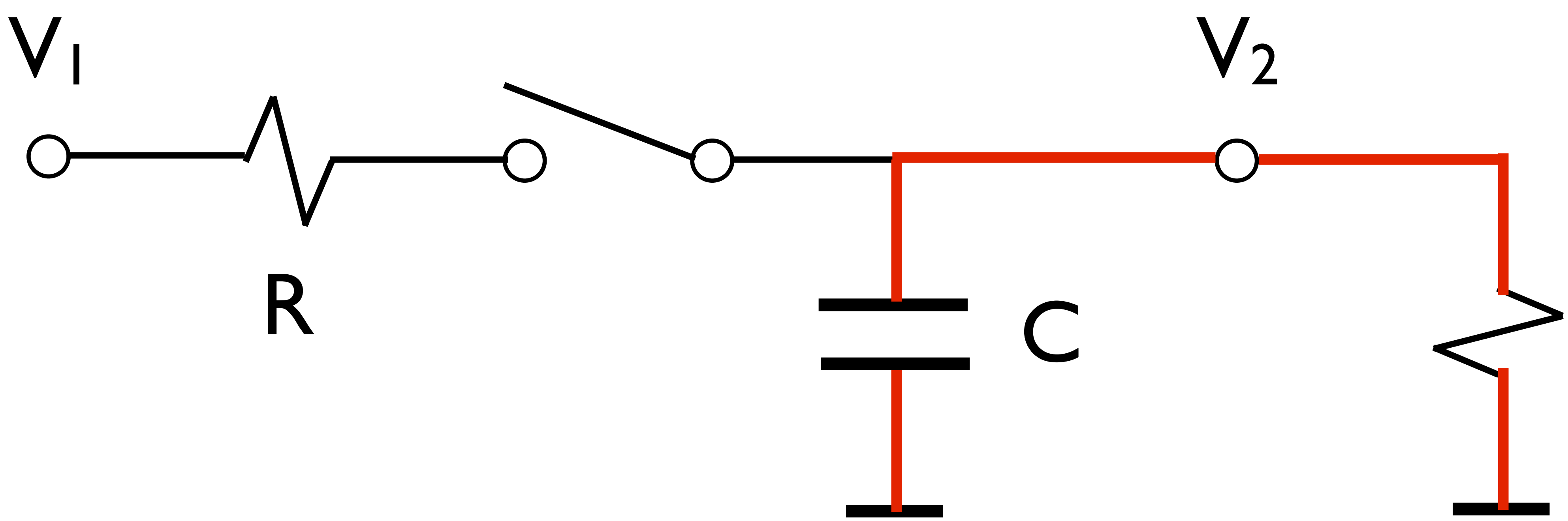
SAMPLE & HOLD





SAMPLE & HOLD

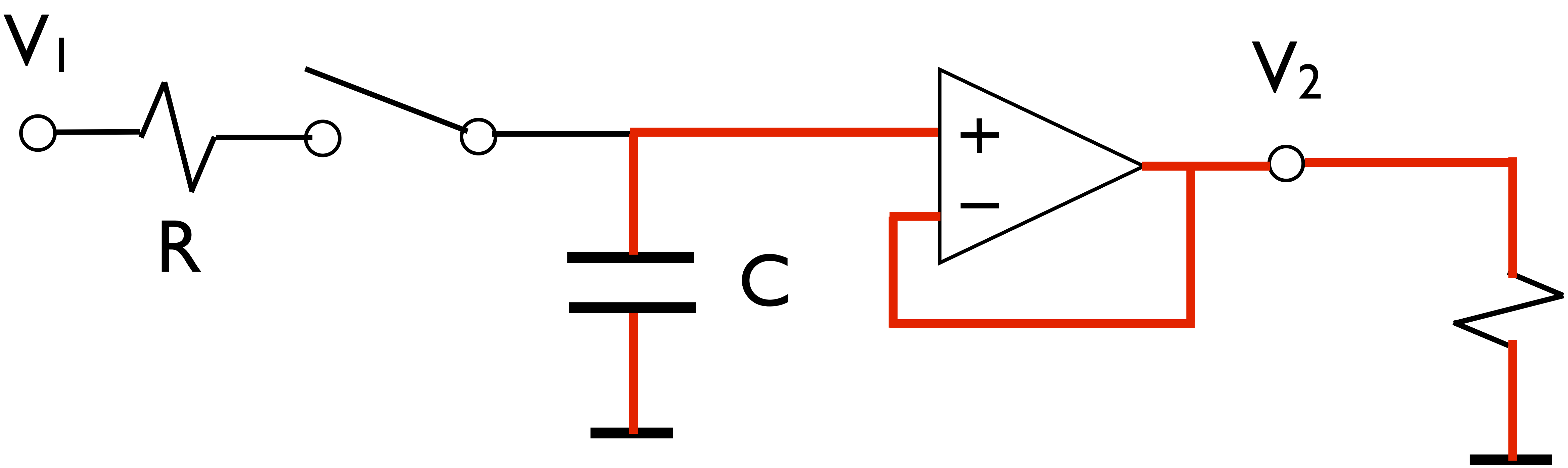
Problem: the capacitor will discharge



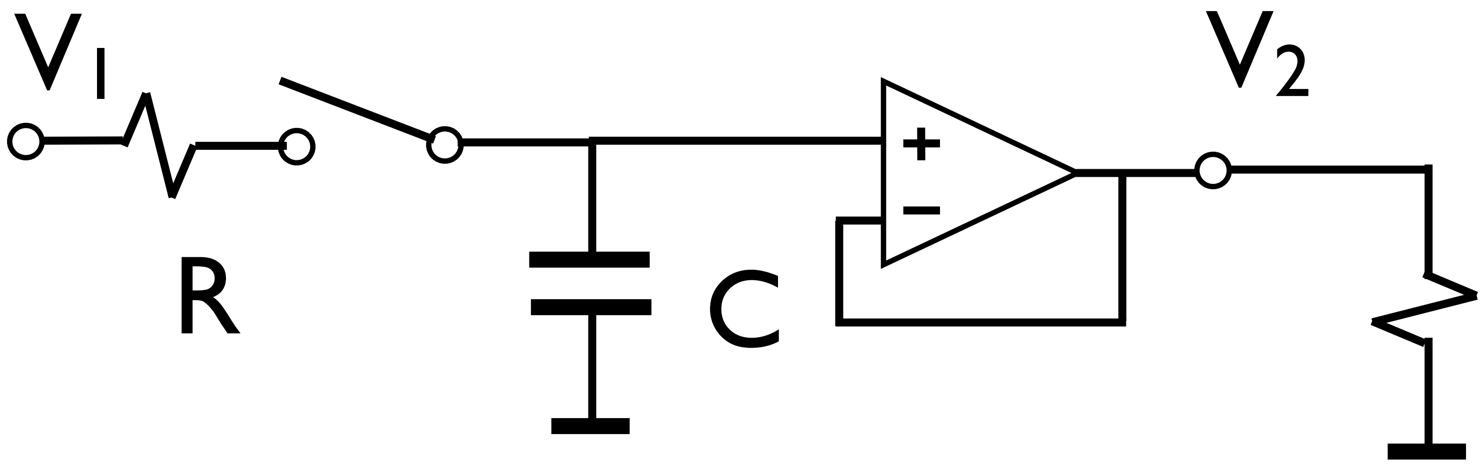
Input impedance of ADC

SAMPLE & HOLD

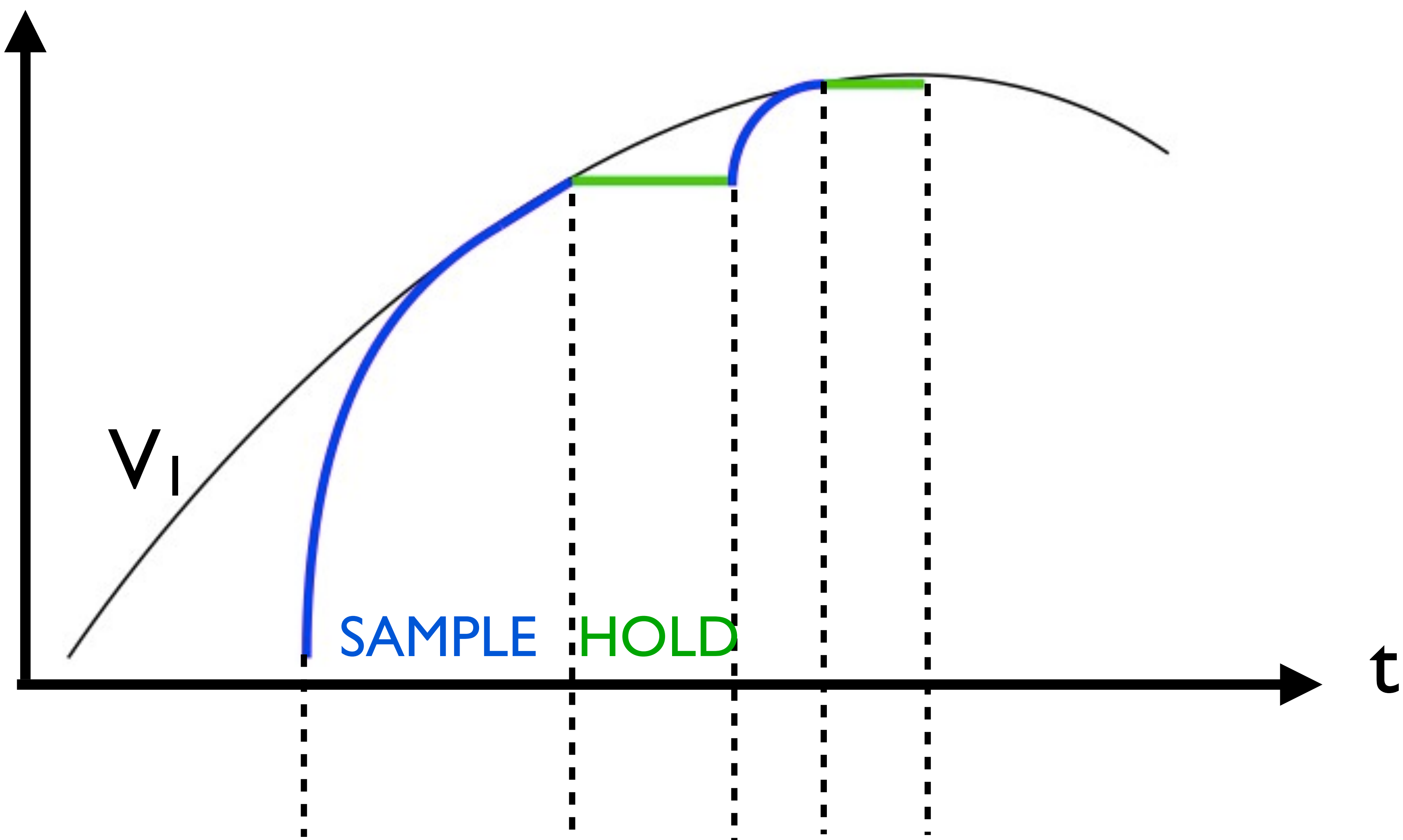
Solution: we use a voltage follower



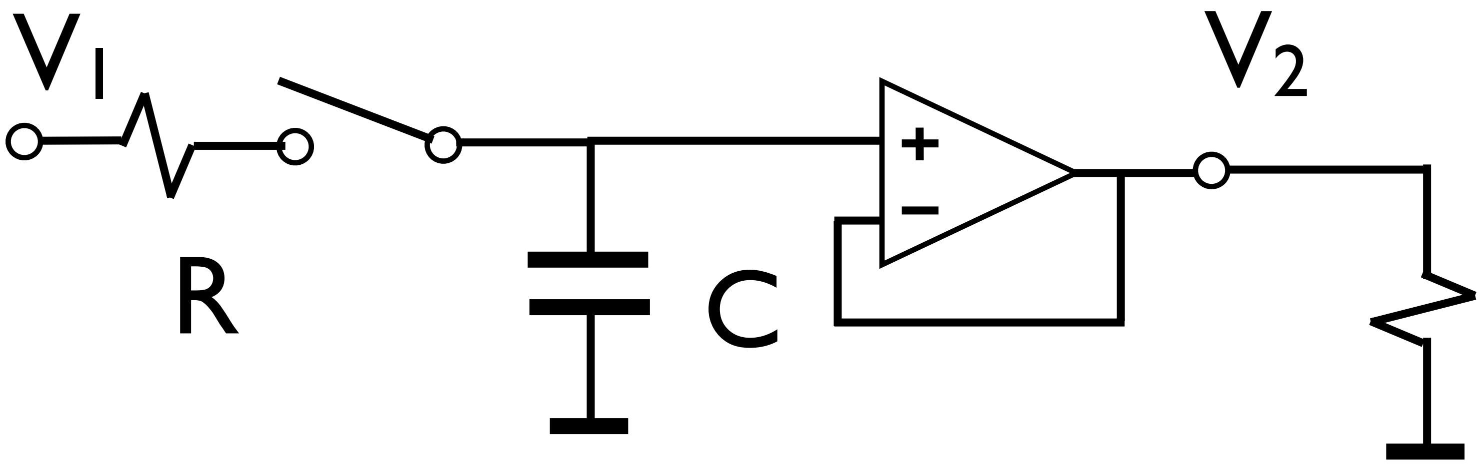
SAMPLE & HOLD



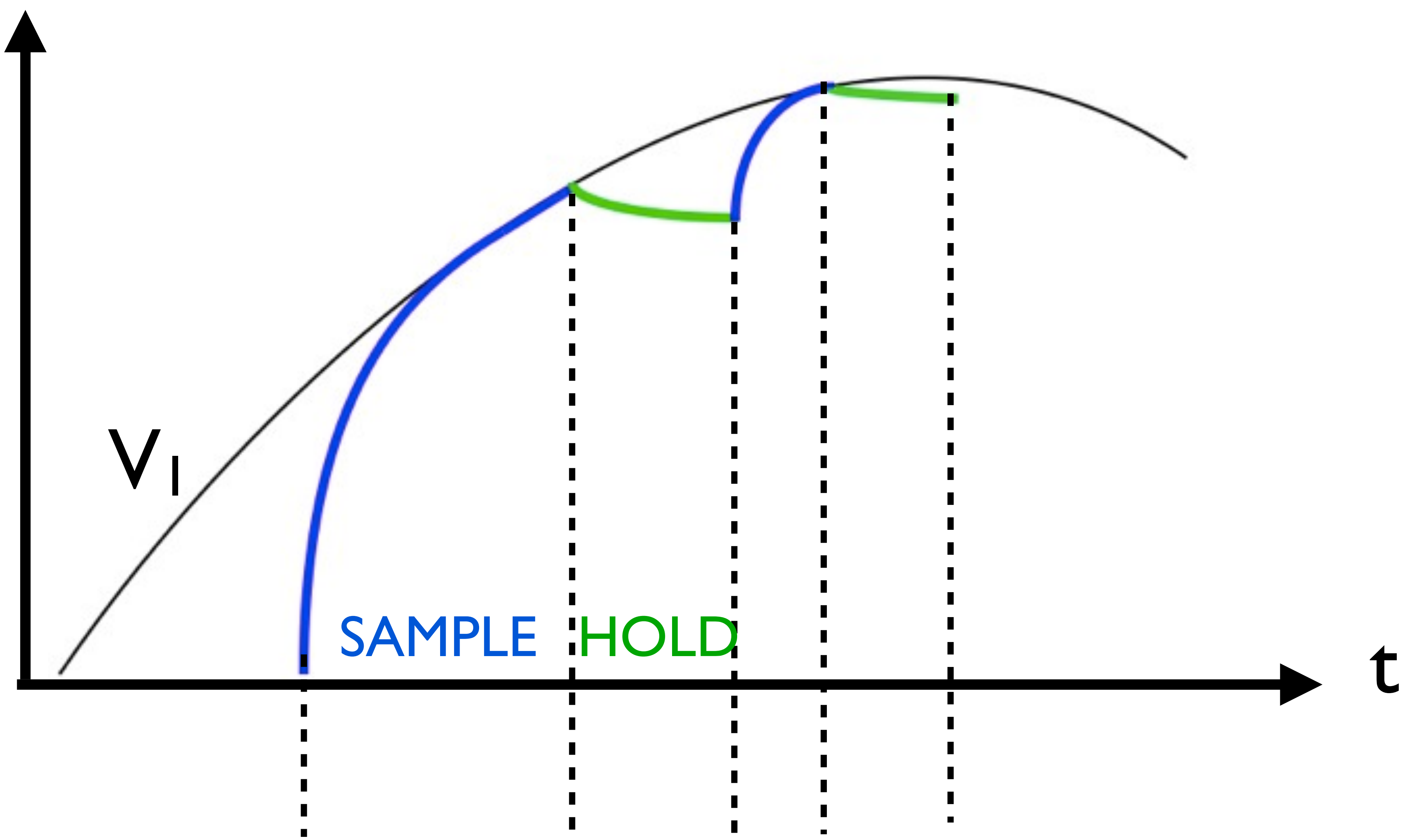
Ideal:



SAMPLE & HOLD



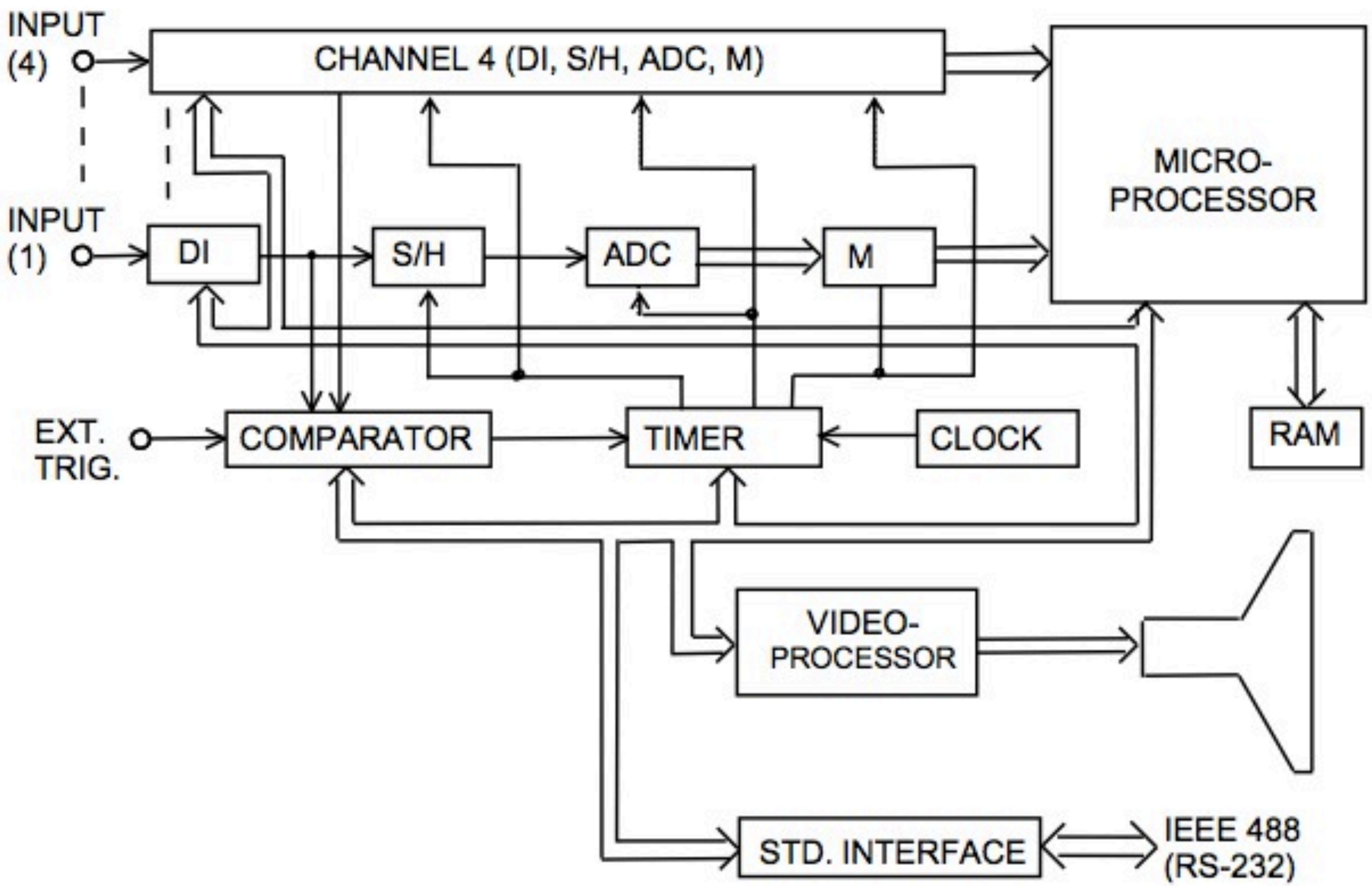
Real:



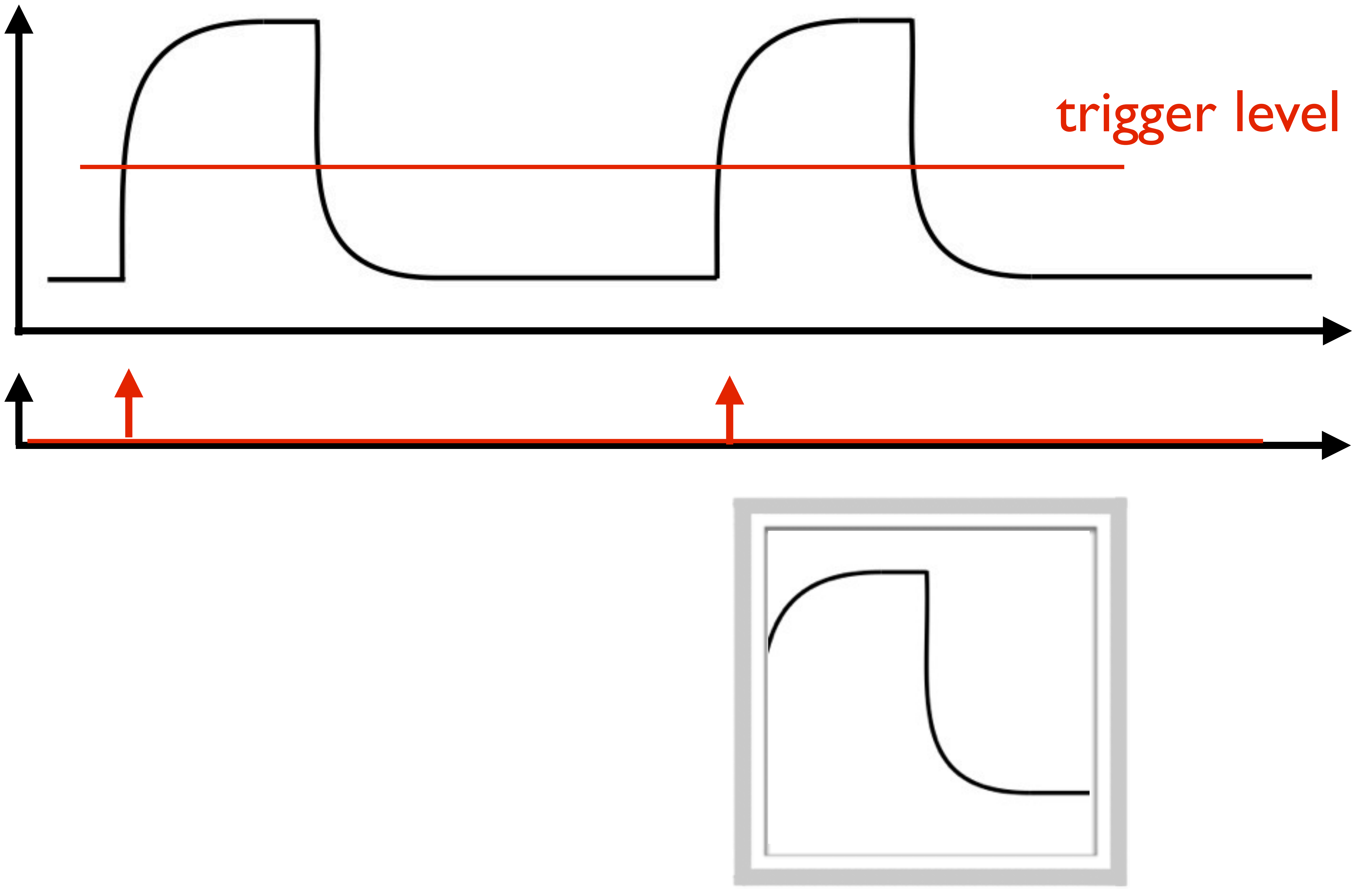
DIGITAL OSCILLOSCOPE

- memory
- computation of many parameters of the waveform
- smart computation such as FFT
- storage of waveform
- pre triggering

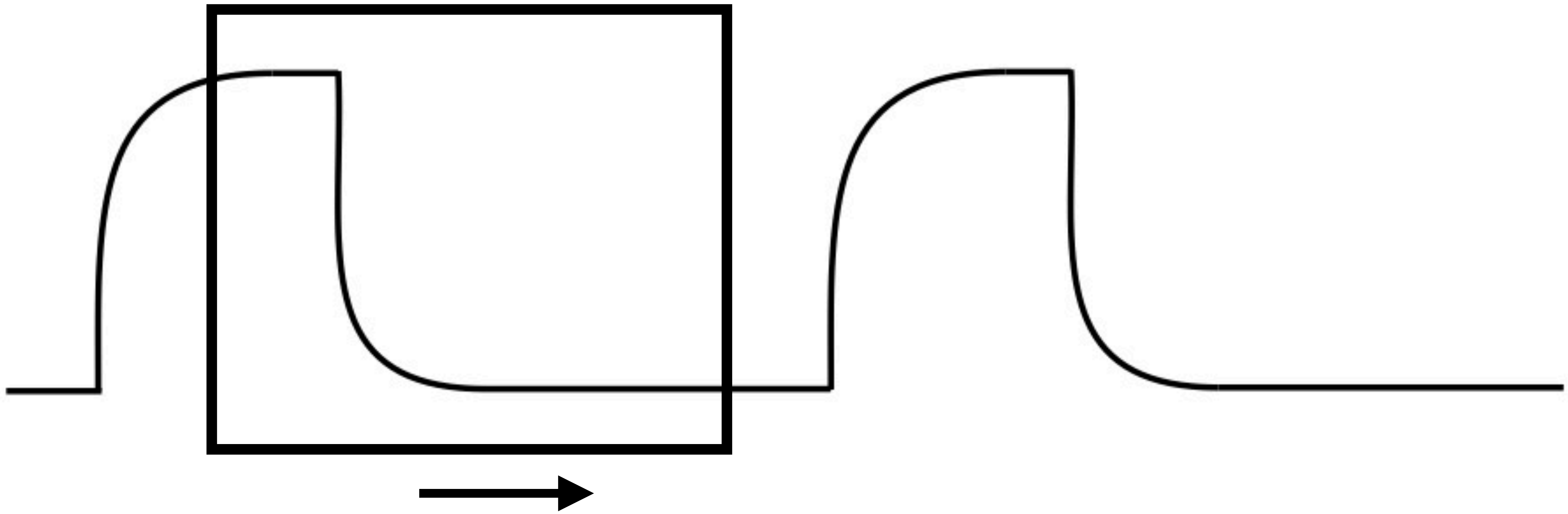
DIGITAL OSCILLOSCOPE
Structure



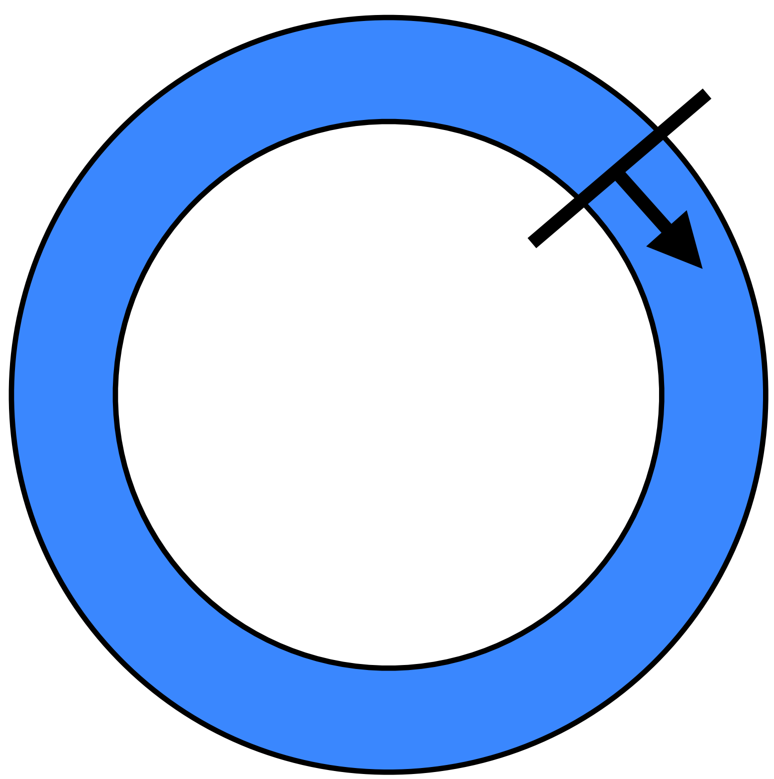
Trigger in analog oscilloscopes



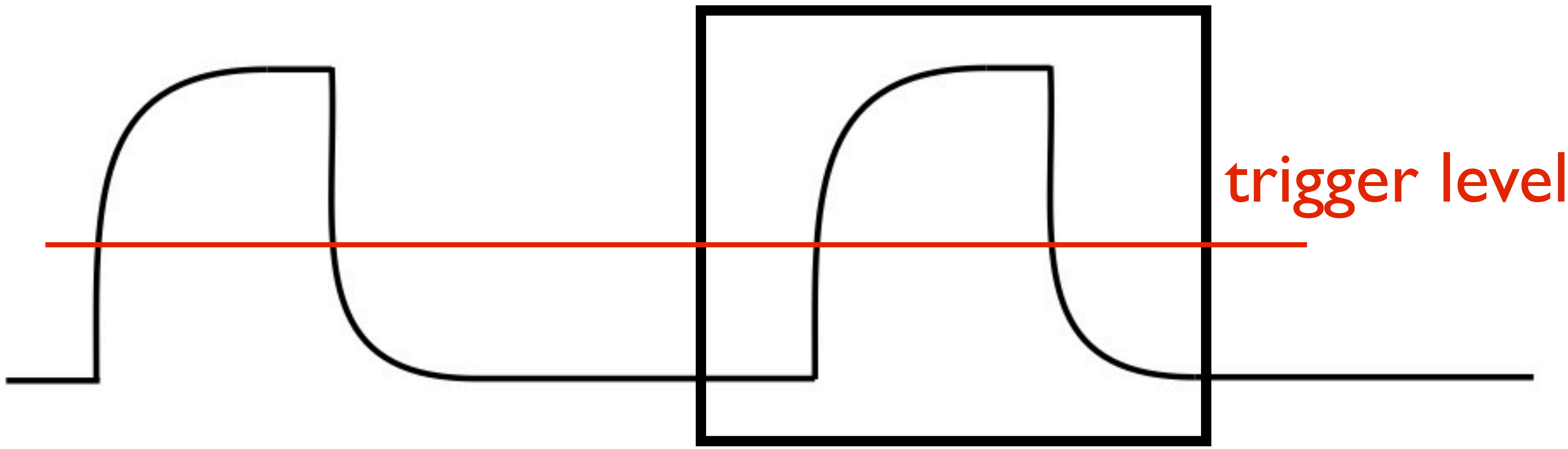
Trigger in digital oscilloscopes



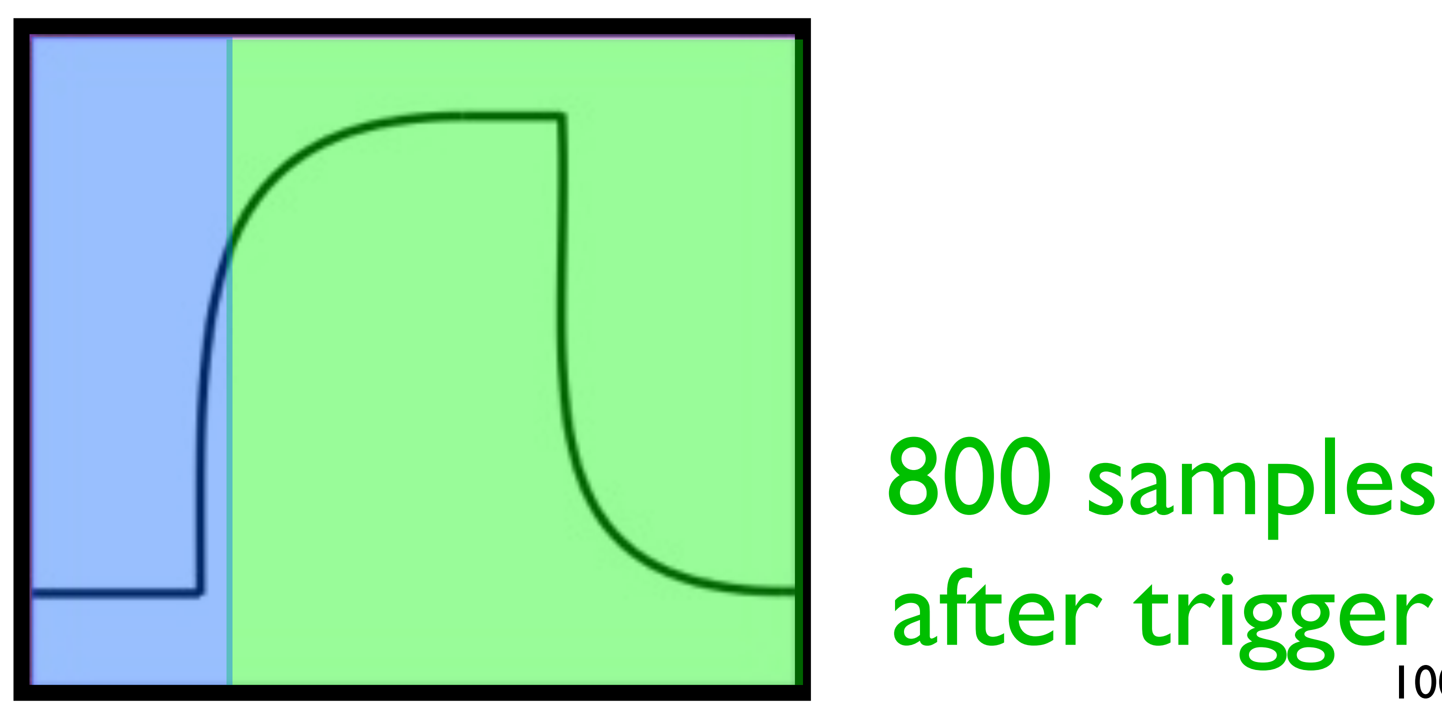
CIRCULAR
MEMORY



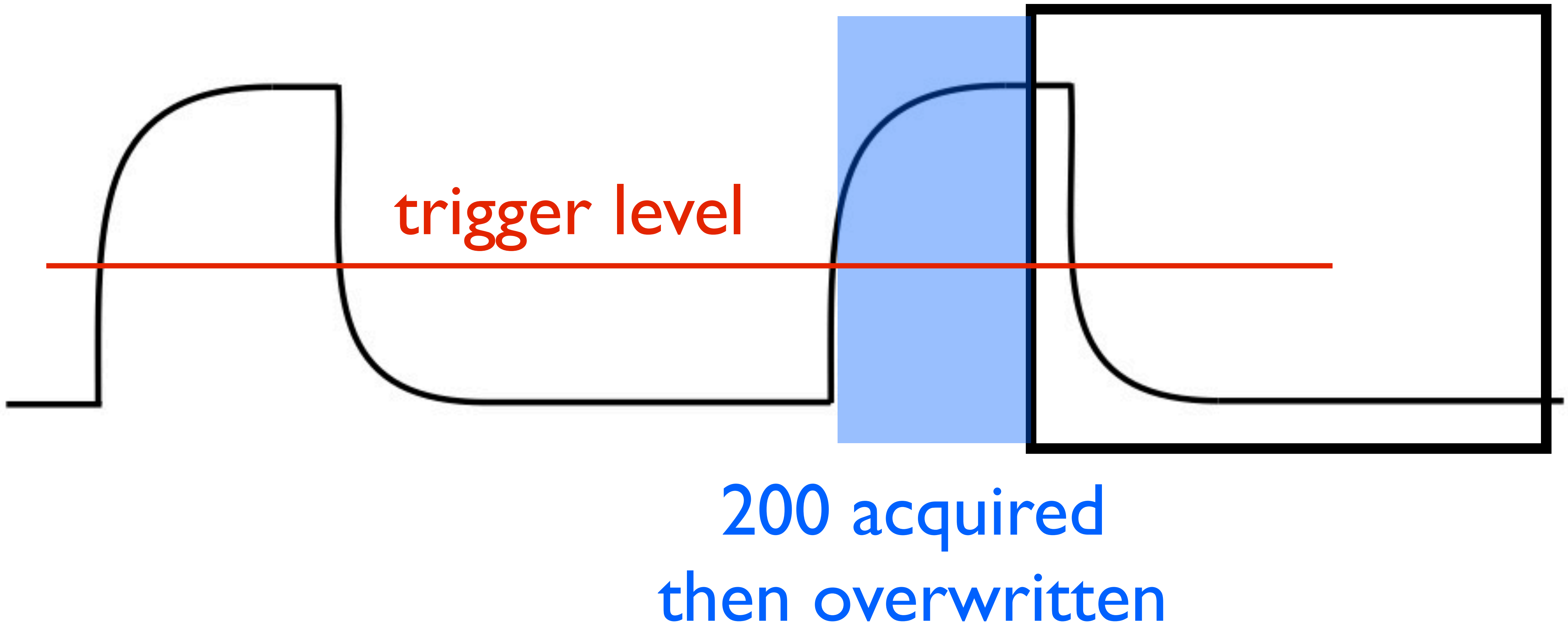
Trigger in digital oscilloscopes: pre triggering



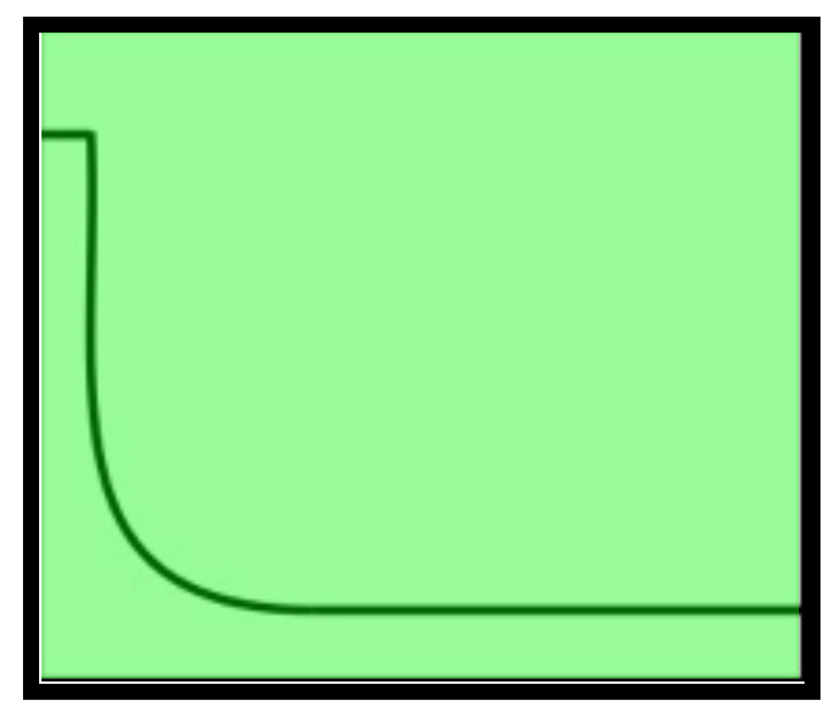
Ex. 1000 samples memory
Pre triggering 20%
OS stores 800 samples after triggering then stops



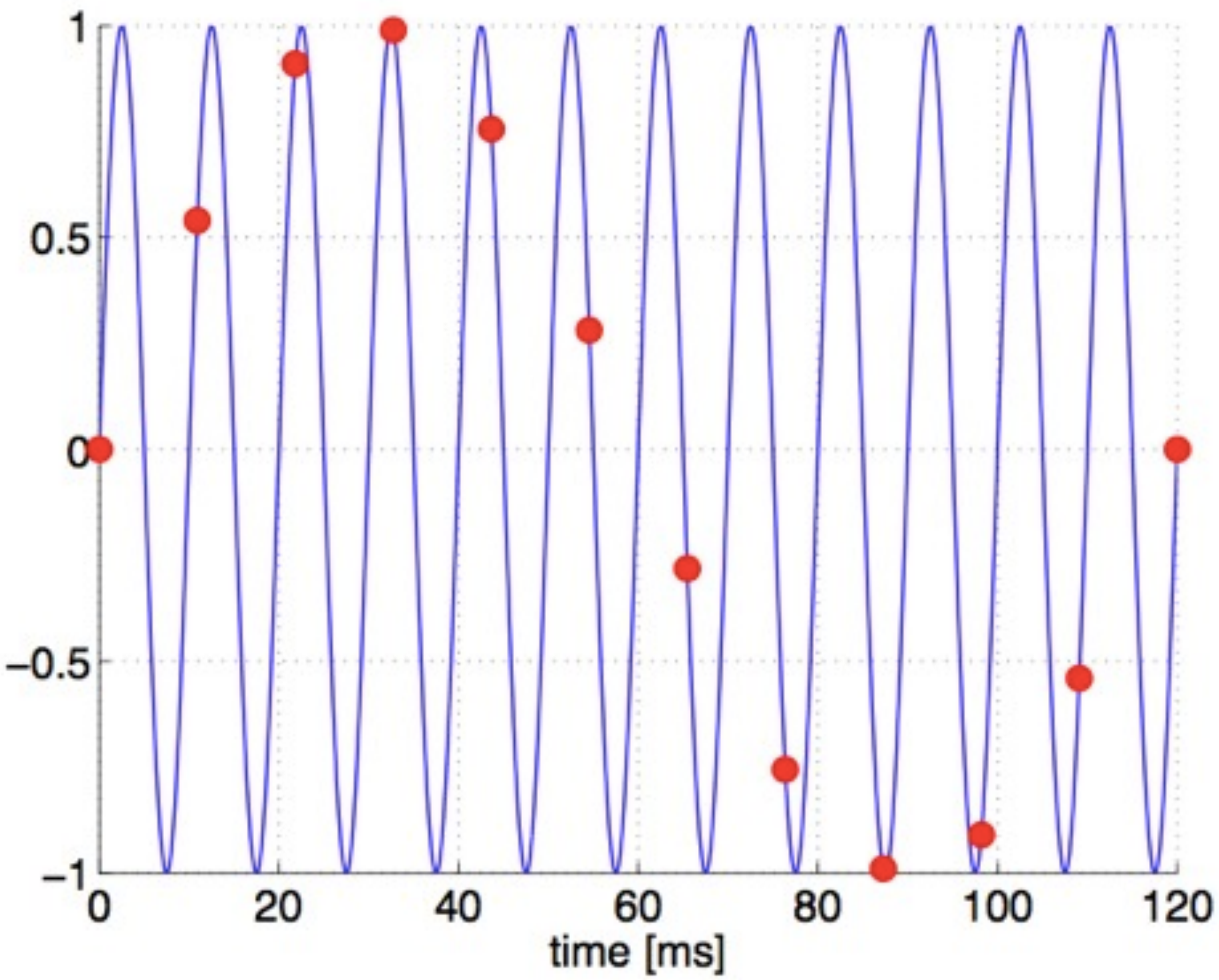
Trigger in digital oscilloscopes: delay

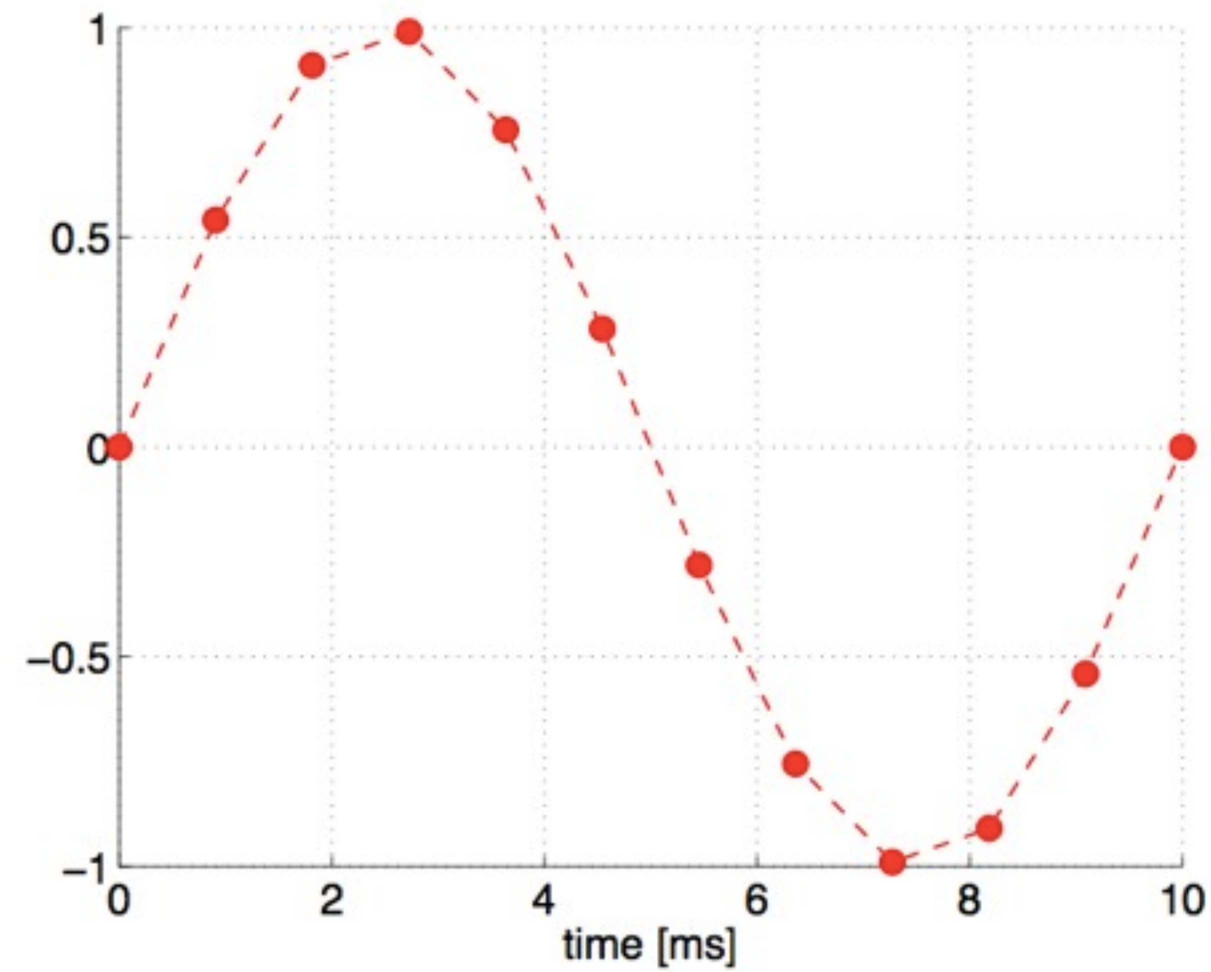


Ex. 1000 samples memory
Delay 20%
OS stores 1200 samples
after triggering then stops



- Equivalent time acquisition





The signal must be periodic

- Random equivalent time acquisition