



PIC18FXX20

Data Sheet

High Performance,
1 Mbit Enhanced FLASH
Microcontrollers with A/D

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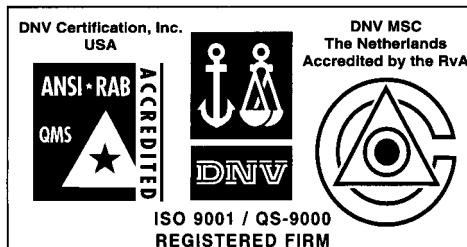
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MICROCHIP

PIC18FXX20

64/80-pin High Performance, 1 Mbit Enhanced FLASH Microcontrollers with A/D

High Performance RISC CPU:

- C compiler optimized architecture/instruction set
 - Source code compatible with the PIC16 and PIC17 instruction sets
- Linear program memory addressing to 128 Kbytes
- Linear data memory addressing to 3840 bytes
- 1 Kbyte of data EEPROM
- Up to 10 MIPS operation:
 - DC - 40 MHz osc./clock input
 - 4 MHz - 10 MHz osc./clock input with PLL active
- 16-bit wide instructions, 8-bit wide data path
- Priority levels for interrupts
- 31-level, software accessible hardware stack
- 8 x 8 Single Cycle Hardware Multiplier

External Memory Interface (PIC18F8X20 Devices Only):

- Address capability of up to 2 Mbytes
- 16-bit interface

Peripheral Features:

- High current sink/source 25 mA/25 mA
- Four external interrupt pins
- Timer0 module: 8-bit/16-bit timer/counter
- Timer1 module: 16-bit timer/counter
- Timer2 module: 8-bit timer/counter
- Timer3 module: 16-bit timer/counter
- Timer4 module: 8-bit timer/counter
- Secondary oscillator clock option - Timer1/Timer3
- Five Capture/Compare/PWM (CCP) modules:
 - Capture is 16-bit, max. resolution 6.25 ns (T_{CY}/16)
 - Compare is 16-bit, max. resolution 100 ns (T_{CY})
 - PWM output: PWM resolution is 1- to 10-bit
- Master Synchronous Serial Port (MSSP) module with two modes of operation:
 - 3-wire SPI™ (supports all 4 SPI modes)
 - I²C™ Master and Slave mode
- Two Addressable USART modules:
 - Supports RS-485 and RS-232
- Parallel Slave Port (PSP) module

Analog Features:

- 10-bit, up to 16-channel Analog-to-Digital Converter (A/D)
 - Conversion available during SLEEP
- Programmable 16-level Low Voltage Detection (LVD) module
 - Supports interrupt on-Low Voltage Detection
- Programmable Brown-out Reset (BOR)
- Dual analog comparators
 - Programmable input/output configuration

Special Microcontroller Features:

- 100,000 erase/write cycle Enhanced FLASH program memory typical
- 1,000,000 erase/write cycle Data EEPROM memory typical
- 1 second programming time
- FLASH/Data EEPROM Retention: > 40 years
- Self-reprogrammable under software control
- Power-on Reset (POR), Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Watchdog Timer (WDT) with its own On-Chip RC Oscillator for reliable operation
- Programmable code protection
- Power-saving SLEEP mode
- Selectable oscillator options including:
 - 4X Phase Lock Loop (of primary oscillator)
 - Secondary Oscillator (32 kHz) clock input
- In-Circuit Serial Programming™ (ICSP™) via two pins
- MPLAB® In-Circuit Debug (ICD) via two pins

CMOS Technology:

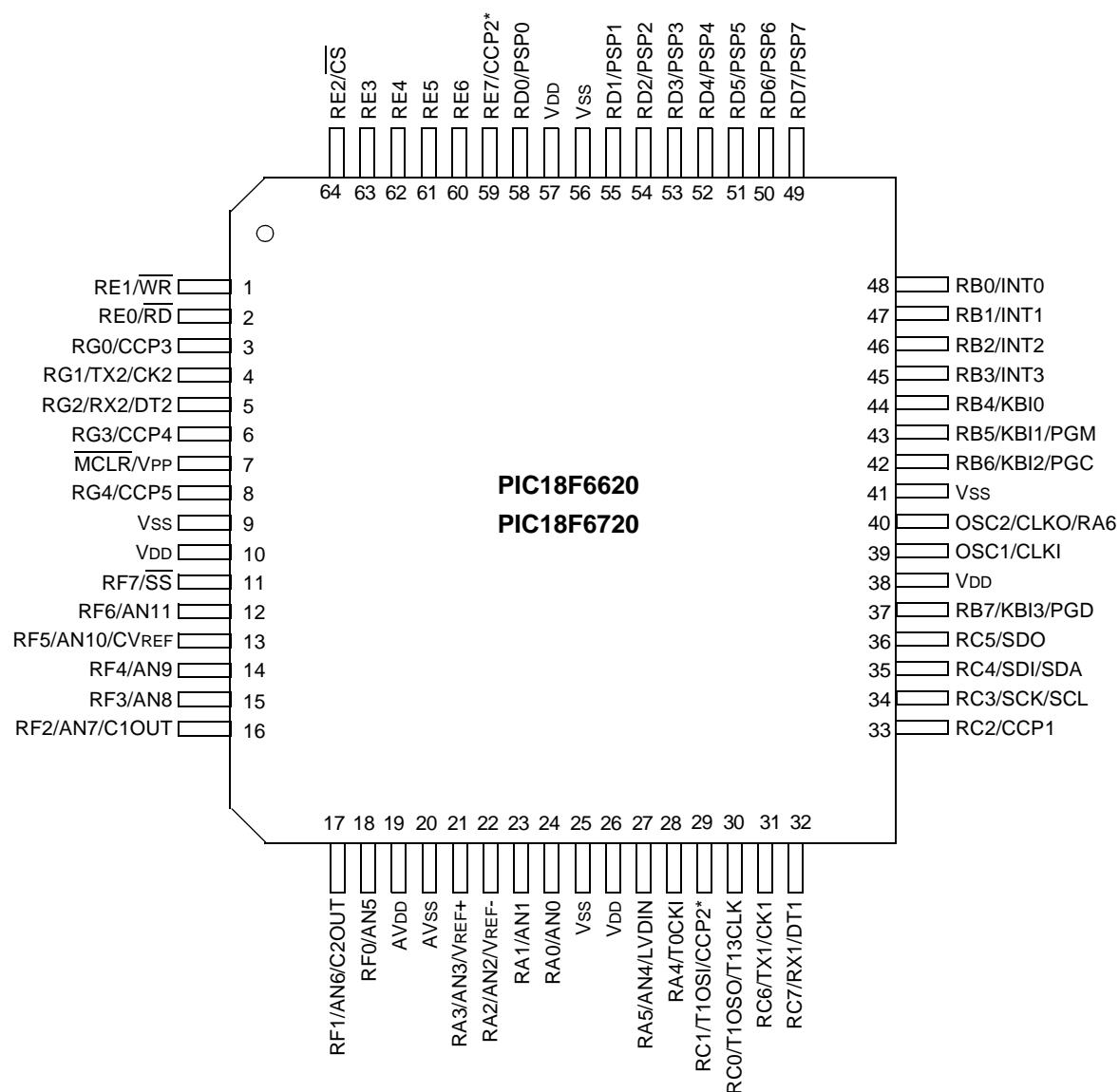
- Low power, high speed FLASH technology
- Fully static design
- Wide operating voltage range (2.0V to 5.5V)
- Industrial and Extended temperature ranges

Device	Program Memory		Data memory		I/O	10-bit A/D (ch)	CCP (PWM)	MSSP		USART	Timers 8-bit/16-bit	Ext Bus
	Bytes	# Single Word Instructions	SRAM (bytes)	EEPROM (bytes)				SPI	Master I ² C			
PIC18F6620	64K	32768	3840	1024	52	12	5	Y	Y	2	2/3	N
PIC18F6720	128K	65536	3840	1024	52	12	5	Y	Y	2	2/3	N
PIC18F8620	64K	32768	3840	1024	68	16	5	Y	Y	2	2/3	Y
PIC18F8720	128K	65536	3840	1024	68	16	5	Y	Y	2	2/3	Y

PIC18FXX20

Pin Diagrams

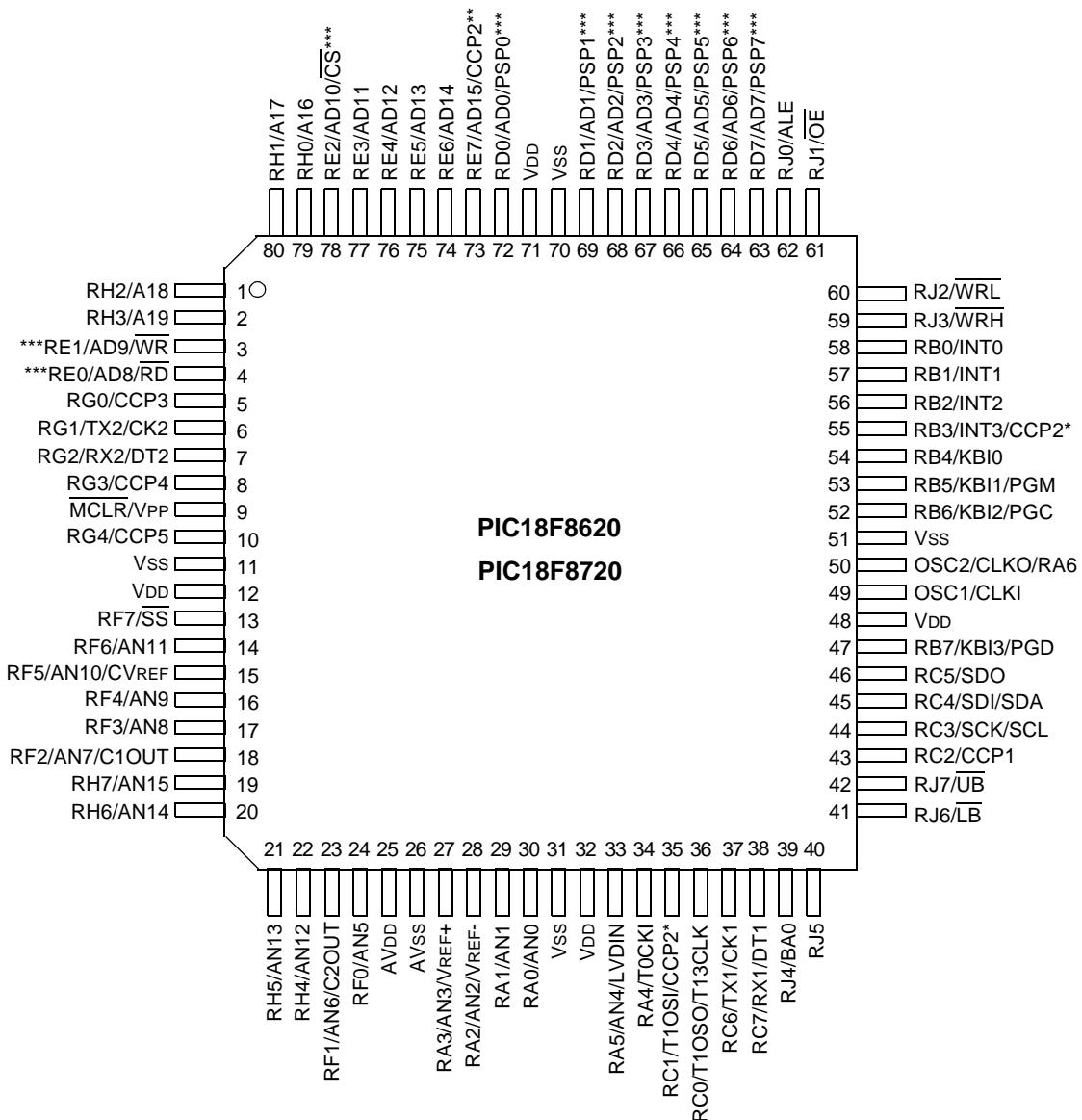
64-pin TQFP



* CCP2 is multiplexed with RC1 when CCP2MX is set.

Pin Diagrams (Cont.'d)

80-pin TQFP



* CCP2 is multiplexed with RC1 when CCP2MX is set.

** CCP2 is multiplexed by default with RE7 when **EXT2 MUX** is set.

*** PSP is available only in Microcontroller mode.

PIC18FXX20

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PIC18FXX20

NOTES:

1.0 DEVICE OVERVIEW

This document contains device specific information for the following devices:

1. PIC18F6620
2. PIC18F6720
3. PIC18F8620
4. PIC18F8720

These devices are available in 64-pin and 80-pin packages. They are differentiated from each other in four ways:

1. FLASH program memory (64 Kbytes for PIC18FX620 devices, 128 Kbytes for PIC18FX720)
2. A/D channels (12 for PIC18F6X20 devices, 16 for PIC18F8X20)
3. I/O ports (7 on PIC18F6X20 devices, 9 on PIC18F8X20)
4. External program memory interface (present only on PIC18F8X20 devices)

All other features for devices in the PIC18FXX20 family are identical. These are summarized in Table 1-1.

Block diagrams of the PIC18F6X20 and PIC18F8X20 devices are provided in Figure 1-1 and Figure 1-2, respectively. The pinouts for these device families are listed in Table 1-2.

TABLE 1-1: PIC18FXX20 DEVICE FEATURES

Features	PIC18F6620	PIC18F6720	PIC18F8620	PIC18F8720
Operating Frequency	DC - 40 MHz			
Program Memory (Bytes)	64K	128K	64K	126K
Program Memory (Instructions)	32768	65536	32768	65536
Data Memory (Bytes)	3840	3840	3840	3840
Data EEPROM Memory (Bytes)	1024	1024	1024	1024
External Memory Interface	No	No	Yes	Yes
Interrupt Sources	17	17	18	18
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
Timers	5	5	5	5
Capture/Compare/PWM Modules	5	5	5	5
Serial Communications	MSSP, Addressable USART (2)	MSSP, Addressable USART (2)	MSSP, Addressable USART (2)	MSSP, Addressable USART (2)
Parallel Communications	PSP	PSP	PSP	PSP
10-bit Analog-to-Digital Module	12 input channels	12 input channels	16 input channels	16 input channels
RESETS (and Delays)	POR, BOR, RESET Instruction, Stack Full, Stack Underflow (PWRT, OST)			
Programmable Low Voltage Detect	Yes	Yes	Yes	Yes
Programmable Brown-out Reset	Yes	Yes	Yes	Yes
Instruction Set	75 Instructions	75 Instructions	75 Instructions	75 Instructions
Package	64-pin TQFP	64-pin TQFP	80-pin TQFP	80-pin TQFP

PIC18FXX20

FIGURE 1-1: PIC18F6X20 BLOCK DIAGRAM

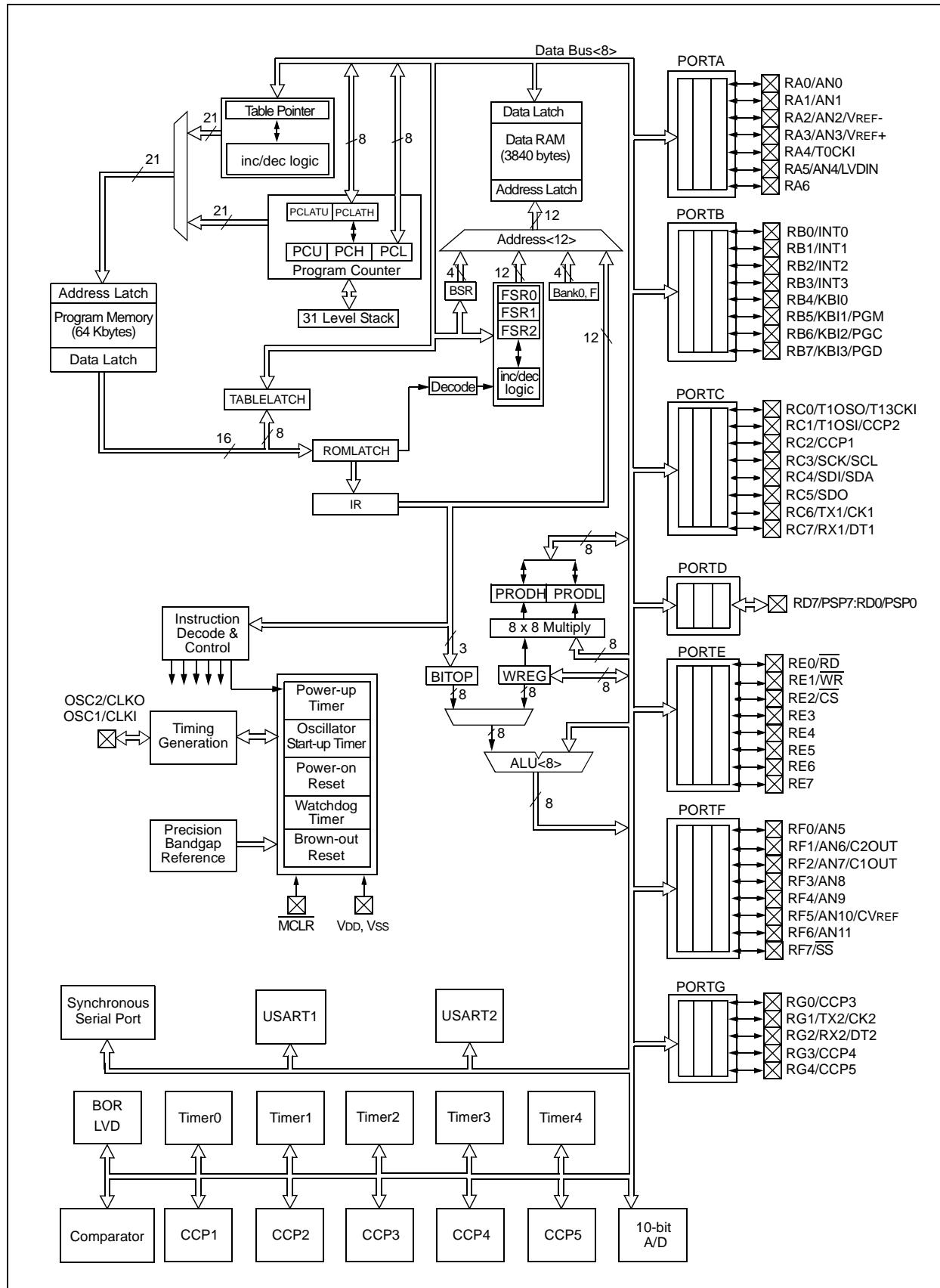
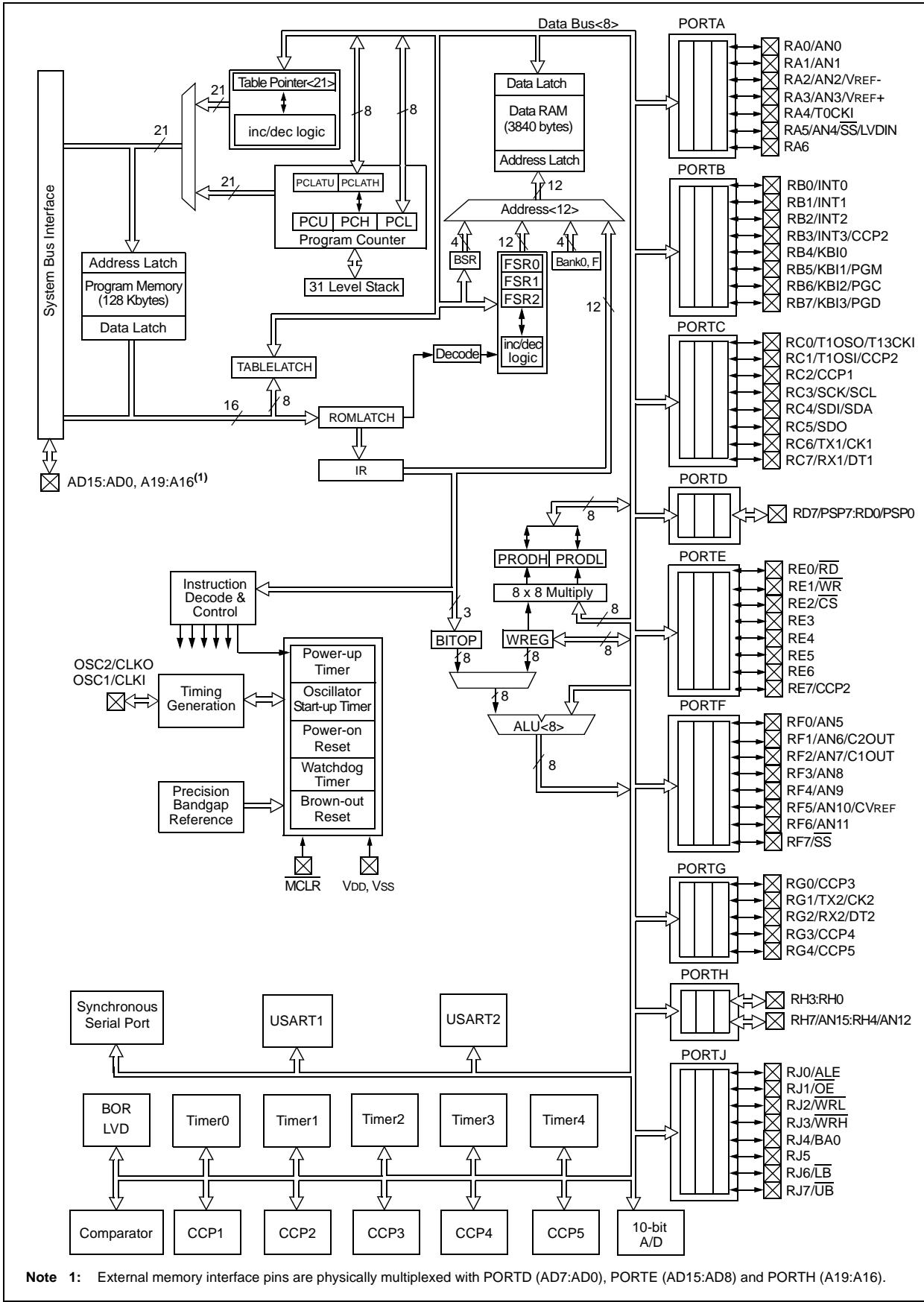


FIGURE 1-2: PIC18F8X20 BLOCK DIAGRAM



PIC18FXX20

TABLE 1-2: PIC18FXX20 PINOUT I/O DESCRIPTIONS

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PIC18F6X20	PIC18F8X20			
MCLR/VPP MCLR VPP	7	9	I P	ST	Master Clear (input) or programming voltage (output). Master Clear (RESET) input. This pin is an active low RESET to the device. Programming voltage input.
OSC1/CLKI OSC1 CLKI	39	49	I	CMOS/ST	Oscillator crystal or external clock input. Oscillator crystal input or external clock source input. ST buffer when configured in RC mode. Otherwise CMOS.
OSC2/CLKO/RA6 OSC2 CLKO	40	50	O O	— —	External clock source input. Always associated with pin function OSC1 (see OSC1/CLKI, OSC2/CLKO pins). Oscillator crystal or clock output. Oscillator crystal output. Connects to crystal or resonator in Crystal Oscillator mode. In RC mode, OSC2 pin outputs CLKO, which has 1/4 the frequency of OSC1 and denotes the instruction cycle rate.
RA6			I/O	TTL	General purpose I/O pin.

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

I = Input

P = Power

CMOS = CMOS compatible input or output

Analog = Analog input

O = Output

OD = Open Drain (no P diode to VDD)

Note 1: Alternate assignment for CCP2 when CCP2MX is not selected (all operating modes except Microcontroller).

2: Default assignment when CCP2MX is set.

3: External memory interface functions are only available on PIC18F8X20 devices.

4: CCP2 is multiplexed with this pin by default when configured in Microcontroller mode. Otherwise, it is multiplexed with either RB3 or RC1.

5: PORTH and PORTJ are only available on PIC18F8X20 (80-pin) devices.

TABLE 1-2: PIC18FXX20 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PIC18F6X20	PIC18F8X20			
RA0/AN0	24	30	I/O	TTL	PORTA is a bi-directional I/O port.
RA0			I	Analog	Digital I/O.
AN0					Analog input 0.
RA1/AN1	23	29	I/O	TTL	Digital I/O.
RA1			I	Analog	Analog input 1.
AN1					
RA2/AN2/VREF-	22	28	I/O	TTL	Digital I/O.
RA2			I	Analog	Analog input 2.
AN2			I	Analog	A/D reference voltage (Low) input.
VREF-					
RA3/AN3/VREF+	21	27	I/O	TTL	Digital I/O.
RA3			I	Analog	Analog input 3.
AN3			I	Analog	A/D reference voltage (High) input.
VREF+					
RA4/T0CKI	28	34	I/O	ST/OD	Digital I/O – Open drain when configured as output.
RA4			I	ST	Timer0 external clock input.
T0CKI					
RA5/AN4/LVDIN	27	33	I/O	TTL	Digital I/O.
RA5			I	Analog	Analog input 4.
AN4			I	Analog	Low voltage detect input.
LVDIN					
RA6					See the OSC2/CLKO/RA6 pin.

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

I = Input

P = Power

CMOS = CMOS compatible input or output

Analog = Analog input

O = Output

OD = Open Drain (no P diode to VDD)

Note 1: Alternate assignment for CCP2 when CCP2MX is not selected (all operating modes except Microcontroller).

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5: PORTH and PORTJ are only available on PIC18F8X20 (80-pin) devices.

PIC18FXX20

TABLE 1-2: PIC18FXX20 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PIC18F6X20	PIC18F8X20			
RB0/INT0 RB0 INT0	48	58	I/O I	TTL ST	PORTB is a bi-directional I/O port. PORTB can be software programmed for internal weak pull-ups on all inputs.
RB1/INT1 RB1 INT1	47	57	I/O I	TTL ST	Digital I/O. External interrupt 0.
RB2/INT2 RB2 INT2	46	56	I/O I	TTL ST	Digital I/O. External interrupt 1.
RB3/INT3/CCP2 RB3 INT3 CCP2 ⁽¹⁾	45	55	I/O I/O I/O	TTL ST ST	Digital I/O. External interrupt 3. Capture2 input, Compare2 output, PWM2 output.
RB4/KBI0 RB4 KBI0	44	54	I/O I	TTL ST	Digital I/O. Interrupt-on-change pin.
RB5/KBI1/PGM RB5 KBI1 PGM	43	53	I/O I I/O	TTL ST ST	Digital I/O. Interrupt-on-change pin. Low voltage ICSP programming enable pin.
RB6/KBI2/PGC RB6 KBI2 PGC	42	52	I/O I I/O	TTL ST ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming clock.
RB7/KBI3/PGD RB7 KBI3 PGD	37	47	I/O I/O	TTL ST	Digital I/O. Interrupt-on-change pin. In-Circuit Debugger and ICSP programming data.

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

I = Input

P = Power

CMOS = CMOS compatible input or output

Analog = Analog input

O = Output

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Note 1: Alternate assignment for CCP2 when CCP2MX is not selected (all operating modes except Microcontroller).

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4: CCP2 is multiplexed with this pin by default when configured in Microcontroller mode. Otherwise, it is multiplexed with either RB3 or RC1.

5: PORTH and PORTJ are only available on PIC18F8X20 (80-pin) devices.

TABLE 1-2: PIC18FXX20 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PIC18F6X20	PIC18F8X20			
RC0/T1OSO/T13CKI RC0 T1OSO T13CKI	30	36	I/O O I	ST — ST	PORTC is a bi-directional I/O port. Digital I/O. Timer1 oscillator output. Timer1/Timer3 external clock input.
RC1/T1OSI/CCP2 RC1 T1OSI CCP2 ⁽²⁾	29	35	I/O I I/O	ST CMOS ST	Digital I/O. Timer1 oscillator input. Capture2 input, Compare2 output, PWM2 output.
RC2/CCP1 RC2 CCP1	33	43	I/O I/O	ST ST	Digital I/O. Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL RC3 SCK SCL	34	44	I/O I/O I/O	ST ST ST	Digital I/O. Synchronous serial clock input/output for SPI mode. Synchronous serial clock input/output for I ² C mode.
RC4/SDI/SDA RC4 SDI SDA	35	45	I/O I I/O	ST ST ST	Digital I/O. SPI data in. I ² C data I/O.
RC5/SDO RC5 SDO	36	46	I/O O	ST —	Digital I/O. SPI data out.
RC6/TX1/CK1 RC6 TX1 CK1	31	37	I/O O I/O	ST — ST	Digital I/O. USART 1 asynchronous transmit. USART 1 synchronous clock (see RX1/DT1).
RC7/RX1/DT1 RC7 RX1 DT1	32	38	I/O I I/O	ST ST ST	Digital I/O. USART 1 asynchronous receive. USART 1 synchronous data (see TX1/CK1).

Legend: TTL = TTL compatible input

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PIC18FXX20

TABLE 1-2: PIC18FXX20 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PIC18F6X20	PIC18F8X20			
RD0/PSP0/AD0 RD0 PSP0 AD0 ⁽³⁾	58	72	I/O	ST	PORTD is a bi-directional I/O port. These pins have TTL input buffers when external memory is enabled.
RD1/PSP1/AD1 RD1 PSP1 AD1 ⁽³⁾	55	69	I/O	TTL	Digital I/O. Parallel Slave Port data. External memory address/data 0.
RD2/PSP2/AD2 RD2 PSP2 AD2 ⁽³⁾	54	68	I/O	ST	Digital I/O. Parallel Slave Port data. External memory address/data 1.
RD3/PSP3/AD3 RD3 PSP3 AD3 ⁽³⁾	53	67	I/O	TTL	Digital I/O. Parallel Slave Port data. External memory address/data 2.
RD4/PSP4/AD4 RD4 PSP4 AD4 ⁽³⁾	52	66	I/O	ST	Digital I/O. Parallel Slave Port data. External memory address/data 3.
RD5/PSP5/AD5 RD5 PSP5 AD5 ⁽³⁾	51	65	I/O	TTL	Digital I/O. Parallel Slave Port data. External memory address/data 4.
RD6/PSP6/AD6 RD6 PSP6 AD6 ⁽³⁾	50	64	I/O	ST	Digital I/O. Parallel Slave Port data. External memory address/data 5.
RD7/PSP7/AD7 RD7 PSP7 AD7 ⁽³⁾	49	63	I/O	TTL	Digital I/O. Parallel Slave Port data. External memory address/data 6.

Legend: TTL = TTL compatible input

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TABLE 1-2: PIC18FXX20 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PIC18F6X20	PIC18F8X20			
RE0/ <u>RD</u> /AD8 RE0 <u>RD</u>	2	4	I/O I	ST TTL	PORTE is a bi-directional I/O port. Digital I/O. Read control for parallel slave port (see WR and CS pins).
AD8 ⁽³⁾			I/O	TTL	External memory address/data 8
RE1/ <u>WR</u> /AD9 RE1 <u>WR</u>	1	3	I/O I	ST TTL	Digital I/O. Write control for parallel slave port (see CS and RD pins).
AD9 ⁽³⁾			I/O	TTL	External memory address/data 9.
RE2/ <u>CS</u> /AD10 RE2 <u>CS</u>	64	78	I/O I	ST TTL	Digital I/O. Chip select control for parallel slave port (see RD and WR).
AD10 ⁽³⁾			I/O	TTL	External memory address/data 10.
RE3/AD11 RE3 AD11 ⁽³⁾	63	77	I/O I/O	ST TTL	Digital I/O. External memory address/data 11.
RE4/AD12 RE4 AD12	62	76	I/O I/O	ST TTL	Digital I/O. External memory address/data 12.
RE5/AD13 RE5 AD13 ⁽³⁾	61	75	I/O I/O	ST TTL	Digital I/O. External memory address/data 13.
RE6/AD14 RE6 AD14 ⁽³⁾	60	74	I/O I/O	ST TTL	Digital I/O. External memory address/data 14.
RE7/CCP2/AD15 RE7 CCP2 ^(1,4)	59	73	I/O I/O	ST ST	Digital I/O. Capture2 input, Compare2 output, PWM2 output.
AD15 ⁽³⁾			I/O	TTL	External memory address/data 15.

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I = Input

P = Power

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Analog = Analog input

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5: PORTH and PORTJ are only available on PIC18F8X20 (80-pin) devices.

PIC18FXX20

TABLE 1-2: PIC18FXX20 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PIC18F6X20	PIC18F8X20			
RF0/AN5 RF0 AN5	18	24	I/O I	ST Analog	PORTF is a bi-directional I/O port. Digital I/O. Analog input 5.
RF1/AN6/C2OUT RF1 AN6 C2OUT	17	23	I/O I O	ST Analog ST	Digital I/O. Analog input 6. Comparator 2 output.
RF2/AN7/C1OUT RF2 AN7 C1OUT	16	18	I/O I O	ST Analog ST	Digital I/O. Analog input 7. Comparator 1 output.
RF3/AN8 RF1 AN8	15	17	I/O I	ST Analog	Digital I/O. Analog input 8.
RF4/AN9 RF1 AN9	14	16	I/O I	ST Analog	Digital I/O. Analog input 9.
RF5/AN10/CVREF RF1 AN10 CVREF	13	15	I/O I O	ST Analog Analog	Digital I/O. Analog input 10. Comparator VREF output.
RF6/AN11 RF6 AN11	12	14	I/O I	ST Analog	Digital I/O. Analog input 11.
RF7/SS RF7 SS	11	13	I/O I	ST TTL	Digital I/O. SPI slave select input.

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

I = Input

P = Power

CMOS = CMOS compatible input or output

Analog = Analog input

O = Output

OD = Open Drain (no P diode to VDD)

Note 1: Alternate assignment for CCP2 when CCP2MX is not selected (all operating modes except Microcontroller).

2: Default assignment when CCP2MX is set.

3: External memory interface functions are only available on PIC18F8X20 devices.

4: CCP2 is multiplexed with this pin by default when configured in Microcontroller mode. Otherwise, it is multiplexed with either RB3 or RC1.

5: PORTH and PORTJ are only available on PIC18F8X20 (80-pin) devices.

TABLE 1-2: PIC18FXX20 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PIC18F6X20	PIC18F8X20			
RG0/CCP3 RG0 CCP3	3	5	I/O I/O	ST ST	PORTG is a bi-directional I/O port. Digital I/O. Capture3 input/Compare3 output/ PWM3 output.
RG1/TX2/CK2 RG1 TX2 CK2	4	6	I/O O I/O	ST — ST	Digital I/O. USART 2 asynchronous transmit. USART 2 synchronous clock (see RX2/DT2).
RG2/RX2/DT2 RG2 RX2 DT2	5	7	I/O I I/O	ST ST ST	Digital I/O. USART 2 asynchronous receive. USART 2 synchronous data (see TX2/CK2).
RG3/CCP4 RG3 CCP4	6	8	I/O I/O	ST ST	Digital I/O. Capture4 input/Compare4 output/ PWM4 output.
RG4/CCP5 RG4 CCP5	8	10	I/O I/O	ST ST	Digital I/O. Capture5 input/Compare5 output/ PWM5 output.

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

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P = Power

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Analog = Analog input

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PIC18FXX20

TABLE 1-2: PIC18FXX20 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PIC18F6X20	PIC18F8X20			
RH0/A16	—	79	I/O	ST	PORTh is a bi-directional I/O port ⁽⁵⁾ .
RH0	—		O	TTL	Digital I/O.
A16	—				External memory address 16.
RH1/A17	—	80	I/O	ST	Digital I/O.
RH1	—		O	TTL	External memory address 17.
A17	—				
RH2/A18	—	1	I/O	ST	Digital I/O.
RH2	—		O	TTL	External memory address 18.
A18	—				
RH3/A19	—	2	I/O	ST	Digital I/O.
RH3	—		O	TTL	External memory address 19.
A19	—				
RH4/AN12	—	22	I/O	ST	Digital I/O.
RH4	—		I	Analog	Analog input 12.
AN12	—				
RH5/AN13	—	21	I/O	ST	Digital I/O.
RH5	—		I	Analog	Analog input 13.
AN13	—				
RH6/AN14	—	20	I/O	ST	Digital I/O.
RH6	—		I	Analog	Analog input 14.
AN14	—				
RH7/AN15	—	19	I/O	ST	Digital I/O.
RH7	—		I	Analog	Analog input 15.
AN15	—				

Legend: TTL = TTL compatible input

ST = Schmitt Trigger input with CMOS levels

I = Input

P = Power

CMOS = CMOS compatible input or output

Analog = Analog input

O = Output

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5: PORTh and PORTJ are only available on PIC18F8X20 (80-pin) devices.

TABLE 1-2: PIC18FXX20 PINOUT I/O DESCRIPTIONS (CONTINUED)

Pin Name	Pin Number		Pin Type	Buffer Type	Description
	PIC18F6X20	PIC18F8X20			
RJ0/ALE	—	62	I/O	ST	PORTJ is a bi-directional I/O port ⁽⁵⁾ .
RJ0	—		O	TTL	Digital I/O.
ALE	—				External memory Address Latch Enable.
RJ1/ <u>OE</u>	—	61	I/O	ST	Digital I/O.
RJ1	—		O	TTL	External memory Output Enable.
<u>OE</u>	—				
RJ2/ <u>WRL</u>	—	60	I/O	ST	Digital I/O.
RJ2	—		O	TTL	External memory Write Low control.
<u>WRL</u>	—				
RJ3/ <u>WRH</u>	—	59	I/O	ST	Digital I/O.
RJ3	—		O	TTL	External memory Write High control.
<u>WRH</u>	—				
RJ4/BA0	—	39	I/O	ST	Digital I/O.
RJ4	—		O	TTL	System bus byte address 0 control.
BA0	—				
RJ5	—	40	I/O	ST	Digital I/O
RJ6/ <u>LB</u>	—	42	I/O	ST	Digital I/O.
RJ6	—		O	TTL	External memory Low Byte select.
<u>LB</u>	—				
RJ7/ <u>UB</u>	—	41	I/O	ST	Digital I/O.
RJ7	—		O	TTL	External memory High Byte select.
<u>UB</u>	—				
Vss	9, 25, 41, 56	11, 31, 51, 70	P	—	Ground reference for logic and I/O pins.
VDD	10, 26, 38, 57	12, 32, 48, 71	P	—	Positive supply for logic and I/O pins.
AVss	20	26	P	—	Ground reference for analog modules.
AVDD	19	25	P	—	Positive supply for analog modules.

Legend: TTL = TTL compatible input

CMOS = CMOS compatible input or output

ST = Schmitt Trigger input with CMOS levels

Analog = Analog input

I = Input

O = Output

P = Power

OD = Open Drain (no P diode to VDD)

Note 1: Alternate assignment for CCP2 when CCP2MX is not selected (all operating modes except Microcontroller).

2: Default assignment when CCP2MX is set.

3: External memory interface functions are only available on PIC18F8X20 devices.

4: CCP2 is multiplexed with this pin by default when configured in Microcontroller mode. Otherwise, it is multiplexed with either RB3 or RC1.

5: PORTH and PORTJ are only available on PIC18F8X20 (80-pin) devices.

PIC18FXX20

NOTES:

2.0 OSCILLATOR CONFIGURATIONS

2.1 Oscillator Types

The PIC18FXX20 devices can be operated in eight different oscillator modes. The user can program three configuration bits (FOSC2, FOSC1, and FOSC0) to select one of these eight modes:

1. LP Low Power Crystal
2. XT Crystal/Resonator
3. HS High Speed Crystal/Resonator
4. HS+PLL High Speed Crystal/Resonator with PLL enabled
5. RC External Resistor/Capacitor
6. RCIO External Resistor/Capacitor with I/O pin enabled
7. EC External Clock
8. ECIO External Clock with I/O pin enabled

2.2 Crystal Oscillator/Ceramic Resonators

In XT, LP, HS or HS+PLL oscillator modes, a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation. Figure 2-1 shows the pin connections.

The PIC18FXX20 oscillator design requires the use of a parallel cut crystal.

Note: Use of a series cut crystal may give a frequency out of the crystal manufacturers specifications.

FIGURE 2-1: CRYSTAL/CERAMIC RESONATOR OPERATION (HS, XT OR LP CONFIGURATION)

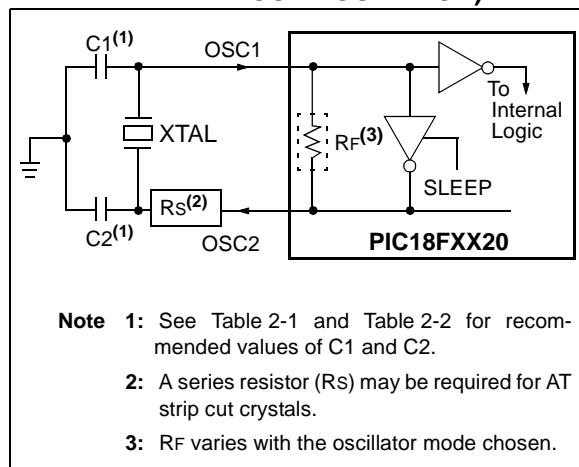


TABLE 2-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Ranges Tested:			
Mode	Freq	C1	C2
XT	455 kHz	68 - 100 pF	68 - 100 pF
	2.0 MHz	15 - 68 pF	15 - 68 pF
	4.0 MHz	15 - 68 pF	15 - 68 pF
HS	8.0 MHz	10 - 68 pF	10 - 68 pF
	16.0 MHz	10 - 22 pF	10 - 22 pF

These values are for design guidance only.
See notes following this table.

Resonators Used:		
455 kHz	Panasonic EFO-A455K04B	$\pm 0.3\%$
2.0 MHz	Murata Erie CSA2.00MG	$\pm 0.5\%$
4.0 MHz	Murata Erie CSA4.00MG	$\pm 0.5\%$
8.0 MHz	Murata Erie CSA8.00MT	$\pm 0.5\%$
16.0 MHz	Murata Erie CSA16.00MX	$\pm 0.5\%$

All resonators used did not have built-in capacitors.

Note 1: Higher capacitance increases the stability of the oscillator, but also increases the start-up time.

2: When operating below 3V VDD, or when using certain ceramic resonators at any voltage, it may be necessary to use high gain HS mode, try a lower frequency resonator, or switch to a crystal oscillator.

3: Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components, or verify oscillator performance.

PIC18FXX20

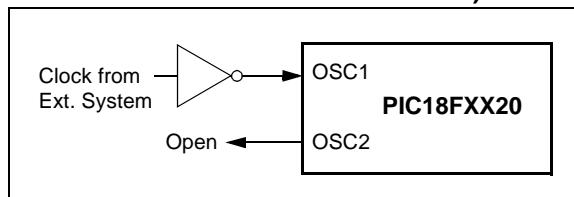
TABLE 2-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Ranges Tested:			
Mode	Freq	C1	C2
LP	32.0 kHz	33 pF	33 pF
	200 kHz	15 pF	15 pF
XT	200 kHz	47-68 pF	47-68 pF
	1.0 MHz	15 pF	15 pF
	4.0 MHz	15 pF	15 pF
HS	4.0 MHz	15 pF	15 pF
	8.0 MHz	15-33 pF	15-33 pF
	20.0 MHz	15-33 pF	15-33 pF
	25.0 MHz	TBD	TBD
These values are for design guidance only. See notes following this table.			
Crystals Used			
32.0 kHz	Epson C-001R32.768K-A	± 20 PPM	
200 kHz	STD XTL 200.000KHz	± 20 PPM	
1.0 MHz	ECS ECS-10-13-1	± 50 PPM	
4.0 MHz	ECS ECS-40-20-1	± 50 PPM	
8.0 MHz	Epson CA-301 8.000M-C	± 30 PPM	
20.0 MHz	Epson CA-301 20.000M-C	± 30 PPM	

- Note 1:** Higher capacitance increases the stability of the oscillator, but also increases the start-up time.
- 2:** R_s (see Figure 2-1) may be required in HS mode, as well as XT mode, to avoid overdriving crystals with low drive level specification.
- 3:** Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components., or verify oscillator performance.

An external clock source may also be connected to the OSC1 pin in the HS, XT and LP modes, as shown in Figure 2-2.

FIGURE 2-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT OR LP OSC CONFIGURATION)

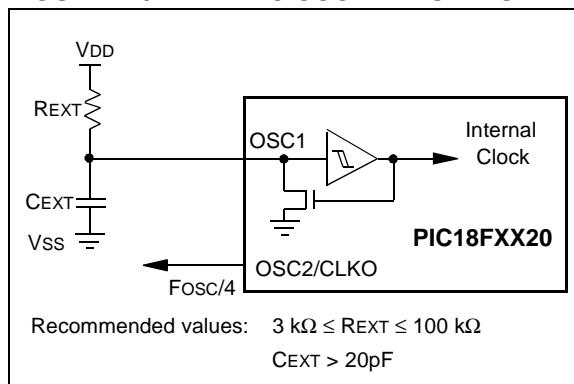


2.3 RC Oscillator

For timing insensitive applications, the “RC” and “RCIO” device options offer additional cost savings. The RC oscillator frequency is a function of the supply voltage, the resistor (R_{EXT}) and capacitor (C_{EXT}) values and the operating temperature. In addition to this, the oscillator frequency will vary from unit to unit, due to normal process parameter variation. Furthermore, the difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low C_{EXT} values. The user also needs to take into account variation due to tolerance of external R and C components used. Figure 2-3 shows how the R/C combination is connected.

In the RC oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic.

FIGURE 2-3: RC OSCILLATOR MODE



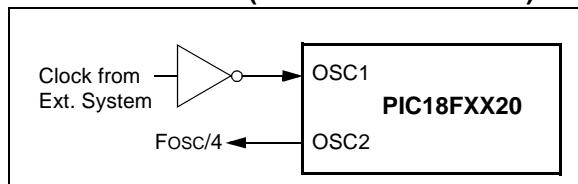
The RCIO oscillator mode functions like the RC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6).

2.4 External Clock Input

The EC and ECIO oscillator modes require an external clock source to be connected to the OSC1 pin. The feedback device between OSC1 and OSC2 is turned off in these modes to save current. There is a maximum 1.5 μ s start-up required after a Power-on Reset, or Wake-up from SLEEP mode.

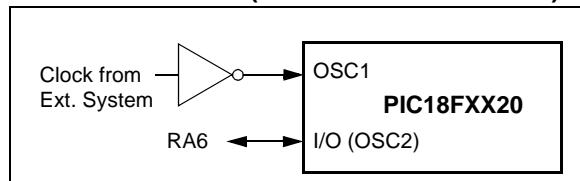
In the EC oscillator mode, the oscillator frequency divided by 4 is available on the OSC2 pin. This signal may be used for test purposes or to synchronize other logic. Figure 2-4 shows the pin connections for the EC oscillator mode.

FIGURE 2-4: EXTERNAL CLOCK INPUT OPERATION (EC CONFIGURATION)



The ECIO oscillator mode functions like the EC mode, except that the OSC2 pin becomes an additional general purpose I/O pin. The I/O pin becomes bit 6 of PORTA (RA6). Figure 2-5 shows the pin connections for the ECIO oscillator mode.

FIGURE 2-5: EXTERNAL CLOCK INPUT OPERATION (ECIO CONFIGURATION)



2.5 HS/PLL

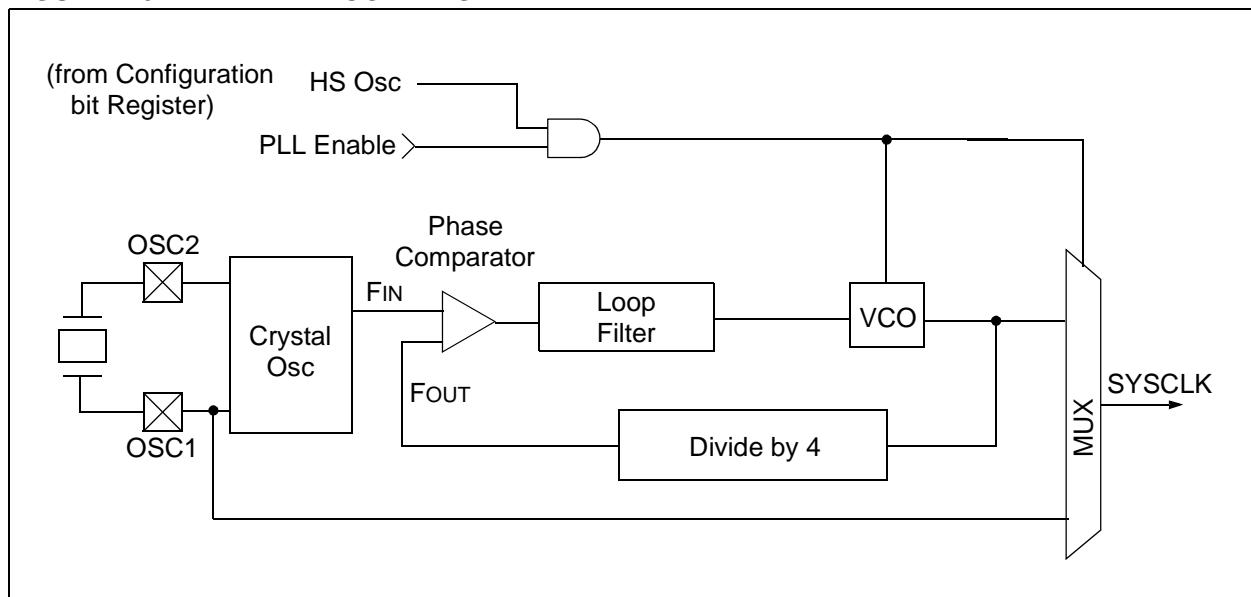
A Phase Locked Loop circuit is provided as a programmable option for users that want to multiply the frequency of the incoming crystal oscillator signal by 4. For an input clock frequency of 10 MHz, the internal clock frequency will be multiplied to 40 MHz. This is useful for customers who are concerned with EMI due to high frequency crystals.

The PLL can only be enabled when the oscillator configuration bits are programmed for HS mode. If they are programmed for any other mode, the PLL is not enabled and the system clock will come directly from OSC1.

The PLL is one of the modes of the FOSC<2:0> configuration bits. The oscillator mode is specified during device programming.

A PLL lock timer is used to ensure that the PLL has locked before device execution starts. The PLL lock timer has a time-out that is called TPLL.

FIGURE 2-6: PLL BLOCK DIAGRAM

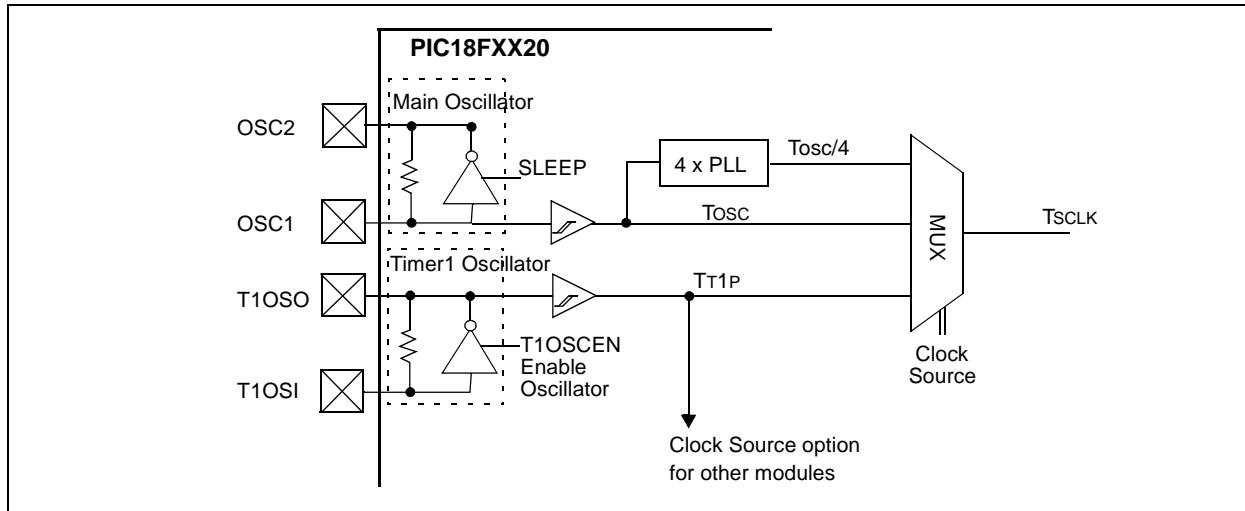


2.6 Oscillator Switching Feature

The PIC18FXX20 devices include a feature that allows the system clock source to be switched from the main oscillator to an alternate low frequency clock source. For the PIC18FXX20 devices, this alternate clock source is the Timer1 oscillator. If a low frequency crystal (32 kHz, for example) has been attached to the Timer1 oscillator pins and the Timer1 oscillator has been enabled, the device can switch to a low power

execution mode. Figure 2-7 shows a block diagram of the system clock sources. The clock switching feature is enabled by programming the Oscillator Switching Enable (OSCSEN) bit in Configuration Register1H to a '0'. Clock switching is disabled in an erased device. See Section 12.0 for further details of the Timer1 oscillator. See Section 23.0 for Configuration Register details.

FIGURE 2-7: DEVICE CLOCK SOURCES



2.6.1 SYSTEM CLOCK SWITCH BIT

The system clock source switching is performed under software control. The system clock switch bit, SCS (OSCCON<0>) controls the clock switching. When the SCS bit is '0', the system clock source comes from the main oscillator that is selected by the FOSC configuration bits in Configuration Register1H. When the SCS bit is set, the system clock source will come from the Timer1 oscillator. The SCS bit is cleared on all forms of RESET.

Note: The Timer1 oscillator must be enabled and operating to switch the system clock source. The Timer1 oscillator is enabled by setting the T1OSCEN bit in the Timer1 control register (T1CON). If the Timer1 oscillator is not enabled, then any write to the SCS bit will be ignored (SCS bit forced cleared) and the main oscillator will continue to be the system clock source.

REGISTER 2-1: OSCCON REGISTER

U-0	R/W-1						
—	—	—	—	—	—	—	SCS bit 0

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **SCS:** System Clock Switch bit

When OSCSEN configuration bit = '0' and T1OSCEN bit is set:

1 = Switch to Timer1 oscillator/clock pin

0 = Use primary oscillator/clock input pin

When OSCSEN and T1OSCEN are in other states:

bit is forced clear

Legend:

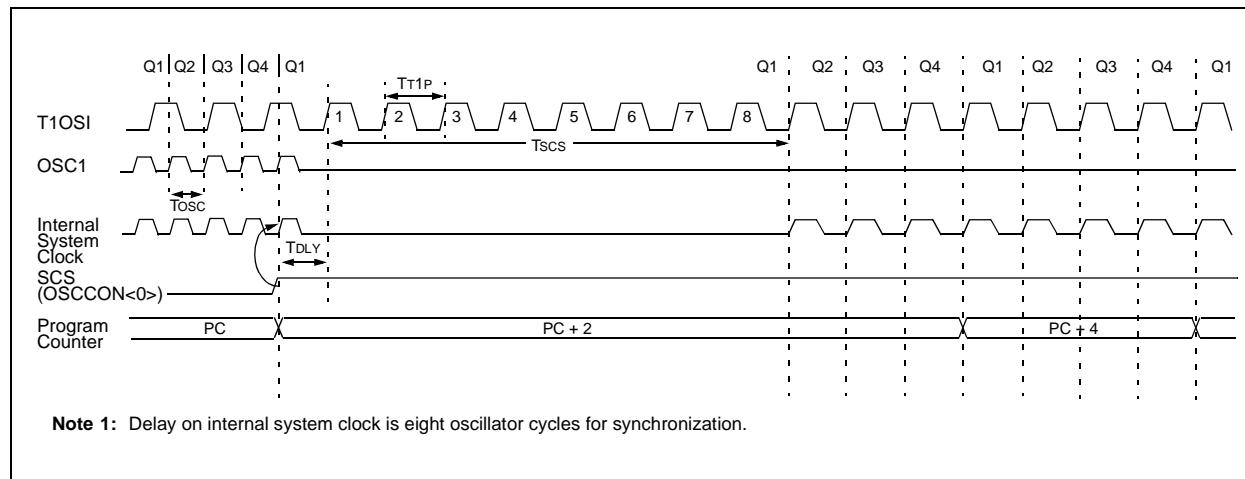
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

2.6.2 OSCILLATOR TRANSITIONS

PIC18FXX20 devices contain circuitry to prevent "glitches" when switching between oscillator sources. Essentially, the circuitry waits for eight rising edges of the clock source that the processor is switching to. This ensures that the new clock source is stable and that its pulse width will not be less than the shortest pulse width of the two clock sources.

A timing diagram indicating the transition from the main oscillator to the Timer1 oscillator is shown in Figure 2-8. The Timer1 oscillator is assumed to be running all the time. After the SCS bit is set, the processor is frozen at the next occurring Q1 cycle. After eight synchronization cycles are counted from the Timer1 oscillator, operation resumes. No additional delays are required after the synchronization cycles.

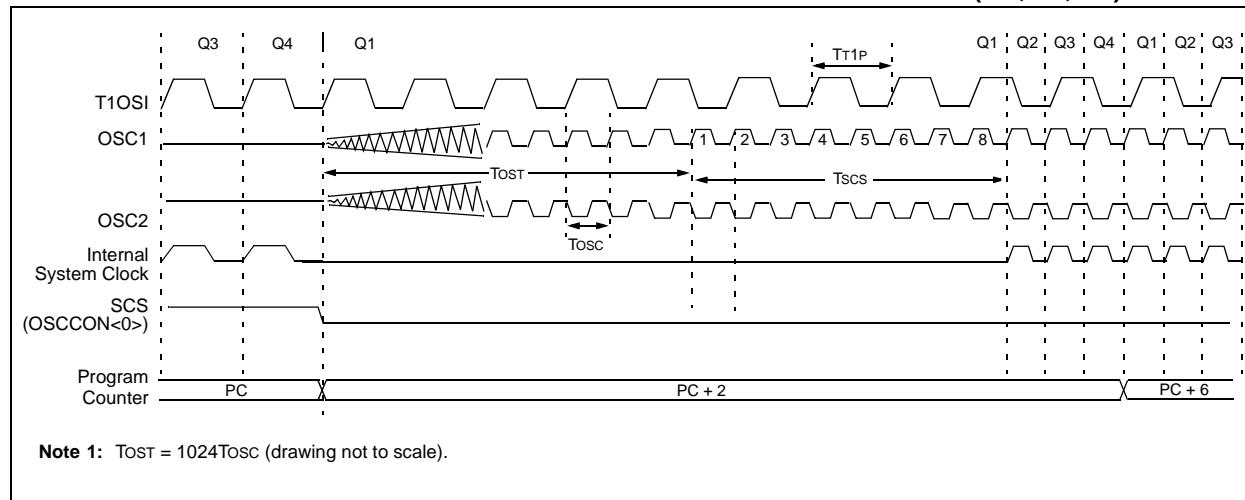
FIGURE 2-8: TIMING DIAGRAM FOR TRANSITION FROM OSC1 TO TIMER1 OSCILLATOR



The sequence of events that takes place when switching from the Timer1 oscillator to the main oscillator will depend on the mode of the main oscillator. In addition to eight clock cycles of the main oscillator, additional delays may take place.

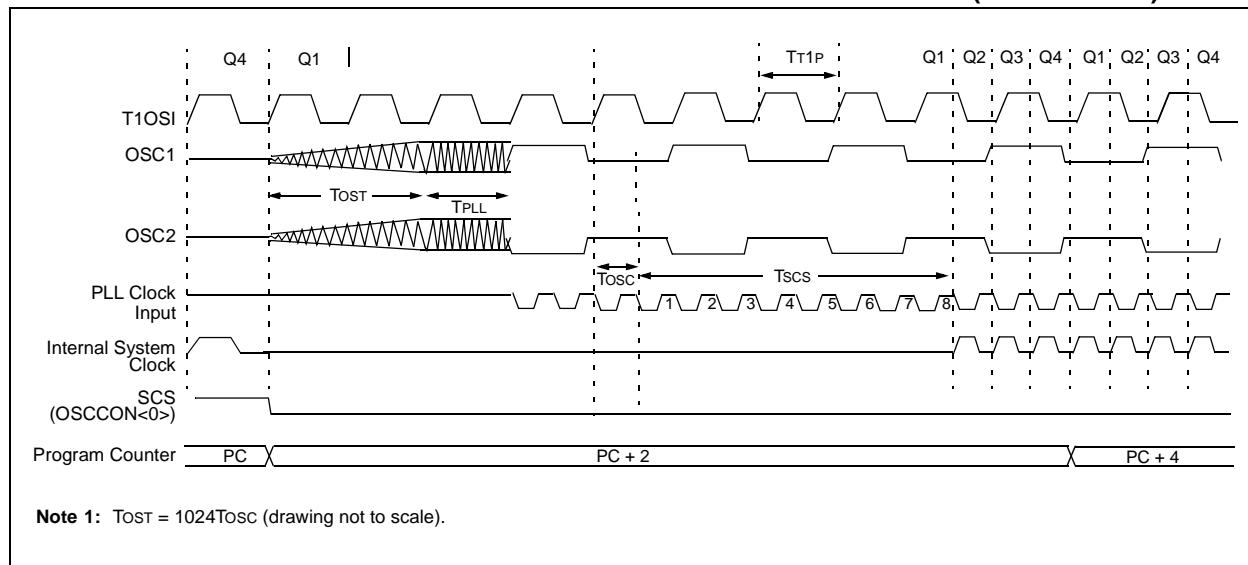
If the main oscillator is configured for an external crystal (HS, XT, LP), then the transition will take place after an oscillator start-up time (TOST) has occurred. A timing diagram, indicating the transition from the Timer1 oscillator to the main oscillator for HS, XT and LP modes, is shown in Figure 2-9.

FIGURE 2-9: TIMING FOR TRANSITION BETWEEN TIMER1 AND OSC1 (HS, XT, LP)



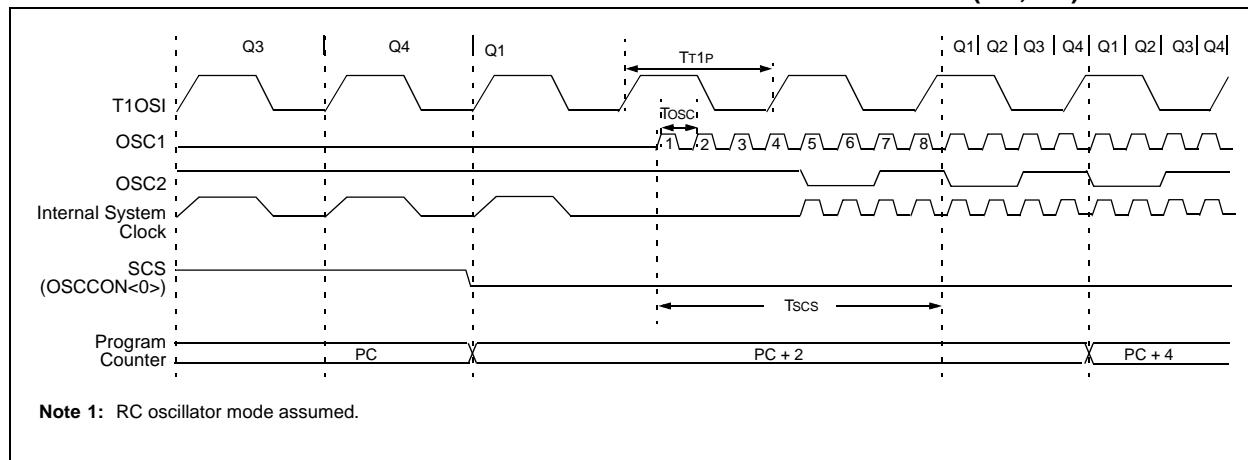
If the main oscillator is configured for HS-PLL mode, an oscillator start-up time (T_{OST}), plus an additional PLL time-out (T_{PLL}), will occur. The PLL time-out is typically 2 ms and allows the PLL to lock to the main oscillator frequency. A timing diagram, indicating the transition from the Timer1 oscillator to the main oscillator for HS-PLL mode, is shown in Figure 2-10.

FIGURE 2-10: TIMING FOR TRANSITION BETWEEN TIMER1 AND OSC1 (HS WITH PLL)



If the main oscillator is configured in the RC, RCIO, EC or ECIO modes, there is no oscillator start-up time-out. Operation will resume after eight cycles of the main oscillator have been counted. A timing diagram, indicating the transition from the Timer1 oscillator to the main oscillator for RC, RCIO, EC and ECIO modes, is shown in Figure 2-11.

FIGURE 2-11: TIMING FOR TRANSITION BETWEEN TIMER1 AND OSC1 (RC, EC)



2.7 Effects of SLEEP Mode on the On-Chip Oscillator

When the device executes a SLEEP instruction, the on-chip clocks and oscillator are turned off and the device is held at the beginning of an instruction cycle (Q1 state). With the oscillator off, the OSC1 and OSC2 signals will stop oscillating. Since all the transistor

switching currents have been removed, SLEEP mode achieves the lowest current consumption of the device (only leakage currents). Enabling any on-chip feature that will operate during SLEEP, will increase the current consumed during SLEEP. The user can wake from SLEEP through external RESET, Watchdog Timer Reset, or through an interrupt.

TABLE 2-3: OSC1 AND OSC2 PIN STATES IN SLEEP MODE

OSC Mode	OSC1 Pin	OSC2 Pin
RC	Floating, external resistor should pull high	At logic low
RCIO	Floating, external resistor should pull high	Configured as PORTA, bit 6
ECIO	Floating	Configured as PORTA, bit 6
EC	Floating	At logic low
LP, XT, and HS	Feedback inverter disabled, at quiescent voltage level	Feedback inverter disabled, at quiescent voltage level

Note: See Table 3-1 in the “Reset” section, for time-outs due to SLEEP and MCLR Reset.

2.8 Power-up Delays

Power up delays are controlled by two timers, so that no external RESET circuitry is required for most applications. The delays ensure that the device is kept in RESET, until the device power supply and clock are stable. For additional information on RESET operation, see the “Reset” section.

The first timer is the Power-up Timer (PWRT), which optionally provides a fixed delay of 72 ms (nominal) on power-up only (POR and BOR). The second timer is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable.

With the PLL enabled (HS/PLL oscillator mode), the time-out sequence following a Power-on Reset is different from other oscillator modes. The time-out sequence is as follows: First, the PWRT time-out is invoked after a POR time delay has expired. Then, the Oscillator Start-up Timer (OST) is invoked. However, this is still not a sufficient amount of time to allow the PLL to lock at high frequencies. The PWRT timer is used to provide an additional fixed 2ms (nominal) time-out to allow the PLL ample time to lock to the incoming clock frequency.

3.0 RESET

The PIC18FXX20 devices differentiate between various kinds of RESET:

- a) Power-on Reset (POR)
- b) MCLR Reset during normal operation
- c) MCLR Reset during SLEEP
- d) Watchdog Timer (WDT) Reset (during normal operation)
- e) Programmable Brown-out Reset (BOR)
- f) RESET Instruction
- g) Stack Full Reset
- h) Stack Underflow Reset

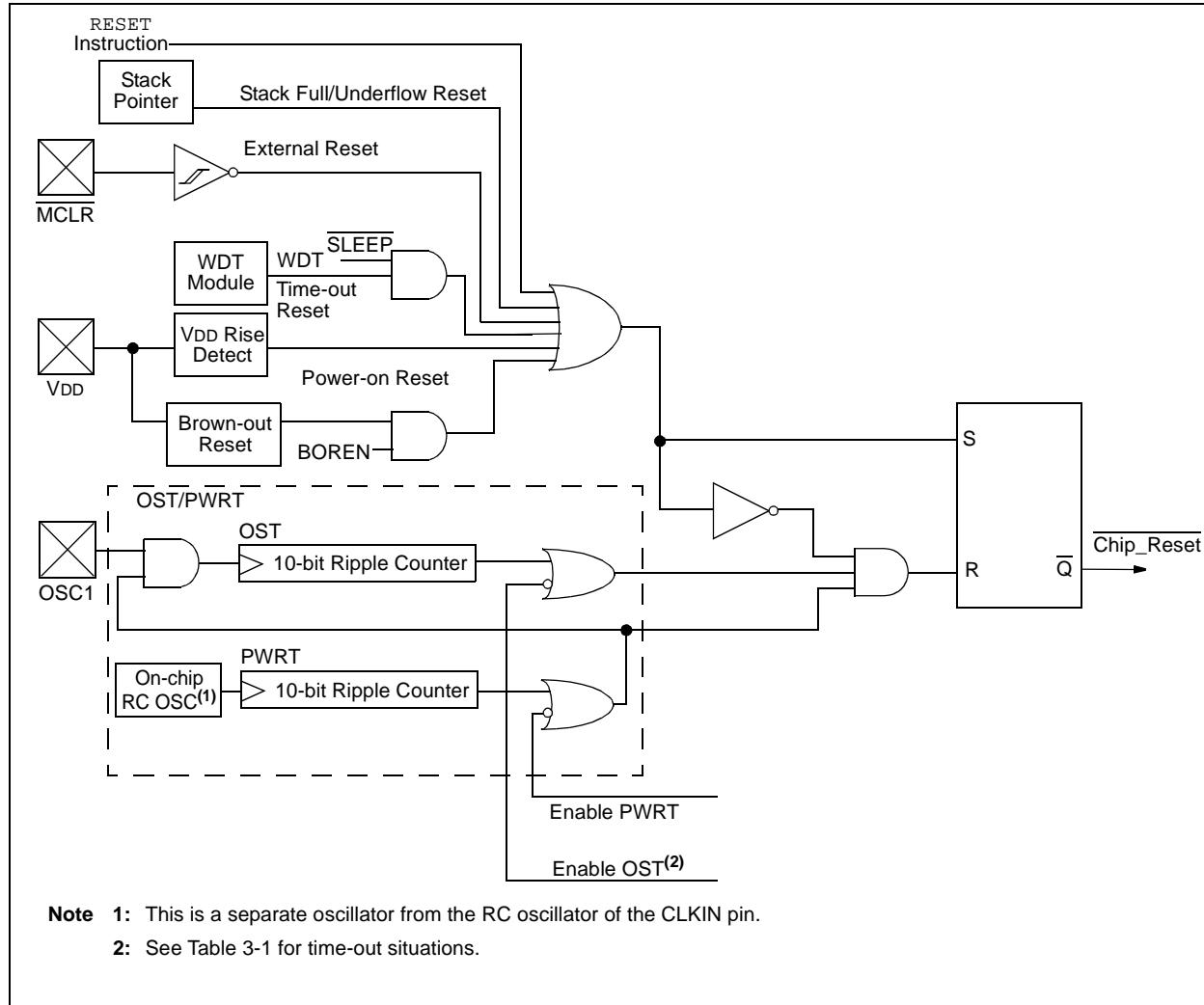
Most registers are unaffected by a RESET. Their status is unknown on POR and unchanged by all other RESETS. The other registers are forced to a "RESET state" on Power-on Reset, MCLR, WDT Reset, Brown-out Reset, MCLR Reset during SLEEP and by the RESET instruction.

Most registers are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. Status bits from the RCON register, RI, TO, PD, POR and BOR, are set or cleared differently in different RESET situations, as indicated in Table 3-2. These bits are used in software to determine the nature of the RESET. See Table 3-3 for a full description of the RESET states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 3-1.

The Enhanced MCU devices have a MCLR noise filter in the MCLR Reset path. The filter will detect and ignore small pulses. The MCLR pin is not driven low by any internal RESETS, including the WDT.

FIGURE 3-1: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT

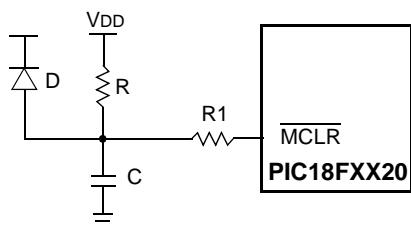


3.1 Power-On Reset (POR)

A Power-on Reset pulse is generated on-chip when VDD rise is detected. To take advantage of the POR circuitry, tie the MCLR pin through a 1 k Ω to 10 k Ω resistor to VDD. This will eliminate external RC components usually needed to create a Power-on Reset delay. A minimum rise rate for VDD is specified (parameter D004). For a slow rise time, see Figure 3-2.

When the device starts normal operation (i.e., exits the RESET condition), device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

FIGURE 3-2: EXTERNAL POWER-ON RESET CIRCUIT (FOR SLOW VDD POWER-UP)



- Note 1:** External Power-on Reset circuit is required only if the VDD power-up slope is too slow. The diode D helps discharge the capacitor quickly when VDD powers down.
- 2:** R < 40 k Ω is recommended to make sure that the voltage drop across R does not violate the device's electrical specification.
- 3:** R1 = 1 k Ω to 10 k Ω will limit any current flowing into MCLR from external capacitor C, in the event of MCLR/VPP pin breakdown due to Electrostatic Discharge (ESD) or Electrical Overstress (EOS).

3.2 Power-up Timer (PWRT)

The Power-up Timer provides a fixed nominal time-out (parameter #33) only on power-up from the POR. The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as the PWRT is active. The PWRT's time delay allows VDD to rise to an acceptable level. A configuration bit is provided to enable/disable the PWRT.

The power-up time delay will vary from chip-to-chip due to VDD, temperature and process variation. See DC parameter #33 for details.

3.3 Oscillator Start-up Timer (OST)

The Oscillator Start-up Timer (OST) provides 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over (parameter #32). This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset, or wake-up from SLEEP.

3.4 PLL Lock Time-out

With the PLL enabled, the time-out sequence following a Power-on Reset is different from other oscillator modes. A portion of the Power-up Timer is used to provide a fixed time-out that is sufficient for the PLL to lock to the main oscillator frequency. This PLL lock time-out (TPLL) is typically 2 ms and follows the oscillator start-up time-out (OST).

3.5 Brown-out Reset (BOR)

A configuration bit, BOREN, can disable (if clear/programmed) or enable (if set) the Brown-out Reset circuitry. If VDD falls below parameter D005 for greater than parameter #35, the brown-out situation will reset the chip. A RESET may not occur if VDD falls below parameter D005 for less than parameter #35. The chip will remain in Brown-out Reset until VDD rises above BVDD. If the Power-up Timer is enabled, it will be invoked after VDD rises above BVDD; it then will keep the chip in RESET for an additional time delay (parameter #33). If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Reset and the Power-up Timer will be initialized. Once VDD rises above BVDD, the Power-up Timer will execute the additional time delay.

3.6 Time-out Sequence

On power-up, the time-out sequence is as follows: First, PWRT time-out is invoked after the POR time delay has expired. Then, OST is activated. The total time-out will vary based on oscillator configuration and the status of the PWRT. For example, in RC mode with the PWRT disabled, there will be no time-out at all. Figure 3-3, Figure 3-4, Figure 3-5, Figure 3-6 and Figure 3-7 depict time-out sequences on power-up.

Since the time-outs occur from the POR pulse, the time-outs will expire if MCLR is kept low long enough. Bringing MCLR high will begin execution immediately (Figure 3-5). This is useful for testing purposes or to synchronize more than one PIC18FXX20 device operating in parallel.

Table 3-2 shows the RESET conditions for some Special Function Registers, while Table 3-3 shows the RESET conditions for all of the registers.

TABLE 3-1: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up ⁽²⁾		Brown-out	Wake-up from SLEEP or Oscillator Switch
	PWRTE = 0	PWRTE = 1		
HS with PLL enabled ⁽¹⁾	72 ms + 1024Tosc + 2ms	1024Tosc + 2 ms	72 ms ⁽²⁾ + 1024Tosc + 2 ms	1024Tosc + 2 ms
HS, XT, LP	72 ms + 1024Tosc	1024TOSC	72 ms ⁽²⁾ + 1024Tosc	1024TOSC
EC	72 ms	1.5 μ s	72 ms ⁽²⁾	1.5 μ s ⁽³⁾
External RC	72 ms	—	72 ms ⁽²⁾	—

Note 1: 2 ms is the nominal time required for the 4x PLL to lock.

2: 72 ms is the nominal power-up timer delay, if implemented.

3: 1.5 μ s is the recovery time from SLEEP. There is no recovery time from oscillator switch.

REGISTER 3-1: RCON REGISTER BITS AND POSITIONS

R/W-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
IPEN	—	—	\overline{RI}	\overline{TO}	\overline{PD}	\overline{POR}	\overline{BOR}

bit 7

bit 0

Note 1: Refer to Section 4.14 (page 59) for bit definitions.

TABLE 3-2: STATUS BITS, THEIR SIGNIFICANCE AND THE INITIALIZATION CONDITION FOR RCON REGISTER

Condition	Program Counter	RCON Register	\overline{RI}	\overline{TO}	\overline{PD}	\overline{POR}	\overline{BOR}	STKFUL	STKUNF
Power-on Reset	0000h	0--1 1100	1	1	1	0	0	u	u
MCLR Reset during normal operation	0000h	0--u uuuu	u	u	u	u	u	u	u
Software Reset during normal operation	0000h	0--0 uuuu	0	u	u	u	u	u	u
Stack Full Reset during normal operation	0000h	0--u uull	u	u	u	u	u	u	1
Stack Underflow Reset during normal operation	0000h	0--u uu11	u	u	u	u	u	1	u
MCLR Reset during SLEEP	0000h	0--u 10uu	u	1	0	u	u	u	u
WDT Reset	0000h	0--u 01uu	1	0	1	u	u	u	u
WDT Wake-up	PC + 2	u--u 00uu	u	0	0	u	u	u	u
Brown-out Reset	0000h	0--1 11u0	1	1	1	1	0	u	u
Interrupt wake-up from SLEEP	PC + 2 ⁽¹⁾	u--u 00uu	u	1	0	u	u	u	u

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0'

Note 1: When the wake-up is due to an interrupt and the GIEH or GIEL bits are set, the PC is loaded with the interrupt vector (0x0000008h or 0x0000018h).

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TABLE 3-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS

Register	Applicable Devices		Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
TOSU	PIC18F6X20	PIC18F8X20	---0 0000	---0 0000	---0 uuuu ⁽³⁾
TOSH	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu ⁽³⁾
TOSL	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu ⁽³⁾
STKPTR	PIC18F6X20	PIC18F8X20	00-0 0000	uu-0 0000	uu-u uuuu ⁽³⁾
PCLATU	PIC18F6X20	PIC18F8X20	---0 0000	---0 0000	---u uuuu
PCLATH	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
PCL	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	PC + 2 ⁽²⁾
TBLPTRU	PIC18F6X20	PIC18F8X20	--00 0000	--00 0000	--uu uuuu
TBLPTRH	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
TBLPTRL	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
TABLAT	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
PRODH	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
PRODL	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
INTCON	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu ⁽¹⁾
INTCON2	PIC18F6X20	PIC18F8X20	1111 1111	1111 1111	uuuu uuuu ⁽¹⁾
INTCON3	PIC18F6X20	PIC18F8X20	1100 0000	1100 0000	uuuu uuuu ⁽¹⁾
INDF0	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A
POSTINC0	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A
POSTDEC0	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A
PREINC0	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A
PLUSW0	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A
FSR0H	PIC18F6X20	PIC18F8X20	---- xxxx	---- uuuu	---- uuuu
FSR0L	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
WREG	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF1	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A
POSTINC1	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A
POSTDEC1	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A
PREINC1	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A
PLUSW1	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.

Shaded cells indicate conditions do not apply for the designated device.

Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

4: See Table 3-2 for RESET value for specific condition.

5: Bit 6 of PORTA, LATA, and TRISA are enabled in ECIO and RCIO oscillator modes only. In all other oscillator modes, they are disabled and read '0'.

6: Bit 6 of PORTA, LATA and TRISA are not available on all devices. When unimplemented, they are read '0'.

TABLE 3-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
FSR1H	PIC18F6X20	PIC18F8X20	---- xxxx	---- uuuu	---- uuuu
FSR1L	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
BSR	PIC18F6X20	PIC18F8X20	---- 0000	---- 0000	---- uuuu
INDF2	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A
POSTINC2	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A
POSTDEC2	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A
PREINC2	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A
PLUSW2	PIC18F6X20	PIC18F8X20	N/A	N/A	N/A
FSR2H	PIC18F6X20	PIC18F8X20	---- xxxx	---- uuuu	---- uuuu
FSR2L	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
STATUS	PIC18F6X20	PIC18F8X20	---x xxxx	--u uuuu	--u uuuu
TMR0H	PIC18F6X20	PIC18F8X20	0000 0000	uuuu uuuu	uuuu uuuu
TMR0L	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
T0CON	PIC18F6X20	PIC18F8X20	1111 1111	1111 1111	uuuu uuuu
OSCCON	PIC18F6X20	PIC18F8X20	---- --0	---- --0	---- --u
LVDCON	PIC18F6X20	PIC18F8X20	--00 0101	--00 0101	--uu uuuu
WDTCON	PIC18F6X20	PIC18F8X20	---- --0	---- --0	---- --u
RCON ⁽⁴⁾	PIC18F6X20	PIC18F8X20	0--q 11qq	0--q qquu	u--u qquu
TMR1H	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR1L	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
T1CON	PIC18F6X20	PIC18F8X20	0-00 0000	u-uu uuuu	u-uu uuuu
TMR2	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
PR2	PIC18F6X20	PIC18F8X20	1111 1111	1111 1111	1111 1111
T2CON	PIC18F6X20	PIC18F8X20	-000 0000	-000 0000	-uuu uuuu
SSPBUF	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
SSPADD	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
SSPSTAT	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
SSPCON1	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
SSPCON2	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.

Shaded cells indicate conditions do not apply for the designated device.

Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

- 2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).
- 3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.
- 4: See Table 3-2 for RESET value for specific condition.
- 5: Bit 6 of PORTA, LATA, and TRISA are enabled in ECIO and RCIO oscillator modes only. In all other oscillator modes, they are disabled and read '0'.
- 6: Bit 6 of PORTA, LATA and TRISA are not available on all devices. When unimplemented, they are read '0'.

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TABLE 3-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
ADRESH	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADRESL	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	PIC18F6X20	PIC18F8X20	--00 0000	--00 0000	--uu uuuu
ADCON1	PIC18F6X20	PIC18F8X20	--00 0000	--00 0000	--uu uuuu
ADCON2	PIC18F6X20	PIC18F8X20	0--- -000	0--- -000	u--- -uuu
CCPR1H	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR1L	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP1CON	PIC18F6X20	PIC18F8X20	--00 0000	--00 0000	--uu uuuu
CCPR2H	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR2L	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP2CON	PIC18F6X20	PIC18F8X20	--00 0000	--00 0000	--uu uuuu
CCPR3H	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR3L	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP3CON	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
CVRCON	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
CMCON	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
TMR3H	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
TMR3L	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
T3CON	PIC18F6X20	PIC18F8X20	0000 0000	uuuu uuuu	uuuu uuuu
PSPCON	PIC18F6X20	PIC18F8X20	0000 ----	0000 ----	uuuu ----
SPBRG1	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
RCREG1	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
TXREG1	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
TXSTA1	PIC18F6X20	PIC18F8X20	0000 -010	0000 -010	uuuu -uuu
RCSTA1	PIC18F6X20	PIC18F8X20	0000 000x	0000 000x	uuuu uuuu
EEADRH	PIC18F6X20	PIC18F8X20	---- --00	---- --00	---- --uu
EEADR	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
EEDATA	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
EECON2	PIC18F6X20	PIC18F8X20	xx-0 x000	uu-0 u000	uu-0 u000
EECON1	PIC18F6X20	PIC18F8X20	-----	-----	-----

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.

Shaded cells indicate conditions do not apply for the designated device.

- Note 1:** One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).
- 2:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).
- 3:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.
- 4:** See Table 3-2 for RESET value for specific condition.
- 5:** Bit 6 of PORTA, LATA, and TRISA are enabled in ECIO and RCIO oscillator modes only. In all other oscillator modes, they are disabled and read '0'.
- 6:** Bit 6 of PORTA, LATA and TRISA are not available on all devices. When unimplemented, they are read '0'.

TABLE 3-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
IPR3	PIC18F6X20	PIC18F8X20	--11 1111	--11 1111	--uu uuuu
PIR3	PIC18F6X20	PIC18F8X20	--00 0000	--00 0000	--uu uuuu
PIE3	PIC18F6X20	PIC18F8X20	--00 0000	--00 0000	--uu uuuu
IPR2	PIC18F6X20	PIC18F8X20	-1-1 1111	-1-1 1111	-u-u uuuu
PIR2	PIC18F6X20	PIC18F8X20	-0-0 0000	-0-0 0000	-u-u uuuu ⁽¹⁾
PIE2	PIC18F6X20	PIC18F8X20	-0-0 0000	-0-0 0000	-u-u uuuu
IPR1	PIC18F6X20	PIC18F8X20	0111 1111	0111 1111	uuuu uuuu
PIR1	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu ⁽¹⁾
PIE1	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
MEMCON	PIC18F6X20	PIC18F8X20	0-00 --00	0-00 --00	u-uu -uu
TRISJ	PIC18F6X20	PIC18F8X20	1111 1111	1111 1111	uuuu uuuu
TRISH	PIC18F6X20	PIC18F8X20	1111 1111	1111 1111	uuuu uuuu
TRISG	PIC18F6X20	PIC18F8X20	---1 1111	---1 1111	---u uuuu
TRISF	PIC18F6X20	PIC18F8X20	1111 1111	1111 1111	uuuu uuuu
TRISE	PIC18F6X20	PIC18F8X20	0000 -111	0000 -111	uuuu -uuu
TRISD	PIC18F6X20	PIC18F8X20	1111 1111	1111 1111	uuuu uuuu
TRISC	PIC18F6X20	PIC18F8X20	1111 1111	1111 1111	uuuu uuuu
TRISB	PIC18F6X20	PIC18F8X20	1111 1111	1111 1111	uuuu uuuu
TRISA ^(5,6)	PIC18F6X20	PIC18F8X20	-111 1111 ⁽⁵⁾	-111 1111 ⁽⁵⁾	-uuu uuuu ⁽⁵⁾
LATJ	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATH	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATG	PIC18F6X20	PIC18F8X20	---x xxxx	---u uuuu	---u uuuu
LATF	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATE	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATD	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATC	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATB	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
LATA ^(5,6)	PIC18F6X20	PIC18F8X20	-xxx xxxx ⁽⁵⁾	-uuu uuuu ⁽⁵⁾	-uuu uuuu ⁽⁵⁾

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.

Shaded cells indicate conditions do not apply for the designated device.

Note 1: One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).

2: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).

3: When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.

4: See Table 3-2 for RESET value for specific condition.

5: Bit 6 of PORTA, LATA, and TRISA are enabled in ECIO and RCIO oscillator modes only. In all other oscillator modes, they are disabled and read '0'.

6: Bit 6 of PORTA, LATA and TRISA are not available on all devices. When unimplemented, they are read '0'.

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TABLE 3-3: INITIALIZATION CONDITIONS FOR ALL REGISTERS (CONTINUED)

Register	Applicable Devices		Power-on Reset, Brown-out Reset	MCLR Resets WDT Reset RESET Instruction Stack Resets	Wake-up via WDT or Interrupt
PORTJ	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTH	PIC18F6X20	PIC18F8X20	0000 xxxx	0000 uuuu	uuuu uuuu
PORTG	PIC18F6X20	PIC18F8X20	---x xxxx	uuuu uuuu	---u uuuu
PORTF	PIC18F6X20	PIC18F8X20	x000 0000	u000 0000	u000 0000
PORTE	PIC18F6X20	PIC18F8X20	---- -000	---- -000	---- -uuu
PORTD	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTC	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTB	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
PORTA ^(5,6)	PIC18F6X20	PIC18F8X20	-x0x 0000 ⁽⁵⁾	-u0u 0000 ⁽⁵⁾	-uuu uuuu ⁽⁵⁾
TMR4	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
PR4	PIC18F6X20	PIC18F8X20	1111 1111	1111 1111	uuuu uuuu
T4CON	PIC18F6X20	PIC18F8X20	-000 0000	-000 0000	-uuu uuuu
CCPR4H	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR4L	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP4CON	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
CCPR5H	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCPR5L	PIC18F6X20	PIC18F8X20	xxxx xxxx	uuuu uuuu	uuuu uuuu
CCP5CON	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
SPBRG2	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
RCREG2	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
TXREG2	PIC18F6X20	PIC18F8X20	0000 0000	0000 0000	uuuu uuuu
TXSTA2	PIC18F6X20	PIC18F8X20	0000 -010	0000 -010	uuuu -uuu
RCSTA2	PIC18F6X20	PIC18F8X20	0000 000x	0000 000x	uuuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, read as '0', q = value depends on condition.

Shaded cells indicate conditions do not apply for the designated device.

- Note 1:** One or more bits in the INTCONx or PIRx registers will be affected (to cause wake-up).
- 2:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the PC is loaded with the interrupt vector (0008h or 0018h).
- 3:** When the wake-up is due to an interrupt and the GIEL or GIEH bit is set, the TOSU, TOSH and TOSL are updated with the current value of the PC. The STKPTR is modified to point to the next location in the hardware stack.
- 4:** See Table 3-2 for RESET value for specific condition.
- 5:** Bit 6 of PORTA, LATA, and TRISA are enabled in ECIO and RCIO oscillator modes only. In all other oscillator modes, they are disabled and read '0'.
- 6:** Bit 6 of PORTA, LATA and TRISA are not available on all devices. When unimplemented, they are read '0'.

FIGURE 3-3: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO VDD VIA 1 k Ω RESISTOR)

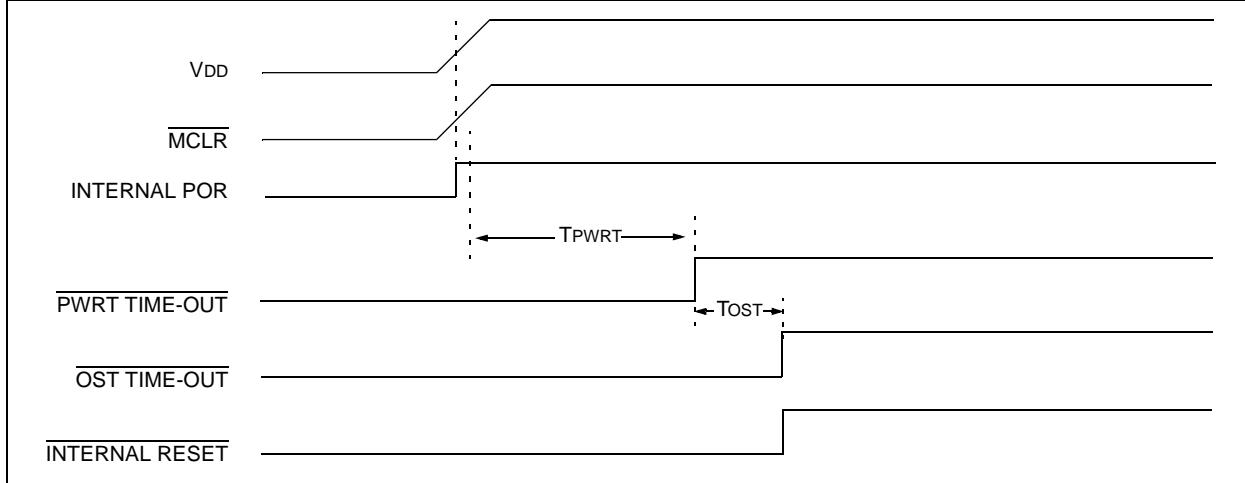


FIGURE 3-4: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 1

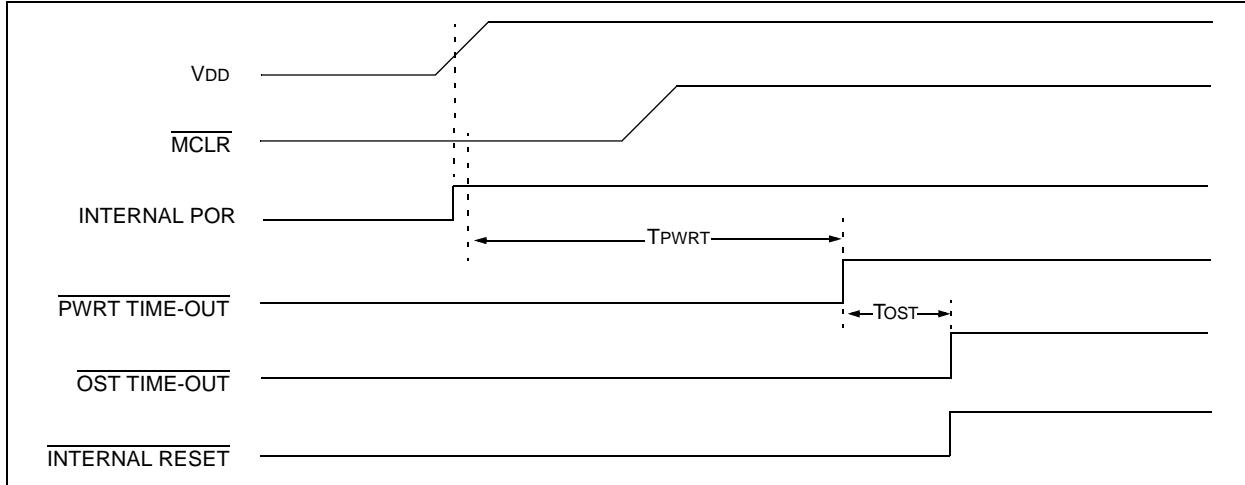
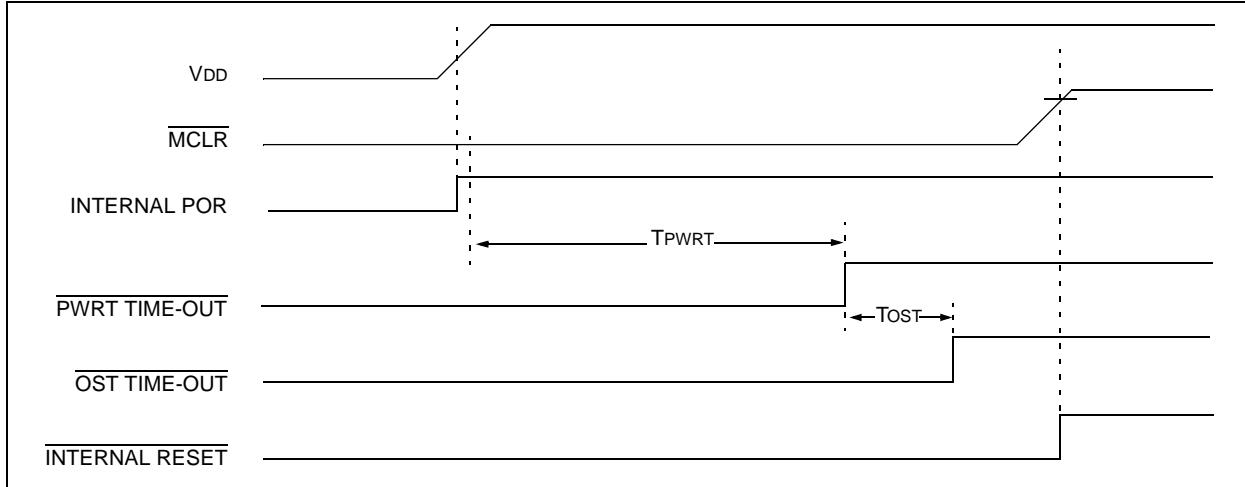


FIGURE 3-5: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO VDD): CASE 2



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FIGURE 3-6: SLOW RISE TIME (MCLR TIED TO V_{DD} VIA 1 kΩ RESISTOR)

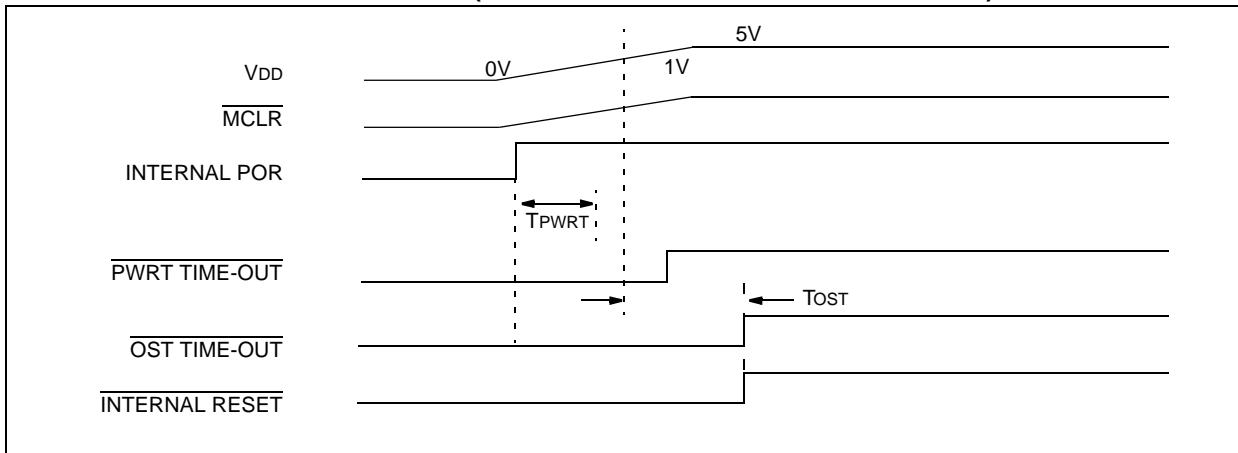
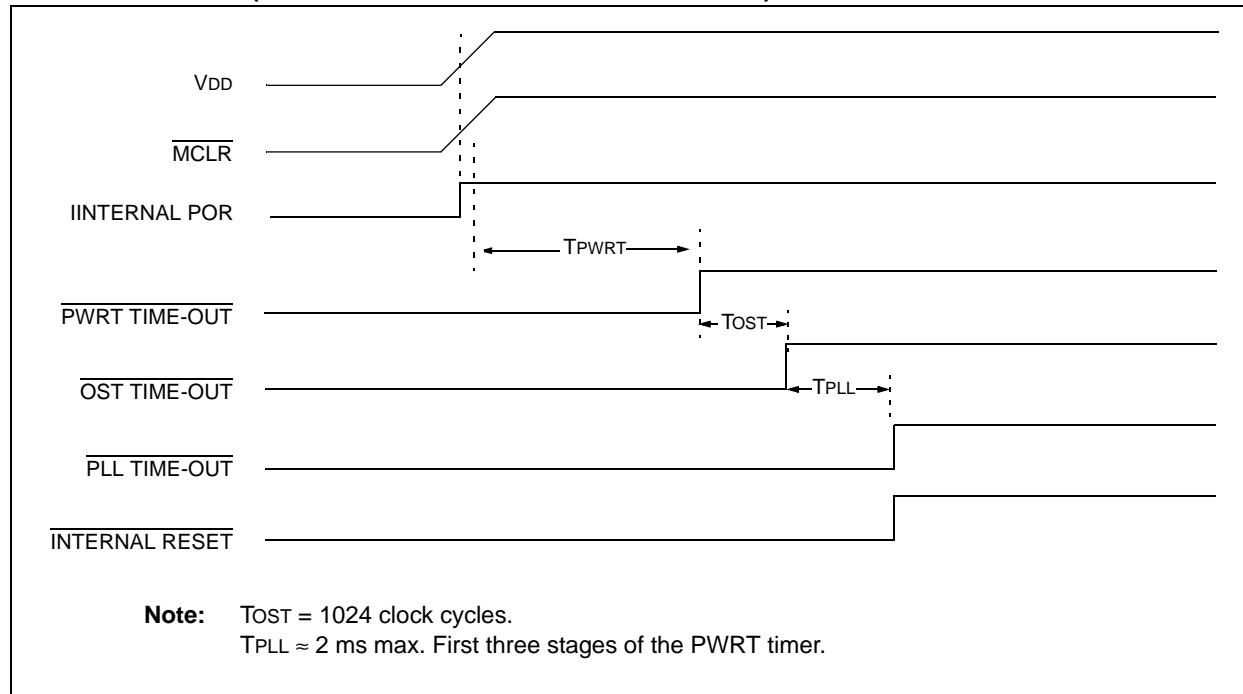


FIGURE 3-7: TIME-OUT SEQUENCE ON POR W/ PLL ENABLED
(MCLR TIED TO V_{DD} VIA 1 kΩ RESISTOR)



4.0 MEMORY ORGANIZATION

There are three memory blocks in PIC18FXX20 devices. They are:

- Program Memory
- Data RAM
- Data EEPROM

Data and program memory use separate busses, which allows for concurrent access of these blocks. Additional detailed information for FLASH program memory and Data EEPROM is provided in Section 5.0 and Section 7.0, respectively.

In addition to on-chip FLASH, the PIC18FXX20 devices are also capable of accessing external program memory through an external memory bus. Depending on the selected operating mode (discussed in Section 4.1.1), the controllers may access either internal or external program memory exclusively, or both internal and external memory in selected blocks. Additional information on the External Memory Interface is provided in Section 6.0.

4.1 Program Memory Organization

A 21-bit program counter is capable of addressing the 2-Mbyte program memory space. Accessing a location between the physically implemented memory and the 2-Mbyte address will cause a read of all '0's (a NOP instruction).

The PIC18F6620 and PIC18F8620 each have 64 Kbytes of on-chip FLASH memory, while the PIC18F6720 and PIC18F8720 have 128 Kbytes of FLASH. This means that PIC18FX620 devices can store internally up to 32,768 single word instructions, and PIC18FX720 devices can store up to 65,536 single word instructions.

The RESET vector address is at 0000h, and the interrupt vector addresses are at 0008h and 0018h.

Figure 4-1 shows the Program Memory Map for PIC18F6620/8620 devices, while Figure 4-2 shows the Program Memory Map for PIC18F6720/8720 devices.

4.1.1 PIC18F8X20 PROGRAM MEMORY MODES

PIC18F8X20 devices differ significantly from their PIC18 predecessors in their utilization of program memory. In addition to available on-chip FLASH program memory, these controllers can also address up to 2 Mbyte of external program memory through external memory interface. There are four distinct operating modes available to the controllers:

- Microprocessor (MP)
- Microprocessor with Boot Block (MPBB)
- Extended Microcontroller (EMC)
- Microcontroller (MC)

The program memory mode is determined by setting the two Least Significant bits of the CONFIG3L configuration byte, as shown in Register 4-1. (See also Section 23.1 for additional details on the device configuration bits.)

The program memory modes operate as follows:

- The **Microprocessor Mode** permits access only to external program memory; the contents of the on-chip FLASH memory is ignored. The 21-bit program counter permits access to a 2 MByte linear program memory space.
- The **Microprocessor with Boot Block Mode** accesses on-chip FLASH memory from addresses 00000h to 0001FFh. Above this, external program memory is accessed all the way up to the 2 MByte limit. Program execution automatically switches between the two memories as required.
- The **Microcontroller Mode** accesses only on-chip FLASH memory. Attempts to read above the physical limit of the on-chip FLASH (0FFFFh for the PIC18F8620, 1FFFFh for the PIC18F8720) causes a read of all '0's (a NOP instruction). The Microcontroller mode is also the only operating mode available to PIC18F6X20 devices.
- The **Extended Microcontroller Mode** allows access to both internal and external program memories as a single block. The device can access its entire on-chip FLASH memory; above this, the device accesses external program memory up to the 2 MByte program space limit. As with Boot Block mode, execution automatically switches between the two memories as required.

In all modes, the microcontroller has complete access to data RAM and EEPROM.

Figure 4-3 compares the memory maps of the different program memory modes. The differences between on-chip and external memory access limitations are more fully explained in Table 4-1.

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FIGURE 4-1: INTERNAL PROGRAM MEMORY MAP AND STACK FOR PIC18F6620/8620

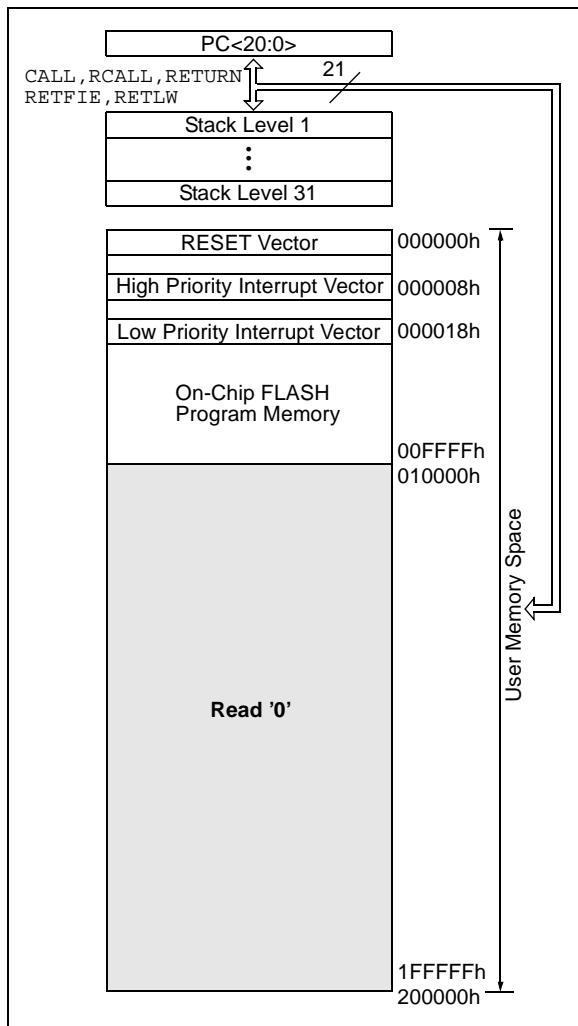


FIGURE 4-2: INTERNAL PROGRAM MEMORY MAP AND STACK FOR PIC18F6720/8720

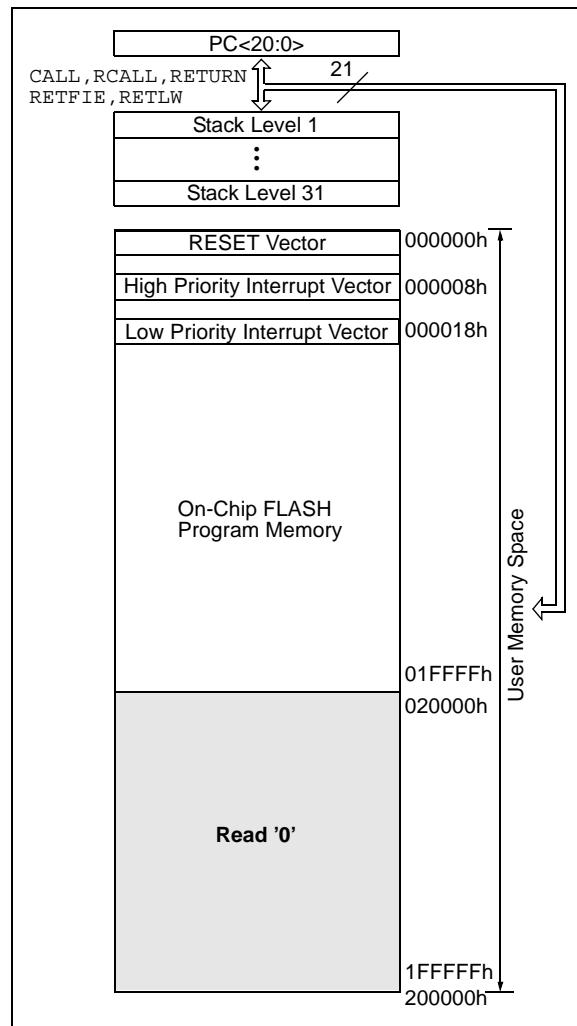


TABLE 4-1: MEMORY ACCESS FOR PIC18F8X20 PROGRAM MEMORY MODES

Operating Mode	Internal Program Memory			External Program Memory		
	Execution From	Table Read From	Table Write To	Execution From	Table Read From	Table Write To
Microprocessor	No Access	No Access	No Access	Yes	Yes	Yes
Microprocessor w/ Boot Block	Yes	Yes	Yes	Yes	Yes	Yes
Microcontroller	Yes	Yes	Yes	No Access	No Access	No Access
Extended Microcontroller	Yes	Yes	Yes	Yes	Yes	Yes

REGISTER 4-1: CONFIG3L CONFIGURATION BYTE

R/P-1	U-0	U-0	U-0	U-0	U-0	R/P-1	R/P-1
WAIT	—	—	—	—	—	PM1	PM0

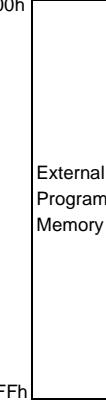
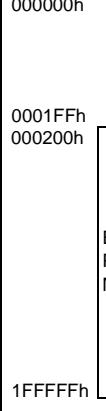
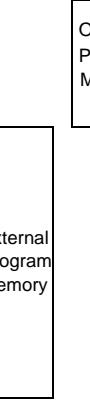
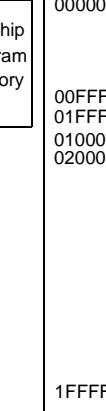
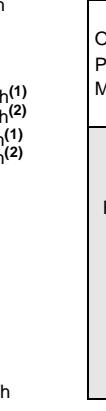
bit 7 bit 0

- bit 7 **WAIT:** External Bus Data Wait Enable bit
1 = Wait selections unavailable, device will not wait
0 = Wait programmed by WAIT1 and WAIT0 bits of MEMCOM register (MEMCOM<5:4>)
- bit 6-2 **Unimplemented:** Read as '0'
- bit 1-0 **PM1:PM0:** Processor Data Memory Mode Select bits
11 = Microcontroller mode
10 = Microprocessor mode
01 = Microcontroller with Boot Block mode
00 = Extended Microcontroller mode

Legend:

R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'
- n = Value after erase	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

FIGURE 4-3: MEMORY MAPS FOR PIC18F8X20 PROGRAM MEMORY MODES

	Microprocessor Mode	Microprocessor with Boot Block Mode	Microcontroller Mode	Extended Microcontroller Mode
Program Space Execution	000000h  1FFFFFFh 	000000h  0001FFh 	000000h  00FFFFh ⁽¹⁾ 01FFFFh ⁽²⁾ 010000h ⁽¹⁾ 020000h ⁽²⁾	000000h  00FFFFh ⁽¹⁾ 01FFFFh ⁽²⁾ 010000h ⁽¹⁾ 020000h ⁽²⁾

Note 1: PIC18F8620 and PIC18F6620.
2: PIC18F8720 and PIC18F6720.

4.2 Return Address Stack

The return address stack allows any combination of up to 31 program calls and interrupts to occur. The PC (Program Counter) is pushed onto the stack when a CALL or RCALL instruction is executed, or an interrupt is acknowledged. The PC value is pulled off the stack on a RETURN, RETLW, or a RETFIE instruction. PCLATU and PCLATH are not affected by any of the RETURN or CALL instructions.

The stack operates as a 31-word by 21-bit RAM and a 5-bit stack pointer, with the stack pointer initialized to 00000b after all RESETS. There is no RAM associated with stack pointer 00000b. This is only a RESET value. During a CALL type instruction, causing a push onto the stack, the stack pointer is first incremented and the RAM location pointed to by the stack pointer is written with the contents of the PC. During a RETURN type instruction, causing a pop from the stack, the contents of the RAM location pointed to by the STKPTR are transferred to the PC and then the stack pointer is decremented.

The stack space is not part of either program or data space. The stack pointer is readable and writable, and the address on the top of the stack is readable and writable through SFR registers. Data can also be pushed to, or popped from, the stack using the top-of-stack SFRs. Status bits indicate if the stack pointer is at, or beyond the 31 levels provided.

4.2.1 TOP-OF-STACK ACCESS

The top of the stack is readable and writable. Three register locations, TOSU, TOSH and TOSL hold the contents of the stack location pointed to by the STKPTR register. This allows users to implement a software stack if necessary. After a CALL, RCALL or interrupt, the software can read the pushed value by reading the TOSU, TOSH and TOSL registers. These values can be placed on a user defined software stack. At return time, the software can replace the TOSU, TOSH and TOSL and do a return.

The user must disable the global interrupt enable bits during this time to prevent inadvertent stack operations.

4.2.2 RETURN STACK POINTER (STKPTR)

The STKPTR register contains the stack pointer value, the STKFUL (stack full) status bit, and the STKUNF (stack underflow) status bits. Register 4-2 shows the STKPTR register. The value of the stack pointer can be 0 through 31. The stack pointer increments when values are pushed onto the stack and decrements when values are popped off the stack. At RESET, the stack pointer value will be 0. The user may read and write the stack pointer value. This feature can be used by a Real Time Operating System for return stack maintenance.

After the PC is pushed onto the stack 31 times (without popping any values off the stack), the STKFUL bit is set. The STKFUL bit can only be cleared in software or by a POR.

The action that takes place when the stack becomes full, depends on the state of the STVREN (Stack Overflow Reset Enable) configuration bit. Refer to Section 24.0 for a description of the device configuration bits. If STVREN is set (default), the 31st push will push the (PC + 2) value onto the stack, set the STKFUL bit, and reset the device. The STKFUL bit will remain set and the stack pointer will be set to 0.

If STVREN is cleared, the STKFUL bit will be set on the 31st push and the stack pointer will increment to 31. Any additional pushes will not overwrite the 31st push, and STKPTR will remain at 31.

When the stack has been popped enough times to unload the stack, the next pop will return a value of zero to the PC and sets the STKUNF bit, while the stack pointer remains at 0. The STKUNF bit will remain set until cleared in software or a POR occurs.

Note: Returning a value of zero to the PC on an underflow has the effect of vecting the program to the RESET vector, where the stack conditions can be verified and appropriate actions can be taken.

REGISTER 4-2: STKPTR REGISTER

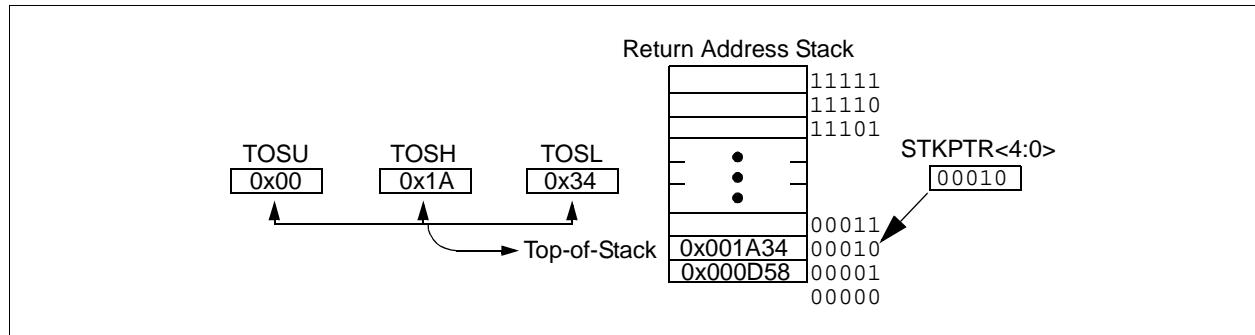
R/C-0	R/C-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
STKFUL ⁽¹⁾	STKUNF ⁽¹⁾	—	SP4	SP3	SP2	SP1	SP0
bit 7				bit 0			

- | | |
|---------|--|
| bit 7 | STKFUL: Stack Full Flag bit
1 = Stack became full or overflowed
0 = Stack has not become full or overflowed |
| bit 6 | STKUNF: Stack Underflow Flag bit
1 = Stack underflow occurred
0 = Stack underflow did not occur |
| bit 5 | Unimplemented: Read as '0' |
| bit 4-0 | SP4:SP0: Stack Pointer Location bits |

Note 1: Bit 7 and bit 6 can only be cleared in user software, or by a POR.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

FIGURE 4-4: RETURN ADDRESS STACK AND ASSOCIATED REGISTERS



4.2.3 PUSH AND POP INSTRUCTIONS

Since the Top-of-Stack (TOS) is readable and writable, the ability to push values onto the stack and pull values off the stack, without disturbing normal program execution, is a desirable option. To push the current PC value onto the stack, a `PUSH` instruction can be executed. This will increment the stack pointer and load the current PC value onto the stack. TOSU, TOSH and TOSL can then be modified to place a return address on the stack.

The ability to pull the TOS value off of the stack and replace it with the value that was previously pushed onto the stack, without disturbing normal execution, is achieved by using the `POP` instruction. The `POP` instruction discards the current TOS by decrementing the stack pointer. The previous value pushed onto the stack then becomes the TOS value.

4.2.4 STACK FULL/UNDERFLOW RESETS

These RESETS are enabled by programming the STVREN configuration bit. When the STVREN bit is disabled, a full or underflow condition will set the appropriate STKFUL or STKUNF bit, but not cause a device RESET. When the STVREN bit is enabled, a full or underflow condition will set the appropriate STKFUL or STKUNF bit and then cause a device RESET. The STKFUL or STKUNF bits are only cleared by the user software or a POR Reset.

4.3 Fast Register Stack

A “fast interrupt return” option is available for interrupts. A Fast Register Stack is provided for the STATUS, WREG and BSR registers and is only one in depth. The stack is not readable or writable and is loaded with the current value of the corresponding register when the processor vectors for an interrupt. The values in the registers are then loaded back into the working registers, if the **FAST RETURN** instruction is used to return from the interrupt.

A low or high priority interrupt source will push values into the stack registers. If both low and high priority interrupts are enabled, the stack registers cannot be used reliably for low priority interrupts. If a high priority interrupt occurs while servicing a low priority interrupt, the stack register values stored by the low priority interrupt will be overwritten.

If high priority interrupts are not disabled during low priority interrupts, users must save the key registers in software during a low priority interrupt.

If no interrupts are used, the fast register stack can be used to restore the STATUS, WREG and BSR registers at the end of a subroutine call. To use the fast register stack for a subroutine call, a **FAST CALL** instruction must be executed.

Example 4-1 shows a source code example that uses the fast register stack.

EXAMPLE 4-1: FAST REGISTER STACK CODE EXAMPLE

```

CALL SUB1, FAST      ; STATUS, WREG, BSR
                      ; SAVED IN FAST REGISTER
                      ; STACK
  .
  .
SUB1   .
  .
  .
RETURN FAST       ; RESTORE VALUES SAVED
                  ; IN FAST REGISTER STACK

```

4.4 PCL, PCLATH and PCLATU

The program counter (PC) specifies the address of the instruction to fetch for execution. The PC is 21 bits wide. The low byte is called the PCL register; this register is readable and writable. The high byte is called the PCH register. This register contains the PC<15:8> bits and is not directly readable or writable; updates to the PCH register may be performed through the PCLATH register. The upper byte is called PCU. This register contains the PC<20:16> bits and is not directly readable or writable; updates to the PCU register may be performed through the PCLATU register.

The PC addresses bytes in the program memory. To prevent the PC from becoming misaligned with word instructions, the LSB of the PCL is fixed to a value of ‘0’. The PC increments by 2 to address sequential instructions in the program memory.

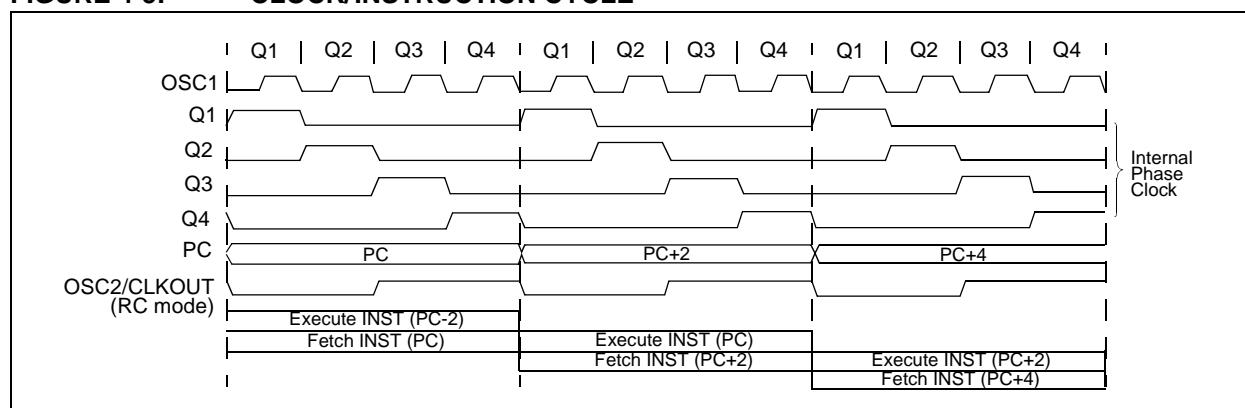
The **CALL**, **RCALL**, **GOTO** and program branch instructions write to the program counter directly. For these instructions, the contents of PCLATH and PCLATU are not transferred to the program counter.

The contents of PCLATH and PCLATU will be transferred to the program counter by an operation that writes PCL. Similarly, the upper two bytes of the program counter will be transferred to PCLATH and PCLATU by an operation that reads PCL. This is useful for computed offsets to the PC (see Section 4.8.1).

4.5 Clocking Scheme/Instruction Cycle

The clock input (from OSC1) is internally divided by four to generate four non-overlapping quadrature clocks, namely Q1, Q2, Q3 and Q4. Internally, the program counter (PC) is incremented every Q1, the instruction is fetched from the program memory and latched into the instruction register in Q4. The instruction is decoded and executed during the following Q1 through Q4. The clocks and instruction execution flow are shown in Figure 4-5.

FIGURE 4-5: CLOCK/INSTRUCTION CYCLE



4.6 Instruction Flow/Pipelining

An “Instruction Cycle” consists of four Q cycles (Q1, Q2, Q3 and Q4). The instruction fetch and execute are pipelined, such that fetch takes one instruction cycle, while decode and execute takes another instruction cycle. However, due to the pipelining, each instruction effectively executes in one cycle. If an instruction causes the program counter to change (e.g., GOTO) then two cycles are required to complete the instruction (Example 4-2).

EXAMPLE 4-2: INSTRUCTION PIPELINE FLOW

	Tcy0	Tcy1	Tcy2	Tcy3	Tcy4	Tcy5
1. MOVLW 55h	Fetch 1	Execute 1				
2. MOVWF PORTB		Fetch 2	Execute 2			
3. BRA SUB_1			Fetch 3	Execute 3		
4. BSF PORTA, BIT3 (Forced NOP)				Fetch 4	Flush (NOP)	
5. Instruction @ address SUB_1					Fetch SUB_1	Execute SUB_1

All instructions are single cycle, except for any program branches. These take two cycles since the fetch instruction is “flushed” from the pipeline, while the new instruction is being fetched and then executed.

4.7 Instructions in Program Memory

The program memory is addressed in bytes. Instructions are stored as two bytes or four bytes in program memory. The Least Significant Byte of an instruction word is always stored in a program memory location with an even address (LSB = '0'). Figure 4-6 shows an example of how instruction words are stored in the program memory. To maintain alignment with instruction boundaries, the PC increments in steps of 2 and the LSB will always read '0' (see Section 4.4).

The CALL and GOTO instructions have an absolute program memory address embedded into the instruction. Since instructions are always stored on word bound-

A fetch cycle begins with the program counter (PC) incrementing in Q1.

In the execution cycle, the fetched instruction is latched into the “Instruction Register” (IR) in cycle Q1. This instruction is then decoded and executed during the Q2, Q3, and Q4 cycles. Data memory is read during Q2 (operand read) and written during Q4 (destination write).

aries, the data contained in the instruction is a word address. The word address is written to PC<20:1>, which accesses the desired byte address in program memory. Instruction #2 in Figure 4-6 shows how the instruction “GOTO 000006h” is encoded in the program memory. Program branch instructions, which encode a relative address offset, operate in the same manner. The offset value stored in a branch instruction represents the number of single word instructions that the PC will be offset by. Section 19.0 provides further details of the instruction set.

FIGURE 4-6: INSTRUCTIONS IN PROGRAM MEMORY

Program Memory Byte Locations →			Word Address ↓		
	LSB = 1	LSB = 0			
Instruction 1:	MOVLW	055h		000000h	
Instruction 2:	GOTO	000006h		000002h	
Instruction 3:	MOVFF	123h, 456h		000004h	
				000006h	
	0Fh	55h		000008h	
	EFh	03h		00000Ah	
	F0h	00h		00000Ch	
	C1h	23h		00000Eh	
	F4h	56h		000010h	
				000012h	
				000014h	

4.7.1 TWO-WORD INSTRUCTIONS

The PIC18FXX20 devices have four two-word instructions: MOVFF, CALL, GOTO and LFSR. The second word of these instructions has the 4 MSBs set to 1's and is a special kind of NOP instruction. The lower 12 bits of the second word contain data to be used by the instruction. If the first word of the instruction is executed, the data in the second word is accessed. If the

second word of the instruction is executed by itself (first word was skipped), it will execute as a NOP. This action is necessary when the two-word instruction is preceded by a conditional instruction that changes the PC. A program example that demonstrates this concept is shown in Example 4-3. Refer to Section 19.0 for further details of the instruction set.

EXAMPLE 4-3: TWO-WORD INSTRUCTIONS

CASE 1:	
Object Code	Source Code
0110 0110 0000 0000	TSTFSZ REG1 ; is RAM location 0?
1100 0001 0010 0011	MOVFF REG1, REG2 ; No, execute 2-word instruction
1111 0100 0101 0110	
0010 0100 0000 0000	ADDWF REG3 ; 2nd operand holds address of REG2
CASE 2:	
Object Code	Source Code
0110 0110 0000 0000	TSTFSZ REG1 ; is RAM location 0?
1100 0001 0010 0011	MOVFF REG1, REG2 ; Yes
1111 0100 0101 0110	
0010 0100 0000 0000	ADDWF REG3 ; 2nd operand becomes NOP

4.8 Lookup Tables

Lookup tables are implemented two ways. These are:

- Computed GOTO
- Table Reads

4.8.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL).

A lookup table can be formed with an ADDWF PCL instruction and a group of RETLW 0xnn instructions. WREG is loaded with an offset into the table before executing a call to that table. The first instruction of the called routine is the ADDWF PCL instruction. The next instruction executed will be one of the RETLW 0xnn instructions, that returns the value 0xnn to the calling function.

The offset value (value in WREG) specifies the number of bytes that the program counter should advance.

In this method, only one data byte may be stored in each instruction location and room on the return address stack is required.

4.8.2 TABLE READS/TABLE WRITES

A better method of storing data in program memory allows 2 bytes of data to be stored in each instruction location.

Lookup table data may be stored 2 bytes per program word by using table reads and writes. The table pointer (TBLPTR) specifies the byte address and the table latch (TABLAT) contains the data that is read from, or written to program memory. Data is transferred to/from program memory, one byte at a time.

A description of the Table Read/Table Write operation is shown in Section 5.0.

4.9 Data Memory Organization

The data memory is implemented as static RAM. Each register in the data memory has a 12-bit address, allowing up to 4096 bytes of data memory. Figure 4-7 shows the data memory organization for the PIC18FXX20 devices.

The data memory map is divided into 16 banks that contain 256 bytes each. The lower 4 bits of the Bank Select Register (BSR<3:0>) select which bank will be accessed. The upper 4 bits for the BSR are not implemented.

The data memory contains Special Function Registers (SFR) and General Purpose Registers (GPR). The SFRs are used for control and status of the controller and peripheral functions, while GPRs are used for data storage and scratch pad operations in the user's application. The SFRs start at the last location of Bank 15 (0FFFh) and extend downwards. Any remaining space beyond the SFRs in the Bank may be implemented as GPRs. GPRs start at the first location of Bank 0 and grow upwards. Any read of an unimplemented location will read as '0's.

The entire data memory may be accessed directly or indirectly. Direct addressing may require the use of the BSR register. Indirect addressing requires the use of a File Select Register (FSRn) and a corresponding Indirect File Operand (INDFn). Each FSR holds a 12-bit address value that can be used to access any location in the Data Memory map without banking.

The instruction set and architecture allow operations across all banks. This may be accomplished by indirect addressing or by the use of the MOVFF instruction. The MOVFF instruction is a two-word/two-cycle instruction that moves a value from one register to another.

To ensure that commonly used registers (SFRs and select GPRs) can be accessed in a single cycle, regardless of the current BSR values, an Access Bank is implemented. A segment of Bank 0 and a segment of Bank 15 comprise the Access RAM. Section 4.10 provides a detailed description of the Access RAM.

4.9.1 GENERAL PURPOSE REGISTER FILE

The register file can be accessed either directly or indirectly. Indirect addressing operates using a File Select Register and corresponding Indirect File Operand. The operation of indirect addressing is shown in Section 4.12.

Enhanced MCU devices may have banked memory in the GPR area. GPRs are not initialized by a Power-on Reset and are unchanged on all other RESETS.

Data RAM is available for use as general purpose registers by all instructions. The top section of Bank 15 (F60h to FFFh) contains SFRs. All other banks of data memory contain GPR registers, starting with Bank 0.

4.9.2 SPECIAL FUNCTION REGISTERS

The Special Function Registers (SFRs) are registers used by the CPU and Peripheral Modules for controlling the desired operation of the device. These registers are implemented as static RAM. A list of these registers is given in Table 4-2 and Table 4-3.

The SFRs can be classified into two sets; those associated with the "core" function and those related to the peripheral functions. Those registers related to the "core" are described in this section, while those related to the operation of the peripheral features are described in the section of that peripheral feature. The SFRs are typically distributed among the peripherals whose functions they control.

The unused SFR locations are unimplemented and read as '0's. The addresses for the SFRs are listed in Table 4-2.

PIC18FXX20

FIGURE 4-7: DATA MEMORY MAP FOR PIC18FXX20 DEVICES

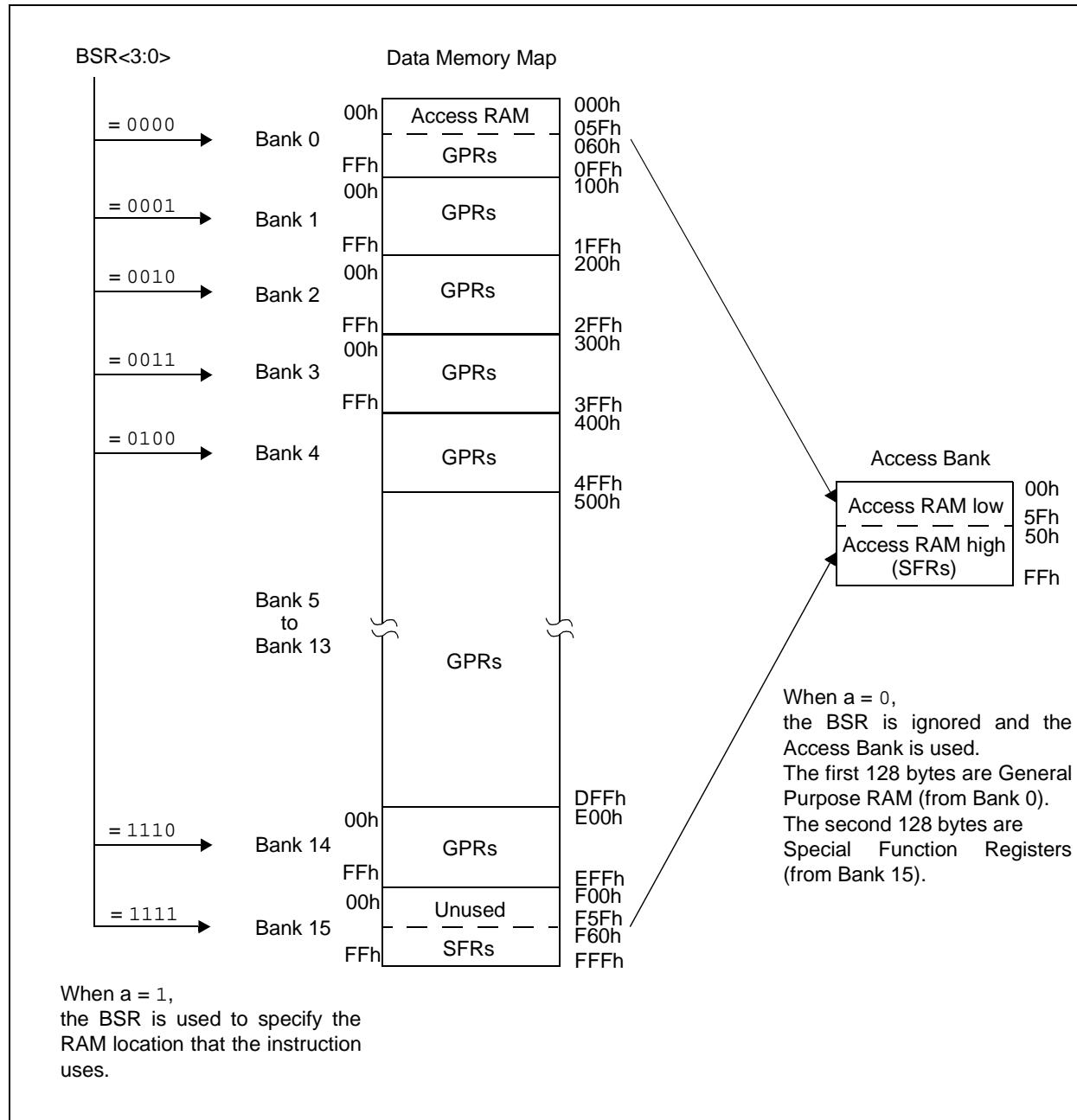


TABLE 4-2: SPECIAL FUNCTION REGISTER MAP

Address	Name	Address	Name	Address	Name	Address	Name
FFFh	TOSU	FDFh	INDF2 ⁽³⁾	FBFh	CCPR1H	F9Fh	IPR1
FFEh	TOSH	FDEh	POSTINC2 ⁽³⁾	FBEh	CCPR1L	F9Eh	PIR1
FFDh	TOSL	FDDh	POSTDEC2 ⁽³⁾	FBDh	CCP1CON	F9Dh	PIE1
FFCh	STKPTR	FDCh	PREINC2 ⁽³⁾	FBCh	CCPR2H	F9Ch	MEMCON ⁽²⁾
FFBh	PCLATU	FDBh	PLUSW2 ⁽³⁾	FBBh	CCPR2L	F9Bh	— ⁽¹⁾
FFAh	PCLATH	FDAh	FSR2H	FBAh	CCP2CON	F9Ah	TRISJ ⁽²⁾
FF9h	PCL	FD9h	FSR2L	FB9h	CCPR3H	F99h	TRISH ⁽²⁾
FF8h	TBLPTRU	FD8h	STATUS	FB8h	CCPR3L	F98h	TRISG
FF7h	TBLPTRH	FD7h	TMR0H	FB7h	CCP3CON	F97h	TRISF
FF6h	TBLPTRL	FD6h	TMR0L	FB6h	— ⁽¹⁾	F96h	TRISE
FF5h	TABLAT	FD5h	T0CON	FB5h	CVRCON	F95h	TRISD
FF4h	PRODH	FD4h	— ⁽¹⁾	FB4h	CMCON	F94h	TRISC
FF3h	PRODL	FD3h	OSCCON	FB3h	TMR3H	F93h	TRISB
FF2h	INTCON	FD2h	LVDCON	FB2h	TMR3L	F92h	TRISA
FF1h	INTCON2	FD1h	WDTCON	FB1h	T3CON	F91h	LATJ ⁽²⁾
FF0h	INTCON3	FD0h	RCON	FB0h	PSPCON	F90h	LATH ⁽²⁾
FEFh	INDF0 ⁽³⁾	FCFh	TMR1H	FAFh	SPBRG1	F8Fh	LATG
FEEh	POSTINC0 ⁽³⁾	FCEh	TMR1L	FAEh	RCREG1	F8Eh	LATF
FEDh	POSTDEC0 ⁽³⁾	FCDh	T1CON	FADh	TXREG1	F8Dh	LATE
FECh	PREINC0 ⁽³⁾	FCCh	TMR2	FACh	TXSTA1	F8Ch	LATD
FEBh	PLUSW0 ⁽³⁾	FCBh	PR2	FABh	RCSTA1	F8Bh	LATC
FEAh	FSR0H	FCAh	T2CON	FAAh	EEADRH	F8Ah	LATB
FE9h	FSR0L	FC9h	SSPBUF	FA9h	EEADR	F89h	LATA
FE8h	WREG	FC8h	SSPADD	FA8h	EEDATA	F88h	PORTJ ⁽²⁾
FE7h	INDF1 ⁽³⁾	FC7h	SSPSTAT	FA7h	EECON2	F87h	PORTH ⁽²⁾
FE6h	POSTINC1 ⁽³⁾	FC6h	SSPCON1	FA6h	EECON1	F86h	PORTG
FE5h	POSTDEC1 ⁽³⁾	FC5h	SSPCON2	FA5h	IPR3	F85h	PORTF
FE4h	PREINC1 ⁽³⁾	FC4h	ADRESH	FA4h	PIR3	F84h	PORTE
FE3h	PLUSW1 ⁽³⁾	FC3h	ADRESL	FA3h	PIE3	F83h	PORTD
FE2h	FSR1H	FC2h	ADCON0	FA2h	IPR2	F82h	PORTC
FE1h	FSR1L	FC1h	ADCON1	FA1h	PIR2	F81h	PORTB
FE0h	BSR	FC0h	ADCON2	FA0h	PIE2	F80h	PORTA

Note 1: Unimplemented registers are read as '0'.

2: This register is not available on PIC18F6X20 devices.

3: This is not a physical register.

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TABLE 4-2: SPECIAL FUNCTION REGISTER MAP (CONTINUED)

Address	Name	Address	Name	Address	Name	Address	Name
F7Fh	__(1)	F5Fh	__(1)	F3Fh	__(1)	F1Fh	__(1)
F7Eh	__(1)	F5Eh	__(1)	F3Eh	__(1)	F1Eh	__(1)
F7Dh	__(1)	F5Dh	__(1)	F3Dh	__(1)	F1Dh	__(1)
F7Ch	__(1)	F5Ch	__(1)	F3Ch	__(1)	F1Ch	__(1)
F7Bh	__(1)	F5Bh	__(1)	F3Bh	__(1)	F1Bh	__(1)
F7Ah	__(1)	F5Ah	__(1)	F3Ah	__(1)	F1Ah	__(1)
F79h	__(1)	F59h	__(1)	F39h	__(1)	F19h	__(1)
F78h	TMR4	F58h	__(1)	F38h	__(1)	F18h	__(1)
F77h	PR4	F57h	__(1)	F37h	__(1)	F17h	__(1)
F76h	T4CON	F56h	__(1)	F36h	__(1)	F16h	__(1)
F75h	CCPR4H	F55h	__(1)	F35h	__(1)	F15h	__(1)
F74h	CCPR4L	F54h	__(1)	F34h	__(1)	F14h	__(1)
F73h	CCP4CON	F53h	__(1)	F33h	__(1)	F13h	__(1)
F72h	CCPR5H	F52h	__(1)	F32h	__(1)	F12h	__(1)
F71h	CCPR5L	F51h	__(1)	F31h	__(1)	F11h	__(1)
F70h	CCP5CON	F50h	__(1)	F30h	__(1)	F10h	__(1)
F6Fh	SPBRG2	F4Fh	__(1)	F2Fh	__(1)	F0Fh	__(1)
F6Eh	RCREG2	F4Eh	__(1)	F2Eh	__(1)	F0Eh	__(1)
F6Dh	TXREG2	F4Dh	__(1)	F2Dh	__(1)	F0Dh	__(1)
F6Ch	TXSTA2	F4Ch	__(1)	F2Ch	__(1)	F0Ch	__(1)
F6Bh	RCSTA2	F4Bh	__(1)	F2Bh	__(1)	F0Bh	__(1)
F6Ah	__(1)	F4Ah	__(1)	F2Ah	__(1)	F0Ah	__(1)
F69h	__(1)	F49h	__(1)	F29h	__(1)	F09h	__(1)
F68h	__(1)	F48h	__(1)	F28h	__(1)	F08h	__(1)
F67h	__(1)	F47h	__(1)	F27h	__(1)	F07h	__(1)
F66h	__(1)	F46h	__(1)	F26h	__(1)	F06h	__(1)
F65h	__(1)	F45h	__(1)	F25h	__(1)	F05h	__(1)
F64h	__(1)	F44h	__(1)	F24h	__(1)	F04h	__(1)
F63h	__(1)	F43h	__(1)	F23h	__(1)	F03h	__(1)
F62h	__(1)	F42h	__(1)	F22h	__(1)	F02h	__(1)
F61h	__(1)	F41h	__(1)	F21h	__(1)	F01h	__(1)
F60h	__(1)	F40h	__(1)	F20h	__(1)	F00h	__(1)

- Note 1:** Unimplemented registers are read as '0'.
2: This register is not available on PIC18F6X20 devices.
3: This is not a physical register.

TABLE 4-3: REGISTER FILE SUMMARY

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
TOSU	—	—	—	Top-of-Stack Upper Byte (TOS<20:16>)						---0 0000 32, 42
TOSH	Top-of-Stack High Byte (TOS<15:8>)						0000 0000 32, 42			
TOSL	Top-of-Stack Low Byte (TOS<7:0>)						0000 0000 32, 42			
STKPTR	STKFUL	STKUNF	—	Return Stack Pointer						00-0 0000 32, 43
PCLATU	—	—	bit21	Holding Register for PC<20:16>						--10 0000 32, 44
PCLATH	Holding Register for PC<15:8>						0000 0000 32, 44			
PCL	PC Low Byte (PC<7:0>)						0000 0000 32, 44			
TBLPTRU	—	—	bit21 ⁽²⁾	Program Memory Table Pointer Upper Byte (TBLPTR<20:16>)						--00 0000 32, 64
TBLPTRH	Program Memory Table Pointer High Byte (TBLPTR<15:8>)						0000 0000 32, 64			
TBLPTRL	Program Memory Table Pointer Low Byte (TBLPTR<7:0>)						0000 0000 32, 64			
TABLAT	Program Memory Table Latch						0000 0000 32, 64			
PRODH	Product Register High Byte						xxxx xxxx 32, 81			
PRODL	Product Register Low Byte						xxxx xxxx 32, 81			
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 0000	32, 85
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	INTEDG3	TMR0IP	INT3IP	RBIP	1111 1111	32, 86
INTCON3	INT2IP	INT1IP	INT3IE	INT2IE	INT1IE	INT3IF	INT2IF	INT1IF	1100 0000	32, 87
INDF0	Uses contents of FSR0 to address data memory - value of FSR0 not changed (not a physical register)								n/a	56
POSTINC0	Uses contents of FSR0 to address data memory - value of FSR0 post-incremented (not a physical register)								n/a	56
POSTDEC0	Uses contents of FSR0 to address data memory - value of FSR0 post-decremented (not a physical register)								n/a	56
PREINC0	Uses contents of FSR0 to address data memory - value of FSR0 pre-incremented (not a physical register)								n/a	56
PLUSW0	Uses contents of FSR0 to address data memory - value of FSR0 pre-incremented (not a physical register) - value of FSR0 offset by value in WREG								n/a	56
FSR0H	—	—	—	—	Indirect Data Memory Address Pointer 0 High Byte					
FSR0L	Indirect Data Memory Address Pointer 0 Low Byte								xxxx xxxx	32, 56
WREG	Working Register								xxxx xxxx	32
INDF1	Uses contents of FSR1 to address data memory - value of FSR1 not changed (not a physical register)								n/a	56
POSTINC1	Uses contents of FSR1 to address data memory - value of FSR1 post-incremented (not a physical register)								n/a	56
POSTDEC1	Uses contents of FSR1 to address data memory - value of FSR1 post-decremented (not a physical register)								n/a	56
PREINC1	Uses contents of FSR1 to address data memory - value of FSR1 pre-incremented (not a physical register)								n/a	56
PLUSW1	Uses contents of FSR1 to address data memory - value of FSR1 pre-incremented (not a physical register) - value of FSR1 offset by value in WREG								n/a	56
FSR1H	—	—	—	—	Indirect Data Memory Address Pointer 1 High Byte					
FSR1L	Indirect Data Memory Address Pointer 1 Low Byte								xxxx xxxx	33, 56
BSR	—	—	—	—	Bank Select Register					
INDF2	Uses contents of FSR2 to address data memory - value of FSR2 not changed (not a physical register)								n/a	56
POSTINC2	Uses contents of FSR2 to address data memory - value of FSR2 post-incremented (not a physical register)								n/a	56
POSTDEC2	Uses contents of FSR2 to address data memory - value of FSR2 post-decremented (not a physical register)								n/a	56

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition

Note 1: RA6 and associated bits are configured as port pins in RCIO and ECIO oscillator mode only and read '0' in all other oscillator modes.

2: Bit 21 of the TBLPTRU allows access to the device configuration bits.

3: These registers are unused on PIC18F6X20 devices; always maintain these clear.

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TABLE 4-3: REGISTER FILE SUMMARY (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
PREINC2	Uses contents of FSR2 to address data memory - value of FSR2 pre-incremented (not a physical register)								n/a	56
PLUSW2	Uses contents of FSR2 to address data memory - value of FSR2 pre-incremented (not a physical register) - value of FSR2 offset by value in WREG								n/a	56
FSR2H	—	—	—	—	Indirect Data Memory Address Pointer 2 High Byte					---- 0000 33, 56
FSR2L	Indirect Data Memory Address Pointer 2 Low Byte								xxxx xxxx	33, 56
STATUS	—	—	—	N	OV	Z	DC	C	--x xxxx	33, 58
TMR0H	Timer0 Register High Byte								0000 0000	33, 129
TMR0L	Timer0 Register Low Byte								xxxx xxxx	33, 129
T0CON	TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0	1111 1111	33, 127
OSCCON	—	—	—	—	—	—	—	SCS	---- ---0	25, 33
LVDCON	—	—	IRVST	LVDEN	LVDL3	LVDL2	LVDL1	LVDL0	--00 0101	33, 229
WDTCON	—	—	—	—	—	—	—	SWDTE	---- ----0	33, 243
RCON	IPEN	—	—	RI	TO	PD	POR	BOR	0--1 11qq	33, 59, 97
TMR1H	Timer1 Register High Byte								xxxx xxxx	33, 131
TMR1L	Timer1 Register Low Byte								xxxx xxxx	33, 131
T1CON	RD16	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0-00 0000	33, 131
TMR2	Timer2 Register								0000 0000	33, 135
PR2	Timer2 Period Register								1111 1111	33, 136
T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	33, 135
SSPBUF	SSP Receive Buffer/Transmit Register								xxxx xxxx	33, 151
SSPADD	SSP Address Register in I ² C Slave mode. SSP Baud Rate Reload Register in I ² C Master mode.								0000 0000	33, 160
SSPSTAT	SMP	CKE	D/A	P	S	R/W	UA	BF	0000 0000	33, 152
SSPCON1	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	33, 153
SSPCON2	GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	0000 0000	33, 163
ADRESH	A/D Result Register High Byte								xxxx xxxx	34, 215
ADRESL	A/D Result Register Low Byte								xxxx xxxx	34, 215
ADCON0	—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON	--00 0000	34, 207
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	--00 0000	34, 208
ADCON2	ADFM	—	—	—	—	ADCS2	ADCS1	ADCS0	0--- -000	34, 209
CCPR1H	Capture/Compare/PWM Register1 High Byte								xxxx xxxx	147, 149
CCPR1L	Capture/Compare/PWM Register1 Low Byte								xxxx xxxx	147, 149
CCP1CON	—	—	DC1B1	DC1B0	CCP1M3	CCP1M2	CCP1M1	CCP1M0	--00 0000	34, 143
CCPR2H	Capture/Compare/PWM Register2 High Byte								xxxx xxxx	34, 147
CCPR2L	Capture/Compare/PWM Register2 Low Byte								xxxx xxxx	34, 147
CCP2CON	—	—	DC2B1	DC2B0	CCP2M3	CCP2M2	CCP2M1	CCP2M0	--00 0000	34, 143
CCPR3H	Capture/Compare/PWM Register3 High Byte								xxxx xxxx	34, 147
CCPR3L	Capture/Compare/PWM Register3 Low Byte								xxxx xxxx	34, 147
CCP3CON	—	—	DCCP3X	DCCP3Y	CCP3M3	CCP3M2	CCP3M1	CCP3M0	--00 0000	34, 143
CVRCN	CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0	0000 0000	34, 223

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition

Note 1: RA6 and associated bits are configured as port pins in RCIO and ECIO oscillator mode only and read '0' in all other oscillator modes.

2: Bit 21 of the TBLPTRU allows access to the device configuration bits.

3: These registers are unused on PIC18F6X20 devices; always maintain these clear.

TABLE 4-3: REGISTER FILE SUMMARY (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:
CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	34, 217
TMR3H	Timer3 Register High Byte								xxxx xxxx	34, 137
TMR3L	Timer3 Register Low Byte								xxxx xxxx	34, 137
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON	0000 0000	34, 137
PSPCON	IBF	OBF	IBOV	PSPMODE	—	—	—	—	0000 ----	34, 125
SPBRG1	USART1 Baud Rate Generator								0000 0000	34, 198
RCREG1	USART1 Receive Register								0000 0000	34, 200
TXREG1	USART1 Transmit Register								0000 0000	34, 198
TXSTA1	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	34, 192
RCSTA1	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	34, 193
EEADRH	—	—	—	—	—	—	EE Adr Register High	----	--00	34, 80
EEADR	Data EEPROM Address Register								0000 0000	34, 80
EEDATA	Data EEPROM Data Register								0000 0000	34, 80
EECON2	Data EEPROM Control Register 2 (not a physical register)								---- -----	34, 80
EECON1	EEPGD	CFGs	—	FREE	WRERR	WREN	WR	RD	00-0 x000	34, 78
IPR3	—	—	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	--11 1111	35, 96
PIR3	—	—	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	--00 0000	35, 90
PIE3	—	—	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	--00 0000	35, 93
IPR2	—	CMIP	—	EEIP	BCLIP	LVDIP	TMR3IP	CCP2IP	-1-1 1111	35, 95
PIR2	—	CMIF	—	EEIF	BCLIF	LVDIF	TMR3IF	CCP2IF	-0-0 0000	35, 89
PIE2	—	CMIE	—	EEIE	BCLIE	LVDIE	TMR3IE	CCP2IE	-0-0 0000	35, 92
IPR1	PSPIP	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	35, 94
PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	35, 88
PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	35, 91
MEMCON ⁽³⁾	EBDIS	—	WAIT1	WAIT0	—	—	WM1	WM0	0-00 --00	35, 71
TRISJ ⁽³⁾	Data Direction Control Register for PORTJ								1111 1111	35, 123
TRISH ⁽³⁾	Data Direction Control Register for PORTH								1111 1111	35, 120
TRISG	—	—	—	Data Direction Control Register for PORTG					---1 1111	35, 117
TRISF	Data Direction Control Register for PORTF								1111 1111	35, 115
TRISE	Data Direction Control Register for PORTE								1111 1111	35, 112
TRISD	Data Direction Control Register for PORTD								1111 1111	35, 109
TRISC	Data Direction Control Register for PORTC								1111 1111	35, 105
TRISB	Data Direction Control Register for PORTB								1111 1111	35, 102
TRISA	—	TRISA6 ⁽¹⁾	Data Direction Control Register for PORTA						-111 1111	35, 99
LATJ ⁽³⁾	Read PORTJ Data Latch, Write PORTJ Data Latch								xxxx xxxx	35, 123
LATH ⁽³⁾	Read PORTH Data Latch, Write PORTH Data Latch								xxxx xxxx	35, 120
LATG	—	—	—	Read PORTG Data Latch, Write PORTG Data Latch					---x xxxx	35, 117
LATF	Read PORTF Data Latch, Write PORTF Data Latch								xxxx xxxx	35, 115
LATE	Read PORTE Data Latch, Write PORTE Data Latch								xxxx xxxx	35, 112
LATD	Read PORTD Data Latch, Write PORTD Data Latch								xxxx xxxx	35, 107
LATC	Read PORTC Data Latch, Write PORTC Data Latch								xxxx xxxx	35, 105
LATB	Read PORTB Data Latch, Write PORTB Data Latch								xxxx xxxx	35, 102

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition

Note 1: RA6 and associated bits are configured as port pins in RCIO and ECIO oscillator mode only and read '0' in all other oscillator modes.

2: Bit 21 of the TBLPTRU allows access to the device configuration bits.

3: These registers are unused on PIC18F6X20 devices; always maintain these clear.

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TABLE 4-3: REGISTER FILE SUMMARY (CONTINUED)

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Details on page:						
LATA	—	LATA6 ⁽¹⁾	Read PORTA Data Latch, Write PORTA Data Latch ⁽¹⁾						-xxxx xxxx	35, 99						
PORTJ ⁽³⁾	Read PORTJ pins, Write PORTJ Data Latch								xxxxx xxxx	36, 123						
PORTH ⁽³⁾	Read PORTH pins, Write PORTH Data Latch								xxxxx xxxx	36, 120						
PORTG	—	—	—	Read PORTG pins, Write PORTG Data Latch						---x xxxx						
PORTF	Read PORTF pins, Write PORTF Data Latch								xxxxx xxxx	36, 115						
PORTE	Read PORTE pins, Write PORTE Data Latch								xxxxx xxxx	36, 110						
PORTD	Read PORTD pins, Write PORTD Data Latch								xxxxx xxxx	36, 107						
PORTC	Read PORTC pins, Write PORTC Data Latch								xxxxx xxxx	36, 105						
PORTB	Read PORTB pins, Write PORTB Data Latch								xxxxx xxxx	36, 102						
PORTA	—	RA6 ⁽¹⁾	Read PORTA pins, Write PORTA Data Latch ⁽¹⁾						-x0x 0000	36, 99						
TMR4	Timer4 Register								0000 0000	36, 142						
PR4	Timer4 Period Register								1111 1111	36, 142						
T4CON	—	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0	-000 0000	36, 141						
CCPR4H	Capture/Compare/PWM Register 4 High Byte								xxxxx xxxx	36, 147						
CCPR4L	Capture/Compare/PWM Register 4 Low Byte								xxxxx xxxx	36, 147						
CCP4CON	—	—	DCCP4X	DCCP4Y	CCP4M3	CCP4M2	CCP4M1	CCP4M0	0000 0000	36, 143						
CCPR5H	Capture/Compare/PWM Register 5 High Byte								xxxxx xxxx	36, 147						
CCPR5L	Capture/Compare/PWM Register 5 Low Byte								xxxxx xxxx	36, 147						
CCP5CON	—	—	DCCP5X	DCCP5Y	CCP5M3	CCP5M2	CCP5M1	CCP5M0	0000 0000	36, 143						
SPBRG2	USART2 Baud Rate Generator								0000 0000	36, 198						
RCREG2	USART2 Receive Register								0000 0000	36, 198						
TXREG2	USART2 Transmit Register								0000 0000	36, 198						
TXSTA2	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	36, 192						
RCSTA2	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	36, 193						

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition

Note 1: RA6 and associated bits are configured as port pins in RCIO and ECIO oscillator mode only and read '0' in all other oscillator modes.

2: Bit 21 of the TBLPTRU allows access to the device configuration bits.

3: These registers are unused on PIC18F6X20 devices; always maintain these clear.

4.10 Access Bank

The Access Bank is an architectural enhancement, which is very useful for C compiler code optimization. The techniques used by the C compiler may also be useful for programs written in assembly.

This data memory region can be used for:

- Intermediate computational values
- Local variables of subroutines
- Faster context saving/swapping of variables
- Common variables
- Faster evaluation/control of SFRs (no banking)

The Access Bank is comprised of the upper 160 bytes in Bank 15 (SFRs) and the lower 96 bytes in Bank 0. These two sections will be referred to as Access RAM High and Access RAM Low, respectively. Figure 4-7 indicates the Access RAM areas.

A bit in the instruction word specifies if the operation is to occur in the bank specified by the BSR register or in the Access Bank. This bit is denoted by the 'a' bit (for access bit).

When forced in the Access Bank ($a = '0'$), the last address in Access RAM Low is followed by the first address in Access RAM High. Access RAM High maps the Special Function registers, so that these registers can be accessed without any software overhead. This is useful for testing status flags and modifying control bits.

4.11 Bank Select Register (BSR)

The need for a large general purpose memory space dictates a RAM banking scheme. The data memory is partitioned into sixteen banks. When using direct addressing, the BSR should be configured for the desired bank.

$\text{BSR}_{<3:0>}$ holds the upper 4 bits of the 12-bit RAM address. The $\text{BSR}_{<7:4>}$ bits will always read '0's, and writes will have no effect.

A `MOVLB` instruction has been provided in the instruction set to assist in selecting banks.

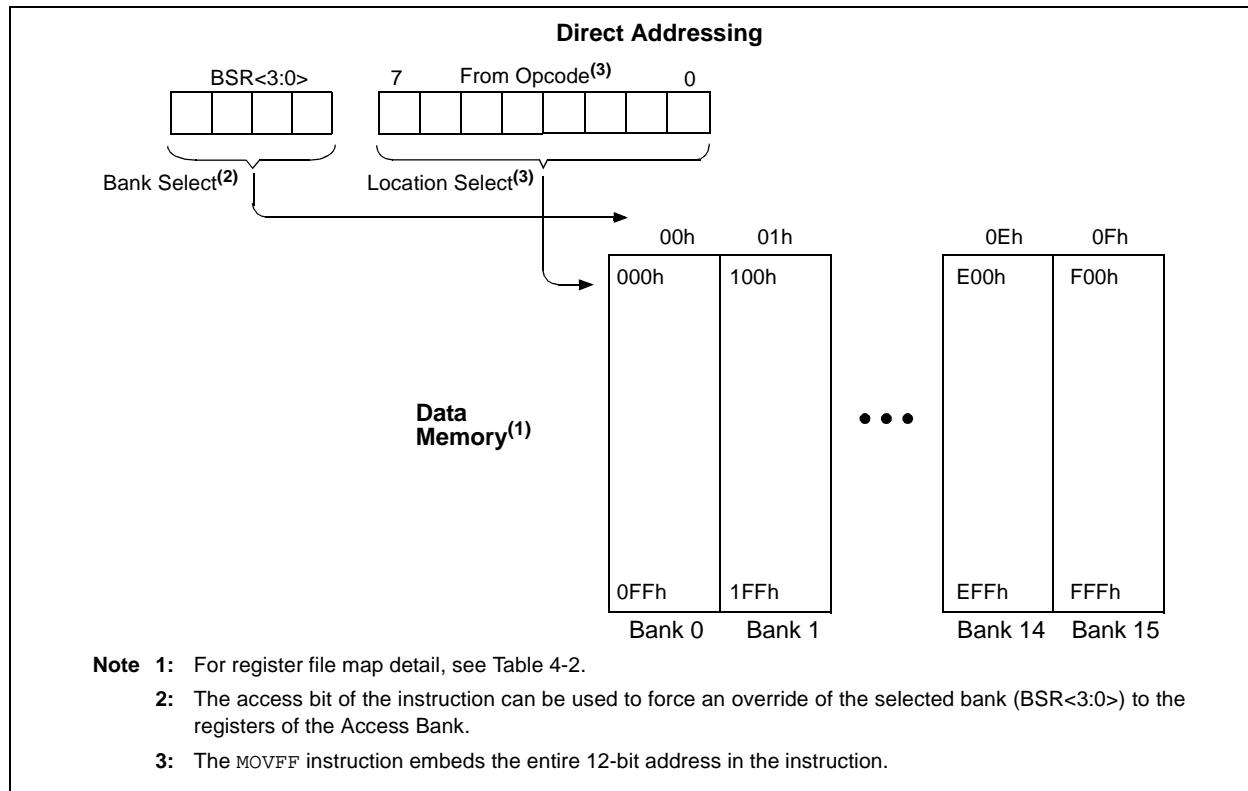
If the currently selected bank is not implemented, any read will return all '0's and all writes are ignored. The STATUS register bits will be set/cleared as appropriate for the instruction performed.

Each Bank extends up to FFh (256 bytes). All data memory is implemented as static RAM.

A `MOVFF` instruction ignores the BSR, since the 12-bit addresses are embedded into the instruction word.

Section 4.12 provides a description of indirect addressing, which allows linear addressing of the entire RAM space.

FIGURE 4-8: DIRECT ADDRESSING



4.12 Indirect Addressing, INDF and FSR Registers

Indirect addressing is a mode of addressing data memory, where the data memory address in the instruction is not fixed. An FSR register is used as a pointer to the data memory location that is to be read or written. Since this pointer is in RAM, the contents can be modified by the program. This can be useful for data tables in the data memory and for software stacks. Figure 4-9 shows the operation of indirect addressing. This shows the moving of the value to the data memory address, specified by the value of the FSR register.

Indirect addressing is possible by using one of the INDF registers. Any instruction using the INDF register actually accesses the register pointed to by the File Select Register, FSR. Reading the INDF register itself, indirectly (FSR = '0'), will read 00h. Writing to the INDF register indirectly, results in a no operation. The FSR register contains a 12-bit address, which is shown in Figure 4-10.

The INDFn register is not a physical register. Addressing INDFn actually addresses the register whose address is contained in the FSRn register (FSRn is a pointer). This is indirect addressing.

Example 4-4 shows a simple use of indirect addressing to clear the RAM in Bank1 (locations 100h-1FFh) in a minimum number of instructions.

EXAMPLE 4-4: HOW TO CLEAR RAM (BANK1) USING INDIRECT ADDRESSING

```
LFSR  FSR0 ,0x100 ;  
NEXT  CLRFL POSTINC0 ; Clear INDF  
; register and  
; inc pointer  
      BTFSS FSR0H, 1 ; All done with  
; Bank1?  
      GOTO  NEXT    ; NO, clear next  
CONTINUE          ; YES, continue
```

There are three indirect addressing registers. To address the entire data memory space (4096 bytes), these registers are 12-bits wide. To store the 12 bits of addressing information, two 8-bit registers are required. These indirect addressing registers are:

1. FSR0: composed of FSR0H:FSR0L
2. FSR1: composed of FSR1H:FSR1L
3. FSR2: composed of FSR2H:FSR2L

In addition, there are registers INDF0, INDF1 and INDF2, which are not physically implemented. Reading or writing to these registers activates indirect addressing, with the value in the corresponding FSR register being the address of the data. If an instruction writes a value to INDF0, the value will be written to the address pointed to by FSR0H:FSR0L. A read from INDF1 reads

the data from the address pointed to by FSR1H:FSR1L. INDFn can be used in code anywhere an operand can be used.

If INDF0, INDF1, or INDF2 are read indirectly via an FSR, all '0's are read (zero bit is set). Similarly, if INDF0, INDF1, or INDF2 are written to indirectly, the operation will be equivalent to a NOP instruction and the STATUS bits are not affected.

4.12.1 INDIRECT ADDRESSING OPERATION

Each FSR register has an INDF register associated with it, plus four additional register addresses. Performing an operation on one of these five registers determines how the FSR will be modified during indirect addressing.

When data access is done to one of the five INDFn locations, the address selected will configure the FSRn register to:

- Do nothing to FSRn after an indirect access (no change) - INDFn.
- Auto-decrement FSRn after an indirect access (post-decrement) - POSTDECn.
- Auto-increment FSRn after an indirect access (post-increment) - POSTINCn.
- Auto-increment FSRn before an indirect access (pre-increment) - PREINCn.
- Use the value in the WREG register as an offset to FSRn. Do not modify the value of the WREG or the FSRn register after an indirect access (no change) - PLUSWn.

When using the auto-increment or auto-decrement features, the effect on the FSR is not reflected in the STATUS register. For example, if the indirect address causes the FSR to equal '0', the Z bit will not be set.

Incrementing or decrementing an FSR affects all 12 bits. That is, when FSRnL overflows from an increment, FSRnH will be incremented automatically.

Adding these features allows the FSRn to be used as a stack pointer, in addition to its uses for table operations in data memory.

Each FSR has an address associated with it that performs an indexed indirect access. When a data access to this INDFn location (PLUSWn) occurs, the FSRn is configured to add the signed value in the WREG register and the value in FSR to form the address before an indirect access. The FSR value is not changed.

If an FSR register contains a value that points to one of the INDFn, an indirect read will read 00h (zero bit is set), while an indirect write will be equivalent to a NOP (STATUS bits are not affected).

If an indirect addressing operation is done where the target address is an FSRnH or FSRnL register, the write operation will dominate over the pre- or post-increment/decrement functions.

FIGURE 4-9: INDIRECT ADDRESSING OPERATION

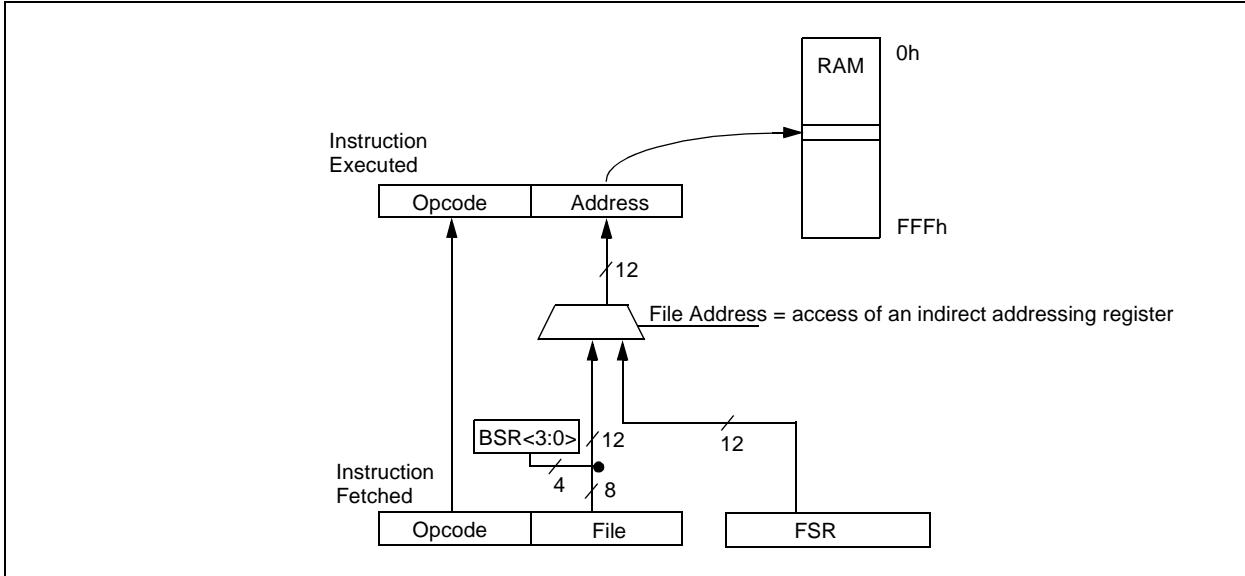
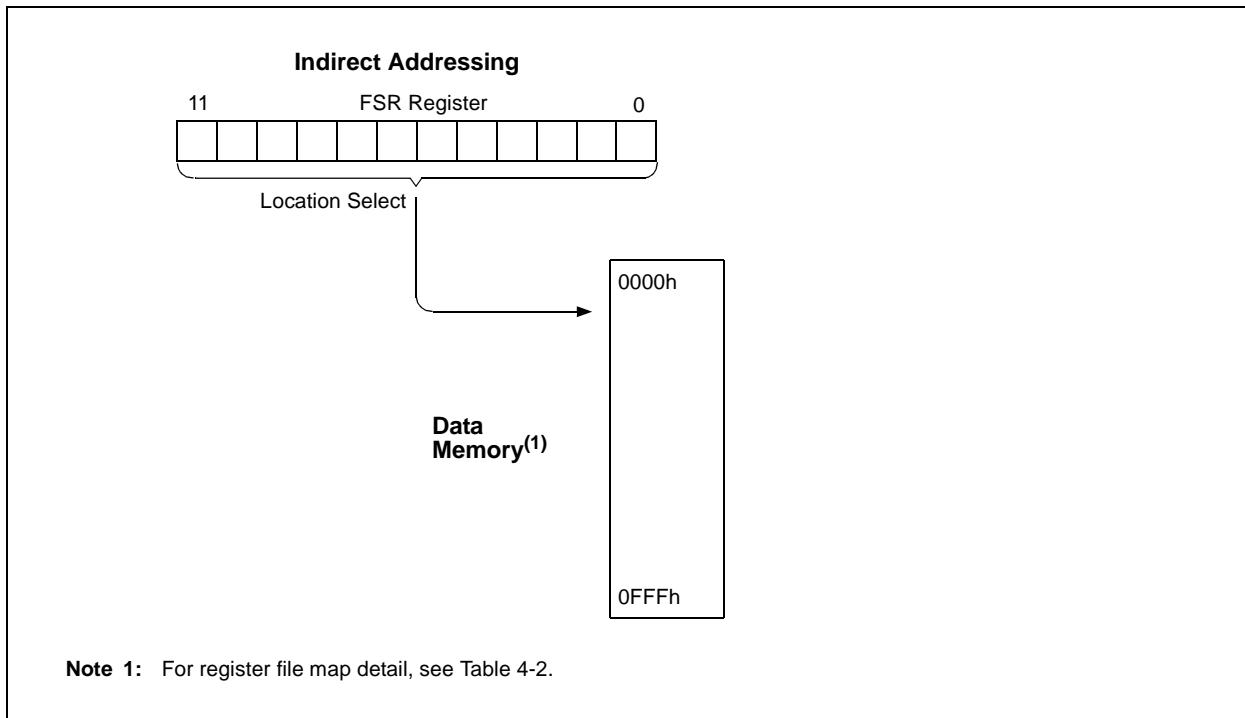


FIGURE 4-10: INDIRECT ADDRESSING



4.14 RCON Register

The Reset Control (RCON) register contains flag bits that allow differentiation between the sources of a device RESET. These flags include the TO, PD, POR, BOR and RI bits. This register is readable and writable.

Note 1: If the BOREN configuration bit is set (Brown-out Reset enabled), the BOR bit is '1' on a Power-on Reset. After a Brown-out Reset has occurred, the BOR bit will be cleared, and must be set by firmware to indicate the occurrence of the next Brown-out Reset.

2: It is recommended that the POR bit be set after a Power-on Reset has been detected, so that subsequent Power-on Resets may be detected.

REGISTER 4-4: RCON REGISTER

R/W-0	U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-0	R/W-0
IPEN	—	—	RI	TO	PD	POR	BOR
bit 7							bit 0

- | | |
|---------|--|
| bit 7 | IPEN: Interrupt Priority Enable bit
1 = Enable priority levels on interrupts
0 = Disable priority levels on interrupts (PIC16CXXX compatibility mode) |
| bit 6-5 | Unimplemented: Read as '0' |
| bit 4 | RI: RESET Instruction Flag bit
1 = The RESET instruction was not executed
0 = The RESET instruction was executed causing a device RESET
(must be set in software after a Brown-out Reset occurs) |
| bit 3 | TO: Watchdog Time-out Flag bit
1 = After power-up, CLRWDT instruction, or SLEEP instruction
0 = A WDT time-out occurred |
| bit 2 | PD: Power-down Detection Flag bit
1 = After power-up or by the CLRWDT instruction
0 = By execution of the SLEEP instruction |
| bit 1 | POR: Power-on Reset Status bit
1 = A Power-on Reset has not occurred
0 = A Power-on Reset occurred
(must be set in software after a Power-on Reset occurs) |
| bit 0 | BOR: Brown-out Reset Status bit
1 = A Brown-out Reset has not occurred
0 = A Brown-out Reset occurred
(must be set in software after a Brown-out Reset occurs) |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR reset '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

PIC18FXX20

NOTES:

5.0 FLASH PROGRAM MEMORY

The FLASH Program Memory is readable, writable, and erasable, during normal operation over the entire VDD range.

A read from program memory is executed on one byte at a time. A write to program memory is executed on blocks of 8 bytes at a time. Program memory is erased in blocks of 64 bytes at a time. A bulk erase operation may not be issued from user code.

Writing or erasing program memory will cease instruction fetches until the operation is complete. The program memory cannot be accessed during the write or erase, therefore, code cannot execute. An internal programming timer terminates program memory writes and erases.

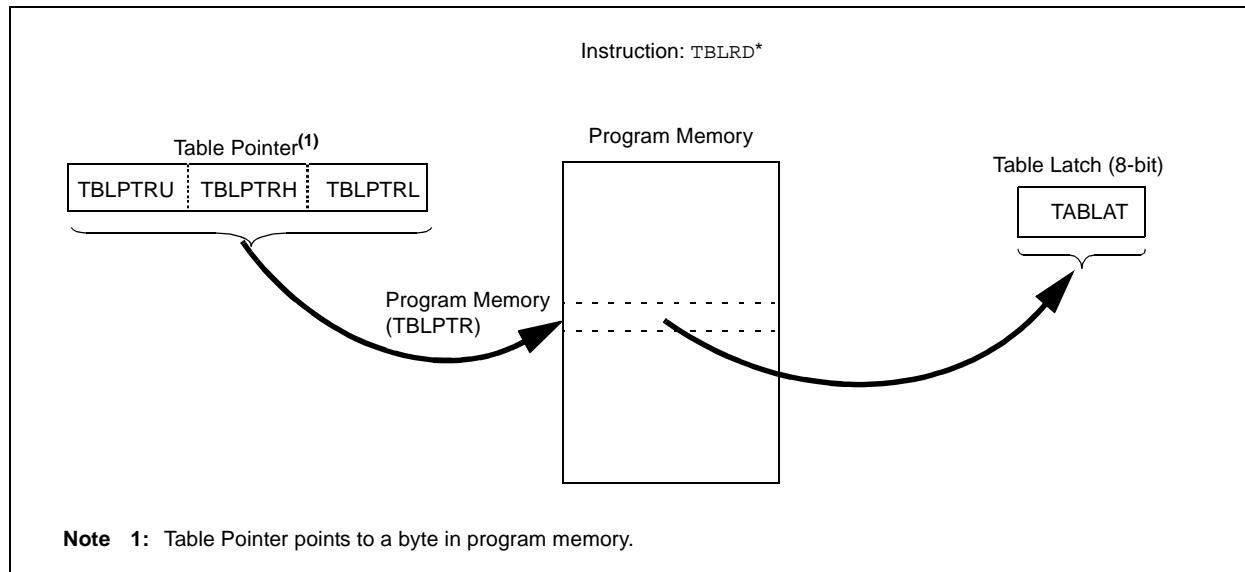
A value written to program memory does not need to be a valid instruction. Executing a program memory location that forms an invalid instruction results in a NOP.

5.1 Table Reads and Table Writes

In order to read and write program memory, there are two operations that allow the processor to move bytes between the program memory space and the data RAM:

- Table Read (TBLRD)
- Table Write (TBLWT)

FIGURE 5-1: TABLE READ OPERATION



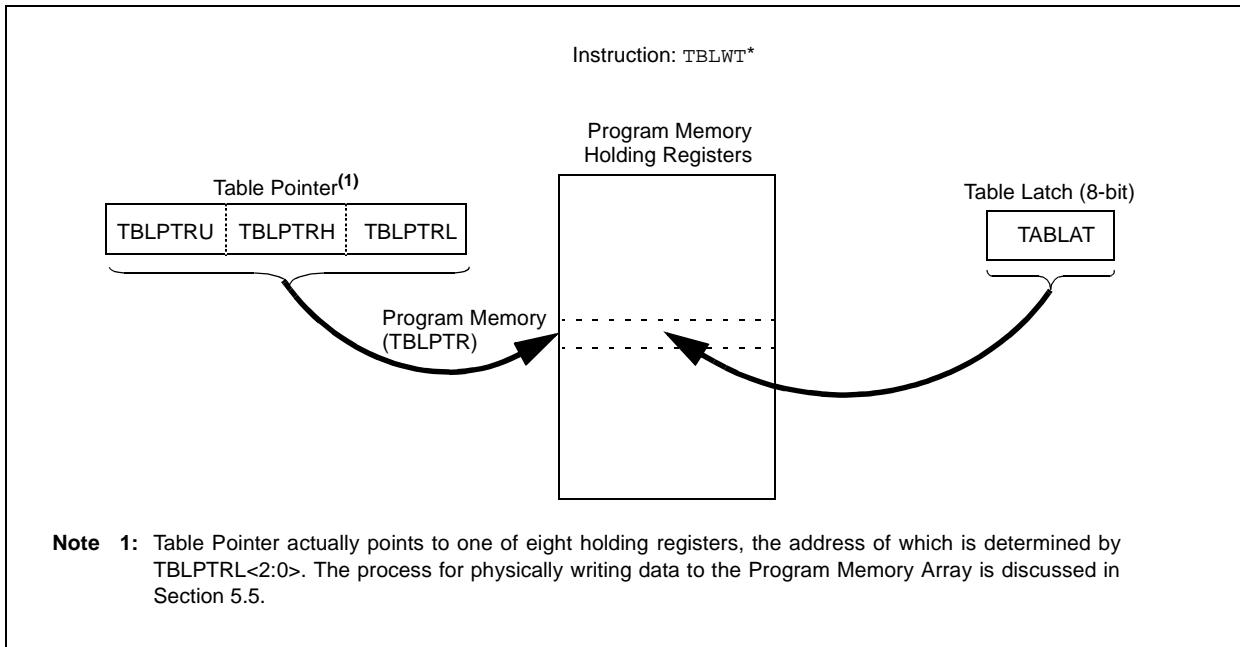
The program memory space is 16-bits wide, while the data RAM space is 8-bits wide. Table Reads and Table Writes move data between these two memory spaces through an 8-bit register (TABLAT).

Table Read operations retrieve data from program memory and places it into the data RAM space. Figure 5-1 shows the operation of a Table Read with program memory and data RAM.

Table Write operations store data from the data memory space into holding registers in program memory. The procedure to write the contents of the holding registers into program memory is detailed in Section 5.5, "Writing to FLASH Program Memory". Figure 5-2 shows the operation of a Table Write with program memory and data RAM.

Table operations work with byte entities. A table block containing data, rather than program instructions, is not required to be word aligned. Therefore, a table block can start and end at any byte address. If a Table Write is being used to write executable code into program memory, program instructions will need to be word aligned.

FIGURE 5-2: TABLE WRITE OPERATION



5.2 Control Registers

Several control registers are used in conjunction with the TBLRD and TBLWT instructions. These include the:

- EECON1 register
- EECON2 register
- TABLAT register
- TBLPTR registers

5.2.1 EECON1 AND EECON2 REGISTERS

EECON1 is the control register for memory accesses.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the memory write and erase sequences.

Control bit EEPGD determines if the access will be a program or data EEPROM memory access. When clear, any subsequent operations will operate on the data EEPROM memory. When set, any subsequent operations will operate on the program memory.

Control bit CFGS determines if the access will be to the configuration/calibration registers, or to program memory/data EEPROM memory. When set, subsequent operations will operate on configuration registers, regardless of EEPGD (see "Special Features of the CPU", Section 23.0). When clear, memory selection access is determined by EEPGD.

The FREE bit, when set, will allow a program memory erase operation. When the FREE bit is set, the erase operation is initiated on the next WR command. When FREE is clear, only writes are enabled.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a MCLR Reset or a WDT Time-out Reset, during normal operation. In these situations, the user can check the WRERR bit and rewrite the location. It is necessary to reload the data and address registers (EEDATA and EEADR), due to RESET values of zero.

The WR control bit, WR, initiates write operations. The bit cannot be cleared, only set, in software; it is cleared in hardware at the completion of the write operation. The inability to clear the WR bit in software prevents the accidental or premature termination of a write operation.

Note: Interrupt flag bit EEIF, in the PIR2 register, is set when the write is complete. It must be cleared in software.

REGISTER 5-1: EECON1 REGISTER (ADDRESS FA6h)

R/W-x	R/W-x	U-0	R/W-0	R/W-x	R/W-0	R/S-0	R/S-0
EEPGD	CFGs	—	FREE	WRERR	WREN	WR	RD
bit 7							bit 0

- bit 7 **EEPGD:** FLASH Program or Data EEPROM Memory Select bit
 1 = Access FLASH Program memory
 0 = Access Data EEPROM memory
- bit 6 **CFGs:** FLASH Program/Data EEPROM or Configuration Select bit
 1 = Access Configuration registers
 0 = Access FLASH Program or Data EEPROM memory
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **FREE:** FLASH Row Erase Enable bit
 1 = Erase the program memory row addressed by TBLPTR on the next WR command
 (cleared by completion of erase operation)
 0 = Perform write only
- bit 3 **WRERR:** FLASH Program/Data EEPROM Error Flag bit
 1 = A write operation is prematurely terminated
 (any RESET during self-timed programming in normal operation)
 0 = The write operation completed
Note: When a WRERR occurs, the EEPGD and CFGS bits are not cleared. This allows tracing of the error condition.
- bit 2 **WREN:** FLASH Program/Data EEPROM Write Enable bit
 1 = Allows write cycles
 0 = Inhibits write to the EEPROM
- bit 1 **WR:** Write Control bit
 1 = Initiates a data EEPROM erase/write cycle or a program memory erase cycle or write cycle.
 (The operation is self-timed and the bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.)
 0 = Write cycle to the EEPROM is complete
- bit 0 **RD:** Read Control bit
 1 = Initiates an EEPROM read
 (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software. RD bit cannot be set when EEPGD = 1.)
 0 = Does not initiate an EEPROM read

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

5.2.2 TABLAT - TABLE LATCH REGISTER

The Table Latch (TABLAT) is an 8-bit register mapped into the SFR space. The Table Latch is used to hold 8-bit data during data transfers between program memory and data RAM.

5.2.3 TBLPTR - TABLE POINTER REGISTER

The Table Pointer (TBLPTR) addresses a byte within the program memory. The TBLPTR is comprised of three SFR registers: Table Pointer Upper Byte, Table Pointer High Byte and Table Pointer Low Byte (TBLPTRU:TBLPTRH:TBLPTRL). These three registers join to form a 22-bit wide pointer. The low order 21 bits allow the device to address up to 2 Mbytes of program memory space. The 22nd bit allows access to the Device ID, the User ID and the Configuration bits.

The table pointer, TBLPTR, is used by the TBLRD and TBLWT instructions. These instructions can update the TBLPTR in one of four ways, based on the table operation. These operations are shown in Table 5-1. These operations on the TBLPTR only affect the low order 21 bits.

5.2.4 TABLE POINTER BOUNDARIES

TBLPTR is used in reads, writes, and erases of the FLASH program memory.

When a TBLRD is executed, all 22 bits of the Table Pointer determine which byte is read from program memory into TABLAT.

When a TBLWT is executed, the three LSbs of the Table Pointer (TBLPTR<2:0>) determine which of the eight program memory holding registers is written to. When the timed write to program memory (long write) begins, the 19 MSbs of the Table Pointer, TBLPTR (TBLPTR<21:3>), will determine which program memory block of 8 bytes is written to. For more detail, see Section 5.5 ("Writing to FLASH Program Memory").

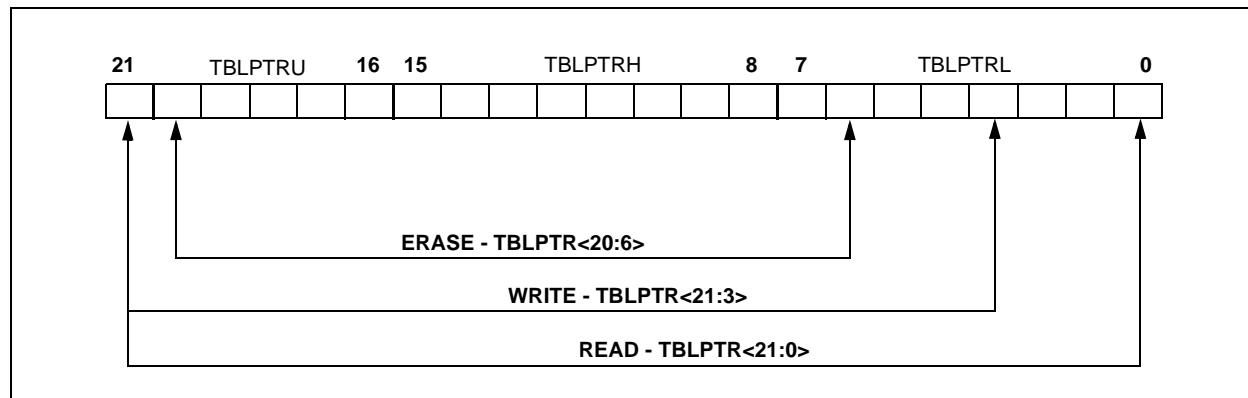
When an erase of program memory is executed, the 16 MSbs of the Table Pointer (TBLPTR<21:6>) point to the 64-byte block that will be erased. The Least Significant bits (TBLPTR<5:0>) are ignored.

Figure 5-3 describes the relevant boundaries of TBLPTR based on FLASH program memory operations.

TABLE 5-1: TABLE POINTER OPERATIONS WITH TBLRD AND TBLWT INSTRUCTIONS

Example	Operation on Table Pointer
TBLRD*	TBLPTR is not modified
TBLWT*	
TBLRD*+	TBLPTR is incremented after the read/write
TBLWT*+	
TBLRD*-	TBLPTR is decremented after the read/write
TBLWT*-	
TBLRD+*	TBLPTR is incremented before the read/write
TBLWT+*	

FIGURE 5-3: TABLE POINTER BOUNDARIES BASED ON OPERATION



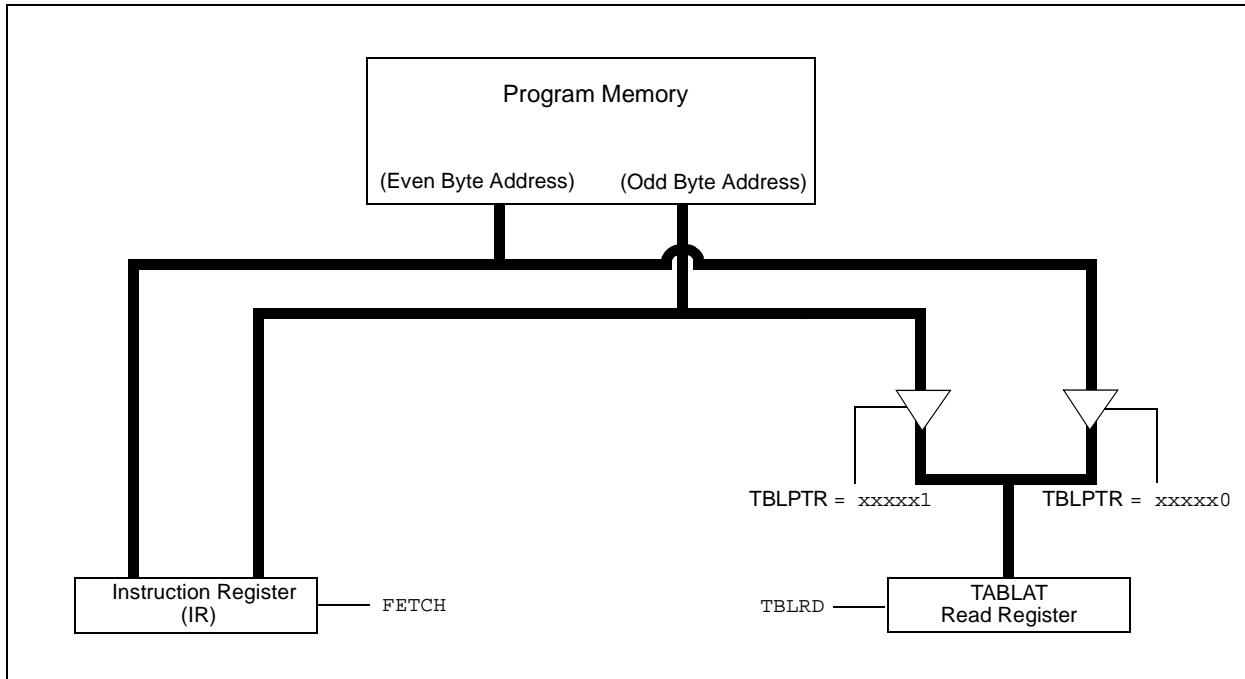
5.3 Reading the FLASH Program Memory

The TBLRD instruction is used to retrieve data from program memory and place into data RAM. Table Reads from program memory are performed one byte at a time.

TBLPTR points to a byte address in program space. Executing TBLRD places the byte pointed to into TABLAT. In addition, TBLPTR can be modified automatically for the next Table Read operation.

The internal program memory is typically organized by words. The Least Significant bit of the address selects between the high and low bytes of the word. Figure 5-4 shows the interface between the internal program memory and the TABLAT.

FIGURE 5-4: READS FROM FLASH PROGRAM MEMORY



EXAMPLE 5-1: READING A FLASH PROGRAM MEMORY WORD

```
MOVLW  CODE_ADDR_UPPER          ; Load TBLPTR with the base
MOVWF  TBLPTRU
MOVLW  CODE_ADDR_HIGH
MOVWF  TBLPTRH
MOVLW  CODE_ADDR_LOW
MOVWF  TBLPTRL

READ_WORD
    TBLRD*+
    MOVF   TABLAT, W             ; read into TABLAT and increment
    MOVWF WORD_EVEN              ; get data
    TBLRD*+
    MOVFW TABLAT, W             ; read into TABLAT and increment
    MOVWF WORD_ODD              ; get data
```

5.4 Erasing FLASH Program Memory

The minimum erase block is 32 words or 64 bytes. Only through the use of an external programmer, or through ICSP control, can larger blocks of program memory be bulk erased. Word erase in the FLASH array is not supported.

When initiating an erase sequence from the microcontroller itself, a block of 64 bytes of program memory is erased. The Most Significant 16 bits of the TBLPTR<21:6> point to the block being erased. TBLPTR<5:0> are ignored.

The EECON1 register commands the erase operation. The EEPGD bit must be set to point to the FLASH program memory. The WREN bit must be set to enable write operations. The FREE bit is set to select an erase operation.

For protection, the write initiate sequence for EECON2 must be used.

A long write is necessary for erasing the internal FLASH. Instruction execution is halted while in a long write cycle. The long write will be terminated by the internal programming timer.

5.4.1 FLASH PROGRAM MEMORY ERASE SEQUENCE

The sequence of events for erasing a block of internal program memory location is:

1. Load table pointer with address of row being erased.
2. Set the EECON1 register for the erase operation:
 - set EEPGD bit to point to program memory;
 - clear the CFGS bit to access program memory;
 - set WREN bit to enable writes;
 - set FREE bit to enable the erase.
3. Disable interrupts.
4. Write 55h to EECON2.
5. Write AAh to EECON2.
6. Set the WR bit. This will begin the row erase cycle.
7. The CPU will stall for duration of the erase (about 2 ms using internal timer).
8. Execute a NOP.
9. Re-enable interrupts.

EXAMPLE 5-2: ERASING A FLASH PROGRAM MEMORY ROW

	MOVLW CODE_ADDR_UPPER	; load TBLPTR with the base
	MOVWF TBLPTRU	; address of the memory block
	MOVLW CODE_ADDR_HIGH	
	MOVWF TBLPTRH	
	MOVLW CODE_ADDR_LOW	
	MOVWF TBLPTRL	
ERASE_ROW	BSF EECON1,EEPGD	; point to FLASH program memory
	BCF EECON1,CFGs	; access FLASH program memory
	BSF EECON1,WREN	; enable write to memory
	BSF EECON1,FREE	; enable Row Erase operation
	BCF INTCON,GIE	; disable interrupts
Required Sequence	MOVLW 55h	; write 55H
	MOVWF EECON2	
	MOVLW AAh	
	MOVWF EECON2	; write AAH
	BSF EECON1,WR	; start erase (CPU stall)
	NOP	
	BSF INTCON,GIE	; re-enable interrupts

5.5 Writing to FLASH Program Memory

The minimum programming block is 4 words or 8 bytes. Word or byte programming is not supported.

Table Writes are used internally to load the holding registers needed to program the FLASH memory. There are 8 holding registers used by the Table Writes for programming.

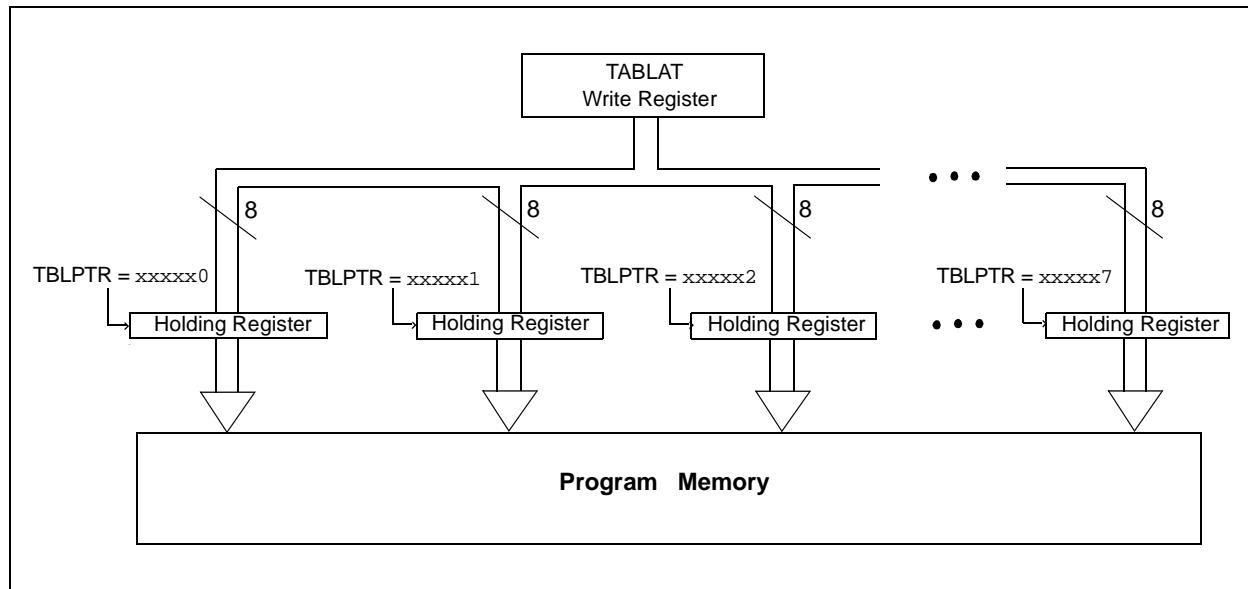
Since the Table Latch (TABLAT) is only a single byte, the TBLWT instruction has to be executed 8 times for each programming operation. All of the Table Write operations will essentially be short writes, because only

the holding registers are written. At the end of updating 8 registers, the EECON1 register must be written to, to start the programming operation with a long write.

The long write is necessary for programming the internal FLASH. Instruction execution is halted while in a long write cycle. The long write will be terminated by the internal programming timer.

The EEPROM on-chip timer controls the write time. The write/erase voltages are generated by an on-chip charge pump, rated to operate over the voltage range of the device for byte or word operations.

FIGURE 5-5: TABLE WRITES TO FLASH PROGRAM MEMORY



5.5.1 FLASH PROGRAM MEMORY WRITE SEQUENCE

The sequence of events for programming an internal program memory location should be:

1. Read 64 bytes into RAM.
2. Update data values in RAM as necessary.
3. Load Table Pointer with address being erased.
4. Do the row erase procedure.
5. Load Table Pointer with address of first byte being written.
6. Write the first 8 bytes into the holding registers with auto-increment.
7. Set the EECON1 register for the write operation:
 - set EEPGD bit to point to program memory;
 - clear the CFGS bit to access program memory;
 - set WREN to enable byte writes.
8. Disable interrupts.
9. Write 55h to EECON2.
10. Write AAh to EECON2.
11. Set the WR bit. This will begin the write cycle.
12. The CPU will stall for duration of the write (about 2 ms using internal timer).
13. Execute a NOP.
14. Re-enable interrupts.
15. Repeat steps 6-14 seven times, to write 64 bytes.
16. Verify the memory (Table Read).

This procedure will require about 18 ms to update one row of 64 bytes of memory. An example of the required code is given in Example 5-3.

Note: Before setting the WR bit, the Table Pointer address needs to be within the intended address range of the eight bytes in the holding register.

EXAMPLE 5-3: WRITING TO FLASH PROGRAM MEMORY

```

        MOVLW  D'64                      ; number of bytes in erase block
        MOVWF  COUNTER
        MOVLW  BUFFER_ADDR_HIGH          ; point to buffer
        MOVWF  FSR0H
        MOVLW  BUFFER_ADDR_LOW
        MOVWF  FSROL
        MOVLW  CODE_ADDR_UPPER          ; Load TBLPTR with the base
        MOVWF  TBLPTRU                  ; address of the memory block
        MOVLW  CODE_ADDR_HIGH
        MOVWF  TBLPTRH
        MOVLW  CODE_ADDR_LOW
        MOVWF  TBLPTRL

READ_BLOCK
        TBLRD*+
        MOVF   TABLAT, W               ; read into TABLAT, and inc
        MOVWF  POSTINCO
        DECFSZ COUNTER
        BRA    READ_BLOCK              ; done?
                                         ; repeat

MODIFY_WORD
        MOVLW  DATA_ADDR_HIGH          ; point to buffer
        MOVWF  FSR0H
        MOVLW  DATA_ADDR_LOW
        MOVWF  FSROL
        MOVLW  NEW_DATA_LOW           ; update buffer word
        MOVWF  POSTINCO
        MOVLW  NEW_DATA_HIGH
        MOVWF  INDF0

ERASE_BLOCK
        MOVLW  CODE_ADDR_UPPER          ; load TBLPTR with the base
        MOVWF  TBLPTRU                  ; address of the memory block
        MOVLW  CODE_ADDR_HIGH
        MOVWF  TBLPTRH
        MOVLW  CODE_ADDR_LOW
        MOVWF  TBLPTRL
        BSF    EECON1,EEPGD            ; point to FLASH program memory
        BCF    EECON1,CFG5
        BSF    EECON1,WREN             ; enable write to memory
        BSF    EECON1,FREE             ; enable Row Erase operation
        BCF    INTCON,GIE              ; disable interrupts

Required Sequence
        MOVLW  55h
        MOVWF  EECON2
        MOVLW  AAh
        MOVWF  EECON2
        BSF    EECON1,WR              ; start erase (CPU stall)
        NOP

        BSF    INTCON,GIE            ; re-enable interrupts
        TBLRD*-                     ; dummy read decrement

WRITE_BUFFER_BACK
        MOVLW  8                       ; number of write buffer groups of 8 bytes
        MOVWF  COUNTER_HI
        MOVLW  BUFFER_ADDR_HIGH          ; point to buffer
        MOVWF  FSR0H
        MOVLW  BUFFER_ADDR_LOW
        MOVWF  FSROL

PROGRAM_LOOP
        MOVLW  8                       ; number of bytes in holding register
        MOVWF  COUNTER

WRITE_WORD_TO_HREGS
        MOVFW  POSTINCO, W             ; get low byte of buffer data
        MOVWF  TABLAT
        TBLWT+*                      ; present data to table latch
                                         ; write data, perform a short write
                                         ; to internal TBLWT holding register.
                                         ; loop until buffers are full
        DECFSZ COUNTER
        BRA    WRITE_WORD_TO_HREGS

```

EXAMPLE 5-3: WRITING TO FLASH PROGRAM MEMORY (CONTINUED)

PROGRAM_MEMORY		
	BSF EECON1, EEPGD	; point to FLASH program memory
	BCF EECON1, CFGS	; access FLASH program memory
	BSF EECON1, WREN	; enable write to memory
	BCF INTCON, GIE	; disable interrupts
Required Sequence	MOVLW 55h	
	MOVWF EECON2	; write 55H
	MOVLW AAh	
	MOVWF EECON2	; write AAH
	BSF EECON1, WR	; start program (CPU stall)
	NOP	
	BSF INTCON, GIE	; re-enable interrupts
	DECFSZ COUNTER_HI	; loop until done
	BRA PROGRAM_LOOP	
	BCF EECON1, WREN	; disable write to memory

5.5.2 WRITE VERIFY

Depending on the application, good programming practice may dictate that the value written to the memory should be verified against the original value. This should be used in applications where excessive writes can stress bits near the specification limit.

5.5.3 UNEXPECTED TERMINATION OF WRITE OPERATION

If a write is terminated by an unplanned event, such as loss of power or an unexpected RESET, the memory location just programmed should be verified and reprogrammed if needed. The WRERR bit is set when a write operation is interrupted by a MCLR Reset, or a WDT

Time-out Reset during normal operation. In these situations, users can check the WRERR bit and rewrite the location.

5.5.4 PROTECTION AGAINST SPURIOUS WRITES

To protect against spurious writes to FLASH program memory, the write initiate sequence must also be followed. See "Special Features of the CPU" (Section 23.0) for more detail.

5.6 FLASH Program Operation During Code Protection

See "Special Features of the CPU" (Section 23.0) for details on code protection of FLASH program memory.

TABLE 5-2: REGISTERS ASSOCIATED WITH PROGRAM FLASH MEMORY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
TBLPTRU	—	—	bit21	Program Memory Table Pointer Upper Byte (TBLPTR<20:16>)					--00 0000	--00 0000
TBPLTRH	Program Memory Table Pointer High Byte (TBLPTR<15:8>)					0000 0000			0000 0000	0000 0000
TBLPTRL	Program Memory Table Pointer High Byte (TBLPTR<7:0>)					0000 0000			0000 0000	0000 0000
TABLAT	Program Memory Table Latch					0000 0000			0000 0000	0000 0000
INTCON	GIE/GIEH	PEIE/GIEL	TMROIE	INTE	RBIE	TMR0IF	INTF	RBIF	0000 0000	0000 0000
EECON2	EEPROM Control Register2 (not a physical register)					—			—	—
EECON1	EEPGD	CFGs	—	FREE	WRERR	WREN	WR	RD	xx-0 x000	uu-0 u000
IPR2	—	CMIP	—	EEIP	BCLIP	LVDIP	TMR3IP	CCP2IP	---1 1111	---1 1111
PIR2	—	CMIF	—	EEIF	BCLIF	LVDIF	TMR3IF	CCP2IF	---0 0000	---0 0000
PIE2	—	CMIE	—	EEIE	BCLIE	LVDIE	TMR3IE	CCP2IE	---0 0000	---0 0000

Legend: x = unknown, u = unchanged, r = reserved, - = unimplemented, read as '0'.

Shaded cells are not used during FLASH/EEPROM access.

6.0 EXTERNAL MEMORY INTERFACE

Note: The External Memory Interface is not implemented on PIC18F6X20 (64-pin) devices.

The External Memory Interface is a feature of the PIC18F8X20 devices that allows the controller to access external memory devices (such as FLASH, EPROM, SRAM, etc.) as program memory.

The physical implementation of the interface uses 27 pins. These pins are reserved for external address/data bus functions; they are multiplexed with I/O port pins on four ports. Three I/O ports are multiplexed with the address/data bus, while the fourth port is multiplexed with the bus control signals. The I/O port functions are enabled when the EBDIS bit in the MEMCON register is set (see Register 6-1). A list of the multiplexed pins and their functions is provided in Table 6-1.

As implemented in the PIC18F8X20 devices, the interface operates in a similar manner to the external memory interface introduced on PIC18C601/801 microcontrollers. The most notable difference is that the interface on PIC18F8X20 devices only operates in 16-bit modes. The 8-bit mode is not supported.

For a more complete discussion of the operating modes that use the external memory interface, refer to Section 4.1.1 (“PIC18F8X20 Program Memory Modes”).

REGISTER 6-1: MEMCON REGISTER

EVDIS: External Bus Disable bit
1 = External system bus disabled, all external bus drivers are mapped as I/O ports
0 = External system bus enabled, and I/O ports are disabled

bit 6 **Unimplemented:** Read as '0'

bit 5-4 **WAIT<1:0>**: Table Reads and Writes Bus Cycle Wait Count bits

11 = Table reads and writes will wait 0 Tcy
10 = Table reads and writes will wait 1 Tcy
01 = Table reads and writes will wait 2 Tcy
00 = Table reads and writes will wait 3 Tcy

bit 3-2 **Unimplemented:** Read as '0'

bit 1-0 **WM<1:0>**: TABLWT Operation with 16-bit Bus bits

1X = Word Write mode: TABLAT0 and TABLAT1 word output, WRH active when TABLAT1 written
 01 = Byte Select mode: TABLAT data copied on both MS and LS Byte, WRH and (UB or LB) will activate
 00 = Byte Write mode: TABLAT data copied on both MS and LS Byte, WRH or WRL will activate

Legend:

R = Readable bit

- n = Value at POR

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

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If the device fetches or accesses external memory while EBDIS = '1', the pins will switch to external bus. If the EBDIS bit is set by a program executing from external memory, the action of setting the bit will be delayed until the program branches into the internal memory. At that time, the pins will change from external bus to I/O ports.

When the device is executing out of internal memory (EBDIS = '0') in Microprocessor with Boot Block mode or Extended Microcontroller mode, the control signals will NOT be active. They will go to a state where the AD<15:0>, A<19:16> are tri-state; the \overline{OE} , WRH, WRL, \overline{UB} and \overline{LB} signals are '1'; and ALE and BA0 are '0'.

TABLE 6-1: PIC18F8X20 EXTERNAL BUS - I/O PORT FUNCTIONS

Name	Port	Bit	Function
RD0/AD0	PORTD	bit0	Input/Output or System Bus Address bit 0 or Data bit 0
RD1/AD1	PORTD	bit1	Input/Output or System Bus Address bit 1 or Data bit 1
RD2/AD2	PORTD	bit2	Input/Output or System Bus Address bit 2 or Data bit 2
RD3/AD3	PORTD	bit3	Input/Output or System Bus Address bit 3 or Data bit 3
RD4/AD4	PORTD	bit4	Input/Output or System Bus Address bit 4 or Data bit 4
RD5/AD5	PORTD	bit5	Input/Output or System Bus Address bit 5 or Data bit 5
RD6/AD6	PORTD	bit6	Input/Output or System Bus Address bit 6 or Data bit 6
RD7/AD7	PORTD	bit7	Input/Output or System Bus Address bit 7 or Data bit 7
RE0/AD8	PORTE	bit0	Input/Output or System Bus Address bit 8 or Data bit 8
RE1/AD9	PORTE	bit1	Input/Output or System Bus Address bit 9 or Data bit 9
RE2/AD10	PORTE	bit2	Input/Output or System Bus Address bit 10 or Data bit 10
RE3/AD11	PORTE	bit3	Input/Output or System Bus Address bit 11 or Data bit 11
RE4/AD12	PORTE	bit4	Input/Output or System Bus Address bit 12 or Data bit 12
RE5/AD13	PORTE	bit5	Input/Output or System Bus Address bit 13 or Data bit 13
RE6/AD14	PORTE	bit6	Input/Output or System Bus Address bit 14 or Data bit 14
RE7/AD15	PORTE	bit7	Input/Output or System Bus Address bit 15 or Data bit 15
RH0/A16	PORTH	bit0	Input/Output or System Bus Address bit 16
RH1/A17	PORTH	bit1	Input/Output or System Bus Address bit 17
RH2/A18	PORTH	bit2	Input/Output or System Bus Address bit 18
RH3/A19	PORTH	bit3	Input/Output or System Bus Address bit 19
RJ0/ALE	PORTJ	bit0	Input/Output or System Bus Address Latch Enable (ALE) Control pin
RJ1/ \overline{OE}	PORTJ	bit1	Input/Output or System Bus Output Enable (\overline{OE}) Control pin
RJ2/WRL	PORTJ	bit2	Input/Output or System Bus Write Low (WRL) Control pin
RJ3/ \overline{WRH}	PORTJ	bit3	Input/Output or System Bus Write High (\overline{WRH}) Control pin
RJ4/BA0	PORTJ	bit4	Input/Output or System Bus Byte Address bit 0
RJ6/ \overline{LB}	PORTJ	bit6	Input/Output or System Bus Lower Byte Enable (\overline{LB}) Control pin
RJ7/ \overline{UB}	PORTJ	bit7	Input/Output or System Bus Upper Byte Enable (\overline{UB}) Control pin

6.2 16-bit Mode

The External Memory Interface implemented in PIC18F8X20 devices operates only in 16-bit mode. The mode selection is not software configurable, but is programmed via the configuration bits.

The WM<1:0> bits in the MEMCON register determine three types of connections in 16-bit mode. They are referred to as:

- 16-bit Byte Write
- 16-bit Word Write
- 16-bit Byte Select

These three different configurations allow the designer maximum flexibility in using 8-bit and 16-bit memory devices.

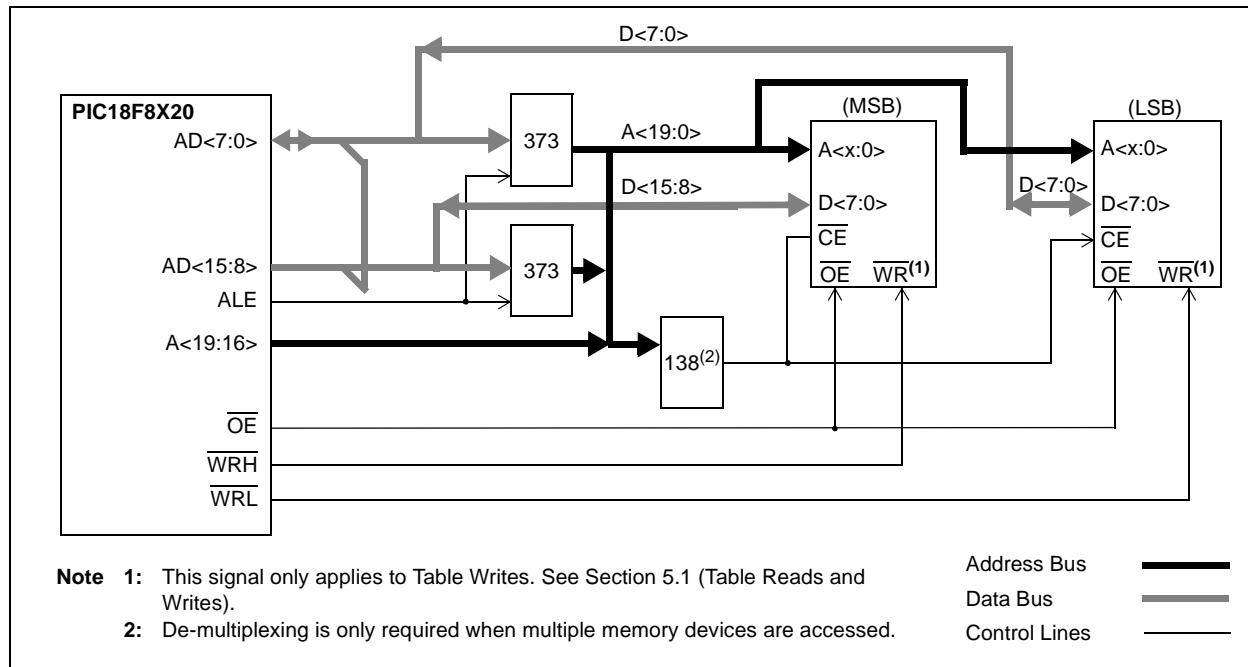
For all 16-bit modes, the Address Latch Enable (ALE) pin indicates that the address bits A<15:0> are available on the External Memory Interface bus. Following the address latch, the output enable signal (\overline{OE}) will enable both bytes of program memory at once to form a 16-bit instruction word.

In Byte Select mode, JEDEC standard FLASH memories will require BA0 for the byte address line, and one I/O line, to select between Byte and Word mode. The other 16-bit modes do not need BA0. JEDEC standard static RAM memories will use the UB or UL signals for byte selection.

6.2.1 16-BIT BYTE WRITE MODE

Figure 6-1 shows an example of 16-bit Byte Write mode for PIC18F8X20 devices.

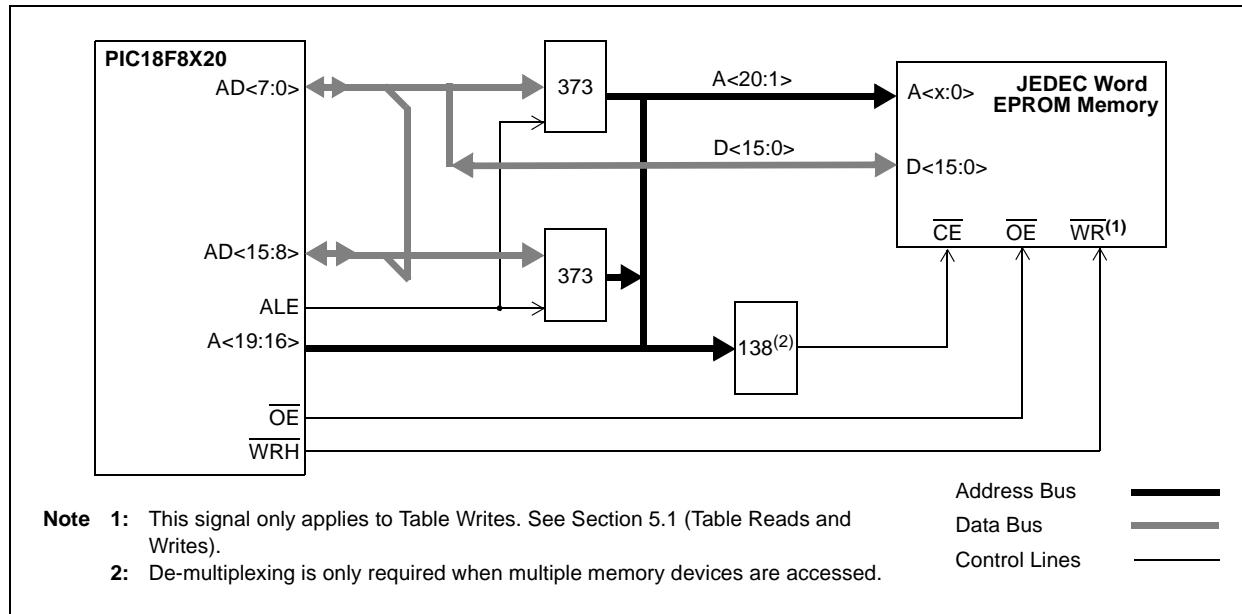
FIGURE 6-1: 16-BIT BYTE WRITE MODE EXAMPLE



6.2.2 16-BIT WORD WRITE MODE

Figure 6-2 shows an example of 16-bit Word Write mode for PIC18F8X20 devices.

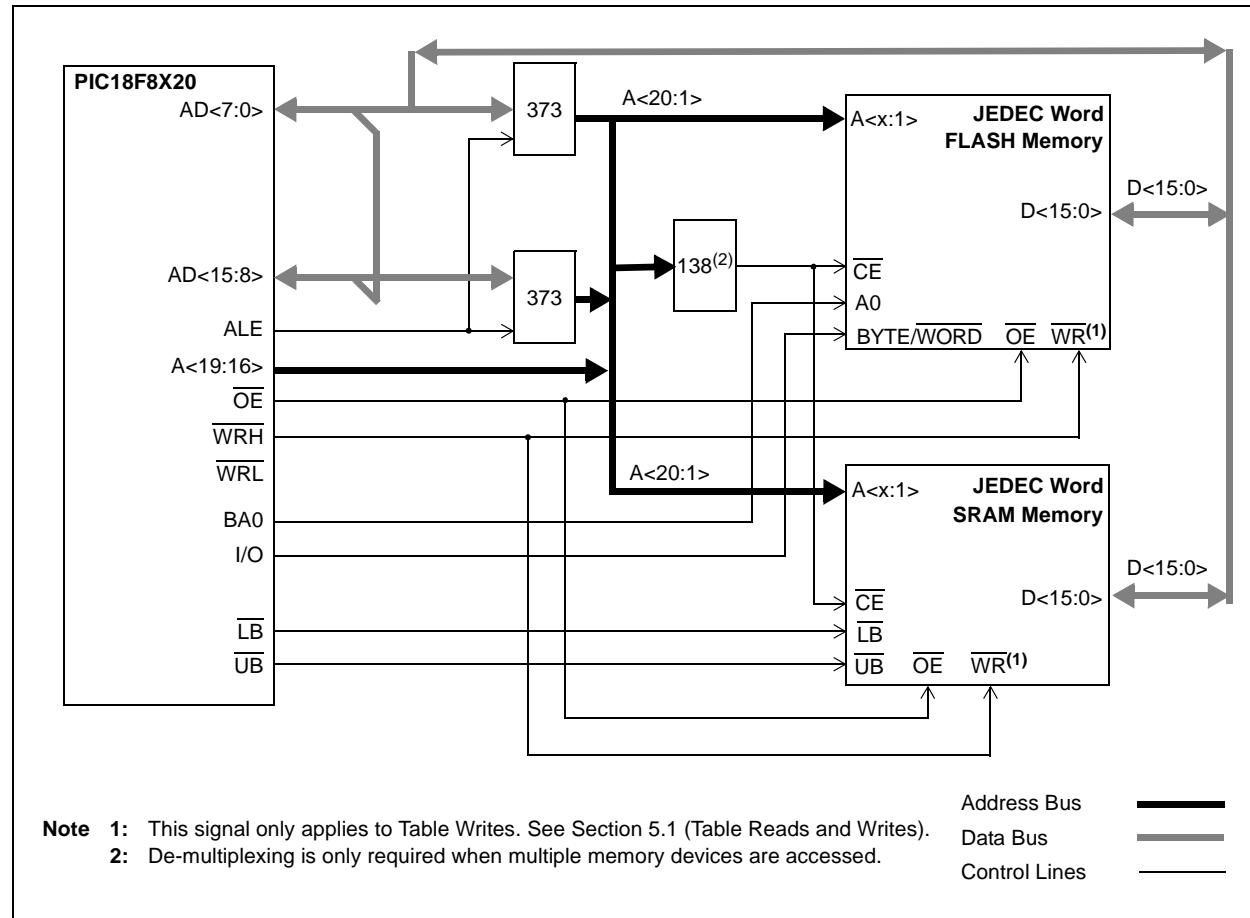
FIGURE 6-2: 16-BIT WORD WRITE MODE EXAMPLE



6.2.3 16-BIT BYTE SELECT MODE

Figure 6-3 shows an example of 16-bit Byte Select mode for PIC18F8X20 devices.

FIGURE 6-3: 16-BIT BYTE SELECT MODE EXAMPLE

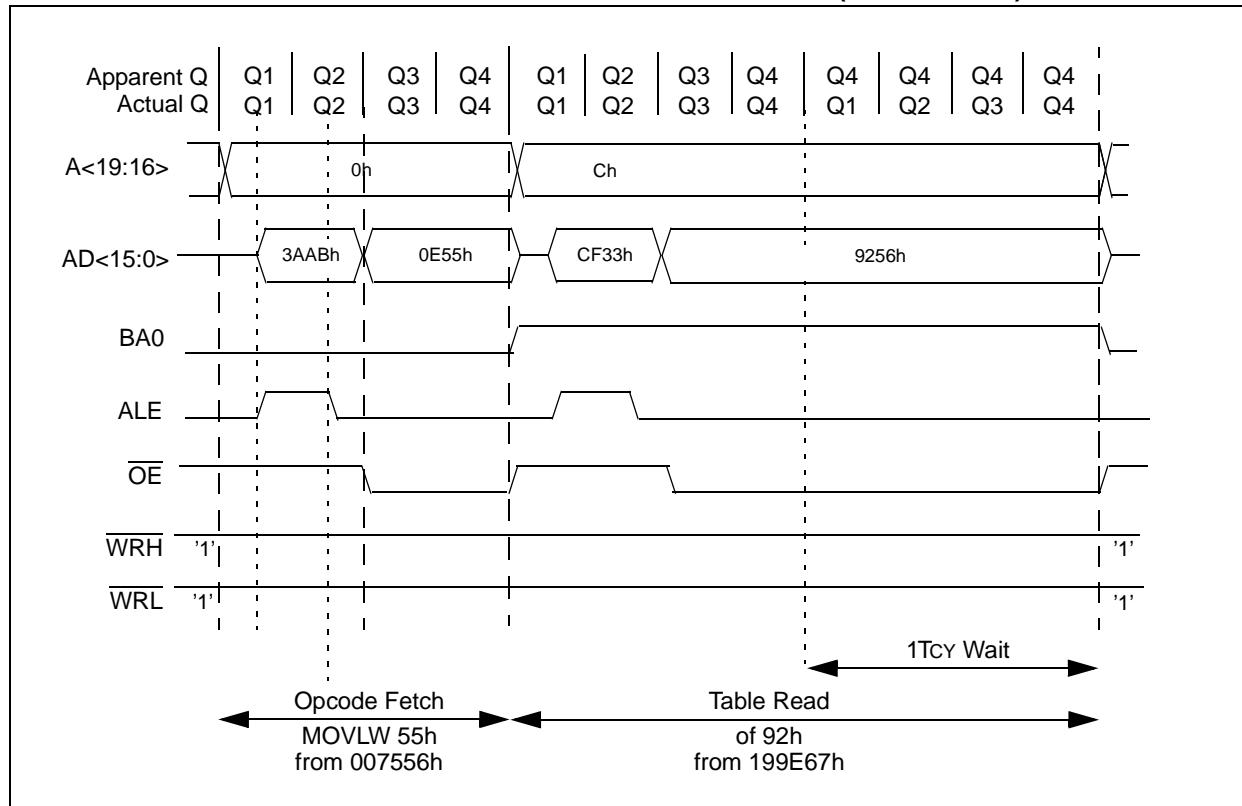


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6.2.4 16-BIT MODE TIMING

Figure 6-4 shows the 16-bit mode external bus timing for PIC18F8X20 devices.

FIGURE 6-4: EXTERNAL PROGRAM MEMORY BUS TIMING (16-BIT MODE)



7.0 DATA EEPROM MEMORY

The Data EEPROM is readable and writable during normal operation over the entire VDD range. The data memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers (SFR).

There are five SFRs used to read and write the program and data EEPROM memory. These registers are:

- EECON1
- EECON2
- EEDATA
- EEADRH
- EEADR

The EEPROM data memory allows byte read and write. When interfacing to the data memory block, EEDATA holds the 8-bit data for read/write. EEADR and EEADRH hold the address of the EEPROM location being accessed. These devices have 1024 bytes of data EEPROM with an address range from 00h to 3FFh.

The EEPROM data memory is rated for high erase/write cycles. A byte write automatically erases the location and writes the new data (erase-before-write). The write time is controlled by an on-chip timer. The write time will vary with voltage and temperature, as well as from chip to chip. Please refer to parameter D122 (Electrical Characteristics, Section 26.0) for exact limits.

7.1 EEADR and EEADRH

The address register pair can address up to a maximum of 1024 bytes of data EEPROM. The two MSbits of the address are stored in EEADRH, while the remaining eight LSbits are stored in EEADR. The six Most Significant bits of EEADRH are unused, and are read as '0'.

7.2 EECON1 and EECON2 Registers

EECON1 is the control register for EEPROM memory accesses.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the EEPROM write sequence.

Control bits RD and WR initiate read and write operations, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at the completion of the read or write operation. The inability to clear the WR bit in software prevents the accidental or premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a MCLR Reset, or a WDT Time-out Reset during normal operation. In these situations, the user can check the WRERR bit and rewrite the location. It is necessary to reload the data and address registers (EEDATA and EEADR), due to the RESET condition forcing the contents of the registers to zero.

Note: Interrupt flag bit, EEIF in the PIR2 register, is set when write is complete. It must be cleared in software.

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REGISTER 7-1: EECON1 REGISTER (ADDRESS FA6h)

- | | |
|-------|--|
| bit 7 | EEPGD: FLASH Program/Data EEPROM Memory Select bit
1 = Access FLASH Program memory
0 = Access Data EEPROM memory |
| bit 6 | CFGS: FLASH Program/Data EEPROM or Configuration Select bit
1 = Access Configuration or Calibration registers
0 = Access FLASH Program or Data EEPROM memory |
| bit 5 | Unimplemented: Read as '0' |
| bit 4 | FREE: FLASH Row Erase Enable bit
1 = Erase the program memory row addressed by TBLPTR on the next WR command
(cleared by completion of erase operation)
0 = Perform write only |
| bit 3 | WRERR: FLASH Program/Data EEPROM Error Flag bit
1 = A write operation is prematurely terminated
(any MCLR or any WDT Reset during self-timed programming in normal operation)
0 = The write operation completed

Note: When a WRERR occurs, the EEPGD or FREE bits are not cleared. This allows tracing of the error condition. |
| bit 2 | WREN: FLASH Program/Data EEPROM Write Enable bit
1 = Allows write cycles
0 = Inhibits write to the EEPROM |
| bit 1 | WR: Write Control bit
1 = Initiates a data EEPROM erase/write cycle or a program memory erase cycle or write cycle.
(The operation is self-timed and the bit is cleared by hardware once write is complete. The WR bit can only be set (not cleared) in software.)
0 = Write cycle to the EEPROM is complete |
| bit 0 | RD: Read Control bit
1 = Initiates an EEPROM read
(Read takes one cycle. RD is cleared in hardware. The RD bit can only be set (not cleared) in software. RD bit cannot be set when EEPGD = 1.)
0 = Does not initiate an EEPROM read |

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared x = Bit is unknown

7.3 Reading the Data EEPROM Memory

To read a data memory location, the user must write the address to the EEADRH:EEADR register pair, clear the EEPGD control bit (EECON1<7>) and then set control

bit RD (EECON1<0>). The data is available for the very next instruction cycle; therefore, the EEDATA register can be read by the next instruction. EEDATA will hold this value until another read operation, or until it is written to by the user (during a write operation).

EXAMPLE 7-1: DATA EEPROM READ

MOVLW	DATA_EE_ADDRH	;
MOVWF	EEADRH	; Upper bits of Data Memory Address to read
MOVLW	DATA_EE_ADDR	;
MOVWF	EEADR	; Lower bits of Data Memory Address to read
BCF	EECON1, EEPGD	; Point to DATA memory
BSF	EECON1, RD	; EEPROM Read
MOVF	EEDATA, W	; W = EEDATA

7.4 Writing to the Data EEPROM Memory

To write an EEPROM data location, the address must first be written to the EEADRH:EEADR register pair and the data written to the EEDATA register. Then the sequence in Example 7-2 must be followed to initiate the write cycle.

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. It is strongly recommended that interrupts be disabled during this code segment.

Additionally, the WREN bit in EECON1 must be set to enable writes. This mechanism prevents accidental writes to data EEPROM due to unexpected code exe-

cution (i.e., runaway programs). The WREN bit should be kept clear at all times, except when updating the EEPROM. The WREN bit is not cleared by hardware

After a write sequence has been initiated, EECON1, EEADRH, EEADR and EEDATA cannot be modified. The WR bit will be inhibited from being set unless the WREN bit is set. The WREN bit must be set on a previous instruction. Both WR and WREN cannot be set with the same instruction.

At the completion of the write cycle, the WR bit is cleared in hardware and the EEPROM Write Complete Interrupt Flag bit (EEIF) is set. The user may either enable this interrupt, or poll this bit. EEIF must be cleared by software.

EXAMPLE 7-2: DATA EEPROM WRITE

	MOVLW	DATA_EE_ADDRH	;
	MOVWF	EEADRH	; Upper bits of Data Memory Address to write
	MOVLW	DATA_EE_ADDR	;
	MOVWF	EEADR	; Lower bits of Data Memory Address to write
	MOVLW	DATA_EE_DATA	;
	MOVWF	EEDATA	; Data Memory Value to write
	BCF	EECON1, EEPGD	; Point to DATA memory
	BSF	EECON1, WREN	; Enable writes
	BCF	INTCON, GIE	; Disable Interrupts
Required Sequence	MOVLW	55h	;
	MOVWF	EECON2	; Write 55h
	MOVLW	AAh	;
	MOVWF	EECON2	; Write AAh
	BSF	EECON1, WR	; Set WR bit to begin write
	BSF	INTCON, GIE	; Enable Interrupts
			; User code execution
	BCF	EECON1, WREN	; Disable writes on write complete (EEIF set)

7.5 Write Verify

Depending on the application, good programming practice may dictate that the value written to the memory should be verified against the original value. This should be used in applications where excessive writes can stress bits near the specification limit.

7.6 Protection Against Spurious Write

There are conditions when the device may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built-in. On power-up, the WREN bit is cleared. Also, the Power-up Timer (72 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during brown-out, power glitch, or software malfunction.

7.7 Operation During Code Protect

Data EEPROM memory has its own code protect mechanism. External Read and Write operations are disabled if either of these mechanisms are enabled.

The microcontroller itself can both read and write to the internal Data EEPROM, regardless of the state of the code protect configuration bit. Refer to "Special Features of the CPU" (Section 23.0) for additional information.

TABLE 7-1: REGISTERS ASSOCIATED WITH DATA EEPROM MEMORY

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
EEADRH	—	—	—	—	—	—	EE Addr Register High	—	— 00	— 00
EEADR	EEPROM Address Register								0000 0000	0000 0000
EEDATA	EEPROM Data Register								0000 0000	0000 0000
EECON2	EEPROM Control Register2 (not a physical register)								—	—
EECON1	EEPGD	CFGs	—	FREE	WRERR	WREN	WR	RD	xx-0 x000	uu-0 u000
IPR2	—	CMIP	—	EEIP	BCLIP	LVDIP	TMR3IP	CCP2IP	---1 1111	---1 1111
PIR2	—	CMIF	—	EEIF	BCLIF	LVDIF	TMR3IF	CCP2IF	---0 0000	---0 0000
PIE2	—	CMIE	—	EEIE	BCLIE	LVDIE	TMR3IE	CCP2IE	---0 0000	---0 0000

Legend: x = unknown, u = unchanged, r = reserved, - = unimplemented, read as '0'.

Shaded cells are not used during FLASH/EEPROM access.

8.0 8 X 8 HARDWARE MULTIPLIER

8.1 Introduction

An 8 x 8 hardware multiplier is included in the ALU of the PIC18FXX20 devices. By making the multiply a hardware operation, it completes in a single instruction cycle. This is an unsigned multiply that gives a 16-bit result. The result is stored in the 16-bit product register pair (PRODH:PRODL). The multiplier does not affect any flags in the ALUSTA register.

Making the 8 x 8 multiplier execute in a single cycle gives the following advantages:

- Higher computational throughput
- Reduces code size requirements for multiply algorithms

The performance increase allows the device to be used in applications previously reserved for Digital Signal Processors.

Table 8-1 shows a performance comparison between enhanced devices using the single cycle hardware multiply, and performing the same function without the hardware multiply.

8.2 Operation

Example 8-1 shows the sequence to do an 8 x 8 unsigned multiply. Only one instruction is required when one argument of the multiply is already loaded in the WREG register.

Example 8-2 shows the sequence to do an 8 x 8 signed multiply. To account for the sign bits of the arguments, each argument's Most Significant bit (MSb) is tested and the appropriate subtractions are done.

EXAMPLE 8-1: 8 x 8 UNSIGNED MULTIPLY ROUTINE

```
MOVF    ARG1, W      ;  
MULWF   ARG2          ; ARG1 * ARG2 ->  
                    ; PRODH:PRODL
```

EXAMPLE 8-2: 8 x 8 SIGNED MULTIPLY ROUTINE

```
MOVF    ARG1, W      ;  
MULWF   ARG2          ; ARG1 * ARG2 ->  
                    ; PRODH:PRODL  
BTFSCL  ARG2, SB     ; Test Sign Bit  
SUBWF   PRODH, F      ; PRODH = PRODH  
                    ; - ARG1  
MOVF    ARG2, W      ;  
BTFSCL  ARG1, SB     ; Test Sign Bit  
SUBWF   PRODH, F      ; PRODH = PRODH  
                    ; - ARG2
```

TABLE 8-1: PERFORMANCE COMPARISON

Routine	Multiply Method	Program Memory (Words)	Cycles (Max)	Time		
				@ 40 MHz	@ 10 MHz	@ 4 MHz
8 x 8 unsigned	Without hardware multiply	13	69	6.9 µs	27.6 µs	69 µs
	Hardware multiply	1	1	100 ns	400 ns	1 µs
8 x 8 signed	Without hardware multiply	33	91	9.1 µs	36.4 µs	91 µs
	Hardware multiply	6	6	600 ns	2.4 µs	6 µs
16 x 16 unsigned	Without hardware multiply	21	242	24.2 µs	96.8 µs	242 µs
	Hardware multiply	24	24	2.4 µs	9.6 µs	24 µs
16 x 16 signed	Without hardware multiply	52	254	25.4 µs	102.6 µs	254 µs
	Hardware multiply	36	36	3.6 µs	14.4 µs	36 µs

Example 8-3 shows the sequence to do a 16 x 16 unsigned multiply. Equation 8-1 shows the algorithm that is used. The 32-bit result is stored in four registers, RES3:RES0.

EQUATION 8-1: 16 x 16 UNSIGNED MULTIPLICATION ALGORITHM

$$\begin{aligned} \text{RES3:RES0} &= \text{ARG1H:ARG1L} \cdot \text{ARG2H:ARG2L} \\ &= (\text{ARG1H} \cdot \text{ARG2H} \cdot 2^{16}) + \\ &\quad (\text{ARG1H} \cdot \text{ARG2L} \cdot 2^8) + \\ &\quad (\text{ARG1L} \cdot \text{ARG2H} \cdot 2^8) + \\ &\quad (\text{ARG1L} \cdot \text{ARG2L}) \end{aligned}$$

EXAMPLE 8-3: 16 x 16 UNSIGNED MULTIPLY ROUTINE

```

MOVF ARG1L, W
MULWF ARG2L      ; ARG1L * ARG2L ->
                  ; PRODH:PRODL
MOVFF PRODH, RES1 ;
MOVFF PRODL, RES0 ;
;

MOVF ARG1H, W
MULWF ARG2H      ; ARG1H * ARG2H ->
                  ; PRODH:PRODL
MOVFF PRODH, RES3 ;
MOVFF PRODL, RES2 ;
;

MOVF ARG1L, W
MULWF ARG2H      ; ARG1L * ARG2H ->
                  ; PRODH:PRODL
MOVF PRODL, W   ;
ADDWF RES1, F    ; Add cross
MOVF PRODH, W   ; products
ADDWFC RES2, F   ;
CLRF WREG       ;
ADDWFC RES3, F   ;
;

MOVF ARG1H, W
MULWF ARG2L      ; ARG1H * ARG2L ->
                  ; PRODH:PRODL
MOVF PRODL, W   ;
ADDWF RES1, F    ; Add cross
MOVF PRODH, W   ; products
ADDWFC RES2, F   ;
CLRF WREG       ;
ADDWFC RES3, F   ;
;
```

Example 8-4 shows the sequence to do a 16 x 16 signed multiply. Equation 8-2 shows the algorithm used. The 32-bit result is stored in four registers, RES3:RES0. To account for the sign bits of the arguments, each argument pairs Most Significant bit (MSb) is tested and the appropriate subtractions are done.

EQUATION 8-2: 16 x 16 SIGNED MULTIPLICATION ALGORITHM

$$\begin{aligned} \text{RES3:RES0} &= \text{ARG1H:ARG1L} \cdot \text{ARG2H:ARG2L} \\ &= (\text{ARG1H} \cdot \text{ARG2H} \cdot 2^{16}) + \\ &\quad (\text{ARG1H} \cdot \text{ARG2L} \cdot 2^8) + \\ &\quad (\text{ARG1L} \cdot \text{ARG2H} \cdot 2^8) + \\ &\quad (\text{ARG1L} \cdot \text{ARG2L}) + \\ &\quad (-1 \cdot \text{ARG2H} < 7> \cdot \text{ARG1H:ARG1L} \cdot 2^{16}) + \\ &\quad (-1 \cdot \text{ARG1H} < 7> \cdot \text{ARG2H:ARG2L} \cdot 2^{16}) \end{aligned}$$

EXAMPLE 8-4: 16 x 16 SIGNED MULTIPLY ROUTINE

```

MOVF ARG1L, W
MULWF ARG2L      ; ARG1L * ARG2L ->
                  ; PRODH:PRODL
MOVFF PRODH, RES1 ;
MOVFF PRODL, RES0 ;
;

MOVF ARG1H, W
MULWF ARG2H      ; ARG1H * ARG2H ->
                  ; PRODH:PRODL
MOVFF PRODH, RES3 ;
MOVFF PRODL, RES2 ;
;

MOVF ARG1L, W
MULWF ARG2H      ; ARG1L * ARG2H ->
                  ; PRODH:PRODL
MOVF PRODL, W   ;
ADDWF RES1, F    ; Add cross
MOVF PRODH, W   ; products
ADDWFC RES2, F   ;
CLRF WREG       ;
ADDWFC RES3, F   ;
;

MOVF ARG1H, W
MULWF ARG2L      ; ARG1H * ARG2L ->
                  ; PRODH:PRODL
MOVF PRODL, W   ;
ADDWF RES1, F    ; Add cross
MOVF PRODH, W   ; products
ADDWFC RES2, F   ;
CLRF WREG       ;
ADDWFC RES3, F   ;
;

BTFS ARG2H, 7     ; ARG2H:ARG2L neg?
BRA SIGN_ARG1    ; no, check ARG1
MOVF ARG1L, W   ;
SUBWF RES2       ;
MOVF ARG1H, W   ;
SUBWFB RES3     ;
;

SIGN_ARG1
BTFS ARG1H, 7     ; ARG1H:ARG1L neg?
BRA CONT_CODE    ; no, done
MOVF ARG2L, W   ;
SUBWF RES2       ;
MOVF ARG2H, W   ;
SUBWFB RES3     ;
;

CONT_CODE
:
```

9.0 INTERRUPTS

The PIC18FXX20 devices have multiple interrupt sources and an interrupt priority feature that allows each interrupt source to be assigned a high or a low priority level. The high priority interrupt vector is at 000008h, while the low priority interrupt vector is at 000018h. High priority interrupt events will override any low priority interrupts that may be in progress.

There are thirteen registers which are used to control interrupt operation. They are:

- RCON
- INTCON
- INTCON2
- INTCON3
- PIR1, PIR2, PIR3
- PIE1, PIE2, PIE3
- IPR1, IPR2, IPR3

It is recommended that the Microchip header files supplied with MPLAB® IDE be used for the symbolic bit names in these registers. This allows the assembler/compiler to automatically take care of the placement of these bits within the specified register.

Each interrupt source has three bits to control its operation. The functions of these bits are:

- Flag bit to indicate that an interrupt event occurred
- Enable bit that allows program execution to branch to the interrupt vector address when the flag bit is set
- Priority bit to select high priority or low priority

The interrupt priority feature is enabled by setting the IPEN bit (RCON<7>). When interrupt priority is enabled, there are two bits which enable interrupts globally. Setting the GIEH bit (INTCON<7>) enables all interrupts that have the priority bit set. Setting the GIEL bit (INTCON<6>) enables all interrupts that have the priority bit cleared. When the interrupt flag, enable bit and appropriate global interrupt enable bit are set, the interrupt will vector immediately to address 000008h or 000018h, depending on the priority level. Individual interrupts can be disabled through their corresponding enable bits.

When the IPEN bit is cleared (default state), the interrupt priority feature is disabled and interrupts are compatible with PICmicro® mid-range devices. In Compatibility mode, the interrupt priority bits for each source have no effect. INTCON<6> is the PEIE bit, which enables/disables all peripheral interrupt sources. INTCON<7> is the GIE bit, which enables/disables all interrupt sources. All interrupts branch to address 000008h in Compatibility mode.

When an interrupt is responded to, the Global Interrupt Enable bit is cleared to disable further interrupts. If the IPEN bit is cleared, this is the GIE bit. If interrupt priority levels are used, this will be either the GIEH or GIEL bit. High priority interrupt sources can interrupt a low priority interrupt.

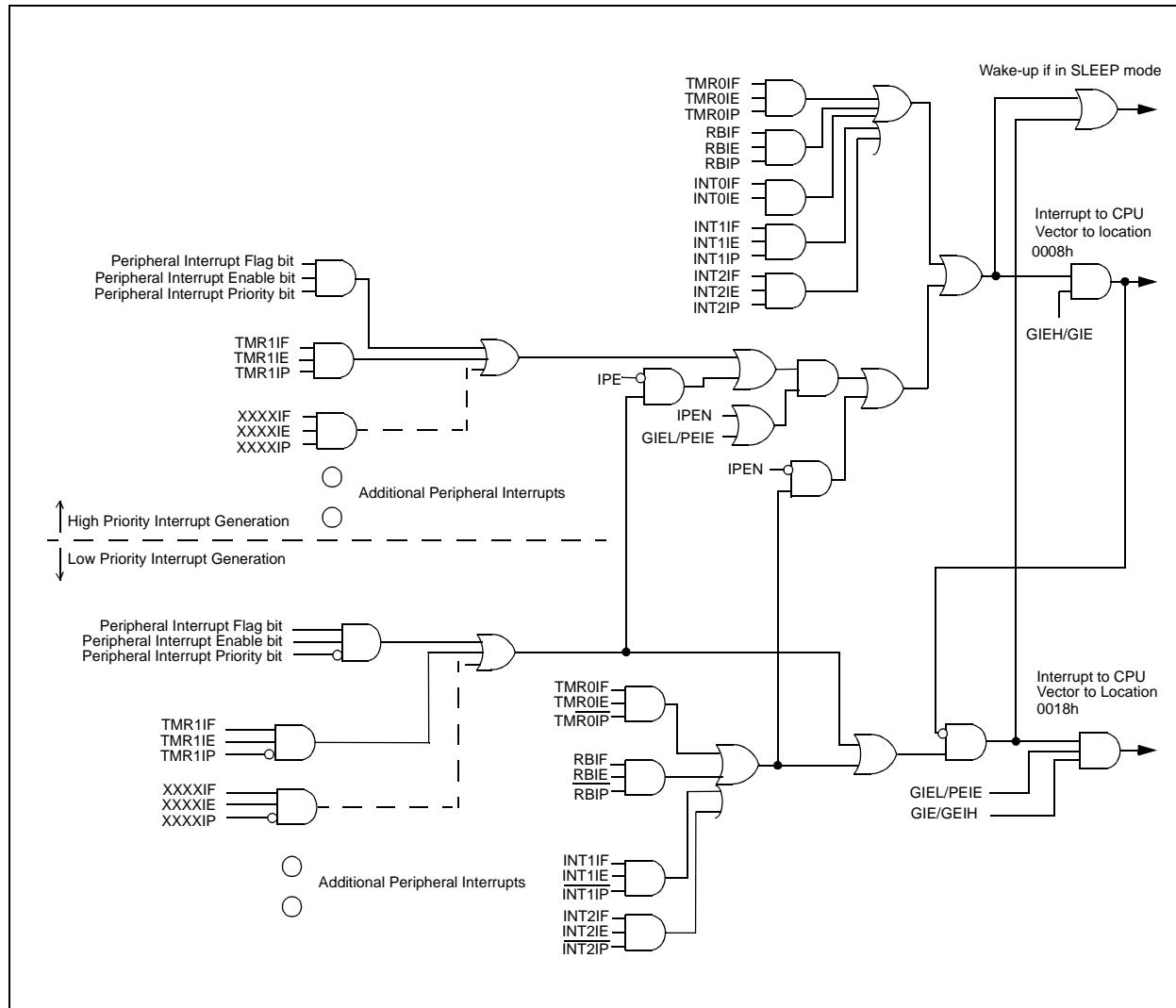
The return address is pushed onto the stack and the PC is loaded with the interrupt vector address (000008h or 000018h). Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bits must be cleared in software before re-enabling interrupts to avoid recursive interrupts.

The “return from interrupt” instruction, RETFIE, exits the interrupt routine and sets the GIE bit (GIEH or GIEL if priority levels are used), which re-enables interrupts.

For external interrupt events, such as the INT pins or the PORTB input change interrupt, the interrupt latency will be three to four instruction cycles. The exact latency is the same for one or two-cycle instructions. Individual interrupt flag bits are set, regardless of the status of their corresponding enable bit or the GIE bit.

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FIGURE 9-1: INTERRUPT LOGIC



9.1 INTCON Registers

The INTCON Registers are readable and writable registers, which contain various enable, priority and flag bits.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

REGISTER 9-1: INTCON REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-x
GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	
bit 7								bit 0

- | | |
|-------|--|
| bit 7 | GIE/GIEH: Global Interrupt Enable bit
<u>When IPEN (RCON<7>) = 0:</u>
1 = Enables all unmasked interrupts
0 = Disables all interrupts
<u>When IPEN (RCON<7>) = 1:</u>
1 = Enables all high priority interrupts
0 = Disables all interrupts |
| bit 6 | PEIE/GIEL: Peripheral Interrupt Enable bit
<u>When IPEN (RCON<7>) = 0:</u>
1 = Enables all unmasked peripheral interrupts
0 = Disables all peripheral interrupts
<u>When IPEN (RCON<7>) = 1:</u>
1 = Enables all low priority peripheral interrupts
0 = Disables all low priority peripheral interrupts |
| bit 5 | TMR0IE: TMR0 Overflow Interrupt Enable bit
1 = Enables the TMR0 overflow interrupt
0 = Disables the TMR0 overflow interrupt |
| bit 4 | INT0IE: INT0 External Interrupt Enable bit
1 = Enables the INT0 external interrupt
0 = Disables the INT0 external interrupt |
| bit 3 | RBIE: RB Port Change Interrupt Enable bit
1 = Enables the RB port change interrupt
0 = Disables the RB port change interrupt |
| bit 2 | TMR0IF: TMR0 Overflow Interrupt Flag bit
1 = TMR0 register has overflowed (must be cleared in software)
0 = TMR0 register did not overflow |
| bit 1 | INT0IF: INT0 External Interrupt Flag bit
1 = The INT0 external interrupt occurred (must be cleared in software)
0 = The INT0 external interrupt did not occur |
| bit 0 | RBIF: RB Port Change Interrupt Flag bit
1 = At least one of the RB7:RB4 pins changed state (must be cleared in software)
0 = None of the RB7:RB4 pins have changed state |

Note: A mismatch condition will continue to set this bit. Reading PORTB will end the mismatch condition and allow the bit to be cleared.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

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REGISTER 9-2: INTCON2 REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
RBPU	INTEDG0	INTEDG1	INTEDG2	INTEDG3	TMR0IP	INT3IP	RBIP

bit 7

bit 0

- bit 7 **RBPU:** PORTB Pull-up Enable bit
1 = All PORTB pull-ups are disabled
0 = PORTB pull-ups are enabled by individual port latch values
- bit 6 **INTEDG0:** External Interrupt0 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge
- bit 5 **INTEDG1:** External Interrupt1 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge
- bit 4 **INTEDG2:** External Interrupt2 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge
- bit 3 **INTEDG3:** External Interrupt3 Edge Select bit
1 = Interrupt on rising edge
0 = Interrupt on falling edge
- bit 2 **TMR0IP:** TMR0 Overflow Interrupt Priority bit
1 = High priority
0 = Low priority
- bit 1 **INT3IP:** INT3 External Interrupt Priority bit
1 = High priority
0 = Low priority
- bit 0 **RBIP:** RB Port Change Interrupt Priority bit
1 = High priority
0 = Low priority

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

REGISTER 9-3: INTCON3 REGISTER

R/W-1	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
INT2IP	INT1IP	INT3IE	INT2IE	INT1IE	INT3IF	INT2IF	INT1IF
bit 7							bit 0

- bit 7 **INT2IP:** INT2 External Interrupt Priority bit
 1 = High priority
 0 = Low priority
- bit 6 **INT1IP:** INT1 External Interrupt Priority bit
 1 = High priority
 0 = Low priority
- bit 5 **INT3IE:** INT3 External Interrupt Enable bit
 1 = Enables the INT3 external interrupt
 0 = Disables the INT3 external interrupt
- bit 4 **INT2IE:** INT2 External Interrupt Enable bit
 1 = Enables the INT2 external interrupt
 0 = Disables the INT2 external interrupt
- bit 3 **INT1IE:** INT1 External Interrupt Enable bit
 1 = Enables the INT1 external interrupt
 0 = Disables the INT1 external interrupt
- bit 2 **INT3IF:** INT3 External Interrupt Flag bit
 1 = The INT3 external interrupt occurred (must be cleared in software)
 0 = The INT3 external interrupt did not occur
- bit 1 **INT2IF:** INT2 External Interrupt Flag bit
 1 = The INT2 external interrupt occurred (must be cleared in software)
 0 = The INT2 external interrupt did not occur
- bit 0 **INT1IF:** INT1 External Interrupt Flag bit
 1 = The INT1 external interrupt occurred (must be cleared in software)
 0 = The INT1 external interrupt did not occur

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit. User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt. This feature allows for software polling.

9.2 PIR Registers

The PIR registers contain the individual flag bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are three Peripheral Interrupt Flag Registers (PIR1, PIR2 and PIR3).

Note 1: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>).

2: User software should ensure the appropriate interrupt flag bits are cleared prior to enabling an interrupt, and after servicing that interrupt.

REGISTER 9-4: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 1 (PIR1)

R/W-0	R/W-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIF ⁽¹⁾	ADIF	RC1IF	TX1IF	SSPIF	CCP1IF	TMR2IF	TMR1IF
bit 7							bit 0

- bit 7 **PSPIF:** Parallel Slave Port Read/Write Interrupt Flag bit⁽¹⁾
 1 = A read or a write operation has taken place (must be cleared in software)
 0 = No read or write has occurred
- bit 6 **ADIF:** A/D Converter Interrupt Flag bit
 1 = An A/D conversion completed (must be cleared in software)
 0 = The A/D conversion is not complete
- bit 5 **RC1IF:** USART1 Receive Interrupt Flag bit
 1 = The USART1 receive buffer, RCREG, is full (cleared when RCREG is read)
 0 = The USART1 receive buffer is empty
- bit 4 **TX1IF:** USART Transmit Interrupt Flag bit
 1 = The USART1 transmit buffer, TXREG, is empty (cleared when TXREG is written)
 0 = The USART1 transmit buffer is full
- bit 3 **SSPIF:** Master Synchronous Serial Port Interrupt Flag bit
 1 = The transmission/reception is complete (must be cleared in software)
 0 = Waiting to transmit/receive
- bit 2 **CCP1IF:** CCP1 Interrupt Flag bit
Capture mode:
 1 = A TMR1 register capture occurred (must be cleared in software)
 0 = No TMR1 register capture occurred
Compare mode:
 1 = A TMR1 register compare match occurred (must be cleared in software)
 0 = No TMR1 register compare match occurred
PWM mode:
 Unused in this mode
- bit 1 **TMR2IF:** TMR2 to PR2 Match Interrupt Flag bit
 1 = TMR2 to PR2 match occurred (must be cleared in software)
 0 = No TMR2 to PR2 match occurred
- bit 0 **TMR1IF:** TMR1 Overflow Interrupt Flag bit
 1 = TMR1 register overflowed (must be cleared in software)
 0 = TMR1 register did not overflow

Note 1: Enabled only in Microcontroller mode for PIC18F8X20 devices.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared

REGISTER 9-5: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 2 (PIR2)

U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CMIF	—	EEIF	BCLIF	LVDIF	TMR3IF	CCP2IF

bit 7

bit 0

- bit 7 **Unimplemented:** Read as '0'
- bit 6 **CMIF:** Comparator Interrupt Flag bit
 1 = The comparator input has changed (must be cleared in software)
 0 = The comparator input has not changed
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **EEIF:** Data EEPROM/FLASH Write Operation Interrupt Flag bit
 1 = The write operation is complete (must be cleared in software)
 0 = The write operation is not complete, or has not been started
- bit 3 **BCLIF:** Bus Collision Interrupt Flag bit
 1 = A bus collision occurred while the SSP module (configured in I²C Master mode)
 was transmitting (must be cleared in software)
 0 = No bus collision occurred
- bit 2 **LVDIF:** Low Voltage Detect Interrupt Flag bit
 1 = A low voltage condition occurred (must be cleared in software)
 0 = The device voltage is above the Low Voltage Detect trip point
- bit 1 **TMR3IF:** TMR3 Overflow Interrupt Flag bit
 1 = TMR3 register overflowed (must be cleared in software)
 0 = TMR3 register did not overflow
- bit 0 **CCP2IF:** CCP2 Interrupt Flag bit
Capture mode:
 1 = A TMR1 or TMR3 register capture occurred (must be cleared in software)
 0 = No TMR1 or TMR3 register capture occurred
Compare mode:
 1 = A TMR1 or TMR3 register compare match occurred (must be cleared in software)
 0 = No TMR1 or TMR3 register compare match occurred
PWM mode:
 Unused in this mode

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

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REGISTER 9-6: PERIPHERAL INTERRUPT REQUEST (FLAG) REGISTER 3 (PIR3)

U-0	U-0	R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF

bit 7- 6	Unimplemented: Read as '0'
bit 5	RC2IF: USART2 Receive Interrupt Flag bit 1 = The USART2 receive buffer, RCREG, is full (cleared when RCREG is read) 0 = The USART2 receive buffer is empty
bit 4	TX2IF: USART2 Transmit Interrupt Flag bit 1 = The USART2 transmit buffer, TXREG, is empty (cleared when TXREG is written) 0 = The USART2 transmit buffer is full
bit 3	TMR4IF: TMR3 Overflow Interrupt Flag bit 1 = TMR4 register overflowed (must be cleared in software) 0 = TMR4 register did not overflow
bit 2-0	CCP2IF: CCPx Interrupt Flag bit (CCP Modules 3,4 and 5) <u>Capture mode:</u> 1 = A TMR1 or TMR3 register capture occurred (must be cleared in software) 0 = No TMR1 or TMR3 register capture occurred <u>Compare mode:</u> 1 = A TMR1 or TMR3 register compare match occurred (must be cleared in software) 0 = No TMR1 or TMR3 register compare match occurred <u>PWM mode:</u> Unused in this mode

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

9.3 PIE Registers

The PIE registers contain the individual enable bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are three Peripheral Interrupt Enable Registers (PIE1, PIE2 and PIE3). When the IPEN bit (RCON<7>) is '0', the PEIE bit must be set to enable any of these peripheral interrupts.

REGISTER 9-7: PERIPHERAL INTERRUPT ENABLE REGISTER 1 (PIE1)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
PSPIE ⁽¹⁾	ADIE	RC1IE	TX1IE	SSPIE	CCP1IE	TMR2IE	TMR1IE

bit 7

bit 0

bit 7 **PSPIE:** Parallel Slave Port Read/Write Interrupt Enable bit⁽¹⁾

1 = Enables the PSP read/write interrupt
0 = Disables the PSP read/write interrupt

bit 6 **ADIE:** A/D Converter Interrupt Enable bit

1 = Enables the A/D interrupt
0 = Disables the A/D interrupt

bit 5 **RC1IE:** USART1 Receive Interrupt Enable bit

1 = Enables the USART1 receive interrupt
0 = Disables the USART1 receive interrupt

bit 4 **TX1IE:** USART1 Transmit Interrupt Enable bit

1 = Enables the USART1 transmit interrupt
0 = Disables the USART1 transmit interrupt

bit 3 **SSPIE:** Master Synchronous Serial Port Interrupt Enable bit

1 = Enables the MSSP interrupt
0 = Disables the MSSP interrupt

bit 2 **CCP1IE:** CCP1 Interrupt Enable bit

1 = Enables the CCP1 interrupt
0 = Disables the CCP1 interrupt

bit 1 **TMR2IE:** TMR2 to PR2 Match Interrupt Enable bit

1 = Enables the TMR2 to PR2 match interrupt
0 = Disables the TMR2 to PR2 match interrupt

bit 0 **TMR1IE:** TMR1 Overflow Interrupt Enable bit

1 = Enables the TMR1 overflow interrupt
0 = Disables the TMR1 overflow interrupt

Note 1: Enabled only in Microcontroller mode for PIC18F8X20 devices.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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REGISTER 9-8: PERIPHERAL INTERRUPT ENABLE REGISTER 2 (PIE2)

U-0	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	CMIE	—	EEIE	BCLIE	LVDIE	TMR3IE	CCP2IE

bit 7

bit 0

- bit 7 **Unimplemented:** Read as '0'
- bit 6 **CMIE:** Comparator Interrupt Enable bit
1 = Enables the comparator interrupt
0 = Disables the comparator interrupt
- bit 5 **Unimplemented:** Read as '0'
- bit 4 **EEIE:** Data EEPROM/FLASH Write Operation Interrupt Enable bit
1 = Enables the write operation interrupt
0 = Disables the write operation interrupt
- bit 3 **BCLIE:** Bus Collision Interrupt Enable bit
1 = Enables the bus collision interrupt
0 = Disables the bus collision interrupt
- bit 2 **LVDIE:** Low Voltage Detect Interrupt Enable bit
1 = Enables the Low Voltage Detect interrupt
0 = Disables the Low Voltage Detect interrupt
- bit 1 **TMR3IE:** TMR3 Overflow Interrupt Enable bit
1 = Enables the TMR3 overflow interrupt
0 = Disables the TMR3 overflow interrupt
- bit 0 **CCP2IE:** CCP2 Interrupt Enable bit
1 = Enables the CCP2 interrupt
0 = Disables the CCP2 interrupt

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared x = Bit is unknown

REGISTER 9-9: PERIPHERAL INTERRUPT ENABLE REGISTER 3 (PIE3)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE
bit 7				bit 0			

- | | |
|---------|--|
| bit 7-6 | Unimplemented: Read as '0' |
| bit 5 | RC2IE: USART2 Receive Interrupt Enable bit
1 = Enables the USART2 receive interrupt
0 = Disables the USART2 receive interrupt |
| bit 4 | TX2IE: USART2 Transmit Interrupt Enable bit
1 = Enables the USART2 transmit interrupt
0 = Disables the USART2 transmit interrupt |
| bit 3 | TMR4IE: TMR4 to PR4 Match Interrupt Enable bit
1 = Enables the TMR4 to PR4 match interrupt
0 = Disables the TMR4 to PR4 match interrupt |
| bit 2-0 | CCPxIE: CCPx Interrupt Enable bit (CCP Modules 3, 4 and 5)
1 = Enables the CCPx interrupt
0 = Disables the CCPx interrupt |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

9.4 IPR Registers

The IPR registers contain the individual priority bits for the peripheral interrupts. Due to the number of peripheral interrupt sources, there are three Peripheral Interrupt Priority Registers (IPR1, IPR2 and IPR3). The operation of the priority bits requires that the Interrupt Priority Enable (IPEN) bit be set.

REGISTER 9-10: PERIPHERAL INTERRUPT PRIORITY REGISTER 1 (IPR1)

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
PSPIP ⁽¹⁾	ADIP	RC1IP	TX1IP	SSPIP	CCP1IP	TMR2IP	TMR1IP
bit 7						bit 0	

- | | |
|-------|---|
| bit 7 | PSPIP: Parallel Slave Port Read/Write Interrupt Priority bit ⁽¹⁾
1 = High priority
0 = Low priority |
| bit 6 | ADIP: A/D Converter Interrupt Priority bit
1 = High priority
0 = Low priority |
| bit 5 | RC1IP: USART1 Receive Interrupt Priority bit
1 = High priority
0 = Low priority |
| bit 4 | TX1IP: USART1 Transmit Interrupt Priority bit
1 = High priority
0 = Low priority |
| bit 3 | SSPIP: Master Synchronous Serial Port Interrupt Priority bit
1 = High priority
0 = Low priority |
| bit 2 | CCP1IP: CCP1 Interrupt Priority bit
1 = High priority
0 = Low priority |
| bit 1 | TMR2IP: TMR2 to PR2 Match Interrupt Priority bit
1 = High priority
0 = Low priority |
| bit 0 | TMR1IP: TMR1 Overflow Interrupt Priority bit
1 = High priority
0 = Low priority |

Note 1: Enabled only in Microcontroller mode for PIC18F8X20 devices.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 9-11: PERIPHERAL INTERRUPT PRIORITY REGISTER 2 (IPR2)

U-0	R/W-1	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	CMIP	—	EEIP	BCLIP	LVDIP	TMR3IP	CCP2IP

- | | |
|-------|--|
| bit 7 | Unimplemented: Read as '0' |
| bit 6 | CMIP: Comparator Interrupt Priority bit
1 = High priority
0 = Low priority |
| bit 5 | Unimplemented: Read as '0' |
| bit 4 | EEIP: Data EEPROM/FLASH Write Operation Interrupt Priority bit
1 = High priority
0 = Low priority |
| bit 3 | BCLIP: Bus Collision Interrupt Priority bit
1 = High priority
0 = Low priority |
| bit 2 | LVDIP: Low Voltage Detect Interrupt Priority bit
1 = High priority
0 = Low priority |
| bit 1 | TMR3IP: TMR3 Overflow Interrupt Priority bit
1 = High priority
0 = Low priority |
| bit 0 | CCP2IP: CCP2 Interrupt Priority bit
1 = High priority
0 = Low priority |

Legend:

R = Readable bit

- n = Value at POR

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' = Bit is cleared

$x = \text{Bit is unknown}$

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REGISTER 9-12: PERIPHERAL INTERRUPT PRIORITY REGISTER 3 (IPR3)

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP

- | | |
|---------|--|
| bit 7-6 | Unimplemented: Read as '0' |
| bit 5 | RC2IP: USART2 Receive Interrupt Priority bit
1 = High priority
0 = Low priority |
| bit 4 | TX2IP: USART2 Transmit Interrupt Priority bit
1 = High priority
0 = Low priority |
| bit 3 | TMR4IP: TMR4 to PR4 Match Interrupt Priority bit
1 = High priority
0 = Low priority |
| bit 2 | CCPxIP: CCPx Interrupt Priority bit (CCP Modules 3, 4 and 5)
1 = High priority
0 = Low priority |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

9.5 RCON Register

The RCON register contains the IPEN bit, which is used to enable prioritized interrupts. The functions of the other bits in this register are discussed in more detail in Section 4.14.

REGISTER 9-13: RCON REGISTER

R/W-0	U-0	U-0	R/W-1	R-1	R-1	R/W-0	R/W-0
IPEN	—	—	RI	TO	PD	POR	BOR

bit 7

bit 0

- bit 7 **IPEN:** Interrupt Priority Enable bit
 1 = Enable priority levels on interrupts
 0 = Disable priority levels on interrupts (PIC16 compatibility mode)
- bit 6-5 **Unimplemented:** Read as '0'
- bit 4 **RI:** RESET Instruction Flag bit
 For details of bit operation, see Register 4-4
- bit 3 **TO:** Watchdog Time-out Flag bit
 For details of bit operation, see Register 4-4
- bit 2 **PD:** Power-down Detection Flag bit
 For details of bit operation, see Register 4-4
- bit 1 **POR:** Power-on Reset Status bit
 For details of bit operation, see Register 4-4
- bit 0 **BOR:** Brown-out Reset Status bit
 For details of bit operation, see Register 4-4

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

9.6 INT0 Interrupt

External interrupts on the RB0/INT0, RB1/INT1, RB2/INT2 and RB3/INT3 pins are edge-triggered: either rising, if the corresponding INTEDG_x bit is set in the INTCON2 register, or falling, if the INTEDG_x bit is clear. When a valid edge appears on the RB_x/INT_x pin, the corresponding flag bit, INTxF is set. This interrupt can be disabled by clearing the corresponding enable bit, INTxE. Flag bit, INTxF, must be cleared in software in the Interrupt Service Routine before re-enabling the interrupt. All external interrupts (INT0, INT1, INT2 and INT3) can wake-up the processor from SLEEP, if bit INTxIE was set prior to going into SLEEP. If the global interrupt enable bit GIE is set, the processor will branch to the interrupt vector following wake-up.

The interrupt priority for INT, INT2 and INT3 is determined by the value contained in the interrupt priority bits: INT1IP (INTCON3<6>), INT2IP (INTCON3<7>) and INT3IP (INTCON2<1>). There is no priority bit associated with INT0; it is always a high priority interrupt source.

9.7 TMR0 Interrupt

In 8-bit mode (which is the default), an overflow in the TMR0 register (FFh → 00h) will set flag bit TMR0IF. In 16-bit mode, an overflow in the TMR0H:TMR0L registers (FFFFh → 0000h) will set flag bit TMR0IF. The interrupt can be enabled/disabled by setting/clearing enable bit, TMR0IE (INTCON<5>). Interrupt priority for Timer0 is determined by the value contained in the interrupt priority bit, TMR0IP (INTCON2<2>). See Section 8.0 for further details on the Timer0 module.

9.8 PORTB Interrupt-on-Change

An input change on PORTB<7:4> sets flag bit RBIF (INTCON<0>). The interrupt can be enabled/disabled by setting/clearing enable bit, RBIE (INTCON<3>). Interrupt priority for PORTB interrupt-on-change is determined by the value contained in the interrupt priority bit, RBIP (INTCON2<0>).

9.9 Context Saving During Interrupts

During an interrupt, the return PC value is saved on the stack. Additionally, the WREG, STATUS and BSR registers are saved on the fast return stack. If a fast return from interrupt is not used (See Section 4.3), the user may need to save the WREG, STATUS and BSR registers in software. Depending on the user's application, other registers may also need to be saved. Example 6-1 saves and restores the WREG, STATUS and BSR registers during an Interrupt Service Routine.

EXAMPLE 9-1: SAVING STATUS, WREG AND BSR REGISTERS IN RAM

```
MOVWF  W_TEMP          ; W_TEMP is in virtual bank
MOVFF  STATUS, STATUS_TEMP   ; STATUS_TEMP located anywhere
MOVFF  BSR,    BSR_TEMP     ; BSR located anywhere
;
; USER ISR CODE
;
MOVFF  BSR_TEMP, BSR      ; Restore BSR
MOVF   W_TEMP,   W          ; Restore WREG
MOVFF  STATUS_TEMP, STATUS ; Restore STATUS
```

10.0 I/O PORTS

Depending on the device selected, there are either seven or nine I/O ports available on PIC18FXX20 devices. Some of their pins are multiplexed with one or more alternate functions from the other peripheral features on the device. In general, when a peripheral is enabled, that pin may not be used as a general purpose I/O pin.

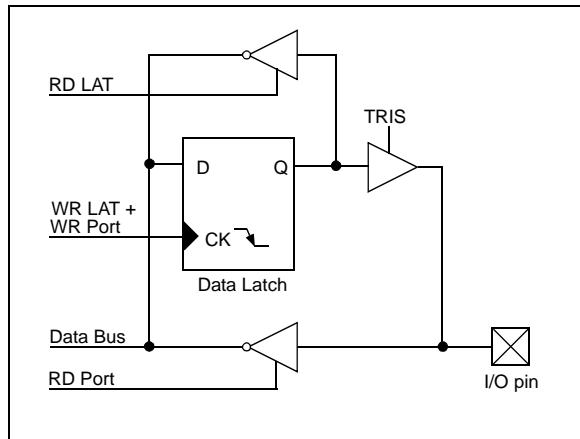
Each port has three registers for its operation. These registers are:

- TRIS register (data direction register)
- PORT register (reads the levels on the pins of the device)
- LAT register (output latch)

The data latch (LAT register) is useful for read-modify-write operations on the value that the I/O pins are driving.

A simplified version of a generic I/O port and its operation is shown in Figure 10-1.

FIGURE 10-1: SIMPLIFIED BLOCK DIAGRAM OF PORT/LAT/TRIS OPERATION



10.1 PORTA, TRISA and LATA Registers

PORTA is a 7-bit wide, bi-directional port. The corresponding Data Direction register is TRISA. Setting a TRISA bit (= '1') will make the corresponding PORTA pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISA bit (= '0') will make the corresponding PORTA pin an output (i.e., put the contents of the output latch on the selected pin).

Reading the PORTA register reads the status of the pins, whereas writing to it will write to the port latch.

The Data Latch register (LATA) is also memory mapped. Read-modify-write operations on the LATA register, read and write the latched output value for PORTA.

The RA4 pin is multiplexed with the Timer0 module clock input to become the RA4/T0CKI pin. The RA4/T0CKI pin is a Schmitt Trigger input and an open drain output. All other RA port pins have TTL input levels and full CMOS output drivers.

The RA6 pin is only enabled as a general I/O pin in ECIO and RCIO oscillator modes.

The other PORTA pins are multiplexed with analog inputs and the analog VREF+ and VREF- inputs. The operation of each pin is selected by clearing/setting the control bits in the ADCON1 register (A/D Control Register1).

Note: On a Power-on Reset, RA5 and RA3:RA0 are configured as analog inputs and read as '0'. RA6 and RA4 are configured as digital inputs.

The TRISA register controls the direction of the RA pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISA register are maintained set when using them as analog inputs.

EXAMPLE 10-1: INITIALIZING PORTA

```

CLRF PORTA      ; Initialize PORTA by
; clearing output
; data latches
CLRF LATA       ; Alternate method
; to clear output
; data latches
MOVLW 0x0F      ; Configure A/D
MOVWF ADCON1    ; for digital inputs
MOVLW 0xCF      ; Value used to
; initialize data
; direction
MOVWF TRISA     ; Set RA<3:0> as inputs
; RA<5:4> as outputs

```

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FIGURE 10-2: BLOCK DIAGRAM OF RA3:RA0 AND RA5 PINS

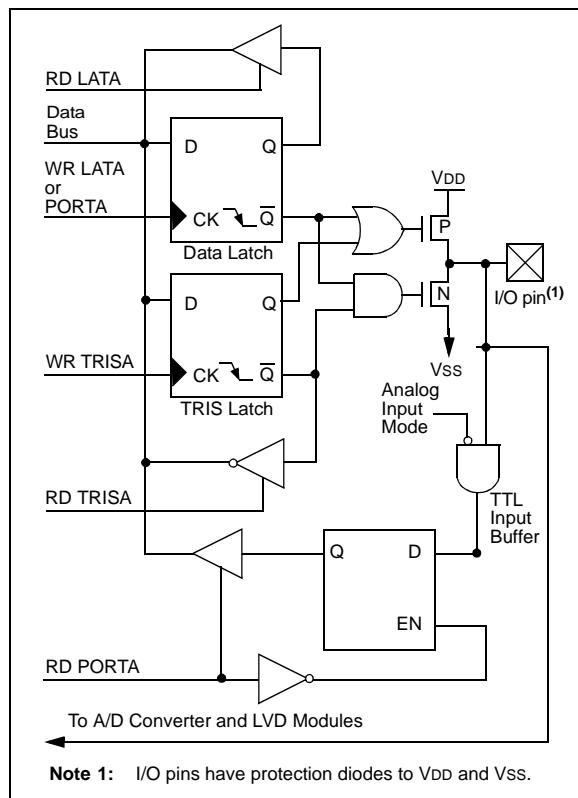


FIGURE 10-3: BLOCK DIAGRAM OF RA4/T0CKI PIN

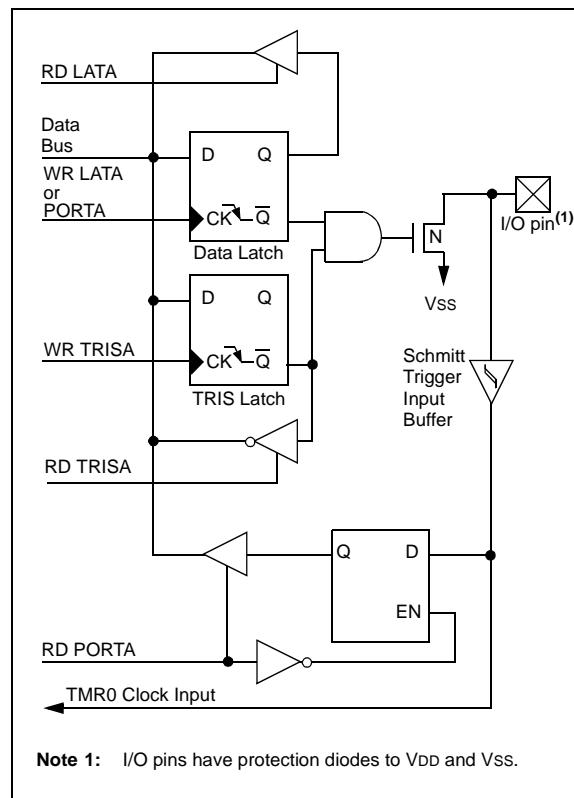


FIGURE 10-4: BLOCK DIAGRAM OF RA6 (WHEN ENABLED AS I/O)

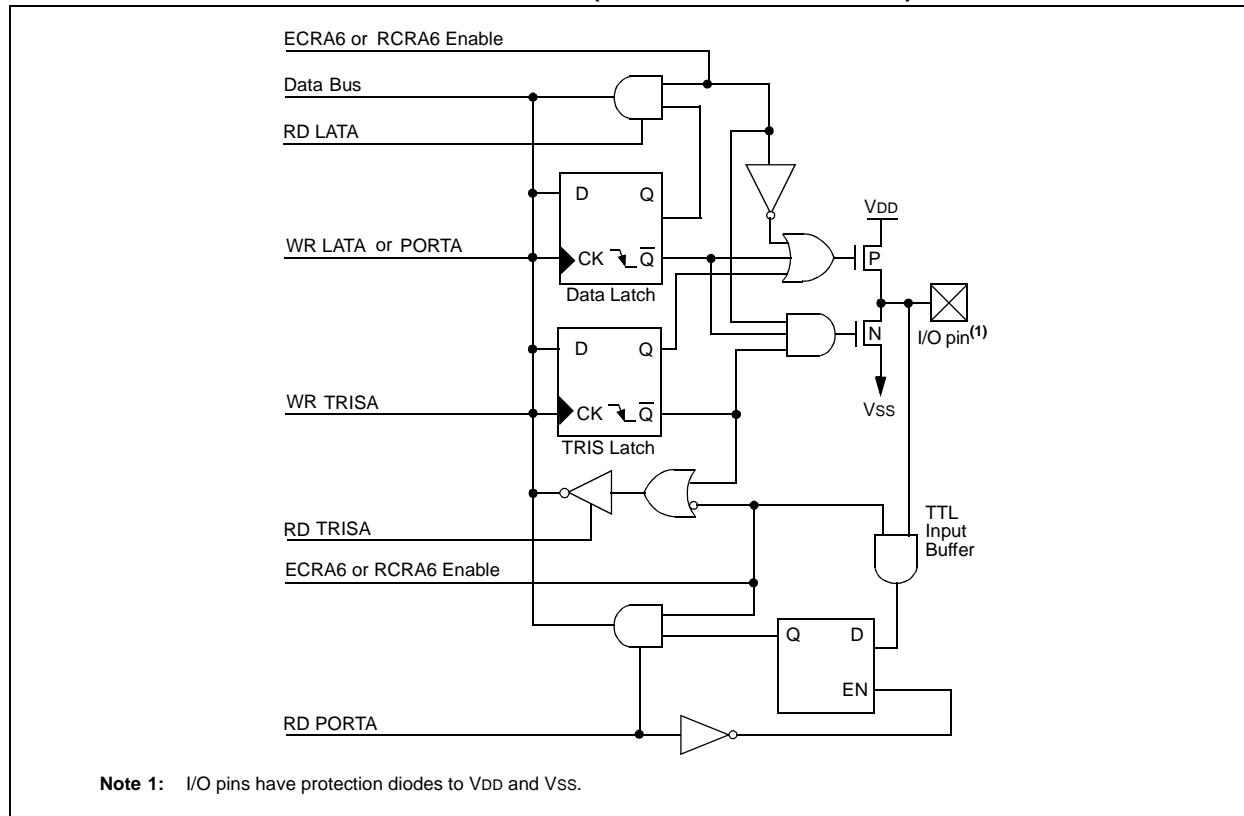


TABLE 10-1: PORTA FUNCTIONS

Name	Bit#	Buffer	Function
RA0/AN0	bit0	TTL	Input/output or analog input.
RA1/AN1	bit1	TTL	Input/output or analog input.
RA2/AN2/VREF-	bit2	TTL	Input/output or analog input or VREF-.
RA3/AN3/VREF+	bit3	TTL	Input/output or analog input or VREF+.
RA4/T0CKI	bit4	ST	Input/output or external clock input for Timer0. Output is open drain type.
RA5/AN4/LVDIN	bit5	TTL	Input/output or slave select input for synchronous serial port or analog input, or low voltage detect input.
OSC2/CLKO/RA6	bit6	TTL	OSC2 or clock output, or I/O pin.

Legend: TTL = TTL input, ST = Schmitt Trigger input

TABLE 10-2: SUMMARY OF REGISTERS ASSOCIATED WITH PORTA

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
PORTA	—	RA6	RA5	RA4	RA3	RA2	RA1	RA0	-x0x 0000	-u0u 0000
LATA	—	LATA Data Output Register							-xxx xxxx	-uuu uuuu
TRISA	—	PORTA Data Direction Register							-111 1111	-111 1111
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'.

Shaded cells are not used by PORTA.

10.2 PORTB, TRISB and LATB Registers

PORTE is an 8-bit wide, bi-directional port. The corresponding Data Direction register is TRISE. Setting a TRISE bit (= '1') will make the corresponding PORTE pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISE bit (= '0') will make the corresponding PORTE pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATB) is also memory mapped. Read-modify-write operations on the LATB register, read and write the latched output value for PORTB.

EXAMPLE 10-2: INITIALIZING PORTB

```
CLRFB PORTB ; Initialize PORTB by
               ; clearing output
               ; data latches
CLRF LATB   ; Alternate method
               ; to clear output
               ; data latches
MOVLW 0xCF  ; Value used to
               ; initialize data
               ; direction
MOVWF TRISB ; Set RB<3:0> as inputs
               ; RB<5:4> as outputs
               ; RB<7:6> as inputs
```

Each of the PORTB pins has a weak internal pull-up. A single control bit can turn on all the pull-ups. This is performed by clearing bit RBPU (INTCON2<7>). The weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset.

Note: On a Power-on Reset, these pins are configured as digital inputs.

Four of the PORTB pins (RB3:RB0) are the external interrupt pins, INT3 through INT0. In order to use these pins as external interrupts, the corresponding TRISB bit must be set to '1'.

The other four PORTB pins (RB7:RB4) have an interrupt-on-change feature. Only pins configured as inputs can cause this interrupt to occur (i.e., any RB7:RB4 pin configured as an output is excluded from the interrupt-on-change comparison). The input pins (of RB7:RB4) are compared with the old value latched on the last read of PORTB. The “mismatch” outputs of RB7:RB4 are OR’ed together to generate the RB Port Change Interrupt with flag bit, RBIF (INTCON<0>).

This interrupt can wake the device from SLEEP. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- a) Any read or write of PORTB (except with the MOVFF instruction). This will end the mismatch condition.
 - b) Clear flag bit RBIF.

A mismatch condition will continue to set flag bit, RBIF. Reading PORTB will end the mismatch condition and allow flag bit RBIF to be cleared.

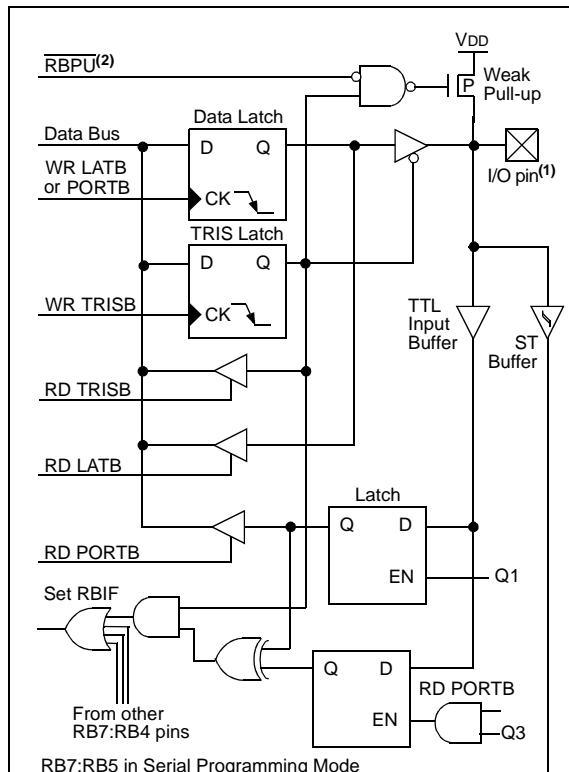
The interrupt-on-change feature is recommended for wake-up on key depression operation and operations where PORTB is only used for the interrupt-on-change feature. Polling of PORTB is not recommended while using the interrupt-on-change feature.

For PIC18F8X20 devices, RB3 can be configured by the configuration bit CCP2MX, as the alternate peripheral pin for the CCP2 module. This is only available when the device is configured in Microprocessor, Microprocessor with Boot Block, or Extended Microcontroller operating modes.

The RB5 pin is used as the LVP programming pin. When the LVP configuration bit is programmed, this pin loses the I/O function and become a programming test function.

Note: When LVP is enabled, the weak pull-up on RB5 is disabled.

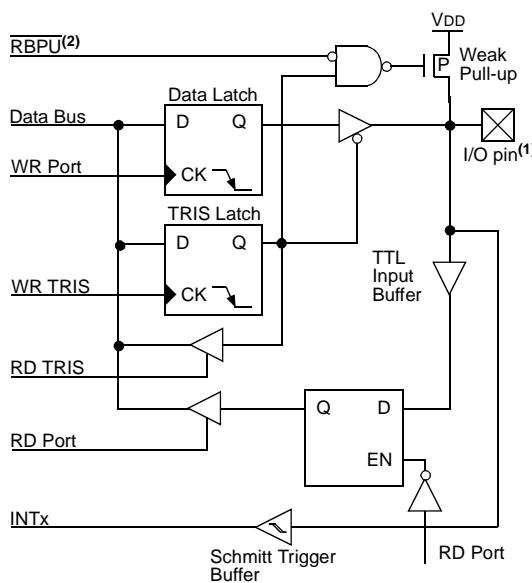
FIGURE 10-5: BLOCK DIAGRAM OF RB7:RB4 PINS



Note 1: I/O pins have diode protection to VDD and Vss.

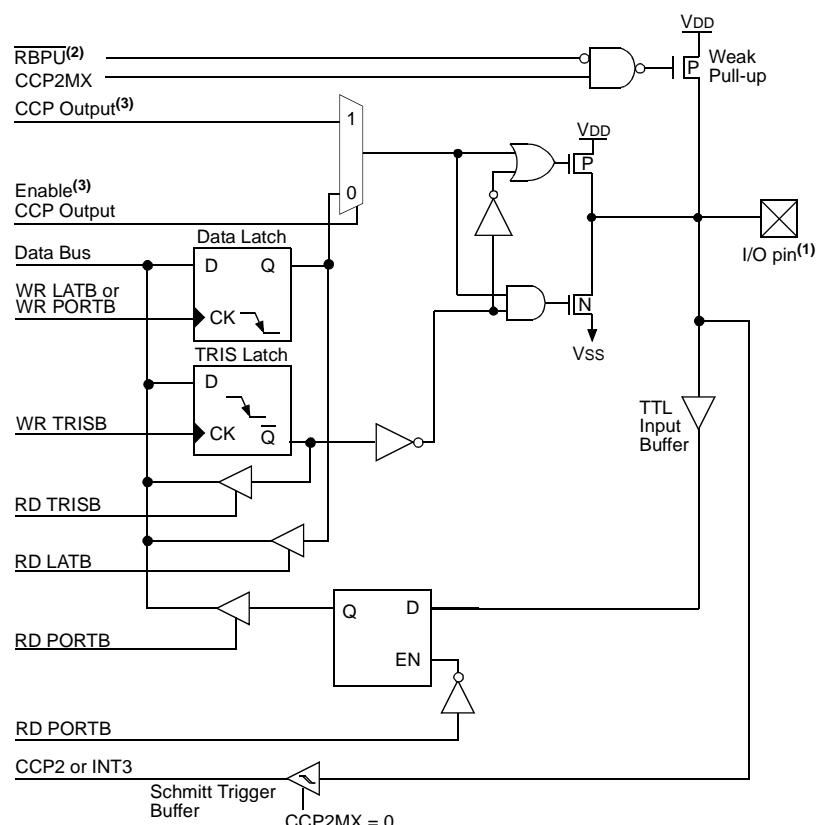
2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBPU bit (INTCON2<7>).

FIGURE 10-6: BLOCK DIAGRAM OF RB2:RB0 PINS



Note 1: I/O pins have diode protection to VDD and Vss.
2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBP_U bit (OPTION_REG<7>).

FIGURE 10-7: BLOCK DIAGRAM OF RB3



Note 1: I/O pin has diode protection to VDD and Vss.
2: To enable weak pull-ups, set the appropriate TRIS bit(s) and clear the RBP_U bit (INTCON2<7>).
3: For PIC18F8X20 parts, the CCP2 input/output is multiplexed with RB3 if the CCP2MX bit is enabled (= '0') in the configuration register and the device is operating in Microprocessor, Microprocessor with Boot Block or Extended Microcontroller mode.

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TABLE 10-3: PORTB FUNCTIONS

Name	Bit#	Buffer	Function
RB0/INT0	bit0	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input0. Internal software programmable weak pull-up.
RB1/INT1	bit1	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input1. Internal software programmable weak pull-up.
RB2/INT2	bit2	TTL/ST ⁽¹⁾	Input/output pin or external interrupt input2. Internal software programmable weak pull-up.
RB3/CCP2 ⁽³⁾ /INT3	bit3	TTL/ST ⁽⁴⁾	Input/output pin, or external interrupt input3. Capture2 input/Compare2 output/PWM output (when CCP2MX configuration bit is enabled, all PIC18F8X20 operating modes except Microcontroller mode). Internal software programmable weak pull-up.
RB4/KBI0	bit4	TTL	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up.
RB5/KBI1/PGM	bit5	TTL/ST ⁽²⁾	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Low voltage ICSP enable pin.
RB6/KBI2/PGC	bit6	TTL/ST ⁽²⁾	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming clock.
RB7/KBI3/PGD	bit7	TTL/ST ⁽²⁾	Input/output pin (with interrupt-on-change). Internal software programmable weak pull-up. Serial programming data.

Legend: TTL = TTL input, ST = Schmitt Trigger input

Note 1: This buffer is a Schmitt Trigger input when configured as the external interrupt.

2: This buffer is a Schmitt Trigger input when used in Serial Programming mode.

3: RC1 is the alternate assignment for CCP2 when CCP2MX is not set (all operating modes except Microcontroller mode).

4: This buffer is a Schmitt Trigger input when configured as the CCP2 input.

TABLE 10-4: SUMMARY OF REGISTERS ASSOCIATED WITH PORTB

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
PORTB	RB7	RB6	RB5	RB4	RB3	RB2	RB1	RB0	xxxx xxxx	uuuu uuuu
LATB	LATB Data Output Register								xxxx xxxx	uuuu uuuu
TRISB	PORTB Data Direction Register								1111 1111	1111 1111
INTCON	GIE/ GIEH	PEIE/ GIEL	TMROIE	INT0IE	RBIE	TMROIF	INT0IF	RBIF	0000 0000	0000 0000
INTCON2	RBPU	INTEDG0	INTEDG1	INTEDG2	INTEDG3	TMROIP	INT3IP	RBIP	1111 1111	1111 1111
INTCON3	INT2IP	INT1IP	INT3IE	INT2IE	INT1IE	INT3IF	INT2IF	INT1IF	1100 0000	1100 0000

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTB.

10.3 PORTC, TRISC and LATC Registers

PORTC is an 8-bit wide, bi-directional port. The corresponding Data Direction register is TRISC. Setting a TRISC bit (= '1') will make the corresponding PORTC pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISC bit (= '0') will make the corresponding PORTC pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATC) is also memory mapped. Read-modify-write operations on the LATC register, read and write the latched output value for PORTC.

PORTC is multiplexed with several peripheral functions (Table 10-5). PORTC pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTC pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

Note: On a Power-on Reset, these pins are configured as digital inputs.

The pin override value is not loaded into the TRIS register. This allows read-modify-write of the TRIS register, without concern due to peripheral overrides.

RC1 is normally configured by configuration bit, CCP2MX, as the default peripheral pin of the CCP2 module (default/erased state, CCP2MX = '1').

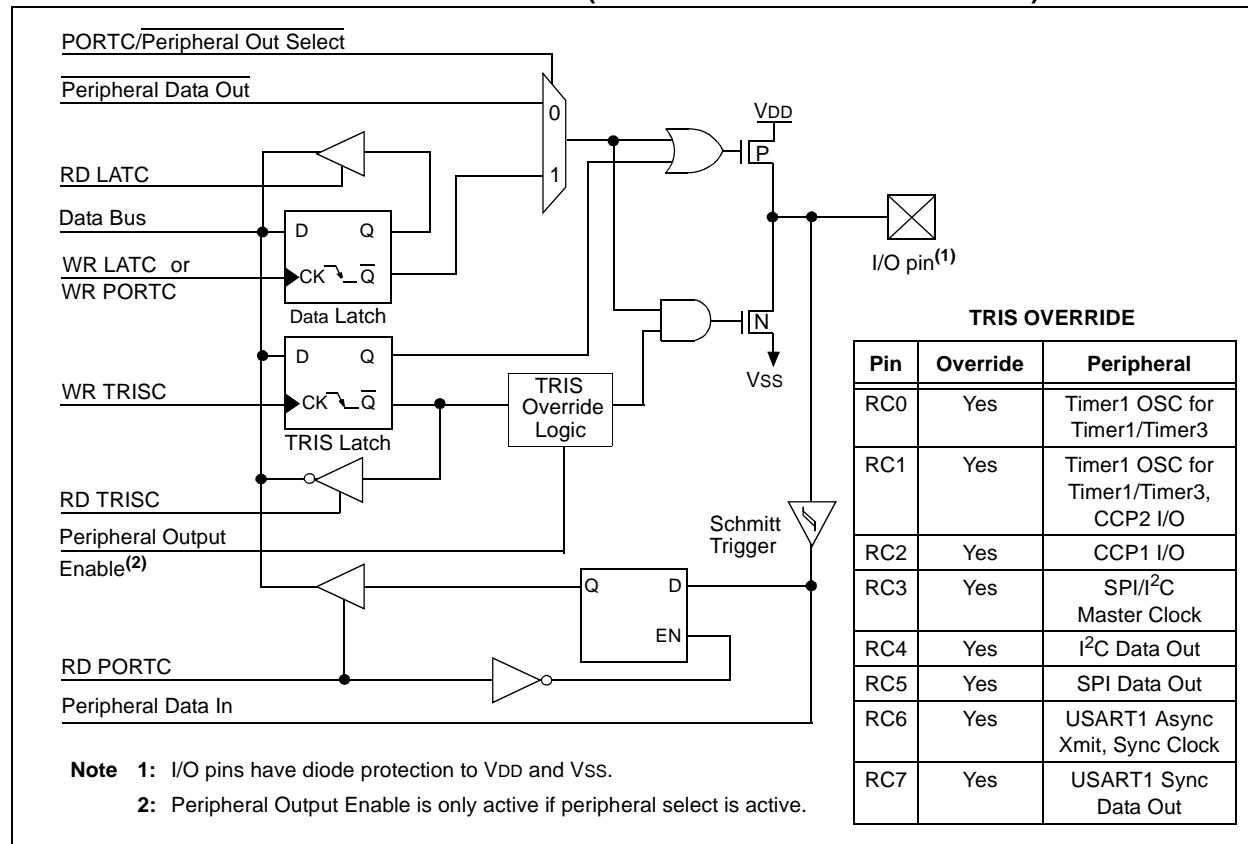
EXAMPLE 10-3: INITIALIZING PORTC

```

CLRF  PORTC    ; Initialize PORTC by
                ; clearing output
                ; data latches
CLRF  LATC     ; Alternate method
                ; to clear output
                ; data latches
MOVLW 0xCF    ; Value used to
                ; initialize data
                ; direction
MOVWF TRISC   ; Set RC<3:0> as inputs
                ; RC<5:4> as outputs
                ; RC<7:6> as inputs

```

FIGURE 10-8: PORTC BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE)



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TABLE 10-5: PORTC FUNCTIONS

Name	Bit#	Buffer Type	Function
RC0/T1OSO/T13CKI	bit0	ST	Input/output port pin, Timer1 oscillator output, or Timer1/Timer3 clock input.
RC1/T1OSI/CCP2 ⁽¹⁾	bit1	ST	Input/output port pin, Timer1 oscillator input, or Capture2 input/ Compare2 output/PWM output (when CCP2MX configuration bit is disabled).
RC2/CCP1	bit2	ST	Input/output port pin or Capture1 input/Compare1 output/PWM1 output.
RC3/SCK/SCL	bit3	ST	RC3 can also be the synchronous serial clock for both SPI and I ² C modes.
RC4/SDI/SDA	bit4	ST	RC4 can also be the SPI Data In (SPI mode) or Data I/O (I ² C mode).
RC5/SDO	bit5	ST	Input/output port pin or Synchronous Serial Port data output.
RC6/TX1/CK1	bit6	ST	Input/output port pin, Addressable USART1 Asynchronous Transmit, or Addressable USART1 Synchronous Clock.
RC7/RX1/DT1	bit7	ST	Input/output port pin, Addressable USART1 Asynchronous Receive, or Addressable USART1 Synchronous Data.

Legend: ST = Schmitt Trigger input

Note 1: RB3 is the alternate assignment for CCP2 when CCP2MX is set.

TABLE 10-6: SUMMARY OF REGISTERS ASSOCIATED WITH PORTC

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
PORTC	RC7	RC6	RC5	RC4	RC3	RC2	RC1	RC0	xxxx xxxx	uuuu uuuu
LATC	LATC Data Output Register								xxxx xxxx	uuuu uuuu
TRISC	PORTC Data Direction Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged

10.4 PORTD, TRISD and LATD Registers

PORTD is an 8-bit wide, bi-directional port. The corresponding Data Direction register is TRISD. Setting a TRISD bit (= '1') will make the corresponding PORTD pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISD bit (= '0') will make the corresponding PORTD pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATD) is also memory mapped. Read-modify-write operations on the LATD register, read and write the latched output value for PORTD.

PORTD is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output.

Note: On a Power-on Reset, these pins are configured as digital inputs.

PORTD is multiplexed with the system bus as the external memory interface; I/O port functions are only available when the system bus is disabled, by setting the EBDIS bit in the MEMCOM register (MEMCON<7>). When operating as the external memory interface, PORTD is the low order byte of the multiplexed address/data bus (AD7:AD0).

PORTD can also be configured as an 8-bit wide microprocessor port (Parallel Slave Port) by setting control bit PSPMODE (TRISE<4>). In this mode, the input buffers are TTL. See Section 10.10 for additional information on the Parallel Slave Port (PSP).

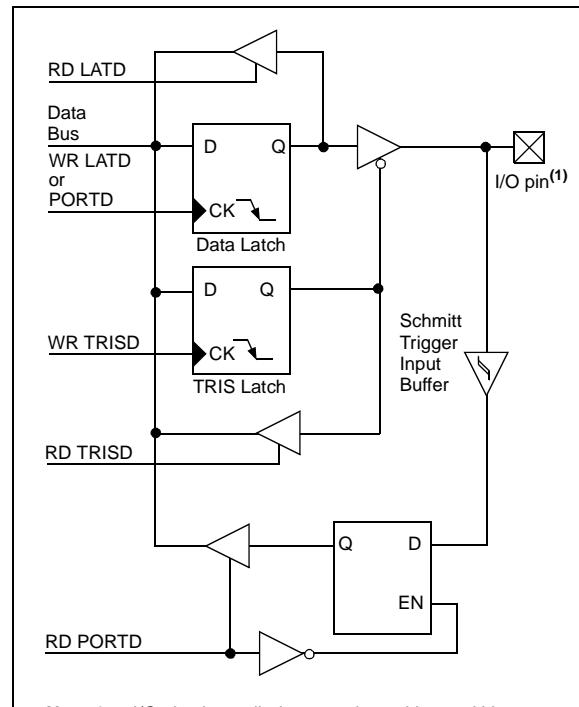
EXAMPLE 10-4: INITIALIZING PORTD

```

CLRF  PORTD    ; Initialize PORTD by
                ; clearing output
                ; data latches
CLRF  LATD     ; Alternate method
                ; to clear output
                ; data latches
MOVLW 0xCF      ; Value used to
                ; initialize data
                ; direction
MOVWF TRISD    ; Set RD<3:0> as inputs
                ; RD<5:4> as outputs
                ; RD<7:6> as inputs

```

FIGURE 10-9: PORTD BLOCK DIAGRAM IN I/O PORT MODE



Note 1: I/O pins have diode protection to VDD and Vss.

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FIGURE 10-10: PORTD BLOCK DIAGRAM IN SYSTEM BUS MODE

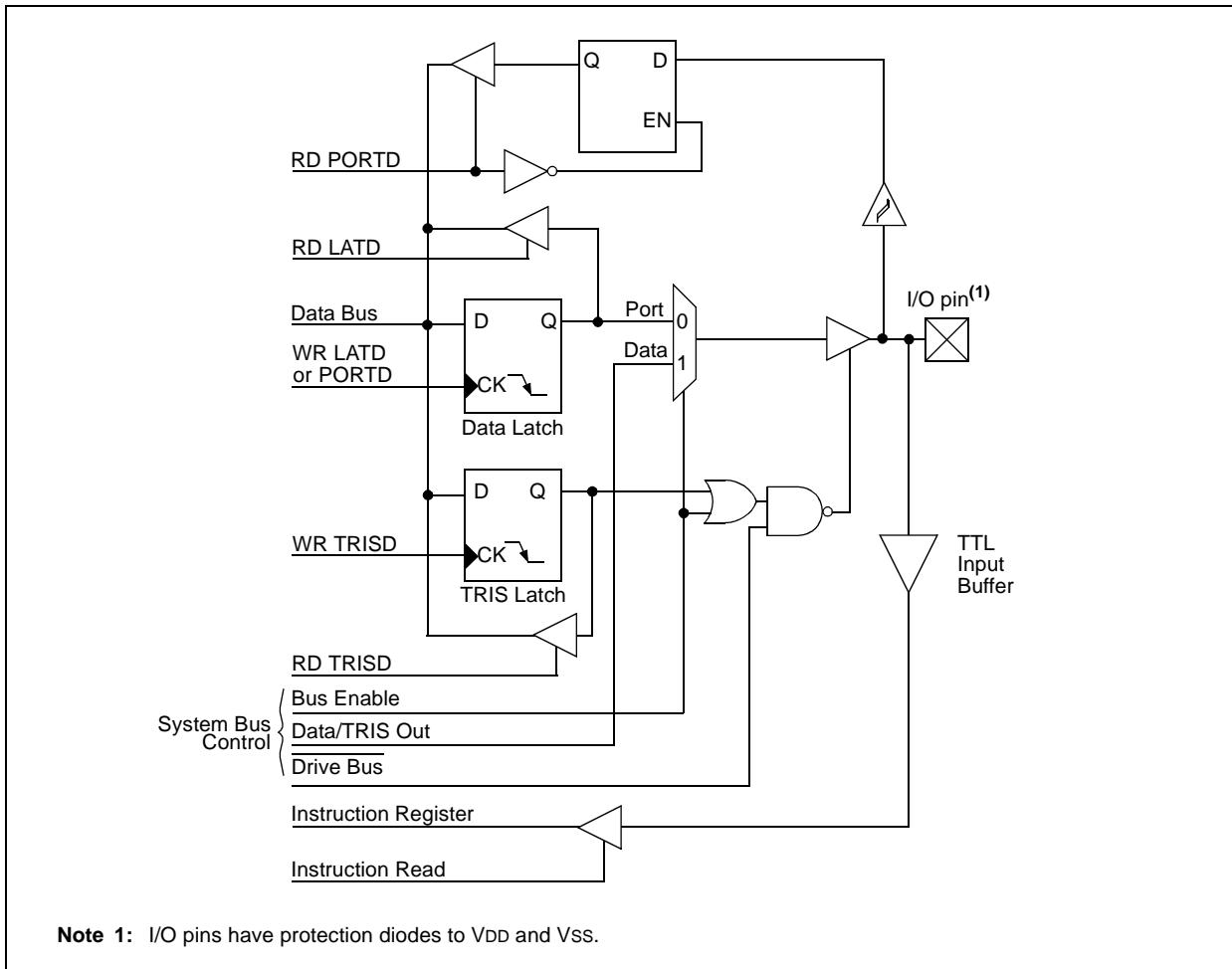


TABLE 10-7: PORTD FUNCTIONS

Name	Bit#	Buffer Type	Function
RD0/AD0/PSP0	bit0	ST/TTL ⁽¹⁾	Input/output port pin, address/data bus bit0 or parallel slave port bit0.
RD1/AD1/PSP1	bit1	ST/TTL ⁽¹⁾	Input/output port pin, address/data bus bit1 or parallel slave port bit1.
RD2/AD2/PSP2	bit2	ST/TTL ⁽¹⁾	Input/output port pin, address/data bus bit2 or parallel slave port bit2.
RD3/AD3/PSP3	bit3	ST/TTL ⁽¹⁾	Input/output port pin, address/data bus bit3 or parallel slave port bit3.
RD4/AD4/PSP4	bit4	ST/TTL ⁽¹⁾	Input/output port pin, address/data bus bit4 or parallel slave port bit4.
RD5/AD5/PSP5	bit5	ST/TTL ⁽¹⁾	Input/output port pin, address/data bus bit5 or parallel slave port bit5.
RD6/AD6/PSP6	bit6	ST/TTL ⁽¹⁾	Input/output port pin, address/data bus bit6 or parallel slave port bit6.
RD7/AD7/PSP7	bit7	ST/TTL ⁽¹⁾	Input/output port pin, address/data bus bit7 or parallel slave port bit7.

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in System Bus or Parallel Slave Port mode.

TABLE 10-8: SUMMARY OF REGISTERS ASSOCIATED WITH PORTD

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
PORTD	RD7	RD6	RD5	RD4	RD3	RD2	RD1	RD0	xxxx xxxx	uuuu uuuu
LATD	LATD Data Output Register								xxxx xxxx	uuuu uuuu
TRISD	PORTD Data Direction Register								1111 1111	1111 1111
PSPCON	IBF	OBF	IBOV	PSPMODE	—	—	—	—	0000 ----	0000 ----
MEMCON	EBDIS	—	WAIT1	WAIT0	—	—	WM1	WM0	0-00 --00	0-00 --00

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PORTD.

10.5 PORTE, TRISE and LATE Registers

PORTE is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISE. Setting a TRISE bit (= '1') will make the corresponding PORTE pin an input (i.e., put the corresponding output driver in a high-Impedance mode). Clearing a TRISE bit (= '0') will make the corresponding PORTE pin an output (i.e., put the contents of the output latch on the selected pin).

Read-modify-write operations on the LATE register, read and write the latched output value for PORTE.

PORTE is an 8-bit port with Schmitt Trigger input buffers. Each pin is individually configurable as an input or output. PORTE is multiplexed with the CCP module (Table 10-9).

On PIC18F8X20 devices, PORTE is also multiplexed with the system bus as the external memory interface; the I/O bus is available only when the system bus is disabled, by setting the EBDIS bit in the MEMCON register (MEMCON<7>). If the device is configured in Microprocessor or Extended Microcontroller mode, then the PORTE<7:0> becomes the high byte of the address/data bus for the external program memory interface. In Microcontroller mode, the PORTE<2:0> pins become the control inputs for the Parallel Slave Port port when bit PSPMODE (PSPCON<4>) is set. (Refer to Section 4.1.1 for more information on program memory modes.)

When the Parallel Slave Port is active, three PORTE pins (RE0/AD/RD8, RE1/AD9/WR, and RE2/AD10/CS) function as its control inputs. This automatically occurs when the PSPMODE bit (PSPCON<4>) is set. Users must also make certain that bits TRISE<2:0> are set to configure the pins as digital inputs, and the ADCON1 register is configured for digital I/O. The PORTE PSP control functions are summarized in Table 10-9.

Pin RE7 can be configured as the alternate peripheral pin for CCP module 2, when the device is operating in Microcontroller mode. This is done by clearing the configuration bit CCP2MX in configuration register, CONFIG3H (CONFIG3H<0>).

Note: For PIC18F8X20 (80-pin) devices operating in Extended Microcontroller mode, PORTE defaults to the system bus on Power-on Reset.

EXAMPLE 10-5: INITIALIZING PORTE

```
CLRF    PORTE    ; Initialize PORTE by
                  ; clearing output
                  ; data latches
CLRF    LATE     ; Alternate method
                  ; to clear output
                  ; data latches
MOVLW  0x03    ; Value used to
                  ; initialize data
                  ; direction
MOVWF  TRISE    ; Set RE1:RE0 as inputs
                  ; RE7:RE2 as outputs
```

FIGURE 10-11: PORTE BLOCK DIAGRAM IN I/O MODE

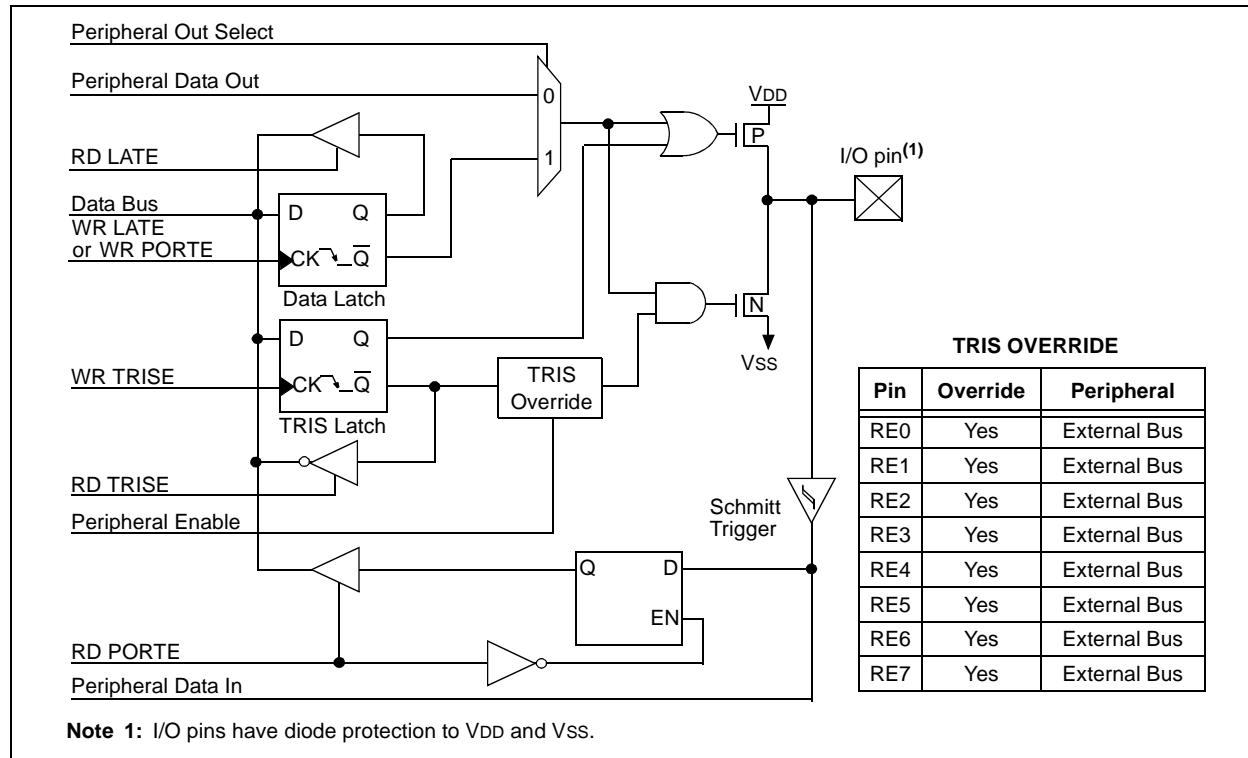
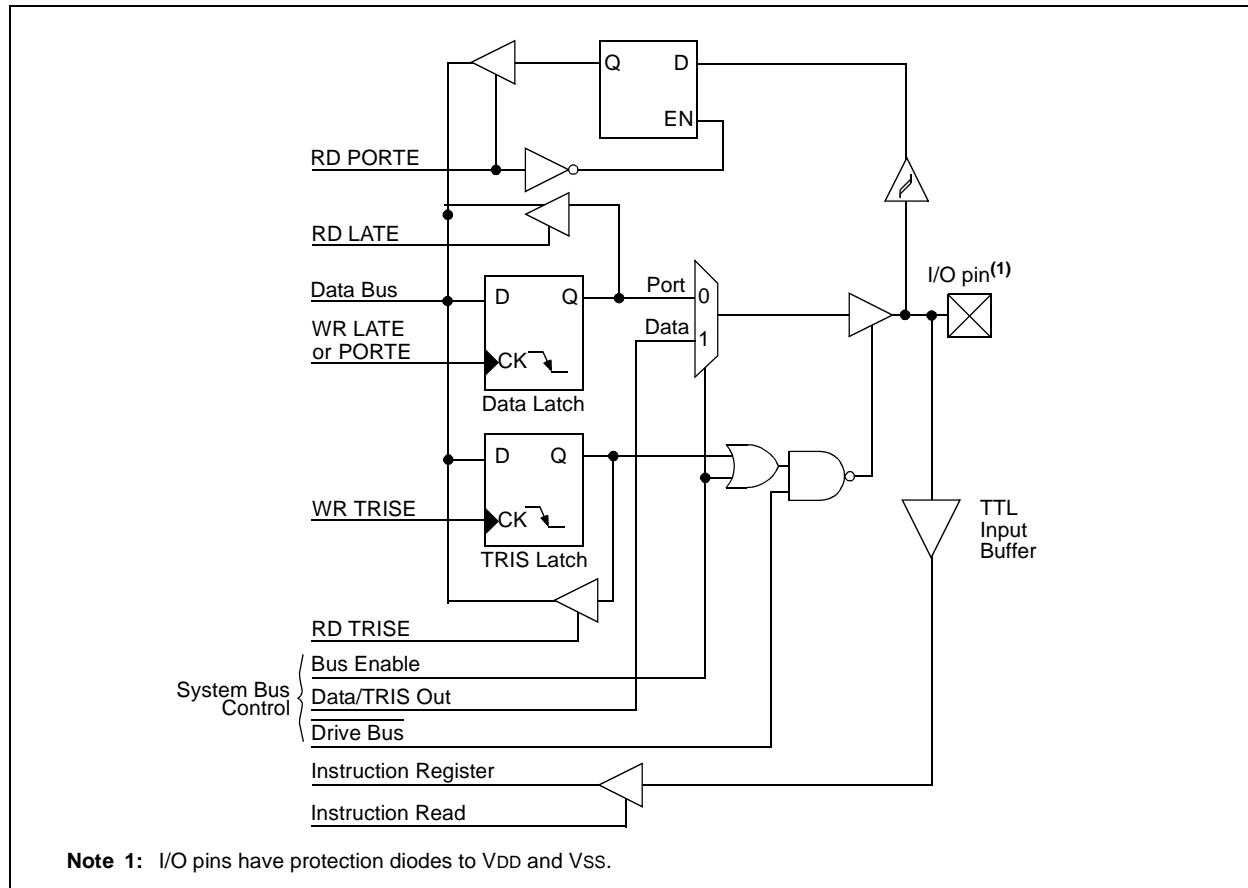


FIGURE 10-12: PORTE BLOCK DIAGRAM IN SYSTEM BUS MODE



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TABLE 10-9: PORTE FUNCTIONS

Name	Bit#	Buffer Type	Function
RE0/AD8/RD	bit0	ST/TTL ⁽¹⁾	Input/output port pin, address/data bit 8, or Read control for parallel slave port For RD (PSP Control mode): 1 = Not a read operation 0 = Read operation, reads PORTD register (if chip selected)
RE1/AD9/WR	bit1	ST/TTL ⁽¹⁾	Input/output port pin, address/data bit 9, or Write control for parallel slave port For WR (PSP Control mode): 1 = Not a write operation 0 = Write operation, writes PORTD register (if chip selected)
RE2/AD10/CS	bit2	ST/TTL ⁽¹⁾	Input/output port pin or address/data bit 10, or Chip Select control for parallel slave port For CS (PSP Control mode): 1 = Device is not selected 0 = Device is selected
RE3/AD11	bit3	ST/TTL ⁽¹⁾	Input/output port pin or address/data bit 11
RE4/AD12	bit4	ST/TTL ⁽¹⁾	Input/output port pin or address/data bit 12
RE5/AD13	bit5	ST/TTL ⁽¹⁾	Input/output port pin or address/data bit 13
RE6/AD14	bit6	ST/TTL ⁽¹⁾	Input/output port pin or address/data bit 14
RE7/AD15/CCP2	bit7	ST/TTL ⁽¹⁾	Input/output port pin, address/data bit 15, or Capture2 input/ Compare2 output/PWM output (PIC18F8X20 devices in Microcontroller mode only).

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O or CCP mode, and TTL buffers when in System Bus or PSP Control mode.

TABLE 10-10: SUMMARY OF REGISTERS ASSOCIATED WITH PORTE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
TRISE	PORTE Data Direction Control Register								1111 1111	1111 1111
PORTE	Read PORTE pin/Write PORTE Data Latch								xxxx xxxx	uuuu uuuu
LATE	Read PORTE Data Latch/Write PORTE Data Latch								xxxx xxxx	uuuu uuuu
MEMCON	EBDIS	—	WAIT1	WAIT0	—	—	WM1	WM0	0-00 --00	0000 --00
PSPCON	IBF	OBF	IBOV	PSPMODE	—	—	—	—	0000 ----	0000 ----

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTE.

10.6 PORTF, LATF, and TRISF Registers

PORTF is an 8-bit wide, bi-directional port. The corresponding Data Direction register is TRISF. Setting a TRISF bit (= '1') will make the corresponding PORTF pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISF bit (= '0') will make the corresponding PORTF pin an output (i.e., put the contents of the output latch on the selected pin).

Read-modify-write operations on the LATF register, read and write the latched output value for PORTF.

PORTF is multiplexed with several analog peripheral functions, including the A/D converter inputs and comparator inputs, outputs, and voltage reference.

Note 1: On a Power-on Reset, the RF6:RF0 pins are configured as inputs and read as '0'.

2: To configure PORTF as digital I/O, turn off comparators and set ADCON1 value.

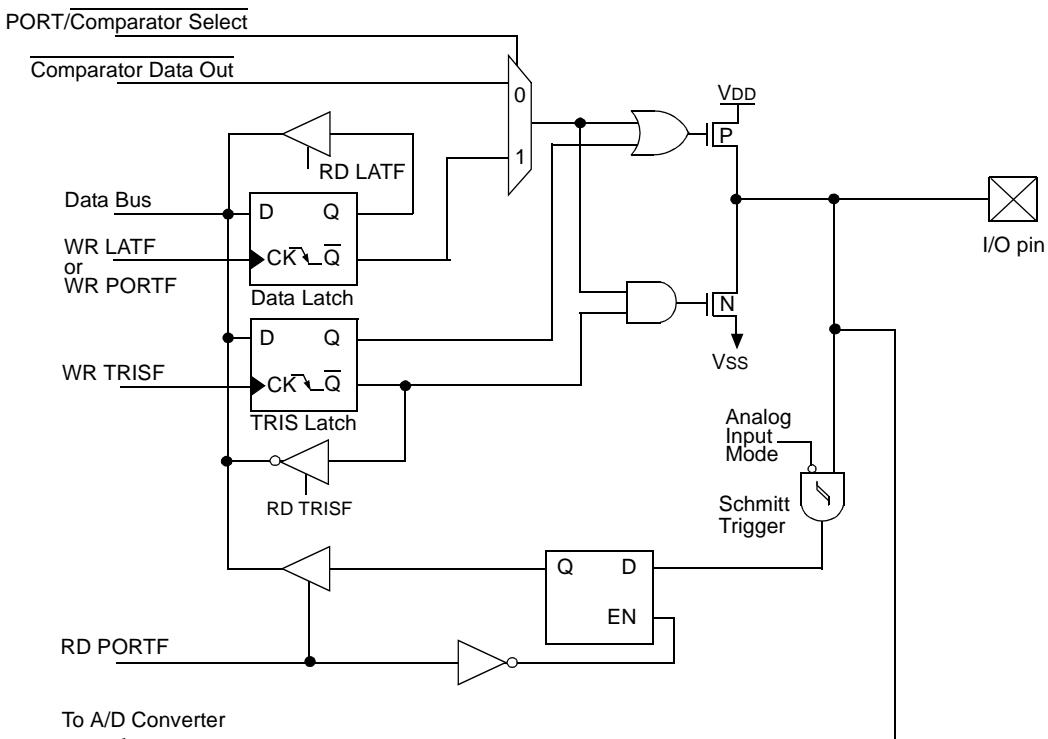
EXAMPLE 10-6: INITIALIZING PORTF

```

CLRF    PORTF      ; Initialize PORTF by
                   ; clearing output
                   ; data latches
CLRF    LATF       ; Alternate method
                   ; to clear output
                   ; data latches
MOVLW  0x07      ;
MOVWF  CMCON     ; Turn off comparators
MOVLW  0x0F      ;
MOVWF  ADCON1    ; Set PORTF as digital I/O
MOVLW  0xCF      ; Value used to
                   ; initialize data
                   ; direction
MOVWF  TRISF     ; Set RF3:RF0 as inputs
                   ; RF5:RF4 as outputs
                   ; RF7:RF6 as inputs

```

FIGURE 10-13: PORTF RF1/AN6/C2OUT, RF2/AN5/C1OUT BLOCK DIAGRAM



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FIGURE 10-14: RF6:RF3 AND RF0 PINS BLOCK DIAGRAM

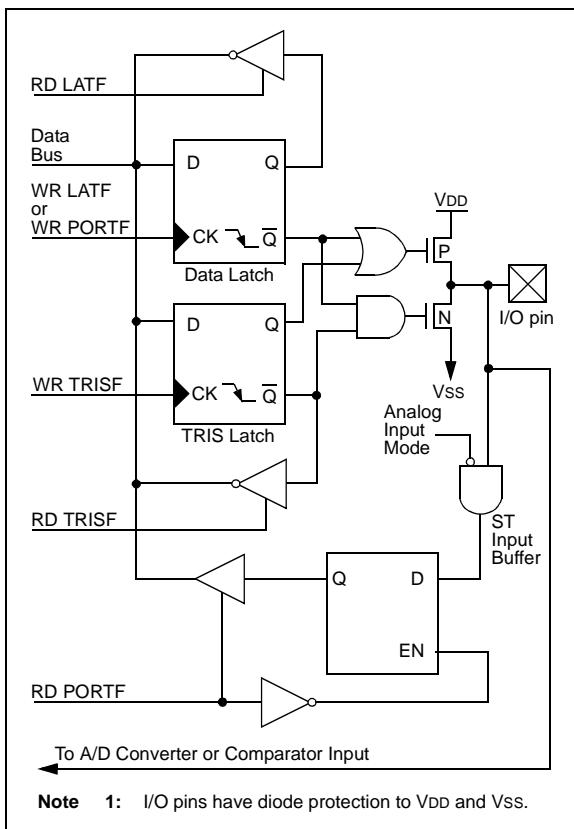


FIGURE 10-15: RF7 PIN BLOCK DIAGRAM

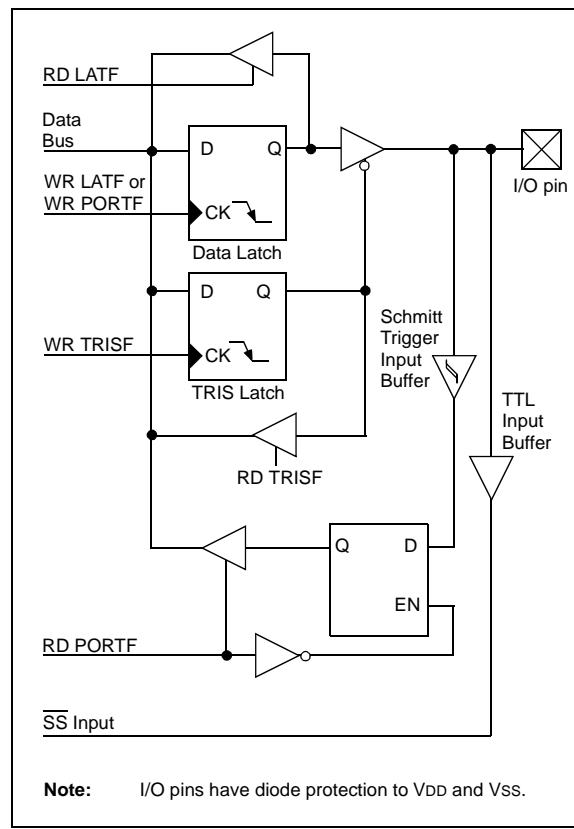


TABLE 10-11: PORTF FUNCTIONS

Name	Bit#	Buffer Type	Function
RF0/AN5	bit0	ST	Input/output port pin or analog input.
RF1/AN6/C2OUT	bit1	ST	Input/output port pin, analog input or comparator 2 output.
RF2/AN7/C1OUT	bit2	ST	Input/output port pin, analog input or comparator 1 output.
RF3/AN8	bit3	ST	Input/output port pin or analog input/comparator input.
RF4/AN9	bit4	ST	Input/output port pin or analog input/comparator input.
RF5/AN10/ CVREF	bit5	ST	Input/output port pin, analog input/comparator input, or comparator reference output.
RF6/AN11	bit6	ST	Input/output port pin or analog input/comparator input.
RF7/SS	bit7	ST/TTL	Input/output port pin or Slave Select pin for Synchronous Serial Port.

Legend: ST = Schmitt Trigger input, TTL = TTL input

TABLE 10-12: SUMMARY OF REGISTERS ASSOCIATED WITH PORTF

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
TRISF	PORTF Data Direction Control Register								1111 1111	1111 1111
PORTF	Read PORTF pin/Write PORTF Data Latch								xxxx xxxx	uuuu uuuu
LATF	Read PORTF Data Latch/Write PORTF Data Latch								0000 0000	uuuu uuuu
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	--00 0000	--00 0000
CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
CVRCN	CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0	0000 0000	0000 0000

Legend: x = unknown, u = unchanged. Shaded cells are not used by PORTF.

10.7 PORTG, TRISG and LATG Registers

PORTG is a 5-bit wide, bi-directional port. The corresponding data direction register is TRISG. Setting a TRISG bit (= '1') will make the corresponding PORTG pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISG bit (= '0') will make the corresponding PORTG pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATG) is also memory mapped. Read-modify-write operations on the LATG register, read and write the latched output value for PORTG.

PORTG is multiplexed with both CCP and USART functions (Table 10-13). PORTG pins have Schmitt Trigger input buffers.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTG pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to

make a pin an input. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

Note: On a Power-on Reset, these pins are configured as digital inputs.

The pin override value is not loaded into the TRIS register. This allows read-modify-write of the TRIS register, without concern due to peripheral overrides.

EXAMPLE 10-7: INITIALIZING PORTG

```

CLRF  PORTG    ; Initialize PORTG by
              ; clearing output
              ; data latches
CLRF  LATG    ; Alternate method
              ; to clear output
              ; data latches
MOVLW 0x04    ; Value used to
              ; initialize data
              ; direction
MOVWF  TRISG   ; Set RG1:RG0 as outputs
              ; RG2 as input
              ; RG4:RG3 as inputs

```

FIGURE 10-16: PORTG BLOCK DIAGRAM (PERIPHERAL OUTPUT OVERRIDE)

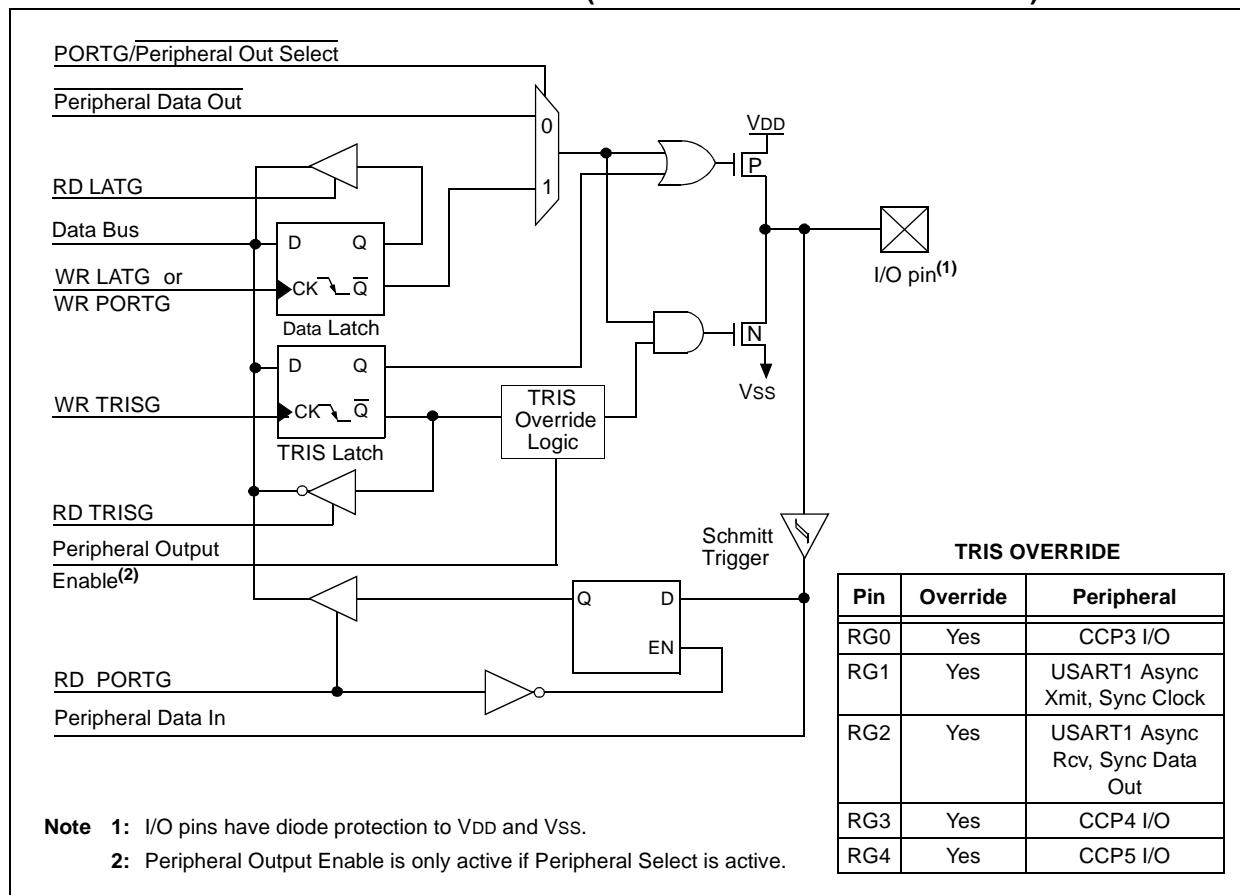


TABLE 10-13: PORTG FUNCTIONS

Name	Bit#	Buffer Type	Function
RG0/CCP3	bit0	ST	Input/output port pin or Capture3 input/Compare3 output/ PWM3 output.
RG1/TX2/CK2	bit1	ST	Input/output port pin, Addressable USART2 Asynchronous Transmit, or Addressable USART2 Synchronous Clock.
RG2/RX2/DT2	bit2	ST	Input/output port pin, Addressable USART2 Asynchronous Receive, or Addressable USART2 Synchronous Data.
RG3/CCP4	bit3	ST	Input/output port pin or Capture4 input/Compare4 output/ PWM4 output.
RG4/CCP5	bit4	ST	Input/output port pin or Capture5 input/Compare5 output/ PWM5 output.

Legend: ST = Schmitt Trigger input

TABLE 10-14: SUMMARY OF REGISTERS ASSOCIATED WITH PORTG

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
PORTG	—	—	—	Read PORTF pin/Write PORTF Data Latch					---x xxxx	---u uuuu
LATG	—	—	—	LATG Data Output Register					---x xxxx	---u uuuu
TRISG	—	—	—	Data Direction Control Register for PORTG					---1 1111	---1 1111

Legend: x = unknown, u = unchanged

10.8 PORTH, LATH, and TRISH Registers

Note: PORTH is available only on PIC18F8X20 devices.

PORTH is an 8-bit wide, bi-directional I/O port. The corresponding data direction register is TRISH. Setting a TRISH bit (= '1') will make the corresponding PORTH pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISH bit (= '0') will make the corresponding PORTH pin an output (i.e., put the contents of the output latch on the selected pin).

Read-modify-write operations on the LATH register, read and write the latched output value for PORTH.

Pins RH7:RH4 are multiplexed with analog inputs AN15:AN12. Pins RH3:RH0 are multiplexed with the system bus as the external memory interface; they are the high order address bits A19:A16. By default, pins RH7:RH4 are enabled as A/D inputs and pins RH3:RH0 are enabled as the system address bus. Register ADCON1 configures RH7:RH4 as I/O or A/D inputs. Register MEMCON configures RH3:RH0 as I/O or system bus pins.

Note 1: On Power-on Reset, PORTH pins RH7:RH4 default to A/D inputs and read as '0'.

2: On Power-on Reset, PORTH pins RH3:RH0 default to system bus signals.

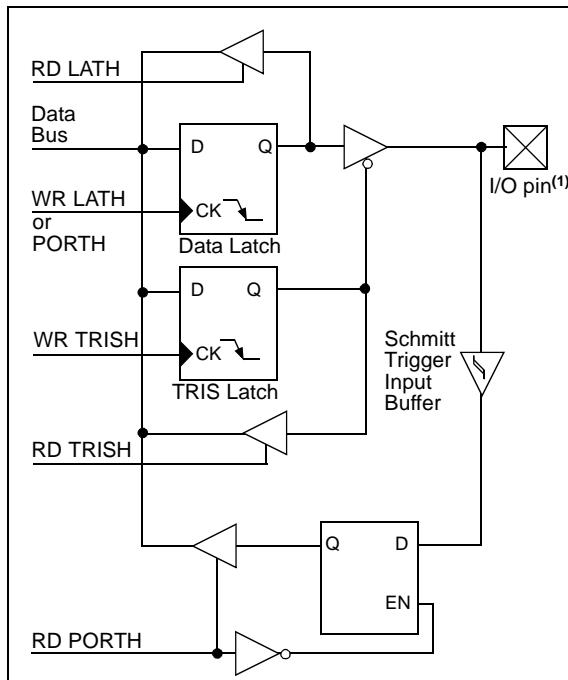
EXAMPLE 10-8: INITIALIZING PORTH

```

CLRF  PORTH      ; Initialize PORTH by
                  ; clearing output
                  ; data latches
CLRF  LATH       ; Alternate method
                  ; to clear output
                  ; data latches
MOVLW  0Fh        ;
MOVWF  ADCON1    ;
MOVLW  0CFh      ; Value used to
                  ; initialize data
                  ; direction
MOVWF  TRISH      ; Set RH3:RH0 as inputs
                  ; RH5:RH4 as outputs
                  ; RH7:RH6 as inputs

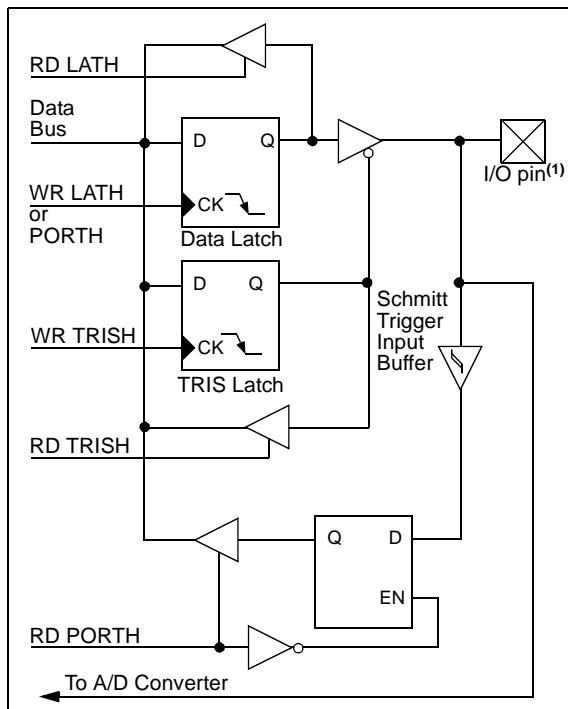
```

FIGURE 10-17: RH3:RH0 PINS BLOCK DIAGRAM IN I/O MODE



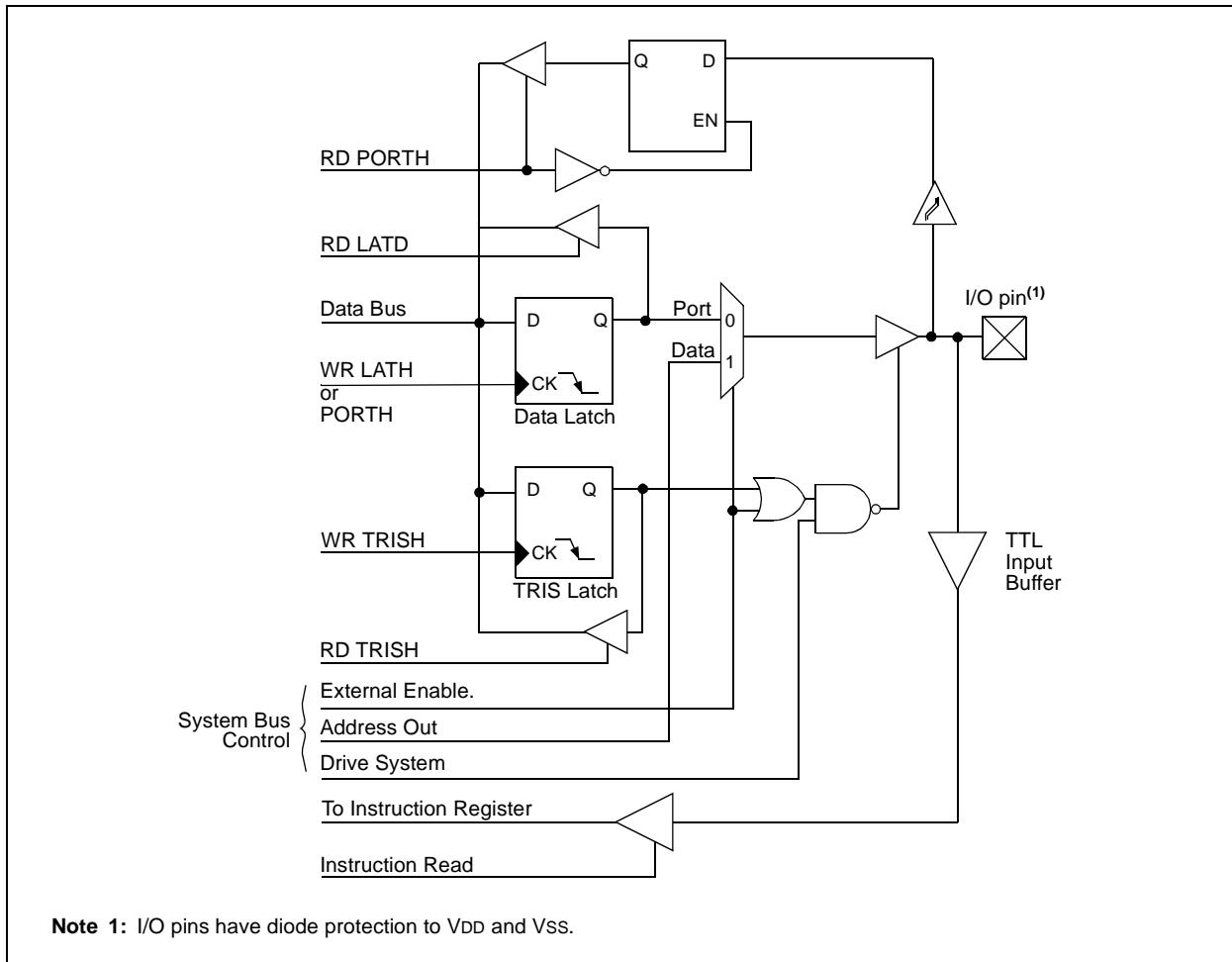
Note 1: I/O pins have diode protection to VDD and Vss.

FIGURE 10-18: RH7:RH4 PINS BLOCK DIAGRAM IN I/O MODE



Note 1: I/O pins have diode protection to VDD and Vss.

FIGURE 10-19: RH3:RH0 PINS BLOCK DIAGRAM IN SYSTEM BUS MODE



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TABLE 10-15: PORTH FUNCTIONS

Name	Bit#	Buffer Type	Function
RH0/A16	bit0	ST/TTL ⁽¹⁾	Input/output port pin or address bit 16 for external memory interface.
RH1/A17	bit1	ST/TTL ⁽¹⁾	Input/output port pin or address bit 17 for external memory interface.
RH2/A18	bit2	ST/TTL ⁽¹⁾	Input/output port pin or address bit 18 for external memory interface.
RH3/A19	bit3	ST/TTL ⁽¹⁾	Input/output port pin or address bit 19 for external memory interface.
RH4/AN12	bit4	ST	Input/output port pin or analog input channel 12.
RH5/AN13	bit5	ST	Input/output port pin or analog input channel 13.
RH6/AN14	bit6	ST	Input/output port pin or analog input channel 14.
RH7/AN15	bit7	ST	Input/output port pin or analog input channel 15.

Legend: ST = Schmitt Trigger input, TTL = TTL input

Note 1: Input buffers are Schmitt Triggers when in I/O mode and TTL buffers when in System Bus or Parallel Slave Port mode.

TABLE 10-16: SUMMARY OF REGISTERS ASSOCIATED WITH PORTH

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOR	Value on all other RESETS
TRISH	PORTH Data Direction Control Register								1111 1111	1111 1111
PORTH	Read PORTH pin/Write PORTH Data Latch								xxxx xxxx	uuuu uuuu
LATH	Read PORTH Data Latch/Write PORTH Data Latch								xxxx xxxx	uuuu uuuu
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	--00 0000	--00 0000
MEMCON	EBDIS	—	WAIT1	WAIT0	—	—	WM1	WM0	0-00 --00	0-00 --00

Legend: x = unknown, u = unchanged, - = unimplemented. Shaded cells are not used by PORTH.

10.9 PORTJ, TRISJ and LATJ Registers

Note: PORTJ is available only on PIC18F8X20 devices.

PORTJ is an 8-bit wide, bi-directional port. The corresponding Data Direction register is TRISJ. Setting a TRISJ bit (= '1') will make the corresponding PORTJ pin an input (i.e., put the corresponding output driver in a Hi-Impedance mode). Clearing a TRISJ bit (= '0') will make the corresponding PORTJ pin an output (i.e., put the contents of the output latch on the selected pin).

The Data Latch register (LATJ) is also memory mapped. Read-modify-write operations on the LATJ register, read and write the latched output value for PORTJ.

PORTJ is multiplexed with the system bus as the external memory interface; I/O port functions are only available when the system bus is disabled. When operating as the external memory interface, PORTJ provides the control signal to external memory devices. The RJ5 pin is not multiplexed with any system bus functions.

When enabling peripheral functions, care should be taken in defining TRIS bits for each PORTJ pin. Some peripherals override the TRIS bit to make a pin an output, while other peripherals override the TRIS bit to make a pin an input. The user should refer to the corresponding peripheral section for the correct TRIS bit settings.

Note: On a Power-on Reset, these pins are configured as digital inputs.

The pin override value is not loaded into the TRIS register. This allows read-modify-write of the TRIS register, without concern due to peripheral overrides.

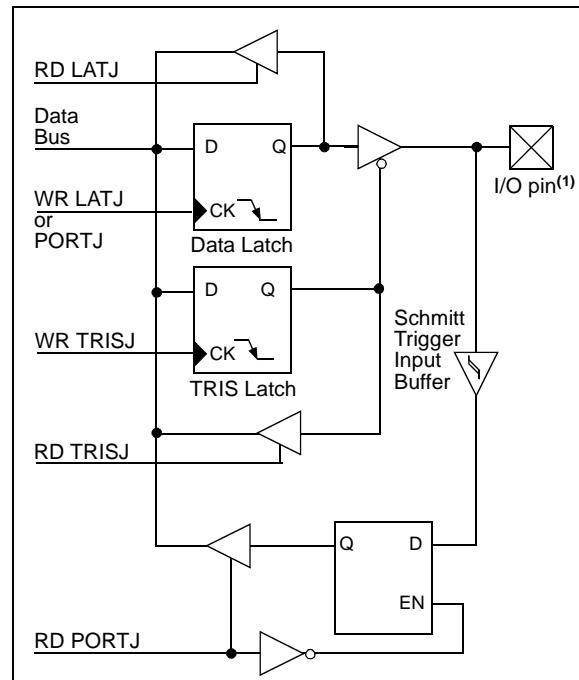
EXAMPLE 10-9: INITIALIZING PORTJ

```

CLRF    PORTJ      ; Initialize PORTJ by
                   ; clearing output
                   ; data latches
CLRF    LATJ       ; Alternate method
                   ; to clear output
                   ; data latches
MOVLW  0xCF       ; Value used to
                   ; initialize data
                   ; direction
MOVWF  TRISJ      ; Set RJ3:RJ0 as inputs
                   ; RJ5:RJ4 as output
                   ; RJ7:RJ6 as inputs

```

FIGURE 10-20: PORTJ BLOCK DIAGRAM IN I/O MODE



Note 1: I/O pins have diode protection to VDD and Vss.

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FIGURE 10-21: RJ4:RJ0 PINS BLOCK DIAGRAM IN SYSTEM BUS MODE

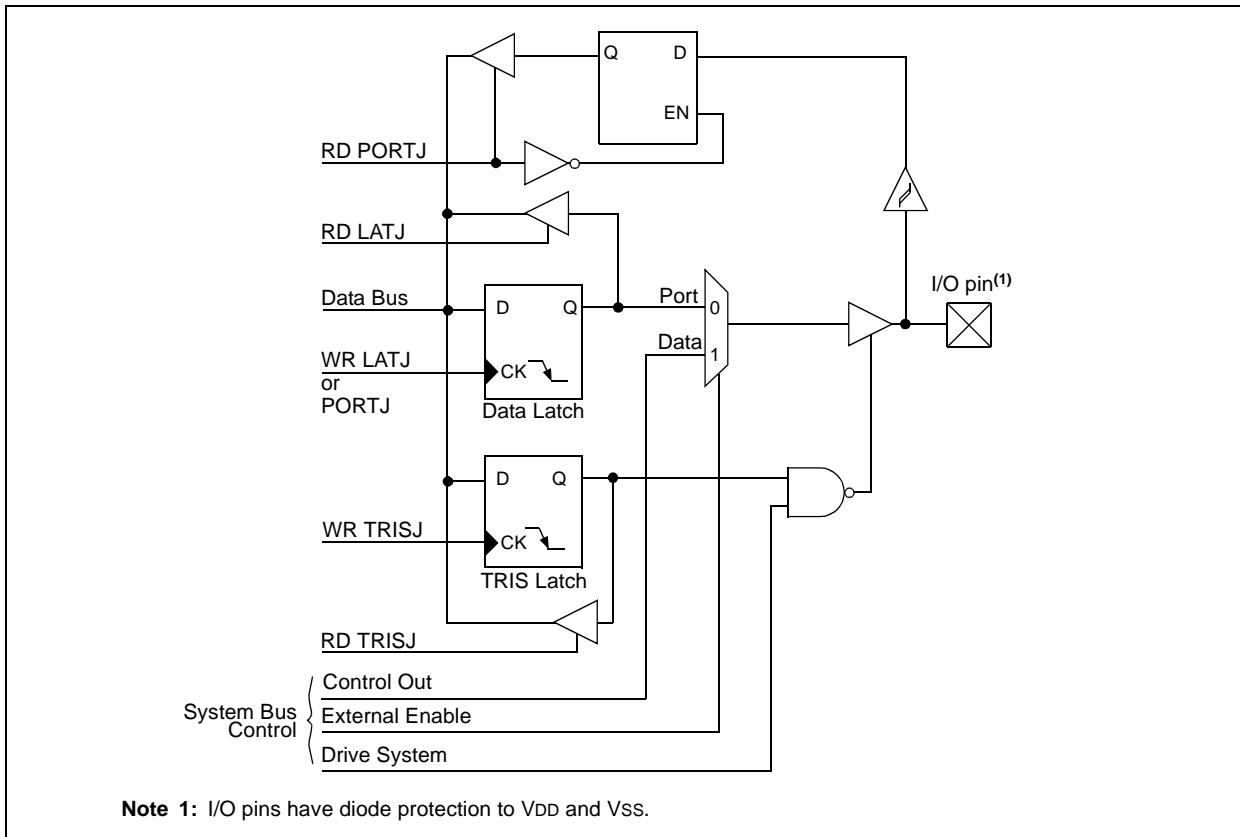


FIGURE 10-22: RJ7:RJ6 PINS BLOCK DIAGRAM IN SYSTEM BUS MODE

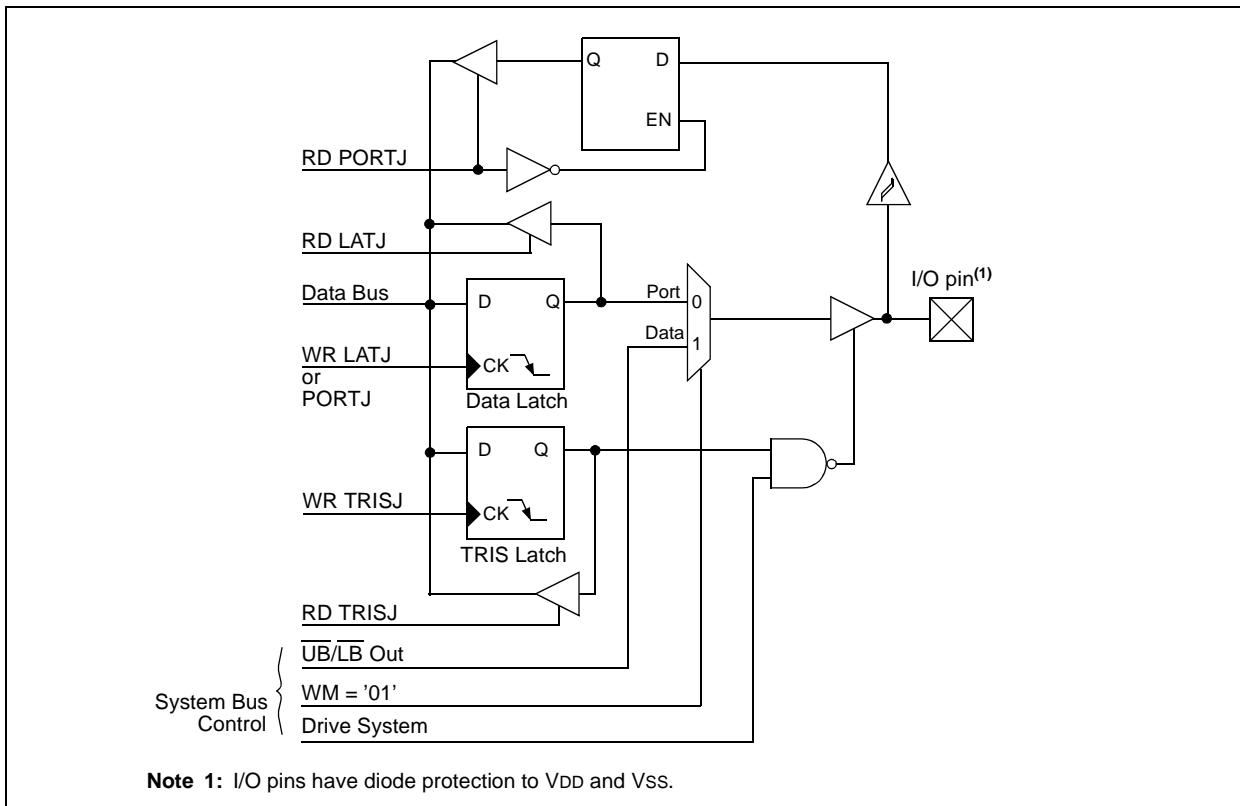


TABLE 10-17: PORTJ FUNCTIONS

Name	Bit#	Buffer Type	Function
RJ0/ALE	bit0	ST	Input/output port pin or Address Latch Enable control for external memory interface.
RJ1/ <u>OE</u>	bit1	ST	Input/output port pin or Output Enable control for external memory interface.
RJ2/ <u>WRL</u>	bit2	ST	Input/output port pin or Write Low Byte control for external memory interface.
RJ3/ <u>WRH</u>	bit3	ST	Input/output port pin or Write High Byte control for external memory interface.
RJ4/BA0	bit4	ST	Input/output port pin or Byte Address 0 control for external memory interface.
RJ5	bit5	ST	Input/output port pin.
RJ6/ <u>LB</u>	bit6	ST	Input/output port pin or Lower Byte Select control for external memory interface.
RJ7/ <u>UB</u>	bit7	ST	Input/output port pin or Upper Byte Select control for external memory interface.

Legend: ST = Schmitt Trigger input

TABLE 10-18: SUMMARY OF REGISTERS ASSOCIATED WITH PORTJ

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
PORTJ	Read PORTJ pin/Write PORTJ Data Latch					xxxx	xxxx	xxxx	xxxx xxxx	uuuu uuuu
LATJ	LATJ Data Output Register					xxxx	xxxx	xxxx	xxxx xxxx	uuuu uuuu
TRISJ	Data Direction Control Register for PORTJ					1111	1111	1111	1111 1111	1111 1111

Legend: x = unknown, u = unchanged

10.10 Parallel Slave Port

PORTD also operates as an 8-bit wide Parallel Slave Port, or microprocessor port, when control bit PSPMODE (TRISE<4>) is set. It is asynchronously readable and writable by the external world through RD control input pin, RE0/RD and WR control input pin, RE1/WR.

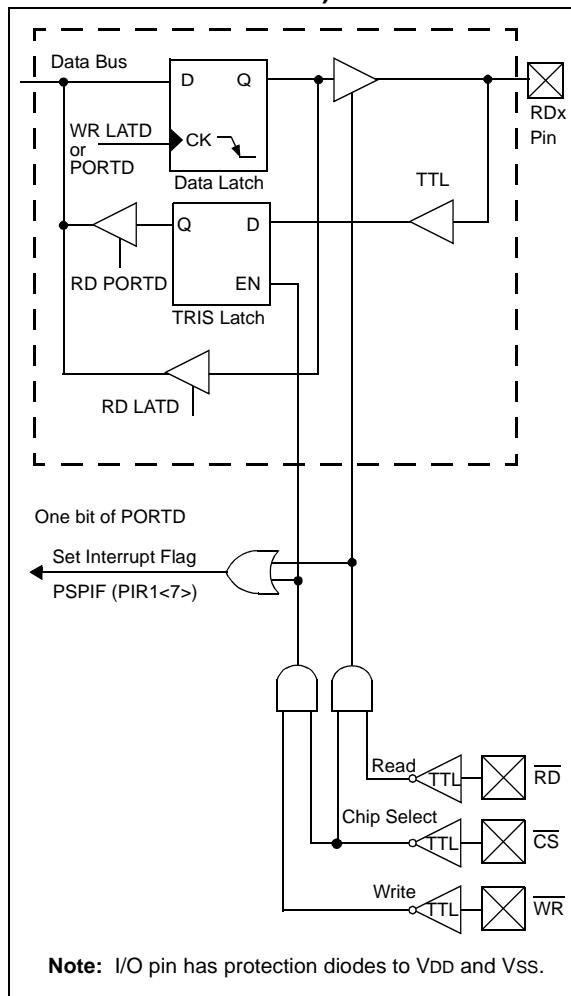
Note: For PIC18F8X20 devices, the Parallel Slave Port is available only in Microcontroller mode.

The PSP can directly interface to an 8-bit microprocessor data bus. The external microprocessor can read or write the PORTD latch as an 8-bit latch. Setting bit PSPMODE enables port pin RE0/RD to be the RD input, RE1/WR to be the WR input and RE2/CS to be the CS (chip select) input. For this functionality, the corresponding data direction bits of the TRISE register (TRISE<2:0>) must be configured as inputs (set). The A/D port configuration bits PCFG2:PCFG0 (ADCON1<2:0>) must be set, which will configure pins RE2:RE0 as digital I/O.

A write to the PSP occurs when both the CS and WR lines are first detected low. A read from the PSP occurs when both the CS and RD lines are first detected low.

The PORTE I/O pins become control inputs for the microprocessor port when bit PSPMODE (PSPCON<4>) is set. In this mode, the user must make sure that the TRISE<2:0> bits are set (pins are configured as digital inputs), and the ADCON1 is configured for digital I/O. In this mode, the input buffers are TTL.

FIGURE 10-23: PORTD AND PORTE BLOCK DIAGRAM (PARALLEL SLAVE PORT)



REGISTER 10-1: PSPCON REGISTER

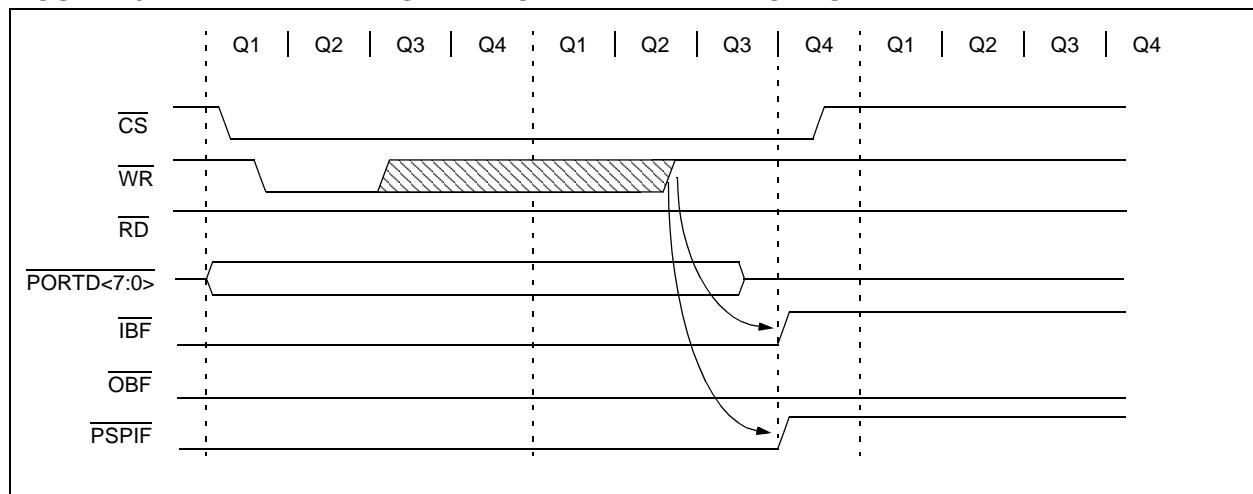
R-0	R-0	R/W-0	R/W-0	U-0	U-0	U-0	U-0
IBF	OBF	IBOV	PSPMODE	—	—	—	—
bit 7							bit 0

- | | |
|---------|---|
| bit 7 | IBF: Input Buffer Full Status bit
1 = A word has been received and is waiting to be read by the CPU
0 = No word has been received |
| bit 6 | OBF: Output Buffer Full Status bit
1 = The output buffer still holds a previously written word
0 = The output buffer has been read |
| bit 5 | IBOV: Input Buffer Overflow Detect bit
1 = A write occurred when a previously input word has not been read
(must be cleared in software)
0 = No overflow occurred |
| bit 4 | PSPMODE: Parallel Slave Port Mode Select bit
1 = Parallel Slave Port mode
0 = General Purpose I/O mode |
| bit 3-0 | Unimplemented: Read as '0' |

Legend:

R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 - n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

FIGURE 10-24: PARALLEL SLAVE PORT WRITE WAVEFORMS



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FIGURE 10-25: PARALLEL SLAVE PORT READ WAVEFORMS

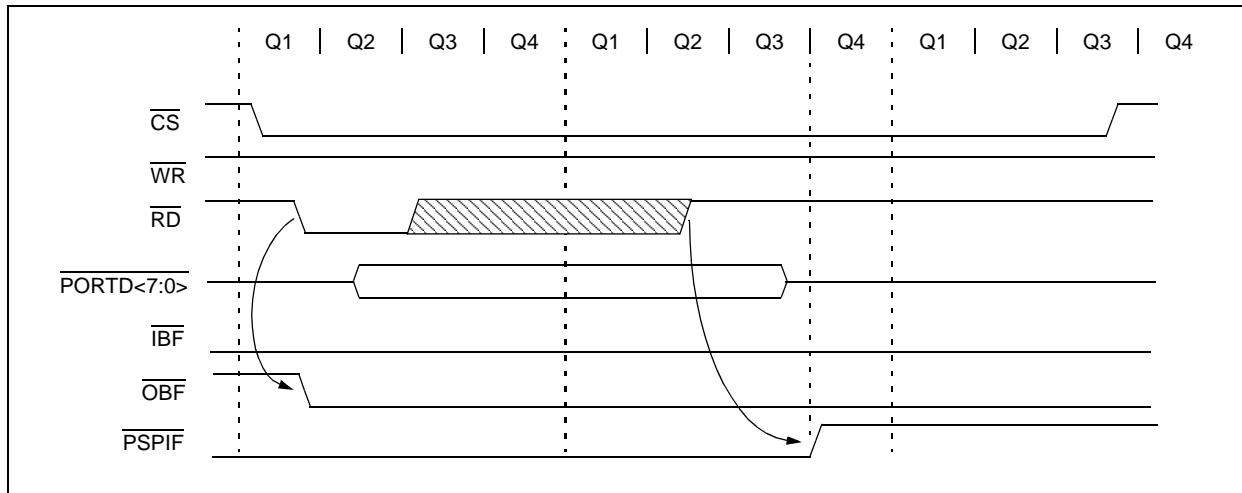


TABLE 10-19: REGISTERS ASSOCIATED WITH PARALLEL SLAVE PORT

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
PORTD	Port Data Latch when written; Port pins when read								xxxx xxxx	uuuu uuuu
LATD	LATD Data Output bits								xxxx xxxx	uuuu uuuu
TRISD	PORTD Data Direction bits								1111 1111	1111 1111
PORTE	—	—	—	—	—	Read PORTE pin/ Write PORTE Data Latch			0000 0000	0000 0000
LATE	—	—	—	—	—	LATE Data Output bits			xxxx xxxx	uuuu uuuu
TRISE	—	—	—	—	—	PORTE Data Direction bits			1111 1111	1111 1111
PSPCON	IBF	OBF	IBOV	PSPMODE	—	—	—	—	0000 ----	0000 ----
INTCON	GIE/ GIEH	PEIE/ GIEL	TMROIF	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
PIR1	PSPIF ⁽¹⁾	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE ⁽¹⁾	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP ⁽¹⁾	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	0111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Parallel Slave Port.

Note 1: Enabled only in Microcontroller mode for PIC18F8X20 devices.

11.0 TIMER0 MODULE

The Timer0 module has the following features:

- Software selectable as an 8-bit or 16-bit timer/counter
- Readable and writable
- Dedicated 8-bit software programmable prescaler
- Clock source selectable to be external or internal
- Interrupt-on-overflow from FFh to 00h in 8-bit mode and FFFFh to 0000h in 16-bit mode
- Edge select for external clock

Figure 11-1 shows a simplified block diagram of the Timer0 module in 8-bit mode and Figure 11-2 shows a simplified block diagram of the Timer0 module in 16-bit mode.

The T0CON register (Register 11-1) is a readable and writable register that controls all the aspects of Timer0, including the prescale selection.

REGISTER 11-1: T0CON: TIMER0 CONTROL REGISTER

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0
bit 7							bit 0

- | | |
|---------|---|
| bit 7 | TMR0ON: Timer0 On/Off Control bit
1 = Enables Timer0
0 = Stops Timer0 |
| bit 6 | T08BIT: Timer0 8-bit/16-bit Control bit
1 = Timer0 is configured as an 8-bit timer/counter
0 = Timer0 is configured as a 16-bit timer/counter |
| bit 5 | T0CS: Timer0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT) |
| bit 4 | T0SE: Timer0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin |
| bit 3 | PSA: Timer0 Prescaler Assignment bit
1 = Timer0 prescaler is NOT assigned. Timer0 clock input bypasses prescaler.
0 = Timer0 prescaler is assigned. Timer0 clock input comes from prescaler output. |
| bit 2-0 | T0PS2:T0PS0: Timer0 Prescaler Select bits
111 = 1:256 prescale value
110 = 1:128 prescale value
101 = 1:64 prescale value
100 = 1:32 prescale value
011 = 1:16 prescale value
010 = 1:8 prescale value
001 = 1:4 prescale value
000 = 1:2 prescale value |

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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FIGURE 11-1: TIMER0 BLOCK DIAGRAM IN 8-BIT MODE

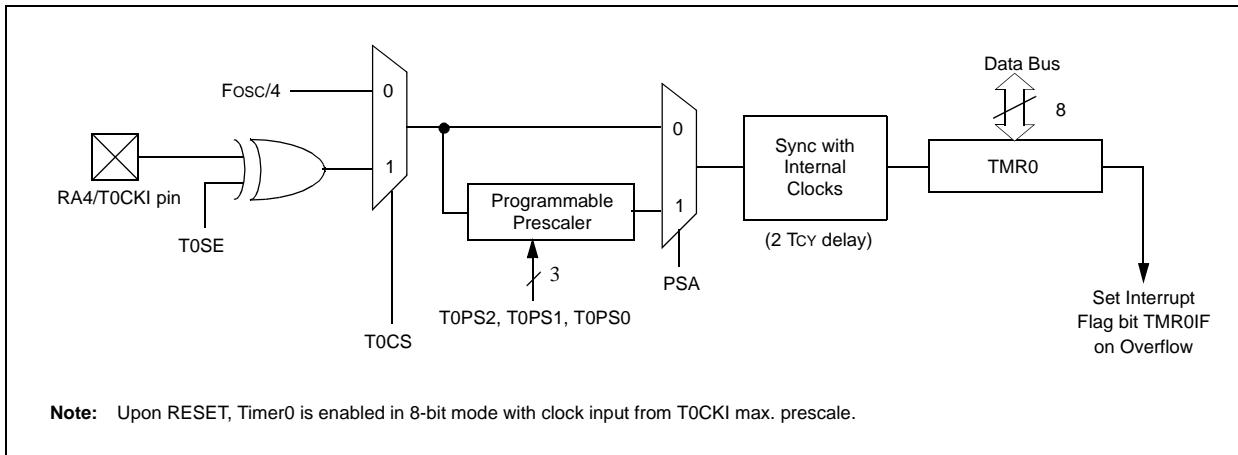
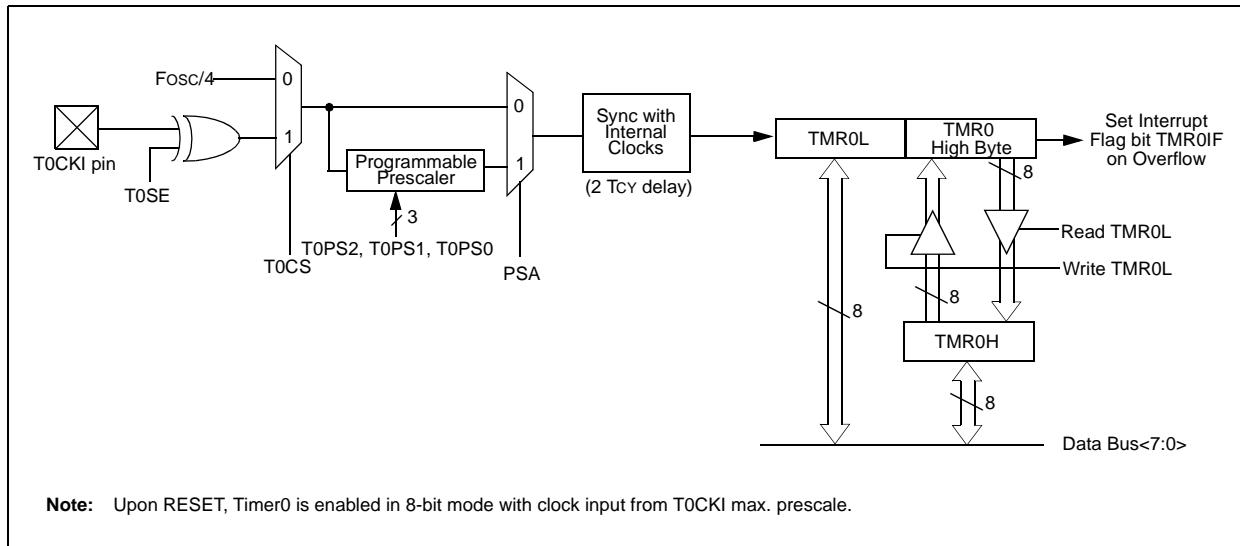


FIGURE 11-2: TIMER0 BLOCK DIAGRAM IN 16-BIT MODE



11.1 Timer0 Operation

Timer0 can operate as a timer or as a counter.

Timer mode is selected by clearing the T0CS bit. In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If the TMR0 register is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

Counter mode is selected by setting the T0CS bit. In Counter mode, Timer0 will increment, either on every rising or falling edge of pin RA4/T0CKI. The incrementing edge is determined by the Timer0 Source Edge Select bit (T0SE). Clearing the T0SE bit selects the rising edge. Restrictions on the external clock input are discussed below.

When an external clock input is used for Timer0, it must meet certain requirements. The requirements ensure the external clock can be synchronized with the internal phase clock (T_{osc}). Also, there is a delay in the actual incrementing of Timer0 after synchronization.

11.2 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module. The prescaler is not readable or writable.

The PSA and T0PS2:T0PS0 bits determine the prescaler assignment and prescale ratio.

Clearing bit PSA will assign the prescaler to the Timer0 module. When the prescaler is assigned to the Timer0 module, prescale values of 1:2, 1:4,..., 1:256 are selectable.

When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF TMR0, MOVWF TMR0, BSF TMR0, x....etc.) will clear the prescaler count.

Note: Writing to TMR0 when the prescaler is assigned to Timer0 will clear the prescaler count, but will not change the prescaler assignment.

11.2.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control, (i.e., it can be changed "on-the-fly" during program execution).

11.3 Timer0 Interrupt

The TMR0 interrupt is generated when the TMR0 register overflows from FFh to 00h in 8-bit mode, or FFFFh to 0000h in 16-bit mode. This overflow sets the TMR0IF bit. The interrupt can be masked by clearing the TMR0IE bit. The TMR0IE bit must be cleared in software by the Timer0 module Interrupt Service Routine, before re-enabling this interrupt. The TMR0 interrupt cannot awaken the processor from SLEEP, since the timer is shut-off during SLEEP.

11.4 16-Bit Mode Timer Reads and Writes

TMR0H is not the high byte of the timer/counter in 16-bit mode, but is actually a buffered version of the high byte of Timer0 (refer to Figure 11-2). The high byte of the Timer0 counter/timer is not directly readable nor writable. TMR0H is updated with the contents of the high byte of Timer0 during a read of TMR0L. This provides the ability to read all 16-bits of Timer0 without having to verify that the read of the high and low byte were valid, due to a rollover between successive reads of the high and low byte.

A write to the high byte of Timer0 must also take place through the TMR0H buffer register. Timer0 high byte is updated with the contents of TMR0H when a write occurs to TMR0L. This allows all 16-bits of Timer0 to be updated at once.

TABLE 11-1: REGISTERS ASSOCIATED WITH TIMER0

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
TMR0L	Timer0 Module Low Byte Register								xxxx xxxx	uuuu uuuu
TMR0H	Timer0 Module High Byte Register								0000 0000	0000 0000
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
T0CON	TMR0ON	T08BIT	T0CS	T0SE	PSA	T0PS2	T0PS1	T0PS0	1111 1111	1111 1111
TRISA	—	PORTA Data Direction Register							-111 1111	-111 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations, read as '0'. Shaded cells are not used by Timer0.

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NOTES:

12.0 TIMER1 MODULE

The Timer1 module timer/counter has the following features:

- 16-bit timer/counter
(two 8-bit registers; TMR1H and TMR1L)
 - Readable and writable (both registers)
 - Internal or external clock select
 - Interrupt-on-overflow from FFFFh to 0000h
 - RESET from CCP module special event trigger

Figure 12-1 is a simplified block diagram of the Timer1 module.

Register 12-1 details the Timer1 control register. This register controls the operating mode of the Timer1 module, and contains the Timer1 oscillator enable bit (T1OSCEN). Timer1 can be enabled or disabled by setting or clearing control bit, TMR1ON (T1CON<0>).

REGISTER 12-1: T1CON: TIMER1 CONTROL REGISTER

- | | |
|---------|--|
| bit 7 | RD16: 16-bit Read/Write Mode Enable bit
1 = Enables register Read/Write of Timer1 in one 16-bit operation
0 = Enables register Read/Write of Timer1 in two 8-bit operations |
| bit 6 | Unimplemented: Read as '0' |
| bit 5-4 | T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale value
10 = 1:4 Prescale value
01 = 1:2 Prescale value
00 = 1:1 Prescale value |
| bit 3 | T1OSCEN: Timer1 Oscillator Enable bit
1 = Timer1 Oscillator is enabled
0 = Timer1 Oscillator is shut-off
The oscillator inverter and feedback resistor are turned off to eliminate power drain. |
| bit 2 | T1SYNC: Timer1 External Clock Input Synchronization Select bit
<u>When TMR1CS = 1:</u>
1 = Do not synchronize external clock input
0 = Synchronize external clock input
<u>When TMR1CS = 0:</u>
This bit is ignored. Timer1 uses the internal clock when TMR1CS = 0. |
| bit 1 | TMR1CS: Timer1 Clock Source Select bit
1 = External clock from pin RC0/T1OSO/T13CKI (on the rising edge)
0 = Internal clock (Fosc/4) |
| bit 0 | TMR1ON: Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1 |

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

12.1 Timer1 Operation

Timer1 can operate in one of these modes:

- As a timer
 - As a synchronous counter
 - As an asynchronous counter

The operating mode is determined by the clock select bit, TMR1CS (T1CON<1>).

When TMR1CS = 0, Timer1 increments every instruction cycle. When TMR1CS = 1, Timer1 increments on every rising edge of the external clock input or the Timer1 oscillator, if enabled.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1OSI and RC0/T1OSO/T1CKI pins become inputs. That is, the TRISC<1:0> value is ignored, and the pins are read as '0'.

Timer1 also has an internal “RESET input”. This RESET can be generated by the CCP module (Section 16.0).

FIGURE 12-1: TIMER1 BLOCK DIAGRAM

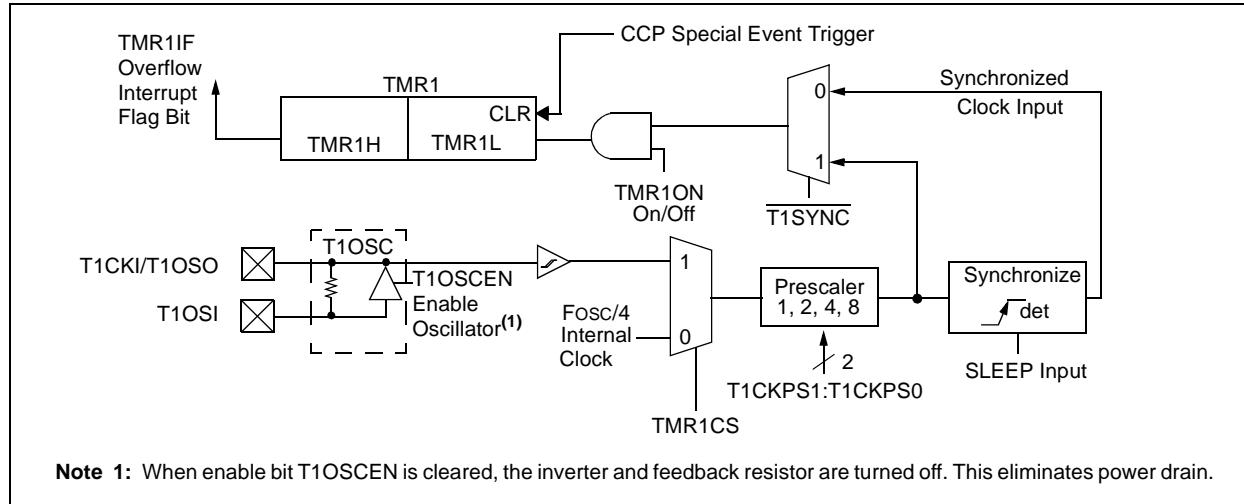
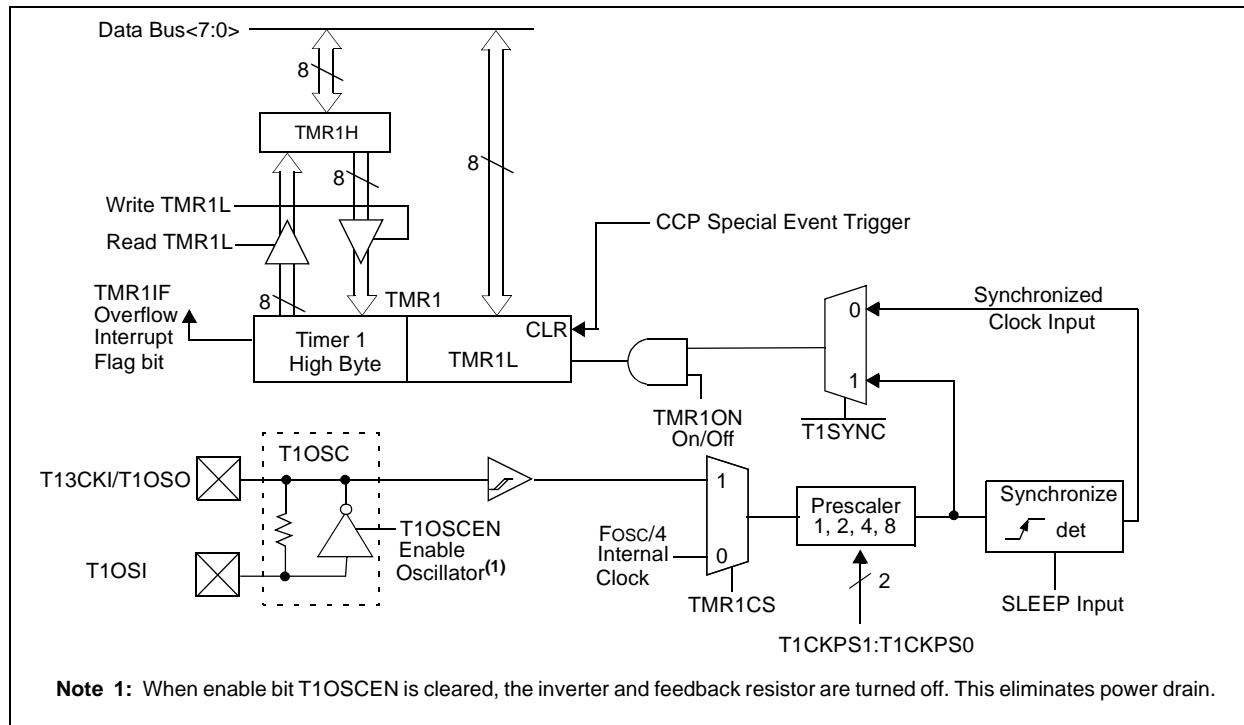


FIGURE 12-2: TIMER1 BLOCK DIAGRAM: 16-BIT READ/WRITE MODE



12.2 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins T1OSI (input) and T1OSO (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 200 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 12-1 shows the capacitor selection for the Timer1 oscillator.

The user must provide a software time delay to ensure proper start-up of the Timer1 oscillator.

TABLE 12-1: CAPACITOR SELECTION FOR THE ALTERNATE OSCILLATOR

Osc Type	Freq	C1	C2
LP	32 kHz	TBD ⁽¹⁾	TBD ⁽¹⁾
Crystal to be Tested:			
32.768 kHz	Epson C-001R32.768kHzA	± 20 PPM	

- Note 1:** Microchip suggests 33 pF as a starting point in validating the oscillator circuit.
- 2:** Higher capacitance increases the stability of the oscillator, but also increases the start-up time.
- 3:** Since each resonator/crystal has its own characteristics, the user should consult the resonator/crystal manufacturer for appropriate values of external components.
- 4:** Capacitor values are for design guidance only.

12.3 Timer1 Interrupt

The TMR1 Register pair (TMR1H:TMR1L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR1 Interrupt, if enabled, is generated on overflow, which is latched in interrupt flag bit, TMR1IF (PIR1<0>). This interrupt can be enabled/disabled by setting/clearing TMR1 interrupt enable bit, TMR1IE (PIE1<0>).

12.4 Resetting Timer1 using a CCP Trigger Output

If the CCP module is configured in Compare mode to generate a “special event trigger” (CCP1M3:CCP1M0 = 1011), this signal will reset Timer1 and start an A/D conversion (if the A/D module is enabled).

Note: The special event triggers from the CCP1 module will not set interrupt flag bit TMR1IF (PIR1<0>).

Timer1 must be configured for either Timer or Synchronized Counter mode to take advantage of this feature. If Timer1 is running in Asynchronous Counter mode, this RESET operation may not work.

In the event that a write to Timer1 coincides with a special event trigger from CCP1, the write will take precedence.

In this mode of operation, the CCP1H:CCP1L registers pair effectively becomes the period register for Timer1.

12.5 Timer1 16-Bit Read/Write Mode

Timer1 can be configured for 16-bit reads and writes (see Figure 12-2). When the RD16 control bit (T1CON<7>) is set, the address for TMR1H is mapped to a buffer register for the high byte of Timer1. A read from TMR1L will load the contents of the high byte of Timer1 into the Timer1 high byte buffer. This provides the user with the ability to accurately read all 16-bits of Timer1 without having to determine whether a read of the high byte, followed by a read of the low byte, is valid, due to a rollover between reads.

A write to the high byte of Timer1 must also take place through the TMR1H buffer register. Timer1 high byte is updated with the contents of TMR1H when a write occurs to TMR1L. This allows a user to write all 16 bits to both the high and low bytes of Timer1 at once.

The high byte of Timer1 is not directly readable or writable in this mode. All reads and writes must take place through the Timer1 high byte buffer register. Writes to TMR1H do not clear the Timer1 prescaler. The prescaler is only cleared on writes to TMR1L.

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TABLE 12-2: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMROIE	INT0IE	RBIE	TMROIF	INT0IF	RBIF	0000 0000	0000 0000
PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	0111 1111
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
T1CON	RD16	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0-00 0000	u-uu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

13.0 TIMER2 MODULE

The Timer2 module timer has the following features:

- 8-bit timer (TMR2 register)
- 8-bit period register (PR2)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)
- Interrupt on TMR2 match of PR2
- SSP module optional use of TMR2 output to generate clock shift

Timer2 has a control register shown in Register 13-1. Timer2 can be shut-off by clearing control bit TMR2ON (T2CON<2>) to minimize power consumption. Figure 13-1 is a simplified block diagram of the Timer2 module. Register 13-1 shows the Timer2 control register. The prescaler and postscaler selection of Timer2 are controlled by this register.

13.1 Timer2 Operation

Timer2 can be used as the PWM time-base for the PWM mode of the CCP module. The TMR2 register is readable and writable, and is cleared on any device RESET. The input clock (Fosc/4) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits, T2CKPS1:T2CKPS0 (T2CON<1:0>). The match output of TMR2 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR2 interrupt (latched in flag bit, TMR2IF (PIR1<1>)).

The prescaler and postscaler counters are cleared when any of the following occurs:

- a write to the TMR2 register
- a write to the T2CON register
- any device RESET (Power-on Reset, MCLR Reset, Watchdog Timer Reset, or Brown-out Reset)

TMR2 is not cleared when T2CON is written.

REGISTER 13-1: T2CON: TIMER2 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	

bit 7

bit 0

- bit 7 **Unimplemented:** Read as '0'
- bit 6-3 **T2OUTPS3:T2OUTPS0:** Timer2 Output Postscale Select bits
 0000 = 1:1 Postscale
 0001 = 1:2 Postscale
 •
 •
 •
 1111 = 1:16 Postscale
- bit 2 **TMR2ON:** Timer2 On bit
 1 = Timer2 is on
 0 = Timer2 is off
- bit 1-0 **T2CKPS1:T2CKPS0:** Timer2 Clock Prescale Select bits
 00 = Prescaler is 1
 01 = Prescaler is 4
 1x = Prescaler is 16

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

13.2 Timer2 Interrupt

The Timer2 module has an 8-bit period register, PR2. Timer2 increments from 00h until it matches PR2 and then resets to 00h on the next increment cycle. PR2 is a readable and writable register. The PR2 register is initialized to FFh upon RESET.

13.3 Output of TMR2

The output of TMR2 (before the postscaler) is fed to the Synchronous Serial Port module, which optionally uses it to generate the shift clock.

FIGURE 13-1: TIMER2 BLOCK DIAGRAM

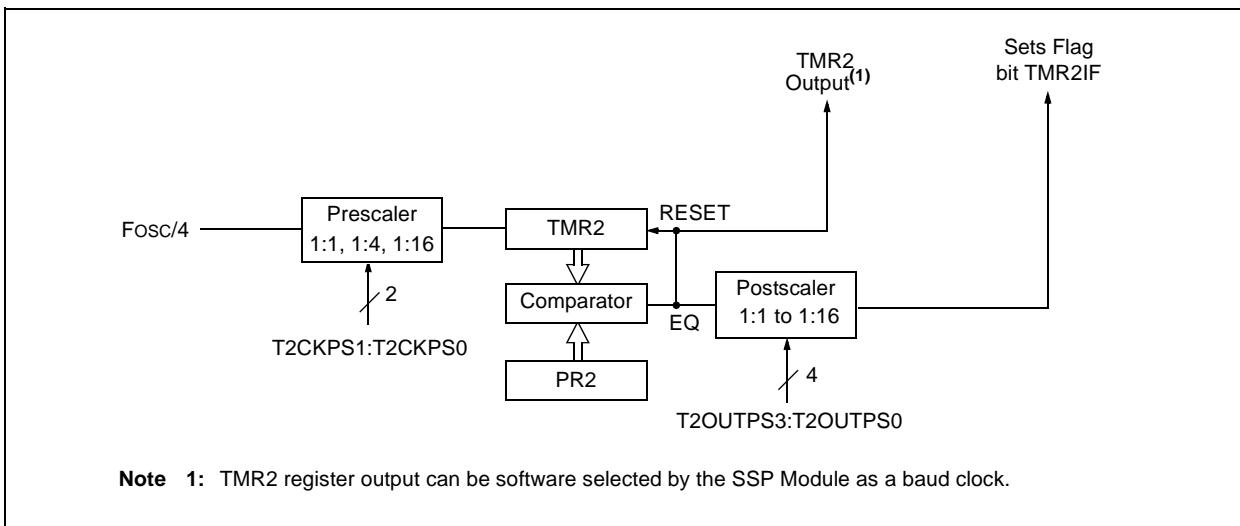


TABLE 13-1: REGISTERS ASSOCIATED WITH TIMER2 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMROIE	INT0IE	RBIE	TMROIF	INT0IF	RBIF	0000 0000	0000 0000
PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	0111 1111
TMR2	Timer2 Module Register								0000 0000	0000 0000
T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
PR2	Timer2 Period Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer2 module.

14.0 TIMER3 MODULE

The Timer3 module timer/counter has the following features:

- 16-bit timer/counter
(two 8-bit registers; TMR3H and TMR3L)
- Readable and writable (both registers)
- Internal or external clock select
- Interrupt-on-overflow from FFFFh to 0000h
- RESET from CCP module trigger

Figure 14-1 is a simplified block diagram of the Timer3 module.

Register 14-1 shows the Timer3 control register. This register controls the operating mode of the Timer3 module and sets the CCP clock source.

Register 12-1 shows the Timer1 control register. This register controls the operating mode of the Timer1 module, as well as contains the Timer1 oscillator enable bit (T1OSCEN), which can be a clock source for Timer3.

REGISTER 14-1: T3CON: TIMER3 CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON	
bit 7								bit 0

- bit 7 **RD16:** 16-bit Read/Write Mode Enable bit
 1 = Enables register Read/Write of Timer3 in one 16-bit operation
 0 = Enables register Read/Write of Timer3 in two 8-bit operations
- bit 6,3 **T3CCP2:T3CCP1:** Timer3 and Timer1 to CCPx Enable bits
 11 = Timer3 and Timer4 are the clock sources for CCP1 through CCP5
 10 = Timer3 and Timer4 are the clock sources for CCP3 through CCP5;
 Timer1 and Timer2 are the clock sources for CCP1 and CCP2
 01 = Timer3 and Timer4 are the clock sources for CCP2 through CCP5;
 Timer1 and Timer2 are the clock sources for CCP1
 00 = Timer1 and Timer2 are the clock sources for CCP1 through CCP5
- bit 5-4 **T3CKPS1:T3CKPS0:** Timer3 Input Clock Prescale Select bits
 11 = 1:8 Prescale value
 10 = 1:4 Prescale value
 01 = 1:2 Prescale value
 00 = 1:1 Prescale value
- bit 2 **T3SYNC:** Timer3 External Clock Input Synchronization Control bit
 (Not usable if the system clock comes from Timer1/Timer3.)
When TMR3CS = 1:
 1 = Do not synchronize external clock input
 0 = Synchronize external clock input
When TMR3CS = 0:
 This bit is ignored. Timer3 uses the internal clock when TMR3CS = 0.
- bit 1 **TMR3CS:** Timer3 Clock Source Select bit
 1 = External clock input from Timer1 oscillator or T1CKI
 (on the rising edge after the first falling edge)
 0 = Internal clock (Fosc/4)
- bit 0 **TMR3ON:** Timer3 On bit
 1 = Enables Timer3
 0 = Stops Timer3

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

14.1 Timer3 Operation

Timer3 can operate in one of these modes:

- As a timer
- As a synchronous counter
- As an asynchronous counter

The operating mode is determined by the clock select bit, TMR3CS (T3CON<1>).

When TMR3CS = 0, Timer3 increments every instruction cycle. When TMR3CS = 1, Timer3 increments on every rising edge of the Timer1 external clock input or the Timer1 oscillator, if enabled.

When the Timer1 oscillator is enabled (T1OSCEN is set), the RC1/T1OSI and RC0/T1OSO/T1CKI pins become inputs. That is, the TRISC<1:0> value is ignored, and the pins are read as '0'.

Timer3 also has an internal "RESET input". This RESET can be generated by the CCP module (Section 14.0).

FIGURE 14-1: TIMER3 BLOCK DIAGRAM

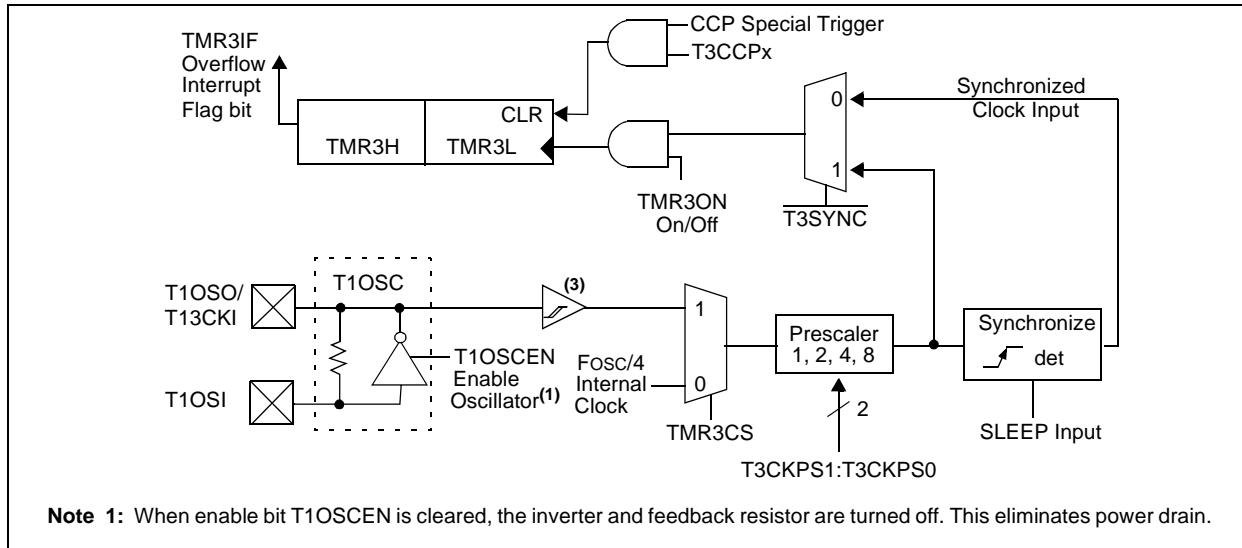
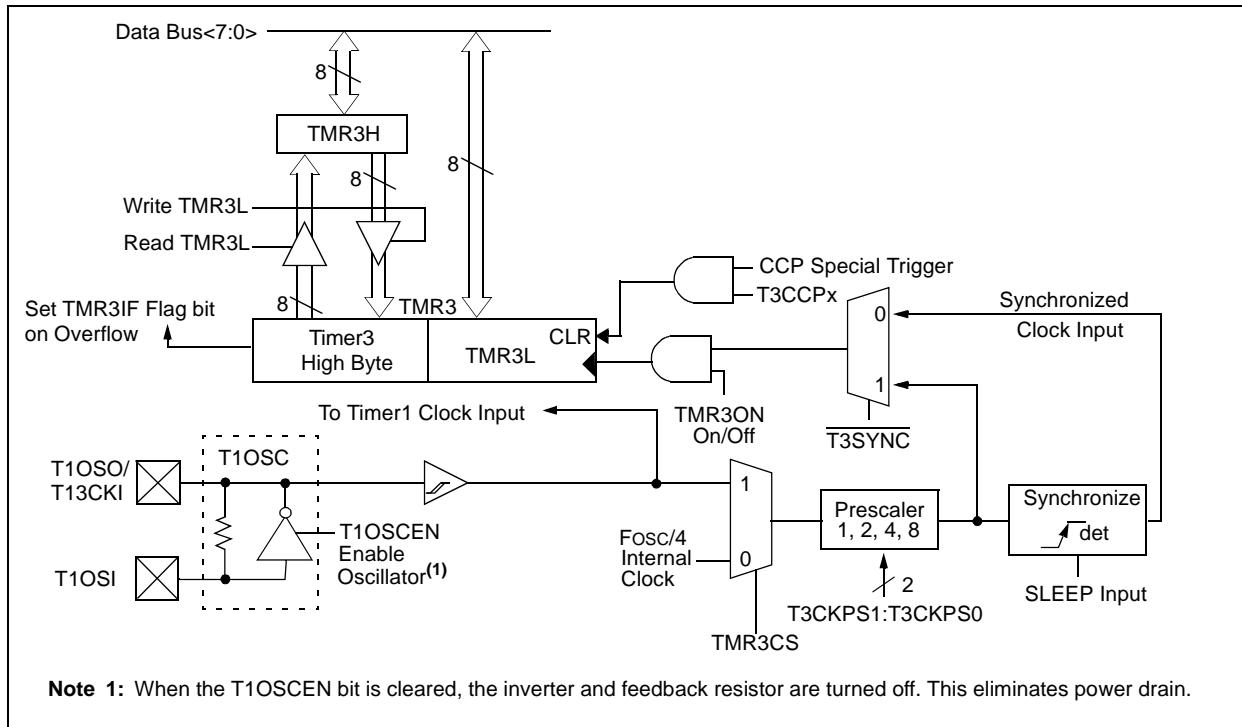


FIGURE 14-2: TIMER3 BLOCK DIAGRAM CONFIGURED IN 16-BIT READ/WRITE MODE



14.2 Timer1 Oscillator

The Timer1 oscillator may be used as the clock source for Timer3. The Timer1 oscillator is enabled by setting the T1OSCEN (T1CON<3>) bit. The oscillator is a low power oscillator rated up to 200 kHz. See Section 12.0 for further details.

14.3 Timer3 Interrupt

The TMR3 Register pair (TMR3H:TMR3L) increments from 0000h to FFFFh and rolls over to 0000h. The TMR3 Interrupt, if enabled, is generated on overflow, which is latched in interrupt flag bit, TMR3IF (PIR2<1>). This interrupt can be enabled/disabled by setting/clearing TMR3 interrupt enable bit, TMR3IE (PIE2<1>).

14.4 Resetting Timer3 Using a CCP Trigger Output

If the CCP module is configured in Compare mode to generate a “special event trigger” (CCP1M3:CCP1M0 = 1011), this signal will reset Timer3.

Note: The special event triggers from the CCP module will not set interrupt flag bit, TMR3IF (PIR1<0>).

Timer3 must be configured for either Timer or Synchronized Counter mode to take advantage of this feature. If Timer3 is running in Asynchronous Counter mode, this RESET operation may not work. In the event that a write to Timer3 coincides with a special event trigger from CCP1, the write will take precedence. In this mode of operation, the CCP1H:CCP1L registers pair effectively becomes the period register for Timer3.

TABLE 14-1: REGISTERS ASSOCIATED WITH TIMER3 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
PIR2	—	—	—	EEIF	BCLIF	LVDIF	TMR3IF	CCP2IF	---0 0000	---0 0000
PIE2	—	—	—	EEIE	BCLIE	LVDIE	TMR3IE	CCP2IE	---0 0000	---0 0000
IPR2	—	—	—	EEIP	BCLIP	LVDIP	TMR3IP	CCP2IP	---1 1111	---1 1111
TMR3L	Holding Register for the Least Significant Byte of the 16-bit TMR3 Register								xxxx xxxx	uuuu uuuu
TMR3H	Holding Register for the Most Significant Byte of the 16-bit TMR3 Register								xxxx xxxx	uuuu uuuu
T1CON	RD16	—	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	0-00 0000	u-uu uuuu
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON	0000 0000	uuuu uuuu

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer3 module.

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NOTES:

15.0 TIMER4 MODULE

The Timer4 module timer has the following features:

- 8-bit timer (TMR4 register)
- 8-bit period register (PR4)
- Readable and writable (both registers)
- Software programmable prescaler (1:1, 1:4, 1:16)
- Software programmable postscaler (1:1 to 1:16)
- Interrupt on TMR4 match of PR4

Timer4 has a control register shown in Register 15-1. Timer4 can be shut-off by clearing control bit TMR4ON (T4CON<2>) to minimize power consumption. The prescaler and postscaler selection of Timer4 are also controlled by this register. Figure 15-1 is a simplified block diagram of the Timer4 module.

15.1 Timer4 Operation

Timer4 can be used as the PWM time-base for the PWM mode of the CCP module. The TMR4 register is readable and writable, and is cleared on any device RESET. The input clock ($F_{osc}/4$) has a prescale option of 1:1, 1:4 or 1:16, selected by control bits T4CKPS1:T4CKPS0 (T4CON<1:0>). The match output of TMR4 goes through a 4-bit postscaler (which gives a 1:1 to 1:16 scaling inclusive) to generate a TMR4 interrupt (latched in flag bit TMR4IF, (PIR3<3>)).

The prescaler and postscaler counters are cleared when any of the following occurs:

- a write to the TMR4 register
- a write to the T4CON register
- any device RESET (Power-on Reset, MCLR Reset, Watchdog Timer Reset, or Brown-out Reset)

TMR4 is not cleared when T4CON is written.

REGISTER 15-1: T4CON: TIMER4 CONTROL REGISTER

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0	

bit 7

bit 0

- bit 7 **Unimplemented:** Read as '0'
- bit 6-3 **T4OUTPS3:T4OUTPS0:** Timer4 Output Postscale Select bits
 0000 = 1:1 Postscale
 0001 = 1:2 Postscale
 •
 •
 •
 1111 = 1:16 Postscale
- bit 2 **TMR4ON:** Timer4 On bit
 1 = Timer4 is on
 0 = Timer4 is off
- bit 1-0 **T4CKPS1:T4CKPS0:** Timer4 Clock Prescale Select bits
 00 = Prescaler is 1
 01 = Prescaler is 4
 1x = Prescaler is 16

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

15.2 Timer4 Interrupt

The Timer4 module has an 8-bit period register, PR4, which is both readable and writable. Timer4 increments from 00h until it matches PR4 and then resets to 00h on the next increment cycle. The PR4 register is initialized to FFh upon RESET.

15.3 Output of TMR4

The output of TMR4 (before the postscaler) is used only as a PWM time-base for the CCP modules. It is not used as a baud rate clock for the MSSP, as is the Timer2 output.

FIGURE 15-1: TIMER4 BLOCK DIAGRAM

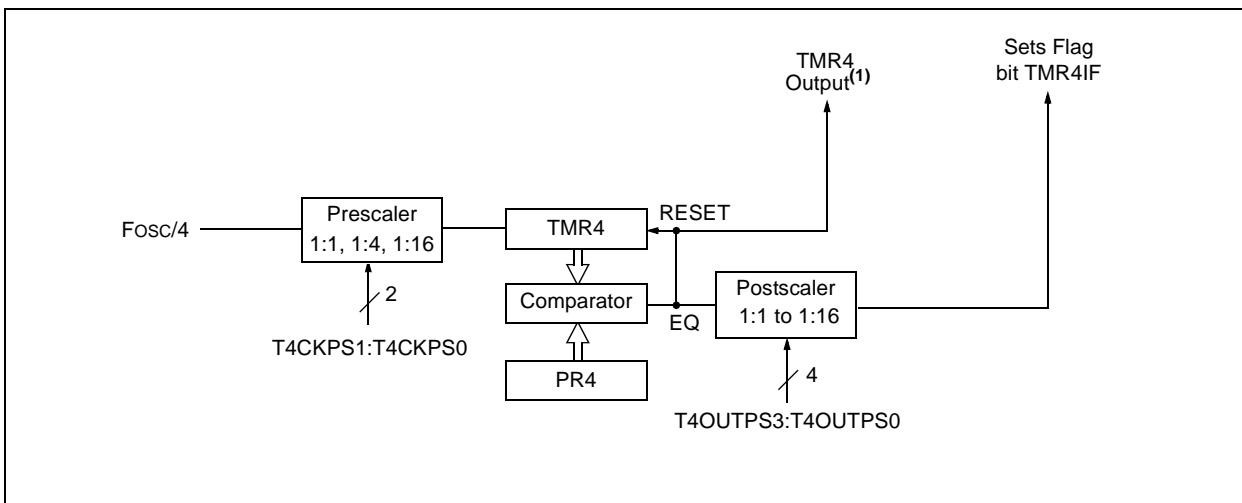


TABLE 15-1: REGISTERS ASSOCIATED WITH TIMER4 AS A TIMER/COUNTER

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
IPR3	—	—	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	--11 1111	--00 0000
PIR3	—	—	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	--00 0000	--00 0000
PIE3	—	—	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	--00 0000	--00 0000
TMR4	Timer4 Module Register								0000 0000	0000 0000
T4CON	—	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0	-000 0000	-000 0000
PR4	Timer4 Period Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer4 module.

16.1 CCP Module Configuration

Each Capture/Compare/PWM module is associated with a control register (generically, CCP x CON) and a data register (CCPR x). The data register in turn is comprised of two 8-bit registers: CCPR x L (low byte) and CCPR x H (high byte). All registers are both readable and writable.

16.1.1 CCP MODULES AND TIMER RESOURCES

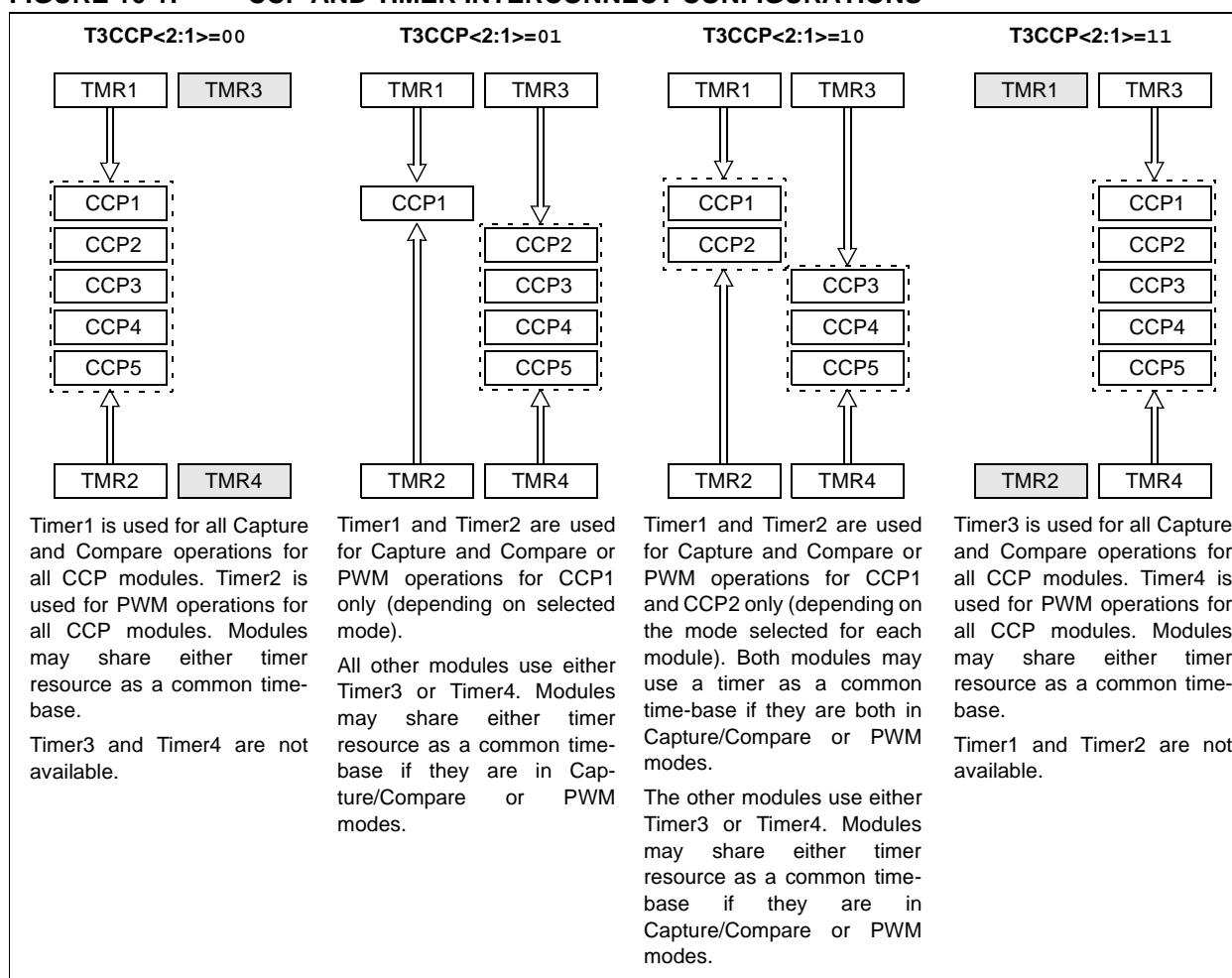
The CCP modules utilize Timers 1, 2, 3 or 4, depending on the mode selected. Timer1 and Timer3 are available to modules in Capture or Compare modes, while Timer2 and Timer4 are available for modules in PWM mode.

TABLE 16-1: CCP MODE - TIMER RESOURCE

CCP Mode	Timer Resource
Capture	Timer1 or Timer3
Compare	Timer1 or Timer3
PWM	Timer2 or Timer4

The assignment of a particular timer to a module is determined by the Timer-to-CCP Enable bits in the T3CON register (Register 14-1, page 137). Depending on the configuration selected, up to four timers may be active at once, with modules in the same configuration (Capture/Compare or PWM) sharing timer resources. The possible configurations are shown in Figure 16-1.

FIGURE 16-1: CCP AND TIMER INTERCONNECT CONFIGURATIONS



16.2 Capture Mode

In Capture mode, CCP1H:CCPR1L captures the 16-bit value of the TMR1 or TMR3 registers when an event occurs on pin RC2/CCP1. An event is defined as one of the following:

- every falling edge
- every rising edge
- every 4th rising edge
- every 16th rising edge

The event is selected by control bits, CCP1M3:CCP1M0 (CCP1CON<3:0>). When a capture is made, the interrupt request flag bit, CCP1IF (PIR1<2>) is set; it must be cleared in software. If another capture occurs before the value in register CCPR1 is read, the old captured value is overwritten by the new captured value.

16.2.1 CCP PIN CONFIGURATION

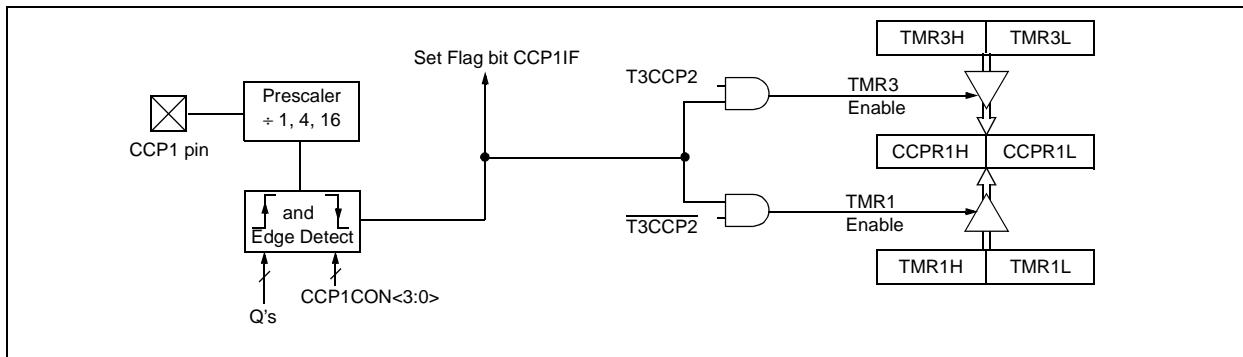
In Capture mode, the RC2/CCP1 pin should be configured as an input by setting the TRISC<2> bit.

Note: If the RC2/CCP1 is configured as an output, a write to the port can cause a capture condition.

16.2.2 TIMER1/TIMER3 MODE SELECTION

The timers that are to be used with the capture feature (Timer1 and/or Timer3) must be running in Timer mode or Synchronized Counter mode. In Asynchronous Counter mode, the capture operation may not work. The timer to be used with each CCP module is selected in the T3CON register (see Section 16.1.1).

FIGURE 16-2: CAPTURE MODE OPERATION BLOCK DIAGRAM



16.2.3 SOFTWARE INTERRUPT

When the Capture mode is changed, a false capture interrupt may be generated. The user should keep bit CCP1IE (PIE1<2>) clear to avoid false interrupts and should clear the flag bit, CCP1IF, following any such change in operating mode.

16.2.4 CCP PRESCALER

There are four prescaler settings, specified by bits CCP1M3:CCP1M0. Whenever the CCP module is turned off or the CCP module is not in Capture mode, the prescaler counter is cleared. This means that any RESET will clear the prescaler counter.

Switching from one capture prescaler to another may generate an interrupt. Also, the prescaler counter will not be cleared, therefore, the first capture may be from a non-zero prescaler. Example 16-1 shows the recommended method for switching between capture prescalers. This example also clears the prescaler counter and will not generate the "false" interrupt.

EXAMPLE 16-1: CHANGING BETWEEN CAPTURE PRESCALERS

```

CLRF    CCP1CON, F ; Turn CCP module off
MOVLW  NEW_CAPT_PS ; Load WREG with the
                     ; new prescaler mode
                     ; value and CCP ON
MOVWF  CCP1CON      ; Load CCP1CON with
                     ; this value

```

16.3 Compare Mode

In Compare mode, the 16-bit CCP1 register value is constantly compared against either the TMR1 register pair value, or the TMR3 register pair value. When a match occurs, the CCP1 pin is:

- driven High
- driven Low
- toggle output (High to Low or Low to High)
- remains unchanged

The action on the pin is based on the value of control bits, CCP1M3:CCP1M0. At the same time, interrupt flag bit, CCP1IF (CCP2IF) is set.

16.3.1 CCP PIN CONFIGURATION

The user must configure the CCPx pin as an output by clearing the appropriate TRIS bit.

Note: Clearing the CCP1CON register will force the RC2/CCP1 compare output latch to the default low level. This is not the PORTC I/O data latch.

16.3.2 TIMER1/TIMER3 MODE SELECTION

Timer1 and/or Timer3 must be running in Timer mode or Synchronized Counter mode, if the CCP module is using the compare feature. In Asynchronous Counter mode, the compare operation may not work.

16.3.3 SOFTWARE INTERRUPT MODE

When generate software interrupt is chosen, the CCP1 pin is not affected. Only a CCP interrupt is generated (if enabled).

16.3.4 SPECIAL EVENT TRIGGER

In this mode, an internal hardware trigger is generated, which may be used to initiate an action.

The special event trigger output of either CCP1 or CCP2 resets the TMR1 or TMR3 register pair, depending on which timer resource is currently selected. This allows the CCP1 register to effectively be a 16-bit programmable period register for Timer1 or Timer3.

The CCP2 Special Event Trigger will also start an A/D conversion if the A/D module is enabled.

Note: The special event trigger from the CCP2 module will not set the Timer1 or Timer3 interrupt flag bits.

FIGURE 16-3: COMPARE MODE OPERATION BLOCK DIAGRAM

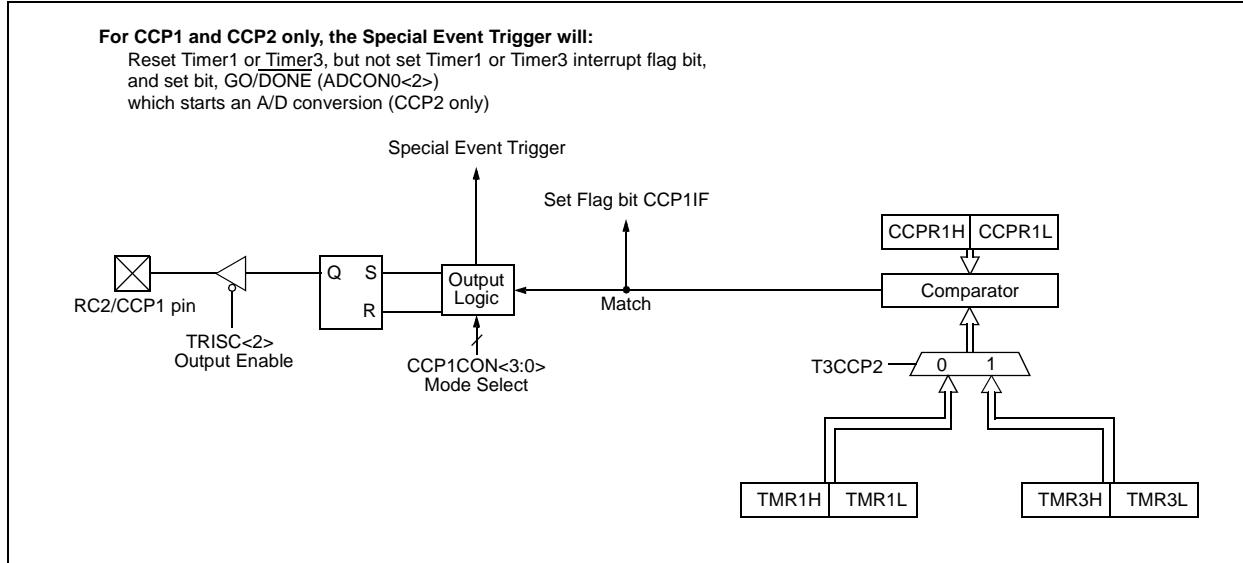


TABLE 16-2: REGISTERS ASSOCIATED WITH CAPTURE, COMPARE, TIMER1 AND TIMER3

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
RCON	IPEN	—	—	RI	TO	PD	POR	BOR	0--1 11qq	0--q quuu
PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	0111 1111
PIR2	—	CMIE	—	EEIE	BCLIF	LVDIF	TMR3IF	CCP2IF	-0-0 0000	--0 0000
PIE2	—	CMIF	—	EEIF	BCLIE	LVDIE	TMR3IE	CCP2IE	-0-0 0000	--0 0000
IPR2	—	CMIP	—	EEIP	BCLIP	LVDIP	TMR3IP	CCP2IP	-1-1 1111	--1 1111
PIR3	—	—	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	--00 0000	--00 0000
PIE3	—	—	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	--00 0000	--00 0000
IPR3	—	—	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	--11 1111	--11 1111
TRISC	PORTC Data Direction Register								1111 1111	1111 1111
TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
T1CON	RD16	—	T1CKPS1	T1CKPS0	T1OSCEN	—	TMR1CS	TMR1ON	0-00 0000	u-uu uuuu
TMR3H	Timer3 Register High Byte								xxxx xxxx	uuuu uuuu
TMR3L	Timer3 Register Low Byte								xxxx xxxx	uuuu uuuu
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	—	TMR3CS	TMR3ON	0000 0000	uuuu uuuu
CCPRxL ⁽¹⁾	Capture/Compare/PWM Register x (LSB)								xxxx xxxx	uuuu uuuu
CCPRxH ⁽¹⁾	Capture/Compare/PWM Register x (MSB)								xxxx xxxx	uuuu uuuu
CCPxCON ⁽¹⁾	—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'.

Shaded cells are not used by Capture and Compare, Timer1 or Timer3.

Note 1: Generic term for all of the identical registers of this name for all CCP modules, where 'x' identifies the individual module (CCP1 through CCP5). Bit assignments and RESET values for all registers of the same generic name are identical.

16.4 PWM Mode

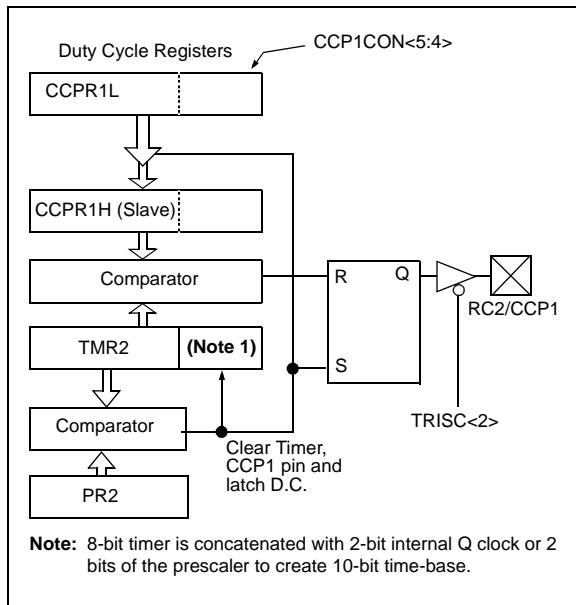
In Pulse Width Modulation (PWM) mode, the CCP1 pin produces up to a 10-bit resolution PWM output. Since the CCP1 pin is multiplexed with the PORTC data latch, the TRISC<2> bit must be cleared to make the CCP1 pin an output.

Note: Clearing the CCP1CON register will force the CCP1 PWM output latch to the default low level. This is not the PORTC I/O data latch.

Figure 16-4 shows a simplified block diagram of the CCP module in PWM mode.

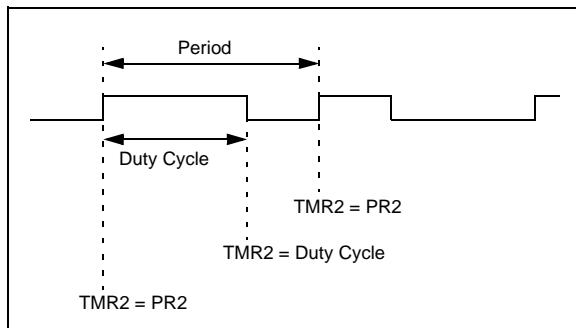
For a step-by-step procedure on how to set up the CCP module for PWM operation, see Section 16.4.3.

FIGURE 16-4: SIMPLIFIED PWM BLOCK DIAGRAM



A PWM output (Figure 16-5) has a time-base (period) and a time that the output stays high (duty cycle). The frequency of the PWM is the inverse of the period (1/period).

FIGURE 16-5: PWM OUTPUT



16.4.1 PWM PERIOD

The PWM period is specified by writing to the PR2 register. The PWM period can be calculated using the following formula:

$$\text{PWM period} = (\text{PR2} + 1) \cdot 4 \cdot \text{Tosc} \cdot (\text{TMR2 prescale value})$$

PWM frequency is defined as $1 / [\text{PWM period}]$.

When TMR2 is equal to PR2, the following three events occur on the next increment cycle:

- TMR2 is cleared
- The CCP1 pin is set (exception: if PWM duty cycle = 0%, the CCP1 pin will not be set)
- The PWM duty cycle is latched from CCPR1L into CCPR1H

Note: The Timer2 and Timer4 postscalers (see Section 13.0) are not used in the determination of the PWM frequency. The postscaler could be used to have a servo update rate at a different frequency than the PWM output.

16.4.2 PWM DUTY CYCLE

The PWM duty cycle is specified by writing to the CCPR1L register and to the CCP1CON<5:4> bits. Up to 10-bit resolution is available. The CCPR1L contains the eight MSbs and the CCP1CON<5:4> contains the two LSbs. This 10-bit value is represented by CCPR1L:CCP1CON<5:4>. The following equation is used to calculate the PWM duty cycle in time:

$$\text{PWM duty cycle} = (\text{CCPR1L:CCP1CON<5:4>} \cdot \text{Tosc} \cdot (\text{TMR2 prescale value}))$$

CCPR1L and CCP1CON<5:4> can be written to at any time, but the duty cycle value is not latched into CCPR1H until after a match between PR2 and TMR2 occurs (i.e., the period is complete). In PWM mode, CCPR1H is a read only register.

The CCPR1H register and a 2-bit internal latch are used to double buffer the PWM duty cycle. This double buffering is essential for glitchless PWM operation.

When the CCPR1H and 2-bit latch match TMR2 concatenated with an internal 2-bit Q clock or 2 bits of the TMR2 prescaler, the CCP1 pin is cleared.

The maximum PWM resolution (bits) for a given PWM frequency is given by the equation:

$$\text{PWM Resolution (max)} = \frac{\log\left(\frac{\text{FOSC}}{\text{FPWM}}\right)}{\log(2)} \text{ bits}$$

Note: If the PWM duty cycle value is longer than the PWM period, the CCP1 pin will not be cleared.

16.4.3 SETUP FOR PWM OPERATION

The following steps should be taken when configuring the CCP module for PWM operation:

1. Set the PWM period by writing to the PR2 register.
2. Set the PWM duty cycle by writing to the CCPR1L register and CCP1CON<5:4> bits.
3. Make the CCP1 pin an output by clearing the TRISC<2> bit.
4. Set the TMR2 prescale value and enable Timer2 by writing to T2CON.
5. Configure the CCP1 module for PWM operation.

TABLE 16-3: EXAMPLE PWM FREQUENCIES AND RESOLUTIONS AT 40 MHz

PWM Frequency	2.44 kHz	9.77 kHz	39.06 kHz	156.25 kHz	312.50 kHz	416.67 kHz
Timer Prescaler (1, 4, 16)	16	4	1	1	1	1
PR2 Value	FFh	FFh	FFh	3Fh	1Fh	17h
Maximum Resolution (bits)	14	12	10	8	7	6.58

TABLE 16-4: REGISTERS ASSOCIATED WITH PWM, TIMER2 AND TIMER4

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
RCON	IPEN	—	—	RI	TO	PD	POR	BOR	0-1 11qq	0--q quuu
PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	0111 1111
PIR2	—	CMIE	—	EEIE	BCLIF	LVDIF	TMR3IF	CCP2IF	-0-0 0000	--0 0000
PIE2	—	CMIF	—	EEIF	BCLIE	LVDIE	TMR3IE	CCP2IE	-0-0 0000	--0 0000
IPR2	—	CMIP	—	EEIP	BCLIP	LVDIP	TMR3IP	CCP2IP	-1-1 1111	--1 1111
PIR3	—	—	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	--00 0000	--00 0000
PIE3	—	—	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	--00 0000	--00 0000
IPR3	—	—	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	--11 1111	--11 1111
TMR2	Timer2 Module Register							0000 0000	0000 0000	
PR2	Timer2 Module Period Register							1111 1111	1111 1111	
T2CON	—	T2OUTPS3	T2OUTPS2	T2OUTPS1	T2OUTPS0	TMR2ON	T2CKPS1	T2CKPS0	-000 0000	-000 0000
T3CON	RD16	T3CCP2	T3CKPS1	T3CKPS0	T3CCP1	T3SYNC	TMR3CS	TMR3ON	0000 0000	uuuu uuuu
TMR4	Timer4 Register							0000 0000	uuuu uuuu	
PR4	Timer4 Period Register							1111 1111	uuuu uuuu	
T4CON	—	T4OUTPS3	T4OUTPS2	T4OUTPS1	T4OUTPS0	TMR4ON	T4CKPS1	T4CKPS0	-000 0000	uuuu uuuu
CCPRxL ⁽¹⁾	Capture/Compare/PWM Register x (LSB)							xxxx xxxx	uuuu uuuu	
CCPRxH ⁽¹⁾	Capture/Compare/PWM Register x (MSB)							xxxx xxxx	uuuu uuuu	
CCPxCON ⁽¹⁾	—	—	DCxB1	DCxB0	CCPxM3	CCPxM2	CCPxM1	CCPxM0	--00 0000	--00 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by PWM, Timer2 or Timer4.

Note 1: Generic term for all of the identical registers of this name for all CCP modules, where 'x' identifies the individual module (CCP1 through CCP5). Bit assignments and RESET values for all registers of the same generic name are identical.

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NOTES:

17.0 MASTER SYNCHRONOUS SERIAL PORT (MSSP) MODULE

17.1 Master SSP (MSSP) Module Overview

The Master Synchronous Serial Port (MSSP) module is a serial interface, useful for communicating with other peripheral or microcontroller devices. These peripheral devices may be serial EEPROMs, shift registers, display drivers, A/D converters, etc. The MSSP module can operate in one of two modes:

- Serial Peripheral Interface (SPI)
- Inter-Integrated Circuit (I^2C)
 - Full Master mode
 - Slave mode (with general address call)

The I^2C interface supports the following modes in hardware:

- Master mode
- Multi-Master mode
- Slave mode

17.2 Control Registers

The MSSP module has three associated registers. These include a status register (SSPSTAT) and two control registers (SSPCON1 and SSPCON2). The use of these registers and their individual configuration bits differ significantly, depending on whether the MSSP module is operated in SPI or I^2C mode.

Additional details are provided under the individual sections.

17.3 SPI Mode

The SPI mode allows 8 bits of data to be synchronously transmitted and received simultaneously. All four modes of SPI are supported. To accomplish communication, typically three pins are used:

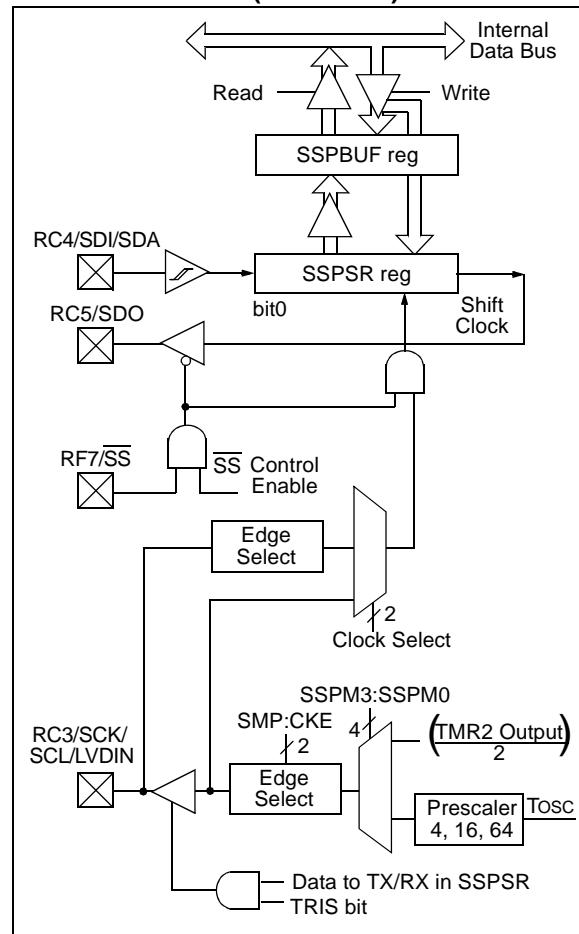
- Serial Data Out (SDO) - RC5/SDO
- Serial Data In (SDI) - RC4/SDI/SDA
- Serial Clock (SCK) - RC3/SCK/SCL/LVDIN

Additionally, a fourth pin may be used when in a Slave mode of operation:

- Slave Select (\overline{SS}) - RF7/ \overline{SS}

Figure 17-1 shows the block diagram of the MSSP module when operating in SPI mode.

FIGURE 17-1: MSSP BLOCK DIAGRAM (SPI MODE)



17.3.1 REGISTERS

The MSSP module has four registers for SPI mode operation. These are:

- MSSP Control Register1 (SSPCON1)
- MSSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- MSSP Shift Register (SSPSR) - Not directly accessible

SSPCON1 and SSPSTAT are the control and status registers in SPI mode operation. The SSPCON1 register is readable and writable. The lower 6 bits of the SSPSTAT are read only. The upper two bits of the SSPSTAT are read/write.

SSPSR is the shift register used for shifting data in or out. SSPBUF is the buffer register to which data bytes are written to or read from.

In receive operations, SSPSR and SSPBUF together create a double buffered receiver. When SSPSR receives a complete byte, it is transferred to SSPBUF and the SSPIF interrupt is set.

During transmission, the SSPBUF is not double buffered. A write to SSPBUF will write to both SSPBUF and SSPSR.

REGISTER 17-1: SSPSTAT: MSSP STATUS REGISTER (SPI MODE)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/A	P	S	R/W	UA	BF
bit 7							bit 0

bit 7 **SMP:** Sample bit

SPI Master mode:

1 = Input data sampled at end of data output time
0 = Input data sampled at middle of data output time

SPI Slave mode:

SMP must be cleared when SPI is used in Slave mode

bit 6 **CKE:** SPI Clock Edge Select bit

When CKP = 0:

1 = Data transmitted on rising edge of SCK
0 = Data transmitted on falling edge of SCK

When CKP = 1:

1 = Data transmitted on falling edge of SCK
0 = Data transmitted on rising edge of SCK

bit 5 **D/A:** Data/Address bit

Used in I²C mode only

bit 4 **P:** STOP bit

Used in I²C mode only. This bit is cleared when the MSSP module is disabled, SSPEN is cleared.

bit 3 **S:** START bit

Used in I²C mode only

bit 2 **R/W:** Read/Write bit information

Used in I²C mode only

bit 1 **UA:** Update Address bit

Used in I²C mode only

bit 0 **BF:** Buffer Full Status bit (Receive mode only)

1 = Receive complete, SSPBUF is full
0 = Receive not complete, SSPBUF is empty

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

REGISTER 17-2: SSPCON1: MSSP CONTROL REGISTER1 (SPI MODE)

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 |
| bit 7 | | | | | | | bit 0 |

- bit 7 **WCOL:** Write Collision Detect bit (Transmit mode only)
 1 = The SSPBUF register is written while it is still transmitting the previous word
 (must be cleared in software)
 0 = No collision
- bit 6 **SSPOV:** Receive Overflow Indicator bit
SPI Slave mode:
 1 = A new byte is received while the SSPBUF register is still holding the previous data. In case of overflow, the data in SSPSR is lost. Overflow can only occur in Slave mode. The user must read the SSPBUF, even if only transmitting data, to avoid setting overflow (must be cleared in software).
 0 = No overflow
Note: In Master mode, the overflow bit is not set, since each new reception (and transmission) is initiated by writing to the SSPBUF register.
- bit 5 **SSPEN:** Synchronous Serial Port Enable bit
 1 = Enables serial port and configures SCK, SDO, SDI, and \overline{SS} as serial port pins
 0 = Disables serial port and configures these pins as I/O port pins
Note: When enabled, these pins must be properly configured as input or output.
- bit 4 **CKP:** Clock Polarity Select bit
 1 = IDLE state for clock is a high level
 0 = IDLE state for clock is a low level
- bit 3-0 **SSPM3:SSPM0:** Synchronous Serial Port Mode Select bits
 0101 = SPI Slave mode, clock = SCK pin, \overline{SS} pin control disabled, \overline{SS} can be used as I/O pin
 0100 = SPI Slave mode, clock = SCK pin, SS pin control enabled
 0011 = SPI Master mode, clock = TMR2 output/2
 0010 = SPI Master mode, clock = Fosc/64
 0001 = SPI Master mode, clock = Fosc/16
 0000 = SPI Master mode, clock = Fosc/4
Note: Bit combinations not specifically listed here are either reserved, or implemented in I²C mode only.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

17.3.2 OPERATION

When initializing the SPI, several options need to be specified. This is done by programming the appropriate control bits (SSPCON1<5:0>) and SSPSTAT<7:6>. These control bits allow the following to be specified:

- Master mode (SCK is the clock output)
- Slave mode (SCK is the clock input)
- Clock Polarity (IDLE state of SCK)
- Data input sample phase (middle or end of data output time)
- Clock edge (output data on rising/falling edge of SCK)
- Clock Rate (Master mode only)
- Slave Select mode (Slave mode only)

The MSSP consists of a transmit/receive Shift Register (SSPSR) and a buffer register (SSPBUF). The SSPSR shifts the data in and out of the device, MSb first. The SSPBUF holds the data that was written to the SSPSR, until the received data is ready. Once the 8 bits of data have been received, that byte is moved to the SSPBUF register. Then the buffer full detect bit, BF (SSPSTAT<0>), and the interrupt flag bit, SSPIF, are set. This double buffering of the received data (SSPBUF) allows the next byte to start reception before

reading the data that was just received. Any write to the SSPBUF register during transmission/reception of data will be ignored, and the write collision detect bit, WCOL (SSPCON1<7>), will be set. User software must clear the WCOL bit so that it can be determined if the following write(s) to the SSPBUF register completed successfully.

When the application software is expecting to receive valid data, the SSPBUF should be read before the next byte of data to transfer is written to the SSPBUF. Buffer full bit, BF (SSPSTAT<0>), indicates when SSPBUF has been loaded with the received data (transmission is complete). When the SSPBUF is read, the BF bit is cleared. This data may be irrelevant if the SPI is only a transmitter. Generally, the MSSP Interrupt is used to determine when the transmission/reception has completed. The SSPBUF must be read and/or written. If the interrupt method is not going to be used, then software polling can be done to ensure that a write collision does not occur. Example 17-1 shows the loading of the SSPBUF (SSPSR) for data transmission.

The SSPSR is not directly readable or writable, and can only be accessed by addressing the SSPBUF register. Additionally, the MSSP status register (SSPSTAT) indicates the various status conditions.

EXAMPLE 17-1: LOADING THE SSPBUF (SSPSR) REGISTER

```
LOOP BTFS  SSPSTAT, BF      ;Has data been received(transmit complete)?  
BRA   LOOP                  ;No  
MOVF  SSPBUF, W              ;WREG reg = contents of SSPBUF  
MOVWF RXDATA                ;Save in user RAM, if data is meaningful  
MOVF  TXDATA, W              ;W reg = contents of TXDATA  
MOVWF SSPBUF                ;New data to xmit
```

17.3.3 ENABLING SPI I/O

To enable the serial port, SSP Enable bit, SSPEN (SSPCON1<5>), must be set. To reset or reconfigure SPI mode, clear the SSPEN bit, re-initialize the SSPCON registers, and then set the SSPEN bit. This configures the SDI, SDO, SCK, and SS pins as serial port pins. For the pins to behave as the serial port function, some must have their data direction bits (in the TRIS register) appropriately programmed as follows:

- SDI is automatically controlled by the SPI module
- SDO must have TRISC<5> bit cleared
- SCK (Master mode) must have TRISC<3> bit cleared
- SCK (Slave mode) must have TRISC<3> bit set
- SS must have TRISF<7> bit set

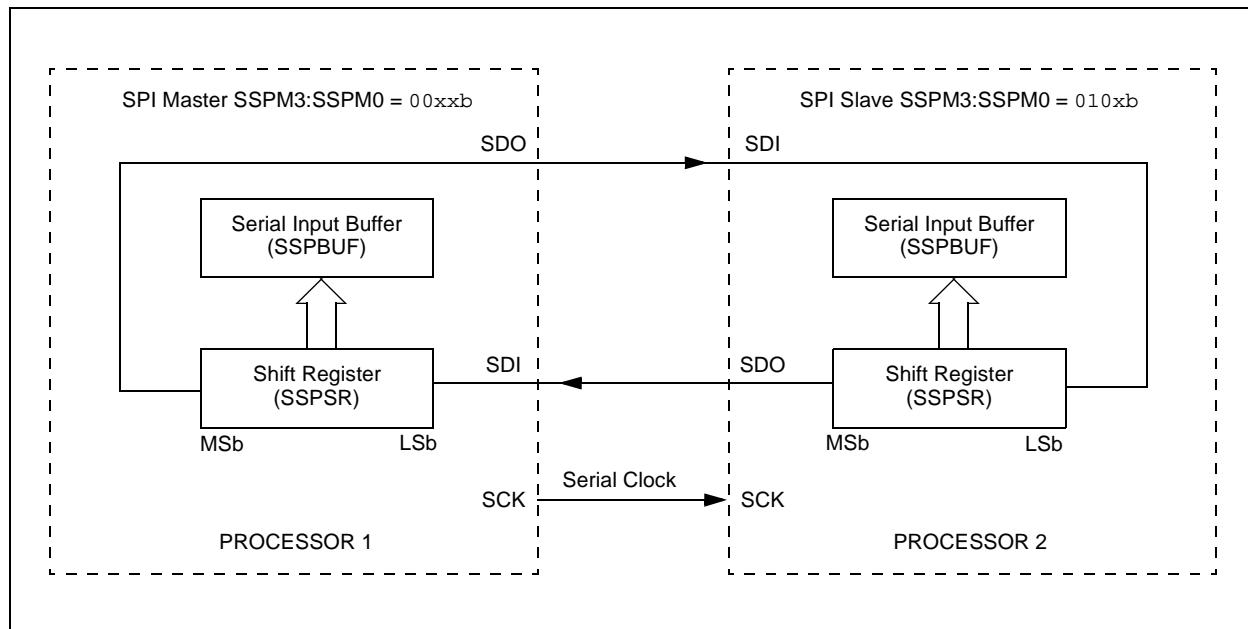
Any serial port function that is not desired may be overridden by programming the corresponding data direction (TRIS) register to the opposite value.

17.3.4 TYPICAL CONNECTION

Figure 17-2 shows a typical connection between two microcontrollers. The master controller (Processor 1) initiates the data transfer by sending the SCK signal. Data is shifted out of both shift registers on their programmed clock edge, and latched on the opposite edge of the clock. Both processors should be programmed to the same Clock Polarity (CKP), then both controllers would send and receive data at the same time. Whether the data is meaningful (or dummy data) depends on the application software. This leads to three scenarios for data transmission:

- Master sends data — Slave sends dummy data
- Master sends data — Slave sends data
- Master sends dummy data — Slave sends data

FIGURE 17-2: SPI MASTER/SLAVE CONNECTION



17.3.5 MASTER MODE

The master can initiate the data transfer at any time because it controls the SCK. The master determines when the slave (Processor 2, Figure 17-2) is to broadcast data by the software protocol.

In Master mode, the data is transmitted/received as soon as the SSPBUF register is written to. If the SPI is only going to receive, the SDO output could be disabled (programmed as an input). The SSPSR register will continue to shift in the signal present on the SDI pin at the programmed clock rate. As each byte is received, it will be loaded into the SSPBUF register as if a normal received byte (interrupts and status bits appropriately set). This could be useful in receiver applications as a "Line Activity Monitor" mode.

The clock polarity is selected by appropriately programming the CKP bit (SSPCON1<4>). This then, would give waveforms for SPI communication as shown in

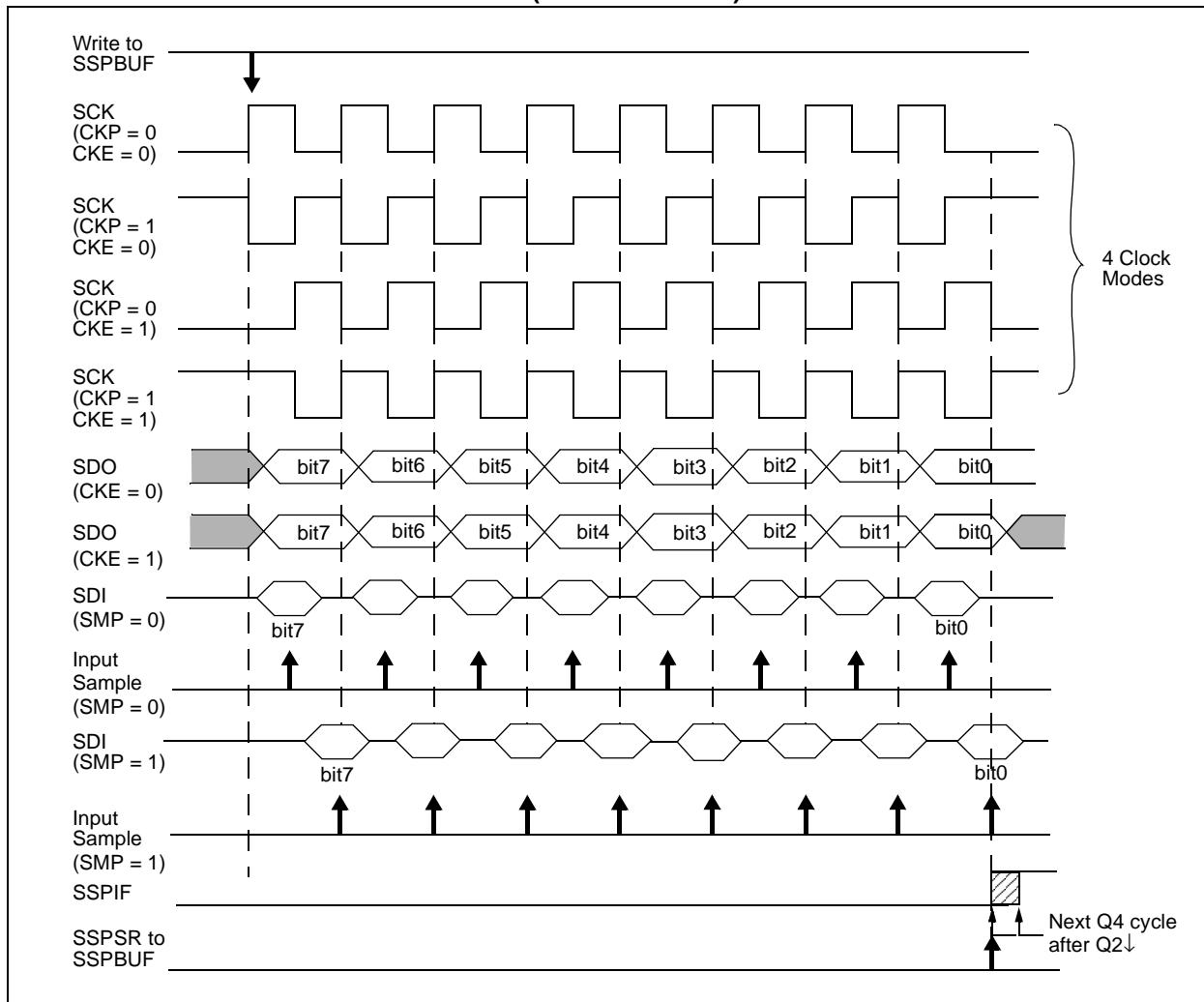
Figure 17-3, Figure 17-5, and Figure 17-6, where the MSB is transmitted first. In Master mode, the SPI clock rate (bit rate) is user programmable to be one of the following:

- Fosc/4 (or Tcy)
- Fosc/16 (or 4 • Tcy)
- Fosc/64 (or 16 • Tcy)
- Timer2 output/2

This allows a maximum data rate (at 40 MHz) of 10.00 Mbps.

Figure 17-3 shows the waveforms for Master mode. When the CKE bit is set, the SDO data is valid before there is a clock edge on SCK. The change of the input sample is shown based on the state of the SMP bit. The time when the SSPBUF is loaded with the received data is shown.

FIGURE 17-3: SPI MODE WAVEFORM (MASTER MODE)



17.3.6 SLAVE MODE

In Slave mode, the data is transmitted and received as the external clock pulses appear on SCK. When the last bit is latched, the SSPIF interrupt flag bit is set.

While in Slave mode, the external clock is supplied by the external clock source on the SCK pin. This external clock must meet the minimum high and low times as specified in the electrical specifications.

While in SLEEP mode, the slave can transmit/receive data. When a byte is received, the device will wake-up from SLEEP.

17.3.7 SLAVE SELECT SYNCHRONIZATION

The SS pin allows a Synchronous Slave mode. The SPI must be in Slave mode with SS pin control enabled (SSP_{CON1<3:0>} = 04h). The pin must not be driven low for the SS pin to function as an input. The Data Latch must be high. When the SS pin is low, transmission and reception are enabled and the SDO pin is driven. When the SS pin goes high,

the SDO pin is no longer driven, even if in the middle of a transmitted byte, and becomes a floating output. External pull-up/pull-down resistors may be desirable, depending on the application.

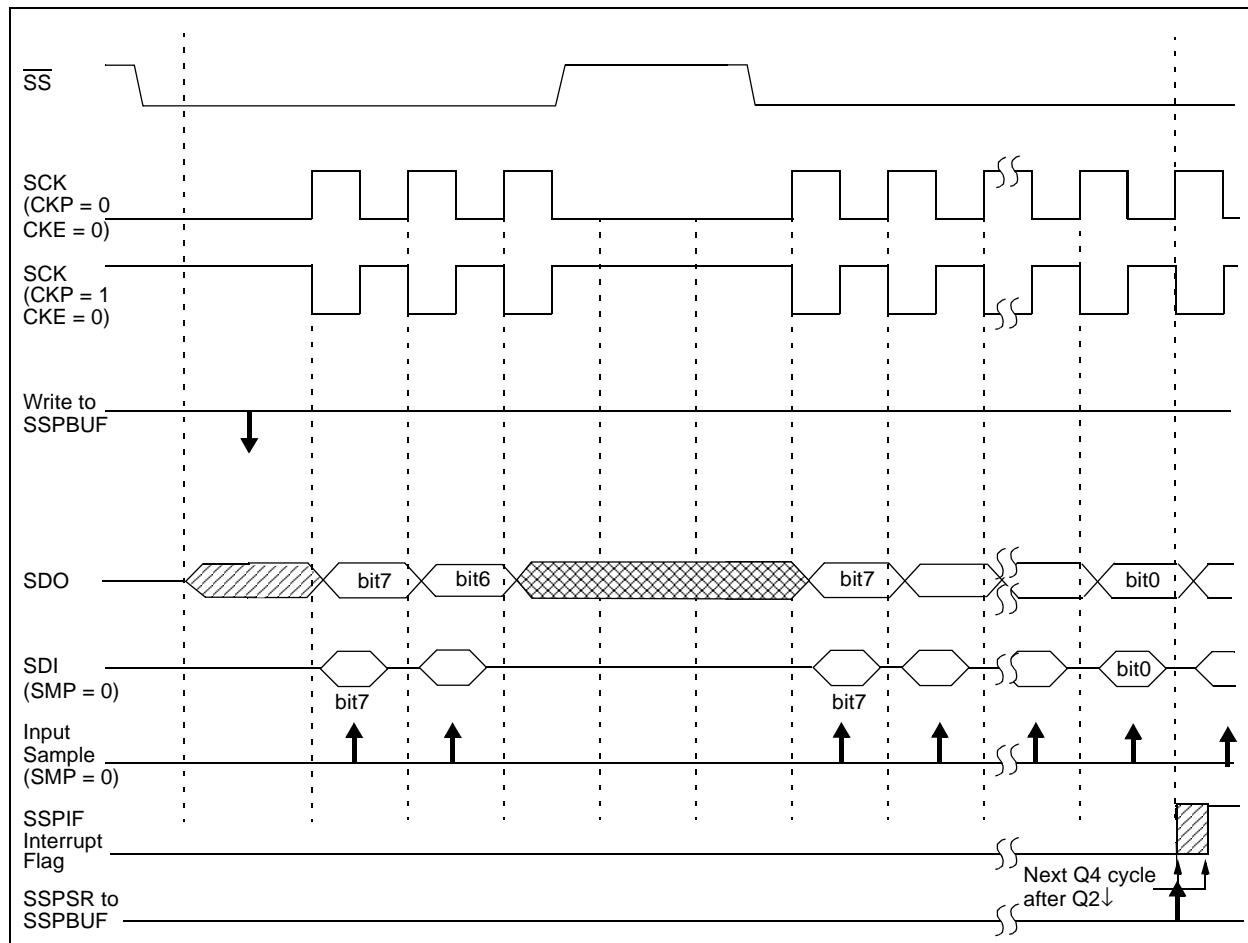
Note 1: When the SPI is in Slave mode with SS pin control enabled (SSP_{CON1<3:0>} = 0100), the SPI module will reset if the SS pin is set to VDD.

2: If the SPI is used in Slave mode with CKE set, then the SS pin control must be enabled.

When the SPI module resets, the bit counter is forced to 0. This can be done by either forcing the SS pin to a high level or clearing the SSPEN bit.

To emulate two-wire communication, the SDO pin can be connected to the SDI pin. When the SPI needs to operate as a receiver, the SDO pin can be configured as an input. This disables transmissions from the SDO. The SDI can always be left as an input (SDI function), since it cannot create a bus conflict.

FIGURE 17-4: SLAVE SYNCHRONIZATION WAVEFORM



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FIGURE 17-5: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 0)

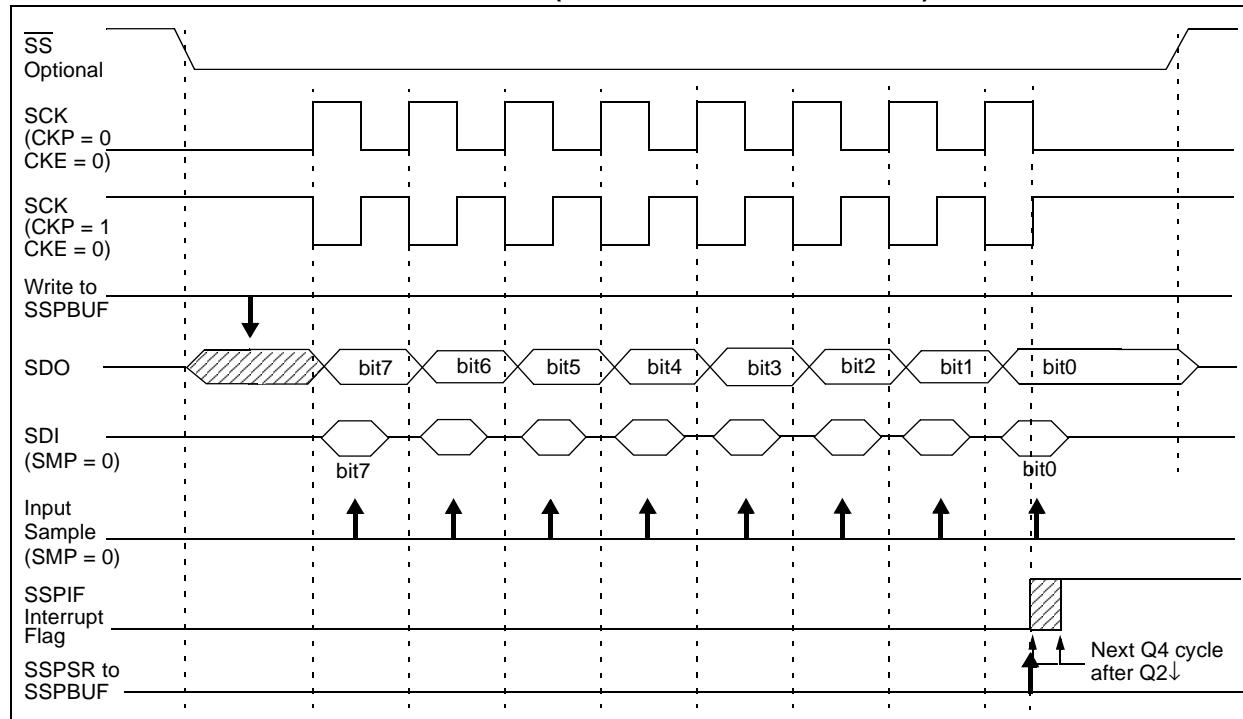
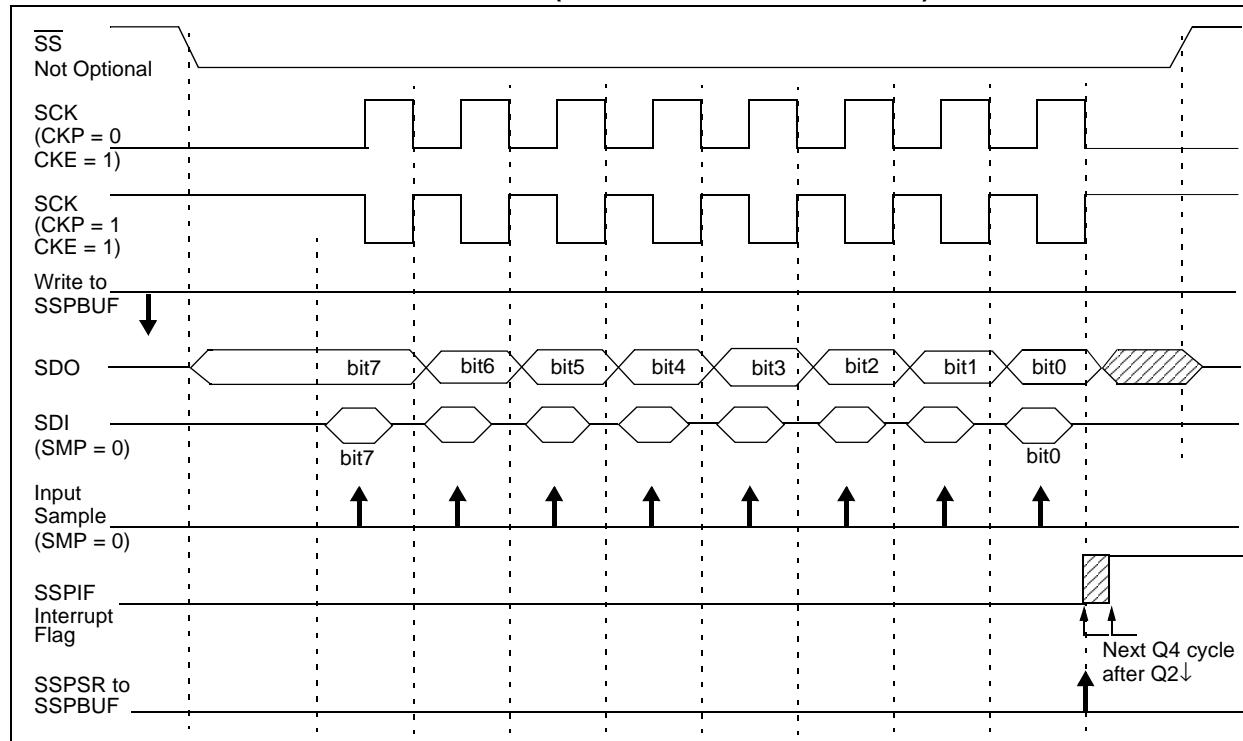


FIGURE 17-6: SPI MODE WAVEFORM (SLAVE MODE WITH CKE = 1)



17.3.8 SLEEP OPERATION

In Master mode, all module clocks are halted and the transmission/reception will remain in that state until the device wakes from SLEEP. After the device returns to normal mode, the module will continue to transmit/receive data.

In Slave mode, the SPI transmit/receive shift register operates asynchronously to the device. This allows the device to be placed in SLEEP mode and data to be shifted into the SPI transmit/receive shift register. When all 8 bits have been received, the MSSP interrupt flag bit will be set and if enabled, will wake the device from SLEEP.

17.3.9 EFFECTS OF A RESET

A RESET disables the MSSP module and terminates the current transfer.

17.3.10 BUS MODE COMPATIBILITY

Table 17-1 shows the compatibility between the standard SPI modes and the states the CKP and CKE control bits.

TABLE 17-1: SPI BUS MODES

Standard SPI Mode Terminology	Control Bits State	
	CKP	CKE
0, 0	0	1
0, 1	0	0
1, 0	1	1
1, 1	1	0

There is also a SMP bit, which controls when the data is sampled.

TABLE 17-2: REGISTERS ASSOCIATED WITH SPI OPERATION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	0111 1111
TRISC	PORTC Data Direction Register								1111 1111	1111 1111
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	1111 1111	uuuu uuuu
SSPBUF	Synchronous Serial Port Receive Buffer/Transmit Register								xxxx xxxx	uuuu uuuu
SSPCON	WCOL	SSPOV	SSPEN	CKP	SSPM3	SSPM2	SSPM1	SSPM0	0000 0000	0000 0000
SSPSTAT	SMP	CKE	D/A	P	S	R/W	UA	BF	0000 0000	0000 0000

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the MSSP in SPI mode.

17.4 I²C Mode

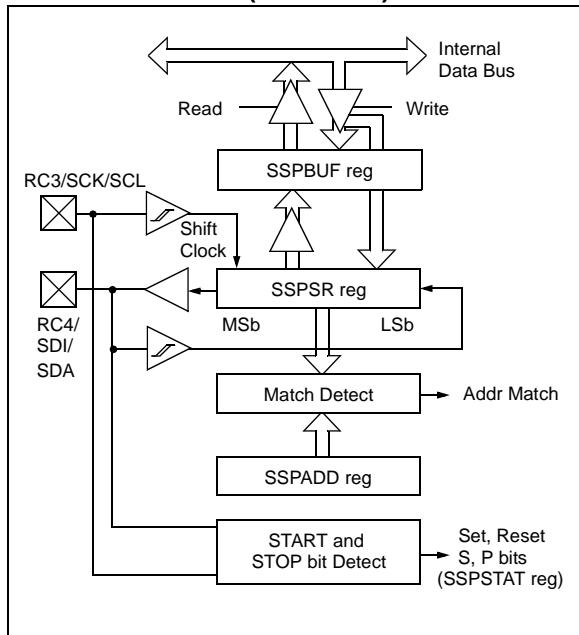
The MSSP module in I²C mode fully implements all master and slave functions (including general call support) and provides interrupts on START and STOP bits in hardware to determine a free bus (multi-master function). The MSSP module implements the standard mode specifications, as well as 7-bit and 10-bit addressing.

Two pins are used for data transfer:

- Serial clock (SCL) - RC3/SCK/SCL
- Serial data (SDA) - RC4/SDI/SDA

The user must configure these pins as inputs or outputs through the TRISC<4:3> bits.

FIGURE 17-7: MSSP BLOCK DIAGRAM (I²C MODE)



17.4.1 REGISTERS

The MSSP module has six registers for I²C operation. These are:

- MSSP Control Register1 (SSPCON1)
- MSSP Control Register2 (SSPCON2)
- MSSP Status Register (SSPSTAT)
- Serial Receive/Transmit Buffer (SSPBUF)
- MSSP Shift Register (SSPSR) - Not directly accessible
- MSSP Address Register (SSPADD)

SSPCON, SSPCON2 and SSPSTAT are the control and status registers in I²C mode operation. The SSPCON and SSPCON2 registers are readable and writable. The lower 6 bits of the SSPSTAT are read only. The upper two bits of the SSPSTAT are read/write.

SSPSR is the shift register used for shifting data in or out. SSPBUF is the buffer register to which data bytes are written to or read from.

SSPADD register holds the slave device address when the SSP is configured in I²C Slave mode. When the SSP is configured in Master mode, the lower seven bits of SSPADD act as the baud rate generator reload value.

In receive operations, SSPSR and SSPBUF together, create a double buffered receiver. When SSPSR receives a complete byte, it is transferred to SSPBUF and the SSPIF interrupt is set.

During transmission, the SSPBUF is not double buffered. A write to SSPBUF will write to both SSPBUF and SSPSR.

REGISTER 17-3: SSPSTAT: MSSP STATUS REGISTER (I²C MODE)

R/W-0	R/W-0	R-0	R-0	R-0	R-0	R-0	R-0
SMP	CKE	D/A	P	S	R/W	UA	BF
bit 7	bit 0						

- bit 7 **SMP:** Slew Rate Control bit
In Master or Slave mode:
 1 = Slew rate control disabled for standard speed mode (100 kHz and 1 MHz)
 0 = Slew rate control enabled for high speed mode (400 kHz)
- bit 6 **CKE:** SMBus Select bit
In Master or Slave mode:
 1 = Enable SMBus specific inputs
 0 = Disable SMBus specific inputs
- bit 5 **D/A:** Data/Address bit
In Master mode:
 Reserved
In Slave mode:
 1 = Indicates that the last byte received or transmitted was data
 0 = Indicates that the last byte received or transmitted was address
- bit 4 **P:** STOP bit
 1 = Indicates that a STOP bit has been detected last
 0 = STOP bit was not detected last
Note: This bit is cleared on RESET and when SSPEN is cleared.
- bit 3 **S:** START bit
 1 = Indicates that a START bit has been detected last
 0 = START bit was not detected last
Note: This bit is cleared on RESET and when SSPEN is cleared.
- bit 2 **R/W:** Read/Write bit Information (I²C mode only)
In Slave mode:
 1 = Read
 0 = Write
Note: This bit holds the R/W bit information following the last address match. This bit is only valid from the address match to the next START bit, STOP bit, or not ACK bit.
In Master mode:
 1 = Transmit is in progress
 0 = Transmit is not in progress
Note: ORing this bit with SEN, RSEN, PEN, RCEN, or ACKEN will indicate if the MSSP is in IDLE mode.
- bit 1 **UA:** Update Address bit (10-bit Slave mode only)
 1 = Indicates that the user needs to update the address in the SSPADD register
 0 = Address does not need to be updated
- bit 0 **BF:** Buffer Full Status bit
In Transmit mode:
 1 = Receive complete, SSPBUF is full
 0 = Receive not complete, SSPBUF is empty
In Receive mode:
 1 = Data transmit in progress (does not include the ACK and STOP bits), SSPBUF is full
 0 = Data transmit complete (does not include the ACK and STOP bits), SSPBUF is empty

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

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REGISTER 17-4: SSPCON1: MSSP CONTROL REGISTER1 (I²C MODE)

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| WCOL | SSPOV | SSPEN | CKP | SSPM3 | SSPM2 | SSPM1 | SSPM0 |

bit 7

bit 0

bit 7 **WCOL:** Write Collision Detect bit

In Master Transmit mode:

1 = A write to the SSPBUF register was attempted while the I²C conditions were not valid for a transmission to be started (must be cleared in software)

0 = No collision

In Slave Transmit mode:

1 = The SSPBUF register is written while it is still transmitting the previous word (must be cleared in software)

0 = No collision

In Receive mode (Master or Slave modes):

This is a "don't care" bit

bit 6 **SSPOV:** Receive Overflow Indicator bit

In Receive mode:

1 = A byte is received while the SSPBUF register is still holding the previous byte (must be cleared in software)

0 = No overflow

In Transmit mode:

This is a "don't care" bit in Transmit mode

bit 5 **SSPEN:** Synchronous Serial Port Enable bit

1 = Enables the serial port and configures the SDA and SCL pins as the serial port pins

0 = Disables serial port and configures these pins as I/O port pins

Note: When enabled, the SDA and SCL pins must be properly configured as input or output.

bit 4 **CKP:** SCK Release Control bit

In Slave mode:

1 = Release clock

0 = Holds clock low (clock stretch), used to ensure data setup time

In Master mode:

Unused in this mode

bit 3-0 **SSPM3:SSPM0:** Synchronous Serial Port Mode Select bits

1111 = I²C Slave mode, 10-bit address with START and STOP bit interrupts enabled

1110 = I²C Slave mode, 7-bit address with START and STOP bit interrupts enabled

1011 = I²C Firmware Controlled Master mode (Slave IDLE)

1000 = I²C Master mode, clock = Fosc / (4 * (SSPADD+1))

0111 = I²C Slave mode, 10-bit address

0110 = I²C Slave mode, 7-bit address

Note: Bit combinations not specifically listed here are either reserved, or implemented in SPI mode only.

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

REGISTER 17-5: SSPCON2: MSSP CONTROL REGISTER 2 (I²C MODE)

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
GCEN	ACKSTAT	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7				bit 0			

- bit 7 **GCEN:** General Call Enable bit (Slave mode only)
 1 = Enable interrupt when a general call address (0000h) is received in the SSPSR
 0 = General call address disabled
- bit 6 **ACKSTAT:** Acknowledge Status bit (Master Transmit mode only)
 1 = Acknowledge was not received from slave
 0 = Acknowledge was received from slave
- bit 5 **ACKDT:** Acknowledge Data bit (Master Receive mode only)
 1 = Not Acknowledge
 0 = Acknowledge
Note: Value that will be transmitted when the user initiates an Acknowledge sequence at the end of a receive.
- bit 4 **ACKEN:** Acknowledge Sequence Enable bit (Master Receive mode only)
 1 = Initiate Acknowledge sequence on SDA and SCL pins, and transmit ACKDT data bit.
 Automatically cleared by hardware.
 0 = Acknowledge sequence IDLE
- bit 3 **RCEN:** Receive Enable bit (Master Mode only)
 1 = Enables Receive mode for I²C
 0 = Receive IDLE
- bit 2 **PEN:** STOP Condition Enable bit (Master mode only)
 1 = Initiate STOP condition on SDA and SCL pins. Automatically cleared by hardware.
 0 = STOP condition IDLE
- bit 1 **RSEN:** Repeated START Condition Enabled bit (Master mode only)
 1 = Initiate Repeated START condition on SDA and SCL pins.
 Automatically cleared by hardware.
 0 = Repeated START condition IDLE
- bit 0 **SEN:** START Condition Enabled/Stretch Enabled bit
In Master mode:
 1 = Initiate START condition on SDA and SCL pins. Automatically cleared by hardware.
 0 = START condition IDLE
In Slave mode:
 1 = Clock stretching is enabled for both Slave Transmit and Slave Receive (stretch enabled)
 0 = Clock stretching is disabled

Note: For bits ACKEN, RCEN, PEN, RSEN, SEN: If the I²C module is not in the IDLE mode, this bit may not be set (no spooling) and the SSPBUF may not be written (or writes to the SSPBUF are disabled).

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

17.4.2 OPERATION

The MSSP module functions are enabled by setting MSSP Enable bit, SSPEN (SSPCON<5>).

The SSPCON1 register allows control of the I²C operation. Four mode selection bits (SSPCON<3:0>) allow one of the following I²C modes to be selected:

- I²C Master mode, clock = OSC/4 (SSPADD +1)
- I²C Slave mode (7-bit address)
- I²C Slave mode (10-bit address)
- I²C Slave mode (7-bit address), with START and STOP bit interrupts enabled
- I²C Slave mode (10-bit address), with START and STOP bit interrupts enabled
- I²C Firmware controlled master operation, slave is IDLE

Selection of any I²C mode, with the SSPEN bit set, forces the SCL and SDA pins to be open drain, provided these pins are programmed to inputs by setting the appropriate TRISC bits. To ensure proper operation of the module, pull-up resistors must be provided externally to the SCL and SDA pins.

17.4.3 SLAVE MODE

In Slave mode, the SCL and SDA pins must be configured as inputs (TRISC<4:3> set). The MSSP module will override the input state with the output data when required (slave-transmitter).

The I²C Slave mode hardware will always generate an interrupt on an address match. Through the mode select bits, the user can also choose to interrupt on START and STOP bits.

When an address is matched or the data transfer after an address match is received, the hardware automatically will generate the Acknowledge (ACK) pulse and load the SSPBUF register with the received value currently in the SSPSR register.

Any combination of the following conditions will cause the MSSP module not to give this ACK pulse:

- The buffer full bit BF (SSPSTAT<0>) was set before the transfer was received.
- The overflow bit SSPOV (SSPCON<6>) was set before the transfer was received.

In this case, the SSPSR register value is not loaded into the SSPBUF, but bit SSPIF (PIR1<3>) is set. The BF bit is cleared by reading the SSPBUF register, while bit SSPOV is cleared through software.

The SCL clock input must have a minimum high and low for proper operation. The high and low times of the I²C specification, as well as the requirement of the MSSP module, are shown in timing parameter #100 and parameter #101.

17.4.3.1 Addressing

Once the MSSP module has been enabled, it waits for a START condition to occur. Following the START condition, the 8-bits are shifted into the SSPSR register. All incoming bits are sampled with the rising edge of the clock (SCL) line. The value of register SSPSR<7:1> is compared to the value of the SSPADD register. The address is compared on the falling edge of the eighth clock (SCL) pulse. If the addresses match, and the BF and SSPOV bits are clear, the following events occur:

1. The SSPSR register value is loaded into the SSPBUF register.
2. The buffer full bit BF is set.
3. An $\overline{\text{ACK}}$ pulse is generated.
4. MSSP interrupt flag bit, SSPIF (PIR1<3>) is set (interrupt is generated, if enabled) on the falling edge of the ninth SCL pulse.

In 10-bit Address mode, two address bytes need to be received by the slave. The five Most Significant bits (MSbs) of the first address byte specify if this is a 10-bit address. Bit R/W (SSPSTAT<2>) must specify a write so the slave device will receive the second address byte. For a 10-bit address, the first byte would equal '11110 A9 A8 0', where 'A9' and 'A8' are the two MSbs of the address. The sequence of events for 10-bit address is as follows, with steps 7 through 9 for the slave-transmitter:

1. Receive first (high) byte of Address (bits SSPIF, BF and bit UA (SSPSTAT<1>) are set).
2. Update the SSPADD register with second (low) byte of Address (clears bit UA and releases the SCL line).
3. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
4. Receive second (low) byte of Address (bits SSPIF, BF, and UA are set).
5. Update the SSPADD register with the first (high) byte of Address. If match releases SCL line, this will clear bit UA.
6. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.
7. Receive Repeated START condition.
8. Receive first (high) byte of Address (bits SSPIF and BF are set).
9. Read the SSPBUF register (clears bit BF) and clear flag bit SSPIF.

17.4.3.2 Reception

When the R/W bit of the address byte is clear and an address match occurs, the R/W bit of the SSPSTAT register is cleared. The received address is loaded into the SSPBUF register and the SDA line is held low (ACK).

When the address byte overflow condition exists, then the No Acknowledge (ACK) pulse is given. An overflow condition is defined as either bit BF (SSPSTAT<0>) is set, or bit SSPOV (SSPCON1<6>) is set.

An MSSP interrupt is generated for each data transfer byte. Flag bit SSPIF (PIR1<3>) must be cleared in software. The SSPSTAT register is used to determine the status of the byte.

If SEN is enabled (SSPCON1<0>=1), RC3/SCK/SCL will be held low (clock stretch) following each data transfer. The clock must be released by setting bit CKP (SSPCON<4>). See Section 17.4.4 ("Clock Stretching"), for more detail.

17.4.3.3 Transmission

When the R/W bit of the incoming address byte is set and an address match occurs, the R/W bit of the SSPSTAT register is set. The received address is loaded into the SSPBUF register. The ACK pulse will be sent on the ninth bit and pin RC3/SCK/SCL is held low, regardless of SEN (see "Clock Stretching", Section 17.4.4, for more detail). By stretching the clock, the master will be unable to assert another clock pulse until the slave is done preparing the transmit data. The transmit data must be loaded into the SSPBUF register, which also loads the SSPSR register. Then pin RC3/SCK/SCL should be enabled by setting bit CKP (SSPCON1<4>). The eight data bits are shifted out on the falling edge of the SCL input. This ensures that the SDA signal is valid during the SCL high time (Figure 17-9).

The ACK pulse from the master-receiver is latched on the rising edge of the ninth SCL input pulse. If the SDA line is high (not ACK), then the data transfer is complete. In this case, when the ACK is latched by the slave, the slave logic is reset (resets SSPSTAT register) and the slave monitors for another occurrence of the START bit. If the SDA line was low (ACK), the next transmit data must be loaded into the SSPBUF register. Again, pin RC3/SCK/SCL must be enabled by setting bit CKP.

An MSSP interrupt is generated for each data transfer byte. The SSPIF bit must be cleared in software and the SSPSTAT register is used to determine the status of the byte. The SSPIF bit is set on the falling edge of the ninth clock pulse.

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FIGURE 17-8: I²C SLAVE MODE TIMING WITH SEN = 0 (RECEPTION, 7-BIT ADDRESS)

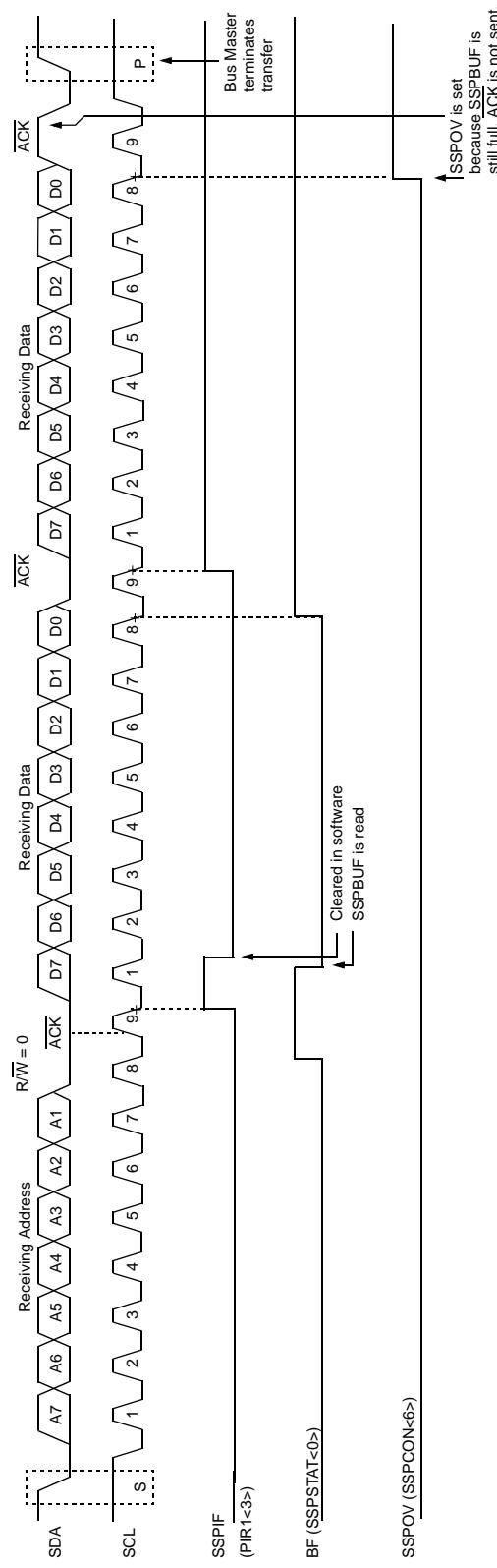
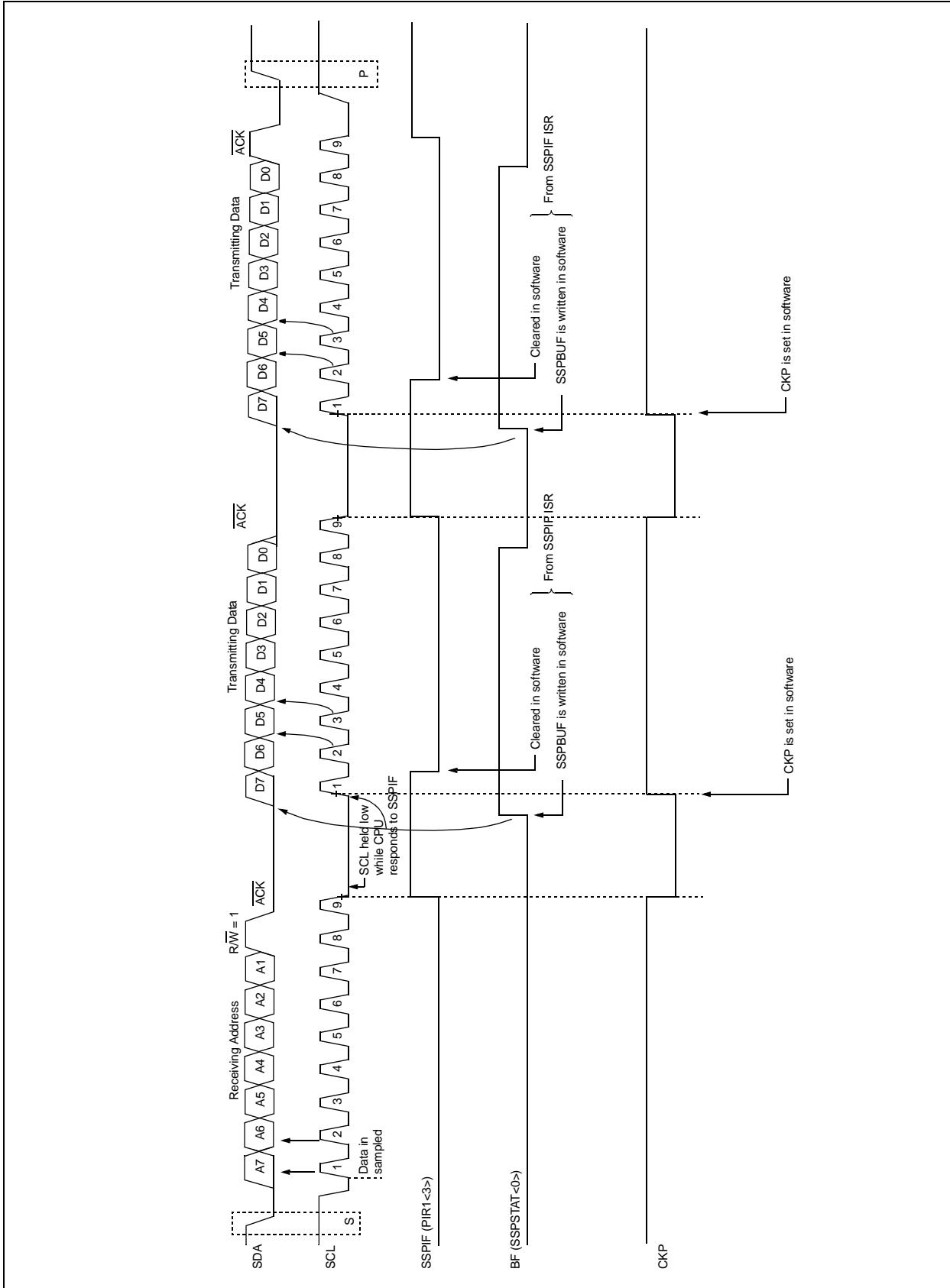


FIGURE 17-9: I²C SLAVE MODE TIMING (TRANSMISSION, 7-BIT ADDRESS)



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FIGURE 17-10: I²C SLAVE MODE TIMING WITH SEN = 0 (RECEPTION, 10-BIT ADDRESS)

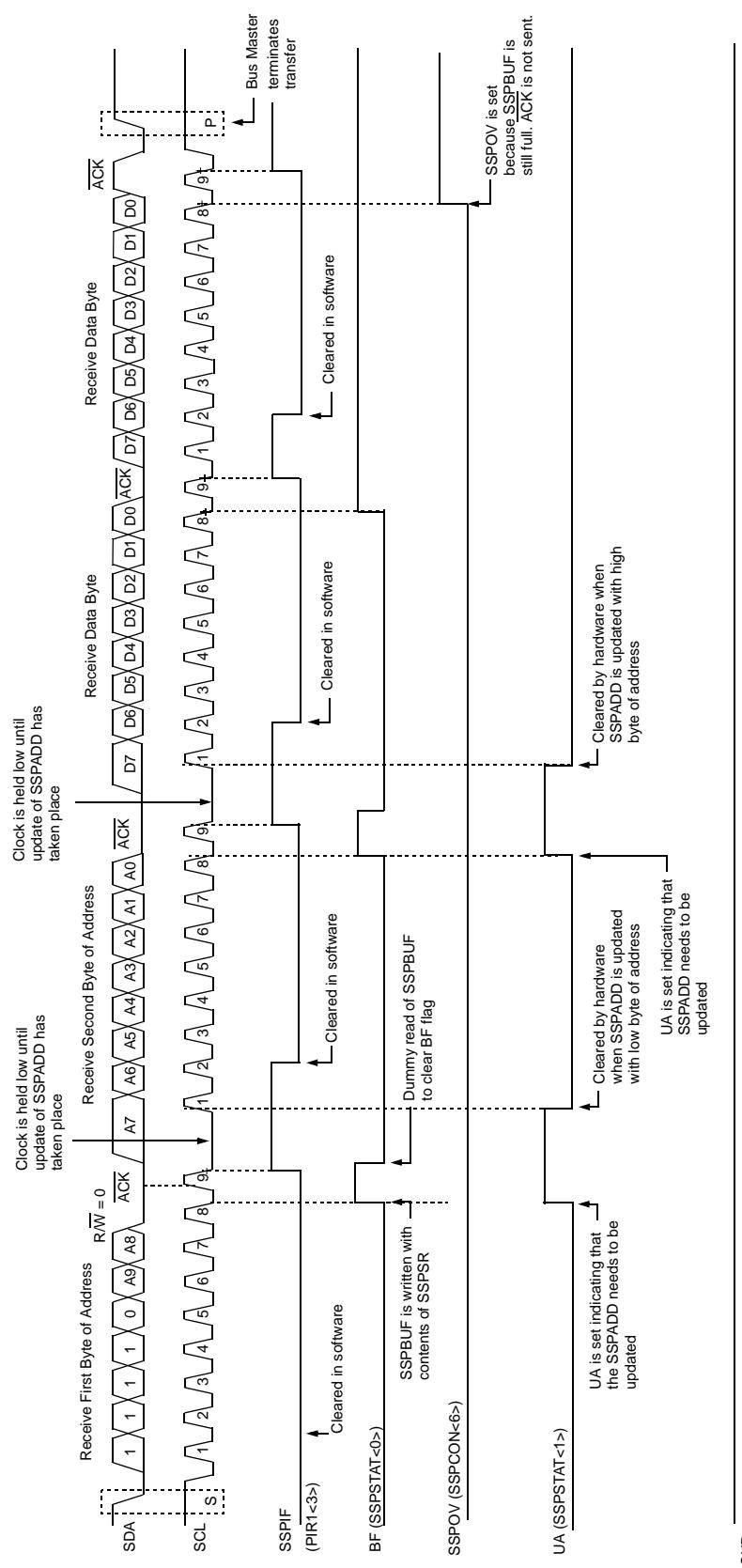
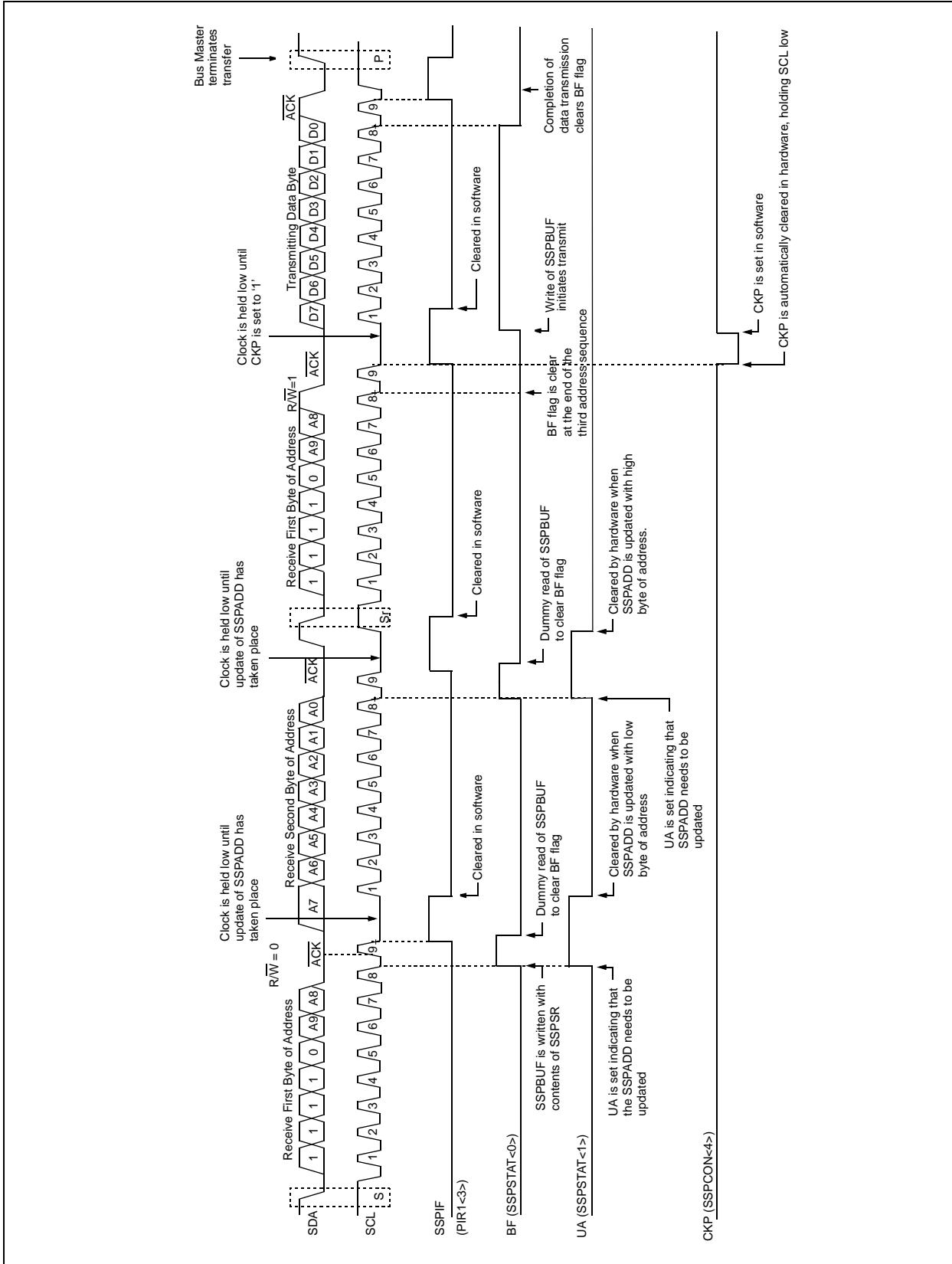


FIGURE 17-11: I²C SLAVE MODE TIMING (TRANSMISSION, 10-BIT ADDRESS)



17.4.4 CLOCK STRETCHING

Both 7- and 10-bit Slave modes implement automatic clock stretching during a transmit sequence.

The SEN bit (SSPCON2<0>) allows clock stretching to be enabled during receives. Setting SEN will cause the SCL pin to be held low at the end of each data receive sequence.

17.4.4.1 Clock Stretching for 7-bit Slave Receive Mode (SEN = 1)

In 7-bit Slave Receive mode, on the falling edge of the ninth clock at the end of the $\overline{\text{ACK}}$ sequence, if the BF bit is set, the CKP bit in the SSPCON1 register is automatically cleared, forcing the SCL output to be held low. The CKP being cleared to '0' will assert the SCL line low. The CKP bit must be set in the user's ISR before reception is allowed to continue. By holding the SCL line low, the user has time to service the ISR and read the contents of the SSPBUF before the master device can initiate another receive sequence. This will prevent buffer overruns from occurring (see Figure 17-13).

- Note 1:** If the user reads the contents of the SSPBUF before the falling edge of the ninth clock, thus clearing the BF bit, the CKP bit will not be cleared and clock stretching will not occur.
- 2:** The CKP bit can be set in software, regardless of the state of the BF bit. The user should be careful to clear the BF bit in the ISR before the next receive sequence, in order to prevent an overflow condition.

17.4.4.2 Clock Stretching for 10-bit Slave Receive Mode (SEN = 1)

In 10-bit Slave Receive mode, during the address sequence, clock stretching automatically takes place but CKP is not cleared. During this time, if the UA bit is set after the ninth clock, clock stretching is initiated. The UA bit is set after receiving the upper byte of the 10-bit address, and following the receive of the second byte of the 10-bit address with the R/W bit cleared to '0'. The release of the clock line occurs upon updating SSPADD. Clock stretching will occur on each data receive sequence as described in 7-bit mode.

- Note:** If the user polls the UA bit and clears it by updating the SSPADD register before the falling edge of the ninth clock occurs, and if the user hasn't cleared the BF bit by reading the SSPBUF register before that time, then the CKP bit will still NOT be asserted low. Clock stretching on the basis of the state of the BF bit only occurs during a data sequence, not an address sequence.

17.4.4.3 Clock Stretching for 7-bit Slave Transmit Mode

7-bit Slave Transmit mode implements clock stretching by clearing the CKP bit after the falling edge of the ninth clock, if the BF bit is clear. This occurs, regardless of the state of the SEN bit.

The user's ISR must set the CKP bit before transmission is allowed to continue. By holding the SCL line low, the user has time to service the ISR and load the contents of the SSPBUF before the master device can initiate another transmit sequence (see Figure 17-9).

- Note 1:** If the user loads the contents of SSPBUF, setting the BF bit before the falling edge of the ninth clock, the CKP bit will not be cleared and clock stretching will not occur.
- 2:** The CKP bit can be set in software, regardless of the state of the BF bit.

17.4.4.4 Clock Stretching for 10-bit Slave Transmit Mode

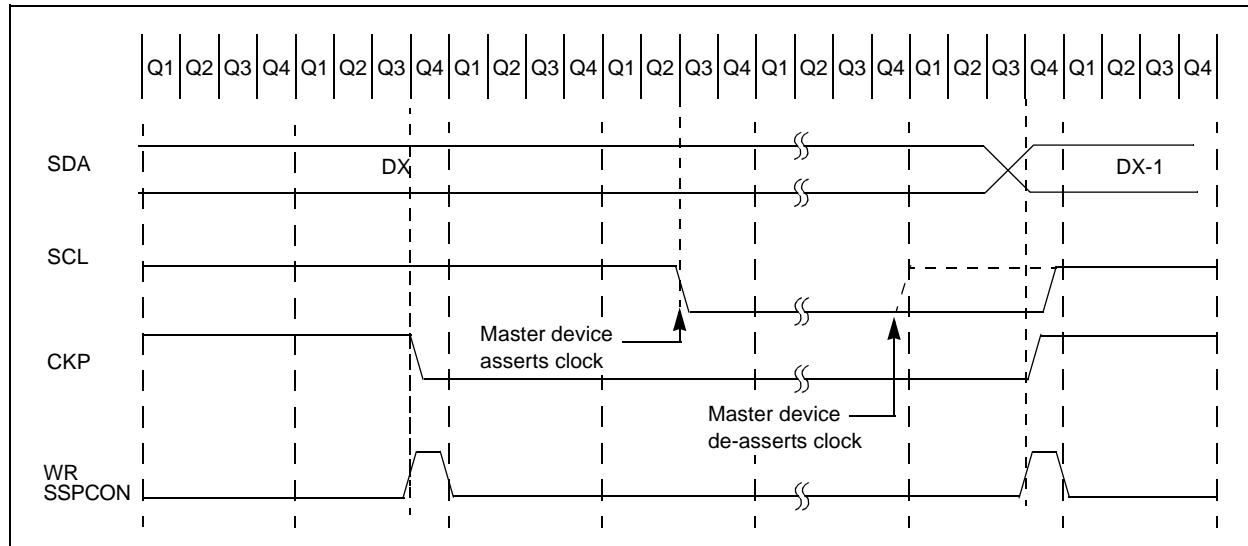
In 10-bit Slave Transmit mode, clock stretching is controlled during the first two address sequences by the state of the UA bit, just as it is in 10-bit Slave Receive mode. The first two addresses are followed by a third address sequence, which contains the high order bits of the 10-bit address and the R/W bit set to '1'. After the third address sequence is performed, the UA bit is not set, the module is now configured in Transmit mode, and clock stretching is controlled by the BF flag, as in 7-bit Slave Transmit mode (see Figure 17-11).

17.4.4.5 Clock Synchronization and the CKP bit

When the CKP bit is cleared, the SCL output is forced to '0'. However, setting the CKP bit will not assert the SCL output low until the SCL output is already sampled low. Therefore, the CKP bit will not assert the SCL line until an external I²C master device has

already asserted the SCL line. The SCL output will remain low until the CKP bit is set, and all other devices on the I²C bus have de-asserted SCL. This ensures that a write to the CKP bit will not violate the minimum high time requirement for SCL (see Figure 17-12).

FIGURE 17-12: CLOCK SYNCHRONIZATION TIMING



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FIGURE 17-13: I²C SLAVE MODE TIMING WITH SEN = 1 (RECEPTION, 7-BIT ADDRESS)

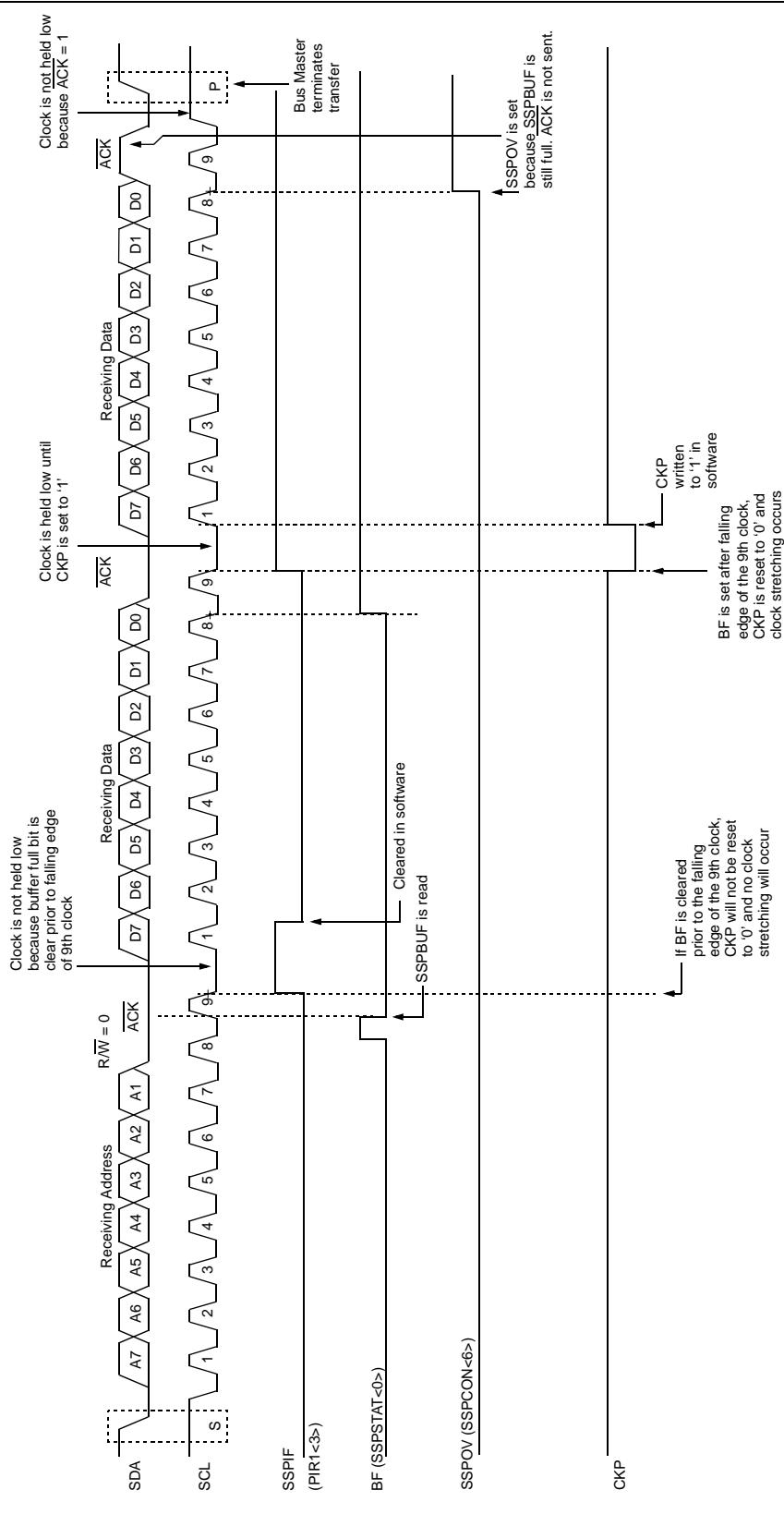
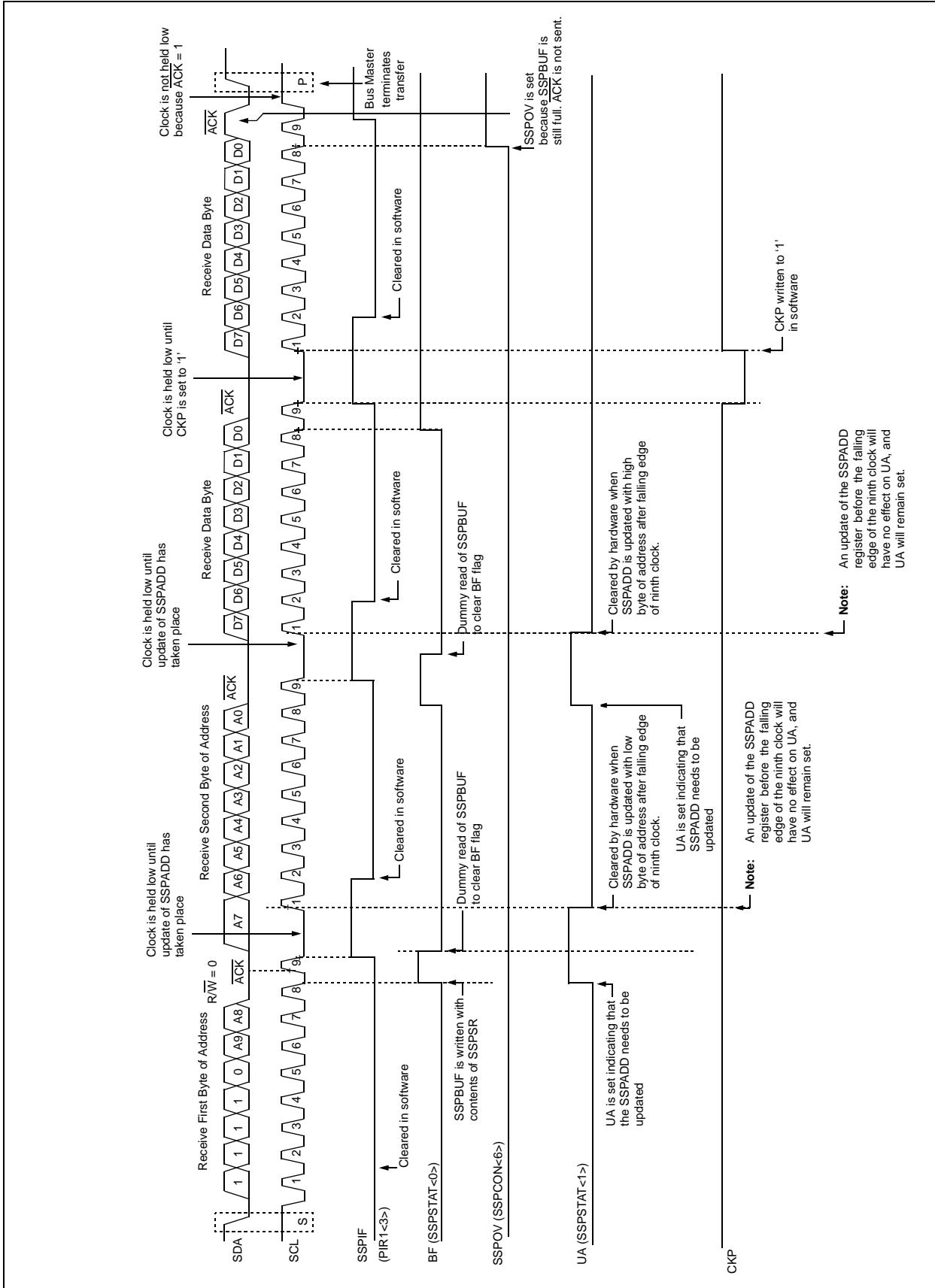


FIGURE 17-14: I²C SLAVE MODE TIMING SEN = 1 (RECEPTION, 10-BIT ADDRESS)



17.4.5 GENERAL CALL ADDRESS SUPPORT

The addressing procedure for the I²C bus is such that the first byte after the START condition usually determines which device will be the slave addressed by the master. The exception is the general call address, which can address all devices. When this address is used, all devices should, in theory, respond with an Acknowledge.

The general call address is one of eight addresses reserved for specific purposes by the I²C protocol. It consists of all 0's with R/W = 0.

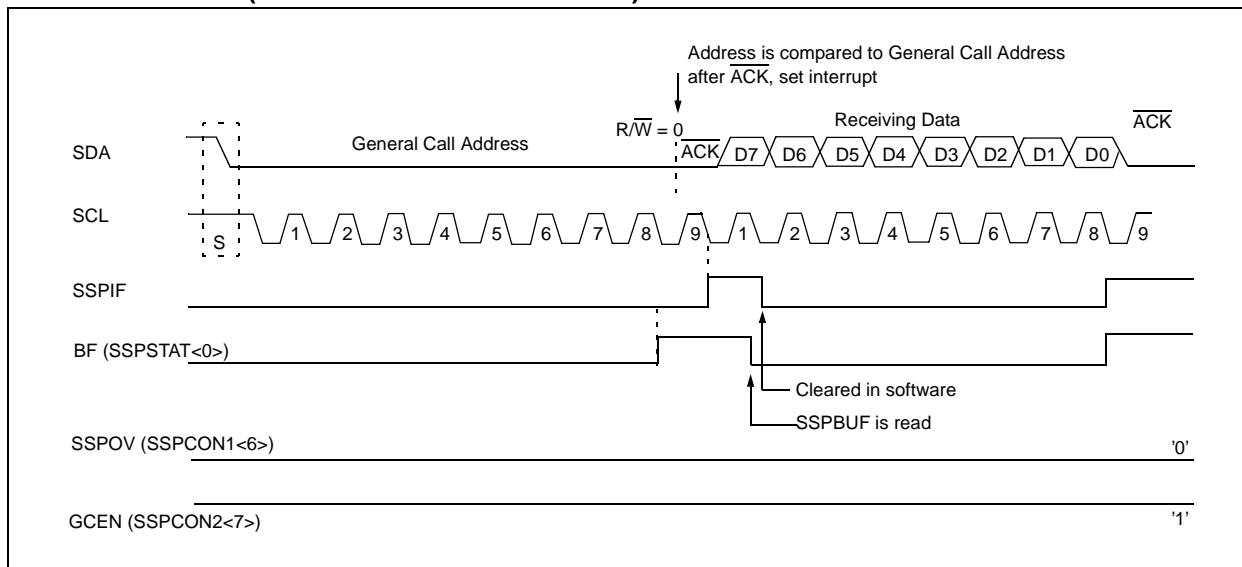
The general call address is recognized when the General Call Enable bit (GCEN) is enabled (SSPCON2<7> set). Following a START bit detect, 8-bits are shifted into the SSPSR and the address is compared against the SSPADD. It is also compared to the general call address and fixed in hardware.

If the general call address matches, the SSPSR is transferred to the SSPBUF, the BF flag bit is set (eighth bit), and on the falling edge of the ninth bit (ACK bit), the SSPIF interrupt flag bit is set.

When the interrupt is serviced, the source for the interrupt can be checked by reading the contents of the SSPBUF. The value can be used to determine if the address was device specific or a general call address.

In 10-bit mode, the SSPADD is required to be updated for the second half of the address to match, and the UA bit is set (SSPSTAT<1>). If the general call address is sampled when the GCEN bit is set, while the slave is configured in 10-bit Address mode, then the second half of the address is not necessary, the UA bit will not be set, and the slave will begin receiving data after the Acknowledge (Figure 17-15).

**FIGURE 17-15: SLAVE MODE GENERAL CALL ADDRESS SEQUENCE
(7 OR 10-BIT ADDRESS MODE)**



17.4.6 MASTER MODE

Master mode is enabled by setting and clearing the appropriate SSPM bits in SSPCON1 and by setting the SSPEN bit. In Master mode, the SCL and SDA lines are manipulated by the MSSP hardware.

Master mode of operation is supported by interrupt generation on the detection of the START and STOP conditions. The STOP (P) and START (S) bits are cleared from a RESET, or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit is set or the bus is IDLE, with both the S and P bits clear.

In Firmware Controlled Master mode, user code conducts all I²C bus operations based on START and STOP bit conditions.

Once Master mode is enabled, the user has six options.

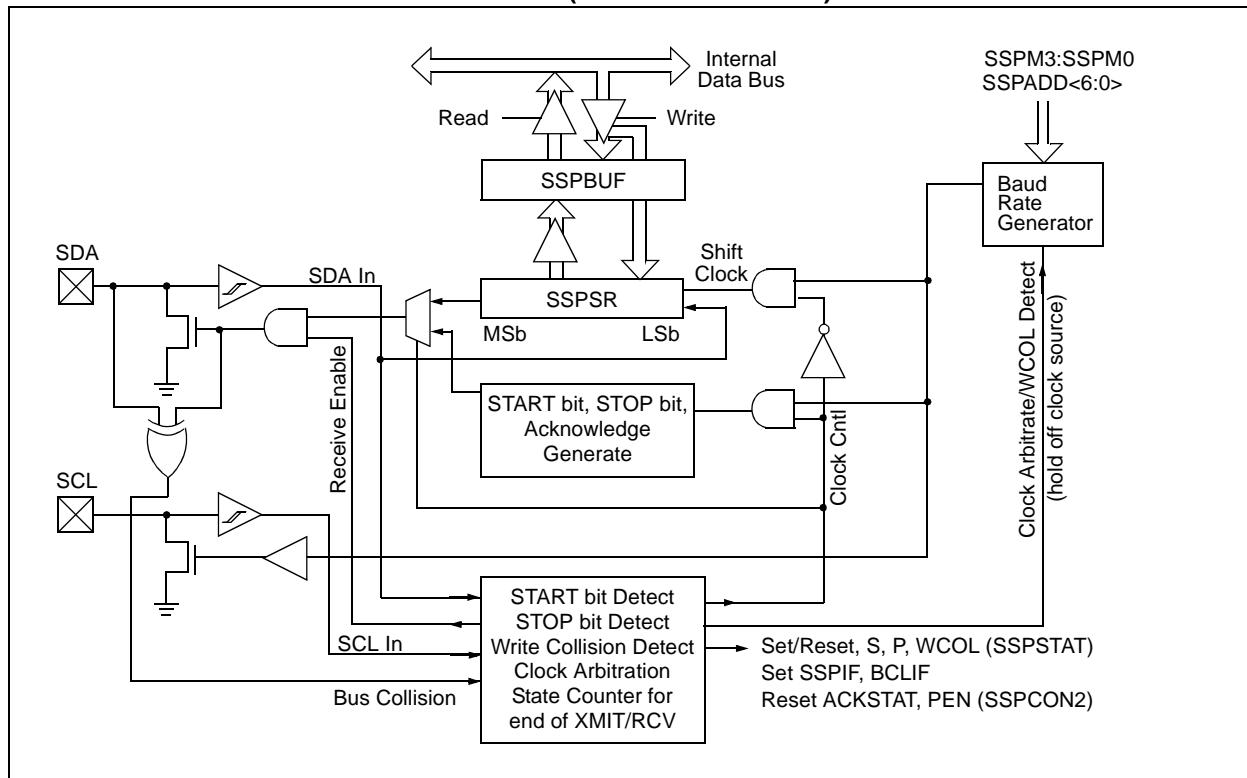
1. Assert a START condition on SDA and SCL.
2. Assert a Repeated START condition on SDA and SCL.
3. Write to the SSPBUF register initiating transmission of data/address.
4. Configure the I²C port to receive data.
5. Generate an Acknowledge condition at the end of a received byte of data.
6. Generate a STOP condition on SDA and SCL.

Note: The MSSP Module, when configured in I²C Master mode, does not allow queueing of events. For instance, the user is not allowed to initiate a START condition and immediately write the SSPBUF register to initiate transmission before the START condition is complete. In this case, the SSPBUF will not be written to and the WCOL bit will be set, indicating that a write to the SSPBUF did not occur.

The following events will cause SSP interrupt flag bit, SSPIF, to be set (SSP interrupt if enabled):

- START condition
- STOP condition
- Data transfer byte transmitted/received
- Acknowledge Transmit
- Repeated START

FIGURE 17-16: MSSP BLOCK DIAGRAM (I²C MASTER MODE)



17.4.6.1 I²C Master Mode Operation

The master device generates all of the serial clock pulses and the START and STOP conditions. A transfer is ended with a STOP condition or with a Repeated START condition. Since the Repeated START condition is also the beginning of the next serial transfer, the I²C bus will not be released.

In Master Transmitter mode, serial data is output through SDA, while SCL outputs the serial clock. The first byte transmitted contains the slave address of the receiving device (7 bits) and the Read/Write (R/W) bit. In this case, the R/W bit will be logic '0'. Serial data is transmitted 8 bits at a time. After each byte is transmitted, an Acknowledge bit is received. START and STOP conditions are output to indicate the beginning and the end of a serial transfer.

In Master Receive mode, the first byte transmitted contains the slave address of the transmitting device (7 bits) and the R/W bit. In this case, the R/W bit will be logic '1'. Thus, the first byte transmitted is a 7-bit slave address followed by a '1' to indicate receive bit. Serial data is received via SDA, while SCL outputs the serial clock. Serial data is received 8 bits at a time. After each byte is received, an Acknowledge bit is transmitted. START and STOP conditions indicate the beginning and end of transmission.

The baud rate generator used for the SPI mode operation is used to set the SCL clock frequency for either 100 kHz, 400 kHz or 1 MHz I²C operation. See Section 17.4.7 ("Baud Rate Generator"), for more detail.

A typical transmit sequence would go as follows:

1. The user generates a START condition by setting the START enable bit, SEN (SSPCON2<0>).
2. SSPIF is set. The MSSP module will wait the required start time before any other operation takes place.
3. The user loads the SSPBUF with the slave address to transmit.
4. Address is shifted out the SDA pin until all 8 bits are transmitted.
5. The MSSP Module shifts in the ACK bit from the slave device and writes its value into the SSPCON2 register (SSPCON2<6>).
6. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPIF bit.
7. The user loads the SSPBUF with eight bits of data.
8. Data is shifted out the SDA pin until all 8 bits are transmitted.
9. The MSSP Module shifts in the ACK bit from the slave device and writes its value into the SSPCON2 register (SSPCON2<6>).
10. The MSSP module generates an interrupt at the end of the ninth clock cycle by setting the SSPIF bit.
11. The user generates a STOP condition by setting the STOP enable bit PEN (SSPCON2<2>).
12. Interrupt is generated once the STOP condition is complete.

17.4.7 BAUD RATE GENERATOR

In I²C Master mode, the baud rate generator (BRG) reload value is placed in the lower 7 bits of the SSPADD register (Figure 17-17). When a write occurs to SSPBUF, the baud rate generator will automatically begin counting. The BRG counts down to 0 and stops until another reload has taken place. The BRG count is decremented twice per instruction cycle (TCY) on the Q2 and Q4 clocks. In I²C Master mode, the BRG is reloaded automatically.

Once the given operation is complete (i.e., transmission of the last data bit is followed by ACK), the internal clock will automatically stop counting and the SCL pin will remain in its last state.

Table 15-3 demonstrates clock rates based on instruction cycles and the BRG value loaded into SSPADD.

FIGURE 17-17: BAUD RATE GENERATOR BLOCK DIAGRAM

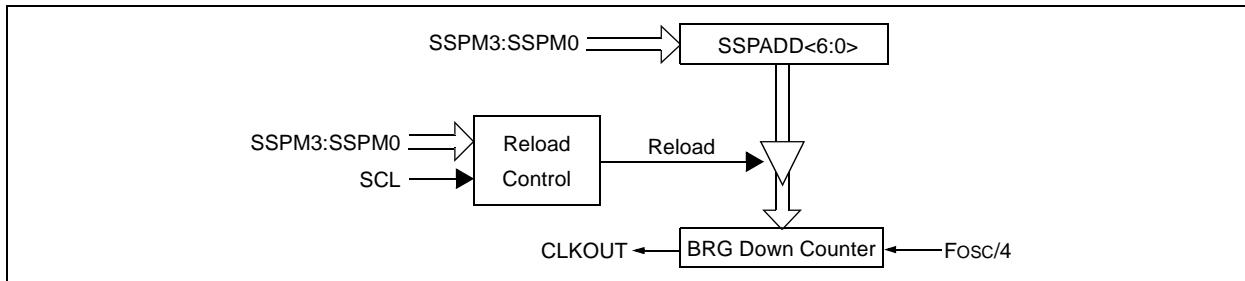


TABLE 17-3: I²C CLOCK RATE W/BRG

F _{CY}	F _{CY} *2	BRG VALUE	F _{SCL} (2 rollovers of BRG)
10 MHz	20 MHz	19h	400 kHz ⁽¹⁾
10 MHz	20 MHz	20h	312.5 kHz
10 MHz	20 MHz	3Fh	100 kHz
4 MHz	8 MHz	0Ah	400 kHz ⁽¹⁾
4 MHz	8 MHz	0Dh	308 kHz
4 MHz	8 MHz	28h	100 kHz
1 MHz	2 MHz	03h	333 kHz ⁽¹⁾
1 MHz	2 MHz	0Ah	100 kHz
1 MHz	2 MHz	00h	1 MHz ⁽¹⁾

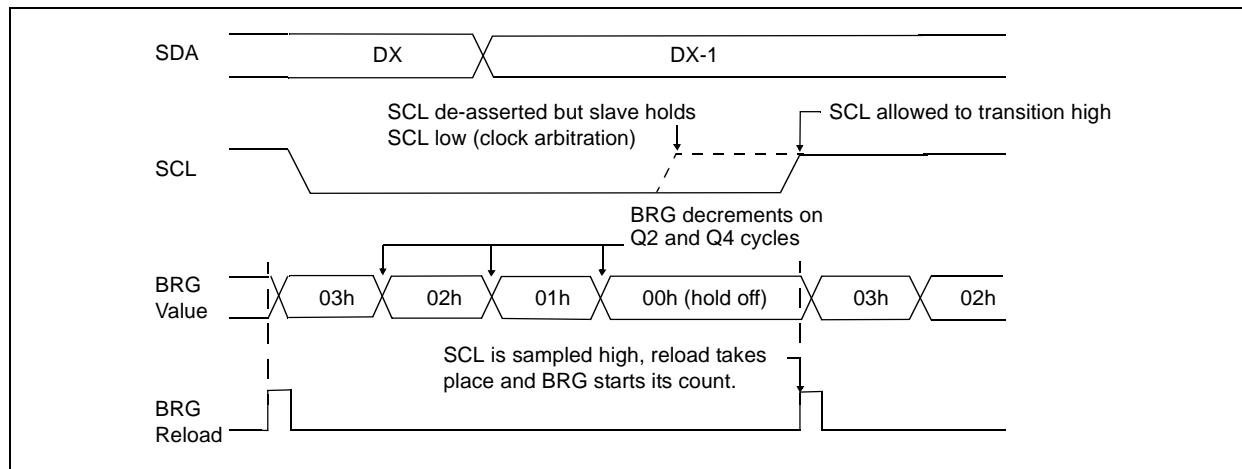
Note 1: The I²C interface does not conform to the 400 kHz I²C specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

17.4.7.1 Clock Arbitration

Clock arbitration occurs when the master, during any receive, transmit or Repeated START/STOP condition, de-asserts the SCL pin (SCL allowed to float high). When the SCL pin is allowed to float high, the baud rate generator (BRG) is suspended from counting until the SCL pin is actually sampled high. When the SCL pin is

sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and begins counting. This ensures that the SCL high time will always be at least one BRG rollover count, in the event that the clock is held low by an external device (Figure 15-18).

FIGURE 17-18: BAUD RATE GENERATOR TIMING WITH CLOCK ARBITRATION



17.4.8 I²C MASTER MODE START CONDITION TIMING

To initiate a START condition, the user sets the START condition enable bit, SEN (SSPCON2<0>). If the SDA and SCL pins are sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and starts its count. If SCL and SDA are both sampled high when the baud rate generator times out (TBRG), the SDA pin is driven low. The action of the SDA being driven low, while SCL is high, is the START condition and causes the S bit (SSPSTAT<3>) to be set. Following this, the baud rate generator is reloaded with the contents of SSPADD<6:0> and resumes its count. When the baud rate generator times out (TBRG), the SEN bit (SSPCON2<0>) will be automatically cleared by hardware, the baud rate generator is suspended, leaving the SDA line held low and the START condition is complete.

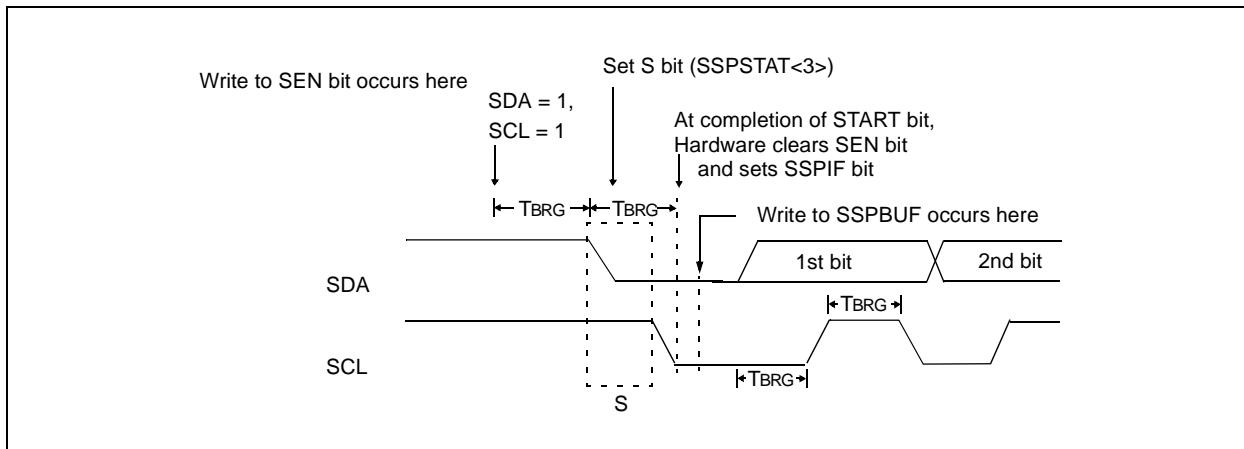
Note: If at the beginning of the START condition, the SDA and SCL pins are already sampled low, or if during the START condition the SCL line is sampled low before the SDA line is driven low, a bus collision occurs, the Bus Collision Interrupt Flag, BCLIF is set, the START condition is aborted, and the I²C module is reset into its IDLE state.

17.4.8.1 WCOL Status Flag

If the user writes the SSPBUF when a START sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Note: Because queueing of events is not allowed, writing to the lower 5 bits of SSPCON2 is disabled until the START condition is complete.

FIGURE 17-19: FIRST START BIT TIMING



17.4.9 I²C MASTER MODE REPEATED START CONDITION TIMING

A Repeated START condition occurs when the RSEN bit (SSPCON2<1>) is programmed high and the I²C logic module is in the IDLE state. When the RSEN bit is set, the SCL pin is asserted low. When the SCL pin is sampled low, the baud rate generator is loaded with the contents of SSPADD<5:0> and begins counting. The SDA pin is released (brought high) for one baud rate generator count (TBRG). When the baud rate generator times out, if SDA is sampled high, the SCL pin will be de-asserted (brought high). When SCL is sampled high, the baud rate generator is reloaded with the contents of SSPADD<6:0> and begins counting. SDA and SCL must be sampled high for one TBRG. This action is then followed by assertion of the SDA pin (SDA = 0) for one TBRG, while SCL is high. Following this, the RSEN bit (SSPCON2<1>) will be automatically cleared and the baud rate generator will not be reloaded, leaving the SDA pin held low. As soon as a START condition is detected on the SDA and SCL pins, the S bit (SSPSTAT<3>) will be set. The SSPIF bit will not be set until the baud rate generator has timed out.

- Note 1:** If RSEN is programmed while any other event is in progress, it will not take effect.
- 2:** A bus collision during the Repeated START condition occurs if:
 - SDA is sampled low when SCL goes from low to high.
 - SCL goes low before SDA is asserted low. This may indicate that another master is attempting to transmit a data "1".

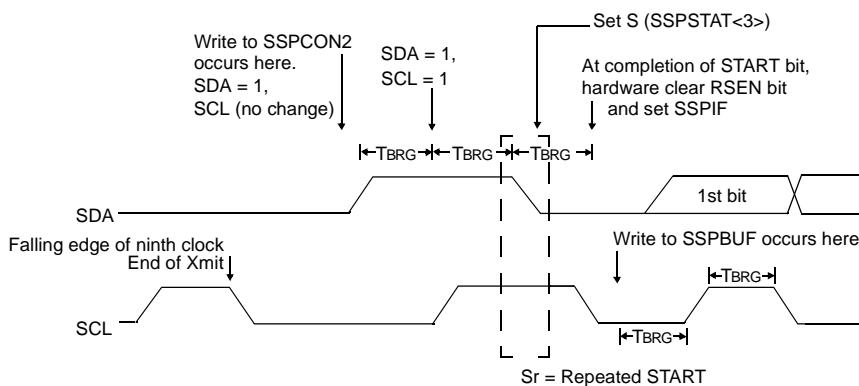
Immediately following the SSPIF bit getting set, the user may write the SSPBUF with the 7-bit address in 7-bit mode, or the default first address in 10-bit mode. After the first eight bits are transmitted and an ACK is received, the user may then transmit an additional eight bits of address (10-bit mode) or eight bits of data (7-bit mode).

17.4.9.1 WCOL Status Flag

If the user writes the SSPBUF when a Repeated START sequence is in progress, the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

Note: Because queuing of events is not allowed, writing of the lower 5 bits of SSPCON2 is disabled until the Repeated START condition is complete.

FIGURE 17-20: REPEAT START CONDITION WAVEFORM



17.4.10 I²C MASTER MODE TRANSMISSION

Transmission of a data byte, a 7-bit address, or the other half of a 10-bit address is accomplished by simply writing a value to the SSPBUF register. This action will set the buffer full flag bit, BF, and allow the baud rate generator to begin counting and start the next transmission. Each bit of address/data will be shifted out onto the SDA pin after the falling edge of SCL is asserted (see data hold time specification parameter #106). SCL is held low for one baud rate generator rollover count (TBRG). Data should be valid before SCL is released high (see data setup time specification parameter #107). When the SCL pin is released high, it is held that way for TBRG. The data on the SDA pin must remain stable for that duration and some hold time, after the next falling edge of SCL. After the eighth bit is shifted out (the falling edge of the eighth clock), the BF flag is cleared and the master releases SDA. This allows the slave device being addressed to respond with an ACK bit during the ninth bit time if an address match occurred, or if data was received properly. The status of ACK is written into the ACKDT bit on the falling edge of the ninth clock. If the master receives an Acknowledge, the Acknowledge status bit, ACKSTAT, is cleared. If not, the bit is set. After the ninth clock, the SSPIF bit is set and the master clock (baud rate generator) is suspended until the next data byte is loaded into the SSPBUF, leaving SCL low and SDA unchanged (Figure 17-21).

After the write to the SSPBUF, each bit of address will be shifted out on the falling edge of SCL, until all seven address bits and the R/W bit are completed. On the falling edge of the eighth clock, the master will de-assert the SDA pin, allowing the slave to respond with an Acknowledge. On the falling edge of the ninth clock, the master will sample the SDA pin to see if the address was recognized by a slave. The status of the ACK bit is loaded into the ACKSTAT status bit (SSPCON2<6>). Following the falling edge of the ninth clock transmission of the address, the SSPIF is set, the BF flag is cleared and the baud rate generator is turned off until another write to the SSPBUF takes place, holding SCL low and allowing SDA to float.

17.4.10.1 BF Status Flag

In Transmit mode, the BF bit (SSPSTAT<0>) is set when the CPU writes to SSPBUF and is cleared when all 8 bits are shifted out.

17.4.10.2 WCOL Status Flag

If the user writes the SSPBUF when a transmit is already in progress (i.e., SSPSR is still shifting out a data byte), the WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

WCOL must be cleared in software.

17.4.10.3 ACKSTAT Status Flag

In Transmit mode, the ACKSTAT bit (SSPCON2<6>) is cleared when the slave has sent an Acknowledge ($\overline{ACK} = 0$), and is set when the slave does not Acknowledge ($\overline{ACK} = 1$). A slave sends an Acknowledge when it has recognized its address (including a general call), or when the slave has properly received its data.

17.4.11 I²C MASTER MODE RECEPTION

Master mode reception is enabled by programming the receive enable bit, RCEN (SSPCON2<3>).

Note: The MSSP module must be in an IDLE state before the RCEN bit is set, or the RCEN bit will be disregarded.

The baud rate generator begins counting, and on each rollover, the state of the SCL pin changes (high to low/low to high) and data is shifted into the SSPSR. After the falling edge of the eighth clock, the receive enable flag is automatically cleared, the contents of the SSPSR are loaded into the SSPBUF, the BF flag bit is set, the SSPIF flag bit is set and the baud rate generator is suspended from counting, holding SCL low. The MSSP is now in IDLE state, awaiting the next command. When the buffer is read by the CPU, the BF flag bit is automatically cleared. The user can then send an Acknowledge sequence enable bit, ACKEN (SSPCON2<4>).

17.4.11.1 BF Status Flag

In receive operation, the BF bit is set when an address or data byte is loaded into SSPBUF from SSPSR. It is cleared when the SSPBUF register is read.

17.4.11.2 SSPOV Status Flag

In receive operation, the SSPOV bit is set when 8 bits are received into the SSPSR and the BF flag bit is already set from a previous reception.

17.4.11.3 WCOL Status Flag

If the user writes the SSPBUF when a receive is already in progress (i.e., SSPSR is still shifting in a data byte), the WCOL bit is set and the contents of the buffer are unchanged (the write doesn't occur).

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FIGURE 17-21: I²C MASTER MODE WAVEFORM (TRANSMISSION, 7 OR 10-BIT ADDRESS)

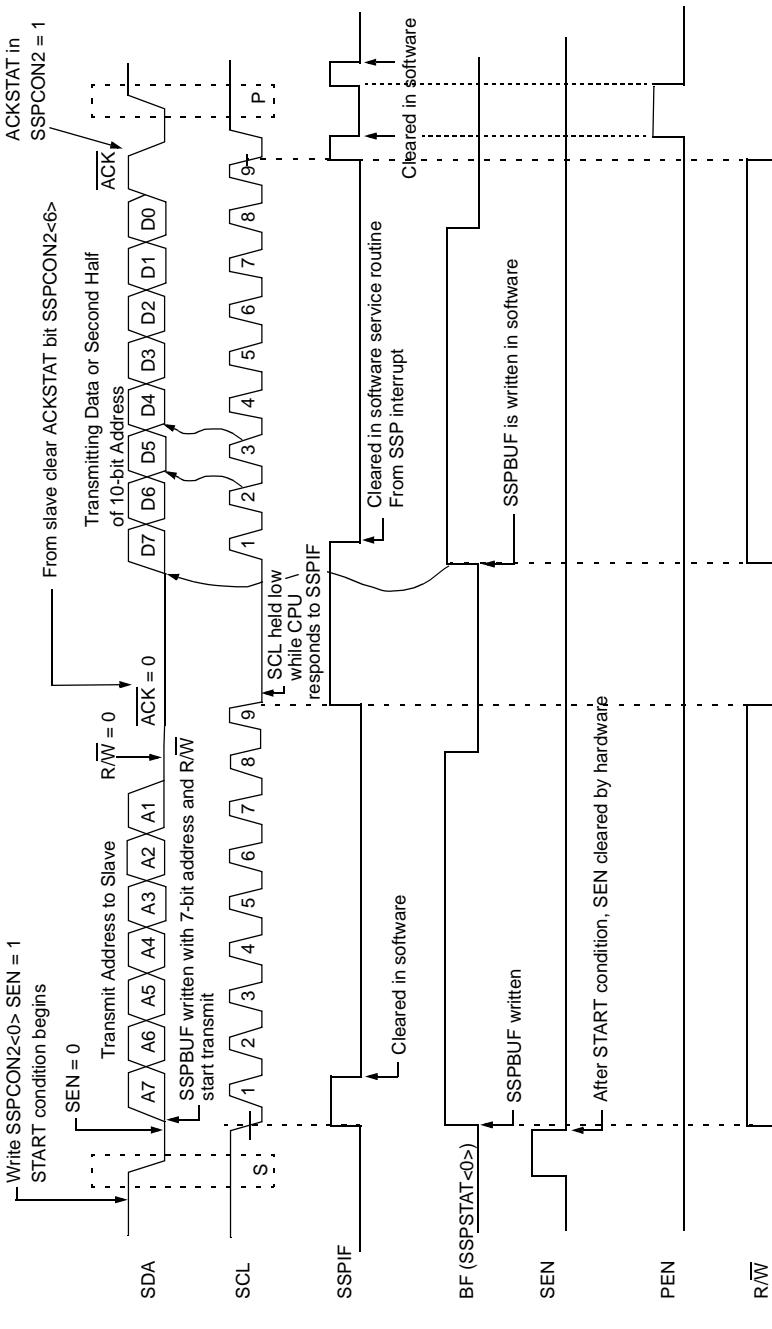
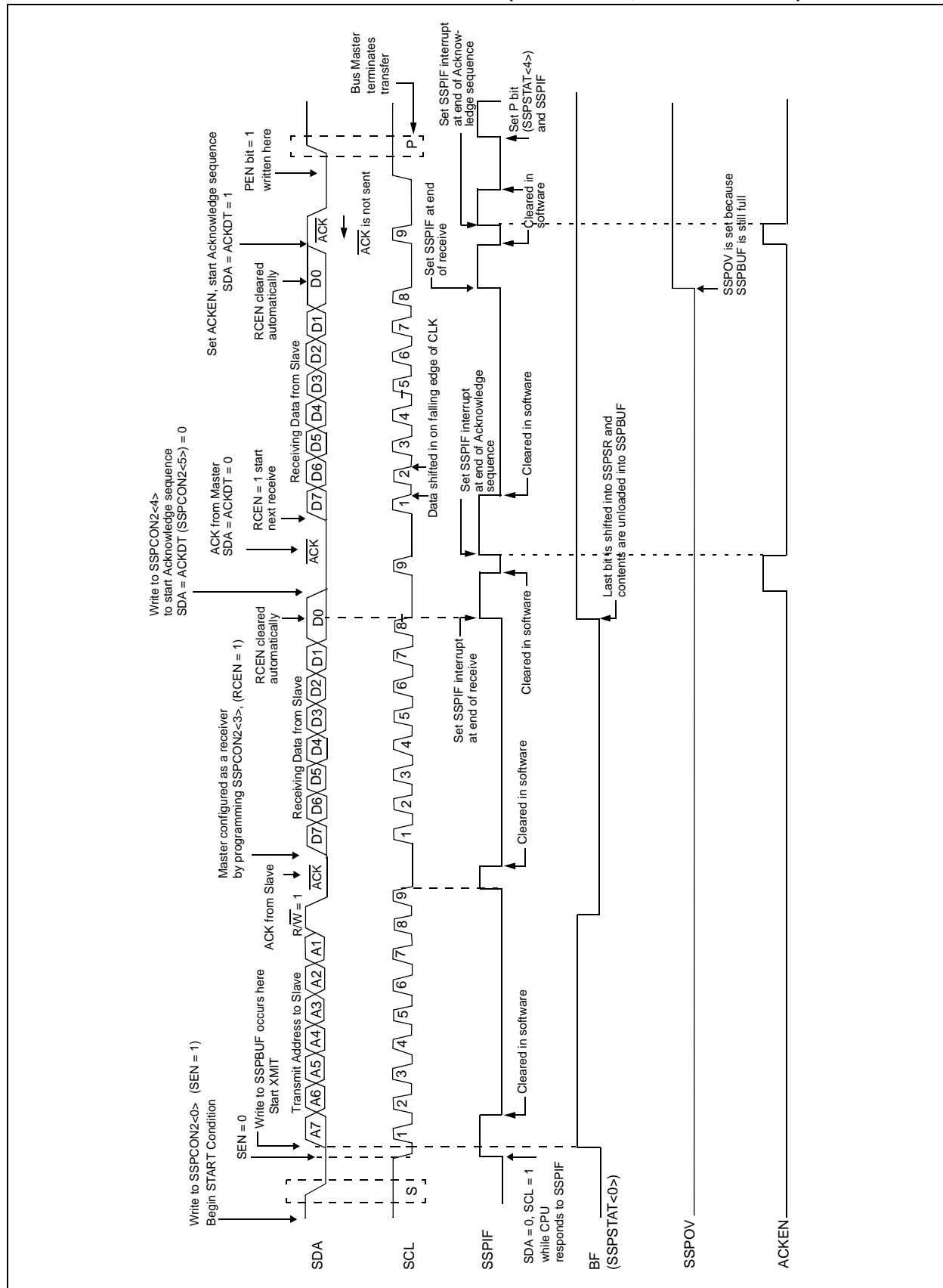


FIGURE 17-22: I²C MASTER MODE WAVEFORM (RECEPTION, 7-BIT ADDRESS)



17.4.12 ACKNOWLEDGE SEQUENCE TIMING

An Acknowledge sequence is enabled by setting the Acknowledge sequence enable bit, ACKEN (SSPCON2<4>). When this bit is set, the SCL pin is pulled low and the contents of the Acknowledge data bit are presented on the SDA pin. If the user wishes to generate an Acknowledge, then the ACKDT bit should be cleared. If not, the user should set the ACKDT bit before starting an Acknowledge sequence. The baud rate generator then counts for one rollover period (TBRG) and the SCL pin is de-asserted (pulled high). When the SCL pin is sampled high (clock arbitration), the baud rate generator counts for TBRG. The SCL pin is then pulled low. Following this, the ACKEN bit is automatically cleared, the baud rate generator is turned off and the MSSP module then goes into IDLE mode (Figure 17-23).

17.4.12.1 WCOL Status Flag

If the user writes the SSPBUF when an Acknowledge sequence is in progress, then WCOL is set and the contents of the buffer are unchanged (the write doesn't occur).

FIGURE 17-23: ACKNOWLEDGE SEQUENCE WAVEFORM

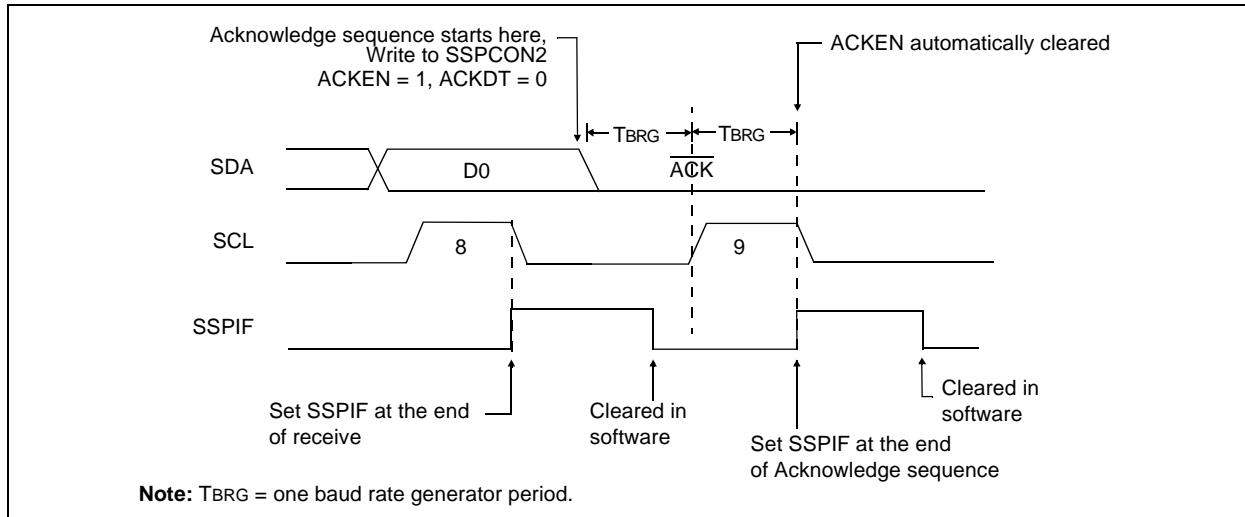
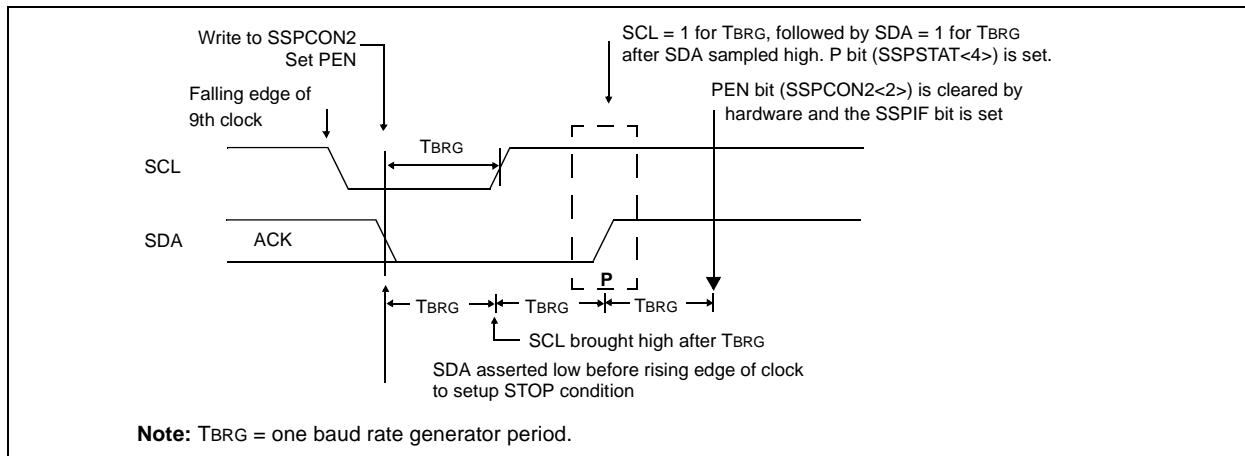


FIGURE 17-24: STOP CONDITION RECEIVE OR TRANSMIT MODE



17.4.14 SLEEP OPERATION

While in SLEEP mode, the I²C module can receive addresses or data, and when an address match or complete byte transfer occurs, wake the processor from SLEEP (if the MSSP interrupt is enabled).

17.4.15 EFFECT OF A RESET

A RESET disables the MSSP module and terminates the current transfer.

17.4.16 MULTI-MASTER MODE

In Multi-Master mode, the interrupt generation on the detection of the START and STOP conditions allows the determination of when the bus is free. The STOP (P) and START (S) bits are cleared from a RESET or when the MSSP module is disabled. Control of the I²C bus may be taken when the P bit (SSPSTAT<4>) is set, or the bus is idle with both the S and P bits clear. When the bus is busy, enabling the SSP interrupt will generate the interrupt when the STOP condition occurs.

In multi-master operation, the SDA line must be monitored for arbitration, to see if the signal level is the expected output level. This check is performed in hardware, with the result placed in the BCLIF bit.

The states where arbitration can be lost are:

- Address Transfer
- Data Transfer
- A START Condition
- A Repeated START Condition
- An Acknowledge Condition

17.4.17 MULTI -MASTER COMMUNICATION, BUS COLLISION, AND BUS ARBITRATION

Multi-Master mode support is achieved by bus arbitration. When the master outputs address/data bits onto the SDA pin, arbitration takes place when the master outputs a '1' on SDA, by letting SDA float high and another master asserts a '0'. When the SCL pin floats high, data should be stable. If the expected data on SDA is a '1' and the data sampled on the SDA pin = '0', then a bus collision has taken place. The master will set the Bus Collision Interrupt Flag, BCLIF and reset the I²C port to its IDLE state (Figure 17-25).

If a transmit was in progress when the bus collision occurred, the transmission is halted, the BF flag is cleared, the SDA and SCL lines are de-asserted, and the SSPBUF can be written to. When the user services the bus collision Interrupt Service Routine, and if the I²C bus is free, the user can resume communication by asserting a START condition.

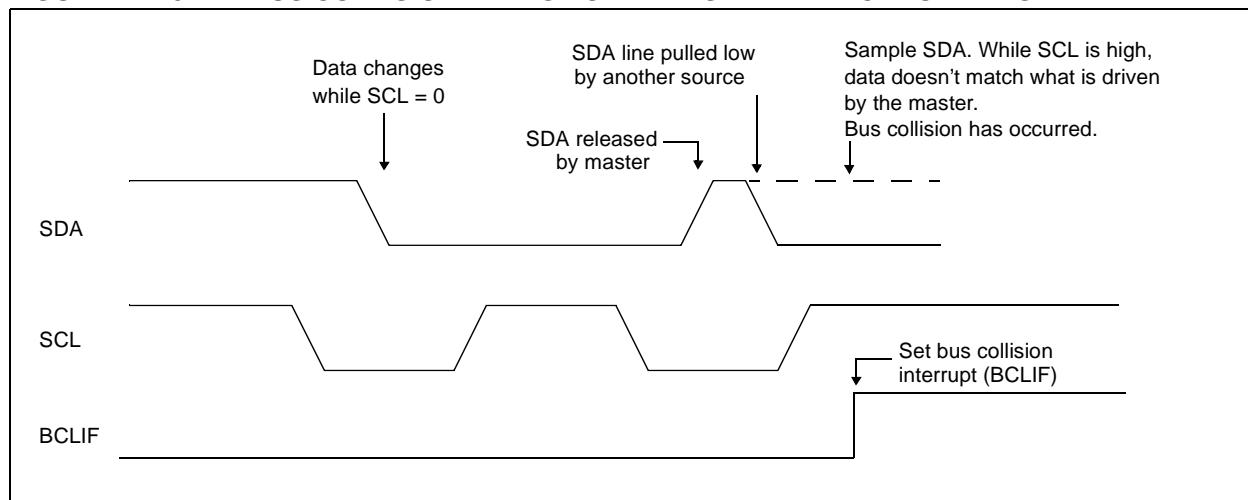
If a START, Repeated START, STOP, or Acknowledge condition was in progress when the bus collision occurred, the condition is aborted, the SDA and SCL lines are de-asserted, and the respective control bits in the SSPCON2 register are cleared. When the user services the bus collision Interrupt Service Routine, and if the I²C bus is free, the user can resume communication by asserting a START condition.

The master will continue to monitor the SDA and SCL pins. If a STOP condition occurs, the SSPIF bit will be set.

A write to the SSPBUF will start the transmission of data at the first data bit, regardless of where the transmitter left off when the bus collision occurred.

In Multi-Master mode, the interrupt generation on the detection of START and STOP conditions allows the determination of when the bus is free. Control of the I²C bus can be taken when the P bit is set in the SSPSTAT register, or the bus is IDLE and the S and P bits are cleared.

FIGURE 17-25: BUS COLLISION TIMING FOR TRANSMIT AND ACKNOWLEDGE



17.4.17.1 Bus Collision During a START Condition

During a START condition, a bus collision occurs if:

- SDA or SCL are sampled low at the beginning of the START condition (Figure 17-26).
- SCL is sampled low before SDA is asserted low (Figure 17-27).

During a START condition, both the SDA and the SCL pins are monitored.

If the SDA pin is already low, or the SCL pin is already low, then all of the following occur:

- the START condition is aborted,
- the BCLIF flag is set, and
- the MSSP module is reset to its IDLE state (Figure 17-26).

The START condition begins with the SDA and SCL pins de-asserted. When the SDA pin is sampled high, the baud rate generator is loaded from SSPADD<6:0> and counts down to 0. If the SCL pin is sampled low while SDA is high, a bus collision occurs, because it is assumed that another master is attempting to drive a data '1' during the START condition.

If the SDA pin is sampled low during this count, the BRG is reset and the SDA line is asserted early (Figure 17-28). If, however, a '1' is sampled on the SDA pin, the SDA pin is asserted low at the end of the BRG count. The baud rate generator is then reloaded and counts down to 0, and during this time, if the SCL pins are sampled as '0', a bus collision does not occur. At the end of the BRG count, the SCL pin is asserted low.

Note: The reason that bus collision is not a factor during a START condition is that no two bus masters can assert a START condition at the exact same time. Therefore, one master will always assert SDA before the other. This condition does not cause a bus collision, because the two masters must be allowed to arbitrate the first address following the START condition. If the address is the same, arbitration must be allowed to continue into the data portion, Repeated START or STOP conditions.

FIGURE 17-26: BUS COLLISION DURING START CONDITION (SDA ONLY)

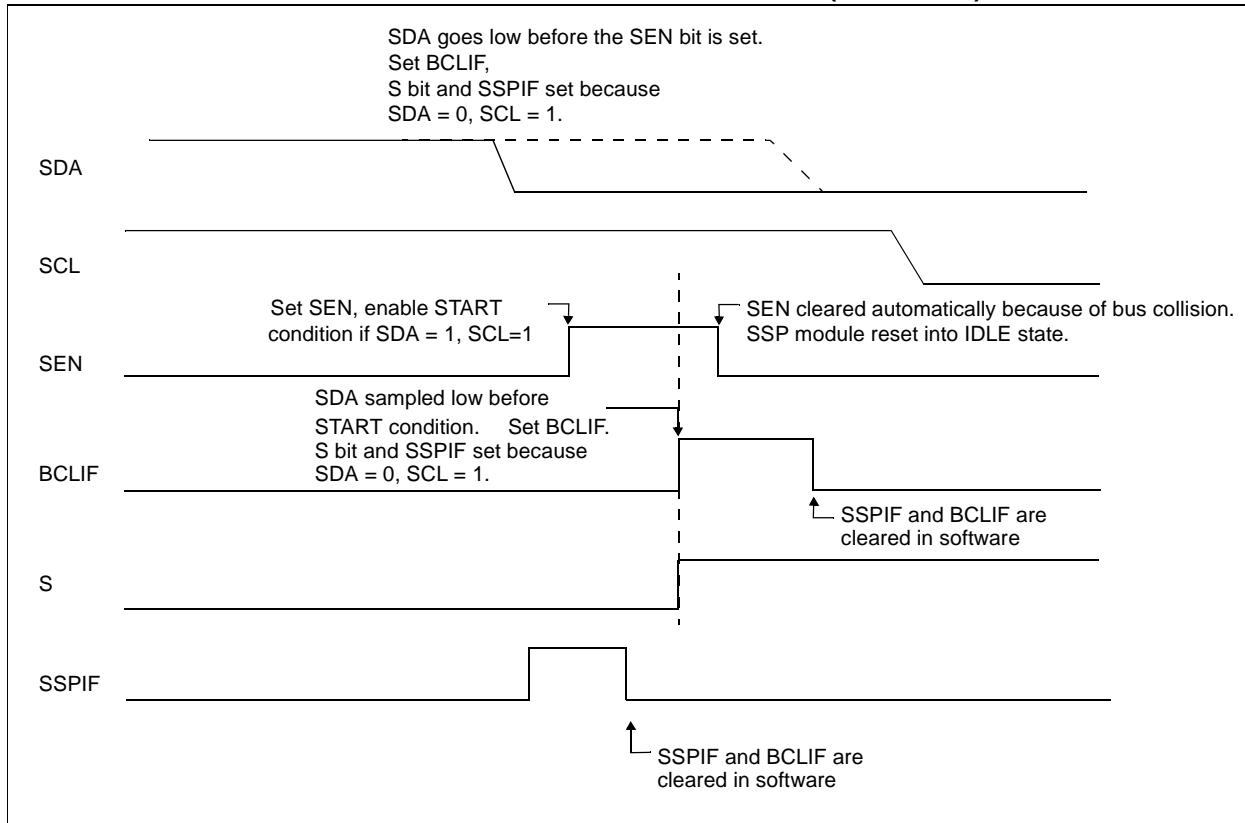


FIGURE 17-27: BUS COLLISION DURING START CONDITION (SCL = 0)

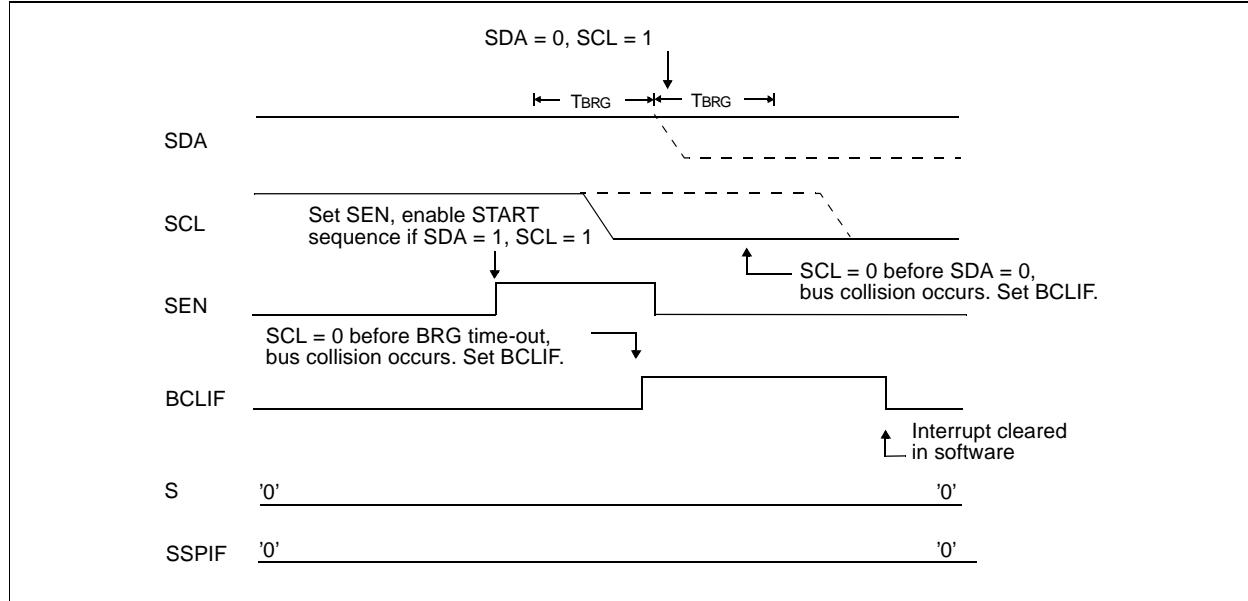
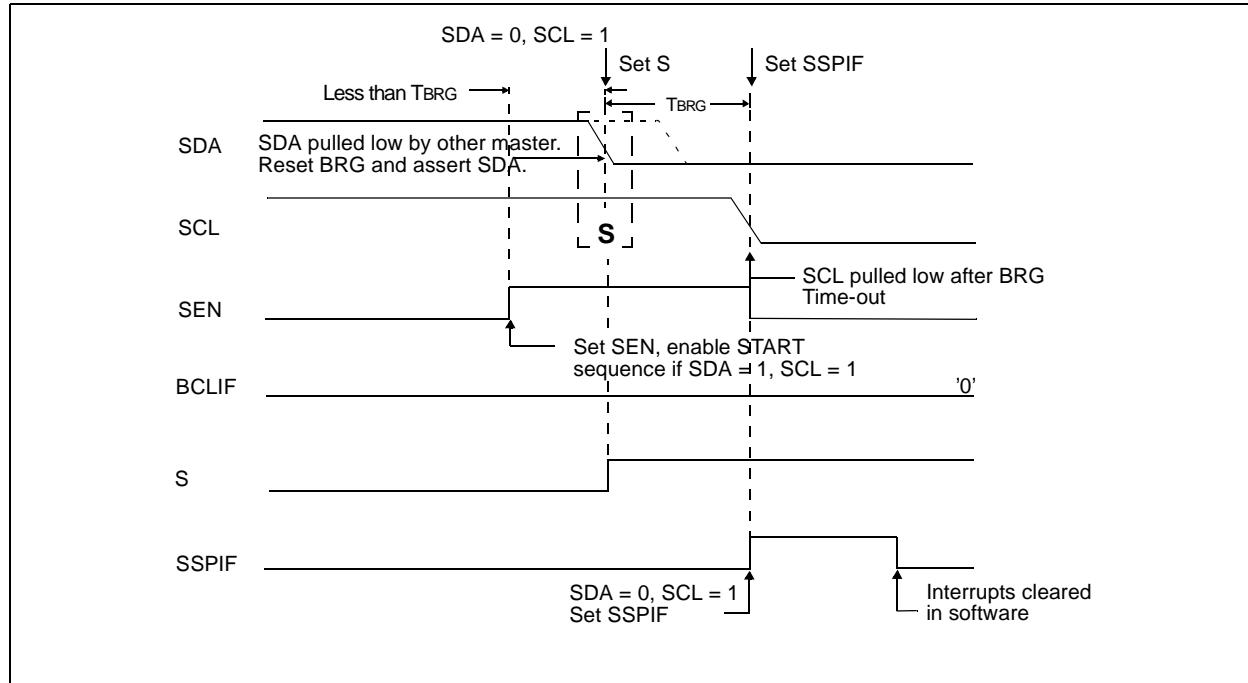


FIGURE 17-28: BRG RESET DUE TO SDA ARBITRATION DURING START CONDITION



17.4.17.2 Bus Collision During a Repeated START Condition

During a Repeated START condition, a bus collision occurs if:

- A low level is sampled on SDA when SCL goes from low level to high level.
- SCL goes low before SDA is asserted low, indicating that another master is attempting to transmit a data '1'.

When the user de-asserts SDA and the pin is allowed to float high, the BRG is loaded with SSPADD<6:0> and counts down to 0. The SCL pin is then de-asserted, and when sampled high, the SDA pin is sampled.

If SDA is low, a bus collision has occurred (i.e., another master is attempting to transmit a data '0', Figure 17-29). If SDA is sampled high, the BRG is

reloaded and begins counting. If SDA goes from high to low before the BRG times out, no bus collision occurs because no two masters can assert SDA at exactly the same time.

If SCL goes from high to low before the BRG times out and SDA has not already been asserted, a bus collision occurs. In this case, another master is attempting to transmit a data '1' during the Repeated START condition, Figure 17-30.

If, at the end of the BRG time-out, both SCL and SDA are still high, the SDA pin is driven low and the BRG is reloaded and begins counting. At the end of the count, regardless of the status of the SCL pin, the SCL pin is driven low and the Repeated START condition is complete.

FIGURE 17-29: BUS COLLISION DURING A REPEATED START CONDITION (CASE 1)

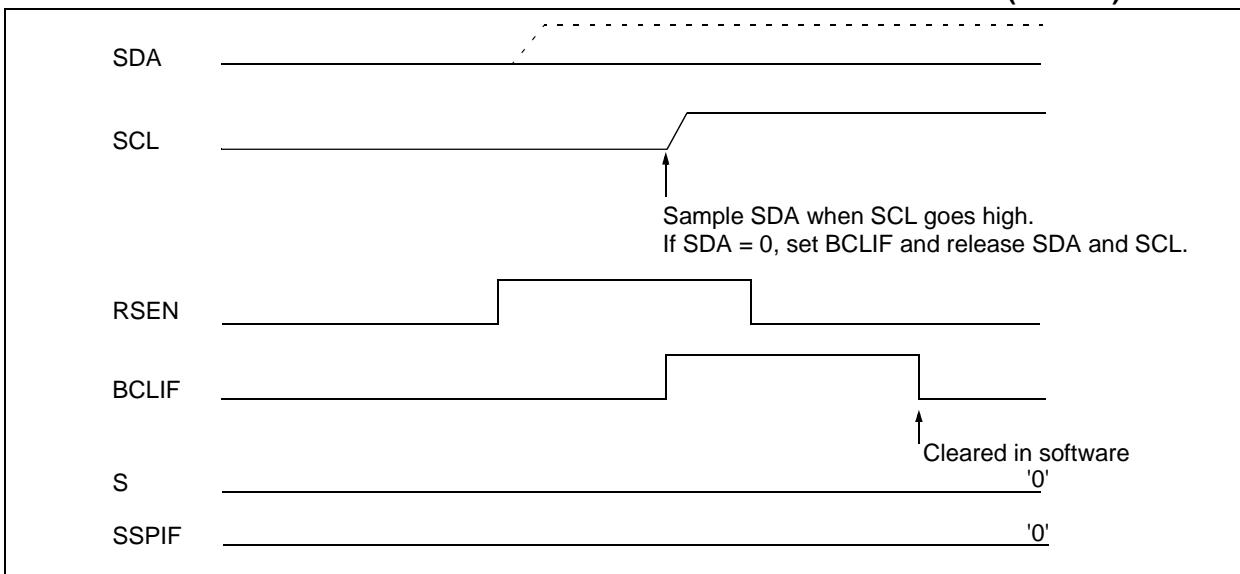
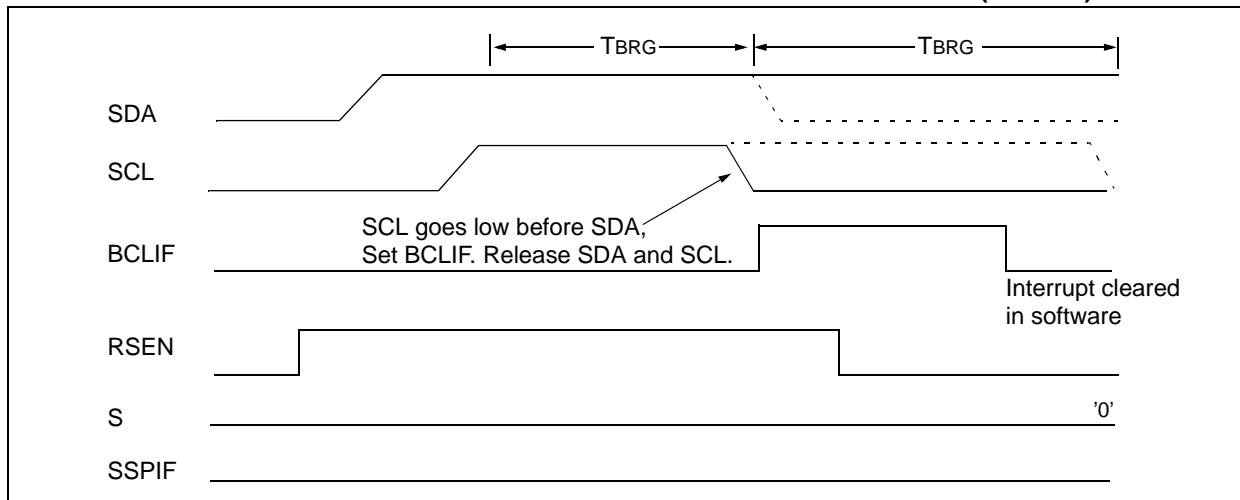


FIGURE 17-30: BUS COLLISION DURING REPEATED START CONDITION (CASE 2)



17.4.17.3 Bus Collision During a STOP Condition

Bus collision occurs during a STOP condition if:

- After the SDA pin has been de-asserted and allowed to float high, SDA is sampled low after the BRG has timed out.
- After the SCL pin is de-asserted, SCL is sampled low before SDA goes high.

The STOP condition begins with SDA asserted low. When SDA is sampled low, the SCL pin is allowed to float. When the pin is sampled high (clock arbitration), the baud rate generator is loaded with SSPADD<6:0> and counts down to 0. After the BRG times out, SDA is sampled. If SDA is sampled low, a bus collision has occurred. This is due to another master attempting to drive a data '0' (Figure 17-31). If the SCL pin is sampled low before SDA is allowed to float high, a bus collision occurs. This is another case of another master attempting to drive a data '0' (Figure 17-32).

FIGURE 17-31: BUS COLLISION DURING A STOP CONDITION (CASE 1)

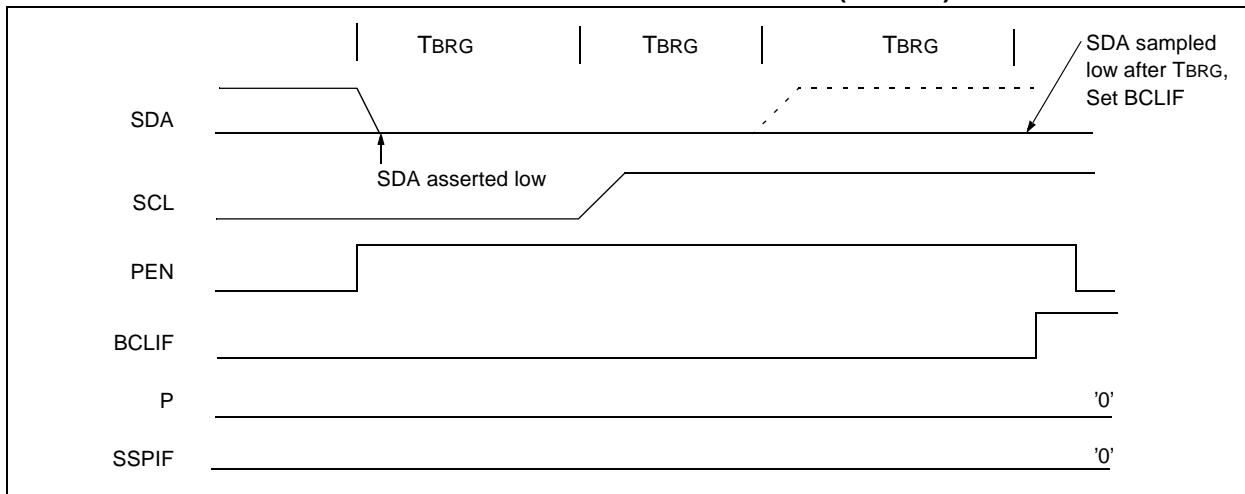
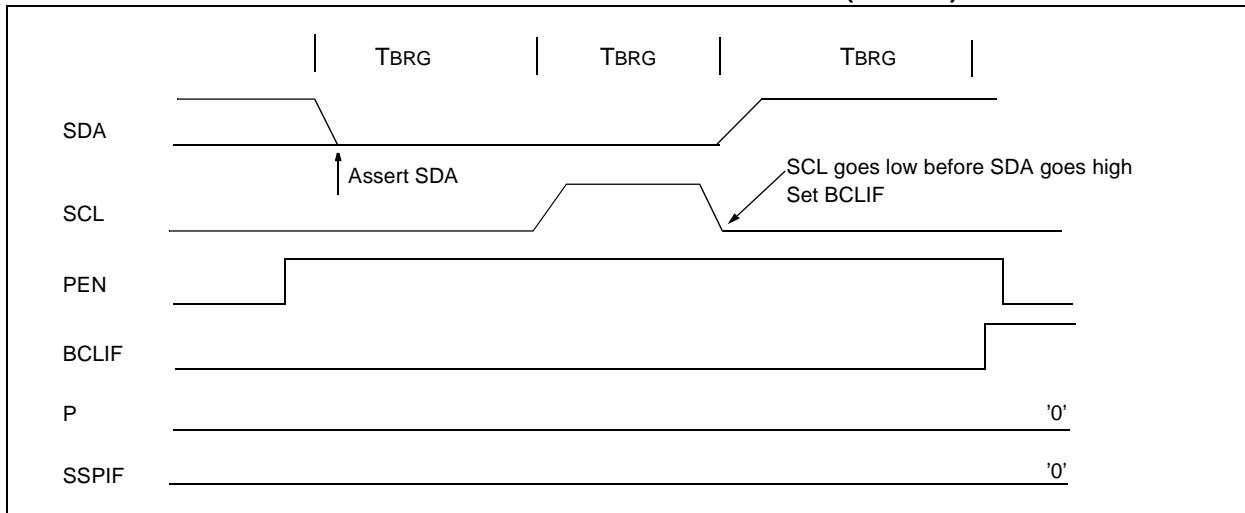


FIGURE 17-32: BUS COLLISION DURING A STOP CONDITION (CASE 2)



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NOTES:

18.0 ADDRESSABLE UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART)

The Universal Synchronous Asynchronous Receiver Transmitter (USART) module (also known as a Serial Communications Interface or SCI) is one of the two types of serial I/O modules available on PIC18FXX20 devices. Each device has two USARTs, which can be configured independently of each other. Each can be configured as a full duplex asynchronous system that can communicate with peripheral devices, such as CRT terminals and personal computers, or as a half-duplex synchronous system that can communicate with peripheral devices, such as A/D or D/A integrated circuits, serial EEPROMs, etc.

The USART can be configured in the following modes:

- Asynchronous (full duplex)
- Synchronous - Master (half duplex)
- Synchronous - Slave (half duplex)

The pins of USART1 and USART2 are multiplexed with the functions of PORTC (RC6/TX1/CK1 and RC7/RX1/DT1) and PORTG (RG1/TX2/CK2 and RG2/RX2/DT2), respectively. In order to configure these pins as a USART:

- For USART1:
 - bit SPEN (RCSTA1<7>) must be set (= 1)
 - bit TRISC<7> must be set (= 1)
 - bit TRISC<6> must be cleared (= 0)
- For USART2:
 - bit SPEN (RCSTA2<7>) must be set (= 1)
 - bit TRISG<2> must be set (= 1)
 - bit TRISG<1> must be cleared (= 0)

Register 18-1 shows the layout of the Transmit Status and Control Registers (TXSTAx) and Register 18-2 shows the layout of the Receive Status and Control Registers (RCSTAx). USART1 and USART2 each have their own independent and distinct pairs of transmit and receive control registers, which are identical to each other apart from their names. Similarly, each USART has its own distinct set of transmit, receive and baud rate registers.

Note: Throughout this section, references to register and bit names that may be associated with a specific USART module are referred to generically by the use of 'x' in place of the specific module number. Thus, "RCSTAx" might refer to the receive status register for either USART1 or USART2.

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REGISTER 18-1: TXSTAx: TRANSMIT STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0	R-1	R/W-0
CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D

bit 7

bit 0

bit 7 **CSRC:** Clock Source Select bit

Asynchronous mode:

Don't care

Synchronous mode:

1 = Master mode (clock generated internally from BRG)

0 = Slave mode (clock from external source)

bit 6 **TX9:** 9-bit Transmit Enable bit

1 = Selects 9-bit transmission

0 = Selects 8-bit transmission

bit 5 **TXEN:** Transmit Enable bit

1 = Transmit enabled

0 = Transmit disabled

Note: SREN/CREN overrides TXEN in SYNC mode.

bit 4 **SYNC:** USART Mode Select bit

1 = Synchronous mode

0 = Asynchronous mode

bit 3 **Unimplemented:** Read as '0'

bit 2 **BRGH:** High Baud Rate Select bit

Asynchronous mode:

1 = High speed

0 = Low speed

Synchronous mode:

Unused in this mode

bit 1 **TRMT:** Transmit Shift Register Status bit

1 = TSR empty

0 = TSR full

bit 0 **TX9D:** 9th bit of Transmit Data

Can be Address/Data bit or a parity bit

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR reset

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

REGISTER 18-2: RCSTAx: RECEIVE STATUS AND CONTROL REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R-0	R-0	R-x
SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D
bit 7							bit 0

- bit 7 **SPEN:** Serial Port Enable bit
 1 = Serial port enabled (configures RX/DT and TX/CK pins as serial port pins)
 0 = Serial port disabled
- bit 6 **RX9:** 9-bit Receive Enable bit
 1 = Selects 9-bit reception
 0 = Selects 8-bit reception
- bit 5 **SREN:** Single Receive Enable bit
Asynchronous mode:
 Don't care
Synchronous mode - Master:
 1 = Enables single receive
 0 = Disables single receive
 This bit is cleared after reception is complete.
Synchronous mode - Slave:
 Don't care
- bit 4 **CREN:** Continuous Receive Enable bit
Asynchronous mode:
 1 = Enables receiver
 0 = Disables receiver
Synchronous mode:
 1 = Enables continuous receive until enable bit CREN is cleared (CREN overrides SREN)
 0 = Disables continuous receive
- bit 3 **ADDEN:** Address Detect Enable bit
Asynchronous mode 9-bit (RX9 = 1):
 1 = Enables address detection, enables interrupt and load of the receive buffer
 when RSR<8> is set
 0 = Disables address detection, all bytes are received, and ninth bit can be used as parity bit
- bit 2 **FERR:** Framing Error bit
 1 = Framing error (can be updated by reading RCREG register and receive next valid byte)
 0 = No framing error
- bit 1 **OERR:** Overrun Error bit
 1 = Overrun error (can be cleared by clearing bit CREN)
 0 = No overrun error
- bit 0 **RX9D:** 9th bit of Received Data
 This can be Address/Data bit or a parity bit, and must be calculated by user firmware

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR reset	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

18.1 USART Baud Rate Generator (BRG)

The BRG supports both the Asynchronous and Synchronous modes of the USARTs. It is a dedicated 8-bit baud rate generator. The SPBRG register controls the period of a free running 8-bit timer. In Asynchronous mode, bit BRGH (TXSTAx<2>) also controls the baud rate. In Synchronous mode, bit BRGH is ignored. Table 18-1 shows the formula for computation of the baud rate for different USART modes, which only apply in Master mode (internal clock).

Given the desired baud rate and Fosc, the nearest integer value for the SPBRGx register can be calculated using the formula in Table 18-1. From this, the error in baud rate can be determined.

Example 18-1 shows the calculation of the baud rate error for the following conditions:

- Fosc = 16 MHz
- Desired Baud Rate = 9600
- BRGH = 0
- SYNC = 0

It may be advantageous to use the high baud rate (BRGH = '1'), even for slower baud clocks. This is because the equation in Example 18-1 can reduce the baud rate error in some cases.

Writing a new value to the SPBRGx register causes the BRG timer to be reset (or cleared). This ensures the BRG does not wait for a timer overflow before outputting the new baud rate.

18.1.1 SAMPLING

The data on the RXx pin (either RC7/RX1/DT1 or RG2/RX2/DT2) is sampled three times by a majority detect circuit to determine if a high or a low level is present at the pin.

EXAMPLE 18-1: CALCULATING BAUD RATE ERROR

Desired Baud Rate	= Fosc / (64 (X + 1))
Solving for X:	
X	= ((Fosc / Desired Baud Rate) / 64) - 1
X	= ((16000000 / 9600) / 64) - 1
X	= [25.042] = 25
Calculated Baud Rate	= 16000000 / (64 (25 + 1))
	= 9615
Error	= $\frac{(\text{Calculated Baud Rate} - \text{Desired Baud Rate})}{\text{Desired Baud Rate}}$
	= $\frac{(9615 - 9600)}{9600}$
	= 0.16%

TABLE 18-1: BAUD RATE FORMULA

SYNC	BRGH = 0 (Low Speed)	BRGH = 1 (High Speed)
0	(Asynchronous) Baud Rate = Fosc/(64(X+1))	Baud Rate = Fosc/(16(X+1))
1	(Synchronous) Baud Rate = Fosc/(4(X+1))	N/A

Legend: X = value in SPBRGx (0 to 255)

TABLE 18-2: REGISTERS ASSOCIATED WITH BAUD RATE GENERATOR

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
TXSTAx	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
RCSTAx	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
SPBRGx	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used by the BRG.

Note: Register names generically refer to both of the identically named registers for the two USART modules, where 'x' indicates the particular module. Bit names and RESET values are identical between modules.

TABLE 18-3: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 0)

BAUD RATE (K)	Fosc = 40 MHz			Fosc = 20 MHz			Fosc = 16 MHz			Fosc = 10 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	NA	—	—									
1.2	NA	—	—	1.221	+1.73	255	1.202	+0.16	207	1.202	+0.16	129
2.4	2.441	-1.70	255	2.404	+0.16	129	2.404	+0.16	103	2.404	+0.16	64
9.6	9.615	-0.16	64	9.469	-1.36	32	9.615	+0.16	25	9.766	+1.73	15
19.2	18.94	+1.38	32	19.53	+1.73	15	19.23	+0.16	12	19.53	+1.73	7
76.8	78.13	-1.70	7	78.13	+1.73	3	83.33	+8.51	2	78.13	+1.73	1
96	89.29	+7.52	6	104.2	+8.51	2	NA	—	—	NA	—	—
300	312.5	-4.00	1	312.5	+4.17	0	NA	—	—	NA	—	—
500	625.0	-20.0	0	NA	—	—	NA	—	—	NA	—	—
HIGH	2.441	—	255	312.5	—	0	250	—	0	156.3	—	0
LOW	625.0	—	0	1.221	—	255	0.977	—	255	0.6104	—	255

BAUD RATE (K)	Fosc = 7.15909 MHz			Fosc = 5.0688 MHz			Fosc = 4 MHz			Fosc = 3.579545 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	NA	—	—	0.31	+3.13	255	0.3005	-0.17	207	0.301	+0.23	185
1.2	1.203	+0.23	92	1.2	0	65	1.202	+1.67	51	1.190	-0.83	46
2.4	2.380	-0.83	46	2.4	0	32	2.404	+1.67	25	2.432	+1.32	22
9.6	9.322	-2.90	11	9.9	+3.13	7	NA	—	—	9.322	-2.90	5
19.2	18.64	-2.90	5	19.8	+3.13	3	NA	—	—	18.64	-2.90	2
76.8	NA	—	—	79.2	+3.13	0	NA	—	—	NA	—	—
96	NA	—	—	NA	—	—	NA	—	—	NA	—	—
300	NA	—	—	NA	—	—	NA	—	—	NA	—	—
500	NA	—	—	NA	—	—	NA	—	—	NA	—	—
HIGH	111.9	—	0	79.2	—	0	62.500	—	0	55.93	—	0
LOW	0.437	—	255	0.3094	—	255	3.906	—	255	0.2185	—	255

BAUD RATE (K)	Fosc = 1 MHz			Fosc = 32.768 kHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
0.3	0.300	+0.16	51	0.256	-14.67	1
1.2	1.202	+0.16	12	NA	—	—
2.4	2.232	-6.99	6	NA	—	—
9.6	NA	—	—	NA	—	—
19.2	NA	—	—	NA	—	—
76.8	NA	—	—	NA	—	—
96	NA	—	—	NA	—	—
300	NA	—	—	NA	—	—
500	NA	—	—	NA	—	—
HIGH	15.63	—	0	0.512	—	0
LOW	0.0610	—	255	0.0020	—	255

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TABLE 18-4: BAUD RATES FOR ASYNCHRONOUS MODE (BRGH = 1)

BAUD RATE (K)	Fosc = 40 MHz			Fosc = 20 MHz			Fosc = 16 MHz			Fosc = 10 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
9.6	9.766	-1.70	255	9.615	+0.16	129	9.615	+0.16	103	9.615	+0.16	64
19.2	19.231	-0.16	129	19.230	+0.16	64	19.230	+0.16	51	18.939	-1.36	32
38.4	38.461	-0.16	64	37.878	-1.36	32	38.461	+0.16	25	39.062	+1.7	15
57.6	58.139	-0.93	42	56.818	-1.36	21	58.823	+2.12	16	56.818	-1.36	10
115.2	113.64	1.38	21	113.63	-1.36	10	111.11	-3.55	8	125	+8.51	4
250	250	0	9	250	0	4	250	0	3	NA	—	—
625	625	0	3	625	0	1	NA	—	—	625	0	0
1250	1250	0	1	1250	0	0	NA	—	—	NA	—	—
BAUD RATE (K)	Fosc = 7.16MHz			Fosc = 5.068 MHz			Fosc = 4 MHz			Fosc = 3.579545 MHz		
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)
9.6	9.520	-0.83	46	9.6	0	32	NA	—	—	9.727	+1.32	22
19.2	19.454	+1.32	22	18.645	-2.94	16	1.202	+0.17	207	18.643	-2.90	11
38.4	37.286	-2.90	11	39.6	+3.12	7	2.403	+0.13	103	37.286	-2.90	5
57.6	55.930	-2.90	7	52.8	-8.33	5	9.615	+0.16	25	55.930	-2.90	3
115.2	111.860	-2.90	3	105.6	-8.33	2	19.231	+0.16	12	111.86	-2.90	1
250	NA	—	—	NA	—	—	NA	—	—	223.72	-10.51	0
625	NA	—	—	NA	—	—	NA	—	—	NA	—	—
1250	NA	—	—	NA	—	—	NA	—	—	NA	—	—
BAUD RATE (K)	Fosc = 1 MHz			Fosc = 32.768 kHz								
	Actual Rate (K)	% Error	SPBRG value (decimal)	Actual Rate (K)	% Error	SPBRG value (decimal)						
9.6	8.928	-6.99	6	NA	—	—						
19.2	20.833	+8.51	2	NA	—	—						
38.4	31.25	-18.61	1	NA	—	—						
57.6	62.5	+8.51	0	NA	—	—						
115.2	NA	—	—	NA	—	—						
250	NA	—	—	NA	—	—						
625	NA	—	—	NA	—	—						
1250	NA	—	—	NA	—	—						

18.2 USART Asynchronous Mode

In this mode, the USARTs use standard non-return-to-zero (NRZ) format (one START bit, eight or nine data bits and one STOP bit). The most common data format is 8 bits. An on-chip dedicated 8-bit baud rate generator can be used to derive standard baud rate frequencies from the oscillator. The USART transmits and receives the L8bit first. The USART's transmitter and receiver are functionally independent, but use the same data format and baud rate. The baud rate generator produces a clock, either 16 or 64 times the bit shift rate, depending on bit BRGH (TXSTAx<2>). Parity is not supported by the hardware, but can be implemented in software (and stored as the ninth data bit). Asynchronous mode is stopped during SLEEP.

Asynchronous mode is selected by clearing bit SYNC (TXSTAx<4>).

The USART Asynchronous module consists of the following important elements:

- Baud Rate Generator
- Sampling Circuit
- Asynchronous Transmitter
- Asynchronous Receiver

18.2.1 USART ASYNCHRONOUS TRANSMITTER

The USART transmitter block diagram is shown in Figure 18-1. The heart of the transmitter is the Transmit (serial) Shift Register (TSR). The shift register obtains its data from the read/write transmit buffer, TXREGx. The TXREGx register is loaded with data in software. The TSR register is not loaded until the STOP bit has been transmitted from the previous load. As soon as the STOP bit is transmitted, the TSR is loaded with new data from the TXREGx register (if available). Once the TXREGx register transfers the data to the TSR register (occurs in one Tcy), the TXREGx register is empty and

flag bit, TXx1IF (PIR1<4> for USART1, PIR3<4> for USART2) is set. This interrupt can be enabled/disabled by setting/clearing enable bit, TXxE (PIE1<4> for USART1, PIE<4> for USART2). Flag bit TXx1IF will be set, regardless of the state of enable bit TXxE and cannot be cleared in software. It will reset only when new data is loaded into the TXREGx register. While flag bit TXIF indicated the status of the TXREGx register, another bit, TRMT (TXSTAx<1>), shows the status of the TSR register. Status bit TRMT is a read only bit, which is set when the TSR register is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty.

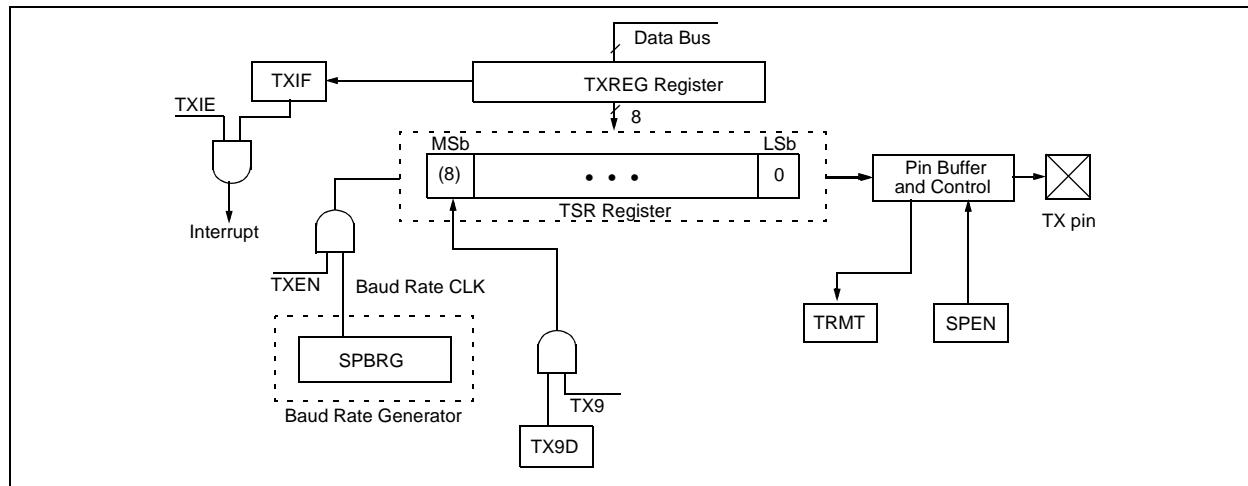
Note 1: The TSR register is not mapped in data memory, so it is not available to the user.

2: Flag bit TXIF is set when enable bit TXEN is set.

To set up an asynchronous transmission:

1. Initialize the SPBRGx register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH (Section 18.1).
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, set enable bit TXxE in the appropriate PIE register.
4. If 9-bit transmission is desired, set transmit bit TX9. Can be used as address/data bit.
5. Enable the transmission by setting bit TXEN, which will also set bit TXIF.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Load data to the TXREGx register (starts transmission).
8. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

FIGURE 18-1: USART TRANSMIT BLOCK DIAGRAM



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FIGURE 18-2: ASYNCHRONOUS TRANSMISSION

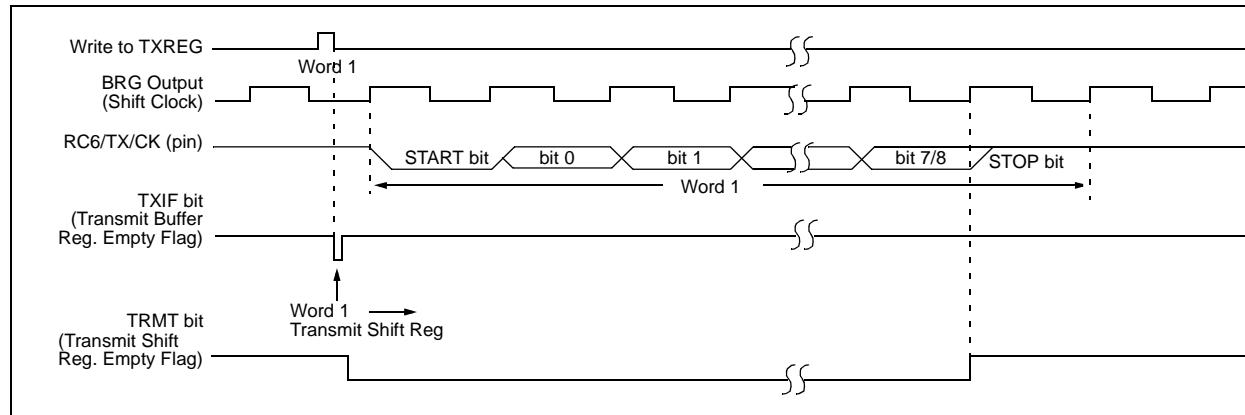


FIGURE 18-3: ASYNCHRONOUS ITRANSMISSION (BACK TO BACK)

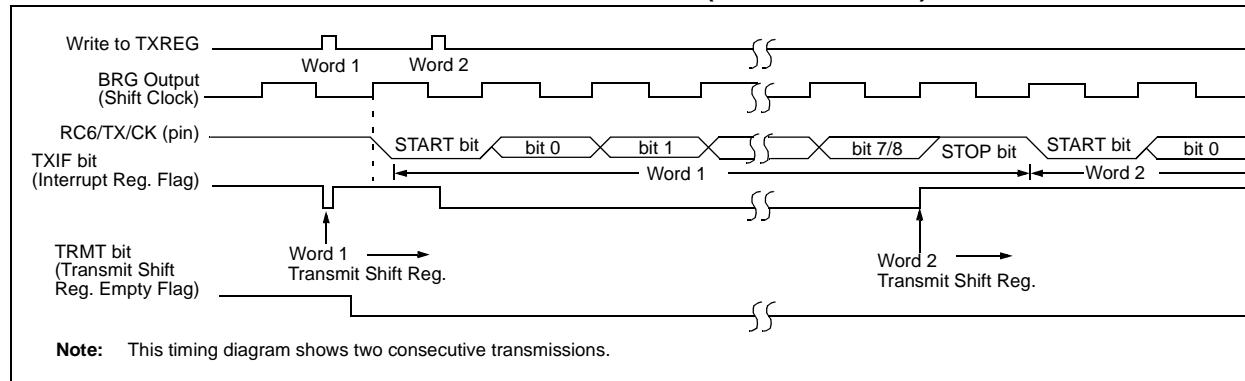


TABLE 18-5: REGISTERS ASSOCIATED WITH ASYNCHRONOUS TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMROIE	INT0IE	RBI	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	0111 1111
PIR3	—	—	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	--00 0000	--00 0000
PIE3	—	—	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	--00 0000	--00 0000
IPR3	—	—	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	--11 1111	--11 1111
RCSTAx ⁽¹⁾	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
TXREGx ⁽¹⁾	USART Transmit Register								0000 0000	0000 0000
TXSTAx ⁽¹⁾	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
SPBRGX ⁽¹⁾	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Transmission.

Note 1: Register names generically refer to both of the identically named registers for the two USART modules, where 'x' indicates the particular module. Bit names and RESET values are identical between modules.

18.2.2 USART ASYNCHRONOUS RECEIVER

The USART receiver block diagram is shown in Figure 18-4. The data is received on the pin (RC7/RX1/DT1 or RG2/RX2/DT2) and drives the data recovery block. The data recovery block is actually a high speed shifter operating at 16 times the baud rate, whereas the main receive serial shifter operates at the bit rate or at Fosc. This mode would typically be used in RS-232 systems.

To set up an Asynchronous Reception:

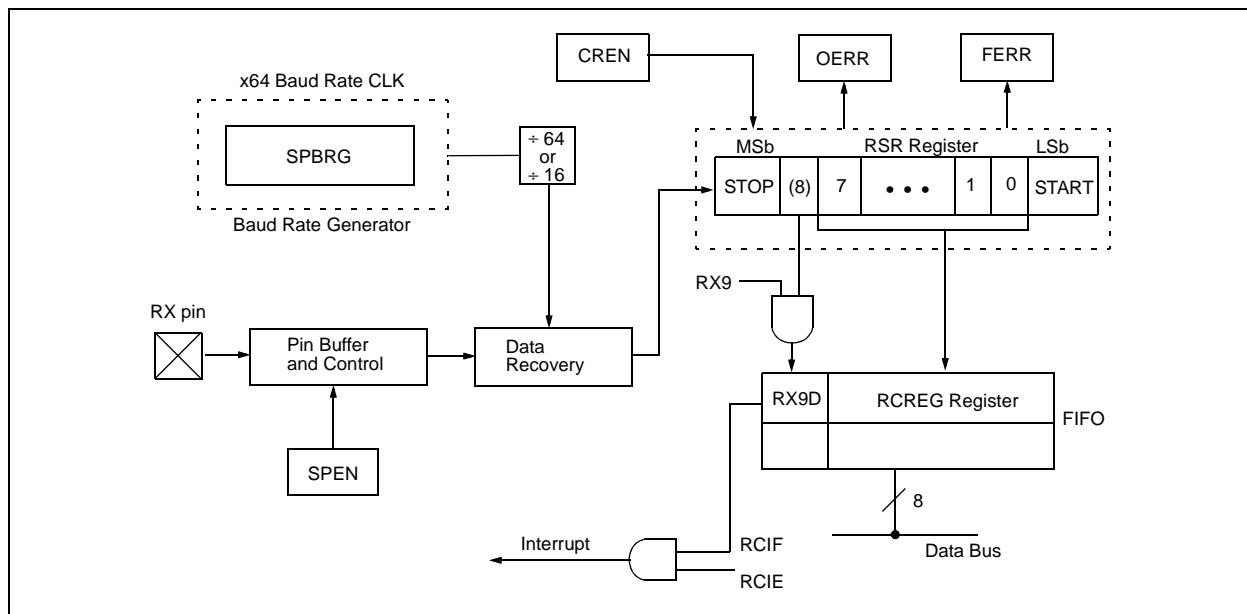
1. Initialize the SPBRG register for the appropriate baud rate. If a high speed baud rate is desired, set bit BRGH (Section 18.1).
2. Enable the asynchronous serial port by clearing bit SYNC and setting bit SPEN.
3. If interrupts are desired, set enable bit RCxIE.
4. If 9-bit reception is desired, set bit RX9.
5. Enable the reception by setting bit CREN.
6. Flag bit RCxIF will be set when reception is complete and an interrupt will be generated if enable bit RCxIE was set.
7. Read the RCSTAx register to get the ninth bit (if enabled) and determine if any error occurred during reception.
8. Read the 8-bit received data by reading the RCREG register.
9. If any error occurred, clear the error by clearing enable bit CREN.
10. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

18.2.3 SETTING UP 9-BIT MODE WITH ADDRESS DETECT

This mode would typically be used in RS-485 systems. To set up an Asynchronous Reception with Address Detect Enable:

1. Initialize the SPBRGx register for the appropriate baud rate. If a high speed baud rate is required, set the BRGH bit.
2. Enable the asynchronous serial port by clearing the SYNC bit and setting the SPEN bit.
3. If interrupts are required, set the RCEN bit and select the desired priority level with the RCIP bit.
4. Set the RX9 bit to enable 9-bit reception.
5. Set the ADDEN bit to enable address detect.
6. Enable reception by setting the CREN bit.
7. The RCxIF bit will be set when reception is complete. The interrupt will be acknowledged if the RCxIE and GIE bits are set.
8. Read the RCSTAx register to determine if any error occurred during reception, as well as read bit 9 of data (if applicable).
9. Read RCREGx to determine if the device is being addressed.
10. If any error occurred, clear the CREN bit.
11. If the device has been addressed, clear the ADDEN bit to allow all received data into the receive buffer and interrupt the CPU.

FIGURE 18-4: USART RECEIVE BLOCK DIAGRAM



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FIGURE 18-5: ASYNCHRONOUS RECEPTION

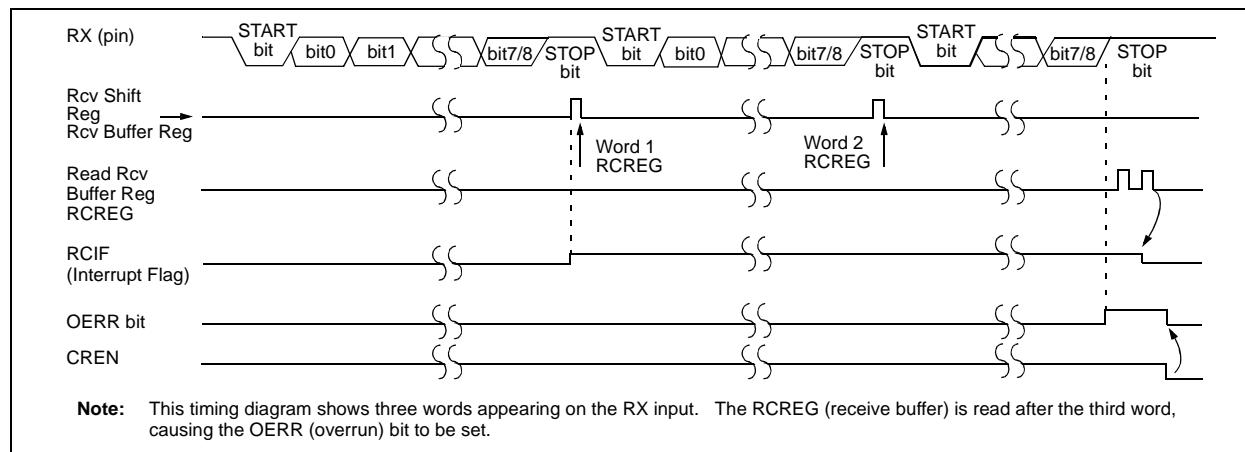


TABLE 18-6: REGISTERS ASSOCIATED WITH ASYNCHRONOUS RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	0111 1111
PIR3	—	—	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	--00 0000	--00 0000
PIE3	—	—	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	--00 0000	--00 0000
IPR3	—	—	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	--11 1111	--11 1111
RCSTAx ⁽¹⁾	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
TXREGx ⁽¹⁾	USART Receive Register								0000 0000	0000 0000
TXSTAx ⁽¹⁾	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
SPBRGx ⁽¹⁾	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented locations read as '0'. Shaded cells are not used for Asynchronous Reception.

Note 1: Register names generically refer to both of the identically named registers for the two USART modules, where 'x' indicates the particular module. Bit names and RESET values are identical between modules.

18.3 USART Synchronous Master Mode

In Synchronous Master mode, the data is transmitted in a half-duplex manner (i.e., transmission and reception do not occur at the same time). When transmitting data, the reception is inhibited and vice versa. Synchronous mode is entered by setting bit SYNC (TXSTAx<4>). In addition, enable bit SPEN (RCSTAx<7>) is set in order to configure the appropriate I/O pins to CK (clock) and DT (data) lines, respectively. The Master mode indicates that the processor transmits the master clock on the CK line. The Master mode is entered by setting bit CSRC (TXSTAx<7>).

18.3.1 USART SYNCHRONOUS MASTER TRANSMISSION

The USART transmitter block diagram is shown in Figure 18-1. The heart of the transmitter is the Transmit (serial) Shift Register (TSR). The shift register obtains its data from the read/write transmit buffer register, TXREG. The TXREGx register is loaded with data in software. The TSR register is not loaded until the last bit has been transmitted from the previous load. As soon as the last bit is transmitted, the TSR is loaded with new data from the TXREGx (if available). Once the TXREGx register transfers the data to the TSR register (occurs in one TCYCLE), the TXREGx is empty and interrupt bit TXxFIF (PIR1<4> for USART1, PIR3<4> for USART2) is set. The interrupt can be enabled/disabled

by setting/clearing enable bit TXxEIE (PIE1<4> for USART1, PIE3<4> for USART2). Flag bit TXxFIF will be set, regardless of the state of enable bit TXxEIE, and cannot be cleared in software. It will reset only when new data is loaded into the TXREGx register. While flag bit TXxFIF indicates the status of the TXREGx register, another bit TRMT (TXSTAx<1>) shows the status of the TSR register. TRMT is a read only bit, which is set when the TSR is empty. No interrupt logic is tied to this bit, so the user has to poll this bit in order to determine if the TSR register is empty. The TSR is not mapped in data memory, so it is not available to the user.

To set up a Synchronous Master Transmission:

1. Initialize the SPBRG register for the appropriate baud rate (Section 18.1).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN, and CSRC.
3. If interrupts are desired, set enable bit TXxEIE in the appropriate PIE register.
4. If 9-bit transmission is desired, set bit TX9.
5. Enable the transmission by setting bit TXEN.
6. If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
7. Start transmission by loading data to the TXREGx register.
8. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

TABLE 18-7: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
PIR1	PSPIF	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	0111 1111
PIR3	—	—	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	--00 0000	--00 0000
PIE3	—	—	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	--00 0000	--00 0000
IPR3	—	—	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	--11 1111	--11 1111
RCSTAx ⁽¹⁾	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
TXREGx ⁽¹⁾	USART Transmit Register								0000 0000	0000 0000
TXSTAx ⁽¹⁾	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
SPBRGx ⁽¹⁾	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for Synchronous Master Transmission.

Note 1: Register names generically refer to both of the identically named registers for the two USART modules, where 'x' indicates the particular module. Bit names and RESET values are identical between modules.

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FIGURE 18-6: SYNCHRONOUS TRANSMISSION

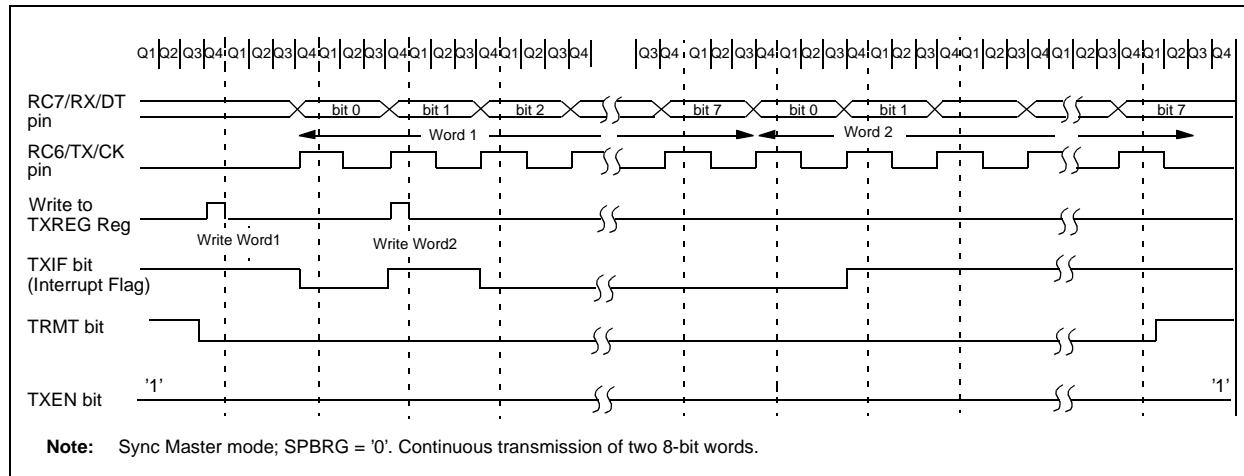
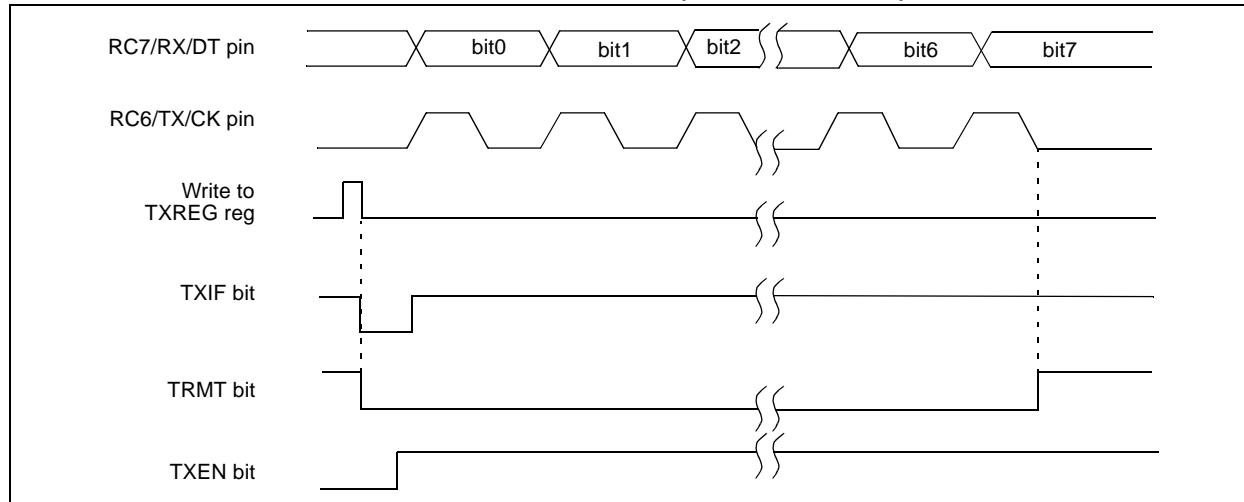


FIGURE 18-7: SYNCHRONOUS TRANSMISSION (THROUGH TXEN)



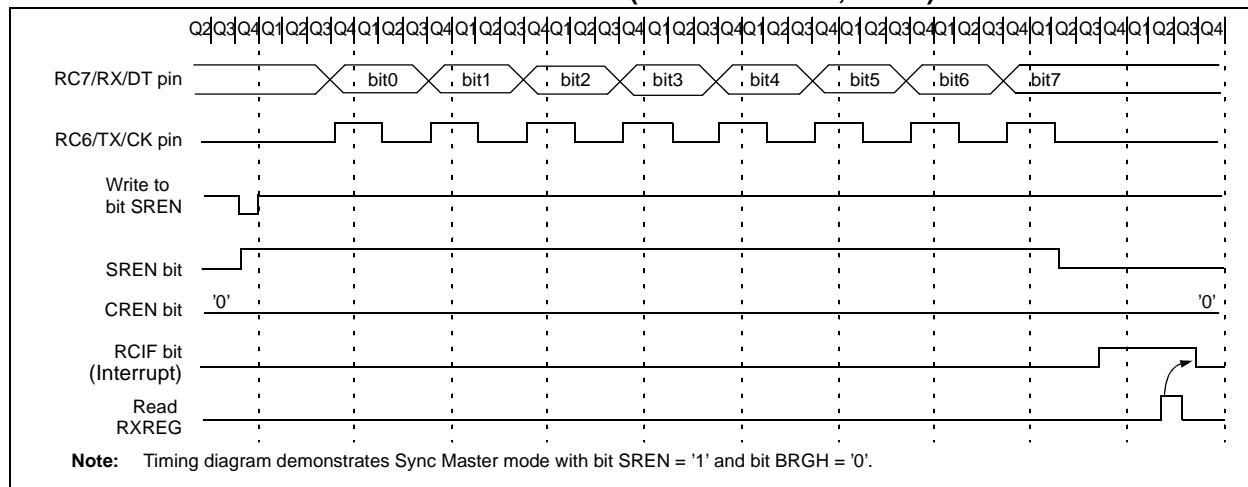
18.3.2 USART SYNCHRONOUS MASTER RECEPTION

Once Synchronous mode is selected, reception is enabled by setting either enable bit SREN (RCSTAx<5>), or enable bit CREN (RCSTAx<4>). Data is sampled on the RXx pin (RC7/RX1/DT1 or RG2/RX2/DT2) on the falling edge of the clock. If enable bit SREN is set, only a single word is received. If enable bit CREN is set, the reception is continuous until CREN is cleared. If both bits are set, then CREN takes precedence.

To set up a Synchronous Master Reception:

1. Initialize the SPBRGx register for the appropriate baud rate (Section 18.1).
2. Enable the synchronous master serial port by setting bits SYNC, SPEN and CSRC.
3. Ensure bits CREN and SREN are clear.
4. If interrupts are desired, set enable bit RCxIE in the appropriate PIE register.
5. If 9-bit reception is desired, set bit RX9.
6. If a single reception is required, set bit SREN. For continuous reception, set bit CREN.
7. Interrupt flag bit RCxF will be set when reception is complete and an interrupt will be generated if the enable bit RCxIE was set.
8. Read the RCSTAx register to get the ninth bit (if enabled) and determine if any error occurred during reception.
9. Read the 8-bit received data by reading the RCREGx register.
10. If any error occurred, clear the error by clearing bit CREN.
11. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

FIGURE 18-8: SYNCHRONOUS RECEPTION (MASTER MODE, SREN)



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TABLE 18-8: REGISTERS ASSOCIATED WITH SYNCHRONOUS MASTER RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/GIEH	PEIE/GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	0111 1111
PIR3	—	—	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	--00 0000	--00 0000
PIE3	—	—	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	--00 0000	--00 0000
IPR3	—	—	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	--11 1111	--11 1111
RCSTAx ⁽¹⁾	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
TXREGx ⁽¹⁾	USART Receive Register								0000 0000	0000 0000
TXSTAx ⁽¹⁾	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
SPBRGx ⁽¹⁾	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for Synchronous Master Reception.

Note 1: Register names generically refer to both of the identically named registers for the two USART modules, where 'x' indicates the particular module. Bit names and RESET values are identical between modules.

18.4 USART Synchronous Slave Mode

Synchronous Slave mode differs from the Master mode in the fact that the shift clock is supplied externally at the TXx pin (RC6/TX1/CK1 or RG1/TX2/CK2), instead of being supplied internally in Master mode. This allows the device to transfer or receive data while in SLEEP mode. Slave mode is entered by clearing bit CSRC (TXSTAx<7>).

18.4.1 USART SYNCHRONOUS SLAVE TRANSMIT

The operation of the Synchronous Master and Slave modes are identical, except in the case of the SLEEP mode.

If two words are written to the TXREG and then the SLEEP instruction is executed, the following will occur:

- The first word will immediately transfer to the TSR register and transmit.
- The second word will remain in TXREG register.
- Flag bit TXxFIF will not be set.
- When the first word has been shifted out of TSR, the TXREGx register will transfer the second word to the TSR and flag bit TXxFIF will now be set.
- If enable bit TXxIE is set, the interrupt will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Transmission:

- Enable the synchronous slave serial port by setting bits SYNC and SPEN and clearing bit CSRC.
- Clear bits CREN and SREN.
- If interrupts are desired, set enable bit TXxIE.
- If 9-bit transmission is desired, set bit TX9.
- Enable the transmission by setting enable bit TXEN.
- If 9-bit transmission is selected, the ninth bit should be loaded in bit TX9D.
- Start transmission by loading data to the TXREGx register.
- If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

TABLE 18-9: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE TRANSMISSION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INT0IE	RBIIE	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	0111 1111
PIR3	—	—	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	--00 0000	--00 0000
PIE3	—	—	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	--00 0000	--00 0000
IPR3	—	—	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	--11 1111	--11 1111
RCSTAx ⁽¹⁾	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	RX9D	0000 000x	0000 000x
TXREGx ⁽¹⁾	USART Transmit Register								0000 0000	0000 0000
TXSTAx ⁽¹⁾	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
SPBRGx ⁽¹⁾	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for Synchronous Slave Transmission.

Note 1: Register names generically refer to both of the identically named registers for the two USART modules, where 'x' indicates the particular module. Bit names and RESET values are identical between modules.

18.4.2 USART SYNCHRONOUS SLAVE RECEPTION

The operation of the Synchronous Master and Slave modes is identical, except in the case of the SLEEP mode and bit SREN, which is a "don't care" in Slave mode.

If receive is enabled by setting bit CREN prior to the SLEEP instruction, then a word may be received during SLEEP. On completely receiving the word, the RSR register will transfer the data to the RCREG register, and if enable bit RCIE bit is set, the interrupt generated will wake the chip from SLEEP. If the global interrupt is enabled, the program will branch to the interrupt vector.

To set up a Synchronous Slave Reception:

1. Enable the synchronous master serial port by setting bits SYNC and SPEN and clearing bit CSRC.
2. If interrupts are desired, set enable bit RCxIE.
3. If 9-bit reception is desired, set bit RX9.
4. To enable reception, set enable bit CREN.
5. Flag bit RCxIF will be set when reception is complete. An interrupt will be generated if enable bit RCxIE was set.
6. Read the RCSTAx register to get the ninth bit (if enabled) and determine if any error occurred during reception.
7. Read the 8-bit received data by reading the RCREGx register.
8. If any error occurred, clear the error by clearing bit CREN.
9. If using interrupts, ensure that the GIE and PEIE bits in the INTCON register (INTCON<7:6>) are set.

TABLE 18-10: REGISTERS ASSOCIATED WITH SYNCHRONOUS SLAVE RECEPTION

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
PIR1	PSPIF	ADIF	RC1IF	TX1IF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSPIE	ADIE	RC1IE	TX1IE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSPIP	ADIP	RC1IP	TX1IP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	0111 1111
PIR3	—	—	RC2IF	TX2IF	TMR4IF	CCP5IF	CCP4IF	CCP3IF	--00 0000	--00 0000
PIE3	—	—	RC2IE	TX2IE	TMR4IE	CCP5IE	CCP4IE	CCP3IE	--00 0000	--00 0000
IPR3	—	—	RC2IP	TX2IP	TMR4IP	CCP5IP	CCP4IP	CCP3IP	--11 1111	--11 1111
RCSTAx ⁽¹⁾	SPEN	RX9	SREN	CREN	ADDEN	FERR	OERR	TX9D	0000 000x	0000 000x
TXREGx ⁽¹⁾	USART Receive Register								0000 0000	0000 0000
TXSTAx ⁽¹⁾	CSRC	TX9	TXEN	SYNC	—	BRGH	TRMT	TX9D	0000 -010	0000 -010
SPBRGx ⁽¹⁾	Baud Rate Generator Register								0000 0000	0000 0000

Legend: x = unknown, - = unimplemented, read as '0'. Shaded cells are not used for Synchronous Slave Reception.

Note 1: Register names generically refer to both of the identically named registers for the two USART modules, where 'x' indicates the particular module. Bit names and RESET values are identical between modules.

19.0 10-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

The analog-to-digital (A/D) converter module has 12 inputs for the PIC18F6X20 devices and 16 for the PIC18F8X20 devices. This module allows conversion of an analog input signal to a corresponding 10-bit digital number.

The module has five registers:

- A/D Result High Register (ADRESH)
- A/D Result Low Register (ADRESL)
- A/D Control Register 0 (ADCON0)
- A/D Control Register 1 ((ADCON1))
- A/D Control Register 2 ((ADCON2))

The ADCON0 register, shown in Register 19-1, controls the operation of the A/D module. The ADCON1 register, shown in Register 19-2, configures the functions of the port pins. The ADCON2, shown in Register 16-3, configures the A/D clock source and justification.

REGISTER 19-1: ADCON0 REGISTER

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	CHS3	CHS2	CHS1	CHS0	GO/DONE	ADON

bit 7

bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-2 **CHS3:CHS0:** Analog Channel Select bits

- 0000 = Channel 0 (AN0)
- 0001 = Channel 1 (AN1)
- 0010 = Channel 2 (AN2)
- 0011 = Channel 3 (AN3)
- 0100 = Channel 4 (AN4)
- 0101 = Channel 5 (AN5)
- 0110 = Channel 6 (AN6)
- 0111 = Channel 7 (AN7)
- 1000 = Channel 8 (AN8)
- 1001 = Channel 9 (AN9)
- 1010 = Channel 10 (AN10)
- 1011 = Channel 11 (AN11)
- 1100 = Channel 12 (AN12)⁽¹⁾
- 1101 = Channel 13 (AN13)⁽¹⁾
- 1110 = Channel 14 (AN14)⁽¹⁾
- 1111 = Channel 15 (AN15)⁽¹⁾

Note 1: These channels are not available on the PIC18F6X20 (64-pin) devices.

bit 1 **GO/DONE:** A/D Conversion Status bit

When ADON = 1:

1 = A/D conversion in progress (setting this bit starts the A/D conversion, which is automatically cleared by hardware when the A/D conversion is complete)

0 = A/D conversion not in progress

bit 0 **ADON:** A/D On bit

1 = A/D converter module is enabled

0 = A/D converter module is disabled

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR reset

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

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REGISTER 19-2: ADCON1 REGISTER

bit 7-6 **Unimplemented:** Read as '0'

bit 5-4 **VCFG1:VCFG0:** Voltage Reference Configuration bits:

VCFG1 VCFG0	A/D VREF+	A/D VREF-
00	AVDD	AVss
01	External VREF+	AVss
10	AVDD	External VREF-
11	External VREF+	External VREF-

bit 3-0 **PCFG3:PCFG0:** A/D Port Configuration Control bits:

A = Analog input D = Digital I/O

Note: Shaded cells indicate A/D channels available only on PIC18F8X20 devices.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 19-3: ADCON2 REGISTER

R/W-0	U-0	U-0	U-0	U-0	R/W-0	R/W-0	R/W-0
ADFM	—	—	—	—	ADCS2	ADCS1	ADCS0
bit 7				bit 0			

bit 7 **ADFM:** A/D Result Format Select bit

1 = Right justified
0 = Left justified

bit 6-3 Unimplemented: Read as '0'

bit 2-0 **ADCS1:ADCS0:** A/D Conversion Clock Select bits

$$000 = \text{Fosc}/2$$

001 = Fosc/8

$$010 = \text{Fosc}/32$$

011 = FRC (clock derived from an RC oscillator = 1 MHz max)

$$100 = F_{osc}/4$$

$$101 = \text{Fosc}/10$$

$$110 = F_{osc}/64$$

111 = FRC (clo)

Legend:

Legend:

R = Readable b

- n = Value at F

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PIC18FXX20

The analog reference voltage is software selectable to either the device's positive and negative supply voltage (VDD and Vss), or the voltage level on the RA3/AN3/VREF+ pin and RA2/AN2/VREF- pin.

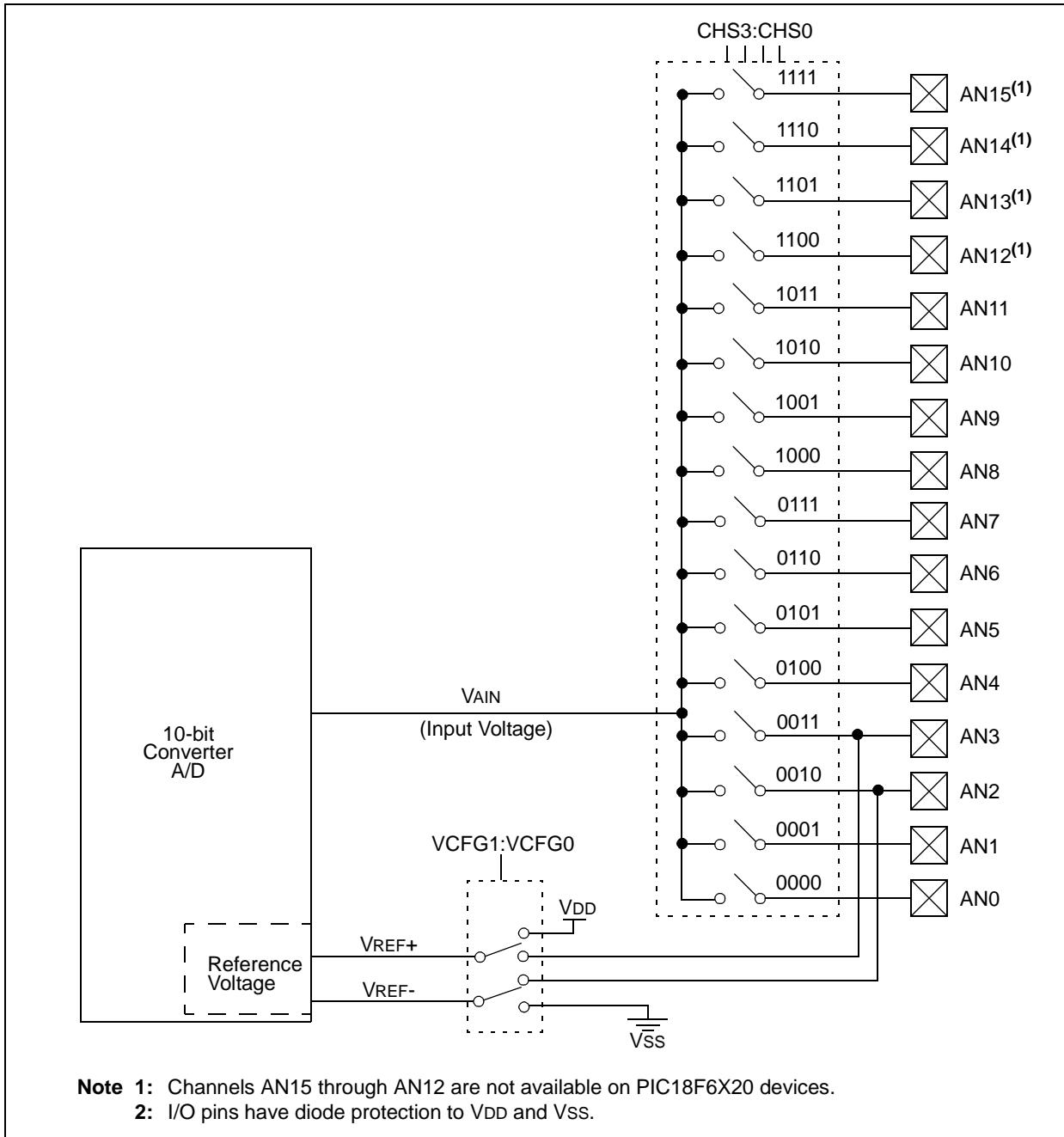
The A/D converter has a unique feature of being able to operate while the device is in SLEEP mode. To operate in SLEEP, the A/D conversion clock must be derived from the A/D's internal RC oscillator.

The output of the sample and hold is the input into the converter, which generates the result via successive approximation.

A device RESET forces all registers to their RESET state. This forces the A/D module to be turned off and any conversion is aborted.

Each port pin associated with the A/D converter can be configured as an analog input (RA3 can also be a voltage reference), or as a digital I/O. The ADRESH and ADRESL registers contain the result of the A/D conversion. When the A/D conversion is complete, the result is loaded into the ADRESH/ADRESL registers, the GO/DONE bit (ADCON0 register) is cleared, and A/D interrupt flag bit, ADIF, is set. The block diagram of the A/D module is shown in Figure 19-1.

FIGURE 19-1: A/D BLOCK DIAGRAM



Note 1: Channels AN15 through AN12 are not available on PIC18F6X20 devices.

2: I/O pins have diode protection to VDD and Vss.

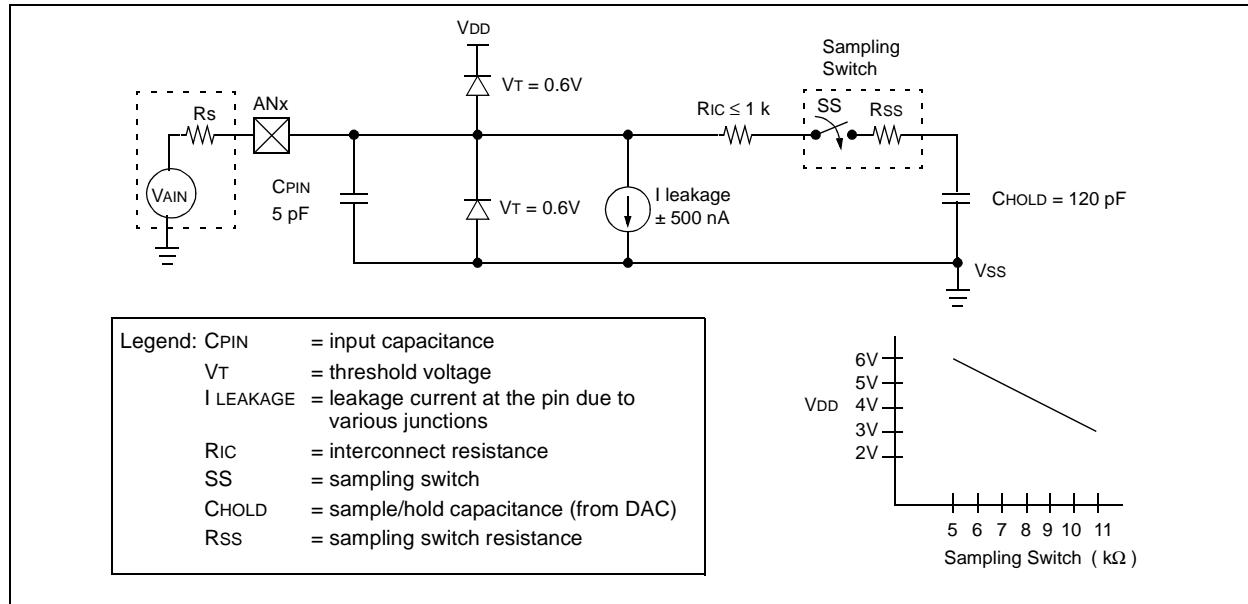
The value in the ADRESH/ADRESL registers is not modified for a Power-on Reset. The ADRESH/ADRESL registers will contain unknown data after a Power-on Reset.

After the A/D module has been configured as desired, the selected channel must be acquired before the conversion is started. The analog input channels must have their corresponding TRIS bits selected as an input. To determine acquisition time, see Section 19.1. After this acquisition time has elapsed, the A/D conversion can be started.

The following steps should be followed to do an A/D conversion:

1. Configure the A/D module:
 - Configure analog pins, voltage reference and digital I/O (ADCON0)
 - Select A/D input channel (ADCON0)
 - Select A/D conversion clock (ADCON2)
 - Turn on A/D module (ADCON0)
2. Configure A/D interrupt (if desired):
 - Clear ADIF bit
 - Set ADIE bit
 - Set GIE bit
3. Wait the required acquisition time.
4. Start conversion:
 - Set GO/DONE bit (ADCON0 register)
5. Wait for A/D conversion to complete, by either:
 - Polling for the GO/DONE bit to be cleared
OR
 - Waiting for the A/D interrupt
6. Read A/D Result registers (ADRESH:ADRESL); clear bit ADIF, if required.
7. For next conversion, go to step 1 or step 2, as required. The A/D conversion time per bit is defined as TAD. A minimum wait of 2 TAD is required before next acquisition starts.

FIGURE 19-2: ANALOG INPUT MODEL



19.1 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 19-2. The source impedance (Rs) and the internal sampling switch (Rss) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (Rss) impedance varies over the device voltage (VDD). The source impedance affects the offset voltage at the analog input (due to pin leakage current). **The maximum recommended impedance for analog sources is 2.5kΩ.** After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

Note: When the conversion is started, the holding capacitor is disconnected from the input pin.

To calculate the minimum acquisition time, Equation 19-1 may be used. This equation assumes that 1/2 LSb error is used (1024 steps for the A/D). The 1/2 LSb error is the maximum error allowed for the A/D to meet its specified resolution.

Example 19-1 shows the calculation of the minimum required acquisition time, TACQ. This calculation is based on the following application system assumptions:

CHOLD	=	120 pF
Rs	=	2.5 kΩ
Conversion Error	≤	1/2 LSb
VDD	=	5V → Rss = 7 kΩ
Temperature	=	50°C (system max.)
VHOLD	=	0V @ time = 0

EQUATION 19-1: ACQUISITION TIME

$$\begin{aligned} TACQ &= \text{Amplifier Settling Time} + \text{Holding Capacitor Charging Time} + \text{Temperature Coefficient} \\ &= TAMP + TC + TCOFF \end{aligned}$$

EQUATION 19-2: A/D MINIMUM CHARGING TIME

$$\begin{aligned} VHOLD &= (VREF - (VREF/2048)) \cdot (1 - e^{(-TC/CHOLD(RIC + RSS + RS))}) \\ \text{or} \\ TC &= -(120 \text{ pF})(1 \text{ kΩ} + RSS + RS) \ln(1/2047) \end{aligned}$$

EXAMPLE 19-1: CALCULATING THE MINIMUM REQUIRED ACQUISITION TIME

$$\begin{aligned} TACQ &= TAMP + TC + TCOFF \\ \text{Temperature coefficient is only required for temperatures } > 25^\circ\text{C.} \\ TACQ &= 2 \mu\text{s} + TC + [(Temp - 25^\circ\text{C})(0.05 \mu\text{s}/^\circ\text{C})] \\ TC &= -CHOLD (RIC + RSS + RS) \ln(1/2047) \\ &\quad -120 \text{ pF} (1 \text{ kΩ} + 7 \text{ kΩ} + 2.5 \text{ kΩ}) \ln(0.0004885) \\ &\quad -120 \text{ pF} (10.5 \text{ kΩ}) \ln(0.0004885) \\ &\quad -1.26 \mu\text{s} (-7.6241) \\ &\quad 9.61 \mu\text{s} \\ TACQ &= 2 \mu\text{s} + 9.61 \mu\text{s} + [(50^\circ\text{C} - 25^\circ\text{C})(0.05 \mu\text{s}/^\circ\text{C})] \\ &\quad 11.61 \mu\text{s} + 1.25 \mu\text{s} \\ &\quad 12.86 \mu\text{s} \end{aligned}$$

19.2 Selecting the A/D Conversion Clock

The A/D conversion time per bit is defined as TAD. The A/D conversion requires 12 TAD per 10-bit conversion. The source of the A/D conversion clock is software selectable. There are seven possible options for TAD:

- 2Tosc
- 4Tosc
- 8Tosc
- 16Tosc
- 32Tosc
- 64Tosc
- Internal RC oscillator

For correct A/D conversions, the A/D conversion clock (TAD) must be selected to ensure a minimum TAD time of 1.6 μ s.

Table 19-1 shows the resultant TAD times derived from the device operating frequencies and the A/D clock source selected.

19.3 Configuring Analog Port Pins

The ADCON1, TRISA, TRISF and TRISH registers control the operation of the A/D port pins. The port pins needed as analog inputs must have their corresponding TRIS bits set (input). If the TRIS bit is cleared (output), the digital output level (VOH or VOL) will be converted.

The A/D operation is independent of the state of the CHS3:CHS0 bits and the TRIS bits.

Note 1: When reading the port register, all pins configured as analog input channels will read as cleared (a low level). Pins configured as digital inputs will convert an analog input. Analog levels on a digitally configured input will not affect the conversion accuracy.

2: Analog levels on any pin defined as a digital input may cause the input buffer to consume current out of the device's specification limits.

TABLE 19-1: TAD vs. DEVICE OPERATING FREQUENCIES

AD Clock Source (TAD)		Maximum Device Frequency	
Operation	ADCS2:ADCS0	PIC18FXX20	PIC18LFXX20 ⁽⁶⁾
2Tosc	000	1.25 MHz	666 kHz
4Tosc	100	2.50 MHz	1.33 MHz
8Tosc	001	5.00 MHz	2.67 MHz
16Tosc	101	10.0 MHz	5.33 MHz
32Tosc	010	20.0 MHz	10.67 MHz
64Tosc	110	40.0 MHz	21.33 MHz
RC	x11	—	—

Note 1: The RC source has a typical TAD time of 4 ms.

2: The RC source has a typical TAD time of 6 ms.

3: These values violate the minimum required TAD time.

4: For faster conversion times, the selection of another clock source is recommended.

5: For device frequencies above 1 MHz, the device must be in SLEEP for the entire conversion or the A/D accuracy may be out of specification.

6: This column is for the LF devices only.

19.4 A/D Conversions

Figure 19-3 shows the operation of the A/D converter after the GO bit has been set. Clearing the GO/DONE bit during a conversion will abort the current conversion. The A/D result register pair will NOT be updated with the partially completed A/D conversion sample. That is, the ADRESH:ADRESL registers will continue to contain the value of the last completed conversion (or the last value written to the ADRESH:ADRESL registers). After the A/D conversion is aborted, a 2 TAD wait is required before the next acquisition is started. After this 2 TAD wait, acquisition on the selected channel is automatically started.

Note: The GO/DONE bit should **NOT** be set in the same instruction that turns on the A/D.

19.5 Use of the CCP2 Trigger

An A/D conversion can be started by the “special event trigger” of the CCP2 module. This requires that the CCP2M3:CCP2M0 bits (CCP2CON<3:0>) be programmed as 1011 and that the A/D module is enabled (ADON bit is set). When the trigger occurs, the GO/DONE bit will be set, starting the A/D conversion, and the Timer1 (or Timer3) counter will be reset to zero. Timer1 (or Timer3) is reset to automatically repeat the A/D acquisition period with minimal software overhead (moving ADRESH/ADRESL to the desired location). The appropriate analog input channel must be selected and the minimum acquisition done before the “special event trigger” sets the GO/DONE bit (starts a conversion).

If the A/D module is not enabled (ADON is cleared), the “special event trigger” will be ignored by the A/D module, but will still reset the Timer1 (or Timer3) counter.

FIGURE 19-3: A/D CONVERSION TAD CYCLES

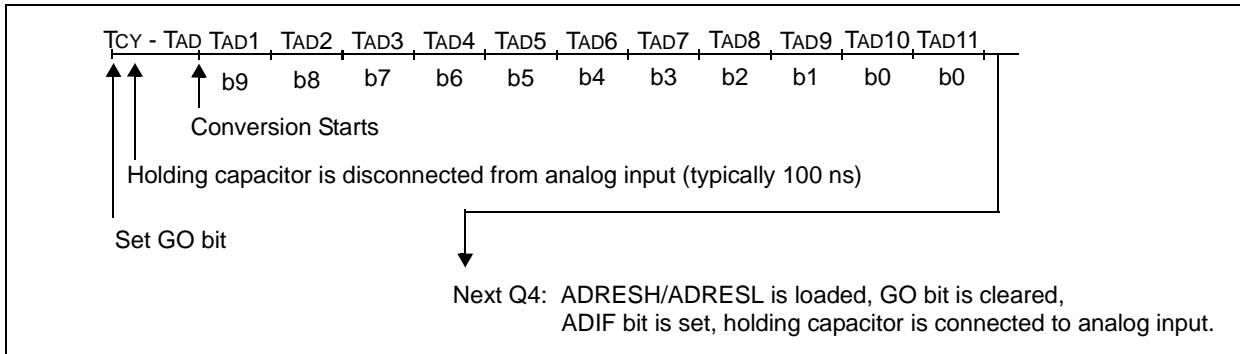


TABLE 19-2: SUMMARY OF A/D REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOR	Value on all other RESETS
INTCON	GIE/ GIEH	PEIE/ GIEL	TMROIE	INT0IE	RBIE	TMROIF	INT0IF	RBIF	0000 0000	0000 0000
PIR1	PSP1F	ADIF	RCIF	TXIF	SSPIF	CCP1IF	TMR2IF	TMR1IF	0000 0000	0000 0000
PIE1	PSP1E	ADIE	RCIE	TXIE	SSPIE	CCP1IE	TMR2IE	TMR1IE	0000 0000	0000 0000
IPR1	PSP1P	ADIP	RCIP	TXIP	SSPIP	CCP1IP	TMR2IP	TMR1IP	0111 1111	0111 1111
PIR2	—	CMIF	—	—	BCLIF	LVDIF	TMR3IF	CCP2IF	-0-- 0000	-0-- 0000
PIE2	—	CMIE	—	—	BCLIE	LVDIE	TMR3IE	CCP2IE	-0-- 0000	-0-- 0000
IPR2	—	CMIP	—	—	BCLIP	LVDIP	TMR3IP	CCP2IP	-0-- 0000	-0-- 0000
ADRESH	A/D Result Register High Byte								xxxx xxxx	uuuu uuuu
ADRESL	A/D Result Register Low Byte								xxxx xxxx	uuuu uuuu
ADCON0	—	—	CHS3	CHS3	CHS1	CHS0	GO/DONE	ADON	--00 0000	--00 0000
ADCON1	—	—	VCFG1	VCFG0	PCFG3	PCFG2	PCFG1	PCFG0	--00 0000	--00 0000
ADCON2	ADFM	—	—	—	—	ADCS2	ADCS1	ADCS0	0--- -000	0--- -000
PORTA	—	RA6	RA5	RA4	RA3	RA2	RA1	RA0	--0x 0000	--0u 0000
TRISA	—	PORTA Data Direction Register							--11 1111	--11 1111
PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	x000 0000	u000 0000
LATF	LATF7	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx xxxx	uuuu uuuu
TRISF	PORTF Data Direction Control Register								1111 1111	1111 1111
PORTH ⁽¹⁾	RH7	RH6	RH5	RH4	RH3	RH2	RH1	RH0	0000 xxxx	0000 xxxx
LATH ⁽¹⁾	LATH7	LATH6	LATH5	LATH4	LATH3	LATH2	LATH1	LATH0	xxxx xxxx	uuuu uuuu
TRISH ⁽¹⁾	PORTH Data Direction Control Register								1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used for A/D conversion.

Note 1: Only available on PIC18F8X20 devices.

PIC18FXX20

NOTES:

20.0 COMPARATOR MODULE

The comparator module contains two analog comparators. The inputs to the comparators are multiplexed with the RF1 through RF6 pins. The on-chip Voltage Reference (Section 21.0) can also be an input to the comparators.

The CMCON register, shown as Register 20-1, controls the comparator input and output multiplexers. A block diagram of the various comparator configurations is shown in Figure 20-1.

REGISTER 20-1: CMCON REGISTER

R-0	R-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0
bit 7							

bit 7	C2OUT: Comparator 2 Output bit <u>When C2INV = 0:</u> 1 = C2 VIN+ > C2 VIN- 0 = C2 VIN+ < C2 VIN- <u>When C2INV = 1:</u> 1 = C2 VIN+ < C2 VIN- 0 = C2 VIN+ > C2 VIN-
bit 6	C1OUT: Comparator 1 Output bit <u>When C1INV = 0:</u> 1 = C1 VIN+ > C1 VIN- 0 = C1 VIN+ < C1 VIN- <u>When C1INV = 1:</u> 1 = C1 VIN+ < C1 VIN- 0 = C1 VIN+ > C1 VIN-
bit 5	C2INV: Comparator 2 Output Inversion bit 1 = C2 output inverted 0 = C2 output not inverted
bit 4	C1INV: Comparator 1 Output Inversion bit 1 = C1 Output inverted 0 = C1 Output not inverted
bit 3	CIS: Comparator Input Switch bit <u>When CM2:CM0 = 110:</u> 1 = C1 VIN- connects to RF5/AN10 C2 VIN- connects to RF3/AN8 0 = C1 VIN- connects to RF6/AN11 C2 VIN- connects to RF4/AN9
bit 2	CM2:CM0: Comparator Mode bits Figure 20-1 shows the Comparator modes and CM2:CM0 bit settings

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

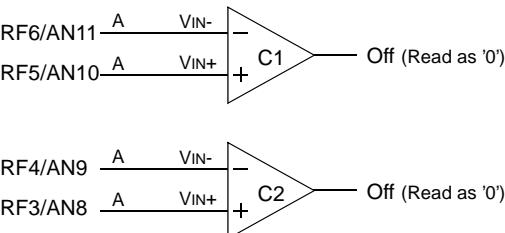
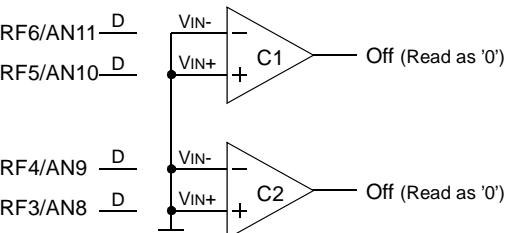
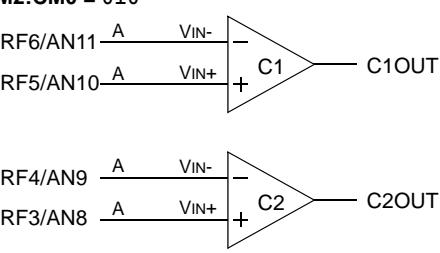
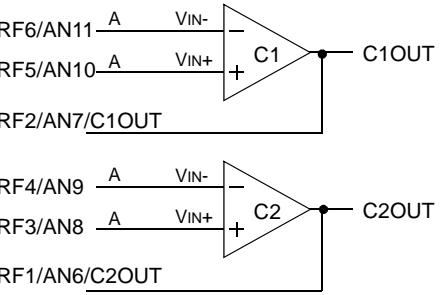
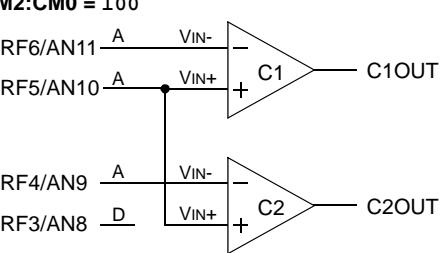
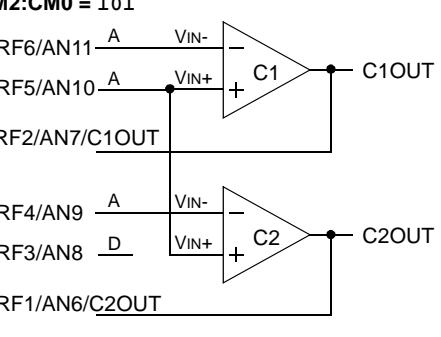
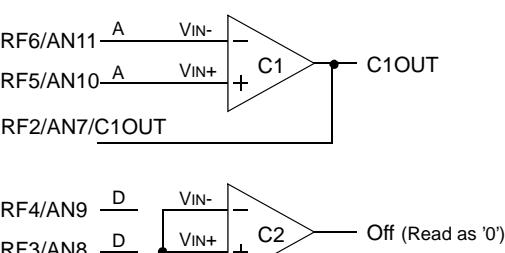
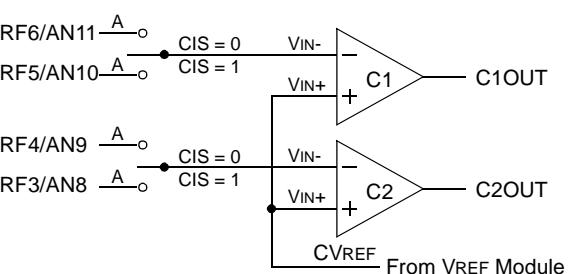
20.1 Comparator Configuration

There are eight modes of operation for the comparators. The CMCON register is used to select these modes. Figure 20-1 shows the eight possible modes. The TRISF register controls the data direction of the comparator pins for each mode. If the Comparator

mode is changed, the comparator output level may not be valid for the specified mode change delay shown in Electrical Specifications (Section 26.0).

Note: Comparator interrupts should be disabled during a Comparator mode change. Otherwise, a false interrupt may occur.

FIGURE 20-1: COMPARATOR I/O OPERATING MODES

Comparators Reset (POR Default Value) CM2:CM0 = 000  <p>RF6/AN11 A V_{IN}- RF5/AN10 A V_{IN}+ + C1 Off (Read as '0') RF4/AN9 A V_{IN}- RF3/AN8 A V_{IN}+ + C2 Off (Read as '0')</p>	Comparators Off CM2:CM0 = 111  <p>RF6/AN11 D V_{IN}- RF5/AN10 D V_{IN}+ + C1 Off (Read as '0') RF4/AN9 D V_{IN}- RF3/AN8 D V_{IN}+ + C2 Off (Read as '0')</p>
Two Independent Comparators CM2:CM0 = 010  <p>RF6/AN11 A V_{IN}- RF5/AN10 A V_{IN}+ + C1 C1OUT RF4/AN9 A V_{IN}- RF3/AN8 A V_{IN}+ + C2 C2OUT</p>	Two Independent Comparators with Outputs CM2:CM0 = 011  <p>RF6/AN11 A V_{IN}- RF5/AN10 A V_{IN}+ + C1 C1OUT RF2/AN7/C1OUT RF4/AN9 A V_{IN}- RF3/AN8 A V_{IN}+ + C2 C2OUT RF1/AN6/C2OUT</p>
Two Common Reference Comparators CM2:CM0 = 100  <p>RF6/AN11 A V_{IN}- RF5/AN10 A V_{IN}+ + C1 C1OUT RF4/AN9 A V_{IN}- RF3/AN8 D V_{IN}+ + C2 C2OUT</p>	Two Common Reference Comparators with Outputs CM2:CM0 = 101  <p>RF6/AN11 A V_{IN}- RF5/AN10 A V_{IN}+ + C1 C1OUT RF2/AN7/C1OUT RF4/AN9 A V_{IN}- RF3/AN8 D V_{IN}+ + C2 C2OUT RF1/AN6/C2OUT</p>
One Independent Comparator with Output CM2:CM0 = 001  <p>RF6/AN11 A V_{IN}- RF5/AN10 A V_{IN}+ + C1 C1OUT RF2/AN7/C1OUT RF4/AN9 D V_{IN}- RF3/AN8 D V_{IN}+ + C2 Off (Read as '0')</p>	Four Inputs Multiplexed to Two Comparators CM2:CM0 = 110  <p>RF6/AN11 A CIS = 0 V_{IN}- RF5/AN10 A CIS = 1 V_{IN}+ + C1 C1OUT RF4/AN9 A CIS = 0 V_{IN}- RF3/AN8 A CIS = 1 V_{IN}+ + C2 C2OUT CVREF From VREF Module</p>

A = Analog Input, port reads zeros always

D = Digital Input

CIS (CMCON<3>) is the Comparator Input Switch

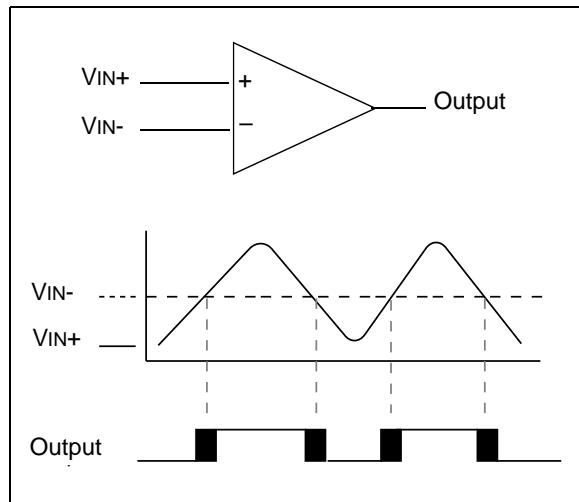
20.2 Comparator Operation

A single comparator is shown in Figure 20-2, along with the relationship between the analog input levels and the digital output. When the analog input at V_{IN+} is less than the analog input V_{IN-} , the output of the comparator is a digital low level. When the analog input at V_{IN+} is greater than the analog input V_{IN-} , the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 20-2 represent the uncertainty, due to input offsets and response time.

20.3 Comparator Reference

An external or internal reference signal may be used, depending on the comparator operating mode. The analog signal present at V_{IN-} is compared to the signal at V_{IN+} , and the digital output of the comparator is adjusted accordingly (Figure 20-2).

FIGURE 20-2: SINGLE COMPARATOR



20.3.1 EXTERNAL REFERENCE SIGNAL

When external voltage references are used, the comparator module can be configured to have the comparators operate from the same, or different reference sources. However, threshold detector applications may require the same reference. The reference signal must be between V_{SS} and V_{DD} , and can be applied to either pin of the comparator(s).

20.3.2 INTERNAL REFERENCE SIGNAL

The comparator module also allows the selection of an internally generated voltage reference for the comparators. Section 21.0 contains a detailed description of the Comparator Voltage Reference Module that provides this signal. The internal reference signal is used when comparators are in mode $CM<2:0> = 110$ (Figure 20-1). In this mode, the internal voltage reference is applied to the V_{IN+} pin of both comparators.

20.4 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output has a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (Section 26.0).

20.5 Comparator Outputs

The comparator outputs are read through the CMCON Register. These bits are read only. The comparator outputs may also be directly output to the RF1 and RF2 I/O pins. When enabled, multiplexors in the output path of the RF1 and RF2 pins will switch and the output of each pin will be the unsynchronized output of the comparator. The uncertainty of each of the comparators is related to the input offset voltage and the response time given in the specifications. Figure 20-3 shows the comparator output block diagram.

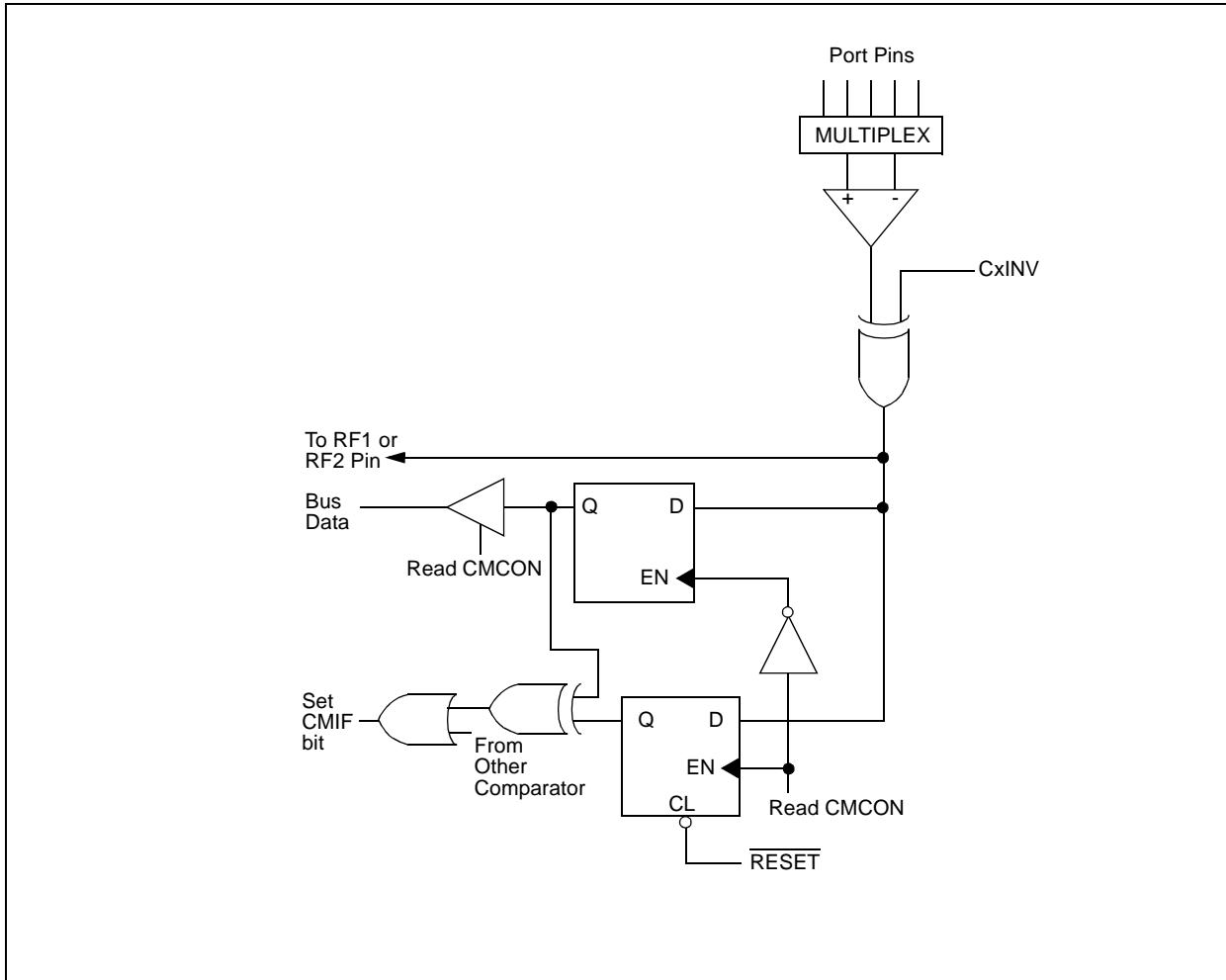
The TRISA bits will still function as an output enable/disable for the RF1 and RF2 pins while in this mode.

The polarity of the comparator outputs can be changed using the C2INV and C1INV bits (CMCON<4:5>).

Note 1: When reading the PORT register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input, according to the Schmitt Trigger input specification.

2: Analog levels on any pin defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 20-3: COMPARATOR OUTPUT BLOCK DIAGRAM



20.6 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of either comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<7:6>, to determine the actual change that occurred. The CMIF bit (PIR registers) is the comparator interrupt flag. The CMIF bit must be RESET by clearing '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit (PIE registers) and the PEIE bit (INTCON register) must be set to enable the interrupt. In addition, the GIE bit must also be set. If any of these bits are clear, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

Note: If a change in the CMCON register (C1OUT or C2OUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF (PIR registers) interrupt flag may not get set.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- Any read or write of CMCON will end the mismatch condition.
- Clear flag bit CMIF.

A mismatch condition will continue to set flag bit CMIF. Reading CMCON will end the mismatch condition, and allow flag bit CMIF to be cleared.

20.7 Comparator Operation During SLEEP

When a comparator is active and the device is placed in SLEEP mode, the comparator remains active and the interrupt is functional, if enabled. This interrupt will wake-up the device from SLEEP mode, when enabled. While the comparator is powered up, higher SLEEP currents than shown in the power-down current specification will occur. Each operational comparator will consume additional current, as shown in the comparator specifications. To minimize power consumption while in SLEEP mode, turn off the comparators, CM<2:0> = 111, before entering SLEEP. If the device wakes up from SLEEP, the contents of the CMCON register are not affected.

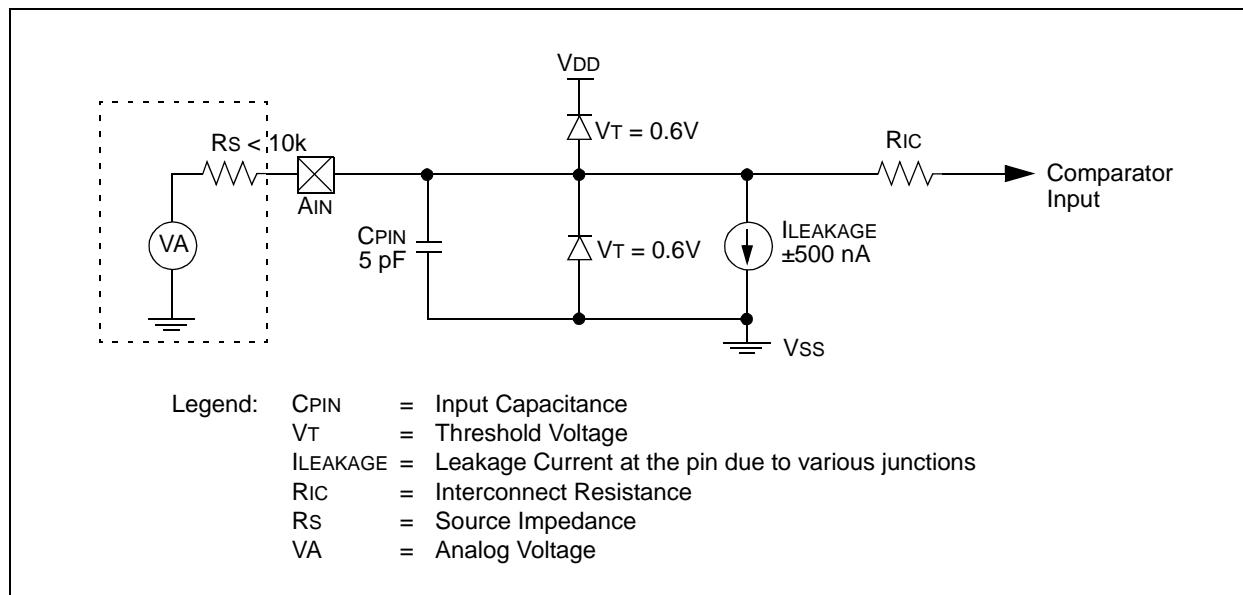
20.8 Effects of a RESET

A device RESET forces the CMCON register to its RESET state, causing the comparator module to be in the comparator RESET mode, CM<2:0> = 000. This ensures that all potential inputs are analog inputs. Device current is minimized when analog inputs are present at RESET time. The comparators will be powered down during the RESET interval.

20.9 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 20-4. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and Vss. The analog input, therefore, must be between Vss and Vdd. If the input voltage deviates from this range by more than 0.6V in either direction, one of the diodes is forward biased and a latchup condition may occur. A maximum source impedance of 10 k Ω is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

FIGURE 20-4: COMPARATOR ANALOG INPUT MODEL



PIC18FXX20

TABLE 20-1: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR	Value on All Other RESETS
CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
CVRCN	CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0	0000 0000	0000 0000
INTCON	GIE/ GIEH	PEIE/ GIEL	TMR0IE	INT0IE	RBIE	TMR0IF	INT0IF	RBIF	0000 0000	0000 0000
PIR2	—	CMIIF	—	—	BCLIF	LVDIF	TMR3IF	CCP2IF	-0-- 0000	-0-- 0000
PIE2	—	CMIE	—	—	BCLIE	LVDIE	TMR3IE	CCP2IE	-0-- 0000	-0-- 0000
IPR2	—	CMIP	—	—	BCLIP	LVDIP	TMR3IP	CCP2IP	-1-- 1111	-1-- 1111
PORTF	RF7	RF6	RF5	RF4	RF3	RF2	RF1	RF0	x000 0000	u000 0000
LATF	LATF7	LATF6	LATF5	LATF4	LATF3	LATF2	LATF1	LATF0	xxxx xxxx	uuuu uuuu
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as "0".

Shaded cells are unused by the comparator module.

21.0 COMPARATOR VOLTAGE REFERENCE MODULE

The Comparator Voltage Reference is a 16-tap resistor ladder network that provides a selectable voltage reference. The resistor ladder is segmented to provide two ranges of CVREF values and has a power-down function to conserve power when the reference is not being used. The CVRCON register controls the operation of the reference as shown in Register 21-1. The block diagram is given in Figure 21-1.

The comparator reference supply voltage can come from either VDD or VSS, or the external VREF+ and VREF- that are multiplexed with RA3 and RA2. The comparator reference supply voltage is controlled by the CVRSS bit.

REGISTER 21-1: CVRCON REGISTER

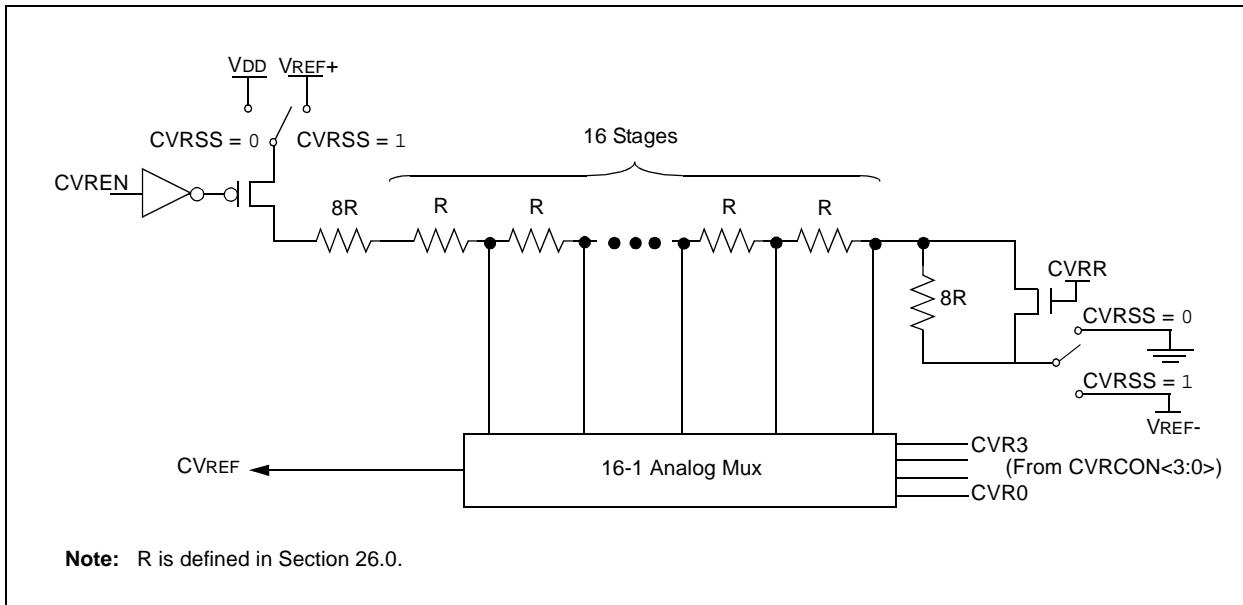
| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| CVREN | CVROE | CVRR | CVRSS | CVR3 | CVR2 | CVR1 | CVR0 |
| bit 7 | | | | bit 0 | | | |

bit 7	CVREN: Comparator Voltage Reference Enable bit 1 = CVREF circuit powered on 0 = CVREF circuit powered down
bit 6	CVROE: Comparator VREF Output Enable bit ⁽¹⁾ 1 = CVREF voltage level is also output on the RF5/AN10/CVREF pin 0 = CVREF voltage is disconnected from the RF5/AN10/CVREF pin
bit 5	CVRR: Comparator VREF Range Selection bit 1 = 0.00 CVRSRC to 0.75 CVRSRC, with CVRSRC/24 step size 0 = 0.25 CVRSRC to 0.75 CVRSRC, with CVRSRC/32 step size
bit 4	CVRSS: Comparator VREF Source Selection bit 1 = Comparator reference source CVRSRC = VREF+ - VREF- 0 = Comparator reference source CVRSRC = VDD - VSS
bit 3-0	CVR3:CVR0: Comparator VREF Value Selection bits (0 ≤ VR3:VR0 ≤ 15) <u>When CVRR = 1:</u> CVREF = (CVR<3:0>/ 24) • (CVRSRC) <u>When CVRR = 0:</u> CVREF = 1/4 • (CVRSRC) + (CVR3:CVR0/ 32) • (CVRSRC)

Note 1: If enabled for output, RF5 must also be configured as an input by setting TRISF<5> to '1'.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

FIGURE 21-1: VOLTAGE REFERENCE BLOCK DIAGRAM



21.2 Voltage Reference Accuracy/Error

The full range of voltage reference cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 21-1) keep $CVREF$ from approaching the reference source rails. The voltage reference is derived from the reference source; therefore, the $CVREF$ output changes with fluctuations in that source. The tested absolute accuracy of the voltage reference can be found in Section 26.0.

21.3 Operation During SLEEP

When the device wakes up from SLEEP through an interrupt or a Watchdog Timer time-out, the contents of the $CVRCON$ register are not affected. To minimize current consumption in SLEEP mode, the voltage reference should be disabled.

21.4 Effects of a RESET

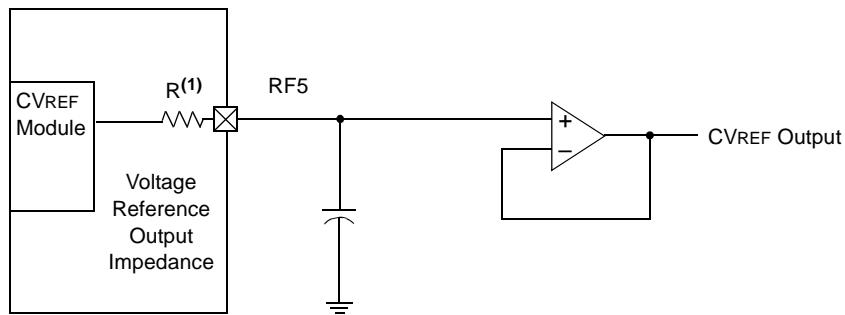
A device RESET disables the voltage reference by clearing bit $CVREN$ ($CVRCON<7>$). This RESET also disconnects the reference from the RA2 pin by clearing bit $CVROE$ ($CVRCON<6>$) and selects the high voltage range by clearing bit $CVRR$ ($CVRCON<5>$). The VRSS value select bits, $CVRCON<3:0>$, are also cleared.

21.5 Connection Considerations

The voltage reference module operates independently of the comparator module. The output of the reference generator may be connected to the RF5 pin if the TRISF<5> bit is set and the CVROE bit is set. Enabling the voltage reference output onto the RF5 pin, with an input signal present, will increase current consumption. Connecting RF5 as a digital output with VRSS enabled will also increase current consumption.

The RF5 pin can be used as a simple D/A output with limited drive capability. Due to the limited current drive capability, a buffer must be used on the voltage reference output for external connections to V_{REF} . Figure 21-2 shows an example buffering technique.

FIGURE 21-2: VOLTAGE REFERENCE OUTPUT BUFFER EXAMPLE



Note 1: R is dependent upon the Voltage Reference Configuration bits CVRCON<3:0> and CVRCON<5>.

TABLE 21-1: REGISTERS ASSOCIATED WITH COMPARATOR VOLTAGE REFERENCE

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value On POR	Value On All Other RESETS
CVRCON	CVREN	CVROE	CVRR	CVRSS	CVR3	CVR2	CVR1	CVR0	0000 0000	0000 0000
CMCON	C2OUT	C1OUT	C2INV	C1INV	CIS	CM2	CM1	CM0	0000 0000	0000 0000
TRISF	TRISF7	TRISF6	TRISF5	TRISF4	TRISF3	TRISF2	TRISF1	TRISF0	1111 1111	1111 1111

Legend: x = unknown, u = unchanged, - = unimplemented, read as "0".

Shaded cells are not used with the comparator voltage reference.

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NOTES:

22.0 LOW VOLTAGE DETECT

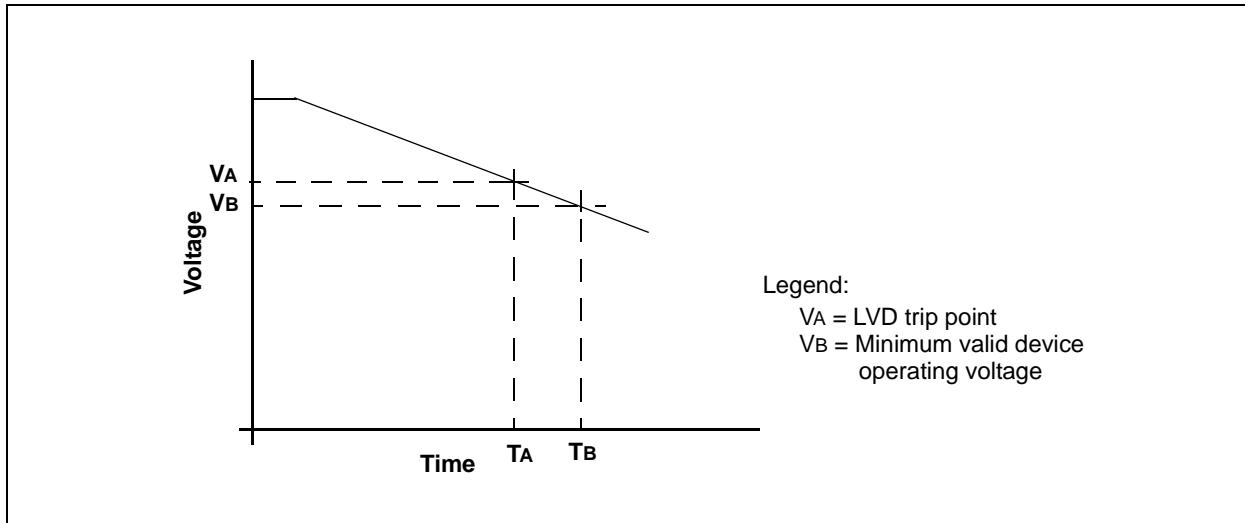
In many applications, the ability to determine if the device voltage (V_{DD}) is below a specified voltage level is a desirable feature. A window of operation for the application can be created, where the application software can do "housekeeping tasks" before the device voltage exits the valid operating range. This can be done using the Low Voltage Detect module.

This module is a software programmable circuitry, where a device voltage trip point can be specified. When the voltage of the device becomes lower than the specified point, an interrupt flag is set. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to that interrupt source.

The Low Voltage Detect circuitry is completely under software control. This allows the circuitry to be "turned off" by the software, which minimizes the current consumption for the device.

Figure 22-1 shows a possible application voltage curve (typically for batteries). Over time, the device voltage decreases. When the device voltage equals voltage V_A , the LVD logic generates an interrupt. This occurs at time T_A . The application software then has the time, until the device voltage is no longer in valid operating range, to shut-down the system. Voltage point V_B is the minimum valid operating voltage specification. This occurs at time T_B . The difference $T_B - T_A$ is the total time for shut-down.

FIGURE 22-1: TYPICAL LOW VOLTAGE DETECT APPLICATION



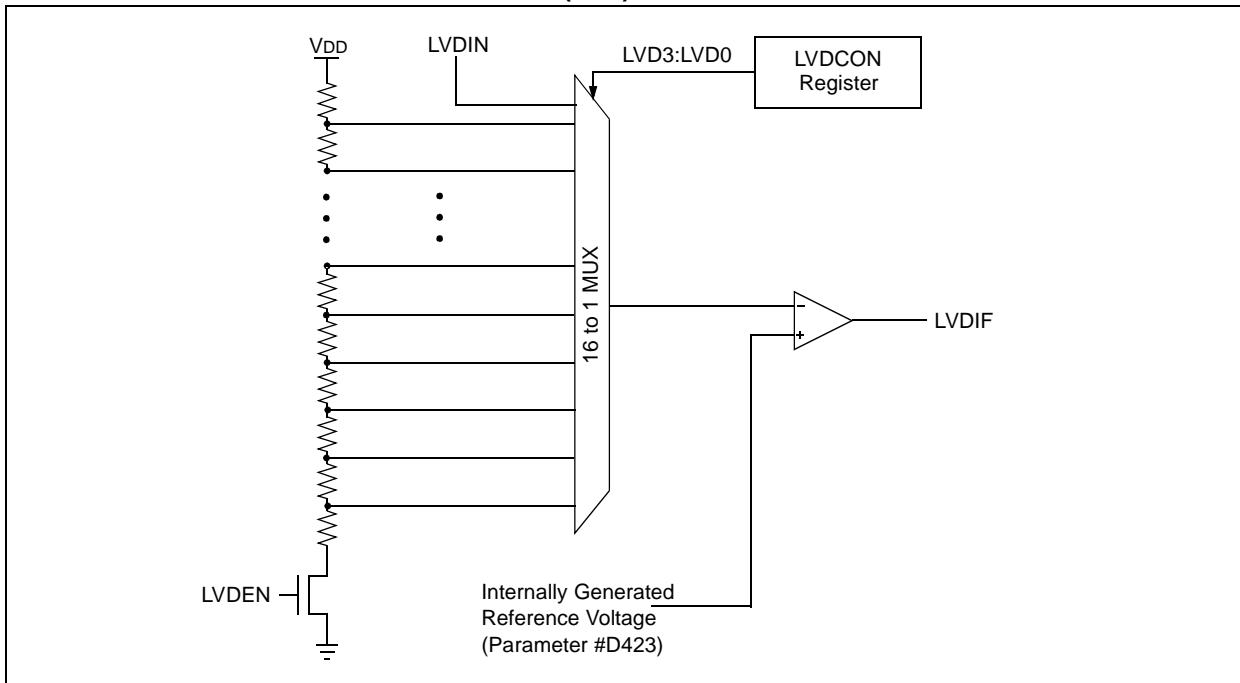
The block diagram for the LVD module is shown in Figure 22-2. A comparator uses an internally generated reference voltage as the set point. When the selected tap output of the device voltage crosses the set point (is lower than), the LVDIF bit is set.

Each node in the resistor divider represents a "trip point" voltage. The "trip point" voltage is the minimum supply voltage level at which the device can operate before the LVD module asserts an interrupt. When the

supply voltage is equal to the trip point, the voltage tapped off of the resistor array is equal to the 1.2V internal reference voltage generated by the voltage reference module. The comparator then generates an interrupt signal setting the LVDIF bit. This voltage is software programmable to any one of 16 values (see Figure 22-2). The trip point is selected by programming the LVLD3:LVLD0 bits (LVDCON<3:0>).

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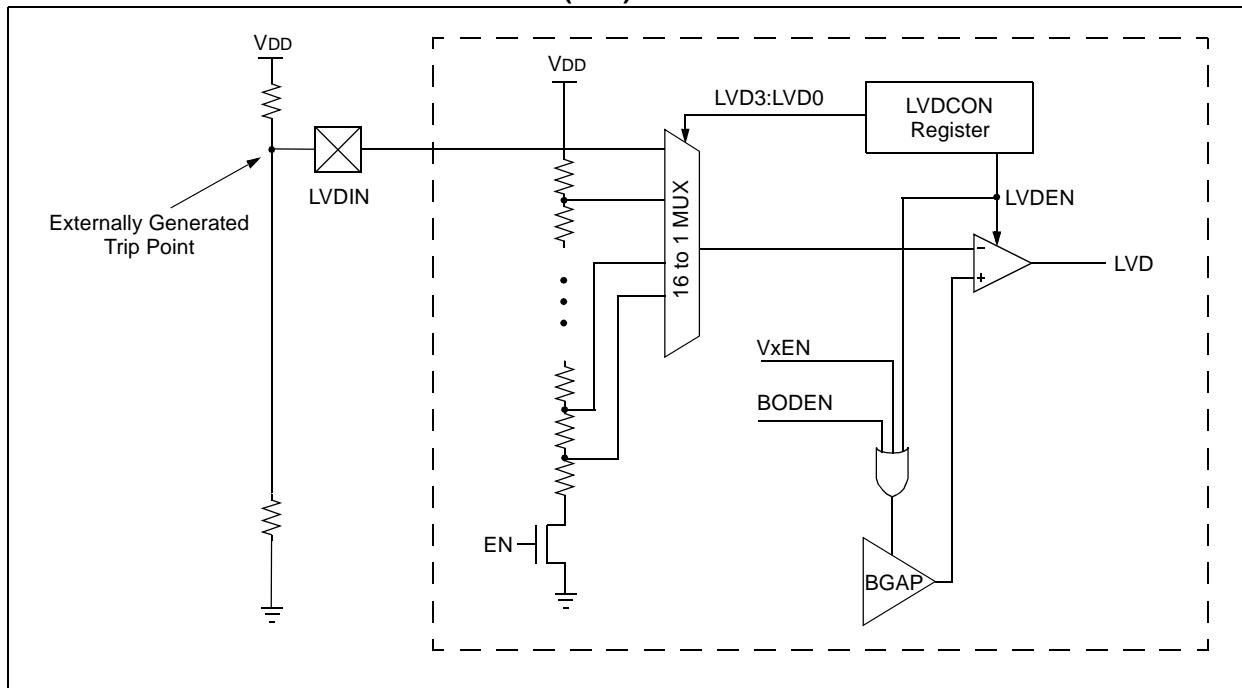
FIGURE 22-2: LOW VOLTAGE DETECT (LVD) BLOCK DIAGRAM



The LVD module has an additional feature that allows the user to supply the trip voltage to the module from an external source. This mode is enabled when bits LVDL3:LVDL0 are set to '1111'. In this state, the comparator input is multiplexed from the external input pin,

LVDIN (Figure 22-3). This gives users flexibility, because it allows them to configure the Low Voltage Detect interrupt to occur at any voltage in the valid operating range.

FIGURE 22-3: LOW VOLTAGE DETECT (LVD) WITH EXTERNAL INPUT BLOCK DIAGRAM



22.1 Control Register

The Low Voltage Detect Control register controls the operation of the Low Voltage Detect circuitry.

REGISTER 22-1: LVDCON REGISTER

U-0	U-0	R-0	R/W-0	R/W-0	R/W-1	R/W-0	R/W-1
—	—	IRVST	LVDEN	LVDL3	LVDL2	LVDL1	LVDL0

- | | |
|---------|--|
| bit 7-6 | Unimplemented: Read as '0' |
| bit 5 | IRVST: Internal Reference Voltage Stable Flag bit
1 = Indicates that the Low Voltage Detect logic will generate the interrupt flag at the specified voltage range
0 = Indicates that the Low Voltage Detect logic will not generate the interrupt flag at the specified voltage range and the LVD interrupt should not be enabled |
| bit 4 | LVDEN: Low Voltage Detect Power Enable bit
1 = Enables LVD, powers up LVD circuit
0 = Disables LVD, powers down LVD circuit |
| bit 3-0 | LVLD3:LVLD0: Low Voltage Detection Limit bits
1111 = External analog input is used (input comes from the LVDIN pin)
1110 = 4.5V - 4.77V
1101 = 4.2V - 4.45V
1100 = 4.0V - 4.24V
1011 = 3.8V - 4.03V
1010 = 3.6V - 3.82V
1001 = 3.5V - 3.71V
1000 = 3.3V - 3.50V
0111 = 3.0V - 3.18V
0110 = 2.8V - 2.97V
0101 = 2.7V - 2.86V
0100 = 2.5V - 2.65V
0011 = 2.4V - 2.54V
0010 = 2.2V - 2.33V
0001 = 2.0V - 2.12V
0000 = Reserved |

Note: LVLD3:LVLD0 modes, which result in a trip point below the valid operating voltage of the device, are not tested.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

22.2 Operation

Depending on the power source for the device voltage, the voltage normally decreases relatively slowly. This means that the LVD module does not need to be constantly operating. To decrease the current requirements, the LVD circuitry only needs to be enabled for short periods, where the voltage is checked. After doing the check, the LVD module may be disabled.

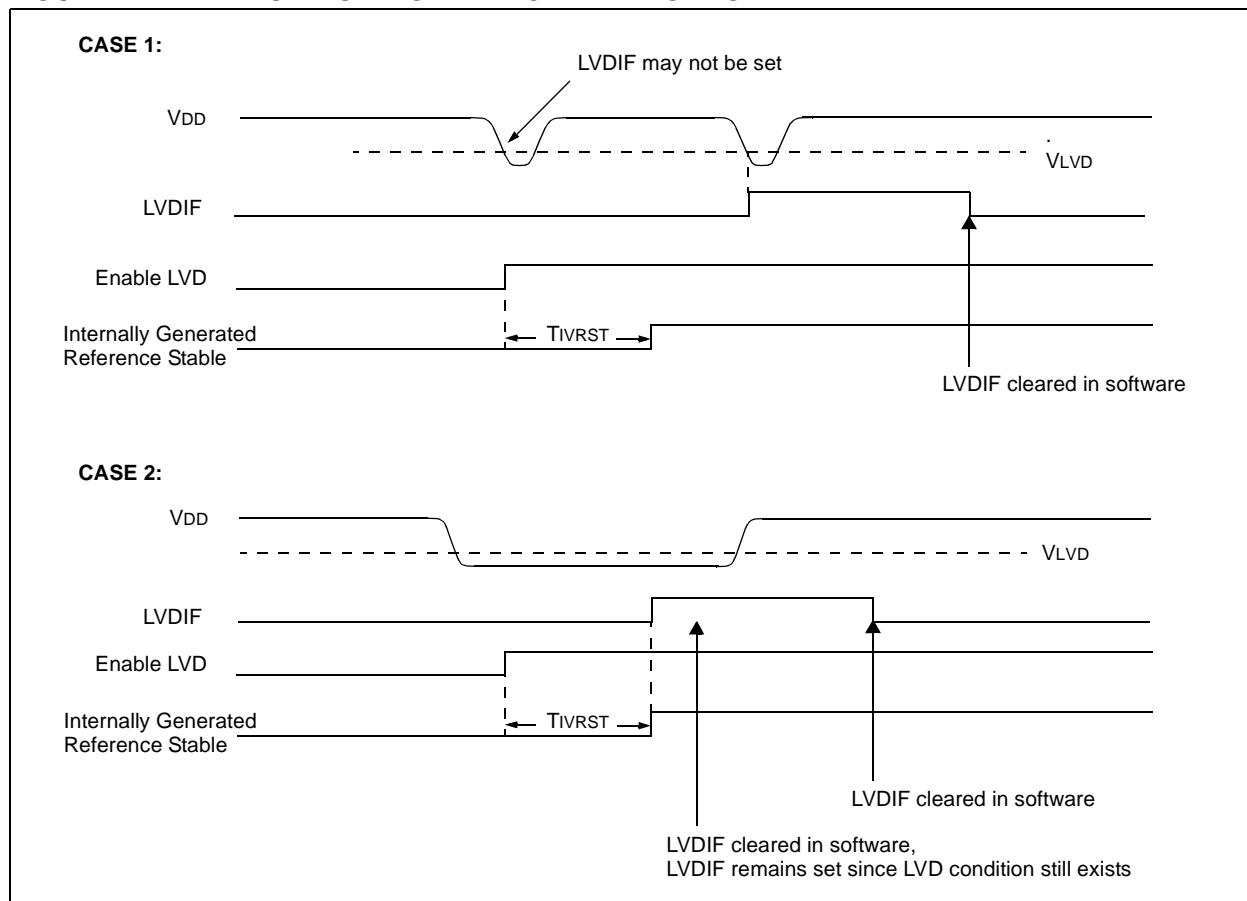
Each time that the LVD module is enabled, the circuitry requires some time to stabilize. After the circuitry has stabilized, all status flags may be cleared. The module will then indicate the proper state of the system.

The following steps are needed to set up the LVD module:

1. Write the value to the LVLD3:LVLD0 bits (LVDCON register), which selects the desired LVD Trip Point.
2. Ensure that LVD interrupts are disabled (the LVDIE bit is cleared or the GIE bit is cleared).
3. Enable the LVD module (set the LVDEN bit in the LVDCON register).
4. Wait for the LVD module to stabilize (the IRVST bit to become set).
5. Clear the LVD interrupt flag, which may have falsely become set, until the LVD module has stabilized (clear the LVDIF bit).
6. Enable the LVD interrupt (set the LVDIE and the GIE bits).

Figure 22-4 shows typical waveforms that the LVD module may be used to detect.

FIGURE 22-4: LOW VOLTAGE DETECT WAVEFORMS



22.2.1 REFERENCE VOLTAGE SET POINT

The Internal Reference Voltage of the LVD module, specified in electrical specification parameter #D423, may be used by other internal circuitry (the Programmable Brown-out Reset). If these circuits are disabled (lower current consumption), the reference voltage circuit requires a time to become stable before a low voltage condition can be reliably detected. This time is invariant of system clock speed. This start-up time is specified in electrical specification parameter #36. The low voltage interrupt flag will not be enabled until a stable reference voltage is reached. Refer to the waveform in Figure 22-4.

22.2.2 CURRENT CONSUMPTION

When the module is enabled, the LVD comparator and voltage divider are enabled and will consume static current. The voltage divider can be tapped from multiple places in the resistor array. Total current consumption, when enabled, is specified in electrical specification parameter #D022B.

22.3 Operation During SLEEP

When enabled, the LVD circuitry continues to operate during SLEEP. If the device voltage crosses the trip point, the LVDIF bit will be set and the device will wake-up from SLEEP. Device execution will continue from the interrupt vector address if interrupts have been globally enabled.

22.4 Effects of a RESET

A device RESET forces all registers to their RESET state. This forces the LVD module to be turned off.

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NOTES:

23.0 SPECIAL FEATURES OF THE CPU

There are several features intended to maximize system reliability, minimize cost through elimination of external components, provide power saving operating modes and offer code protection. These are:

- OSC Selection
- RESET
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Reset (BOR)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code Protection
- ID Locations
- In-Circuit Serial Programming

All PIC18FXX20 devices have a Watchdog Timer, which is permanently enabled via the configuration bits, or software controlled. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay on power-up only, designed to keep the part in RESET while the power supply stabilizes. With these two timers on-chip, most applications need no external RESET circuitry.

SLEEP mode is designed to offer a very low current power-down mode. The user can wake-up from SLEEP through external RESET, Watchdog Timer Wake-up, or through an interrupt. Several oscillator options are also made available to allow the part to fit the application. The RC oscillator option saves system cost, while the LP crystal option saves power. A set of configuration bits are used to select various options.

23.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1'), to select various device configurations. These bits are mapped, starting at program memory location 300000h.

The user will note that address 300000h is beyond the user program memory space. In fact, it belongs to the configuration memory space (300000h through 3FFFFFFh), which can only be accessed using Table Reads and Table Writes.

Programming the configuration registers is done in a manner similar to programming the FLASH memory. The EECON1 register WR bit starts a self-timed write to the configuration register. In normal operation mode, a TBLWT instruction with the TBLPTR pointed to the configuration register sets up the address and the data for the configuration register write. Setting the WR bit starts a long write to the configuration register. The configuration registers are written a byte at a time. To write or erase a configuration cell, a TBLWT instruction can write a '1' or a '0' into the cell.

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TABLE 23-1: CONFIGURATION BITS AND DEVICE IDS

File Name		Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Default/ Unprogrammed Value
300001h	CONFIG1H	—	—	OSCSEN	—	—	FOSC2	FOSC1	FOSC0	--1- -111
300002h	CONFIG2L	—	—	—	—	BORV1	BORV0	BODEN	PWRREN	---- 1111
300003h	CONFIG2H	—	—	—	—	WDTPS2	WDTPS1	WDTPS0	WDTEN	---- 1111
300004h ⁽¹⁾	CONFIG3L	WAIT	—	—	—	—	—	PM1	PM0	1--- --11
300005h	CONFIG3H	—	—	—	—	—	—	—	CCP2MX	---- ---1
300006h	CONFIG4L	DEBUG	—	—	—	—	LVP	—	STVREN	1--- -1-1
300008h	CONFIG5L	CP7 ⁽²⁾	CP6 ⁽²⁾	CP5 ⁽²⁾	CP4 ⁽²⁾	CP3	CP2	CP1	CP0	1111 1111
300009h	CONFIG5H	CPD	CPB	—	—	—	—	—	—	11-- ----
30000Ah	CONFIG6L	WRT7 ⁽²⁾	WRT6 ⁽²⁾	WRT5 ⁽²⁾	WRT4 ⁽²⁾	WRT3	WRT2	WRT1	WRT0	1111 1111
30000Bh	CONFIG6H	WRTD	WRTB	WRTC	—	—	—	—	—	111- ----
30000Ch	CONFIG7L	EBTR7 ⁽²⁾	EBTR6 ⁽²⁾	EBTR5 ⁽²⁾	EBTR4 ⁽²⁾	EBTR3	EBTR2	EBTR1	EBTR0	1111 1111
30000Dh	CONFIG7H	—	EBTRB	—	—	—	—	—	—	-1-- ----
3FFFFEh	DEVID1	DEV2	DEV1	DEVO	REV4	REV3	REV2	REV1	REV0	(3)
3FFFFFh	DEVID2	DEV10	DEV9	DEV8	DEV7	DEV6	DEV5	DEV4	DEV3	0000 0110

Legend: x = unknown, u = unchanged, - = unimplemented, q = value depends on condition.

Shaded cells are unimplemented, read as '0'.

Note 1: Unimplemented in PIC18F6X20 devices; maintain this bit set.

2: Unimplemented in PIC18FX620 devices; maintain this bit set.

3: See Register 23-13 for DEVID1 values.

REGISTER 23-1: CONFIGURATION REGISTER 1 HIGH (CONFIG1H: BYTE ADDRESS 300001h)

U-0	U-0	R/P-1	U-0	U-0	R/P-1	R/P-1	R/P-1
—	—	OSCSEN	—	—	FOSC2	FOSC1	FOSC0

bit 7

bit 0

bit 7-6 **Unimplemented:** Read as '0'bit 5 **OSCSEN:** Oscillator System Clock Switch Enable bit

1 = Oscillator system clock switch option is disabled (main oscillator is source)

0 = Timer1 Oscillator system clock switch option is enabled (oscillator switching is enabled)

bit 4-3 **Unimplemented:** Read as '0'bit 2-0 **FOSC2:FOSC0:** Oscillator Selection bits

111 = RC oscillator w/ OSC2 configured as RA6

110 = HS oscillator with PLL enabled/Clock frequency = (4 x Fosc)

101 = EC oscillator w/ OSC2 configured as RA6

100 = EC oscillator w/ OSC2 configured as divide-by-4 clock output

011 = RC oscillator w/ OSC2 configured as divide-by-4 clock output

010 = HS oscillator

001 = XT oscillator

000 = LP oscillator

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'

- n = Value when device is unprogrammed u = Unchanged from programmed state

REGISTER 23-2: CONFIGURATION REGISTER 2 LOW (CONFIG2L: BYTE ADDRESS 300002h)

U-0	U-0	U-0	U-0	R/P-1	R/P-1	R/P-1	R/P-1
—	—	—	—	BORV1	BORV0	BOREN	PWRTE

bit 7

bit 0

bit 7-4 **Unimplemented:** Read as '0'bit 3-2 **BORV1:BORV0:** Brown-out Reset Voltage bits

11 = VBOR set to 2.5V

10 = VBOR set to 2.7V

01 = VBOR set to 4.2V

00 = VBOR set to 4.5V

bit 1 **BOREN:** Brown-out Reset Enable bit⁽¹⁾

1 = Brown-out Reset enabled

0 = Brown-out Reset disabled

bit 0 **PWRTE:** Power-up Timer Enable bit⁽¹⁾

1 = PWRT disabled

0 = PWRT enabled

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'

- n = Value when device is unprogrammed u = Unchanged from programmed state

REGISTER 23-5: CONFIGURATION REGISTER 3 HIGH (CONFIG3H: BYTE ADDRESS 300005h)

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **CCP2MX:** CCP2 Mux bit

In Microcontroller mode:

1 = CCP2 input/output is multiplexed with RC1
0 = CCP2 input/output is multiplexed with RE7

In Microprocessor, Microprocessor with Boot Block and Extended Microcontroller modes (PIC18F8X20 devices only):

1 = CCP2 input/output is multiplexed with RC1
0 = CCP2 input/output is multiplexed with RB3

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
- n = Value when device is unprogrammed u = Unchanged from programmed state

REGISTER 23-6: CONFIGURATION REGISTER 4 LOW (CONFIG4L: BYTE ADDRESS 300006h)

R/P-1	U-0	U-0	U-0	U-0	R/P-1	U-0	R/P-1
DEBUG	—	—	—	—	LVP	—	STVREN
bit 7							bit 0

bit 7 DEBUG: Background Debugger Enable bit

1 = Background Debugger disabled. RB6 and RB7 configured as general purpose I/O pins.
0 = Background Debugger enabled. RB6 and RB7 are dedicated to In-Circuit Debug.

bit 6-3 **Unimplemented:** Read as '0'

LVP: Low Voltage ICSP Enable bit

1 = Low Voltage ICSP enabled
0 = Low Voltage ICSP disabled

bit 1 **Unimplemented:** Read as '0'

STVREN: Stack Full/I Underflow Reset Enable bit

1 = Stack Full/Underflow will cause RESET
0 = Stack Full/Underflow will not cause RESET

Legend:

Legend: P = Readable bit U = Programmable bit UU = Unimplemented bit, read as '0'

- p = Value when device is unprogrammed u = Unchanged from programmed state

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REGISTER 23-7: CONFIGURATION REGISTER 5 LOW (CONFIG5L: BYTE ADDRESS 300008h)

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
CP7 ⁽¹⁾	CP6 ⁽¹⁾	CP5 ⁽¹⁾	CP4 ⁽¹⁾	CP3	CP2	CP1	CP0
bit 7				bit 0			

- | | |
|-------|---|
| bit 7 | CP7: Code Protection bit ⁽¹⁾ |
| | 1 = Block 7 (01C000-01FFFFh) not code protected |
| | 0 = Block 7 (01C000-01FFFFh) code protected |
| bit 6 | CP6: Code Protection bit ⁽¹⁾ |
| | 1 = Block 6 (018000-01BFFFh) not code protected |
| | 0 = Block 6 (018000-01BFFFh) code protected |
| bit 5 | CP5: Code Protection bit ⁽¹⁾ |
| | 1 = Block 5 (014000-017FFFh) not code protected |
| | 0 = Block 5 (014000-017FFFh) code protected |
| bit 4 | CP4: Code Protection bit ⁽¹⁾ |
| | 1 = Block 4 (010000-013FFFh) not code protected |
| | 0 = Block 4 (010000-013FFFh) code protected |
| bit 3 | CP3: Code Protection bit |
| | 1 = Block 3 (00C000-00FFFFFFh) not code protected |
| | 0 = Block 3 (00C000-00FFFFFFh) code protected |
| bit 2 | CP2: Code Protection bit |
| | 1 = Block 2 (008000-00BFFFh) not code protected |
| | 0 = Block 2 (008000-00BFFFh) code protected |
| bit 1 | CP1: Code Protection bit |
| | 1 = Block 1 (004000-007FFFh) not code protected |
| | 0 = Block 1 (004000-007FFFh) code protected |
| bit 0 | CP0: Code Protection bit |
| | 1 = Block 0 (000200-003FFFh) not code protected |
| | 0 = Block 0 (000200-003FFFh) code protected |

Note 1: Unimplemented in PIC18FX620 devices; maintain this bit set.

Legend:
R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
- n = Value when device is unprogrammed u = Unchanged from programmed state

REGISTER 23-8: CONFIGURATION REGISTER 5 HIGH (CONFIG5H: BYTE ADDRESS 300009h)

R/C-1	R/C-1	U-0	U-0	U-0	U-0	U-0	U-0
CPD	CPB	—	—	—	—	—	—
bit 7				bit 0			

- | | |
|---------|--|
| bit 7 | CPD: Data EEPROM Code Protection bit
1 = Data EEPROM not code protected
0 = Data EEPROM code protected |
| bit 6 | CPB: Boot Block Code Protection bit
1 = Boot Block (000000-0001FFh) not code protected
0 = Boot Block (000000-0001FFh) code protected |
| bit 5-0 | Unimplemented: Read as '0' |

Legend:

R = Readable bit	C = Clearable bit	U = Unimplemented bit, read as '0'
- n = Value when device is unprogrammed		u = Unchanged from programmed state

REGISTER 23-9: CONFIGURATION REGISTER 6 LOW (CONFIG6L: BYTE ADDRESS 30000Ah)

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
WRT7 ⁽¹⁾	WRT6 ⁽¹⁾	WRT5 ⁽¹⁾	WRT4 ⁽¹⁾	WRT3	WRT2	WRT1	WRT0
bit 7							bit 0

- bit 7 **WR7:** Write Protection bit⁽¹⁾
 1 = Block 7 (01C000-01FFFFh) not write protected
 0 = Block 7 (01C000-01FFFFh) write protected
- bit 6 **WR6:** Write Protection bit⁽¹⁾
 1 = Block 6 (018000-01BFFFh) not write protected
 0 = Block 6 (018000-01BFFFh) write protected
- bit 5 **WR5:** Write Protection bit⁽¹⁾
 1 = Block 5 (014000-017FFFh) not write protected
 0 = Block 5 (014000-017FFFh) write protected
- bit 4 **WR4:** Write Protection bit⁽¹⁾
 1 = Block 4 (010000-013FFFh) not write protected
 0 = Block 4 (010000-013FFFh) write protected
- bit 3 **WR3:** Write Protection bit
 1 = Block 3 (00C000-00FFFFh) not write protected
 0 = Block 3 (00C000-00FFFFh) write protected
- bit 2 **WR2:** Write Protection bit
 1 = Block 2 (008000-00BFFFh) not write protected
 0 = Block 2 (008000-00BFFFh) write protected
- bit 1 **WR1:** Write Protection bit
 1 = Block 1 (004000-007FFFh) not write protected
 0 = Block 1 (004000-007FFFh) write protected
- bit 0 **WR0:** Write Protection bit
 1 = Block 0 (000200-003FFFh) not write protected
 0 = Block 0 (000200-003FFFh) write protected

Note 1: Unimplemented in PIC18FX620 devices; maintain this bit set.

Legend:

R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'
- n = Value when device is unprogrammed		u = Unchanged from programmed state

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REGISTER 23-10: CONFIGURATION REGISTER 6 HIGH (CONFIG6H: BYTE ADDRESS 30000Bh)

R/P-1	R/P-1	R-1	U-0	U-0	U-0	U-0	U-0
WRTD	WRTB	WR ⁽¹⁾	—	—	—	—	—
bit 7				bit 0			

- | | |
|---------|---|
| bit 7 | WRTD: Data EEPROM Write Protection bit
1 = Data EEPROM not write protected
0 = Data EEPROM write protected |
| bit 6 | WRTB: Boot Block Write Protection bit
1 = Boot Block (000000-0001FFh) not write protected
0 = Boot Block (000000-0001FFh) write protected |
| bit 5 | WRTC: Configuration Register Write Protection bit ⁽¹⁾
1 = Configuration registers (300000-3000FFh) not write protected
0 = Configuration registers (300000-3000FFh) write protected |
| bit 4-0 | Note 1: This bit is read only, and cannot be changed in user mode
Unimplemented: Read as '0' |

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
- n = Value when device is unprogrammed u = Unchanged from programmed state

REGISTER 23-11: CONFIGURATION REGISTER 7 LOW (CONFIG7L: BYTE ADDRESS 30000Ch)

R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1	R/P-1
EBTR7 ⁽¹⁾	EBTR6 ⁽¹⁾	EBTR5 ⁽¹⁾	EBTR4 ⁽¹⁾	EBTR3	EBTR2	EBTR1	EBTR0
bit 7							bit 0

- bit 7 **EBTR7:** Table Read Protection bit⁽¹⁾
 1 = Block 3 (01C000-01FFFFh) not protected from Table Reads executed in other blocks
 0 = Block 3 (01C000-01FFFFh) protected from Table Reads executed in other blocks
- bit 6 **EBTR6:** Table Read Protection bit⁽¹⁾
 1 = Block 2 (018000-01BFFFh) not protected from Table Reads executed in other blocks
 0 = Block 2 (018000-01BFFFh) protected from Table Reads executed in other blocks
- bit 5 **EBTR5:** Table Read Protection bit⁽¹⁾
 1 = Block 1 (014000-017FFFh) not protected from Table Reads executed in other blocks
 0 = Block 1 (014000-017FFFh) protected from Table Reads executed in other blocks
- bit 4 **EBTR4:** Table Read Protection bit⁽¹⁾
 1 = Block 0 (010000-013FFFh) not protected from Table Reads executed in other blocks
 0 = Block 0 (010000-013FFFh) protected from Table Reads executed in other blocks
- bit 3 **EBTR3:** Table Read Protection bit
 1 = Block 3 (00C000-00FFFFh) not protected from Table Reads executed in other blocks
 0 = Block 3 (00C000-00FFFFh) protected from Table Reads executed in other blocks
- bit 2 **EBTR2:** Table Read Protection bit
 1 = Block 2 (008000-00BFFFh) not protected from Table Reads executed in other blocks
 0 = Block 2 (008000-00BFFFh) protected from Table Reads executed in other blocks
- bit 1 **EBTR1:** Table Read Protection bit
 1 = Block 1 (004000-007FFFh) not protected from Table Reads executed in other blocks
 0 = Block 1 (004000-007FFFh) protected from Table Reads executed in other blocks
- bit 0 **EBTR0:** Table Read Protection bit
 1 = Block 0 (000200-003FFFh) not protected from Table Reads executed in other blocks
 0 = Block 0 (000200-003FFFh) protected from Table Reads executed in other blocks

Note 1: Unimplemented in PIC18FX620 devices; maintain this bit set.

Legend:

R = Readable bit	P = Programmable bit	U = Unimplemented bit, read as '0'
- n = Value when device is unprogrammed		u = Unchanged from programmed state

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REGISTER 23-12: CONFIGURATION REGISTER 7 HIGH (CONFIG7H: BYTE ADDRESS 30000Dh)

U-0	R/P-1	U-0	U-0	U-0	U-0	U-0	U-0
—	EBTRB	—	—	—	—	—	—

- | | |
|---------|--|
| bit 7 | Unimplemented: Read as '0' |
| bit 6 | EBTRB: Boot Block Table Read Protection bit
1 = Boot Block (000000-0001FFh) not protected from Table Reads executed in other blocks
0 = Boot Block (000000-0001FFh) protected from Table Reads executed in other blocks |
| bit 5-0 | Unimplemented: Read as '0' |

Legend:

R = Readable bit P = Programmable bit U = Unimplemented bit, read as '0'
 - n = Value when device is unprogrammed u = Unchanged from programmed state

REGISTER 23-13: DEVICE ID REGISTER 1 FOR PIC18FXX20 DEVICES (ADDRESS 3FFFFEh)

- | | |
|---------|--|
| bit 7-5 | DEV2:DEV0: Device ID bits |
| | 000 = PIC18F8720 |
| | 001 = PIC18F6720 |
| | 100 = PIC18F8620 |
| | 101 = PIC18F6620 |
| bit 4-0 | REV4:REV0: Revision ID bits |
| | These bits are used to indicate the device revision. |

Legend:

R = Readable bit **P** = Programmable bit **U** = Unimplemented bit, read as '0'
- n = Value when device is unprogrammed **u** = Unchanged from programmed state

REGISTER 23-14: DEVICE ID REGISTER 2 FOR PIC18FXX20 DEVICES (ADDRESS 3FFFFFh)

- bit 7-0 DEV10:DEV3:** Device ID bits
These bits are used with the DEV2:DEV0 bits in the Device ID Register 1 to identify the part number

Legend:

R = Readable bit P =Programmable bit U = Unimplemented bit, read as '0'
 - n = Value when device is unprogrammed u = Unchanged from programmed state

23.2 Watchdog Timer (WDT)

The Watchdog Timer is a free running on-chip RC oscillator, which does not require any external components. This RC oscillator is separate from the RC oscillator of the OSC1/CLKI pin. That means that the WDT will run, even if the clock on the OSC1/CLKI and OSC2/CLKO/RA6 pins of the device has been stopped, for example, by execution of a SLEEP instruction.

During normal operation, a WDT time-out generates a device RESET (Watchdog Timer Reset). If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation (Watchdog Timer Wake-up). The TO bit in the RCON register will be cleared upon a WDT time-out.

The Watchdog Timer is enabled/disabled by a device configuration bit. If the WDT is enabled, software execution may not disable this function. When the WDTEN configuration bit is cleared, the SWDTEN bit enables/disables the operation of the WDT.

The WDT time-out period values may be found in the Electrical Specifications section under parameter #31. Values for the WDT postscaler may be assigned using the configuration bits.

Note 1: The CLRWD and SLEEP instructions clear the WDT and the postscaler, if assigned to the WDT and prevent it from timing out and generating a device RESET condition.

2: When a CLRWD instruction is executed and the postscaler is assigned to the WDT, the postscaler count will be cleared, but the postscaler assignment is not changed.

23.2.1 CONTROL REGISTER

Register 23-15 shows the WDTCON register. This is a readable and writable register, which contains a control bit that allows software to override the WDT enable configuration bit, only when the configuration bit has disabled the WDT.

REGISTER 23-15: WDTCON REGISTER

U-0	R/W-0						
—	—	—	—	—	—	—	SWDTEN

bit 7

bit 0

bit 7-1 **Unimplemented:** Read as '0'

bit 0 **SWDTEN:** Software Controlled Watchdog Timer Enable bit

1 = Watchdog Timer is on

0 = Watchdog Timer is turned off if the WDTEN configuration bit in the configuration register = '0'

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR reset

'1' = Bit is set

'0' = Bit is cleared x = Bit is unknown

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23.2.2 WDT POSTSCALER

The WDT has a postscaler that can extend the WDT Reset period. The postscaler is selected at the time of the device programming, by the value written to the CONFIG2H configuration register.

FIGURE 23-1: WATCHDOG TIMER BLOCK DIAGRAM

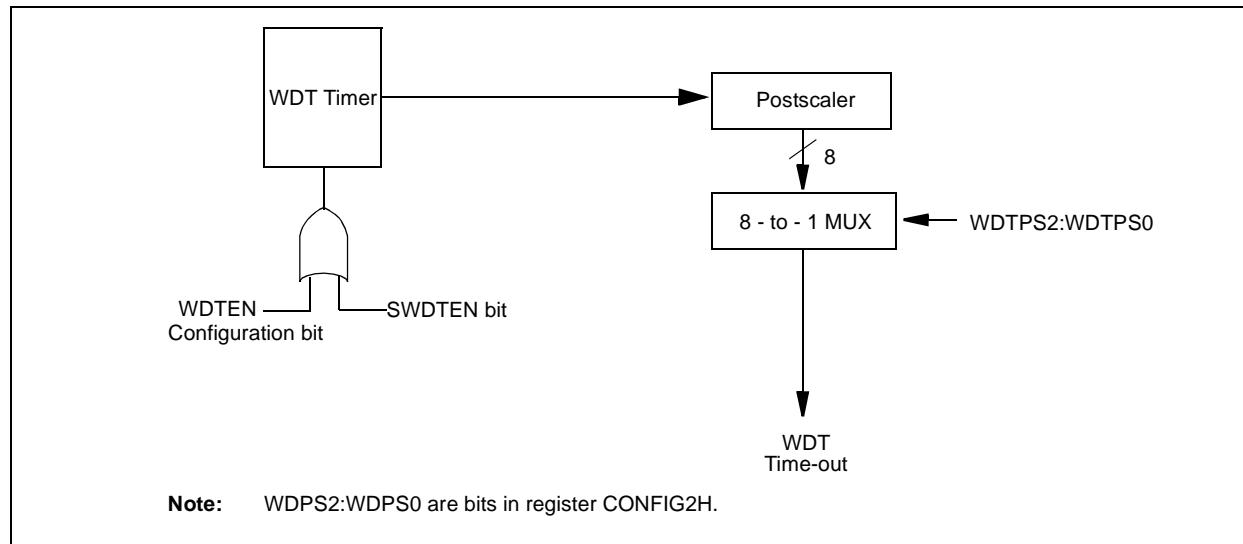


TABLE 23-2: SUMMARY OF WATCHDOG TIMER REGISTERS

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CONFIG2H	—	—	—	—	WDTPS2	WDTPS2	WDTPS0	WDTEN
RCON	IPEN	—	—	RI	TO	PD	POR	BOR
WDTCON	—	—	—	—	—	—	—	SWDTEN

Legend: Shaded cells are not used by the Watchdog Timer.

23.3 Power-down Mode (SLEEP)

Power-down mode is entered by executing a `SLEEP` instruction.

If enabled, the Watchdog Timer will be cleared, but keeps running, the `PD` bit (`RCON<3>`) is cleared, the `TO` (`RCON<4>`) bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had before the `SLEEP` instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, place all I/O pins at either `VDD` or `Vss`, ensure no external circuitry is drawing current from the I/O pin, power-down the A/D and disable external clocks. Pull all I/O pins that are hi-impedance inputs, high or low externally, to avoid switching currents caused by floating inputs. The `T0CKI` input should also be at `VDD` or `Vss` for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The `MCLR` pin must be at a logic high level (`VIHMC`).

23.3.1 WAKE-UP FROM SLEEP

The device can wake-up from `SLEEP` through one of the following events:

1. External RESET input on `MCLR` pin.
2. Watchdog Timer Wake-up (if WDT was enabled).
3. Interrupt from INT pin, RB port change or a Peripheral Interrupt.

The following peripheral interrupts can wake the device from `SLEEP`:

1. PSP read or write.
2. TMR1 interrupt. Timer1 must be operating as an asynchronous counter.
3. TMR3 interrupt. Timer3 must be operating as an asynchronous counter.
4. CCP Capture mode interrupt.
5. Special event trigger (Timer1 in Asynchronous mode using an external clock).
6. MSSP (START/STOP) bit detect interrupt.
7. MSSP transmit or receive in Slave mode (SPI/I²C).
8. USART RX or TX (Synchronous Slave mode).
9. A/D conversion (when A/D clock source is RC).
10. EEPROM write operation complete.
11. LVD interrupt.

Other peripherals cannot generate interrupts, since during `SLEEP`, no on-chip clocks are present.

External `MCLR` Reset will cause a device `RESET`. All other events are considered a continuation of program execution and will cause a “wake-up”. The `TO` and `PD` bits in the `RCON` register can be used to determine the cause of the device `RESET`. The `PD` bit, which is set on power-up, is cleared when `SLEEP` is invoked. The `TO` bit is cleared if a WDT time-out occurred (and caused wake-up).

When the `SLEEP` instruction is being executed, the next instruction (`PC + 2`) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the `GIE` bit. If the `GIE` bit is clear (disabled), the device continues execution at the instruction after the `SLEEP` instruction. If the `GIE` bit is set (enabled), the device executes the instruction after the `SLEEP` instruction and then branches to the interrupt address. In cases where the execution of the instruction following `SLEEP` is not desirable, the user should have a `NOP` after the `SLEEP` instruction.

23.3.2 WAKE-UP USING INTERRUPTS

When global interrupts are disabled (`GIE` cleared) and any interrupt source has both its interrupt enable bit and interrupt flag bit set, one of the following will occur:

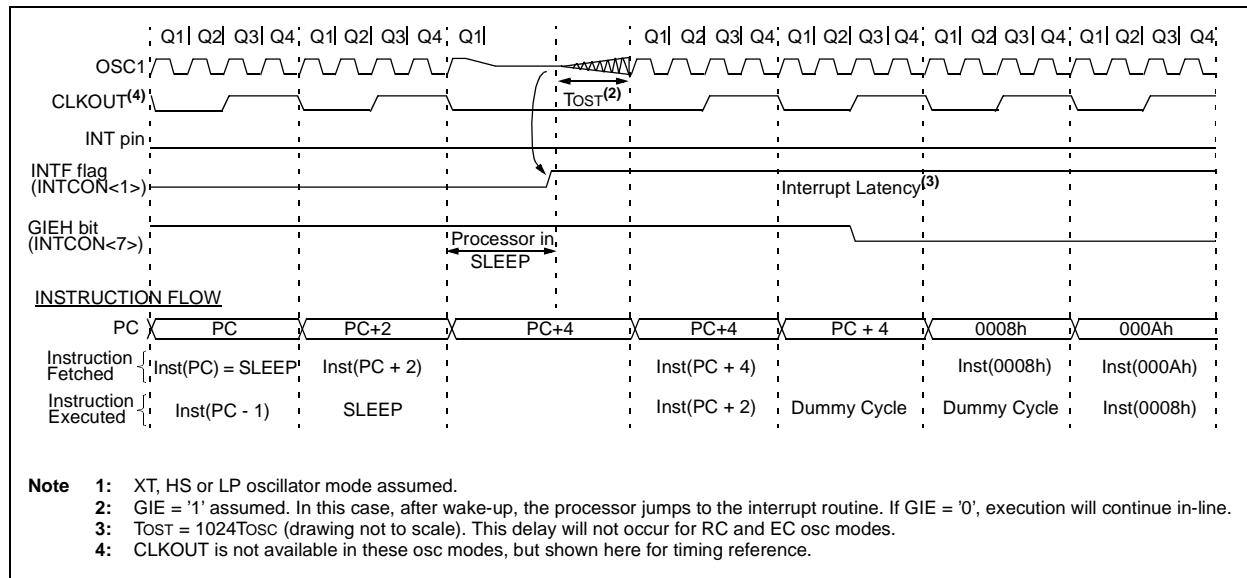
- If an interrupt condition (interrupt flag bit and interrupt enable bits are set) occurs **before** the execution of a `SLEEP` instruction, the `SLEEP` instruction will complete as a `NOP`. Therefore, the `WDT` and `WDT postscaler` will not be cleared, the `TO` bit will not be set and `PD` bits will not be cleared.
- If the interrupt condition occurs **during or after** the execution of a `SLEEP` instruction, the device will immediately wake-up from `SLEEP`. The `SLEEP` instruction will be completely executed before the wake-up. Therefore, the `WDT` and `WDT postscaler` will be cleared, the `TO` bit will be set and the `PD` bit will be cleared.

Even if the flag bits were checked before executing a `SLEEP` instruction, it may be possible for flag bits to become set before the `SLEEP` instruction completes. To determine whether a `SLEEP` instruction executed, test the `PD` bit. If the `PD` bit is set, the `SLEEP` instruction was executed as a `NOP`.

To ensure that the `WDT` is cleared, a `CLRWDT` instruction should be executed before a `SLEEP` instruction.

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FIGURE 23-2: WAKE-UP FROM SLEEP THROUGH INTERRUPT^(1,2)



23.4 Program Verification and Code Protection

The overall structure of the code protection on the PIC18 FLASH devices differs significantly from other PICmicro devices.

The user program memory is divided on binary boundaries into eight blocks of 16 Kbyte each. The first block is further divided into a boot block of 512 bytes and a second block (Block 0) of 15.5 Kbyte, for a total of nine blocks.

Each of the blocks has three code protection bits associated with them. They are:

- Code Protect bit (CPn)
- Write Protect bit (WRTn)
- External Block Table Read bit (EBTRn)

Figure 23-3 shows the program memory organization for 64 and 128 Kbyte devices, and the specific code protection bit associated with each block. The actual locations of the bits are summarized in Table 23-3.

FIGURE 23-3: CODE PROTECTED PROGRAM MEMORY FOR PIC18FXX20 DEVICES

MEMORY SIZE / DEVICE		Address Range	Block Code Protection Controlled By:
64 Kbytes (PIC18FX620)	128 Kbytes (PIC18FX720)		
Boot Block	Boot Block	000000h 0001FFh	CPB, WRTB, EBTRB
Block 0	Block 0	000200h 003FFFh	CP0, WRT0, EBTR0
Block 1	Block 1	004000h 007FFFh	CP1, WRT1, EBTR1
Block 2	Block 2	008000h 00BFFFh	CP2, WRT2, EBTR2
Block 3	Block 3	00C000h 00FFFFh	CP3, WRT3, EBTR3
Unimplemented Read 0s	Block 4	010000h 013FFFh	CP4, WRT4, EBTR4
	Block 5	014000h 017FFFh	CP5, WRT5, EBTR5
	Block 6	018000h 01BFFFh	CP6, WRT6, EBTR6
	Block 7	01C000h 01FFFFh	CP7, WRT7, EBTR7

TABLE 23-3: SUMMARY OF CODE PROTECTION REGISTERS

File Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
300008h	CONFIG5L	CP7*	CP6*	CP5*	CP4*	CP3	CP2	CP1	CP0
300009h	CONFIG5H	CPD	CPB	—	—	—	—	—	
3000Ah	CONFIG6L	WRT7*	WRT6*	WRT5*	WRT4*	WRT3	WRT2	WRT1	WRT0
3000Bh	CONFIG6H	WRTD	WRTB	WRTE	—	—	—	—	
3000Ch	CONFIG7L	EBTR7*	EBTR6*	EBTR5*	EBTR4*	EBTR3	EBTR2	EBTR1	EBTR0
3000Dh	CONFIG7H	—	EBTRB	—	—	—	—	—	

Legend: Shaded cells are unimplemented.

* Unimplemented in PIC18FX620 devices.

23.4.1 PROGRAM MEMORY CODE PROTECTION

The user memory may be read to or written from any location using the Table Read and Table Write instructions. The device ID may be read with Table Reads. The configuration registers may be read and written with the Table Read and Table Write instructions.

In user mode, the CPn bits have no direct effect. CPn bits inhibit external reads and writes. A block of user memory may be protected from Table Writes if the WRTn configuration bit is '0'. The EBTRn bits control Table Reads. For a block of user memory with the EBTRn bit set to '0', a Table Read instruction that executes from within that block is allowed to read. A Table Read instruction that executes from a location outside

of that block is not allowed to read, and will result in reading '0's. Figures 23-4 through 23-6 illustrate Table Write and Table Read protection.

Note: Code protection bits may only be written to a '0' from a '1' state. It is not possible to write a '1' to a bit in the '0' state. Code protection bits are only set to '1' by a full chip erase or block erase function. The full chip erase and block erase functions can only be initiated via ICSP or an external programmer.

FIGURE 23-4: TABLE WRITE (WRTn) DISALLOWED

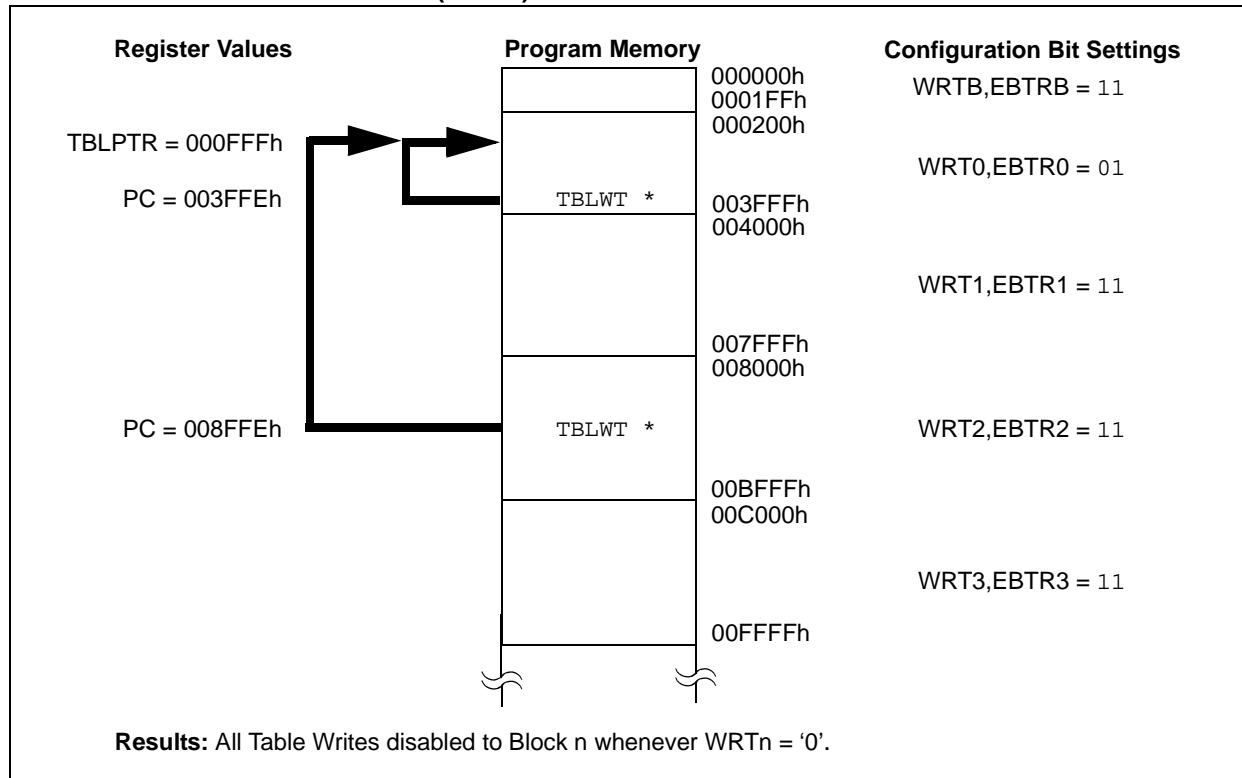


FIGURE 23-5: EXTERNAL BLOCK TABLE READ (EBTRn) DISALLOWED

Register Values	Program Memory	Configuration Bit Settings
TBLPTR = 000FFFh	000000h 0001FFh 000200h	WRTB,EBTRB = 11
PC = 004FFEh	003FFFh 004000h TBLRD *	WRT0,EBTR0 = 10
	007FFFh 008000h	WRT1,EBTR1 = 11
	00BFFFh 00C000h	WRT2,EBTR2 = 11
	00FFFFh	WRT3,EBTR3 = 11

Results: All Table Reads from external blocks to Block n are disabled whenever EBTRn = '0'. TABLAT register returns a value of "0".

FIGURE 23-6: EXTERNAL BLOCK TABLE READ (EBTRn) ALLOWED

Register Values	Program Memory	Configuration Bit Settings
TBLPTR = 000FFFh	000000h 0001FFh 000200h	WRTB,EBTRB = 11
PC = 003FFEh	003FFFh 004000h TBLRD *	WRT0,EBTR0 = 10
	007FFFh 008000h	WRT1,EBTR1 = 11
	00BFFFh 00C000h	WRT2,EBTR2 = 11
	00FFFFh	WRT3,EBTR3 = 11

Results: Table Reads permitted within Block n, even when EBTRBn = '0'. TABLAT register returns the value of the data at the location TBLPTR.

23.4.2 DATA EEPROM CODE PROTECTION

The entire Data EEPROM is protected from external reads and writes by two bits: CPD and WRTD. CPD inhibits external reads and writes of Data EEPROM. WRTD inhibits external writes to Data EEPROM. The CPU can continue to read and write Data EEPROM, regardless of the protection bit settings.

23.4.3 CONFIGURATION REGISTER PROTECTION

The configuration registers can be write protected. The WRTC bit controls protection of the configuration registers. In user mode, the WRTC bit is readable only. WRTC can only be written via ICSP or an external programmer.

23.5 ID Locations

Eight memory locations (200000h - 200007h) are designated as ID locations, where the user can store checksum or other code identification numbers. These locations are accessible during normal execution through the TBLRD and TBLWT instructions, or during program/verify. The ID locations can be read when the device is code protected.

23.6 In-Circuit Serial Programming

PIC18FXX20 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for power, ground and the programming voltage. This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

23.7 In-Circuit Debugger

When the DEBUG bit in configuration register CONFIG4L is programmed to a '0', the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB® IDE. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 23-4 shows which features are consumed by the background debugger.

TABLE 23-4: DEBUGGER RESOURCES

I/O pins	RB6, RB7
Stack	2 levels
Program Memory	512 bytes
Data Memory	10 bytes

To use the In-Circuit Debugger function of the microcontroller, the design must implement In-Circuit Serial Programming connections to MCLR/VPP, VDD, GND, RB7 and RB6. This will interface to the In-Circuit Debugger module available from Microchip or one of the third party development tool companies.

23.8 Low Voltage ICSP Programming

The LVP bit configuration register, CONFIG4L, enables low voltage ICSP programming. This mode allows the microcontroller to be programmed via ICSP using a VDD source in the operating voltage range. This only means that VPP does not have to be brought to VIHH, but can instead be left at the normal operating voltage. In this mode, the RB5/PGM pin is dedicated to the programming function and ceases to be a general purpose I/O pin. During programming, VDD is applied to the MCLR/VPP pin. To enter Programming mode, VDD must be applied to the RB5/PGM, provided the LVP bit is set. The LVP bit defaults to a ('1') from the factory.

Note 1: The High Voltage Programming mode is always available, regardless of the state of the LVP bit, by applying VIHH to the MCLR pin.

- 2:** While in Low Voltage ICSP mode, the RB5 pin can no longer be used as a general purpose I/O pin, and should be held low during normal operation.
- 3:** When using low voltage ICSP programming (LVP) and the pull-ups on PORTB are enabled, bit 5 in the TRISB register must be cleared to disable the pull-up on RB5 and ensure the proper operation of the device.

If Low Voltage Programming mode is not used, the LVP bit can be programmed to a '0' and RB5/PGM becomes a digital I/O pin. However, the LVP bit may only be programmed when programming is entered with VIHH on MCLR/VPP.

It should be noted that once the LVP bit is programmed to 0, only the High Voltage Programming mode is available and only High Voltage Programming mode can be used to program the device.

When using low voltage ICSP, the part must be supplied 4.5V to 5.5V, if a bulk erase will be executed. This includes reprogramming of the code protect bits from an on-state to off-state. For all other cases of low voltage ICSP, the part may be programmed at the normal operating voltage. This means unique user IDs, or user code can be reprogrammed or added.

24.0 INSTRUCTION SET SUMMARY

The PIC18 instruction set adds many enhancements to the previous PICmicro instruction sets, while maintaining an easy migration from these PICmicro instruction sets.

Most instructions are a single program memory word (16 bits), but there are three instructions that require two program memory locations.

Each single word instruction is a 16-bit word divided into an OPCODE, which specifies the instruction type and one or more operands, which further specify the operation of the instruction.

The instruction set is highly orthogonal and is grouped into four basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal** operations
- **Control** operations

The PIC18 instruction set summary in Table 24-2 lists **byte-oriented**, **bit-oriented**, **literal** and **control** operations. Table 24-1 shows the opcode field descriptions.

Most **byte-oriented** instructions have three operands:

1. The file register (specified by 'f')
2. The destination of the result (specified by 'd')
3. The accessed memory (specified by 'a')

The file register designator 'f' specifies which file register is to be used by the instruction.

The destination designator 'd' specifies where the result of the operation is to be placed. If 'd' is zero, the result is placed in the WREG register. If 'd' is one, the result is placed in the file register specified in the instruction.

All **bit-oriented** instructions have three operands:

1. The file register (specified by 'f')
2. The bit in the file register (specified by 'b')
3. The accessed memory (specified by 'a')

The bit field designator 'b' selects the number of the bit affected by the operation, while the file register designator 'f' represents the number of the file in which the bit is located.

The **literal** instructions may use some of the following operands:

- A literal value to be loaded into a file register (specified by 'k')
- The desired FSR register to load the literal value into (specified by 'f')
- No operand required (specified by '—')

The **control** instructions may use some of the following operands:

- A program memory address (specified by 'n')
- The mode of the Call or Return instructions (specified by 's')
- The mode of the Table Read and Table Write instructions (specified by 'm')
- No operand required (specified by '—')

All instructions are a single word, except for three double-word instructions. These three instructions were made double-word instructions so that all the required information is available in these 32 bits. In the second word, the 4 MSbs are 1's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

All single word instructions are executed in a single instruction cycle, unless a conditional test is true or the program counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles with the additional instruction cycle(s) executed as a NOP.

The double-word instructions execute in two instruction cycles.

One instruction cycle consists of four oscillator periods. Thus, for an oscillator frequency of 4 MHz, the normal instruction execution time is 1 μ s. If a conditional test is true, or the program counter is changed as a result of an instruction, the instruction execution time is 2 μ s. Two-word branch instructions (if true) would take 3 μ s.

Figure 24-1 shows the general formats that the instructions can have.

All examples use the format 'nnh' to represent a hexadecimal number, where 'h' signifies a hexadecimal digit.

The Instruction Set Summary, shown in Table 24-2, lists the instructions recognized by the Microchip Assembler (MPASMTM).

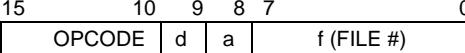
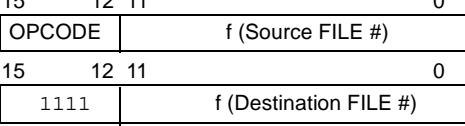
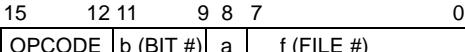
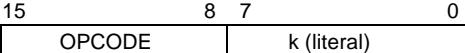
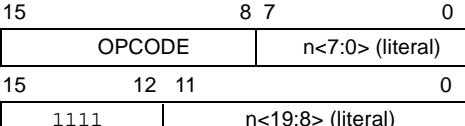
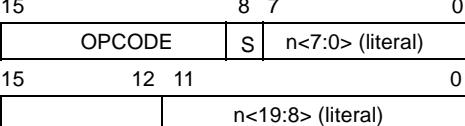
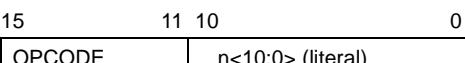
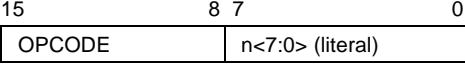
Section 24.1 provides a description of each instruction.

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TABLE 24-1: OPCODE FIELD DESCRIPTIONS

Field	Description
a	RAM access bit a = 0: RAM location in Access RAM (BSR register is ignored) a = 1: RAM bank is specified by BSR register
bbb	Bit address within an 8-bit file register (0 to 7)
BSR	Bank Select Register. Used to select the current RAM bank.
d	Destination select bit d = 0: store result in WREG d = 1: store result in file register f.
dest	Destination either the WREG register or the specified register file location
f	8-bit Register file address (0x00 to 0xFF)
fs	12-bit Register file address (0x000 to 0xFFFF). This is the source address.
fd	12-bit Register file address (0x000 to 0xFFFF). This is the destination address.
k	Literal field, constant data or label (may be either an 8-bit, 12-bit or a 20-bit value)
label	Label name
mm	The mode of the TBLPTR register for the Table Read and Table Write instructions. Only used with Table Read and Table Write instructions: * No Change to register (such as TBLPTR with Table reads and writes) *+ Post-Increment register (such as TBLPTR with Table reads and writes) *- Post-Decrement register (such as TBLPTR with Table reads and writes) +* Pre-Increment register (such as TBLPTR with Table reads and writes)
n	The relative address (2's complement number) for relative branch instructions, or the direct address for Call/Branch and Return instructions
PRODH	Product of Multiply high byte
PRODL	Product of Multiply low byte
s	Fast Call/Return mode select bit s = 0: do not update into/from shadow registers s = 1: certain registers loaded into/from shadow registers (Fast mode)
u	Unused or Unchanged
WREG	Working register (accumulator)
x	Don't care (0 or 1) The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
TBLPTR	21-bit Table Pointer (points to a Program Memory location)
TABLAT	8-bit Table Latch
TOS	Top-of-Stack
PC	Program Counter
PCL	Program Counter Low Byte
PCH	Program Counter High Byte
PCLATH	Program Counter High Byte Latch
PCLATU	Program Counter Upper Byte Latch
GIE	Global Interrupt Enable bit
WDT	Watchdog Timer
TO	Time-out bit
PD	Power-down bit
C, DC, Z, OV, N	ALU status bits Carry, Digit Carry, Zero, Overflow, Negative
[]	Optional
()	Contents
→	Assigned to
< >	Register bit field
ε	In the set of
italics	User defined term (font is courier)

FIGURE 24-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations	Example Instruction
 d = 0 for result destination to be WREG register d = 1 for result destination to be file register (f) a = 0 to force Access Bank a = 1 for BSR to select bank f = 8-bit file register address	ADDWF MYREG, W, B
Byte to Byte move operations (2-word)	
 f = 12-bit file register address	MOVFF MYREG1, MYREG2
Bit-oriented file register operations	
 b = 3-bit position of bit in file register (f) a = 0 to force Access Bank a = 1 for BSR to select bank f = 8-bit file register address	BSF MYREG, bit, B
Literal operations	
 k = 8-bit immediate value	MOVLW 0x7F
Control operations	
CALL, GOTO and Branch operations	
 n = 20-bit immediate value	GOTO Label
 S = Fast bit	CALL MYFUNC
	BRA MYFUNC
	BC MYFUNC

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TABLE 24-2: PIC18FXXX INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	16-Bit Instruction Word				Status Affected	Notes
			MSb	Lsb				
BYTE-ORIENTED FILE REGISTER OPERATIONS								
ADDWF f, d, a	Add WREG and f	1	0010 01da	ffff ffff			C, DC, Z, OV, N	1, 2
ADDWFC f, d, a	Add WREG and Carry bit to f	1	0010 00da	ffff ffff			C, DC, Z, OV, N	1, 2
ANDWF f, d, a	AND WREG with f	1	0001 01da	ffff ffff			Z, N	1, 2
CLRF f, a	Clear f	1	0110 101a	ffff ffff			Z	2
COMF f, d, a	Complement f	1	0001 11da	ffff ffff			Z, N	1, 2
CPFSEQ f, a	Compare f with WREG, skip =	1 (2 or 3)	0110 001a	ffff ffff			None	4
CPFSGT f, a	Compare f with WREG, skip >	1 (2 or 3)	0110 010a	ffff ffff			None	4
CPFSLT f, a	Compare f with WREG, skip <	1 (2 or 3)	0110 000a	ffff ffff			None	1, 2
DECF f, d, a	Decrement f	1	0000 01da	ffff ffff			C, DC, Z, OV, N	1, 2, 3, 4
DECFSZ f, d, a	Decrement f, Skip if 0	1 (2 or 3)	0010 11da	ffff ffff			None	1, 2, 3, 4
DCFSNZ f, d, a	Decrement f, Skip if Not 0	1 (2 or 3)	0100 11da	ffff ffff			None	1, 2
INCF f, d, a	Increment f	1	0010 10da	ffff ffff			C, DC, Z, OV, N	1, 2, 3, 4
INCFSZ f, d, a	Increment f, Skip if 0	1 (2 or 3)	0011 11da	ffff ffff			None	4
INFSNZ f, d, a	Increment f, Skip if Not 0	1 (2 or 3)	0100 10da	ffff ffff			None	1, 2
IORWF f, d, a	Inclusive OR WREG with f	1	0001 00da	ffff ffff			Z, N	1, 2
MOVF f, d, a	Move f	1	0101 00da	ffff ffff			Z, N	1
MOVFF f _s , f _d	Move f _s (source) to 1st word f _d (destination)2nd word	2	1100 ffff ffff ffff				None	
MOVWF f, a	Move WREG to f	1	0110 111a	ffff ffff			None	
MULWF f, a	Multiply WREG with f	1	0000 001a	ffff ffff			None	
NEGF f, a	Negate f	1	0110 110a	ffff ffff			C, DC, Z, OV, N	1, 2
RLCF f, d, a	Rotate Left f through Carry	1	0011 01da	ffff ffff			C, Z, N	
RLNCF f, d, a	Rotate Left f (No Carry)	1	0100 01da	ffff ffff			Z, N	1, 2
RRCF f, d, a	Rotate Right f through Carry	1	0011 00da	ffff ffff			C, Z, N	
RRNCF f, d, a	Rotate Right f (No Carry)	1	0100 00da	ffff ffff			Z, N	
SETF f, a	Set f	1	0110 100a	ffff ffff			None	
SUBFWB f, d, a	Subtract f from WREG with borrow	1	0101 01da	ffff ffff			C, DC, Z, OV, N	1, 2
SUBWF f, d, a	Subtract WREG from f	1	0101 11da	ffff ffff			C, DC, Z, OV, N	
SUBWFB f, d, a	Subtract WREG from f with borrow	1	0101 10da	ffff ffff			C, DC, Z, OV, N	1, 2
SWAPF f, d, a	Swap nibbles in f	1	0011 10da	ffff ffff			None	4
TSTFSZ f, a	Test f, skip if 0	1 (2 or 3)	0110 011a	ffff ffff			None	1, 2
XORWF f, d, a	Exclusive OR WREG with f	1	0001 10da	ffff ffff			Z, N	
BIT-ORIENTED FILE REGISTER OPERATIONS								
BCF f, b, a	Bit Clear f	1	1001 bbba	ffff ffff			None	1, 2
BSF f, b, a	Bit Set f	1	1000 bbba	ffff ffff			None	1, 2
BTFSC f, b, a	Bit Test f, Skip if Clear	1 (2 or 3)	1011 bbba	ffff ffff			None	3, 4
BTFSS f, b, a	Bit Test f, Skip if Set	1 (2 or 3)	1010 bbba	ffff ffff			None	3, 4
BTG f, d, a	Bit Toggle f	1	0111 bbba	ffff ffff			None	1, 2

Note 1: When a PORT register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

- 2:** If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned.
- 3:** If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.
- 4:** Some instructions are 2-word instructions. The second word of these instructions will be executed as a NOP, unless the first word of the instruction retrieves the information embedded in these 16-bits. This ensures that all program memory locations have a valid instruction.
- 5:** If the Table Write starts the write cycle to internal memory, the write will continue until terminated.

TABLE 24-2: PIC18FXXX INSTRUCTION SET (CONTINUED)

Mnemonic, Operands	Description	Cycles	16-Bit Instruction Word				Status Affected	Notes
			MSb			LSb		
CONTROL OPERATIONS								
BC n	Branch if Carry	1 (2)	1110	0010	nnnn	nnnn	None	
BN n	Branch if Negative	1 (2)	1110	0110	nnnn	nnnn	None	
BNC n	Branch if Not Carry	1 (2)	1110	0011	nnnn	nnnn	None	
BNN n	Branch if Not Negative	1 (2)	1110	0111	nnnn	nnnn	None	
BNOV n	Branch if Not Overflow	1 (2)	1110	0101	nnnn	nnnn	None	
BNZ n	Branch if Not Zero	2	1110	0001	nnnn	nnnn	None	
BOV n	Branch if Overflow	1 (2)	1110	0100	nnnn	nnnn	None	
BRA n	Branch Unconditionally	1 (2)	1101	0nnn	nnnn	nnnn	None	
BZ n	Branch if Zero	1 (2)	1110	0000	nnnn	nnnn	None	
CALL n, s	Call subroutine1st word 2nd word	2	1110	110s	kkkk	kkkk	None	
CLRWDT —	Clear Watchdog Timer	1	0000	0000	0000	0100	TO, PD	
DAW —	Decimal Adjust WREG	1	0000	0000	0000	0111	C	
GOTO n	Go to address1st word 2nd word	2	1110	1111	kkkk	kkkk	None	
NOP —	No Operation	1	0000	0000	0000	0000	None	
NOP —	No Operation (Note 4)	1	1111	xxxx	xxxx	xxxx	None	
POP —	Pop top of return stack (TOS)	1	0000	0000	0000	0110	None	
PUSH —	Push top of return stack (TOS)	1	0000	0000	0000	0101	None	
RCALL n	Relative Call	2	1101	1nnn	nnnn	nnnn	None	
RESET	Software device RESET	1	0000	0000	1111	1111	All	
RETFIE s	Return from interrupt enable	2	0000	0000	0001	000s	GIE/GIEH, PEIE/GIEL	
RETLW k	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None	
RETURN s	Return from Subroutine	2	0000	0000	0001	001s	None	
SLEEP —	Go into standby mode	1	0000	0000	0000	0011	TO, PD	

Note 1: When a PORT register is modified as a function of itself (e.g., `MOVF PORTB, 1, 0`), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.

- 2:** If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned.
- 3:** If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.
- 4:** Some instructions are 2-word instructions. The second word of these instructions will be executed as a NOP, unless the first word of the instruction retrieves the information embedded in these 16-bits. This ensures that all program memory locations have a valid instruction.
- 5:** If the Table Write starts the write cycle to internal memory, the write will continue until terminated.

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TABLE 24-2: PIC18FXXX INSTRUCTION SET (CONTINUED)

Mnemonic, Operands	Description	Cycles	16-Bit Instruction Word				Status Affected	Notes	
			MSb	LSb					
LITERAL OPERATIONS									
ADDLW k	Add literal and WREG	1	0000	1111	kkkk	kkkk	C, DC, Z, OV, N		
ANDLW k	AND literal with WREG	1	0000	1011	kkkk	kkkk	Z, N		
IORLW k	Inclusive OR literal with WREG	1	0000	1001	kkkk	kkkk	Z, N		
LFSR f, k	Move literal (12-bit) 2nd word to FSRx 1st word	2	1110	1110	00ff	kkkk	None		
			1111	0000	kkkk	kkkk			
MOVLB k	Move literal to BSR<3:0>	1	0000	0001	0000	kkkk	None		
MOVLW k	Move literal to WREG	1	0000	1110	kkkk	kkkk	None		
MULLW k	Multiply literal with WREG	1	0000	1101	kkkk	kkkk	None		
RETLW k	Return with literal in WREG	2	0000	1100	kkkk	kkkk	None		
SUBLW k	Subtract WREG from literal	1	0000	1000	kkkk	kkkk	C, DC, Z, OV, N		
XORLW k	Exclusive OR literal with WREG	1	0000	1010	kkkk	kkkk	Z, N		
DATA MEMORY ↔ PROGRAM MEMORY OPERATIONS									
TBLRD*	Table Read	2	0000	0000	0000	1000	None		
TBLRD*+	Table Read with post-increment		0000	0000	0000	1001	None		
TBLRD*-	Table Read with post-decrement		0000	0000	0000	1010	None		
TBLRD+*	Table Read with pre-increment		0000	0000	0000	1011	None		
TBLWT*	Table Write	2 (5)	0000	0000	0000	1100	None		
TBLWT*+	Table Write with post-increment		0000	0000	0000	1101	None		
TBLWT*-	Table Write with post-decrement		0000	0000	0000	1110	None		
TBLWT+*	Table Write with pre-increment		0000	0000	0000	1111	None		

- Note 1:** When a PORT register is modified as a function of itself (e.g., MOVF PORTB, 1, 0), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 2:** If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned.
- 3:** If Program Counter (PC) is modified or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.
- 4:** Some instructions are 2-word instructions. The second word of these instructions will be executed as a NOP, unless the first word of the instruction retrieves the information embedded in these 16-bits. This ensures that all program memory locations have a valid instruction.
- 5:** If the Table Write starts the write cycle to internal memory, the write will continue until terminated.

24.1 Instruction Set

ADDLW	ADD literal to W											
Syntax:	[<i>label</i>] ADDLW <i>k</i>											
Operands:	0 ≤ <i>k</i> ≤ 255											
Operation:	(W) + <i>k</i> → W											
Status Affected:	N, OV, C, DC, Z											
Encoding:	0000	1111	kkkk	kkkk								
Description:	The contents of W are added to the 8-bit literal 'k' and the result is placed in W.											
Words:	1											
Cycles:	1											
Q Cycle Activity:	<table border="1" style="width: 100%; text-align: center;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read literal 'k'</td><td>Process Data</td><td>Write to W</td></tr> </table>				Q1	Q2	Q3	Q4	Decode	Read literal 'k'	Process Data	Write to W
Q1	Q2	Q3	Q4									
Decode	Read literal 'k'	Process Data	Write to W									

Example: ADDLW 0x15

Before Instruction

W = 0x10

After Instruction

W = 0x25

ADDWF	ADD W to f											
Syntax:	[<i>label</i>] ADDWF <i>f</i> [,d[,a]]											
Operands:	0 ≤ <i>f</i> ≤ 255 d ∈ [0,1] a ∈ [0,1]											
Operation:	(W) + (f) → dest											
Status Affected:	N, OV, C, DC, Z											
Encoding:	0010	01da	ffff	ffff								
Description:	Add W to register 'f'. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected. If 'a' is 1, the BSR is used.											
Words:	1											
Cycles:	1											
Q Cycle Activity:	<table border="1" style="width: 100%; text-align: center;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>Write to destination</td></tr> </table>				Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write to destination
Q1	Q2	Q3	Q4									
Decode	Read register 'f'	Process Data	Write to destination									

Example: ADDWF REG, 0, 0

Before Instruction

W = 0x17
REG = 0xC2

After Instruction

W = 0xD9
REG = 0xC2

ADDWFC	ADD W and Carry bit to f								
Syntax:	[<i>label</i>] ADDWFC f [,d [,a]								
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]								
Operation:	(W) + (f) + (C) → dest								
Status Affected:	N,OV, C, DC, Z								
Encoding:	0010 00da ffff ffff								
Description:	Add W, the Carry Flag and data memory location 'f'. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is placed in data memory location 'f'. If 'a' is 0, the Access Bank will be selected. If 'a' is 1, the BSR will not be overridden.								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1"> <thead> <tr> <th>Q1</th> <th>Q2</th> <th>Q3</th> <th>Q4</th> </tr> </thead> <tbody> <tr> <td>Decode</td> <td>Read register 'f'</td> <td>Process Data</td> <td>Write to destination</td> </tr> </tbody> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write to destination
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write to destination						

Example: ADDWFC REG, 0, 1

Before Instruction

Carry bit = 1
REG = 0x02
W = 0x4D

After Instruction

Carry bit = 0
REG = 0x02
W = 0x50

ANDLW	AND literal with W								
Syntax:	[<i>label</i>] ANDLW k								
Operands:	0 ≤ k ≤ 255								
Operation:	(W) .AND. k → W								
Status Affected:	N,Z								
Encoding:	0000 1011 kkkk kkkk								
Description:	The contents of W are ANDed with the 8-bit literal 'k'. The result is placed in W.								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1"> <thead> <tr> <th>Q1</th> <th>Q2</th> <th>Q3</th> <th>Q4</th> </tr> </thead> <tbody> <tr> <td>Decode</td> <td>Read literal 'k'</td> <td>Process Data</td> <td>Write to W</td> </tr> </tbody> </table>	Q1	Q2	Q3	Q4	Decode	Read literal 'k'	Process Data	Write to W
Q1	Q2	Q3	Q4						
Decode	Read literal 'k'	Process Data	Write to W						

Example: ANDLW 0x5F

Before Instruction

W = 0xA3

After Instruction

W = 0x03

ANDWF	AND W with f								
Syntax:	[<i>label</i>] ANDWF f [,d [,a]								
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]								
Operation:	(W) .AND. (f) → dest								
Status Affected:	N,Z								
Encoding:	0001 01da ffff ffff								
Description:	The contents of W are AND'ed with register 'f'. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected. If 'a' is 1, the BSR will not be overridden (default).								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>Write to destination</td></tr> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write to destination
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write to destination						

Example: ANDWF REG, 0, 0

Before Instruction

W = 0x17
REG = 0xC2

After Instruction

W = 0x02
REG = 0xC2

BC	Branch if Carry												
Syntax:	[<i>label</i>] BC n												
Operands:	-128 ≤ n ≤ 127												
Operation:	if carry bit is '1' (PC) + 2 + 2n → PC												
Status Affected:	None												
Encoding:	1110 0010 nnnn nnnn												
Description:	If the Carry bit is '1', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then a two-cycle instruction.												
Words:	1												
Cycles:	1(2)												
Q Cycle Activity:	<table border="1"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read literal 'n'</td><td>Process Data</td><td>Write to PC</td></tr> <tr> <td>No operation</td><td>No operation</td><td>No operation</td><td>No operation</td></tr> </table>	Q1	Q2	Q3	Q4	Decode	Read literal 'n'	Process Data	Write to PC	No operation	No operation	No operation	No operation
Q1	Q2	Q3	Q4										
Decode	Read literal 'n'	Process Data	Write to PC										
No operation	No operation	No operation	No operation										

If Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE BC 5

Before Instruction

PC = address (HERE)

After Instruction

If Carry = 1;
PC = address (HERE+12)
If Carry = 0;
PC = address (HERE+2)

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BCF		Bit Clear f	
Syntax:	[<i>label</i>] BCF f,b[,a]		
Operands:	0 ≤ f ≤ 255 0 ≤ b ≤ 7 a ∈ [0,1]		
Operation:	0 → f		
Status Affected:	None		
Encoding:	1001 bbba ffff ffff		
Description:	Bit 'b' in register 'f' is cleared. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).		
Words:	1		
Cycles:	1		
Q Cycle Activity:			
	Q1 Q2 Q3 Q4		
	Decode Read register 'f' Process Data Write register 'f'		

Example: BCF FLAG_REG, 7, 0

Before Instruction
FLAG_REG = 0xC7
After Instruction
FLAG_REG = 0x47

BN		Branch if Negative	
Syntax:	[<i>label</i>] BN n		
Operands:	-128 ≤ n ≤ 127		
Operation:	if negative bit is '1' (PC) + 2 + 2n → PC		
Status Affected:	None		
Encoding:	1110 0110 nnnn nnnn		
Description:	If the Negative bit is '1', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then a two-cycle instruction.		
Words:	1		
Cycles:	1(2)		
Q Cycle Activity:			
If Jump:			
	Q1 Q2 Q3 Q4		
	Decode Read literal 'n' Process Data Write to PC		
	No operation No operation No operation No operation		
If No Jump:			
	Q1 Q2 Q3 Q4		
	Decode Read literal 'n' Process Data No operation		

Example: HERE BN Jump

Before Instruction
PC = address (HERE)
After Instruction
If Negative = 1;
PC = address (Jump)
If Negative = 0;
PC = address (HERE+2)

BNC	Branch if Not Carry			
Syntax:	[<i>label</i>] BNC <i>n</i>			
Operands:	$-128 \leq n \leq 127$			
Operation:	if carry bit is '0' $(PC) + 2 + 2n \rightarrow PC$			
Status Affected:	None			
Encoding:	1110	0011	nnnn	nnnn
Description:	<p>If the Carry bit is '0', then the program will branch.</p> <p>The 2's complement number '$2n$' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be $PC+2+2n$. This instruction is then a two-cycle instruction.</p>			
Words:	1			
Cycles:	1(2)			
Q Cycle Activity:				
If Jump:				
	Q1	Q2	Q3	Q4
	Decode	Read literal 'n'	Process Data	Write to PC
	No operation	No operation	No operation	No operation
If No Jump:				
	Q1	Q2	Q3	Q4
	Decode	Read literal 'n'	Process Data	No operation

Example: HERE BNC Jump

Before Instruction

PC = address (HERE)

After Instruction

If Carry	=	0;
PC	=	address (Jump)
If Carry	=	1;
PC	=	address (HERE+2)

BNN	Branch if Not Negative			
Syntax:	[<i>label</i>] BNN <i>n</i>			
Operands:	$-128 \leq n \leq 127$			
Operation:	if negative bit is '0' $(PC) + 2 + 2n \rightarrow PC$			
Status Affected:	None			
Encoding:	1110	0111	nnnn	nnnn
Description:	<p>If the Negative bit is '0', then the program will branch.</p> <p>The 2's complement number '$2n$' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be $PC+2+2n$. This instruction is then a two-cycle instruction.</p>			
Words:	1			
Cycles:	1(2)			
Q Cycle Activity:				
If Jump:				
	Q1	Q2	Q3	Q4
	Decode	Read literal 'n'	Process Data	Write to PC
	No operation	No operation	No operation	No operation
If No Jump:				
	Q1	Q2	Q3	Q4
	Decode	Read literal 'n'	Process Data	No operation

Example: HERE BNN Jump

Before Instruction

PC = address (HERE)

After Instruction

If Negative	=	0;
PC	=	address (Jump)
If Negative	=	1;
PC	=	address (HERE+2)

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BNOV	Branch if Not Overflow			
Syntax:	[<i>label</i>] BNOV n			
Operands:	-128 ≤ n ≤ 127			
Operation:	if overflow bit is '0' (PC) + 2 + 2n → PC			
Status Affected:	None			
Encoding:	1110	0101	nnnn	nnnn
Description:	If the Overflow bit is '0', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then a two-cycle instruction.			
Words:	1			
Cycles:	1(2)			
Q Cycle Activity:				
If Jump:				
	Q1	Q2	Q3	Q4
	Decode	Read literal 'n'	Process Data	Write to PC
	No operation	No operation	No operation	No operation
If No Jump:				
	Q1	Q2	Q3	Q4
	Decode	Read literal 'n'	Process Data	No operation

Example: HERE BNOV Jump

Before Instruction

PC = address (HERE)

After Instruction

If Overflow = 0;

PC = address (Jump)

If Overflow = 1;

PC = address (HERE+2)

BNZ	Branch if Not Zero			
Syntax:	[<i>label</i>] BNZ n			
Operands:	-128 ≤ n ≤ 127			
Operation:	if zero bit is '0' (PC) + 2 + 2n → PC			
Status Affected:	None			
Encoding:	1110	0001	nnnn	nnnn
Description:	If the Zero bit is '0', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then a two-cycle instruction.			
Words:	1			
Cycles:	1(2)			
Q Cycle Activity:				
If Jump:				
	Q1	Q2	Q3	Q4
	Decode	Read literal 'n'	Process Data	Write to PC
	No operation	No operation	No operation	No operation
If No Jump:				
	Q1	Q2	Q3	Q4
	Decode	Read literal 'n'	Process Data	No operation

Example: HERE BNZ Jump

Before Instruction

PC = address (HERE)

After Instruction

If Zero = 0;

PC = address (Jump)

If Zero = 1;

PC = address (HERE+2)

BRA	Unconditional Branch												
Syntax:	[<i>label</i>] BRA n												
Operands:	-1024 ≤ n ≤ 1023												
Operation:	(PC) + 2 + 2n → PC												
Status Affected:	None												
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>1101</td><td>0nnn</td><td>nnnn</td><td>nnnn</td></tr> </table>	1101	0nnn	nnnn	nnnn								
1101	0nnn	nnnn	nnnn										
Description:	Add the 2's complement number '2n' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is a two-cycle instruction.												
Words:	1												
Cycles:	2												
Q Cycle Activity:	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Q1</th><th style="text-align: center;">Q2</th><th style="text-align: center;">Q3</th><th style="text-align: center;">Q4</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">Decode</td><td style="text-align: center;">Read literal 'n'</td><td style="text-align: center;">Process Data</td><td style="text-align: center;">Write to PC</td></tr> <tr> <td style="text-align: center;">No operation</td><td style="text-align: center;">No operation</td><td style="text-align: center;">No operation</td><td style="text-align: center;">No operation</td></tr> </tbody> </table>	Q1	Q2	Q3	Q4	Decode	Read literal 'n'	Process Data	Write to PC	No operation	No operation	No operation	No operation
Q1	Q2	Q3	Q4										
Decode	Read literal 'n'	Process Data	Write to PC										
No operation	No operation	No operation	No operation										

Example: HERE BRA Jump

Before Instruction
 PC = address (HERE)

After Instruction
 PC = address (Jump)

BSF	Bit Set f								
Syntax:	[<i>label</i>] BSF f,b[,a]								
Operands:	0 ≤ f ≤ 255 0 ≤ b ≤ 7 a ∈ [0,1]								
Operation:	1 → f								
Status Affected:	None								
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>1000</td><td>bbba</td><td>ffff</td><td>ffff</td></tr> </table>	1000	bbba	ffff	ffff				
1000	bbba	ffff	ffff						
Description:	Bit 'b' in register 'f' is set. If 'a' is 0 Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value.								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Q1</th><th style="text-align: center;">Q2</th><th style="text-align: center;">Q3</th><th style="text-align: center;">Q4</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">Decode</td><td style="text-align: center;">Read register 'f'</td><td style="text-align: center;">Process Data</td><td style="text-align: center;">Write register 'f'</td></tr> </tbody> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write register 'f'
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write register 'f'						

Example: BSF FLAG_REG, 7, 1

Before Instruction
 FLAG_REG = 0x0A

After Instruction
 FLAG_REG = 0x8A

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BTFSC	Bit Test File, Skip if Clear												
Syntax:	[<i>label</i>] BTFSC f,b[,a]												
Operands:	0 ≤ f ≤ 255 0 ≤ b ≤ 7 a ∈ [0,1]												
Operation:	skip if (f) = 0												
Status Affected:	None												
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>1011</td><td>bbba</td><td>ffff</td><td>ffff</td></tr> </table>	1011	bbba	ffff	ffff								
1011	bbba	ffff	ffff										
Description:	<p>If bit 'b' in register 'f' is 0, then the next instruction is skipped.</p> <p>If bit 'b' is 0, then the next instruction fetched during the current instruction execution is discarded, and a NOP is executed instead, making this a two-cycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).</p>												
Words:	1												
Cycles:	1(2)												
Note:	3 cycles if skip and followed by a 2-word instruction.												
Q Cycle Activity:	<table border="1" style="width: 100%; text-align: center;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>No operation</td></tr> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	No operation				
Q1	Q2	Q3	Q4										
Decode	Read register 'f'	Process Data	No operation										
If skip:	<table border="1" style="width: 100%; text-align: center;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>No operation</td><td>No operation</td><td>No operation</td><td>No operation</td></tr> </table>	Q1	Q2	Q3	Q4	No operation	No operation	No operation	No operation				
Q1	Q2	Q3	Q4										
No operation	No operation	No operation	No operation										
If skip and followed by 2-word instruction:	<table border="1" style="width: 100%; text-align: center;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>No operation</td><td>No operation</td><td>No operation</td><td>No operation</td></tr> <tr> <td>No operation</td><td>No operation</td><td>No operation</td><td>No operation</td></tr> </table>	Q1	Q2	Q3	Q4	No operation	No operation	No operation	No operation	No operation	No operation	No operation	No operation
Q1	Q2	Q3	Q4										
No operation	No operation	No operation	No operation										
No operation	No operation	No operation	No operation										

Example: HERE BTFSC FLAG, 1, 0
 FALSE :
 TRUE :

Before Instruction
 PC = address (HERE)

After Instruction
 If FLAG<1> = 0;
 PC = address (TRUE)
 If FLAG<1> = 1;
 PC = address (FALSE)

BTFSS	Bit Test File, Skip if Set												
Syntax:	[<i>label</i>] BTFSS f,b[,a]												
Operands:	0 ≤ f ≤ 255 0 ≤ b < 7 a ∈ [0,1]												
Operation:	skip if (f) = 1												
Status Affected:	None												
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>1010</td><td>bbba</td><td>ffff</td><td>ffff</td></tr> </table>	1010	bbba	ffff	ffff								
1010	bbba	ffff	ffff										
Description:	<p>If bit 'b' in register 'f' is 1, then the next instruction is skipped.</p> <p>If bit 'b' is 1, then the next instruction fetched during the current instruction execution is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).</p>												
Words:	1												
Cycles:	1(2)												
Note:	3 cycles if skip and followed by a 2-word instruction.												
Q Cycle Activity:	<table border="1" style="width: 100%; text-align: center;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>No operation</td></tr> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	No operation				
Q1	Q2	Q3	Q4										
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Q1	Q2	Q3	Q4										
No operation	No operation	No operation	No operation										
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Q1	Q2	Q3	Q4										
No operation	No operation	No operation	No operation										
No operation	No operation	No operation	No operation										

Example: HERE BTFSS FLAG, 1, 0
 FALSE :
 TRUE :

Before Instruction
 PC = address (HERE)

After Instruction
 If FLAG<1> = 0;
 PC = address (FALSE)
 If FLAG<1> = 1;
 PC = address (TRUE)

BTG	Bit Toggle f								
Syntax:	[<i>label</i>] BTG f,b[<i>a</i>]								
Operands:	$0 \leq f \leq 255$ $0 \leq b < 7$ $a \in [0,1]$								
Operation:	$(f) \rightarrow f$								
Status Affected:	None								
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>0111</td><td>bbba</td><td>ffff</td><td>ffff</td></tr> </table>	0111	bbba	ffff	ffff				
0111	bbba	ffff	ffff						
Description:	Bit 'b' in data memory location 'f' is inverted. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1" style="width: 100%; text-align: center;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>Write register 'f'</td></tr> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write register 'f'
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write register 'f'						

Example: BTG PORTC, 4, 0

Before Instruction:

PORTC = 0111 0101 [0x75]

After Instruction:

PORTC = 0110 0101 [0x65]

BOV	Branch if Overflow												
Syntax:	[<i>label</i>] BOV n												
Operands:	$-128 \leq n \leq 127$												
Operation:	if overflow bit is '1' $(PC) + 2 + 2n \rightarrow PC$												
Status Affected:	None												
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>1110</td><td>0100</td><td>nnnn</td><td>nnnn</td></tr> </table>	1110	0100	nnnn	nnnn								
1110	0100	nnnn	nnnn										
Description:	If the Overflow bit is '1', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be $PC+2+2n$. This instruction is then a two-cycle instruction.												
Words:	1												
Cycles:	1(2)												
Q Cycle Activity:	<table border="1" style="width: 100%; text-align: center;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read literal 'n'</td><td>Process Data</td><td>Write to PC</td></tr> <tr> <td>No operation</td><td>No operation</td><td>No operation</td><td>No operation</td></tr> </table>	Q1	Q2	Q3	Q4	Decode	Read literal 'n'	Process Data	Write to PC	No operation	No operation	No operation	No operation
Q1	Q2	Q3	Q4										
Decode	Read literal 'n'	Process Data	Write to PC										
No operation	No operation	No operation	No operation										

If No Jump:

Q1	Q2	Q3	Q4
Decode	Read literal 'n'	Process Data	No operation

Example: HERE BOV Jump

Before Instruction

PC = address (HERE)

After Instruction

If Overflow = 1;
PC = address (Jump)
If Overflow = 0;
PC = address (HERE+2)

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BZ	Branch if Zero			
Syntax:	[<i>label</i>] BZ n			
Operands:	-128 ≤ n ≤ 127			
Operation:	if Zero bit is '1' (PC) + 2 + 2n → PC			
Status Affected:	None			
Encoding:	1110	0000	nnnn	nnnn
Description:	If the Zero bit is '1', then the program will branch. The 2's complement number '2n' is added to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is then a two-cycle instruction.			
Words:	1			
Cycles:	1(2)			
Q Cycle Activity:				
If Jump:				
	Q1	Q2	Q3	Q4
	Decode	Read literal 'n'	Process Data	Write to PC
	No operation	No operation	No operation	No operation
If No Jump:				
	Q1	Q2	Q3	Q4
	Decode	Read literal 'n'	Process Data	No operation

Example: HERE BZ Jump

Before Instruction

PC = address (HERE)

After Instruction

If Zero PC = 1;

PC = address (Jump)

If Zero PC = 0;

PC = address (HERE+2)

CALL	Subroutine Call			
Syntax:	[<i>label</i>] CALL k [.s]			
Operands:	0 ≤ k ≤ 1048575 s ∈ {0,1}			
Operation:	(PC) + 4 → TOS, k → PC<20:1>, if s = 1 (W) → WS, (STATUS) → STATUS,SS, (BSR) → BSRS			
Status Affected:	None			
Encoding:	1110	110s	k ₇ kkk	kkkk ₀
1st word (k<7:0>)	1111	k ₁₉ kkk	kkkk	kkkk ₈
2nd word(k<19:8>)				
Description:	Subroutine call of entire 2 Mbyte memory range. First, return address (PC+ 4) is pushed onto the return stack. If 's' = 1, the W, STATUS and BSR registers are also pushed into their respective shadow registers, WS, STATUS,SS and BSRS. If 's' = 0, no update occurs (default). Then, the 20-bit value 'k' is loaded into PC<20:1>. CALL is a two-cycle instruction.			
Words:	2			
Cycles:	2			
Q Cycle Activity:				
	Q1	Q2	Q3	Q4
	Decode	Read literal 'k'<7:0>,	Push PC to stack	Read literal 'k'<19:8>, Write to PC
	No operation	No operation	No operation	No operation

Example: HERE CALL THERE,1

Before Instruction

PC = address (HERE)

After Instruction

PC = address (THERE)

TOS = address (HERE + 4)

WS = W

BSRS = BSR

STATUS= STATUS

CLRF	Clear f				
Syntax:	[label] CLRF f [,a]				
Operands:	$0 \leq f \leq 255$ $a \in [0,1]$				
Operation:	$000h \rightarrow f$ $1 \rightarrow Z$				
Status Affected:	Z				
Encoding:	<table border="1"><tr><td>0110</td><td>101a</td><td>ffff</td><td>ffff</td></tr></table>	0110	101a	ffff	ffff
0110	101a	ffff	ffff		
Description:	Clears the contents of the specified register. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).				
Words:	1				
Cycles:	1				
Q Cycle Activity:					
	Q1 Q2 Q3 Q4				
	Decode Read register 'f' Process Data Write register 'f'				

Example: CLRF FLAG_REG,1

Before Instruction

FLAG_REG = 0x5A

After Instruction

FLAG_REG = 0x00

CLRWDT	Clear Watchdog Timer				
Syntax:	[label] CLRWDT				
Operands:	None				
Operation:	$000h \rightarrow WDT$, $000h \rightarrow WDT$ postscaler, $1 \rightarrow \overline{TO}$, $1 \rightarrow \overline{PD}$				
Status Affected:	$\overline{TO}, \overline{PD}$				
Encoding:	<table border="1"><tr><td>0000</td><td>0000</td><td>0000</td><td>0100</td></tr></table>	0000	0000	0000	0100
0000	0000	0000	0100		
Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the postscaler of the WDT. Status bits TO and PD are set.				
Words:	1				
Cycles:	1				
Q Cycle Activity:					
	Q1 Q2 Q3 Q4				
	Decode No operation Process Data No operation				

Example: CLRWDT

Before Instruction

WDT Counter = ?

After Instruction

WDT Counter = 0x00

WDT Postscaler = 0

TO = 1

PD = 1

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COMF	Complement f								
Syntax:	[label] COMF f [,d [,a]]								
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]								
Operation:	(f) → dest								
Status Affected:	N, Z								
Encoding:	0001 11da ffff ffff								
Description:	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).								
Words:	1								
Cycles:	1								
Q Cycle Activity:									
	<table border="1"> <thead> <tr> <th>Q1</th> <th>Q2</th> <th>Q3</th> <th>Q4</th> </tr> </thead> <tbody> <tr> <td>Decode</td> <td>Read register 'f'</td> <td>Process Data</td> <td>Write to destination</td> </tr> </tbody> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write to destination
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write to destination						

Example: COMF REG, 0 , 0

Before Instruction
REG = 0x13

After Instruction
REG = 0x13
W = 0xEC

CPFSEQ	Compare f with W, skip if f = W
Syntax:	[label] CPFSEQ f [,a]
Operands:	0 ≤ f ≤ 255 a ∈ [0,1]
Operation:	(f) – (W), skip if (f) = (W) (unsigned comparison)
Status Affected:	None
Encoding:	0110 001a ffff ffff
Description:	Compares the contents of data memory location 'f' to the contents of W by performing an unsigned subtraction. If f' = W, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).
Words:	1
Cycles:	1(2)
Note:	3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	No operation

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example: HERE CPFSEQ REG, 0
NEQUAL :
EQUAL :

Before Instruction

PC Address = HERE
W = ?
REG = ?

After Instruction

If REG = W;
PC = Address (EQUAL)
If REG ≠ W;
PC = Address (NEQUAL)

CPFSGT	Compare f with W, skip if f > W												
Syntax:	[label] CPFSGT f [,a]												
Operands:	$0 \leq f \leq 255$ $a \in [0,1]$												
Operation:	$(f) - (W)$, skip if $(f) > (W)$ (unsigned comparison)												
Status Affected:	None												
Encoding:	<table border="1"><tr><td>0110</td><td>010a</td><td>ffff</td><td>ffff</td></tr></table>	0110	010a	ffff	ffff								
0110	010a	ffff	ffff										
Description:	Compares the contents of data memory location 'f' to the contents of the W by performing an unsigned subtraction. If the contents of 'f' are greater than the contents of WREG, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).												
Words:	1												
Cycles:	1(2) Note: 3 cycles if skip and followed by a 2-word instruction.												
Q Cycle Activity:	<table border="1"><tr><td>Q1</td><td>Q2</td><td>Q3</td><td>Q4</td></tr><tr><td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>No operation</td></tr></table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	No operation				
Q1	Q2	Q3	Q4										
Decode	Read register 'f'	Process Data	No operation										
If skip:	<table border="1"><tr><td>Q1</td><td>Q2</td><td>Q3</td><td>Q4</td></tr><tr><td>No operation</td><td>No operation</td><td>No operation</td><td>No operation</td></tr></table>	Q1	Q2	Q3	Q4	No operation	No operation	No operation	No operation				
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Q1	Q2	Q3	Q4										
No operation	No operation	No operation	No operation										
No operation	No operation	No operation	No operation										

Example: HERE CPFSGT REG, 0
NGREATER :
GREATER :

Before Instruction
PC = Address (HERE)
W = ?

After Instruction
If REG > W;
PC = Address (GREATER)
If REG \leq W;
PC = Address (NGREATER)

CPFSLT	Compare f with W, skip if f < W												
Syntax:	[label] CPFSLT f [,a]												
Operands:	$0 \leq f \leq 255$ $a \in [0,1]$												
Operation:	$(f) - (W)$, skip if $(f) < (W)$ (unsigned comparison)												
Status Affected:	None												
Encoding:	<table border="1"><tr><td>0110</td><td>000a</td><td>ffff</td><td>ffff</td></tr></table>	0110	000a	ffff	ffff								
0110	000a	ffff	ffff										
Description:	Compares the contents of data memory location 'f' to the contents of W by performing an unsigned subtraction. If the contents of 'f' are less than the contents of W, then the fetched instruction is discarded and a NOP is executed instead, making this a two-cycle instruction. If 'a' is 0, the Access Bank will be selected. If 'a' is 1, the BSR will not be overridden (default).												
Words:	1												
Cycles:	1(2) Note: 3 cycles if skip and followed by a 2-word instruction.												
Q Cycle Activity:	<table border="1"><tr><td>Q1</td><td>Q2</td><td>Q3</td><td>Q4</td></tr><tr><td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>No operation</td></tr></table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	No operation				
Q1	Q2	Q3	Q4										
Decode	Read register 'f'	Process Data	No operation										
If skip:	<table border="1"><tr><td>Q1</td><td>Q2</td><td>Q3</td><td>Q4</td></tr><tr><td>No operation</td><td>No operation</td><td>No operation</td><td>No operation</td></tr></table>	Q1	Q2	Q3	Q4	No operation	No operation	No operation	No operation				
Q1	Q2	Q3	Q4										
No operation	No operation	No operation	No operation										
If skip and followed by 2-word instruction:	<table border="1"><tr><td>Q1</td><td>Q2</td><td>Q3</td><td>Q4</td></tr><tr><td>No operation</td><td>No operation</td><td>No operation</td><td>No operation</td></tr><tr><td>No operation</td><td>No operation</td><td>No operation</td><td>No operation</td></tr></table>	Q1	Q2	Q3	Q4	No operation	No operation	No operation	No operation	No operation	No operation	No operation	No operation
Q1	Q2	Q3	Q4										
No operation	No operation	No operation	No operation										
No operation	No operation	No operation	No operation										

Example: HERE CPFSLT REG, 1
NLESS :
LESS :

Before Instruction
PC = Address (HERE)
W = ?

After Instruction
If REG < W;
PC = Address (LESS)
If REG \geq W;
PC = Address (NLESS)

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DAW	Decimal Adjust W Register								
Syntax:	[label] DAW								
Operands:	None								
Operation:	If [W<3:0> >9] or [DC = 1] then (W<3:0>) + 6 → W<3:0>; else (W<3:0>) → W<3:0>; If [W<7:4> >9] or [C = 1] then (W<7:4>) + 6 → W<7:4>; else (W<7:4>) → W<7:4>;								
Status Affected:	C								
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>0000</td><td>0000</td><td>0000</td><td>0111</td></tr> </table>	0000	0000	0000	0111				
0000	0000	0000	0111						
Description:	DAW adjusts the eight-bit value in W, resulting from the earlier addition of two variables (each in packed BCD format) and produces a correct packed BCD result.								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read register W</td><td>Process Data</td><td>Write W</td></tr> </table>	Q1	Q2	Q3	Q4	Decode	Read register W	Process Data	Write W
Q1	Q2	Q3	Q4						
Decode	Read register W	Process Data	Write W						

Example1: DAW

Before Instruction

```

W      = 0xA5
C      = 0
DC     = 0

```

After Instruction

```

W      = 0x05
C      = 1
DC     = 0

```

Example 2:

Before Instruction

```

W      = 0xCE
C      = 0
DC     = 0

```

After Instruction

```

W      = 0x34
C      = 1
DC     = 0

```

DECF	Decrement f								
Syntax:	[label] DECF f [,d [,a]]								
Operands:	0 ≤ f ≤ 255 d ∈ {0, 1} a ∈ {0, 1}								
Operation:	(f) – 1 → dest								
Status Affected:	C, DC, N, OV, Z								
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>0000</td><td>01da</td><td>ffff</td><td>ffff</td></tr> </table>	0000	01da	ffff	ffff				
0000	01da	ffff	ffff						
Description:	Decrement register 'f'. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>Write to destination</td></tr> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write to destination
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write to destination						

Example: DECF CNT, 1, 0

Before Instruction

```

CNT    = 0x01
Z      = 0

```

After Instruction

```

CNT    = 0x00
Z      = 1

```

DECFSZ	Decrement f, skip if 0
Syntax:	[<i>label</i>] DECFSZ f [,d [,a]]
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]
Operation:	(f) – 1 → dest, skip if result = 0
Status Affected:	None
Encoding:	0010 11da ffff ffff
Description:	The contents of register 'f' are decremented. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is placed back in register 'f' (default). If the result is 0, the next instruction, which is already fetched, is discarded and a NOP is executed instead, making it a two-cycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).
Words:	1
Cycles:	1(2)
Note:	3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example: HERE DECFSZ CNT, 1, 1
GOTO LOOP
CONTINUE

Before Instruction

PC = Address (HERE)

After Instruction

CNT = CNT - 1
If CNT = 0;
PC = Address (CONTINUE)
If CNT ≠ 0;
PC = Address (HERE+2)

DCFSNZ	Decrement f, skip if not 0
Syntax:	[<i>label</i>] DCFSNZ f [,d [,a]]
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]
Operation:	(f) – 1 → dest, skip if result ≠ 0
Status Affected:	None
Encoding:	0100 11da ffff ffff
Description:	The contents of register 'f' are decremented. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is placed back in register 'f' (default). If the result is not 0, the next instruction, which is already fetched, is discarded, and a NOP is executed instead, making it a two-cycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).

Words:

1

Cycles:

1(2)

Note: 3 cycles if skip and followed by a 2-word instruction.

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f'	Process Data	Write to destination

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

Example: HERE DCFSNZ TEMP, 1, 0
ZERO :
NZERO :

Before Instruction

TEMP = ?

After Instruction

TEMP = TEMP - 1,
If TEMP = 0;
PC = Address (ZERO)
If TEMP ≠ 0;
PC = Address (NZERO)

PIC18FXX20

GOTO		Unconditional Branch														
Syntax:		[<i>label</i>] GOTO k														
Operands:		0 ≤ k ≤ 1048575														
Operation:		k → PC<20:1>														
Status Affected:		None														
Encoding:		<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>1110</td> <td>1111</td> <td>k₇kkk</td> <td>kkk₀</td> </tr> <tr> <td>1111</td> <td>k₁₉kkk</td> <td>kkkk</td> <td>kkk₈</td> </tr> </table>				1110	1111	k ₇ kkk	kkk ₀	1111	k ₁₉ kkk	kkkk	kkk ₈			
1110	1111	k ₇ kkk	kkk ₀													
1111	k ₁₉ kkk	kkkk	kkk ₈													
Description:		<p>GOTO allows an unconditional branch anywhere within entire 2 Mbyte memory range. The 20-bit value 'k' is loaded into PC<20:1>. GOTO is always a two-cycle instruction.</p>														
Words:	2															
Cycles:	2															
Q Cycle Activity:																
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">Q1</th> <th style="width: 25%;">Q2</th> <th style="width: 25%;">Q3</th> <th style="width: 25%;">Q4</th> </tr> </thead> <tbody> <tr> <td>Decode</td> <td>Read literal 'k'<7:0>,</td> <td>No operation</td> <td>Read literal 'k'<19:8>, Write to PC</td> </tr> <tr> <td>No operation</td> <td>No operation</td> <td>No operation</td> <td>No operation</td> </tr> </tbody> </table>					Q1	Q2	Q3	Q4	Decode	Read literal 'k'<7:0>,	No operation	Read literal 'k'<19:8>, Write to PC	No operation	No operation	No operation	No operation
Q1	Q2	Q3	Q4													
Decode	Read literal 'k'<7:0>,	No operation	Read literal 'k'<19:8>, Write to PC													
No operation	No operation	No operation	No operation													

Example: GOTO THERE

After Instruction

PC = Address (THERE)

INCF		Increment f										
Syntax:		[<i>label</i>] INCF f [,d [,a]]										
Operands:		0 ≤ f ≤ 255										
		d ∈ [0,1]										
		a ∈ [0,1]										
Operation:		(f) + 1 → dest										
Status Affected:		C, DC, N, OV, Z										
Encoding:		<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>0010</td> <td>10da</td> <td>ffff</td> <td>ffff</td> </tr> </table>				0010	10da	ffff	ffff			
0010	10da	ffff	ffff									
Description:		<p>The contents of register 'f' are incremented. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is placed back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).</p>										
Words:	1											
Cycles:	1											
Q Cycle Activity:												
<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">Q1</th> <th style="width: 25%;">Q2</th> <th style="width: 25%;">Q3</th> <th style="width: 25%;">Q4</th> </tr> </thead> <tbody> <tr> <td>Decode</td> <td>Read register 'f'</td> <td>Process Data</td> <td>Write to destination</td> </tr> </tbody> </table>					Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write to destination
Q1	Q2	Q3	Q4									
Decode	Read register 'f'	Process Data	Write to destination									

Example: INCF CNT, 1, 0

Before Instruction

CNT	=	0xFF
Z	=	0
C	=	?
DC	=	?

After Instruction

CNT	=	0x00
Z	=	1
C	=	1
DC	=	1

INCFSZ	Increment f, skip if 0							
Syntax:	[label] INCFSZ f [,d [,a]]							
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]							
Operation:	(f) + 1 → dest, skip if result = 0							
Status Affected:	None							
Encoding:	0011	11da	ffff	ffff				
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is placed back in register 'f'. (default). If the result is 0, the next instruction, which is already fetched, is discarded, and a NOP is executed instead, making it a two-cycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).							
Words:	1							
Cycles:	1(2)							
Note: 3 cycles if skip and followed by a 2-word instruction.								
Q Cycle Activity:								
	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process Data	Write to destination				

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example: HERE INCFSZ CNT, 1, 0
NZERO :
ZERO :

Before Instruction

PC = Address (HERE)

After Instruction

CNT = CNT + 1
If CNT = 0;
PC = Address (ZERO)
If CNT ≠ 0;
PC = Address (NZERO)

INFSNZ	Increment f, skip if not 0							
Syntax:	[label] INFSNZ f [,d [,a]]							
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]							
Operation:	(f) + 1 → dest, skip if result ≠ 0							
Status Affected:	None							
Encoding:	0100	10da	ffff	ffff				
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is placed back in register 'f' (default). If the result is not 0, the next instruction, which is already fetched, is discarded, and a NOP is executed instead, making it a two-cycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).							
Words:	1							
Cycles:	1(2)							
Note: 3 cycles if skip and followed by a 2-word instruction.								
Q Cycle Activity:								
	Q1	Q2	Q3	Q4				
	Decode	Read register 'f'	Process Data	Write to destination				

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example: HERE INFSNZ REG, 1, 0
ZERO :
NZERO :

Before Instruction

PC = Address (HERE)

After Instruction

REG = REG + 1
If REG ≠ 0;
PC = Address (NZERO)
If REG = 0;
PC = Address (ZERO)

PIC18FXX20

IORLW	Inclusive OR literal with W								
Syntax:	[label] IORLW k								
Operands:	$0 \leq k \leq 255$								
Operation:	(W) .OR. k \rightarrow W								
Status Affected:	N, Z								
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0000</td> <td>1001</td> <td>kkkk</td> <td>kkkk</td> </tr> </table>	0000	1001	kkkk	kkkk				
0000	1001	kkkk	kkkk						
Description:	The contents of W are OR'ed with the eight-bit literal 'k'. The result is placed in W.								
Words:	1								
Cycles:	1								
Q Cycle Activity:									
	<table border="1" style="display: inline-table; width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">Q1</th> <th style="width: 25%;">Q2</th> <th style="width: 25%;">Q3</th> <th style="width: 25%;">Q4</th> </tr> </thead> <tbody> <tr> <td>Decode</td> <td>Read literal 'k'</td> <td>Process Data</td> <td>Write to W</td> </tr> </tbody> </table>	Q1	Q2	Q3	Q4	Decode	Read literal 'k'	Process Data	Write to W
Q1	Q2	Q3	Q4						
Decode	Read literal 'k'	Process Data	Write to W						

Example: IORLW 0x35

Before Instruction

W = 0x9A

After Instruction

W = 0xBF

IORWF	Inclusive OR W with f								
Syntax:	[label] IORWF f [,d [,a]								
Operands:	$0 \leq f \leq 255$ $d \in [0,1]$ $a \in [0,1]$								
Operation:	(W) .OR. (f) \rightarrow dest								
Status Affected:	N, Z								
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0001</td> <td>00da</td> <td>ffff</td> <td>ffff</td> </tr> </table>	0001	00da	ffff	ffff				
0001	00da	ffff	ffff						
Description:	Inclusive OR W with register 'f'. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is placed back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).								
Words:	1								
Cycles:	1								
Q Cycle Activity:									
	<table border="1" style="display: inline-table; width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="width: 25%;">Q1</th> <th style="width: 25%;">Q2</th> <th style="width: 25%;">Q3</th> <th style="width: 25%;">Q4</th> </tr> </thead> <tbody> <tr> <td>Decode</td> <td>Read register 'f'</td> <td>Process Data</td> <td>Write to destination</td> </tr> </tbody> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write to destination
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write to destination						

Example: IORWF RESULT, 0, 1

Before Instruction

RESULT = 0x13

W = 0x91

After Instruction

RESULT = 0x13

W = 0x93

LFSR	Load FSR															
Syntax:	[<i>label</i>] LFSR <i>f,k</i>															
Operands:	0 ≤ <i>f</i> ≤ 2 0 ≤ <i>k</i> ≤ 4095															
Operation:	<i>k</i> → FSR <i>f</i>															
Status Affected:	None															
Encoding:	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>1110</td><td>1110</td><td>00ff</td><td>$k_{11}k_{kkk}$</td></tr> <tr> <td>1111</td><td>0000</td><td>$k_{7}k_{kk}$</td><td>k_{kkk}</td></tr> </table>				1110	1110	00ff	$k_{11}k_{kkk}$	1111	0000	$k_{7}k_{kk}$	k_{kkk}				
1110	1110	00ff	$k_{11}k_{kkk}$													
1111	0000	$k_{7}k_{kk}$	k_{kkk}													
Description:	The 12-bit literal 'k' is loaded into the file select register pointed to by ' <i>f</i> '.															
Words:	2															
Cycles:	2															
Q Cycle Activity:	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Q1</th><th style="text-align: center;">Q2</th><th style="text-align: center;">Q3</th><th style="text-align: center;">Q4</th></tr> </thead> <tbody> <tr> <td style="text-align: center;">Decode</td><td style="text-align: center;">Read literal '<i>k</i>' MSB</td><td style="text-align: center;">Process Data</td><td style="text-align: center;">Write literal '<i>k</i>' MSB to FSR<i>fH</i></td></tr> <tr> <td style="text-align: center;">Decode</td><td style="text-align: center;">Read literal '<i>k</i>' LSB</td><td style="text-align: center;">Process Data</td><td style="text-align: center;">Write literal '<i>k</i>' to FSR<i>fL</i></td></tr> </tbody> </table>				Q1	Q2	Q3	Q4	Decode	Read literal ' <i>k</i> ' MSB	Process Data	Write literal ' <i>k</i> ' MSB to FSR <i>fH</i>	Decode	Read literal ' <i>k</i> ' LSB	Process Data	Write literal ' <i>k</i> ' to FSR <i>fL</i>
Q1	Q2	Q3	Q4													
Decode	Read literal ' <i>k</i> ' MSB	Process Data	Write literal ' <i>k</i> ' MSB to FSR <i>fH</i>													
Decode	Read literal ' <i>k</i> ' LSB	Process Data	Write literal ' <i>k</i> ' to FSR <i>fL</i>													

Example: LFSR 2, 0x3AB

After Instruction

FSR2H	=	0x03
FSR2L	=	0xAB

MOVF	Move f							
Syntax:	[<i>label</i>] MOVF <i>f,[d],[a]</i>							
Operands:	0 ≤ <i>f</i> ≤ 255 <i>d</i> ∈ [0,1] <i>a</i> ∈ [0,1]							
Operation:	<i>f</i> → dest							
Status Affected:	N, Z							
Encoding:	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <td>0101</td><td>00da</td><td>ffff</td><td>ffff</td></tr> </table>				0101	00da	ffff	ffff
0101	00da	ffff	ffff					
Description:	The contents of register ' <i>f</i> ' are moved to a destination dependent upon the status of ' <i>d</i> '. If ' <i>d</i> ' is 0, the result is placed in <i>W</i> . If ' <i>d</i> ' is 1, the result is placed back in register ' <i>f</i> ' (default). Location ' <i>f</i> ' can be anywhere in the 256 byte bank. If ' <i>a</i> ' is 0, the Access Bank will be selected, overriding the BSR value. If ' <i>a</i> ' = 1, then the bank will be selected as per the BSR value (default).							
Words:	1							
Cycles:	1							

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register ' <i>f</i> '	Process Data	Write <i>W</i>

Example: MOVF REG, 0, 0

Before Instruction

REG	=	0x22
W	=	0xFF

After Instruction

REG	=	0x22
W	=	0x22

PIC18FXX20

MOVFF	Move f to f
Syntax:	[label] MOVFF f _s ,f _d
Operands:	0 ≤ f _s ≤ 4095 0 ≤ f _d ≤ 4095
Operation:	(f _s) → f _d
Status Affected:	None
Encoding:	
1st word (source)	1100 ffff ffff ffff _s
2nd word (destin.)	1111 ffff ffff ffff _d
Description:	<p>The contents of source register 'f_s' are moved to destination register 'f_d'. Location of source 'f_s' can be anywhere in the 4096 byte data space (000h to FFFh), and location of destination 'f_d' can also be anywhere from 000h to FFFh.</p> <p>Either source or destination can be W (a useful special situation).</p> <p>MOVFF is particularly useful for transferring a data memory location to a peripheral register (such as the transmit buffer or an I/O port).</p> <p>The MOVFF instruction cannot use the PCL, TOSU, TOSH or TOSL as the destination register</p>
Words:	2
Cycles:	2 (3)

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	Read register 'f' (src)	Process Data	No operation
Decode	No operation No dummy read	No operation	Write register 'f' (dest)

Example: MOVFF REG1, REG2

Before Instruction

REG1 = 0x33
REG2 = 0x11

After Instruction

REG1 = 0x33,
REG2 = 0x33

MOVLB	Move literal to low nibble in BSR		
Syntax:	[label] MOVLB k		
Operands:	0 ≤ k ≤ 255		
Operation:	k → BSR		
Status Affected:	None		
Encoding:			
Description:	The 8-bit literal 'k' is loaded into the Bank Select Register (BSR).		
Words:	1		
Cycles:	1		
Q Cycle Activity:			
Q1	Q2	Q3	Q4
Decode	Read literal 'k'	Process Data	Write literal 'k' to BSR

Example: MOVLB 5

Before Instruction
BSR register = 0x02
After Instruction
BSR register = 0x05

MOVLW
Move literal to W

Syntax:	[<i>label</i>] MOVLW <i>k</i>			
Operands:	0 ≤ <i>k</i> ≤ 255			
Operation:	<i>k</i> → W			
Status Affected:	None			
Encoding:	0000	1110	kkkk	kkkk
Description:	The eight-bit literal ' <i>k</i> ' is loaded into W.			
Words:	1			
Cycles:	1			
Q Cycle Activity:				
	Q1	Q2	Q3	Q4
	Decode	Read literal ' <i>k</i> '	Process Data	Write to W

Example: MOVLW 0x5A

After Instruction

$$W = 0x5A$$

MOVWF
Move W to f

Syntax:	[<i>label</i>] MOVWF <i>f</i> [, <i>a</i>]			
Operands:	0 ≤ <i>f</i> ≤ 255 <i>a</i> ∈ [0,1]			
Operation:	(W) → <i>f</i>			
Status Affected:	None			
Encoding:	0110	111a	ffff	ffff
Description:	Move data from W to register ' <i>f</i> '. Location ' <i>f</i> ' can be anywhere in the 256 byte bank. If ' <i>a</i> ' is 0, the Access Bank will be selected, overriding the BSR value. If ' <i>a</i> ' = 1, then the bank will be selected as per the BSR value (default).			

Words: 1

Cycles: 1

Q Cycle Activity:

	Q1	Q2	Q3	Q4
	Decode	Read register ' <i>f</i> '	Process Data	Write register ' <i>f</i> '

Example: MOVWF REG, 0

Before Instruction

$$\begin{aligned} W &= 0x4F \\ \text{REG} &= 0xFF \end{aligned}$$

After Instruction

$$\begin{aligned} W &= 0x4F \\ \text{REG} &= 0x4F \end{aligned}$$

MULLW	Multiply Literal with W											
Syntax:	[label]	MULLW	k									
Operands:	0 ≤ k ≤ 255											
Operation:	(W) x k → PRODH:PRODL											
Status Affected:	None											
Encoding:	0000	1101	kkkk	kkkk								
Description:	An unsigned multiplication is carried out between the contents of W and the 8-bit literal 'k'. The 16-bit result is placed in PRODH:PRODL register pair. PRODH contains the high byte. W is unchanged. None of the status flags are affected. Note that neither overflow nor carry is possible in this operation. A zero result is possible but not detected.											
Words:	1											
Cycles:	1											
Q Cycle Activity:	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read literal 'k'</td><td>Process Data</td><td>Write registers PRODH: PRODL</td></tr> </table>				Q1	Q2	Q3	Q4	Decode	Read literal 'k'	Process Data	Write registers PRODH: PRODL
Q1	Q2	Q3	Q4									
Decode	Read literal 'k'	Process Data	Write registers PRODH: PRODL									

Example: MULLW 0xC4

Before Instruction

W	=	0xE2
PRODH	=	?
PRODL	=	?

After Instruction

W	=	0xE2
PRODH	=	0xAD
PRODL	=	0x08

MULWF	Multiply W with f											
Syntax:	[label]	MULWF	f [,a]									
Operands:	0 ≤ f ≤ 255											
	a ∈ [0,1]											
Operation:	(W) x (f) → PRODH:PRODL											
Status Affected:	None											
Encoding:	0000	001a	ffff	ffff								
Description:	An unsigned multiplication is carried out between the contents of W and the register file location 'f'. The 16-bit result is stored in the PRODH:PRODL register pair. PRODH contains the high byte. Both W and 'f' are unchanged. None of the status flags are affected. Note that neither overflow nor carry is possible in this operation. A zero result is possible but not detected. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a'= 1, then the bank will be selected as per the BSR value (default).											
Words:	1											
Cycles:	1											
Q Cycle Activity:	<table border="1" style="margin-left: auto; margin-right: auto;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>Write registers PRODH: PRODL</td></tr> </table>				Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write registers PRODH: PRODL
Q1	Q2	Q3	Q4									
Decode	Read register 'f'	Process Data	Write registers PRODH: PRODL									

Example: MULWF REG, 1

Before Instruction

W	=	0xC4
REG	=	0xB5
PRODH	=	?
PRODL	=	?

After Instruction

W	=	0xC4
REG	=	0xB5
PRODH	=	0x8A
PRODL	=	0x94

NEGF	Negate f								
Syntax:	[label] NEGF f [,a]								
Operands:	$0 \leq f \leq 255$ $a \in [0,1]$								
Operation:	$(\bar{f}) + 1 \rightarrow f$								
Status Affected:	N, OV, C, DC, Z								
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0110</td> <td>110a</td> <td>ffff</td> <td>ffff</td> </tr> </table>	0110	110a	ffff	ffff				
0110	110a	ffff	ffff						
Description:	Location 'f' is negated using two's complement. The result is placed in the data memory location 'f'. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value.								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <th>Q1</th> <th>Q2</th> <th>Q3</th> <th>Q4</th> </tr> <tr> <td>Decode</td> <td>Read register 'f'</td> <td>Process Data</td> <td>Write register 'f'</td> </tr> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write register 'f'
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write register 'f'						

Example: NEGREG , 1

Before Instruction

REG = 0011 1010 [0x3A]

After Instruction

REG = 1100 0110 [0xC6]

NOP	No Operation								
Syntax:	[label] NOP								
Operands:	None								
Operation:	No operation								
Status Affected:	None								
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0000</td> <td>0000</td> <td>0000</td> <td>0000</td> </tr> <tr> <td>1111</td> <td>xxxx</td> <td>xxxx</td> <td>xxxx</td> </tr> </table>	0000	0000	0000	0000	1111	xxxx	xxxx	xxxx
0000	0000	0000	0000						
1111	xxxx	xxxx	xxxx						
Description:	No operation.								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <th>Q1</th> <th>Q2</th> <th>Q3</th> <th>Q4</th> </tr> <tr> <td>Decode</td> <td>No operation</td> <td>No operation</td> <td>No operation</td> </tr> </table>	Q1	Q2	Q3	Q4	Decode	No operation	No operation	No operation
Q1	Q2	Q3	Q4						
Decode	No operation	No operation	No operation						

Example:

None.

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POP		Pop Top of Return Stack	
Syntax:	[<i>label</i>] POP		
Operands:	None		
Operation:	(TOS) → bit bucket		
Status Affected:	None		
Encoding:	0000 0000 0000 0110		
Description:	The TOS value is pulled off the return stack and is discarded. The TOS value then becomes the previous value that was pushed onto the return stack. This instruction is provided to enable the user to properly manage the return stack to incorporate a software stack.		
Words:	1		
Cycles:	1		
Q Cycle Activity:			
	Q1 Q2 Q3 Q4		
	Decode No operation POP TOS value No operation		

<u>Example:</u>	POP	
	GOTO	NEW
Before Instruction		
TOS Stack (1 level down)		
	= 0031A2h	
	= 014332h	
After Instruction		
TOS	= 014332h	
PC	= NEW	

PUSH		Push Top of Return Stack	
Syntax:	[<i>label</i>] PUSH		
Operands:	None		
Operation:	(PC+2) → TOS		
Status Affected:	None		
Encoding:	0000 0000 0000 0101		
Description:	The PC+2 is pushed onto the top of the return stack. The previous TOS value is pushed down on the stack. This instruction allows implementing a software stack by modifying TOS, and then pushing it onto the return stack.		
Words:	1		
Cycles:	1		
Q Cycle Activity:			
	Q1 Q2 Q3 Q4		
	Decode PUSH PC+2 onto return stack No operation No operation		

<u>Example:</u>	PUSH	
Before Instruction		
TOS PC		
	= 00345Ah	
	= 000124h	
After Instruction		
PC	= 000126h	
TOS	= 000126h	
Stack (1 level down)	= 00345Ah	

RCALL	Relative Call												
Syntax:	[<i>label</i>] RCALL n												
Operands:	-1024 ≤ n ≤ 1023												
Operation:	(PC) + 2 → TOS, (PC) + 2 + 2n → PC												
Status Affected:	None												
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>1101</td> <td>1nnn</td> <td>nnnn</td> <td>nnnn</td> </tr> </table>	1101	1nnn	nnnn	nnnn								
1101	1nnn	nnnn	nnnn										
Description:	Subroutine call with a jump up to 1K from the current location. First, return address (PC+2) is pushed onto the stack. Then, add the 2's complement number '2n' to the PC. Since the PC will have incremented to fetch the next instruction, the new address will be PC+2+2n. This instruction is a two-cycle instruction.												
Words:	1												
Cycles:	2												
Q Cycle Activity:	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Q1</th> <th style="text-align: center;">Q2</th> <th style="text-align: center;">Q3</th> <th style="text-align: center;">Q4</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Decode</td> <td style="text-align: center;">Start reset</td> <td style="text-align: center;">No operation</td> <td style="text-align: center;">No operation</td> </tr> <tr> <td style="text-align: center;">No operation</td> <td style="text-align: center;">No operation</td> <td style="text-align: center;">No operation</td> <td style="text-align: center;">No operation</td> </tr> </tbody> </table>	Q1	Q2	Q3	Q4	Decode	Start reset	No operation	No operation	No operation	No operation	No operation	No operation
Q1	Q2	Q3	Q4										
Decode	Start reset	No operation	No operation										
No operation	No operation	No operation	No operation										

Example: HERE RCALL Jump

Before Instruction

PC = Address (HERE)

After Instruction

PC = Address (Jump)
TOS = Address (HERE+2)

RESET	Reset								
Syntax:	[<i>label</i>] RESET								
Operands:	None								
Operation:	Reset all registers and flags that are affected by a MCLR Reset.								
Status Affected:	All								
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0000</td> <td>0000</td> <td>1111</td> <td>1111</td> </tr> </table>	0000	0000	1111	1111				
0000	0000	1111	1111						
Description:	This instruction provides a way to execute a MCLR Reset in software.								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th style="text-align: center;">Q1</th> <th style="text-align: center;">Q2</th> <th style="text-align: center;">Q3</th> <th style="text-align: center;">Q4</th> </tr> </thead> <tbody> <tr> <td style="text-align: center;">Decode</td> <td style="text-align: center;">Start reset</td> <td style="text-align: center;">No operation</td> <td style="text-align: center;">No operation</td> </tr> </tbody> </table>	Q1	Q2	Q3	Q4	Decode	Start reset	No operation	No operation
Q1	Q2	Q3	Q4						
Decode	Start reset	No operation	No operation						

Example: RESET

After Instruction

Registers = Reset Value
Flags* = Reset Value

RETFIE	Return from Interrupt				
Syntax:	[<i>label</i>] RETFIE [s]				
Operands:	s ∈ [0,1]				
Operation:	(TOS) → PC, 1 → GIE/GIEH or PEIE/GIEL, if s = 1 (WS) → W, (STATUS) → STATUS, (BSRS) → BSR, PCLATU, PCLATH are unchanged.				
Status Affected:	GIE/GIEH, PEIE/GIEL.				
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0000</td> <td>0000</td> <td>0001</td> <td>000s</td> </tr> </table>	0000	0000	0001	000s
0000	0000	0001	000s		
Description:	Return from Interrupt. Stack is popped and Top-of-Stack (TOS) is loaded into the PC. Interrupts are enabled by setting either the high or low priority global interrupt enable bit. If 's' = 1, the contents of the shadow registers WS, STATUS and BSRS are loaded into their corresponding registers, W, STATUS and BSR. If 's' = 0, no update of these registers occurs (default).				
Words:	1				
Cycles:	2				

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	No operation	pop PC from stack Set GIEH or GIEL
No operation	No operation	No operation	No operation

Example: RETFIE 1

After Interrupt

PC	=	TOS
W	=	WS
BSR	=	BSRS
STATUS	=	STATUS
GIE/GIEH, PEIE/GIEL	=	1

RETLW	Return Literal to W												
Syntax:	[<i>label</i>] RETLW k												
Operands:	0 ≤ k ≤ 255												
Operation:	k → W, (TOS) → PC, PCLATU, PCLATH are unchanged												
Status Affected:	None												
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <td>0000</td> <td>1100</td> <td>kkkk</td> <td>kkkk</td> </tr> </table>	0000	1100	kkkk	kkkk								
0000	1100	kkkk	kkkk										
Description:	W is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). The high address latch (PCLATH) remains unchanged.												
Words:	1												
Cycles:	2												
Q Cycle Activity:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr> <th>Q1</th> <th>Q2</th> <th>Q3</th> <th>Q4</th> </tr> <tr> <td>Decode</td> <td>Read literal 'k'</td> <td>Process Data</td> <td>pop PC from stack, Write to W</td> </tr> <tr> <td>No operation</td> <td>No operation</td> <td>No operation</td> <td>No operation</td> </tr> </table>	Q1	Q2	Q3	Q4	Decode	Read literal 'k'	Process Data	pop PC from stack, Write to W	No operation	No operation	No operation	No operation
Q1	Q2	Q3	Q4										
Decode	Read literal 'k'	Process Data	pop PC from stack, Write to W										
No operation	No operation	No operation	No operation										

Example:

```

CALL TABLE ; W contains table
            ; offset value
            ; W now has
            ; table value
:
TABLE
    ADDWF PCL ; W = offset
    RETLW k0 ; Begin table
    RETLW k1 ;
:
:
RETLW kn ; End of table

```

Before Instruction

W = 0x07

After Instruction

W = value of kn

RETURN	Return from Subroutine												
Syntax:	[<i>label</i>] RETURN [s]												
Operands:	s ∈ [0,1]												
Operation:	(TOS) → PC, if s = 1 (WS) → W, (STATUSS) → STATUS, (BSRS) → BSR, PCLATU, PCLATH are unchanged												
Status Affected:	None												
Encoding:	0000 0000 0001 001s												
Description:	Return from subroutine. The stack is popped and the top of the stack (TOS) is loaded into the program counter. If 's' = 1, the contents of the shadow registers WS, STATUSS and BSRS are loaded into their corresponding registers, W, STATUS and BSR. If 's' = 0, no update of these registers occurs (default).												
Words:	1												
Cycles:	2												
Q Cycle Activity:													
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> </thead> <tbody> <tr> <td>Decode</td><td>No operation</td><td>Process Data</td><td>pop PC from stack</td></tr> <tr> <td>No operation</td><td>No operation</td><td>No operation</td><td>No operation</td></tr> </tbody> </table>	Q1	Q2	Q3	Q4	Decode	No operation	Process Data	pop PC from stack	No operation	No operation	No operation	No operation
Q1	Q2	Q3	Q4										
Decode	No operation	Process Data	pop PC from stack										
No operation	No operation	No operation	No operation										

Example: RETURN

After Interrupt
PC = TOS

RLCF	Rotate Left f through Carry								
Syntax:	[<i>label</i>] RLCF f [d [a]								
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]								
Operation:	(f<n>) → dest<n+1>, (f<7>) → C, (C) → dest<0>								
Status Affected:	C, N, Z								
Encoding:	0011 01da ffff ffff								
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' = 1, then the bank will be selected as per the BSR value (default).								
	<pre> graph LR C((C)) --> F[register f] F --> C </pre>								
Words:	1								
Cycles:	1								
Q Cycle Activity:									
	<table border="1" style="width: 100%; border-collapse: collapse;"> <thead> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> </thead> <tbody> <tr> <td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>Write to destination</td></tr> </tbody> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write to destination
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write to destination						

Example: RLCF REG, 0, 0

Before Instruction

REG = 1110 0110
C = 0

After Instruction

REG = 1110 0110
W = 1100 1100
C = 1

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RLNCF	Rotate Left f (no carry)			
Syntax:	[label] RLNCF f [,d [,a]]			
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]			
Operation:	(f<n>) → dest<n+1>, (f<7>) → dest<0>			
Status Affected:	N, Z			
Encoding:	0100 01da ffff ffff			
Description:	The contents of register 'f' are rotated one bit to the left. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).			
Words:	1			
Cycles:	1			
Q Cycle Activity:				
	Q1 Q2 Q3 Q4			
	Decode	Read register 'f'	Process Data	Write to destination

Example: RLNCF REG, 1, 0

Before Instruction

REG = 1010 1011

After Instruction

REG = 0101 0111

RRCF	Rotate Right f through Carry			
Syntax:	[label] RRCF f [,d [,a]]			
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]			
Operation:	(f<n>) → dest<n-1>, (f<0>) → C, (C) → dest<7>			
Status Affected:	C, N, Z			
Encoding:	0011 00da ffff ffff			
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is placed back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).			
Words:	1			
Cycles:	1			
Q Cycle Activity:				
	Q1 Q2 Q3 Q4			
	Decode	Read register 'f'	Process Data	Write to destination

Example: RRCF REG, 0, 0

Before Instruction

REG = 1110 0110
C = 0

After Instruction

REG = 1110 0110
W = 0111 0011
C = 0

RRNCF	Rotate Right f (no carry)								
Syntax:	[label] RRNCF f [,d [,a]]								
Operands:	$0 \leq f \leq 255$ $d \in [0,1]$ $a \in [0,1]$								
Operation:	$(f < n >) \rightarrow \text{dest} < n-1 >$, $(f < 0 >) \rightarrow \text{dest} < 7 >$								
Status Affected:	N, Z								
Encoding:	0100 00da ffff ffff								
Description:	The contents of register 'f' are rotated one bit to the right. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is placed back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1"> <tr> <th>Q1</th> <th>Q2</th> <th>Q3</th> <th>Q4</th> </tr> <tr> <td>Decode</td> <td>Read register 'f'</td> <td>Process Data</td> <td>Write register 'f'</td> </tr> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write register 'f'
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write register 'f'						

Example 1: RRNCF REG, 1, 0

Before Instruction
REG = 1101 0111
After Instruction
REG = 1110 1011

Example 2: RRNCF REG, 0, 0

Before Instruction
W = ?
REG = 1101 0111
After Instruction
W = 1110 1011
REG = 1101 0111

SETF	Set f								
Syntax:	[label] SETF f [,a]								
Operands:	$0 \leq f \leq 255$ $a \in [0,1]$								
Operation:	FFh \rightarrow f								
Status Affected:	None								
Encoding:	0110 100a ffff ffff								
Description:	The contents of the specified register are set to FFh. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1"> <tr> <th>Q1</th> <th>Q2</th> <th>Q3</th> <th>Q4</th> </tr> <tr> <td>Decode</td> <td>Read register 'f'</td> <td>Process Data</td> <td>Write register 'f'</td> </tr> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write register 'f'
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write register 'f'						

Example: SETF REG, 1

Before Instruction
REG = 0x5A
After Instruction
REG = 0xFF

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SLEEP	Enter SLEEP mode								
Syntax:	[label] SLEEP								
Operands:	None								
Operation:	00h → WDT, 0 → WDT postscaler, 1 → $\overline{\text{TO}}$, 0 → $\overline{\text{PD}}$								
Status Affected:	$\overline{\text{TO}}$, $\overline{\text{PD}}$								
Encoding:	<table border="1"><tr><td>0000</td><td>0000</td><td>0000</td><td>0011</td></tr></table>	0000	0000	0000	0011				
0000	0000	0000	0011						
Description:	The power-down status bit (PD) is cleared. The time-out status bit ($\overline{\text{TO}}$) is set. Watchdog Timer and its postscaler are cleared. The processor is put into SLEEP mode with the oscillator stopped.								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>No operation</td><td>Process Data</td><td>Go to sleep</td></tr> </table>	Q1	Q2	Q3	Q4	Decode	No operation	Process Data	Go to sleep
Q1	Q2	Q3	Q4						
Decode	No operation	Process Data	Go to sleep						

Example: SLEEP

Before Instruction

$$\begin{array}{l} \overline{\text{TO}} = ? \\ \overline{\text{PD}} = ? \end{array}$$

After Instruction

$$\begin{array}{l} \overline{\text{TO}} = 1 \dagger \\ \overline{\text{PD}} = 0 \end{array}$$

† If WDT causes wake-up, this bit is cleared.

SUBFWB	Subtract f from W with borrow								
Syntax:	[label] SUBFWB f [,d [,a]]								
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]								
Operation:	(W) – (f) – ($\overline{\text{C}}$) → dest								
Status Affected:	N, OV, C, DC, Z								
Encoding:	<table border="1"><tr><td>0101</td><td>01da</td><td>ffff</td><td>ffff</td></tr></table>	0101	01da	ffff	ffff				
0101	01da	ffff	ffff						
Description:	Subtract register 'f' and carry flag (borrow) from W (2's complement method). If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>Write to destination</td></tr> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write to destination
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write to destination						

Example 1: SUBFWB REG, 1, 0

Before Instruction

$$\begin{array}{l} \text{REG} = 3 \\ \text{W} = 2 \\ \text{C} = 1 \end{array}$$

After Instruction

$$\begin{array}{l} \text{REG} = \text{FF} \\ \text{W} = 2 \\ \text{C} = 0 \\ \text{Z} = 0 \\ \text{N} = 1 \quad ; \text{result is negative} \end{array}$$

Example 2: SUBFWB REG, 0, 0

Before Instruction

$$\begin{array}{l} \text{REG} = 2 \\ \text{W} = 5 \\ \text{C} = 1 \end{array}$$

After Instruction

$$\begin{array}{l} \text{REG} = 2 \\ \text{W} = 3 \\ \text{C} = 1 \\ \text{Z} = 0 \\ \text{N} = 0 \quad ; \text{result is positive} \end{array}$$

Example 3: SUBFWB REG, 1, 0

Before Instruction

$$\begin{array}{l} \text{REG} = 1 \\ \text{W} = 2 \\ \text{C} = 0 \end{array}$$

After Instruction

$$\begin{array}{l} \text{REG} = 0 \\ \text{W} = 2 \\ \text{C} = 1 \\ \text{Z} = 1 \quad ; \text{result is zero} \\ \text{N} = 0 \end{array}$$

SUBLW	Subtract W from literal								
Syntax:	[label] SUBLW k								
Operands:	0 ≤ k ≤ 255								
Operation:	k – (W) → W								
Status Affected:	N, OV, C, DC, Z								
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>0000</td><td>1000</td><td>kkkk</td><td>kkkk</td></tr> </table>	0000	1000	kkkk	kkkk				
0000	1000	kkkk	kkkk						
Description:	W is subtracted from the eight-bit literal 'k'. The result is placed in W.								
Words:	1								
Cycles:	1								
Q Cycle Activity:									
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 25%;">Q1</th><th style="width: 25%;">Q2</th><th style="width: 25%;">Q3</th><th style="width: 25%;">Q4</th></tr> <tr> <td style="padding: 2px;">Decode</td><td style="padding: 2px;">Read literal 'k'</td><td style="padding: 2px;">Process Data</td><td style="padding: 2px;">Write to W</td></tr> </table>	Q1	Q2	Q3	Q4	Decode	Read literal 'k'	Process Data	Write to W	
Q1	Q2	Q3	Q4						
Decode	Read literal 'k'	Process Data	Write to W						

Example 1: SUBLW 0x02

Before Instruction

W	=	1
C	=	?

After Instruction

W	=	1
C	=	1
Z	=	0
N	=	0

; result is positive

Example 2: SUBLW 0x02

Before Instruction

W	=	2
C	=	?

After Instruction

W	=	0
C	=	1
Z	=	1
N	=	0

; result is zero

Example 3: SUBLW 0x02

Before Instruction

W	=	3
C	=	?

After Instruction

W	=	FF
C	=	0
Z	=	0
N	=	1

; (2's complement)
; result is negative

SUBWF	Subtract W from f								
Syntax:	[label] SUBWF f [,d [,a]]								
Operands:	0 ≤ f ≤ 255								
	d ∈ [0,1]								
	a ∈ [0,1]								
Operation:	(f) – (W) → dest								
Status Affected:	N, OV, C, DC, Z								
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>0101</td><td>11da</td><td>ffff</td><td>ffff</td></tr> </table>	0101	11da	ffff	ffff				
0101	11da	ffff	ffff						
Description:	Subtract W from register 'f' (2's complement method). If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).								
Words:	1								
Cycles:	1								
Q Cycle Activity:									
<table border="1" style="width: 100%; border-collapse: collapse;"> <tr> <th style="width: 25%;">Q1</th><th style="width: 25%;">Q2</th><th style="width: 25%;">Q3</th><th style="width: 25%;">Q4</th></tr> <tr> <td style="padding: 2px;">Decode</td><td style="padding: 2px;">Read register 'f'</td><td style="padding: 2px;">Process Data</td><td style="padding: 2px;">Write to destination</td></tr> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write to destination	
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write to destination						

Example 1: SUBWF REG, 1, 0

Before Instruction

REG	=	3
W	=	2
C	=	?

After Instruction

REG	=	1
W	=	2
C	=	1
Z	=	0
N	=	0

; result is positive

Example 2: SUBWF REG, 0, 0

Before Instruction

REG	=	2
W	=	2
C	=	?

After Instruction

REG	=	2
W	=	0
C	=	1
Z	=	1
N	=	0

; result is zero

Example 3: SUBWF REG, 1, 0

Before Instruction

REG	=	1
W	=	2
C	=	?

After Instruction

REG	=	FFh
W	=	2
C	=	0
Z	=	0
N	=	1

; (2's complement)
; result is negative

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SUBWFB	Subtract W from f with Borrow								
Syntax:	[label] SUBWFB f [,d [,a]]								
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]								
Operation:	(f) – (W) – (C) → dest								
Status Affected:	N, OV, C, DC, Z								
Encoding:	0101 10da ffff ffff								
Description:	Subtract W and the carry flag (borrow) from register 'f' (2's complement method). If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>Write to destination</td></tr> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write to destination
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write to destination						

Example 1: SUBWFB REG, 1, 0

Before Instruction

```
REG = 0x19 (0001 1001)
W = 0x0D (0000 1101)
C = 1
```

After Instruction

```
REG = 0x0C (0000 1011)
W = 0x0D (0000 1101)
C = 1
Z = 0
N = 0 ; result is positive
```

Example 2: SUBWFB REG, 0, 0

Before Instruction

```
REG = 0x1B (0001 1011)
W = 0x1A (0001 1010)
C = 0
```

After Instruction

```
REG = 0x1B (0001 1011)
W = 0x00
C = 1
Z = 1 ; result is zero
N = 0
```

Example 3: SUBWFB REG, 1, 0

Before Instruction

```
REG = 0x03 (0000 0011)
W = 0x0E (0000 1101)
C = 1
```

After Instruction

```
REG = 0xF5 (1111 0100)
; [2's comp]
W = 0x0E (0000 1101)
C = 0
Z = 0
N = 1 ; result is negative
```

SWAPF	Swap f								
Syntax:	[label] SWAPF f [,d [,a]]								
Operands:	0 ≤ f ≤ 255 d ∈ [0,1] a ∈ [0,1]								
Operation:	(f<3:0>) → dest<7:4>, (f<7:4>) → dest<3:0>								
Status Affected:	None								
Encoding:	0011 10da ffff ffff								
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in W. If 'd' is 1, the result is placed in register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>Write to destination</td></tr> </table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write to destination
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write to destination						

Example: SWAPF REG, 1, 0

Before Instruction

```
REG = 0x53
```

After Instruction

```
REG = 0x35
```

TBLRD	Table Read				
Syntax:	[<i>label</i>] TBLRD (*; *+; *-; +*)				
Operands:	None				
Operation:	if TBLRD *, (Prog Mem (TBLPTR)) → TABLAT; TBLPTR - No Change; if TBLRD *+, (Prog Mem (TBLPTR)) → TABLAT; (TBLPTR) +1 → TBLPTR; if TBLRD *-, (Prog Mem (TBLPTR)) → TABLAT; (TBLPTR) -1 → TBLPTR; if TBLRD +*, (TBLPTR) +1 → TBLPTR; (Prog Mem (TBLPTR)) → TABLAT;				
Status Affected:	None				
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>0000</td><td>0000</td><td>0000</td><td>10nn nn=0 * =1 *+ =2 *- =3 +*</td></tr> </table>	0000	0000	0000	10nn nn=0 * =1 *+ =2 *- =3 +*
0000	0000	0000	10nn nn=0 * =1 *+ =2 *- =3 +*		
Description:	<p>This instruction is used to read the contents of Program Memory (P.M.). To address the program memory, a pointer called Table Pointer (TBLPTR) is used. The TBLPTR (a 21-bit pointer) points to each byte in the program memory. TBLPTR has a 2 Mbyte address range.</p> <p style="margin-left: 20px;">TBLPTR[0] = 0: Least Significant Byte of Program Memory Word</p> <p style="margin-left: 20px;">TBLPTR[0] = 1: Most Significant Byte of Program Memory Word</p> <p>The TBLRD instruction can modify the value of TBLPTR as follows:</p> <ul style="list-style-type: none"> • no change • post-increment • post-decrement • pre-increment 				
Words:	1				
Cycles:	2				
Q Cycle Activity:					

Q1	Q2	Q3	Q4
Decode	No operation	No operation	No operation
No operation	No operation (Read Program Memory)	No operation	No operation (Write TABLAT)

TBLRD	Table Read (cont'd)
Example1:	TBLRD *+ ; Before Instruction TABLAT = 0x55 TBLPTR = 0x00A356 MEMORY(0x00A356) = 0x34
	After Instruction TABLAT = 0x34 TBLPTR = 0x00A357
Example2:	TBLRD +* ; Before Instruction TABLAT = 0xAA TBLPTR = 0x01A357 MEMORY(0x01A357) = 0x12 MEMORY(0x01A358) = 0x34
	After Instruction TABLAT = 0x34 TBLPTR = 0x01A358

TBLWT	Table Write				
Syntax:	[<i>label</i>] TBLWT (*; *+; *-; +*)				
Operands:	None				
Operation:	<pre> if TBLWT*, (TABLAT) → Holding Register; TBLPTR - No Change; if TBLWT*+, (TABLAT) → Holding Register; (TBLPTR) +1 → TBLPTR; if TBLWT*-, (TABLAT) → Holding Register; (TBLPTR) -1 → TBLPTR; if TBLWT+*, (TBLPTR) +1 → TBLPTR; (TABLAT) → Holding Register; </pre>				
Status Affected:	None				
Encoding:	<table border="1"> <tr> <td>0000</td> <td>0000</td> <td>0000</td> <td>11nn nn=0 * =1 *+ =2 *- =3 +*</td> </tr> </table>	0000	0000	0000	11nn nn=0 * =1 *+ =2 *- =3 +*
0000	0000	0000	11nn nn=0 * =1 *+ =2 *- =3 +*		
Description:	<p>This instruction uses the 3 LSBs of TBLPTR to determine which of the 8 holding registers the TABLAT is written to. The holding registers are used to program the contents of Program Memory (P.M.). (Refer to Section 5.0 for additional details on programming FLASH memory.)</p> <p>The TBLPTR (a 21-bit pointer) points to each byte in the program memory. TBLPTR has a 2 MByte address range. The LSb of the TBLPTR selects which byte of the program memory location to access.</p> <p style="margin-left: 40px;">TBLPTR[0] = 0: Least Significant Byte of Program Memory Word</p> <p style="margin-left: 40px;">TBLPTR[0] = 1: Most Significant Byte of Program Memory Word</p> <p>The TBLWT instruction can modify the value of TBLPTR as follows:</p> <ul style="list-style-type: none"> • no change • post-increment • post-decrement • pre-increment 				

TBLWT Table Write (Continued)

Words: 1

Cycles: 2

Q Cycle Activity:

Q1	Q2	Q3	Q4
Decode	No operation	No operation	No operation
No operation	No operation (Read TABLAT)	No operation	No operation (Write to Holding Register)

Example1: TBLWT *+;

Before Instruction

TABLAT = 0x55
TBLPTR = 0x00A356
HOLDING REGISTER (0x00A356) = 0xFF

After Instructions (table write completion)

TABLAT = 0x55
TBLPTR = 0x00A357
HOLDING REGISTER (0x00A356) = 0x55

Example 2: TBLWT +*;

Before Instruction

TABLAT = 0x34
TBLPTR = 0x01389A
HOLDING REGISTER (0x01389A) = 0xFF
HOLDING REGISTER (0x01389B) = 0xFF

After Instruction (table write completion)

TABLAT = 0x34
TBLPTR = 0x01389B
HOLDING REGISTER (0x01389A) = 0xFF
HOLDING REGISTER (0x01389B) = 0x34

TSTFSZ	Test f, skip if 0								
Syntax:	[label] TSTFSZ f [.a]								
Operands:	$0 \leq f \leq 255$ $a \in [0,1]$								
Operation:	skip if $f = 0$								
Status Affected:	None								
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>0110</td><td>011a</td><td>ffff</td><td>ffff</td></tr> </table>	0110	011a	ffff	ffff				
0110	011a	ffff	ffff						
Description:	If 'f' = 0, the next instruction, fetched during the current instruction execution, is discarded and a NOP is executed, making this a two-cycle instruction. If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).								
Words:	1								
Cycles:	1(2)								
Note: 3 cycles if skip and followed by a 2-word instruction.									
Q Cycle Activity:									
<table border="1" style="width: 100%; text-align: center;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>No operation</td></tr> </table>		Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	No operation
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	No operation						

If skip:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation

If skip and followed by 2-word instruction:

Q1	Q2	Q3	Q4
No operation	No operation	No operation	No operation
No operation	No operation	No operation	No operation

Example: HERE TSTFSZ CNT, 1
NZERO :
ZERO :

Before Instruction

PC = Address (HERE)

After Instruction

If CNT	=	0x00,
PC	=	Address (ZERO)
If CNT	≠	0x00,
PC	=	Address (NZERO)

XORLW	Exclusive OR literal with W								
Syntax:	[label] XORLW k								
Operands:	$0 \leq k \leq 255$								
Operation:	(W) .XOR. k → W								
Status Affected:	N, Z								
Encoding:	<table border="1" style="display: inline-table; vertical-align: middle;"> <tr><td>0000</td><td>1010</td><td>kkkk</td><td>kkkk</td></tr> </table>	0000	1010	kkkk	kkkk				
0000	1010	kkkk	kkkk						
Description:	The contents of W are XORed with the 8-bit literal 'k'. The result is placed in W.								
Words:	1								
Cycles:	1								
Q Cycle Activity:									
<table border="1" style="width: 100%; text-align: center;"> <tr> <th>Q1</th><th>Q2</th><th>Q3</th><th>Q4</th></tr> <tr> <td>Decode</td><td>Read literal 'k'</td><td>Process Data</td><td>Write to W</td></tr> </table>		Q1	Q2	Q3	Q4	Decode	Read literal 'k'	Process Data	Write to W
Q1	Q2	Q3	Q4						
Decode	Read literal 'k'	Process Data	Write to W						

Example: XORLW 0xAF

Before Instruction

W = 0xB5

After Instruction

W = 0x1A

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XORWF Exclusive OR W with f

Syntax:	[<i>label</i>] XORWF f [,d [,a]								
Operands:	$0 \leq f \leq 255$ $d \in [0,1]$ $a \in [0,1]$								
Operation:	(W) .XOR. (f) \rightarrow dest								
Status Affected:	N, Z								
Encoding:	<table border="1"><tr><td>0001</td><td>10da</td><td>ffff</td><td>ffff</td></tr></table>	0001	10da	ffff	ffff				
0001	10da	ffff	ffff						
Description:	Exclusive OR the contents of W with register 'f'. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in the register 'f' (default). If 'a' is 0, the Access Bank will be selected, overriding the BSR value. If 'a' is 1, then the bank will be selected as per the BSR value (default).								
Words:	1								
Cycles:	1								
Q Cycle Activity:	<table border="1"><tr><td>Q1</td><td>Q2</td><td>Q3</td><td>Q4</td></tr><tr><td>Decode</td><td>Read register 'f'</td><td>Process Data</td><td>Write to destination</td></tr></table>	Q1	Q2	Q3	Q4	Decode	Read register 'f'	Process Data	Write to destination
Q1	Q2	Q3	Q4						
Decode	Read register 'f'	Process Data	Write to destination						

Example: XORWF REG, 1, 0

Before Instruction

REG = 0xAF
W = 0xB5

After Instruction

REG = 0x1A
W = 0xB5

25.0 DEVELOPMENT SUPPORT

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
 - MPASM™ Assembler
 - MPLAB C17 and MPLAB C18 C Compilers
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
- Simulators
 - MPLAB SIM Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - ICEPIC™ In-Circuit Emulator
- In-Circuit Debugger
 - MPLAB ICD
- Device Programmers
 - PRO MATE® II Universal Device Programmer
 - PICSTART® Plus Entry-Level Development
Programmer
- Low Cost Demonstration Boards
 - PICDEM™ 1 Demonstration Board
 - PICDEM 2 Demonstration Board
 - PICDEM 3 Demonstration Board
 - PICDEM 17 Demonstration Board
 - KEELoQ® Demonstration Board

25.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8-bit microcontroller market. The MPLAB IDE is a Windows®-based application that contains:

- An interface to debugging tools
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
 - in-circuit debugger (sold separately)
- A full-featured editor
- A project manager
- Customizable toolbar and key mapping
- A status bar
- On-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or 'C')
- One touch assemble (or compile) and download to PICmicro emulator and simulator tools (automatically updates all project information)
- Debug using:
 - source files
 - absolute listing file
 - machine code

The ability to use MPLAB IDE with multiple debugging tools allows users to easily switch from the cost-effective simulator to a full-featured emulator with minimal retraining.

25.2 MPASM Assembler

The MPASM assembler is a full-featured universal macro assembler for all PICmicro MCU's.

The MPASM assembler has a command line interface and a Windows shell. It can be used as a stand-alone application on a Windows 3.x or greater system, or it can be used through MPLAB IDE. The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, an absolute LST file that contains source lines and generated machine code, and a COD file for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects.
- User-defined macros to streamline assembly code.
- Conditional assembly for multi-purpose source files.
- Directives that allow complete control over the assembly process.

25.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI 'C' compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers, respectively. These compilers provide powerful integration capabilities and ease of use not found with other compilers.

For easier source level debugging, the compilers provide symbol information that is compatible with the MPLAB IDE memory display.

25.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can also link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian is a librarian for pre-compiled code to be used with the MPLINK object linker. When a routine from a library is called from another source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications. The MPLIB object librarian manages the creation and modification of library files.

The MPLINK object linker features include:

- Integration with MPASM assembler and MPLAB C17 and MPLAB C18 C compilers.
- Allows all memory areas to be defined as sections to provide link-time flexibility.

The MPLIB object librarian features include:

- Easier linking because single libraries can be included instead of many smaller files.
- Helps keep code maintainable by grouping related modules together.
- Allows libraries to be created and modules to be added, listed, replaced, deleted or extracted.

25.5 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC-hosted environment by simulating the PICmicro series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user-defined key press, to any of the pins. The execution can be performed in single step, execute until break, or trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and the MPLAB C18 C compilers and the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent multi-project software development tool.

25.6 MPLAB ICE High Performance Universal In-Circuit Emulator with MPLAB IDE

The MPLAB ICE universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers (MCUs). Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment (IDE), which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE in-circuit emulator system has been designed as a real-time emulation system, with advanced features that are generally found on more expensive development tools. The PC platform and Microsoft® Windows environment were chosen to best make these features available to you, the end user.

25.7 ICEPIC In-Circuit Emulator

The ICEPIC low cost, in-circuit emulator is a solution for the Microchip Technology PIC16C5X, PIC16C6X, PIC16C7X and PIC16CXXX families of 8-bit One-Time-Programmable (OTP) microcontrollers. The modular system can support different subsets of PIC16C5X or PIC16CXXX products through the use of interchangeable personality modules, or daughter boards. The emulator is capable of emulating without target application circuitry being present.

25.8 MPLAB ICD In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD, is a powerful, low cost, run-time development tool. This tool is based on the FLASH PICmicro MCUs and can be used to develop for this and other PICmicro microcontrollers. The MPLAB ICD utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming™ protocol, offers cost-effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by watching variables, single-stepping and setting break points. Running at full speed enables testing hardware in real-time.

25.9 PRO MATE II Universal Device Programmer

The PRO MATE II universal device programmer is a full-featured programmer, capable of operating in stand-alone mode, as well as PC-hosted mode. The PRO MATE II device programmer is CE compliant.

The PRO MATE II device programmer has programmable VDD and VPP supplies, which allow it to verify programmed memory at VDD min and VDD max for maximum reliability. It has an LCD display for instructions and error messages, keys to enter commands and a modular detachable socket assembly to support various package types. In stand-alone mode, the PRO MATE II device programmer can read, verify, or program PICmicro devices. It can also set code protection in this mode.

25.10 PICSTART Plus Entry Level Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient.

The PICSTART Plus development programmer supports all PICmicro devices with up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

25.11 PICDEM 1 Low Cost PICmicro Demonstration Board

The PICDEM 1 demonstration board is a simple board which demonstrates the capabilities of several of Microchip's microcontrollers. The microcontrollers supported are: PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The user can program the sample microcontrollers provided with the PICDEM 1 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The user can also connect the PICDEM 1 demonstration board to the MPLAB ICE in-circuit emulator and download the firmware to the emulator for testing. A prototype area is available for the user to build some additional hardware and connect it to the microcontroller socket(s). Some of the features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs connected to PORTB.

25.12 PICDEM 2 Low Cost PIC16CXX Demonstration Board

The PICDEM 2 demonstration board is a simple demonstration board that supports the PIC16C62, PIC16C64, PIC16C65, PIC16C73 and PIC16C74 microcontrollers. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 2 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area has been provided to the user for adding additional hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a serial EEPROM to demonstrate usage of the I²C™ bus and separate headers for connection to an LCD module and a keypad.

25.13 PICDEM 3 Low Cost PIC16CXXX Demonstration Board

The PICDEM 3 demonstration board is a simple demonstration board that supports the PIC16C923 and PIC16C924 in the PLCC package. It will also support future 44-pin PLCC microcontrollers with an LCD Module. All the necessary hardware and software is included to run the basic demonstration programs. The user can program the sample microcontrollers provided with the PICDEM 3 demonstration board on a PRO MATE II device programmer, or a PICSTART Plus development programmer with an adapter socket, and easily test firmware. The MPLAB ICE in-circuit emulator may also be used with the PICDEM 3 demonstration board to test firmware. A prototype area has been provided to the user for adding hardware and connecting it to the microcontroller socket(s). Some of the features include a RS-232 interface, push button switches, a potentiometer for simulated analog input, a thermistor and separate headers for connection to an external LCD module and a keypad. Also provided on the PICDEM 3 demonstration board is a LCD panel, with 4 commons and 12 segments, that is capable of displaying time, temperature and day of the week. The PICDEM 3 demonstration board provides an additional RS-232 interface and Windows software for showing the demultiplexed LCD signals on a PC. A simple serial interface allows the user to construct a hardware demultiplexer for the LCD signals.

25.14 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. All necessary hardware is included to run basic demo programs, which are supplied on a 3.5-inch disk. A programmed sample is included and the user may erase it and program it with the other sample programs using the PRO MATE II device programmer, or the PICSTART Plus development programmer, and easily debug and test the sample code. In addition, the PICDEM 17 demonstration board supports downloading of programs to and executing out of external FLASH memory on board. The PICDEM 17 demonstration board is also usable with the MPLAB ICE in-circuit emulator, or the PICMASTER emulator and all of the sample programs can be run and modified using either emulator. Additionally, a generous prototype area is available for user hardware.

25.15 KEELOQ Evaluation and Programming Tools

KEELOQ evaluation and programming tools support Microchip's HCS Secure Data Products. The HCS evaluation kit includes a LCD display to show changing codes, a decoder to decode transmissions and a programming interface to program test transmitters.

TABLE 25-1: DEVELOPMENT TOOLS FROM MICROCHIP

	MPLAB® Integrated Development Environment	MPLAB® C17 C Compiler	MPLAB® C18 C Compiler	MPSIM™ Assembler/ MPLINK™ Object Linker	MPLAB® ICE In-Circuit Emulator	ICEPIC™ In-Circuit Emulator	MPLAB® ICD In-Circuit Debugger	Programmers	Emulators	Debuggers	Software Tools	Demo Boards and Eval Kits
MCP2510												
MCRFXX												
HCSXXX												
24CXX/ 25CXX/ 93CXX												
PIC18FXX	✓											
PIC18CXX2	✓	✓										
PIC17C7XX	✓	✓	✓									
PIC17C4X	✓	✓	✓									
PIC16C9XX	✓	✓										
PIC16F8XX	✓	✓										
PIC16C8X	✓	✓										
PIC16C7XX	✓	✓										
PIC16C7X	✓	✓										
PIC16F62X	✓	✓										
PIC16CXXX	✓	✓										
PIC16C6X	✓	✓										
PIC16C5X	✓	✓										
PIC14000	✓											
PIC12CXXX	✓											

* Contact the Microchip Technology Inc. web site at www.microchip.com for information on how to use the MPLAB® ICD In-Circuit Debugger (DV164001) with PIC16C62, 63, 64, 65, 72, 73, 74, 76, 77.

** Contact Microchip Technology Inc. for availability date.
† Development tool is available on select devices.

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NOTES:

26.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings ^(†)

Ambient temperature under bias.....	-55°C to +125°C
Storage temperature	-65°C to +150°C
Voltage on any pin with respect to Vss (except VDD, MCLR, and RA4)	0.3V to (VDD + 0.3V)
Voltage on VDD with respect to Vss	-0.3V to +5.5V
Voltage on MCLR with respect to Vss (Note 2)	0V to +13.25V
Voltage on RA4 with respect to Vss	0V to +12.0V
Total power dissipation (Note 1)	1.0W
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD}).....	±20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD}).....	±20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin.....	25 mA
Maximum current sunk by all ports.....	200 mA
Maximum current sourced by all ports.....	200 mA

Note 1: Power dissipation is calculated as follows:

$$P_{dis} = V_{DD} \times \{I_{DD} - \sum I_{OH}\} + \sum \{(V_{DD}-V_{OH}) \times I_{OH}\} + \sum (V_{OL} \times I_{OL})$$

2: Voltage spikes below V_{SS} at the MCLR/VPP pin, inducing currents greater than 80 mA, may cause latchup. Thus, a series resistor of 50-100Ω should be used when applying a “low” level to the MCLR/VPP pin, rather than pulling this pin directly to V_{SS}.

[†] NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

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FIGURE 26-1: PIC18FXX20 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)

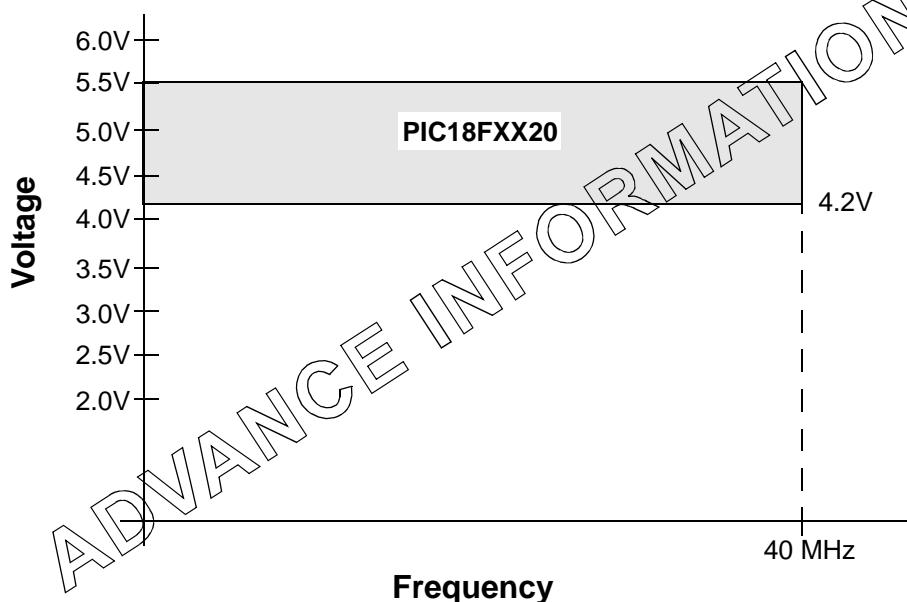
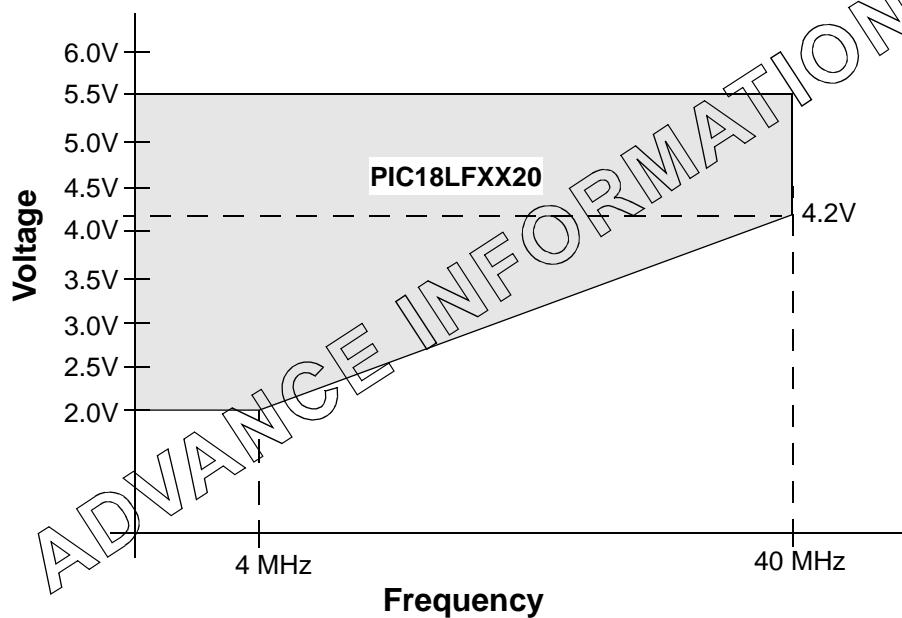


FIGURE 26-2: PIC18LFXX20 VOLTAGE-FREQUENCY GRAPH (INDUSTRIAL)



$$F_{MAX} = (16.36 \text{ MHz/V}) (V_{DDAPPMIN} - 2.0V) + 4 \text{ MHz}$$

Note: $V_{DDAPPMIN}$ is the minimum voltage of the PICmicro® device in the application.

26.1 DC Characteristics: PIC18FXX20 (Industrial, Extended) PIC18LFXX20 (Industrial)

PIC18LFXX20 (Industrial)			Standard Operating Conditions (unless otherwise stated)				
PIC18FXX20 (Industrial, Extended)			Standard Operating Conditions (unless otherwise stated)				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
D001	VDD	Supply Voltage					
		PIC18LFXX20	2.0	—	5.5	V	XT, RC and LP osc mode
D001		PIC18FXX20	4.2	—	5.5	V	
D002	VDR	RAM Data Retention Voltage⁽¹⁾	1.5	—	—	V	
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	—	0.7	V	See section on Power-on Reset for details
D004	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05	—	—	V/ms	See section on Power-on Reset for details
D005	VBOR	Brown-out Reset Voltage					
		PIC18LFXX20					
		BORV1:BORV0 = 11	2.0	—	2.16	V	
		BORV1:BORV0 = 10	2.7	—	2.86	V	
		BORV1:BORV0 = 01	4.2	—	4.46	V	
		BORV1:BORV0 = 00	4.5	—	4.78	V	
D005		PIC18FXX20					
		BORV1:BORV0 = 1x	N.A.	—	N.A.	V	Not in operating voltage range of device
		BORV1:BORV0 = 01	4.2	—	4.46	V	
		BORV1:BORV0 = 00	4.5	—	4.78	V	

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode, or during a device RESET, without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD
MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or Vss, and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR,...).

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula $I_r = VDD/2REXT$ (mA) with REXT in kOhm.

PIC18FXX20

26.1 DC Characteristics: PIC18FXX20 (Industrial, Extended) PIC18LFXX20 (Industrial) (Continued)

PIC18LFXX20 (Industrial)			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial				
PIC18FXX20 (Industrial, Extended)			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for extended				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
D010	IDD	Supply Current ^(2,4)					
		PIC18LFXX20	—	.068	2	mA	XT, RC, RCIO osc configurations Fosc = 4 MHz, Vdd = 2.0V
		PIC18FXX20	—	.4	4	mA	XT, RC, RCIO osc configurations Fosc = 4 MHz, Vdd = 4.2V
		PIC18LFXX20	—	28	55	μA	LP osc configuration Fosc = 32 kHz, Vdd = 2.0V
		PIC18FXX20	—	88	250	μA	LP osc configuration Fosc = 32 kHz, Vdd = 4.2V
		PIC18LFXX20	—	—	38	mA	EC, ECIO osc configurations Fosc = 40 MHz, Vdd = 5.5V
		PIC18FXX20	—	—	38	mA	EC, ECIO osc configurations Fosc = 40 MHz, Vdd = 5.5V
		PIC18LFXX20	—	1.32	3.5	mA	HS osc configuration Fosc = 6 MHz, Vdd = 2.0V
			—	13.46	25	mA	Fosc = 25 MHz, Vdd = 5.5V
			—	19.1	38	mA	HS + PLL osc configurations Fosc = 10 MHz, Vdd = 5.5V
D013		PIC18FXX20	—	13.46	25	mA	HS osc configuration Fosc = 25 MHz, Vdd = 5.5V
			—	19.1	38	mA	HS + PLL osc configurations Fosc = 10 MHz, Vdd = 5.5V
D014		PIC18LFXX20	—	29.6	55	μA	Timer1 osc configuration Fosc = 32 kHz, Vdd = 2.0V
D014		PIC18FXX20	—	—	200	μA	OSCB osc configuration Fosc = 32 kHz, Vdd = 4.2V, $-40^{\circ}\text{C} \text{ to } +85^{\circ}\text{C}$
			—	—	250	μA	Fosc = 32 kHz, Vdd = 4.2V, $-40^{\circ}\text{C} \text{ to } +125^{\circ}\text{C}$

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which Vdd can be lowered in SLEEP mode, or during a device RESET, without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to Vdd
MCLR = Vdd; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to Vdd or Vss, and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR,...).

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula $I_r = Vdd/2REXT$ (mA) with REXT in kOhm.

26.1 DC Characteristics: PIC18FXX20 (Industrial, Extended) PIC18LFXX20 (Industrial) (Continued)

PIC18LFXX20 (Industrial)			Standard Operating Conditions (unless otherwise stated)				
PIC18FXX20 (Industrial, Extended)			Standard Operating Conditions (unless otherwise stated)				
Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
D020	IPD	Power-down Current⁽³⁾					
		PIC18LFXX20	—	.09	2	μA	VDD = 2.0V, -40°C to +85°C
D020		PIC18FXX20	—	.11	4	μA	VDD = 5.5V, -40°C to +85°C
		PIC18FXX20	—	.1	3	μA	VDD = 4.2V, -40°C to +85°C
D021B		PIC18FXX20	—	.11	4	μA	VDD = 5.5V, -40°C to +85°C
		PIC18FXX20	—	.1	15	μA	VDD = 4.2V, -40°C to +125°C
—	—	PIC18FXX20	—	.11	20	μA	VDD = 5.5V, -40°C to +125°C
D022	ΔI _{WDT}	Module Differential Current					
		Watchdog Timer PIC18LFXX20	—	—	1	μA	VDD = 2.0V
D022		Watchdog Timer PIC18FXX20	—	—	15	μA	VDD = 5.5V, -40°C to +85°C
		PIC18FXX20	—	—	20	μA	VDD = 5.5V, -40°C to +125°C
D022A	ΔI _{BOR}	Brown-out Reset PIC18LFXX20	—	—	45	μA	VDD = 5.5V
D022A		Brown-out Reset PIC18FXX20	—	—	50	μA	VDD = 5.5V, -40°C to +85°C
D022A		PIC18FXX20	—	—	50	μA	VDD = 5.5V, -40°C to +125°C
D022B	ΔI _{LVD}	Low Voltage Detect PIC18LFXX20	—	—	45	μA	VDD = 2.0V
D022B		PIC18FXX20	—	—	40	μA	VDD = 4.2V, -40°C to +85°C
D022B		PIC18FXX20	—	—	50	μA	VDD = 4.2V, -40°C to +125°C
D025	ΔI _{OSCB}	Timer1 Oscillator PIC18LFXX20	—	—	15	μA	VDD = 2.0V
D025		PIC18FXX20	—	—	100	μA	VDD = 4.2V, -40°C to +85°C
D025		PIC18FXX20	—	—	120	μA	VDD = 4.2V, -40°C to +125°C

Legend: Shading of rows is to assist in readability of the table.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode, or during a device RESET, without losing RAM data.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors, such as I/O pin loading and switching rate, oscillator type, internal code execution pattern and temperature, also have an impact on the current consumption.

The test conditions for all IDD measurements in active operation mode are:

OSC1 = external square wave, from rail-to-rail; all I/O pins tri-stated, pulled to VDD
MCLR = VDD; WDT enabled/disabled as specified.

3: The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to VDD or VSS, and all features that add delta current disabled (such as WDT, Timer1 Oscillator, BOR,...).

4: For RC osc configuration, current through REXT is not included. The current through the resistor can be estimated by the formula $I_R = VDD/2REXT$ (mA) with REXT in kOhm.

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26.2 DC Characteristics: PIC18FXX20 (Industrial, Extended) PIC18LFXXX20 (Industrial)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for extended			
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
D030 D030A D031 D032 D032A D033	VIL	Input Low Voltage I/O ports: with TTL buffer	Vss	0.15VDD		
			—	0.8		
		with Schmitt Trigger buffer RC3 and RC4	Vss	0.2VDD		
		MCLR	Vss	0.3VDD		
		OSC1 (in XT, HS and LP modes) and T1OSI	Vss	0.2VDD		
		OSC1 (in RC and EC mode) ⁽¹⁾	Vss	0.3VDD		
D040 D040A D041 D042 D042A D043	VIH	Input High Voltage I/O ports: with TTL buffer	0.25VDD + 0.8V	VDD	V	VDD < 4.5V
			2.0	VDD	V	4.5V ≤ VDD ≤ 5.5V
		with Schmitt Trigger buffer RC3 and RC4	0.8VDD	VDD	V	
		MCLR, OSC1 (EC mode)	0.7VDD	VDD	V	
		OSC1 (in XT, HS and LP modes) and T1OSI	0.8VDD	VDD	V	
		OSC1 (RC mode) ⁽¹⁾	0.7VDD	VDD	V	
D060 D061 D063	IIL	Input Leakage Current ^(2,3) I/O ports	—	±1	µA	Vss ≤ VPIN ≤ VDD, Pin at hi-impedance
		MCLR	—	±5	µA	Vss ≤ VPIN ≤ VDD
		OSC1	—	±5	µA	Vss ≤ VPIN ≤ VDD
D070	IPU IPURB	Weak Pull-up Current PORTB weak pull-up current	50	400	µA	VDD = 5V, VPIN = Vss

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PICmicro device be driven with an external clock while in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: Parameter is characterized but not tested.

26.2 DC Characteristics: PIC18FXX20 (Industrial, Extended) PIC18LFXX20 (Industrial) (Continued)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)			
Param No.	Symbol	Characteristic	Min	Max	Units	Conditions
D080	VOL	Output Low Voltage I/O ports	—	0.6	V	$I_{OL} = 8.5 \text{ mA}$, $VDD = 4.5\text{V}$, -40°C to $+85^\circ\text{C}$
			—	0.6	V	$I_{OL} = 7.0 \text{ mA}$, $VDD = 4.5\text{V}$, -40°C to $+125^\circ\text{C}$
		OSC2/CLKOUT (RC mode)	—	0.6	V	$I_{OL} = 1.6 \text{ mA}$, $VDD = 4.5\text{V}$, -40°C to $+85^\circ\text{C}$
			—	0.6	V	$I_{OL} = 1.2 \text{ mA}$, $VDD = 4.5\text{V}$, -40°C to $+125^\circ\text{C}$
D090	VOH	Output High Voltage⁽³⁾ I/O ports	—	—	V	$I_{OH} = -3.0 \text{ mA}$, $VDD = 4.5\text{V}$, -40°C to $+85^\circ\text{C}$
			—	—	V	$I_{OH} = -2.5 \text{ mA}$, $VDD = 4.5\text{V}$, -40°C to $+125^\circ\text{C}$
		OSC2/CLKOUT (RC mode)	—	—	V	$I_{OH} = -1.3 \text{ mA}$, $VDD = 4.5\text{V}$, -40°C to $+85^\circ\text{C}$
			—	—	V	$I_{OH} = -1.0 \text{ mA}$, $VDD = 4.5\text{V}$, -40°C to $+125^\circ\text{C}$
D150	VOD	Open Drain High Voltage	—	8.5	V	RA4 pin
D100 ⁽⁴⁾	CosC2	Capacitive Loading Specs on Output Pins OSC2 pin	—	15	pF	In XT, HS and LP modes when external clock is used to drive OSC1
			—	50	pF	To meet the AC Timing Specifications
D101	CIO	All I/O pins and OSC2 (in RC mode)	—	400	pF	In I ² C mode
D102	CB	SCL, SDA	—	—	—	—

Note 1: In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended that the PICmicro device be driven with an external clock while in RC mode.

2: The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.

3: Negative current is defined as current sourced by the pin.

4: Parameter is characterized but not tested.

PIC18FXX20

TABLE 26-1: COMPARATOR SPECIFICATIONS

Operating Conditions: $3.0V < VDD < 5.5V$, $-40^{\circ}C < TA < +125^{\circ}C$, unless otherwise stated							
Param No.	Characteristics	Sym	Min	Typ	Max	Units	Comments
D300	Input Offset Voltage	V _{IOFF}	—	± 5.0	± 10	mV	
D301	Input Common Mode Voltage	V _{ICM}	0	-	$VDD - 1.5$	V	
D302	Common Mode Rejection Ratio	CMRR	55	-	—	dB	
300 300A	Response Time ⁽¹⁾	T _{RESP}	—	150	400	ns	PIC18FXX20
301	Comparator Mode Change to Output Valid	T _{M2OV}	—	—	600	ns	PIC18LFXX20
					10	μs	

Note 1: Response time measured with one comparator input at $(VDD - 1.5)/2$ while the other input transitions from V_{SS} to V_{DD}.

TABLE 26-2: VOLTAGE REFERENCE SPECIFICATIONS

Operating Conditions: $3.0V < VDD < 5.5V$, $-40^{\circ}C < TA < +125^{\circ}C$, unless otherwise stated							
Spec No.	Characteristics	Sym	Min	Typ	Max	Units	Comments
D310	Resolution	V _{RES}	$VDD/24$	—	$VDD/32$	LSb	
D311	Absolute Accuracy	V _{RAA}	— —	— —	1/4 1/2	LSb LSb	Low Range (VRR = '1') High Range (VRR = '0')
D312	Unit Resistor Value (R)	V _{RUR}	—	2k	—	Ω	
310	Settling Time ⁽¹⁾	T _{SET}	—	—	10	μs	

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.

FIGURE 26-3: LOW VOLTAGE DETECT CHARACTERISTICS

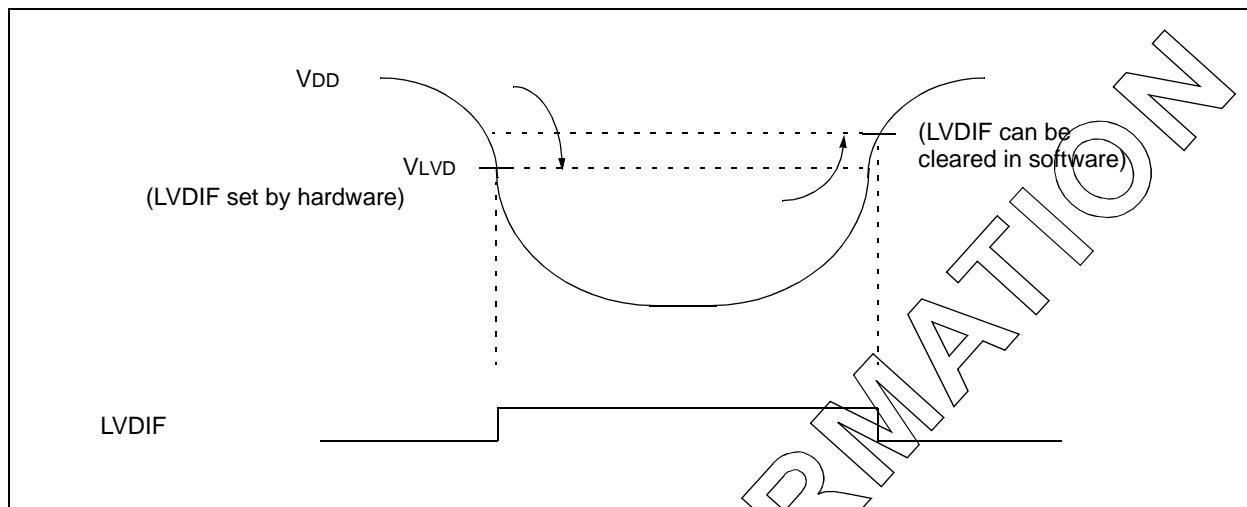


TABLE 26-3: LOW VOLTAGE DETECT CHARACTERISTICS

Standard Operating Conditions (unless otherwise stated)					
Operating temperature $-40^{\circ}\text{C} \leq TA \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq TA \leq +125^{\circ}\text{C}$ for extended					
Param No.	Symbol	Characteristic	Min	Typ†	Max
D420		LVD Voltage on V_{DD} transition high to low	$LVV = 0000$	1.8	1.86
			$LVV = 0001$	2.0	2.06
			$LVV = 0010$	2.2	2.27
			$LVV = 0011$	2.4	2.47
			$LVV = 0100$	2.5	2.58
			$LVV = 0101$	2.7	2.78
			$LVV = 0110$	2.8	2.89
			$LVV = 0111$	3.0	3.1
			$LVV = 1000$	3.3	3.41
			$LVV = 1001$	3.5	3.61
			$LVV = 1010$	3.6	3.72
			$LVV = 1011$	3.8	3.92
			$LVV = 1100$	4.0	4.13
			$LVV = 1101$	4.2	4.33
			$LVV = 1110$	4.5	4.64
D423	VBG	Bandgap Reference Voltage Value	—	1.22	—
Units					
Conditions					

† Production tested at $T_{AMB} = 25^{\circ}\text{C}$. Specifications over temp. limits ensured by characterization.

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TABLE 26-4: MEMORY PROGRAMMING REQUIREMENTS

DC Characteristics			Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D110	VPP	Internal Program Memory Programming Specifications (Note 1) Voltage on <u>MCLR/VPP</u> pin	9.00	—	13.25	V	(Note 2)
D112	I _{PP}	Current into <u>MCLR/VPP</u> pin	—	—	5	μA	
D113	I _{DDP}	Supply Current during Programming	—	—	10	mA	
D120	E _D	Data EEPROM Memory Cell Endurance	100K	1M	—	E/W	-40°C to $+85^{\circ}\text{C}$
D120A	E _D	Cell Endurance	10K	100K	—	E/W	$+85^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
D121	V _{DRW}	V _{DD} for Read/Write	V _{MIN}	—	5.5	V	Using EECON to read/write V _{MIN} = Minimum operating voltage
D122	T _{DEW}	Erase/Write Cycle Time	—	4	—	ms	
D130	E _P	Program FLASH Memory Cell Endurance	10K	100K	—	E/W	-40°C to $+85^{\circ}\text{C}$
D130A	E _P	Cell Endurance	1000	10K	—	E/W	$+85^{\circ}\text{C}$ to $+125^{\circ}\text{C}$
D131	V _{PR}	V _{DD} for Read	V _{MIN}	—	5.5	V	V _{MIN} = Minimum operating voltage
D132	V _{IE}	V _{DD} for Block Erase	4.5	—	5.5	V	Using ICSP port
D132A	V _{IW}	V _{DD} for Externally Timed Erase or Write	4.5	—	5.5	V	Using ICSP port
D132B	V _{PEW}	V _{DD} for Self-timed Write	V _{MIN}	—	5.5	V	V _{MIN} = Minimum operating voltage
D133	T _{IE}	ICSP Block Erase Cycle Time	—	5	—	ms	V _{DD} > 4.5V
D133A	T _{IW}	ICSP Erase or Write Cycle Time (externally timed)	1	—	—	ms	V _{DD} > 4.5V
D133A	T _{IW}	Self-timed Write Cycle Time	—	2.5	—	ms	

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: These specifications are for programming the on-chip program memory through the use of Table Write instructions.

2: The pin may be kept in this range at times other than programming, but it is not recommended.

26.3 AC (Timing) Characteristics

26.3.1 TIMING PARAMETER SYMOLOGY

The timing parameter symbols have been created following one of the following formats:

1. TppS2ppS

3. Tcc:ST (I^2C specifications only)

2. TppS

4. Ts (I^2C specifications only)

T		T	Time
F	Frequency		

Lowercase letters (pp) and their meanings:

pp			
cc	CCP1	osc	OSC1
ck	CLKOUT	rd	\overline{RD}
cs	\overline{CS}	rw	\overline{RD} or \overline{WR}
di	SDI	sc	SCK
do	SDO	ss	\overline{SS}
dt	Data in	t0	T0CKI
io	I/O port	t1	T1CKI
mc	MCLR	wr	\overline{WR}

Uppercase letters and their meanings:

S		P	Period
F	Fall	R	Rise
H	High	V	Valid
I	Invalid (Hi-impedance)	Z	Hi-impedance
L	Low	High	High
I^2C only		Low	Low
AA	output access		
BUF	Bus free		

Tcc:ST (I^2C specifications only)

CC		SU	Setup
HD	Hold		
ST		STO	STOP condition
DAT	DATA input hold		
STA	START condition		

PIC18FXX20

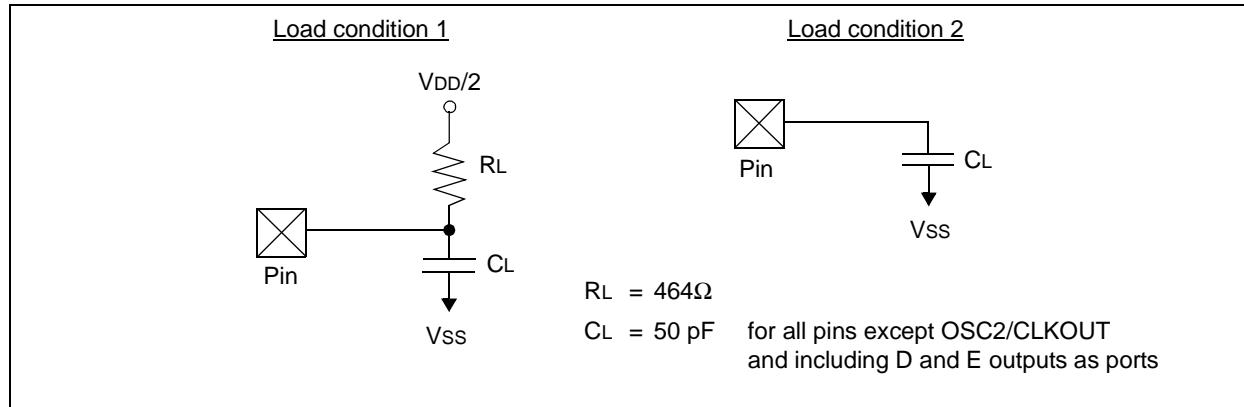
26.3.2 TIMING CONDITIONS

The temperature and voltages specified in Table 26-5 apply to all timing specifications, unless otherwise noted. Figure 26-4 specifies the load conditions for the timing specifications.

TABLE 26-5: TEMPERATURE AND VOLTAGE SPECIFICATIONS - AC

AC CHARACTERISTICS	Standard Operating Conditions (unless otherwise stated)	
	Operating temperature	-40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended
Operating voltage VDD range as described in DC spec Section 26.1 and Section 26.2. LC parts operate for industrial temperatures only.		

FIGURE 26-4: LOAD CONDITIONS FOR DEVICE TIMING SPECIFICATIONS



26.3.3 TIMING DIAGRAMS AND SPECIFICATIONS

FIGURE 26-5: EXTERNAL CLOCK TIMING (ALL MODES EXCEPT PLL)

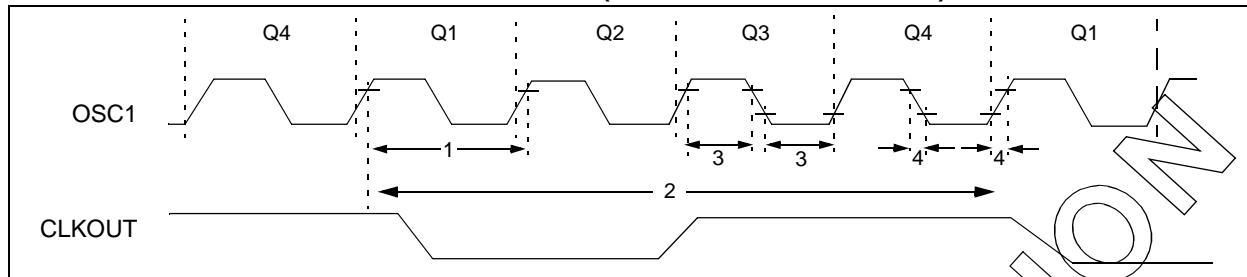


TABLE 26-6: EXTERNAL CLOCK TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
1A	Fosc	External CLKIN Frequency ⁽¹⁾ Oscillator Frequency ⁽¹⁾	DC DC 0.1 4 4 5	40 4 4 25 10 200	MHz MHz MHz MHz MHz kHz	EC, ECIO RC osc XT osc HS osc HS + PLL osc LP osc mode
1	Tosc	External CLKIN Period ⁽¹⁾ Oscillator Period ⁽¹⁾	28 250 250 25 25 25	— — — 10,000 250 250	ns ns ns ns ns μs	EC, ECIO RC osc XT osc HS osc HS + PLL osc LP osc
2	Tcy	Instruction Cycle Time ⁽¹⁾	100	—	ns	Tcy = 4/Fosc
3	TosL, TosH	External Clock in (OSC1) High or Low Time	30 2.5 10	— — —	ns μs ns	XT osc LP osc HS osc
4	TosR, TosF	External Clock in (OSC1) Rise or Fall Time	— — —	20 50 7.5	ns ns ns	XT osc LP osc HS osc

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period for all configurations except PLL. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at "min." values with an external clock applied to the OSC1/CLKIN pin. When an external clock input is used, the "max." cycle time limit is "DC" (no clock) for all devices.

TABLE 26-7: PLL CLOCK TIMING SPECIFICATIONS (VDD = 4.2 TO 5.5V)

Param. No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
—	Fosc	Oscillator Frequency Range	4	—	10	MHz	HS mode
—	Fsys	On-chip VCO System Frequency	16	—	40	MHz	HS mode
—	t _{rc}	PLL Start-up Time (Lock Time)	—	—	2	ms	
—	ΔCLK	CLKOUT Stability (Jitter)	-2	—	+2	%	

† Data in "Typ" column is at 5V, 25°C, unless otherwise stated. These parameters are for design guidance only and are not tested.

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FIGURE 26-6: CLKOUT AND I/O TIMING

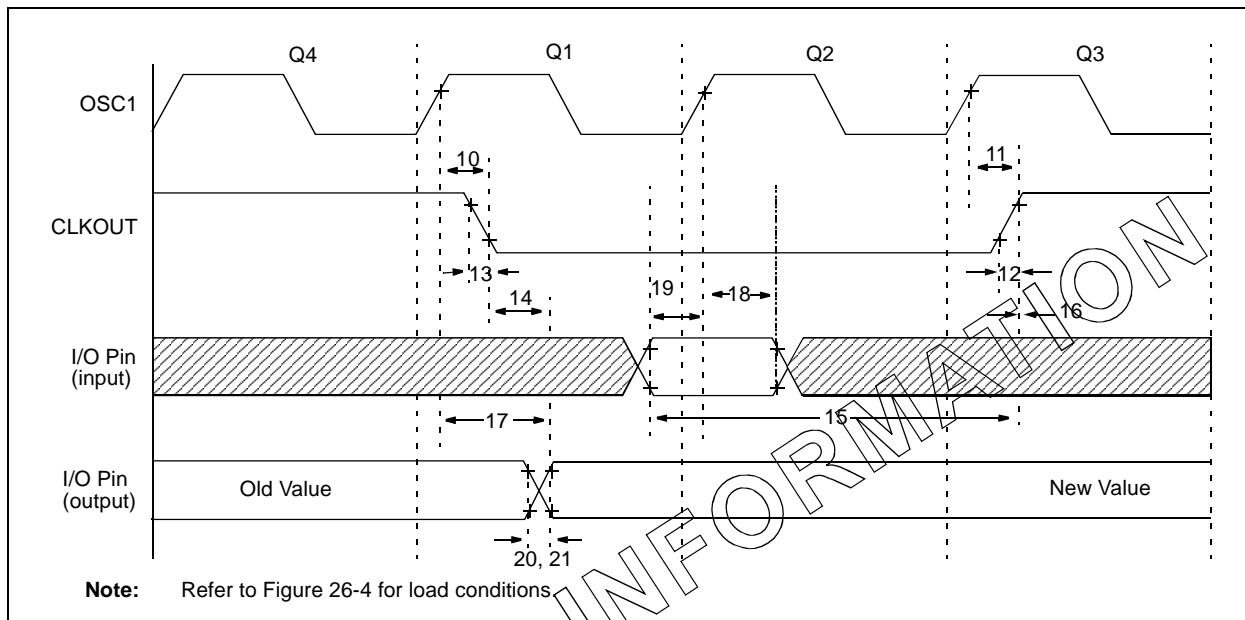


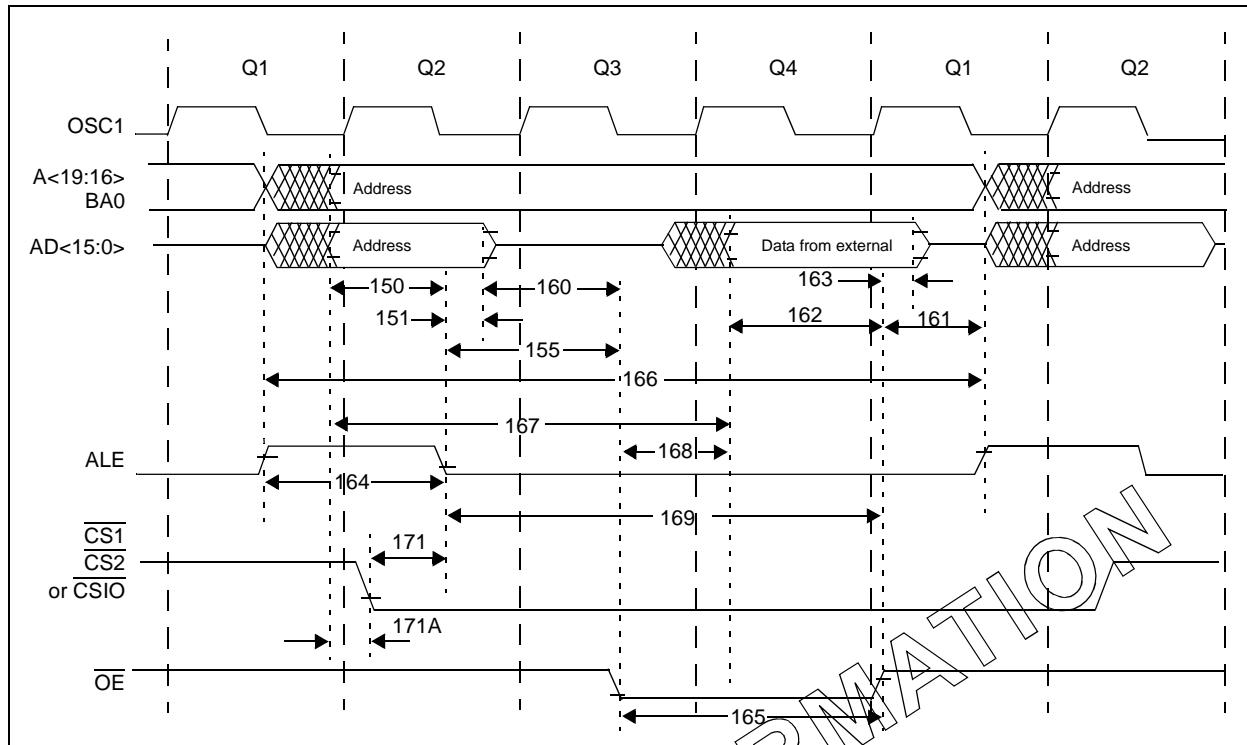
TABLE 26-8: CLKOUT AND I/O TIMING REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
10	TosH2ckL	OSC1↑ to CLKOUT↓	—	75	200	ns	(1)
11	TosH2ckH	OSC1↑ to CLKOUT↑	—	75	200	ns	(1)
12	TckR	CLKOUT rise time	—	35	100	ns	(1)
13	TdkF	CLKOUT fall time	—	35	100	ns	(1)
14	TckL2ioV	CLKOUT↓ to Port out valid	—	—	0.5Tcy + 20	ns	(1)
15	TioV2ckH	Port in valid before CLKOUT↑	0.25Tcy + 25	—	—	ns	(1)
16	TckH2iol	Port in hold after CLKOUT↑	0	—	—	ns	(1)
17	TosH2ioV	OSC1↑ (Q1 cycle) to Port out valid	—	50	150	ns	
18	TosH2iol	OSC1↑ (Q2 cycle) to PIC18FXX20	100	—	—	ns	
18A		Port input invalid (I/O in hold time)	200	—	—	ns	
19	TioV2osH	Port input valid to OSC1↑ (I/O in setup time)	0	—	—	ns	
20	TioR	Port output rise time	PIC18FXX20	—	10	25	ns
20A			PIC18LFXX20	—	—	60	ns
21	TioF	Port output fall time	PIC18FXX20	—	10	25	ns
21A			PIC18LFXX20	—	—	60	ns
22††	TINP	INT pin high or low time	Tcy	—	—	ns	
23††	TRBP	RB7:RB4 change INT high or low time	Tcy	—	—	ns	
24††	TRCP	RC7:RC4 change INT high or low time	20	—	—	ns	

†† These parameters are asynchronous events not related to any internal clock edges.

Note 1: Measurements are taken in RC mode, where CLKOUT output is 4 x Tosc.

FIGURE 26-7: PROGRAM MEMORY READ TIMING DIAGRAM



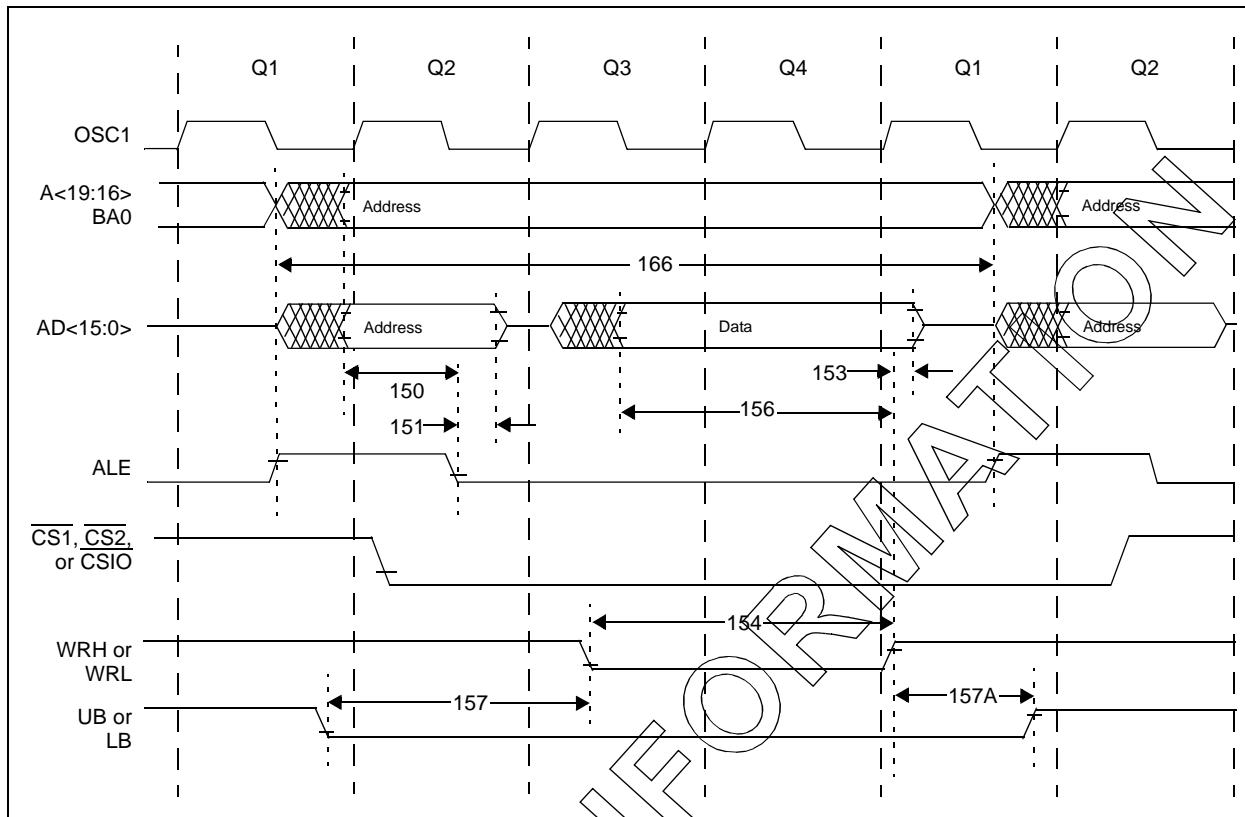
Operating Conditions: $2.0V < V_{CC} < 5.5V$, $-40^{\circ}C < TA < 125^{\circ}C$ unless otherwise stated.

TABLE 26-9: CLKOUT AND I/O TIMING REQUIREMENTS

Param. No	Symbol	Characteristics	Min	Typ	Max	Units
150	TadV2all	Address out valid to ALE ↓ (address setup time)	0.25TCY-10	—	—	ns
151	TalL2adL	ALE ↓ to address out invalid (address hold time)	5	—	—	ns
155	TalL2oeL	ALE ↓ to OE ↓	10	0.125TCY	—	ns
160	TadZ2oeL	AD high-Z to OE ↓ (bus release to OE)	0	—	—	ns
161	ToeH2adD	OE ↑ to AD driven	0.125TCY-5	—	—	ns
162	TadV2oeH	LS Data valid before OE ↑ (data setup time)	20	—	—	ns
163	ToeH2adL	OE ↑ to data in invalid (data hold time)	0	—	—	ns
164	TalH2all	ALE pulse width	—	TCY	—	ns
165	ToeL2oeH	OE pulse width	0.5TCY-5	0.5TCY	—	ns
166	TalH2alH	ALE ↑ to ALE ↑ (cycle time)	—	0.25TCY	—	ns
167	Tacc	Address valid to data valid	0.75TCY-25	—	—	ns
168	Toe	OE ↓ to data valid	—	—	0.5TCY-25	ns
169	TalL2oeH	ALE ↓ to OE ↑	0.625TCY-10	—	0.625TCY+10	ns
171	TalH2csL	Chip select active to ALE ↓	0.25TCY-20	—	—	ns
171A	TubL2oeH	AD valid to chip select active	—	—	10	ns

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FIGURE 26-8: PROGRAM MEMORY WRITE TIMING DIAGRAM



Operating Conditions: $2.0V < V_{CC} < 5.5V$, $-40^{\circ}C < T_A < 125^{\circ}C$ unless otherwise stated.

TABLE 26-10: PROGRAM MEMORY WRITE TIMING REQUIREMENTS

Param. No	Symbol	Characteristics	Min	Typ	Max	Units
150	TadV2all	Address out valid to ALE ↓ (address setup time)	0.25TCY-10	—	—	ns
151	Tail2adl	ALE ↓ to address out invalid (address hold time)	5	—	—	ns
153	TwrH2adl	WRn ↑ to data out invalid (data hold time)	5	—	—	ns
154	TwrL	WRn pulse width	0.5TCY-5	0.5TCY	—	ns
156	TadV2wrH	Data valid before WRn ↑ (data setup time)	0.5TCY-10	—	—	ns
157	TbsV2wrl	Byte select valid before WRn ↓ (byte select setup time)	0.25TCY	—	—	ns
157A	TwrH2bsl	WRn ↑ to byte select invalid (byte select hold time)	0.125TCY-5	—	—	ns
166	TalH2alH	ALE ↑ to ALE ↑ (cycle time)	—	0.25TCY	—	ns
36	TIVRST	Time for Internal Reference Voltage to become stable	—	20	50	μs

FIGURE 26-9: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

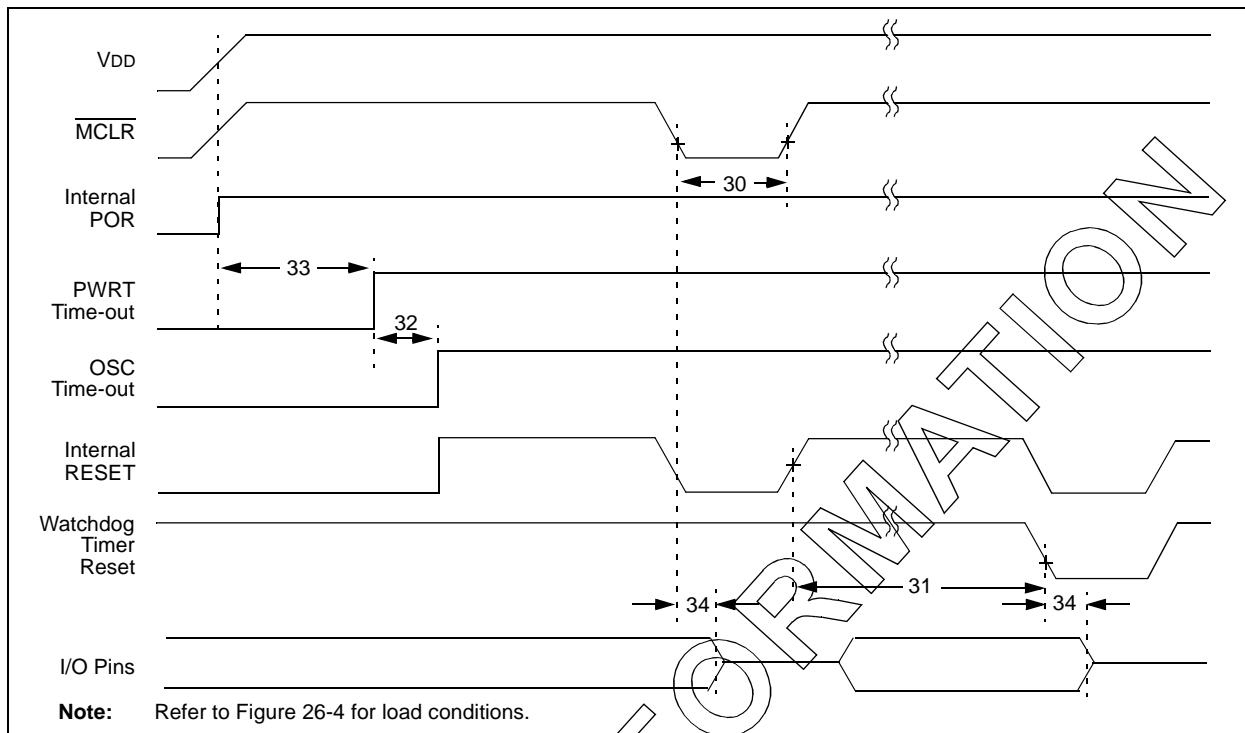


FIGURE 26-10: BROWN-OUT RESET TIMING

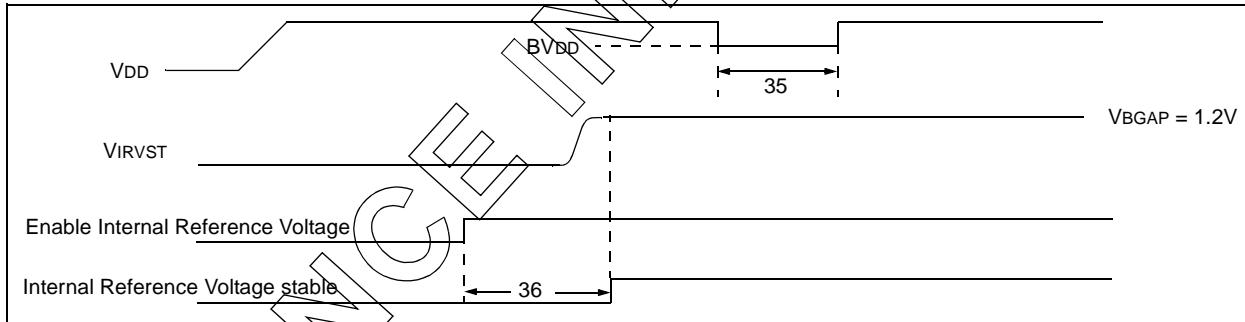


TABLE 26-11: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER AND BROWN-OUT RESET REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
30	T _{mcl}	MCLR Pulse Width (low)	2	—	—	μs	
31	T _{WDT}	Watchdog Timer Time-out Period (No Postscaler)	7	18	33	ms	
32	T _{OSS}	Oscillation Start-up Timer Period	1024T _{OSSC}	—	1024T _{OSSC}	—	T _{OSSC} = OSC1 period
33	T _{PWRT}	Power up Timer Period	28	72	132	ms	
34	T _{IOZ}	I/O Hi-Impedance from MCLR Low or Watchdog Timer Reset	—	2	—	μs	
35	T _{BOR}	Brown-out Reset Pulse Width	200	—	—	μs	V _D ≤ V _B (see D005)
36	T _{IVRST}	Time for Internal Reference Voltage to become stable	—	20	50	μs	
37	T _{LVD}	Low Voltage Detect Pulse Width	200	—	—	μs	V _D ≤ V _{LVD}

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FIGURE 26-11: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

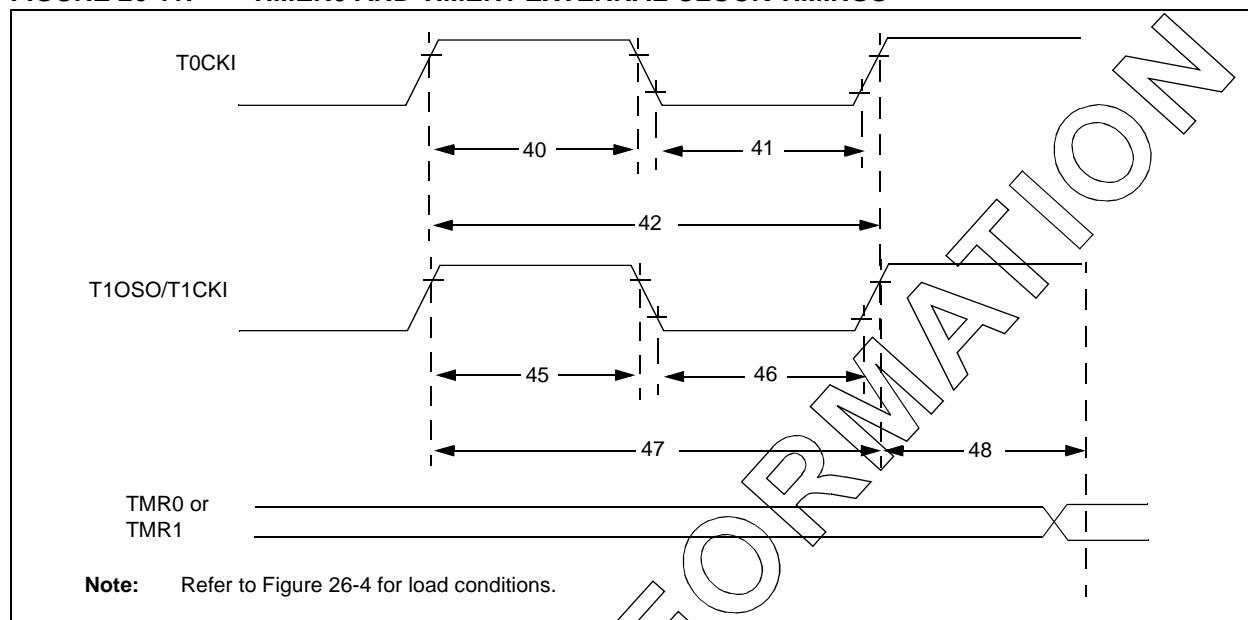


TABLE 26-12: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
40	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5TCY + 20	—	ns	
			With Prescaler	10	—	ns	
41	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5TCY + 20	—	ns	
			With Prescaler	10	—	ns	
42	Tt0P	T0CKI Period	No Prescaler	TCY + 10	—	ns	N = prescale value (1, 2, 4,..., 256)
			With Prescaler	Greater of: 20 ns or $\frac{TCY + 40}{N}$	—	ns	
45	Tt1H	T1CKI High Time	Synchronous, no prescaler	0.5TCY + 20	—	ns	
			PIC18FXX20	10	—	ns	
			PIC18LFX20	25	—	ns	
			Asynchronous	PIC18FXX20	30	—	ns
				PIC18LFX20	50	—	ns
46	Tt1L	T1CKI Low Time	Synchronous, no prescaler	0.5TCY + 5	—	ns	
			PIC18FXX20	10	—	ns	
			PIC18LFX20	25	—	ns	
			Asynchronous	PIC18FXX20	30	—	ns
				PIC18LFX20	TBD	TBD	ns
47	Tt1P	T1CKI Input Period	Synchronous	Greater of: 20 ns or $\frac{TCY + 40}{N}$	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous		60	—	
	Ft1	T1CKI Oscillator Input Frequency Range	DC	50	kHz		
48	Tcke2tmrl	Delay from External T1CKI Clock Edge to Timer Increment	2Tosc	7Tosc	—		

FIGURE 26-12: CAPTURE/COMPARE/PWM TIMINGS (ALL CCP MODULES)

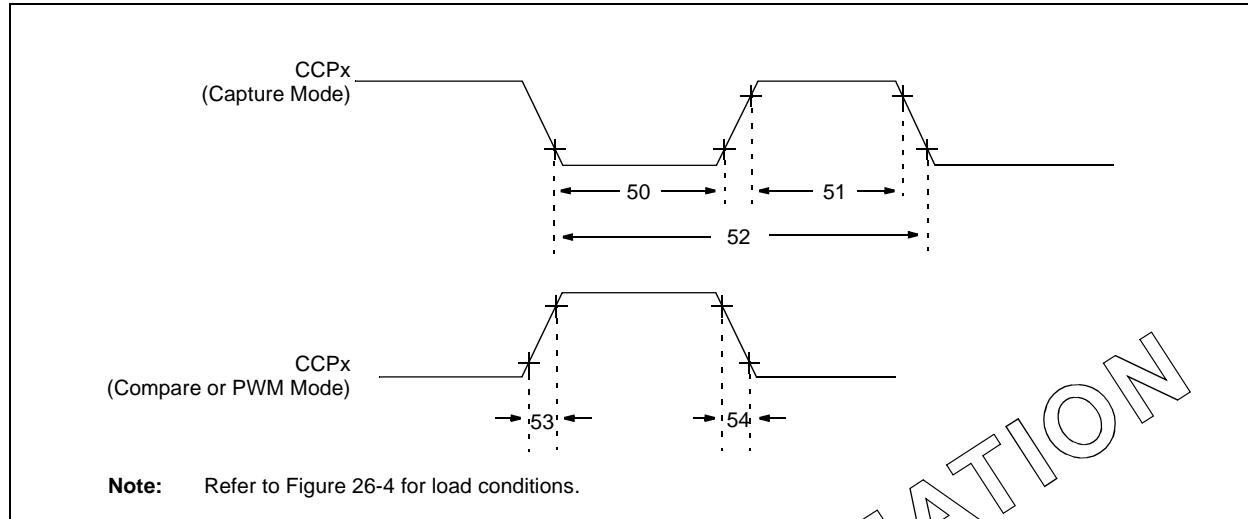


TABLE 26-13: CAPTURE/COMPARE/PWM REQUIREMENTS (ALL CCP MODULES)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
50	TccL	CCPx Input Low Time	No Prescaler	0.5TCY + 20	—	ns	
			With Prescaler	PIC18FXX20	10	—	
			With Prescaler	PIC18LFXX20	20	—	
51	TccH	CCPx Input High Time	No Prescaler	0.5TCY + 20	—	ns	
			With Prescaler	PIC18FXX20	10	—	
			With Prescaler	PIC18LFXX20	20	—	
52	TccP	CCPx Input Period		$\frac{3TCY + 40}{N}$	—	ns	N = prescale value (1, 4 or 16)
53	TccR	CCPx Output Fall Time	PIC18FXX20	—	25	ns	
			PIC18LFXX20	—	45	ns	
54	TccF	CCPx Output Fall Time	PIC18FXX20	—	25	ns	
			PIC18LFXX20	—	45	ns	

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FIGURE 26-13: PARALLEL SLAVE PORT TIMING (PIC18F8X20)

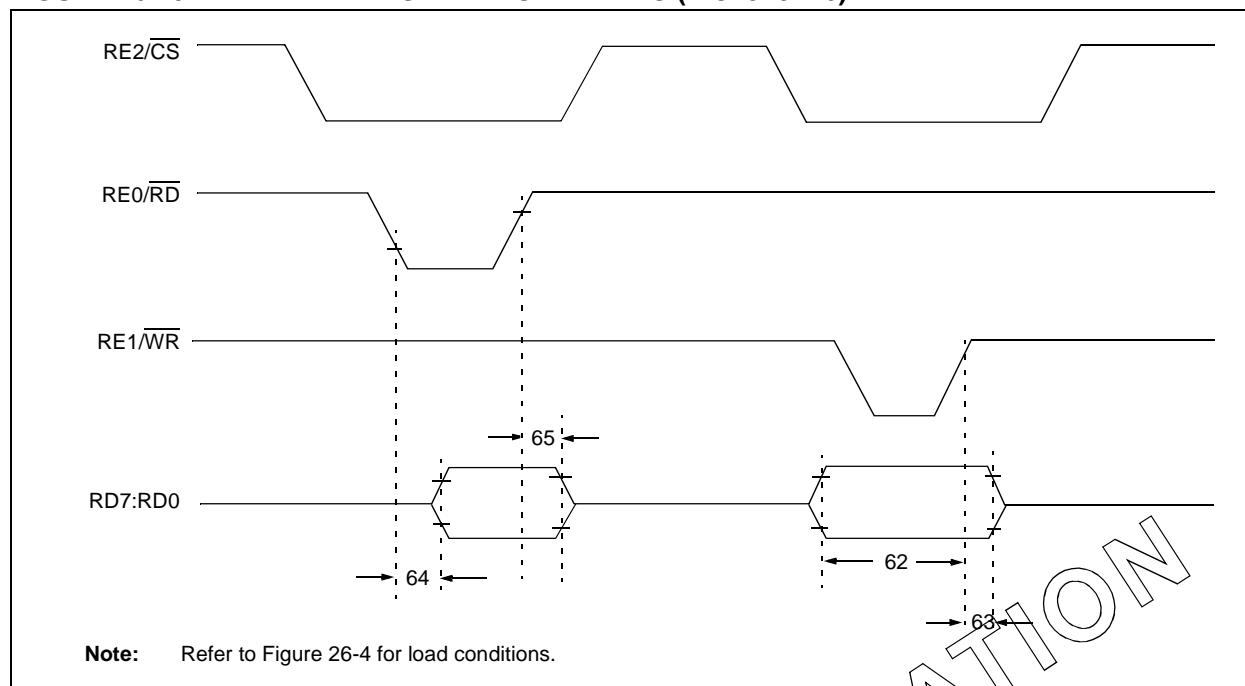


TABLE 26-14: PARALLEL SLAVE PORT REQUIREMENTS (PIC18F8X20)

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
62	TdtV2wrH	Data in valid before WR ↑ or CS ↑ (setup time)	20 25	— —	ns ns	Extended Temp. range
63	TwrH2dtl	WR ↑ or CS ↑ to data-in invalid (hold time)	PIC18FXX20	20	—	ns
				35	—	ns
64	TrdL2dtV	RD ↓ and CS ↓ to data-out valid	— —	80 90	ns ns	Extended Temp. range
65	TrdH2dtl	RD ↑ or CS ↓ to data-out invalid	10	30	ns	
66	TibfNH	Inhibit of the IBF flag bit being cleared from WR ↑ or CS ↑	—	3TCY		

FIGURE 26-14: EXAMPLE SPI MASTER MODE TIMING (CKE = 0)

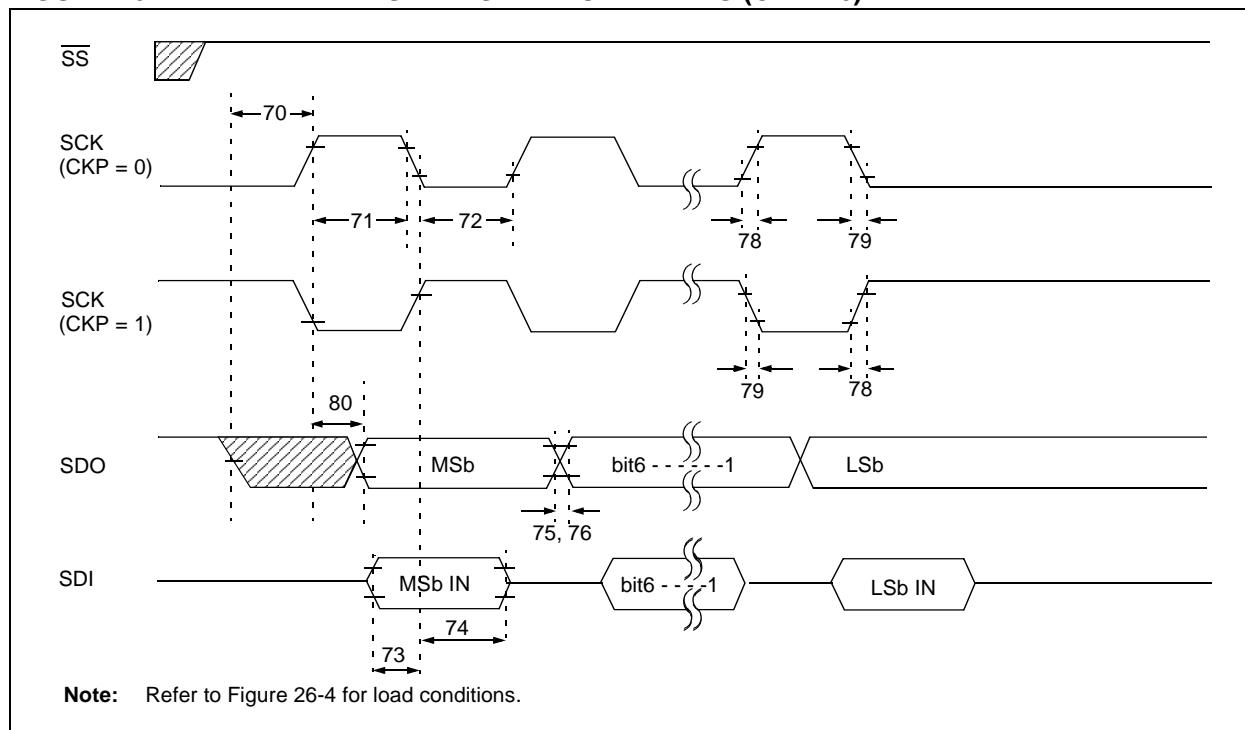


TABLE 26-15: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 0)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	$\overline{SS} \downarrow$ to SCK \downarrow or SCK \uparrow input		—	Tcy	—	ns (Note 1)
71	TscH	SCK input high time (Slave mode)	Continuous	1.25TCY + 30	—	ns	
71A			Single Byte	40	—	ns	(Note 1)
72	TscL	SCK input low time (Slave mode)	Continuous	1.25TCY + 30	—	ns	
72A			Single Byte	40	—	ns	(Note 1)
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge		100	—	ns	
73A	Tb2B	Last clock edge of Byte1 to the 1st clock edge of Byte2		1.5TCY + 40	—	ns	(Note 2)
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge		100	—	ns	
75	TdoR	SDO data output rise time	PIC18FXX20	—	25	ns	
			PIC18LFXX20	—	45	ns	
76	TdoF	SDO data output fall time		—	25	ns	
78	TscR	SCK output rise time (Master mode)	PIC18FXX20	—	25	ns	
			PIC18LFXX20	—	45	ns	
79	TscF	SCK output fall time (Master mode)		—	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC18FXX20	—	50	ns	
			PIC18LFXX20	—	100	ns	

Note 1: Requires the use of Parameter #73A.

2: Only if Parameter #71A and #72A are used.

PIC18FXX20

FIGURE 26-15: EXAMPLE SPI MASTER MODE TIMING (CKE = 1)

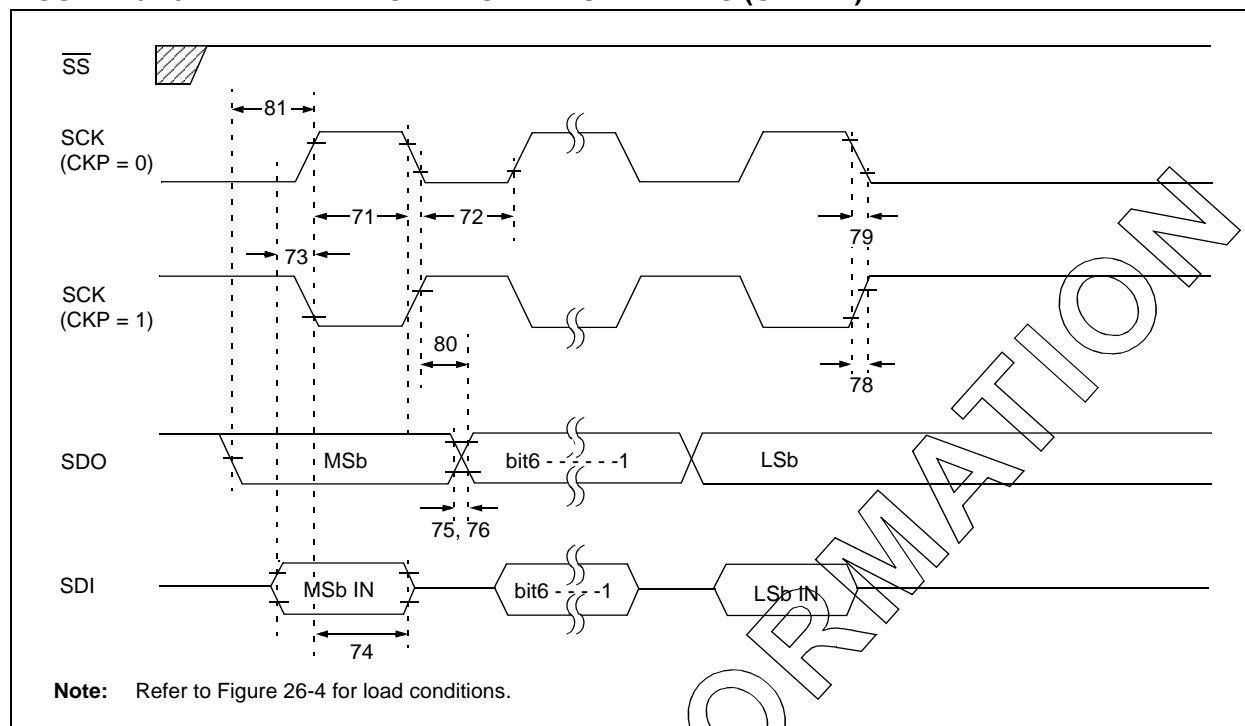


TABLE 26-16: EXAMPLE SPI MODE REQUIREMENTS (MASTER MODE, CKE = 1)

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
71	TscH	SCK input high time (Slave mode)	Continuous	1.25TCY + 30	—	ns
71A			Single Byte	40	—	ns (Note 1)
72	TscL	SCK input low time (Slave mode)	Continuous	1.25TCY + 30	—	ns
72A			Single Byte	40	—	ns (Note 1)
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	100	—	ns	
73A	TB2B	Last clock edge of Byte1 to the 1st clock edge of Byte2	1.5TCY + 40	—	ns	(Note 2)
74	TscH2dil, TscL2dil	Hold time of SDI data input to SCK edge	100	—	ns	
75	TdoR	SDO data output rise time	PIC18FXX20	—	25	ns
			PIC18LFXX20		45	ns
76	TdoF	SDO data output fall time	—	25	ns	
78	TscR	SCK output rise time (Master mode)	PIC18FXX20	—	25	ns
			PIC18LFXX20		45	ns
79	TscF	SCK output fall time (Master mode)	—	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC18FXX20	—	50	ns
			PIC18LFXX20		100	ns
81	TdoV2scH, TdoV2scL	SDO data output setup to SCK edge	TCY	—	ns	

Note 1: Requires the use of Parameter #73A.

2: Only if Parameter #71A and #72A are used.

FIGURE 26-16: EXAMPLE SPI SLAVE MODE TIMING (CKE = 0)

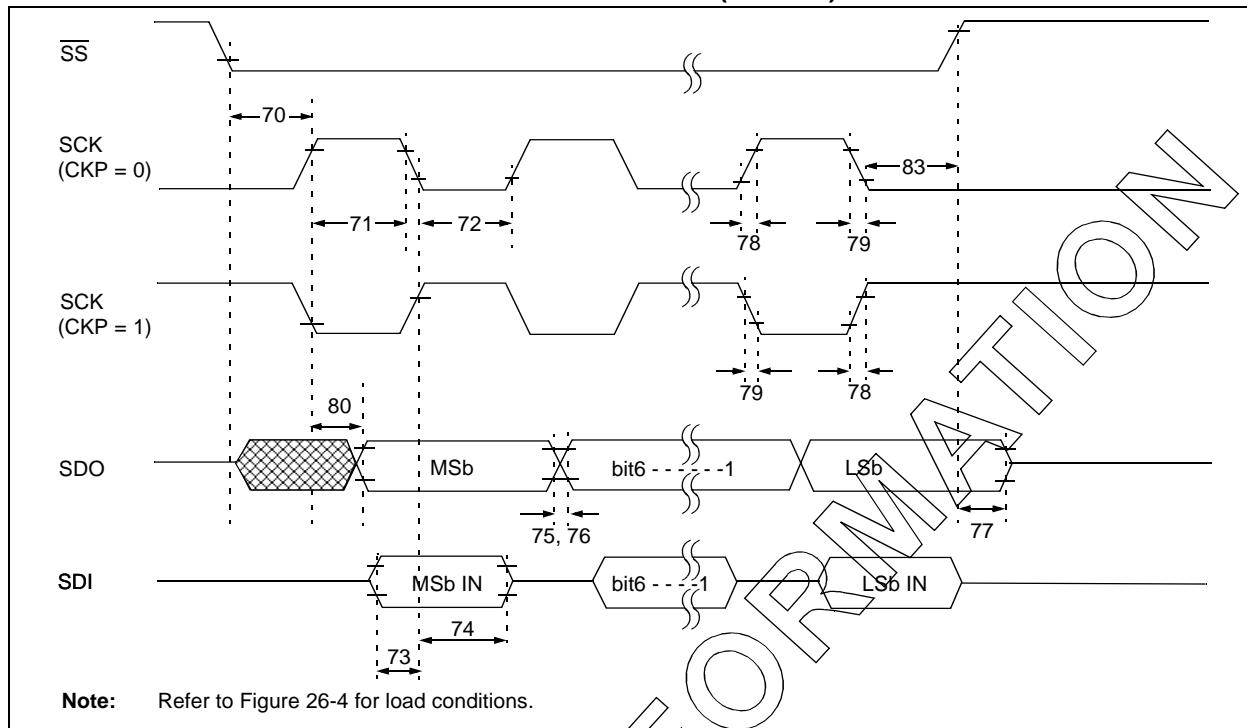


TABLE 26-17: EXAMPLE SPI MODE REQUIREMENTS (SLAVE MODE TIMING (CKE = 0))

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	SS ↓ to SCK ↓ or SCK ↑ input	TCY	—	ns	
71	TscH	SCK input high time (Slave mode)	Continuous	1.25TCY + 30	—	ns
71A			Single Byte	40	—	ns (Note 1)
72	TscL	SCK input low time (Slave mode)	Continuous	1.25TCY + 30	—	ns
72A			Single Byte	40	—	ns (Note 1)
73	TdiV2scH, TdiV2scL	Setup time of SDI data input to SCK edge	100	—	ns	
73A	TB2B	Last clock edge of Byte1 to the first clock edge of Byte2	1.5TCY + 40	—	ns	(Note 2)
74	TscH2dil, Tscl2dil	Hold time of SDI data input to SCK edge	100	—	ns	
75	TdoR	SDO data output rise time	PIC18FXX20	—	25	ns
76			PIC18LFXX20	—	45	ns
77	TssH2doZ	SS ↑ to SDO output hi-impedance	10	50	ns	
78	TscR	SCK output rise time (Master mode)	PIC18FXX20	—	25	ns
79			PIC18LFXX20	—	45	ns
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC18FXX20	—	50	ns
83	TscH2ssH, TscL2ssH	SS ↑ after SCK edge	PIC18LFXX20	—	100	ns
			1.5TCY + 40	—	ns	

Note 1: Requires the use of Parameter #73A.

2: Only if Parameter #71A and #72A are used.

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FIGURE 26-17: EXAMPLE SPI SLAVE MODE TIMING (CKE = 1)

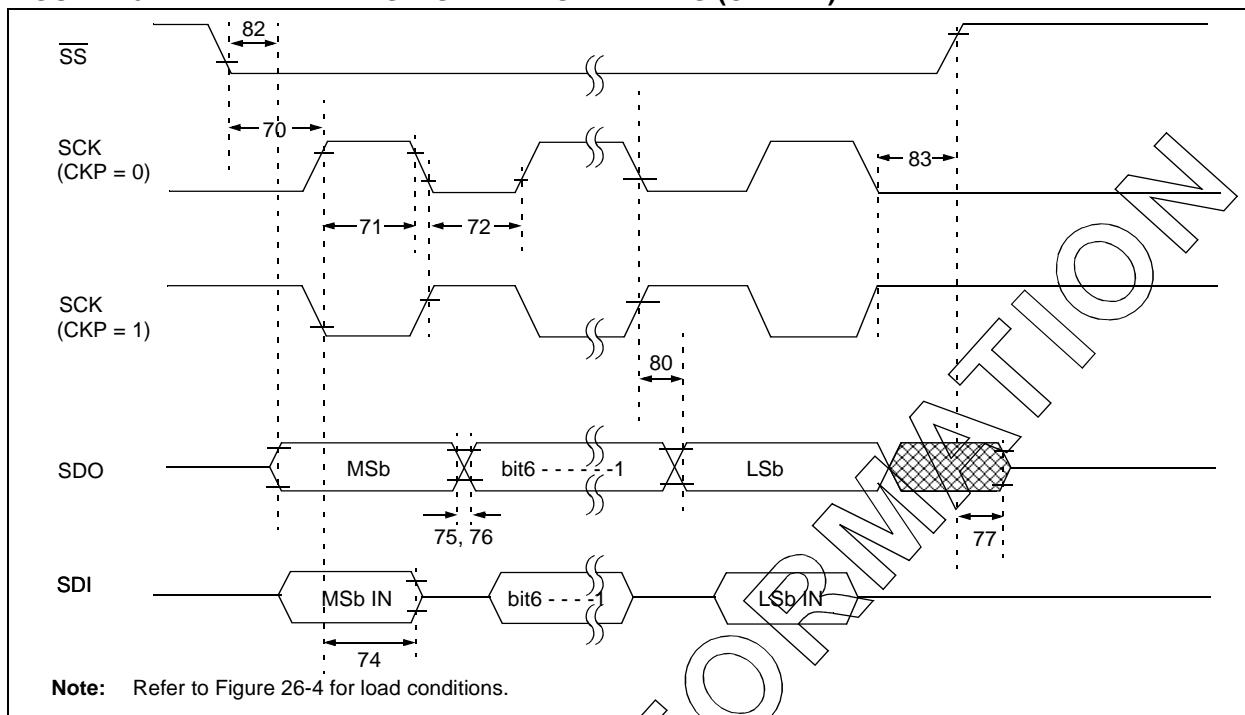


TABLE 26-18: EXAMPLE SPI SLAVE MODE REQUIREMENTS (CKE = 1)

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
70	TssL2scH, TssL2scL	SS ↓ to SCK ↓ or SCK ↑ input	TCY	—	ns	
71	TscH	SCK input high time (Slave mode)	Continuous	1.25TCY + 30	—	ns
71A			Single Byte	40	—	ns (Note 1)
72	TscL	SCK input low time (Slave mode)	Continuous	1.25TCY + 30	—	ns
72A			Single Byte	40	—	ns (Note 1)
73A	TB2B	Last clock edge of Byte1 to the first clock edge of Byte2	1.5TCY + 40	—	ns	(Note 2)
74	TscH2diL, TscL2diL	Hold time of SDI data input to SCK edge	100	—	ns	
75	TdoR	SDO data output rise time	PIC18FXX20	—	25	ns
			PIC18LFXX20		45	ns
76	TdoF	SDO data output fall time	—	25	ns	
77	TssH2doZ	SS ↑ to SDO output hi-impedance	10	50	ns	
78	TscR	SCK output rise time (Master mode)	PIC18FXX20	—	25	ns
			PIC18LFXX20		45	ns
79	TscF	SCK output fall time (Master mode)	—	25	ns	
80	TscH2doV, TscL2doV	SDO data output valid after SCK edge	PIC18FXX20	—	50	ns
			PIC18LFXX20		100	ns
82	TssL2doV	SDO data output valid after SS ↓ edge	PIC18FXX20	—	50	ns
			PIC18LFXX20		100	ns
83	TscH2ssH, TscL2ssH	SS ↑ after SCK edge	1.5TCY + 40	—	ns	

Note 1: Requires the use of Parameter #73A.

2: Only if Parameter #71A and #72A are used.

FIGURE 26-18: I²C BUS START/STOP BITS TIMING

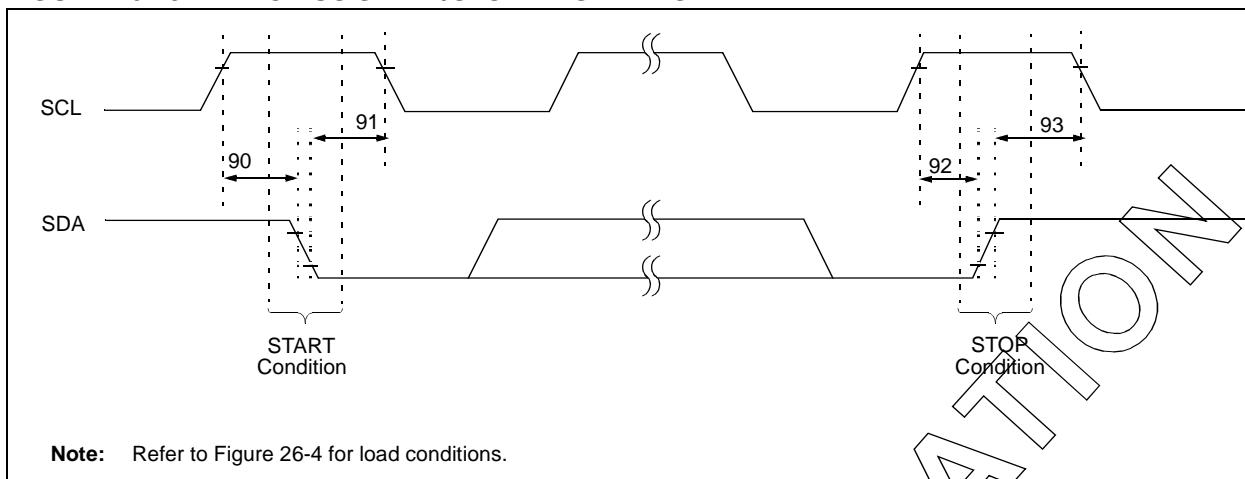
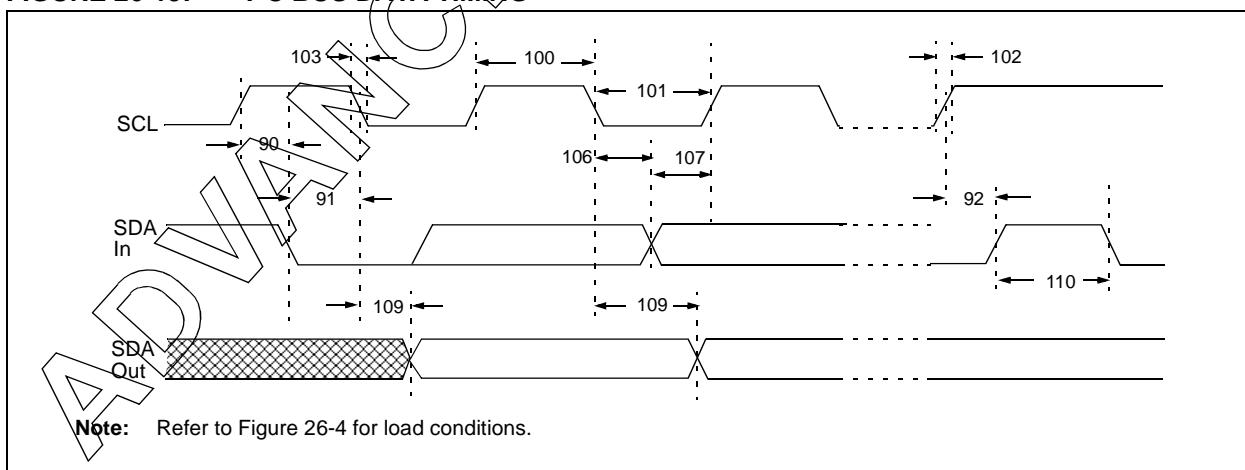


TABLE 26-19: I²C BUS START/STOP BITS REQUIREMENTS (SLAVE MODE)

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
90	TSU:STA	START condition Setup time	100 kHz mode 400 kHz mode	4700 600	—	ns Only relevant for Repeated START condition
		Hold time	100 kHz mode 400 kHz mode	4000 600	—	
91	THD:STA	START condition Hold time	100 kHz mode 400 kHz mode	4000 600	—	ns After this period, the first clock pulse is generated
		Setup time	100 kHz mode 400 kHz mode	4700 600	—	
92	TSU:STO	STOP condition Setup time	100 kHz mode 400 kHz mode	4700 600	—	ns
		Hold time	100 kHz mode 400 kHz mode	4000 600	—	
93	THD:STO	STOP condition Hold time	100 kHz mode 400 kHz mode	4000 600	—	ns

FIGURE 26-19: I²C BUS DATA TIMING



PIC18FXX20

TABLE 26-20: I²C BUS DATA REQUIREMENTS (SLAVE MODE)

Param. No.	Symbol	Characteristic		Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	4.0	—	μs	PIC18FXX20 must operate at a minimum of 1.5 MHz
			400 kHz mode	0.6	—	μs	PIC18FXX20 must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—	—	—
101	TLOW	Clock low time	100 kHz mode	4.7	—	μs	PIC18FXX20 must operate at a minimum of 1.5 MHz
			400 kHz mode	1.3	—	μs	PIC18FXX20 must operate at a minimum of 10 MHz
			SSP Module	1.5TCY	—	—	—
102	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns	—
			400 kHz mode	20 + 0.1CB	300	ns	CB is specified to be from 10 to 400 pF
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns	—
			400 kHz mode	20 + 0.1CB	300	ns	CB is specified to be from 10 to 400 pF
90	TSU:STA	START condition setup time	100 kHz mode	4.7	—	μs	Only relevant for Repeated START condition
			400 kHz mode	0.6	—	μs	—
91	THD:STA	START condition hold time	100 kHz mode	4.0	—	μs	After this period, the first clock pulse is generated
			400 kHz mode	0.6	—	μs	—
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns	—
			400 kHz mode	0	0.9	μs	—
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns	(Note 2)
			400 kHz mode	100	—	ns	—
92	TSU:STO	STOP condition setup time	100 kHz mode	4.7	—	μs	—
			400 kHz mode	0.6	—	μs	—
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns	(Note 1)
			400 kHz mode	—	—	ns	—
110	TBUF	Bus free time	100 kHz mode	4.7	—	μs	Time the bus must be free before a new transmission can start
			400 kHz mode	1.3	—	μs	—
D102	CB	Bus capacitive loading		—	400	pF	—

Note 1: As a transmitter, the device must provide this internal minimum delay time to bridge the undefined region (min. 300 ns) of the falling edge of SCL to avoid unintended generation of START or STOP conditions.

2: A fast mode I²C bus device can be used in a standard mode I²C bus system, but the requirement TSU:DAT ≥ 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line.

TR max. + TSU:DAT = 1000 + 250 = 1250 ns (according to the standard mode I²C bus specification) before the SCL line is released.

FIGURE 26-20: MASTER SSP I²C BUS START/STOP BITS TIMING WAVEFORMS

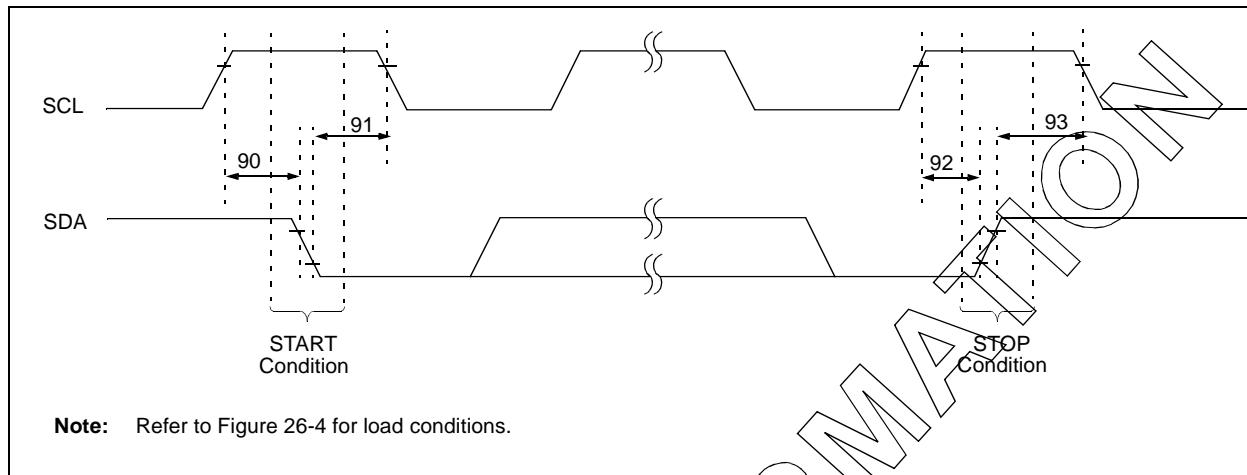
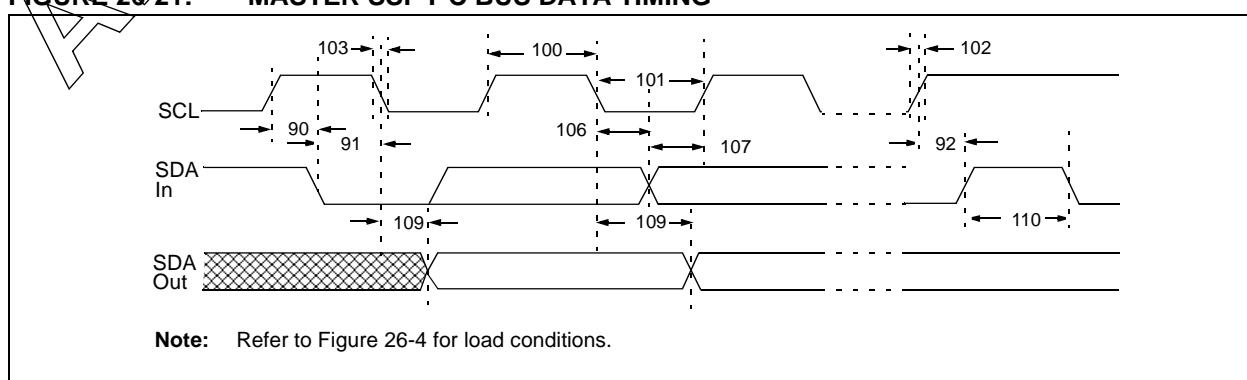


TABLE 26-21: MASTER SSP I²C BUS START/STOP BITS REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
90	TSU:STA	START condition	100 kHz mode	2(Tosc)(BRG + 1)	—	ns Only relevant for Repeated START condition
		Setup time	400 kHz mode	2(Tosc)(BRG + 1)	—	
		1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	—	—	
91	THD:STA	START condition	100 kHz mode	2(Tosc)(BRG + 1)	—	ns After this period, the first clock pulse is generated
		Hold time	400 kHz mode	2(Tosc)(BRG + 1)	—	
		1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	—	—	
92	TSU:STO	STOP condition	100 kHz mode	2(Tosc)(BRG + 1)	—	ns
		Setup time	400 kHz mode	2(Tosc)(BRG + 1)	—	
		1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	—	—	
93	THD:STO	STOP condition	100 kHz mode	2(Tosc)(BRG + 1)	—	ns
		Hold time	400 kHz mode	2(Tosc)(BRG + 1)	—	
		1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	—	—	

Note 1: Maximum pin capacitance = 10 pF for all I²C pins.

FIGURE 26-21: MASTER SSP I²C BUS DATA TIMING



PIC18FXX20

TABLE 26-22: MASTER SSP I²C BUS DATA REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
100	THIGH	Clock high time	100 kHz mode	2(Tosc)(BRG + 1)	—	ms
			400 kHz mode	2(Tosc)(BRG + 1)	—	ms
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	—	ms
101	TLOW	Clock low time	100 kHz mode	2(Tosc)(BRG + 1)	—	ms
			400 kHz mode	2(Tosc)(BRG + 1)	—	ms
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	—	ms
102	TR	SDA and SCL rise time	100 kHz mode	—	1000	ns ✓ CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1CB	300	ns
			1 MHz mode ⁽¹⁾	—	300	ns
103	TF	SDA and SCL fall time	100 kHz mode	—	300	ns ✓ CB is specified to be from 10 to 400 pF
			400 kHz mode	20 + 0.1CB	300	ns
			1 MHz mode ⁽¹⁾	—	100	ns
90	TSU:STA	START condition setup time	100 kHz mode	2(Tosc)(BRG + 1)	—	ms
			400 kHz mode	2(Tosc)(BRG + 1)	—	ms
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	—	ms
91	THD:STA	START condition hold time	100 kHz mode	2(Tosc)(BRG + 1)	—	ms
			400 kHz mode	2(Tosc)(BRG + 1)	—	ms
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	—	ms
106	THD:DAT	Data input hold time	100 kHz mode	0	—	ns
			400 kHz mode	0	0.9	ms
			1 MHz mode ⁽¹⁾	TBD	—	ns
107	TSU:DAT	Data input setup time	100 kHz mode	250	—	ns
			400 kHz mode	100	—	ns
			1 MHz mode ⁽¹⁾	TBD	—	ns
92	TSU:STO	STOP condition setup time	100 kHz mode	2(Tosc)(BRG + 1)	—	ms
			400 kHz mode	2(Tosc)(BRG + 1)	—	ms
			1 MHz mode ⁽¹⁾	2(Tosc)(BRG + 1)	—	ms
109	TAA	Output valid from clock	100 kHz mode	—	3500	ns
			400 kHz mode	—	1000	ns
			1 MHz mode ⁽¹⁾	—	—	ns
110	TBUF	Bus free time	100 kHz mode	4.7	—	ms
			400 kHz mode	1.3	—	ms
			1 MHz mode ⁽¹⁾	TBD	—	ms
D102	CB	Bus capacitive loading	—	400	pF	

Note 1: Maximum pin capacitance = 10 pF for all I²C pins.

2: A fast mode I²C bus device can be used in a standard mode I²C bus system, but parameter #107 \geq 250 ns must then be met. This will automatically be the case if the device does not stretch the LOW period of the SCL signal. If such a device does stretch the LOW period of the SCL signal, it must output the next data bit to the SDA line, parameter #102.+ parameter #107 = 1000 + 250 = 1250 ns (for 100 kHz mode) before the SCL line is released.

FIGURE 26-22: USART SYNCHRONOUS TRANSMISSION (MASTER/SLAVE) TIMING

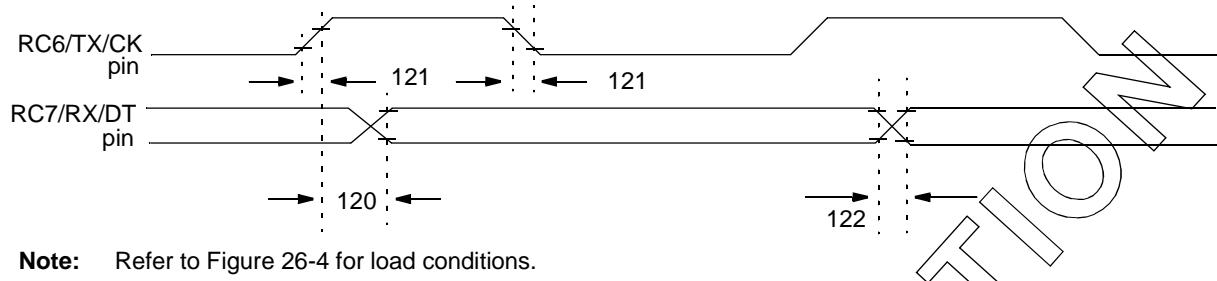


TABLE 26-23: USART SYNCHRONOUS TRANSMISSION REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions	
120	TckH2dtV	SYNC XMIT (MASTER & SLAVE) Clock high to data out valid	PIC18FXX20 PIC18LFXX20	—	40	ns	
				—	100	ns	
121	Tckrf	Clock out rise time and fall time (Master mode)	PIC18FXX20 PIC18LFXX20	—	20	ns	
				—	50	ns	
122	Tdtrf	Data out rise time and fall time	PIC18FXX20 PIC18LFXX20	—	20	ns	
				—	50	ns	

FIGURE 26-23: USART SYNCHRONOUS RECEIVE (MASTER/SLAVE) TIMING

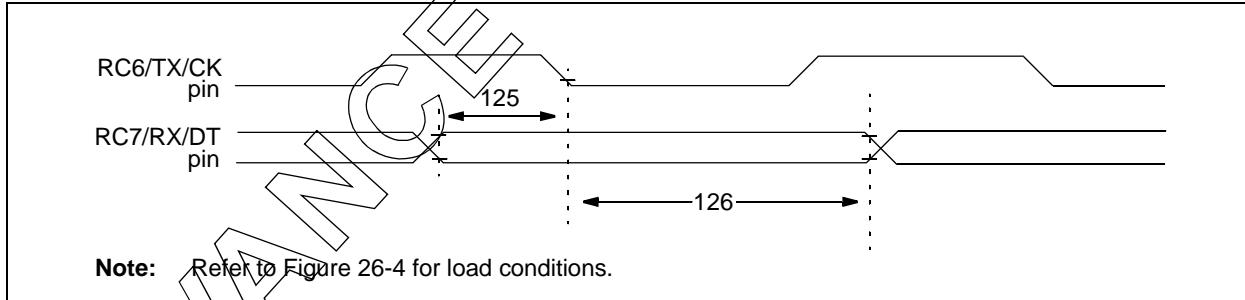


TABLE 26-24: USART SYNCHRONOUS RECEIVE REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
125	TdtV2clk	SYNC RCV (MASTER & SLAVE) Data hold before CK ↓ (DT hold time)	10	—	ns	
126	TckL2dtl	Data hold after CK ↓ (DT hold time)	15	—	ns	

PIC18FXX20

**TABLE 26-25: A/D CONVERTER CHARACTERISTICS: PIC18FXX20 (INDUSTRIAL, EXTENDED)
PIC18LFXX20 (INDUSTRIAL)**

Param No.	Symbol	Characteristic	Min	Typ	Max	Units	Conditions
A01	NR	Resolution	— —	— —	10 TBD	bit bit	$V_{REF} = V_{DD} \geq 3.0V$ $V_{REF} = V_{DD} < 3.0V$
A03	EIL	Integral linearity error	— —	— —	$<\pm 1$ TBD	LSb LSb	$V_{REF} = V_{DD} \geq 3.0V$ $V_{REF} = V_{DD} < 3.0V$
A04	EDL	Differential linearity error	— —	— —	$<\pm 1$ TBD	LSb LSb	$V_{REF} = V_{DD} \geq 3.0V$ $V_{REF} = V_{DD} < 3.0V$
A05	EFS	Full scale error	— —	— —	$<\pm 1$ TBD	LSb LSb	$V_{REF} = V_{DD} \geq 3.0V$ $V_{REF} = V_{DD} < 3.0V$
A06	E _{OFF}	Offset error	— —	— —	$<\pm 1$ TBD	LSb LSb	$V_{REF} = V_{DD} \geq 3.0V$ $V_{REF} = V_{DD} < 3.0V$
A10	—	Monotonicity	guaranteed ⁽³⁾			—	$V_{SS} \leq V_{AIN} \leq V_{REF}$
A20	V _{REF}	Reference voltage (V _{REFH} - V _{REFL})	0V 3V	—	—	V	
A20A				—	—	V	For 10-bit resolution
A21	V _{REFH}	Reference voltage High	AV _{SS}	—	AV _{DD} + 0.3V	V	
A22	V _{REFL}	Reference voltage Low	AV _{SS} - 0.3V	—	AV _{DD}	V	
A25	V _{AIN}	Analog input voltage	AV _{SS} - 0.3V	—	V _{REF} + 0.3V	V	
A30	Z _{AIN}	Recommended impedance of analog voltage source	—	—	10.0	kΩ	
A40	I _{AD}	A/D conversion current (V _{DD})	PIC18FXX20 PIC18LFXX20	180 —	— —	μA μA	Average current consumption when A/D is on (Note 1)
A50	I _{REF}	V _{REF} input current (Note 2)	—	10 —	1000 10	μA μA	During V _{AIN} acquisition. Based on differential of V _{HOLD} to V _{AIN} . To charge C _{HOLD} see Section 19.0. During A/D conversion cycle.

Note 1: When A/D is off, it will not consume any current other than minor leakage current. The power-down current spec includes any such leakage from the A/D module.

V_{REF}/current is from RA2/AN2/V_{REF}- and RA3/AN3/V_{REF}+ pins or AV_{DD} and AV_{SS} pins, whichever is selected as reference input.

2: $V_{SS} \leq V_{AIN} \leq V_{REF}$

3: The A/D conversion result never decreases with an increase in the Input Voltage, and has no missing codes.

FIGURE 26-24: A/D CONVERSION TIMING

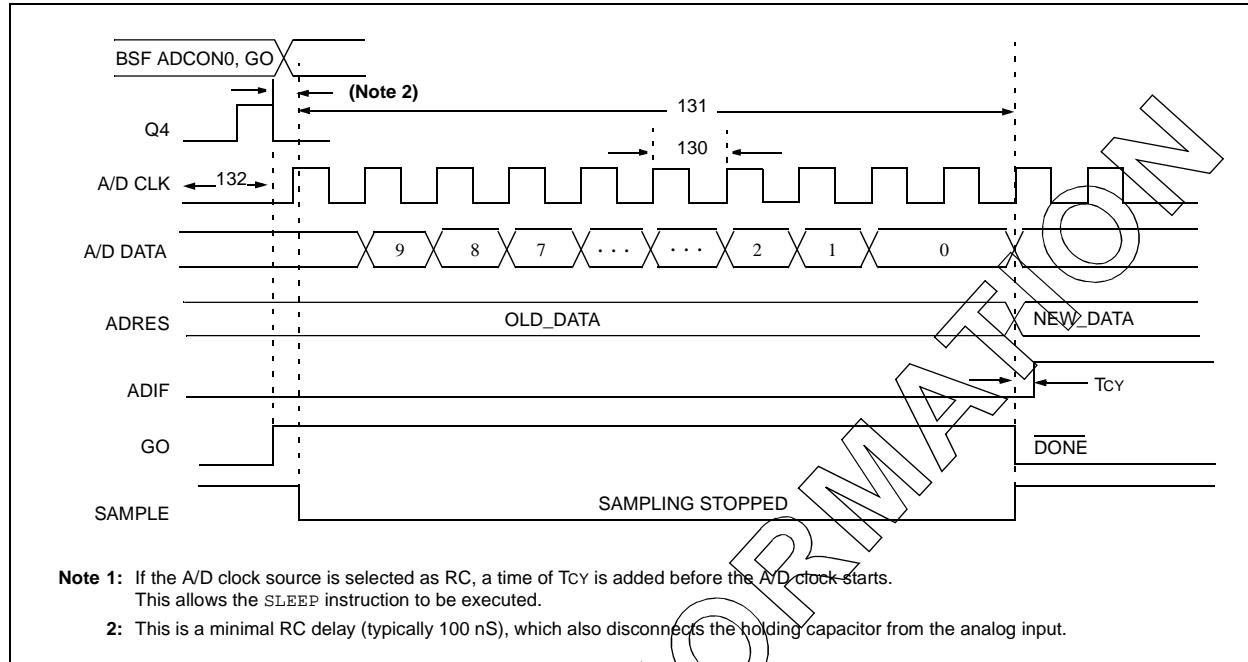


TABLE 26-26: A/D CONVERSION REQUIREMENTS

Param. No.	Symbol	Characteristic	Min	Max	Units	Conditions
130	TAD	A/D clock period PIC18FXX20	1.6	20 ⁽⁵⁾	μs	Tosc based, VREF ≥ 3.0V
			3.0	20 ⁽⁵⁾	μs	Tosc based, VREF full range
			2.0	6.0	μs	A/D RC mode
			3.0	9.0	μs	A/D RC mode
131	T _{CNV}	Conversion time (not including acquisition time) (Note 1)	11	12	TAD	
132	T _{ACQ}	Acquisition time (Note 3)	15	—	μs	-40°C ≤ Temp ≤ 125°C
			10	—	μs	0°C ≤ Temp ≤ 125°C
135	T _{SWC}	Switching time from convert → sample	—	(Note 4)		
136	T _{AMP}	Amplifier settling time (Note 2)	1	—	μs	This may be used if the "new" input voltage has not changed by more than 1 Lsb (i.e., 5 mV @ 5.12V) from the last sampled voltage (as stated on CHOLD).

Note 1: ADRES register may be read on the following T_{CY} cycle.

2: See Section 19.0 for minimum conditions, when input voltage has changed more than 1 Lsb.

3: The time for the holding capacitor to acquire the "New" input voltage, when the voltage changes full scale after the conversion (AVDD to AVss, or AVss to AVDD). The source impedance (R_s) on the input channels is 50Ω.

4: On the next Q4 cycle of the device clock.

5: The time of the A/D clock period is dependent on the device frequency and the TAD clock divider.

PIC18FXX20

NOTES:

27.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

Graphs are not available at this time.

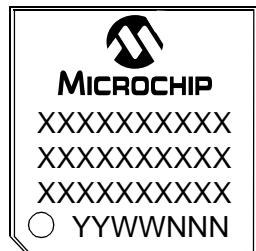
PIC18FXX20

NOTES:

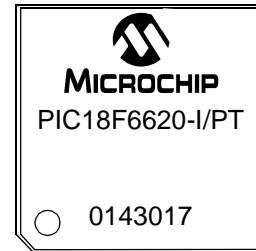
28.0 PACKAGING INFORMATION

28.1 Package Marking Information

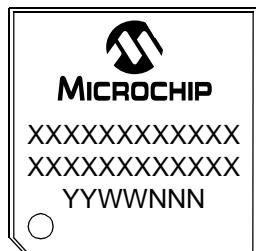
64-Lead TQFP



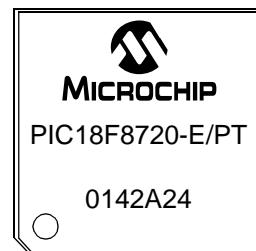
Example



80-Lead TQFP



Example



Legend:

XX...X	Customer specific information*
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

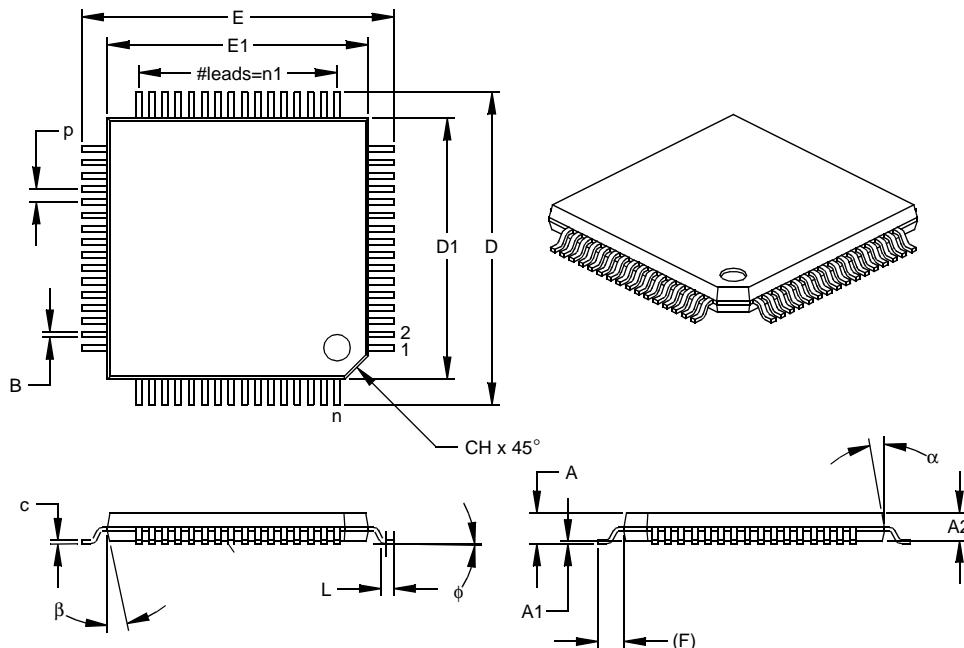
* Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

PIC18FXX20

28.2 Package Details

The following sections give the technical details of the packages.

64-Lead Plastic Thin Quad Flatpack (PT) 10x10x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)



Dimension Limits	INCHES			MILLIMETERS*			
	MIN	NOM	MAX	MIN	NOM	MAX	
Number of Pins	n		64			64	
Pitch	p		.020			0.50	
Pins per Side	n1		16			16	
Overall Height	A	.039	.043	.047	1.00	1.10	1.20
Molded Package Thickness	A2	.037	.039	.041	0.95	1.00	1.05
Standoff §	A1	.002	.006	.010	0.05	0.15	0.25
Foot Length	L	.018	.024	.030	0.45	0.60	0.75
Footprint (Reference)	(F)		.039			1.00	
Foot Angle	φ	0	3.5	7	0	3.5	7
Overall Width	E	.463	.472	.482	11.75	12.00	12.25
Overall Length	D	.463	.472	.482	11.75	12.00	12.25
Molded Package Width	E1	.390	.394	.398	9.90	10.00	10.10
Molded Package Length	D1	.390	.394	.398	9.90	10.00	10.10
Lead Thickness	c	.005	.007	.009	0.13	0.18	0.23
Lead Width	B	.007	.009	.011	0.17	0.22	0.27
Pin 1 Corner Chamfer	CH	.025	.035	.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

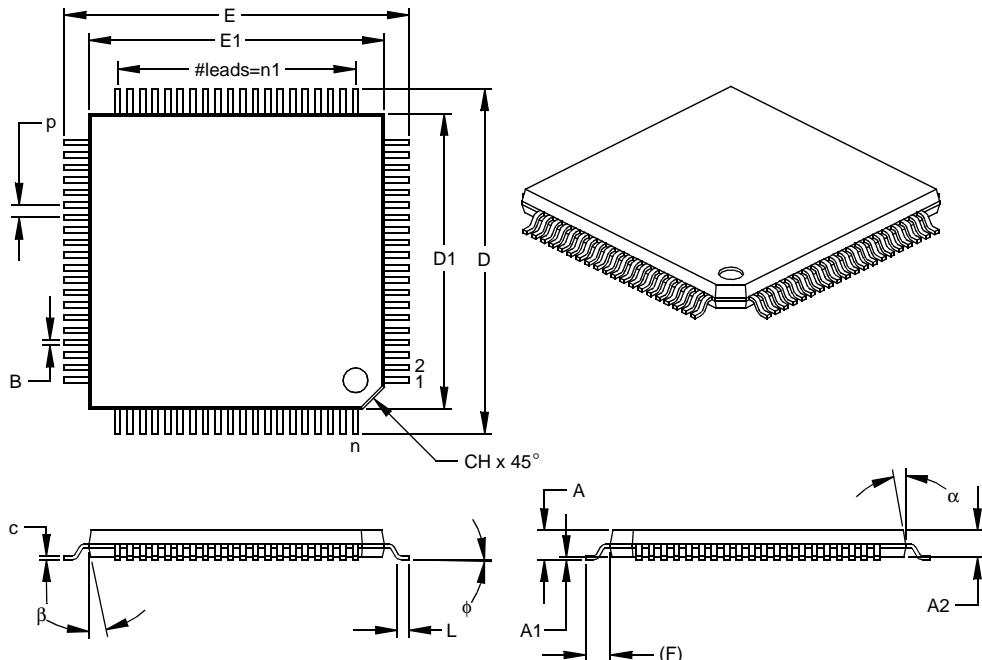
Notes:

Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-026

Drawing No. C04-085

80-Lead Plastic Thin Quad Flatpack (PT) 12x12x1 mm Body, 1.0/0.10 mm Lead Form (TQFP)



Dimension	Limits	INCHES			MILLIMETERS*		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		80			80	
Pitch	P		.020			0.50	
Pins per Side	n1		20			20	
Overall Height	A	.039	.043	.047	1.00	1.10	1.20
Molded Package Thickness	A2	.037	.039	.041	0.95	1.00	1.05
Standoff §	A1	.002	.004	.006	0.05	0.10	0.15
Foot Length	L	.018	.024	.030	0.45	0.60	0.75
Footprint (Reference)	(F)		.039			1.00	
Foot Angle	ϕ	0	3.5	7	0	3.5	7
Overall Width	E	.541	.551	.561	13.75	14.00	14.25
Overall Length	D	.541	.551	.561	13.75	14.00	14.25
Molded Package Width	E1	.463	.472	.482	11.75	12.00	12.25
Molded Package Length	D1	.463	.472	.482	11.75	12.00	12.25
Lead Thickness	c	.004	.006	.008	0.09	0.15	0.20
Lead Width	B	.007	.009	.011	0.17	0.22	0.27
Pin 1 Corner Chamfer	CH	.025	.035	.045	0.64	0.89	1.14
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

Notes:

Dimensions D1 and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-026
Drawing No. C04-092

PIC18FXX20

NOTES:

APPENDIX A: REVISION HISTORY

Revision A (October 2001)

Original data sheet for PIC18FXX20 family.

APPENDIX B: DEVICE DIFFERENCES

The differences between the devices listed in this data sheet are shown in Table 1.

TABLE 1: DEVICE DIFFERENCES

Feature	PIC18F6620	PIC18F6720	PIC18F8620	PIC18F8720
On-chip Program Memory (Kbytes)	64	128	64	128
I/O Ports	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G	Ports A, B, C, D, E, F, G, H, J	Ports A, B, C, D, E, F, G, H, J
A/D Channels	12	12	16	16
External Memory Interface	No	No	Yes	Yes
Package Types	64-pin TQFP	64-pin TQFP	80-pin TQFP	80-pin TQFP

APPENDIX C: CONVERSION CONSIDERATIONS

This appendix discusses the considerations for converting from previous versions of a device to the ones listed in this data sheet. Typically, these changes are due to the differences in the process technology used. An example of this type of conversion is from a PIC17C756 to a PIC18F8720.

Not Applicable

APPENDIX D: MIGRATION FROM MID-RANGE TO ENHANCED DEVICES

A detailed discussion of the differences between the mid-range MCU devices (i.e., PIC16CXXX) and the enhanced devices (i.e., PIC18FXXX) is provided in AN716, "Migrating Designs from PIC16C74A/74B to PIC18F442." The changes discussed, while device specific, are generally applicable to all mid-range to enhanced device migrations.

This Application Note is available as Literature Number DS00716.

APPENDIX E: MIGRATION FROM HIGH-END TO ENHANCED DEVICES

A detailed discussion of the migration pathway and differences between the high-end MCU devices (i.e., PIC17CXXX) and the enhanced devices (i.e., PIC18FXXXX) is provided in AN726, "PIC17CXXX to PIC18FXXX Migration." This Application Note is available as Literature Number DS00726.

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