Built In Self-Test

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| Test | Result | Test | PC | Reason |
| Test 1: Shift Left (8: ASL) | B4 | 01 | 0x0C | Result is not D0 |
|  | 68 |  |  |  |
|  | D0 |  |  |  |
| Test 2: Rotate Left (9: ROL) | 68 | 02 | 0x1A | Carry is not set |
|  | D0 |  | 0x1F | Result is not 0x41 |
|  | A0 |  |  |  |
|  | 41 |  |  |  |
| Test 3: Logic SR (A: LSR) | 43 | 03 | 0x29 | Carry is not set |
|  | 21 |  | 0x2D | Result is not 0x21 |
| Test 4: Arithmetic SR (B: ASR) | C3 | 04 | 0x37 | Carry is not set |
|  | E1 |  | 0x3B | Result is not 0xE1 |
| Test 5: Add (1234 + 6DCD) = 0x8001 | 01 | 05 | 0x43 | Carry is not set |
|  | 80 |  | 0x49 | Carry is set |
|  |  |  | 0x4D | Result is not 0x80 |
| Test 6: Sub (A765 – 34AB) = 0x72BA | BA | 06 | 0x55 | Carry is set |
|  | 72 |  | 0x5B | Carry is not set |
|  |  |  | 0x5F | Result is not 0x72 |
| Test 7: Rotate Right (C: ROR) | 1B | 07 | 0x70 | Carry is not set |
|  | 0D |  | 0x74 | Result is not 0x61 |
|  | 86 |  |  |  |
|  | C3 |  |  |  |
|  | 61 |  |  |  |
| Test 8: SRAM Imediate Load Store  LMA / SMA | 33 | 08 |  |  |
|  | 22 |  |  |  |
|  | 00 |  | 0x86 | Result was not 00 |
| Test 9: SRAM Register Load/Store  LMR / SMR | 5,4,3,2,1 | 09 | 0x9A | Last Read was not 5 |
|  | 24,1 |  |  |  |
|  | 23,2 |  |  |  |
|  | 22,3 |  |  |  |
|  | 21,4 |  |  |  |
|  | 20,5 |  |  |  |
| Test 10: Stack PUSH/POP | 1E9 |  | 0x1E9 |  |
| END |  | 0A | 0x9D | PASS |

BIST Coverage

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| **Op code** | **Instruction** | **BIST test** | **Details** |
| 0x00 | NOP |  | No operation |
| 0x01 | BRK | All | Halt the program |
| 0x02 | ALU (Format ALU Rd, Rs1, Rs2) | #1 ASL  #2 ROL  #6 SUB  #5 ADD  OR  AND  XOR  NOT  #3 LSR  #4 ASR  #7 ROR  #5 ADC  #6 SBC | ALU instruction  (OR, AND, XOR, NOT, ADD, SUB, ASL, ROL, LSR, ASR, ROR, ADC, SBC) |
| 0x03 | LDR | #2 | Load Register from immediate |
| 0x04 | MOV |  | Copy Register (MOV instruction in ARM) |
| 0x05 | Branch Absolute | BCS  BEQ  JMP  BMI  BPL  BCC  BNE | Jump to an address (8bit)  JMP, BMI, BCS, BEQ, BPL, BCC, BNE |
| 0x06 | ALU Immediate  (Format: ALU Rd, Rd, imm) | #9 INC  #9 DEC | ALU instruction with value from immediate |
| 0x07 | BRANCH Relative | #2 BCS  #1 BEQ  JMP  BMI  BPL  #5 BCC  #9 BNE | Relative Branch (+127 to -128) |
| 0x08 | OUT register | All | Print a register as a character or integer |
| 0x09 | LMA | #8 | Load register from address |
| 0x0A | SMA | #8 | Store register to address |
| 0x0B | LMR | #9 | Load register from address in another register |
| 0x0C | SMR | #9 | Store register into an address in another register |
| 0x0D | OUT Immediate | All | Print the immediate next byte as a character or integer |
| 0x0E | PUSH | #10 |  |
| 0x0F | POP | #10 |  |
| 0x10 | JSR |  | Jump Subroutine, store current PC in stack |
| 0x11 | RTS |  | Return Subroutine, Load PC from stack |
| 0x12 | TST Registers |  | Compare registers |
| 0x13 | TST Register |  | Compare register and immediate |
| 0x14 | LD Special Pointer |  | Data Pointer. Stack Pointer, Program counter |

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| Covered by BIST |
| Completed |
| Planned |