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| Department of Software Engineering | |

**Lab Report: Design and Verification of a Half Adder Circuit**

**Objective:**

To design, simulate, and verify a **Half Adder circuit** using basic logic gates in **Electronics Workbench / Multisim**, and observe the **Sum** and **Carry** outputs.

**Theory:**

A **Half Adder** is a **combinational circuit** that performs the addition of **two single-bit binary numbers**, producing a **Sum (S)** and a **Carry (C)**.

Let:

* Inputs: **A**, **B**
* Outputs:
  + **Sum (S)** = A ⊕ B (**XOR Gate**)
  + **Carry (C)** = A · B (**AND Gate**)

**Boolean Expressions:**

* **Sum (S)** = A XOR B = A⊕B
* **Carry (C)** = A AND B = A·B

This logic is implemented using:

* **1 XOR gate**
* **1 AND gate**

**Components Required:**

* **Electronics Workbench / Multisim**
* Logic Gates: XOR, AND
* 2 Input Switches (A and B)
* 2 LEDs (for Sum and Carry output)
* Connecting wires

**🔌 Half Adder Circuit Diagram**

***(Insert your simulation screenshot below)***

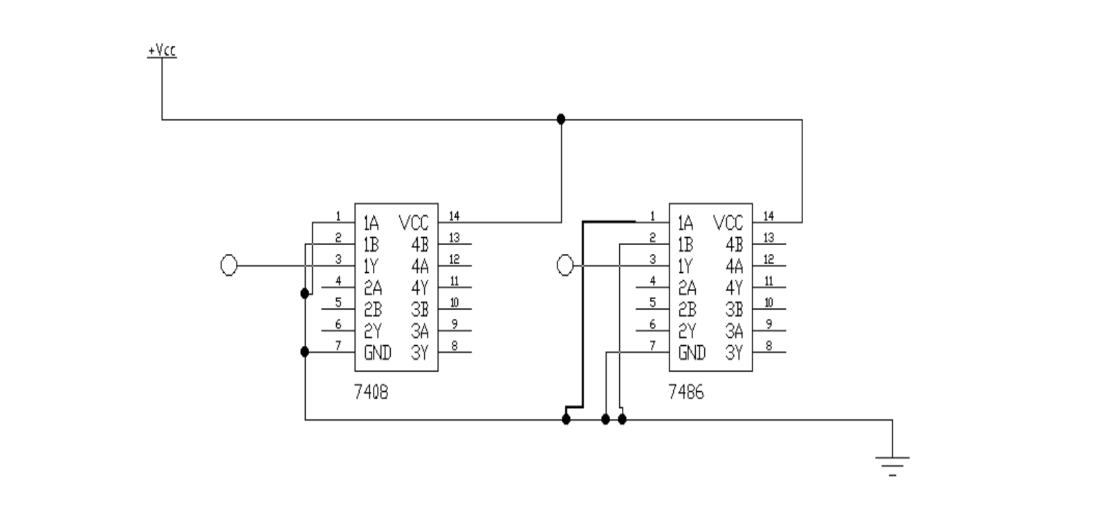
* Input **A and B** connected to:
  + **XOR gate → Sum LED**
  + **AND gate → Carry LED**
* Use LEDs to visually observe output:
  + **ON = 1 (logic high)**
  + **OFF = 0 (logic low)**

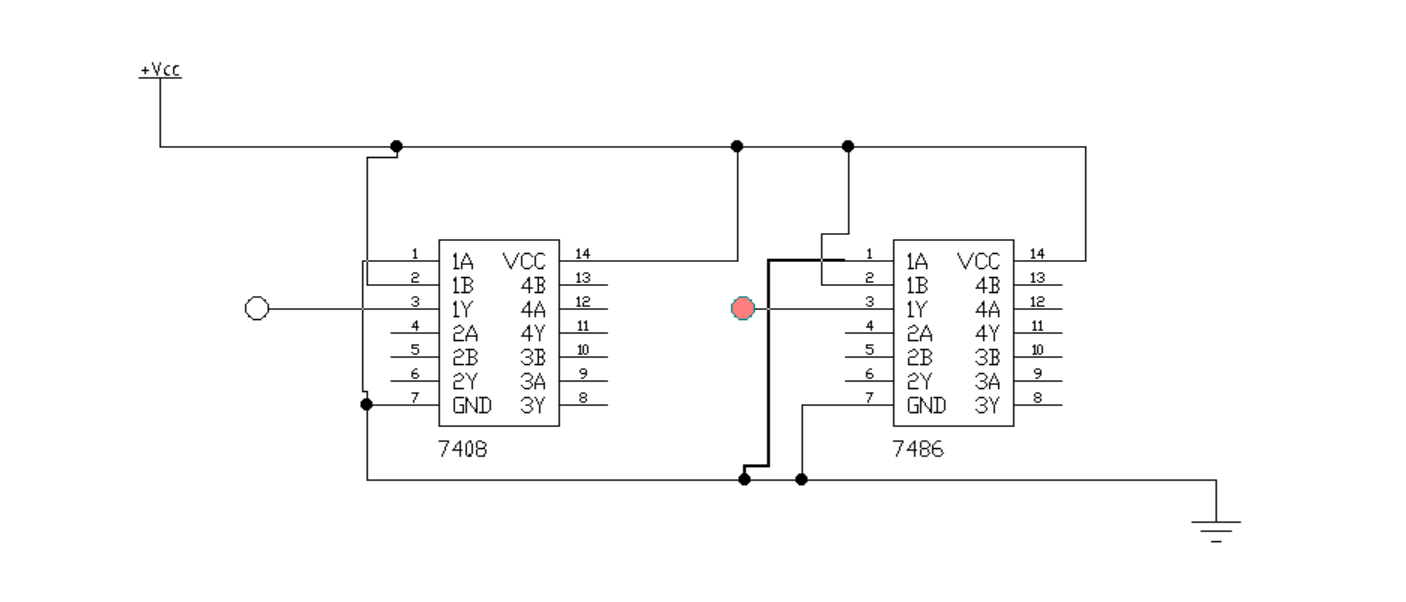
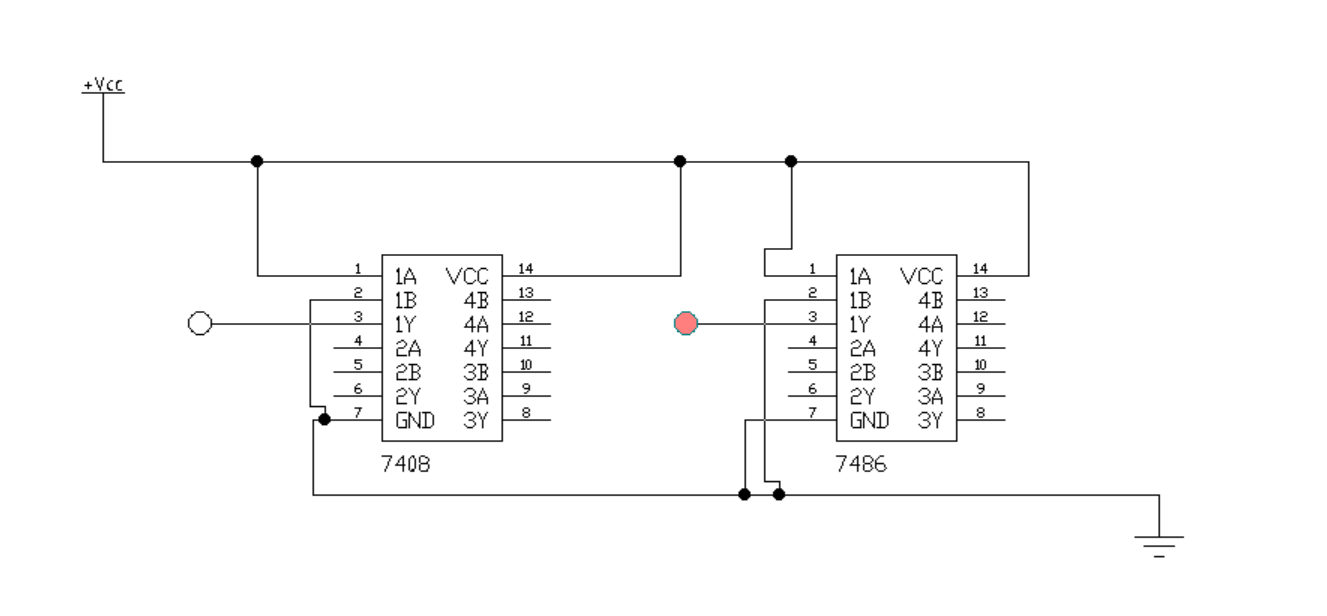
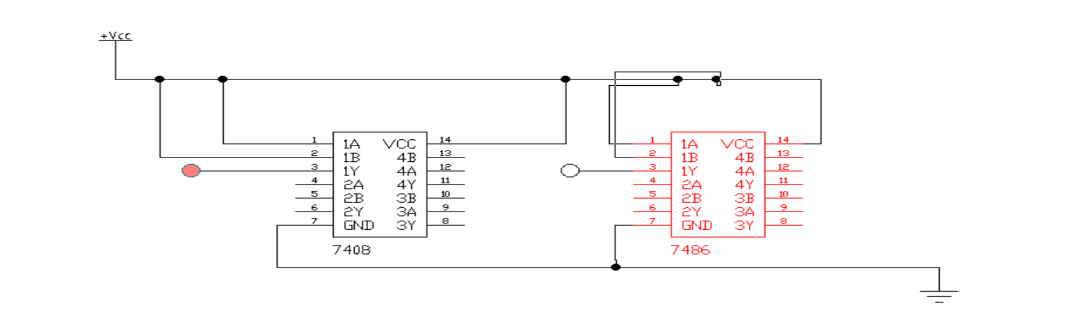
**Truth Table for Half Adder**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| A | B | A⊕B (Sum) | A·B (Carry) | Sum LED | Carry LED |
| 0 | 0 | 0 | 0 | OFF | OFF |
| 0 | 1 | 1 | 0 | ON | OFF |
| 1 | 0 | 1 | 0 | ON | OFF |
| 1 | 1 | 0 | 1 | OFF | ON |

**Explanation of LED States:**

* **When A=0, B=0** → Sum = 0, Carry = 0 → **Both LEDs OFF**



* **When A=0, B=1** or **A=1, B=0** → Sum = 1, Carry = 0 → **Sum LED ON**, Carry LED OFF
* **When A=1, B=1** → Sum = 0, Carry = 1 → **Sum LED OFF**, **Carry LED ON**
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**Conclusion:**

* The Half Adder circuit was successfully simulated.
* The **truth table** and the **LED outputs** from the circuit match the expected logical behavior of a Half Adder.
* Therefore, the circuit is working correctly and verifies the **functionality of binary addition using logic gates**.(Click on the picture)

