Subject: Computing Platforms on a Chip
Code: 32440
Institution: Escuela Politécnica Superior
Degree: Master's program in Research and Innovation in Information and Communications Technologies (RI^2CT)
Level: Master
Type: Elective [High-Performance Systems]
ECTS: 6

COURSE GUIDE: Computing Platforms on a Chip (CPC)

Academic year: 2012-2013

Program: Master's program in Research and Innovation in Information and Communications Technologies (RI^2CT)
Center: Escuela Politécnica Superior
University: Universidad Autónoma de Madrid

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1. ASIGNATURA / COURSE (ID)

Plataformas de Computación en un Chip
Computing Platforms on a Chip (CPC)

1.1. Programa / program

Máster Universitario en Investigación e Innovación en Tecnologías de la Información y las Comunicaciones (I^2-TIC)

Master's program in Research and Innovation in Information and Communications Technologies (RI^{2}CT) [Officially certified]

1.2. Course code

32440

1.3. Course areas

High-Performance Systems

1.4. Tipo de asignatura / Course type

Optativa [itinerario: Sistemas de Altas Prestaciones]
Elective [itinerary: High-Performance Systems]

1.5. Semester

Second semester

1.6. Credits

6 ETCS

1.7. Language of instruction

The lecture notes are in English. The lectures are in Spanish.

1.8. Recommendations / Related subjects

Basic knowledge of digital systems, computer architecture and FPGA design.

Related subjects are Advanced Reconfigurable Systems (it is advisable to enrol this course in order to gain experience in FPGA design), High-Performance Communication Systems, Algorithm Acceleration in Heterogeneous Systems.

1.9. Lecturers

Add @uam.es to all email addresses below.

Lectures and labs:

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1.10. Objetivos de la asignatura / Course objectives

Esta asignatura capacita al estudiante para abordar desarrollos de sistemas en un chip de altas prestaciones, que incluyan uno o varios microprocesadores, comunicaciones de alta velocidad y aceleración hardware. Como tecnología de referencia se emplearán dispositivos lógicos reconfigurables (FPGA), que ofrecen un compromiso adecuado entre capacidad de cálculo, coste y dificultad de desarrollo. La aproximación que se seguirá es mixta hardware/software, se enseñarán los modelos de programación que permiten aprovechar los elementos hardware que se presentan en esta asignatura.

This course provides the skills required to tackle development of high-performance systems-on-a-chip. These systems include one or many microprocessors, high-speed communications and hardware acceleration. The primary technology will be programmable logic devices (FPGA), since it provides an adequate compromise between computing power, cost, and development time. This course follows a mixed HW/SW approach: It presents the

programming models that allow users to utilize the different hardware elements that are being studied.

At the end of each unit, the student should be able to:

UNIT BY UNIT SPECIFIC OBJECTIVES	
UNIT 1.- Fundamentals	
2.1.	Understand what are the benefits and drawbacks of SoC technology
2.2.	Identify the right SoC technology for solving a given problem
2.3.	Know the design methodologies and programming models of SoCs
2.4.	Be able to design a simple FPGA-based SoC using platform-based design tools
2.5.	Be familiar with the basic building blocks of FPGA-based SoCs
2.6.	Know the fundamentals of programming for FPGA-based SoCs
2.7.	Know the basic HW and SW verification tools for FPGA-based SoCs
2.8.	Understand the basic concepts of design for reuse
2.9.	Know the bus infrastructure used in SoCs
2.10.	Be able to develop custom peripherals and integrate them into a platform-based tool
2.11.	Understand the fundamentals of driver development
UNIT 2.- Advanced design	
2.1.	Know the advanced building blocks of FPGA-based SoCs
2.2.	Understand what peripherals are available for hi-speed comms
2.3.	Be able to integrate a simple operating system
2.4.	Know advanced programming methodologies
2.5.	Know advanced HW and SW-level verification techniques
2.6.	Understand the fundamentals of HW/SW cosimulation tools
UNIT 3.- Performance enhancement techniques	
3.1.	Be able to use on-chip verification tools
3.2.	Know the different architectures of multiprocessor SoCs
3.3.	Understand the programming models of multiprocessor SoCs
3.4.	Be able to implement a simple multiprocessor system on a FPGA-based SoC
3.5.	Understand SW and HW-based acceleration techniques
3.6.	Know the different coprocessing techniques
3.7.	Be able to implement a custom coprocessor on a FPGA-based SoC

1.11. Course contents

PART I – Fundamentals of System-on-Chip

1. Introduction to System-on-Chip technologies
    a. Concept and usage models
    b. Fabrication technologies
    c. Design methodology

   d. Programming models
   e. Introduction to platform-based design

2. FPGA-based SoC (I)
   a. Development tools
   b. Basic building blocks
   c. Fundamentals of programming
   d. Basic HW and SW verification tools

3. Development of custom peripherals
   a. Design for reuse
   b. Bus infrastructure
   c. Integration of IP blocks in platform-based development tools
   d. Basic driver development

PART II – Advanced FPGA-based SoC design

4. FPGA-based SoC (II)
   a. Advanced building blocks
   b. Hi-speed communication peripherals
   c. Integration with operating system
   d. Advanced programming

5. Advanced Verification
   a. Advanced HW verification techniques: System-C, TLM
   b. Advanced SW verification techniques: Emulators
   c. HW/SW coverification tools
   d. On-chip verification tools

PART III – Performance enhancement techniques

6. Multiprocessor systems
   a. Architectures: symmetric vs. heterogeneous processing
   b. Programming model
   c. FPGA-based implementation

7. Acceleration techniques
   a. SW optimization techniques
   b. HW acceleration alternatives
   c. Coprocessing interfaces
   d. Design of custom coprocessors for FPGA-based systems

1.12. Course bibliography

1. "Computer System Design: System-on-Chip", Michael J. Flynn, Wayne Luk, Wiley 2011
2. "Processor Design: System-On-Chip Computing for ASICs and FPGAs", Jari Nurmi, Springer, 2007
3. "Multiprocessor system-on-chip hardware design and tool integration", Michael Hübner, Springer, 2011
4. "Reconfigurable system design and verification", Pao-Ann Hsiung, CRC Press, 2009
5. "SystemVerilog for verification a guide to learning the testbench language features 2nd ed.", Chris Spear, Springer, 2010
6. "Reuse Methodology Manual for System-On-A-Chip Designs", Michael Keating, Kluwer, 2002
7. "EDK Concepts, Tools, and Techniques", Xilinx Inc., 2011

1.13. Coursework and evaluation

The course involves lectures and exercises, which will be turned in by the student in the classroom, and a seminar presentation on the final project.

It will also include lab assignments and it is necessary to pass both practice and classroom exercises to pass the subject.

In the ordinary exam period, the evaluation will be made according to the following scheme:

- 30 % Classroom exercises and class participation
- 40 % Lab assignments
- 30 % Seminar presentation on the final project

In case of a fail grade in the ordinary exam period, in the extraordinary exam period, the student is required to:

- Turn in all the exercises with corrections
- Turn in all the lab assignments with corrections
- Turn in the final project

In the extraordinary exam period, evaluation will follow the same percentages as in the ordinary exam period.