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12.3.15

Cmsc 130
LE3

#2

State Table:

Current State			Input	Next State			Output
A	B	C	x	A_n	B_n	C_n	y
0	0	0	0	0	1	1	0
0	0	0	1	1	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	1	0	0	1
0	1	0	0	0	1	0	0
0	1	0	1	0	0	0	1
0	1	1	0	0	0	1	0
0	1	1	1	0	1	0	1
1	0	0	0	0	1	0	0
1	0	0	1	0	1	1	0

State Equations:

$A_{next} = A'B'x$
$B_{next} = A + C'x' + A'BCx$
$C_{next} = A'B'x' + Cx' + Ax$
$y = A'x$

#3

a. Minimum Possible Width for the AND-OR gate (PAL) : 4
b. Minimum Number of AND gates (PLA): 11