

Assignment #1

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2. 1)

By closely examining the I_D vs V_{GS} graph, we can observe that the current does not suddenly drop to zero at V_{TH} . Instead, there is a residual current beyond V_{TH} , which then decreases exponentially with further reduction in V_{GS} . At $V_{GS} = 0V$, a very small amount of current remains, known as the Off-Current of the device. Due to the small magnitude of this current, it is often plotted on a logarithmic scale for better clarity. On this scale, the plot becomes linear in the exponential region, and the slope of this line directly reflects the n-factor.

NMOS:

Normal scale

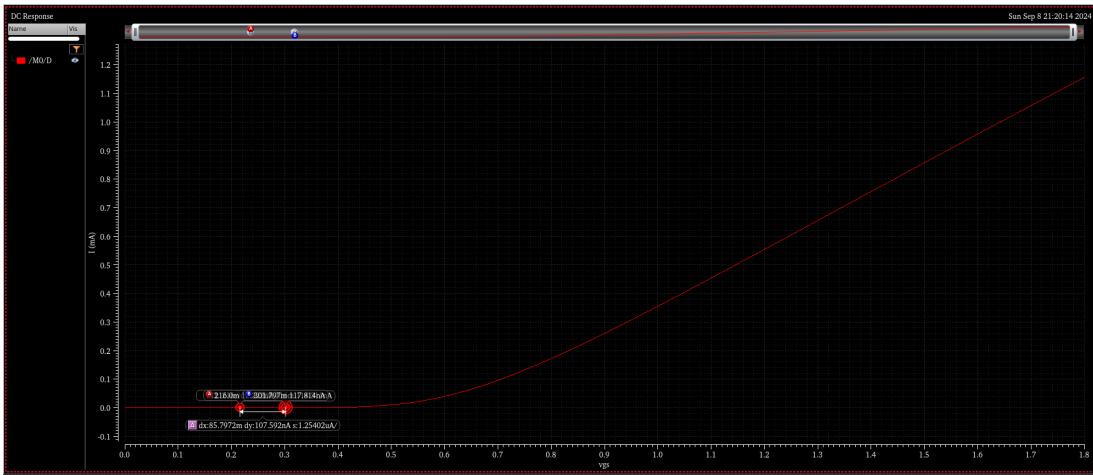


Fig. 1.

Log scale

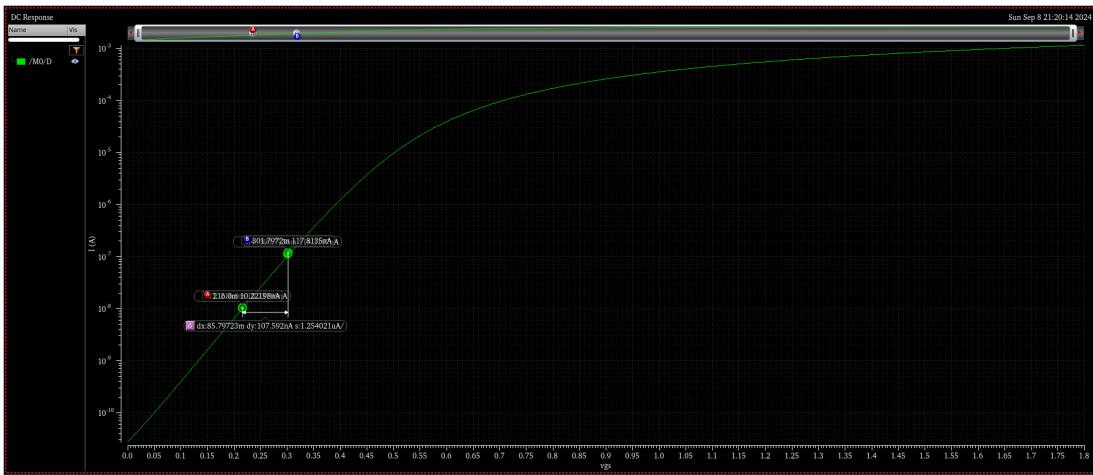


Fig. 2.

$$I_D = I_S \times e^{\frac{V_{GS}}{\eta V_T}} \times (1 - e^{\frac{-V_{DS}}{V_T}})$$

$$\log_{10} I_D = \frac{V_{GS}}{\eta V_T} \log_{10} e + \log_{10} I_C \text{ where, } I_C = I_S \cdot (1 - e^{\frac{-V_{DS}}{V_T}})$$

$$slope = \frac{1}{\eta V_T \ln 10}$$

$V_T = 25mV$ at $300K$

$$\frac{\log_{10} 10^{-7} - \log_{10} 10^{-8}}{85mV} = \frac{1}{\eta V_T \ln(10)}$$

$$\eta_{NMOS} = 1.453$$

PMOS:

Normal scale

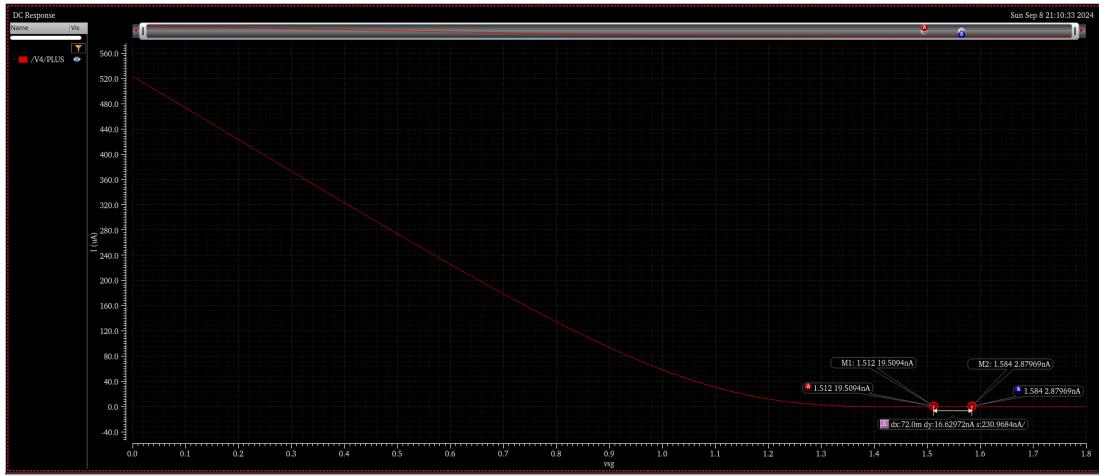


Fig. 3.

Log scale

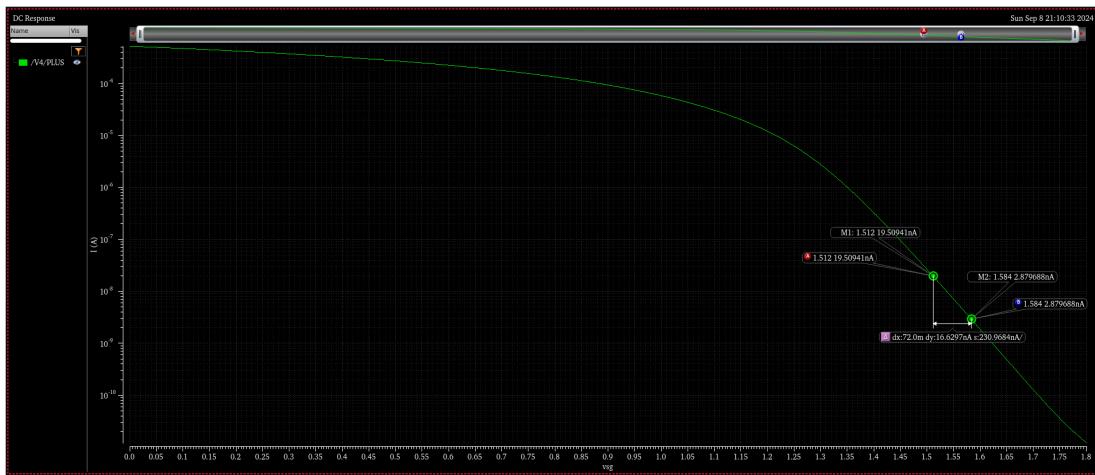
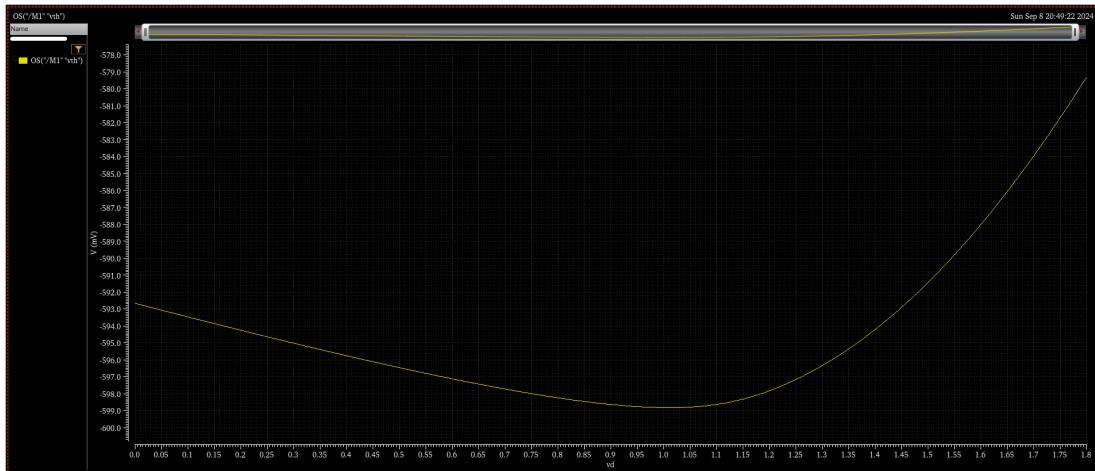


Fig. 4.

$$I_D = I_S \times e^{\frac{V_{GS}}{\eta V_T}} \times \left(1 - e^{\frac{-V_{DS}}{V_T}}\right)$$

2. 2)

Fig. 5. V_T vs V_{DS} For PMOS

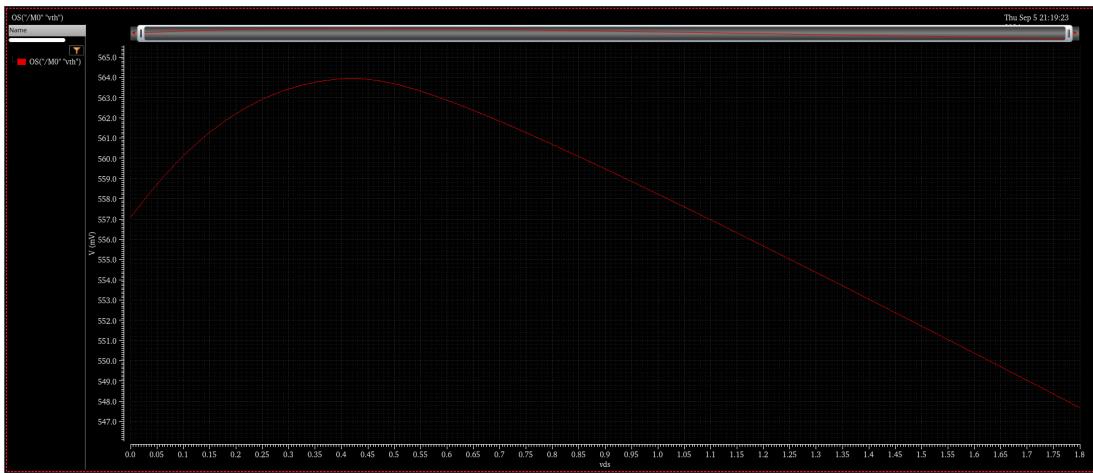
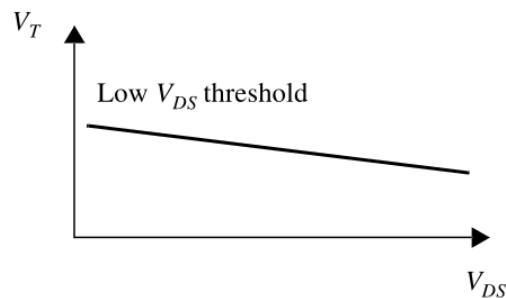
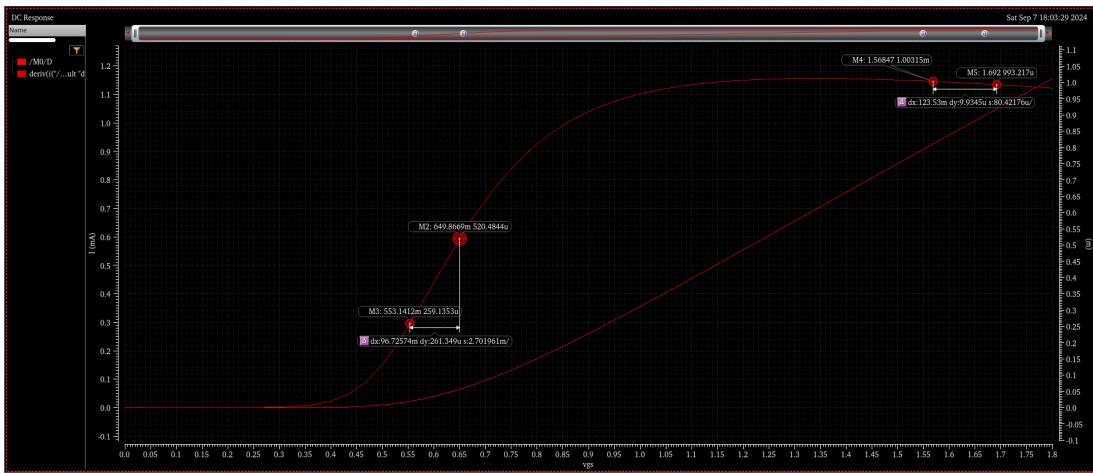
Fig. 6. V_T vs V_{DS} For NMOS(b) Drain-induced barrier lowering (for low L)

Fig. 7. Another figure

2. 3)

Following is the plot of $\frac{\partial I_D}{\partial V_{GS}}$ vs V_{GS} for NMOS (with I_D vs V_{GS})

Fig. 8. $\frac{\partial I_D}{\partial V_{GS}}$ vs V_{GS}

By extrapolating Linear and Quadratic region we observe that the boundary point for NMOS is at: $(0.827901V, 0.00103533A)$

Following is the plot of $\frac{\partial I_D}{\partial V_{GS}}$ vs V_{GS} for PMOS (with I_D vs V_{GS})

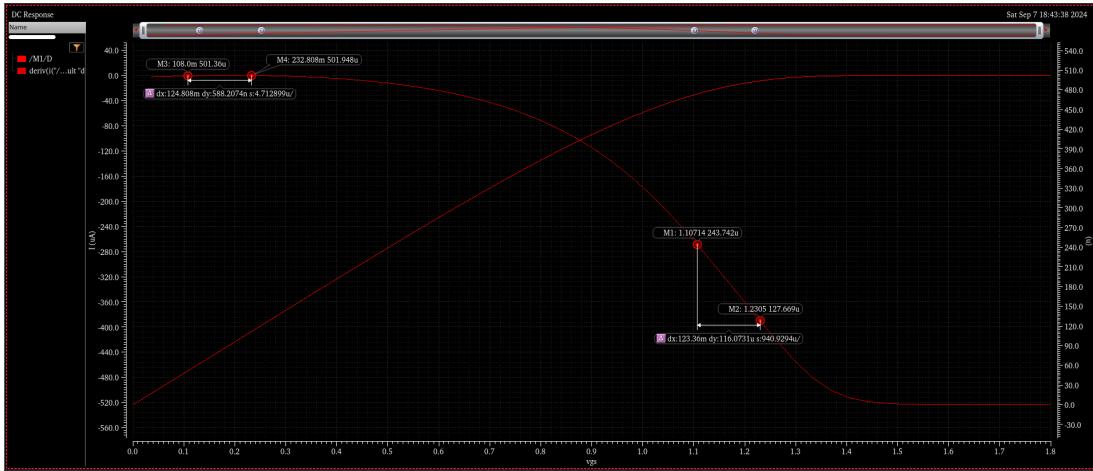


Fig. 9. $\frac{\partial I_D}{\partial V_{GS}}$ vs V_{GS}

By extrapolating Linear and Quadratic region we observe that the boundary point for NMOS is at: $(0.828544V, 0.00128277A)$

3(a) **NMOS:** The plots for I_D vs V_{DS} for $V_{GS} = \{2V_T, 3V_T, V_{DD}\}$ NMOS device:

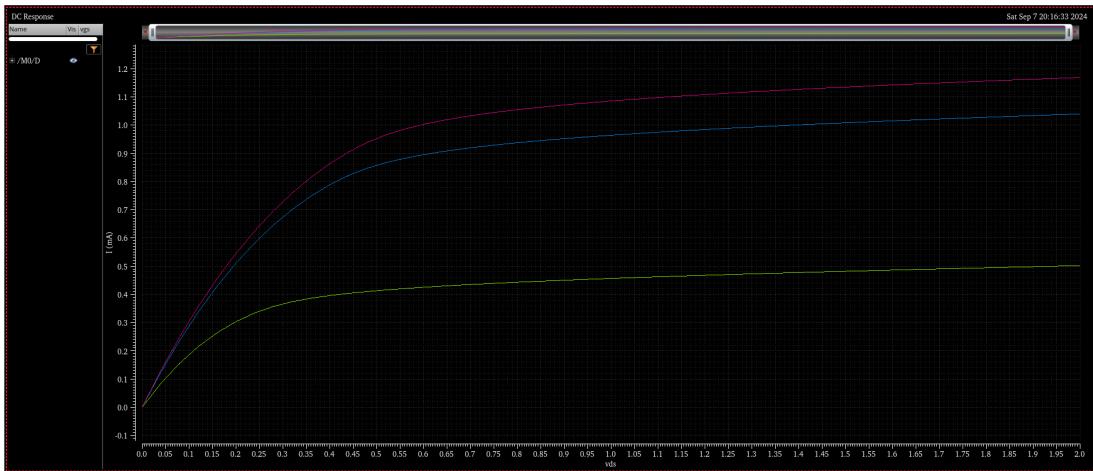


Fig. 10. ■ : $V_{GS} = 2V_T$; ■ : $V_{GS} = 3V_T$; ■ : $V_{GS} = V_{DD}$

3(b) **PMOS:** The plots for I_D vs V_{DS} for $V_{GS} = \{2V_T, 3V_T, V_{DD}\}$ PMOS device:

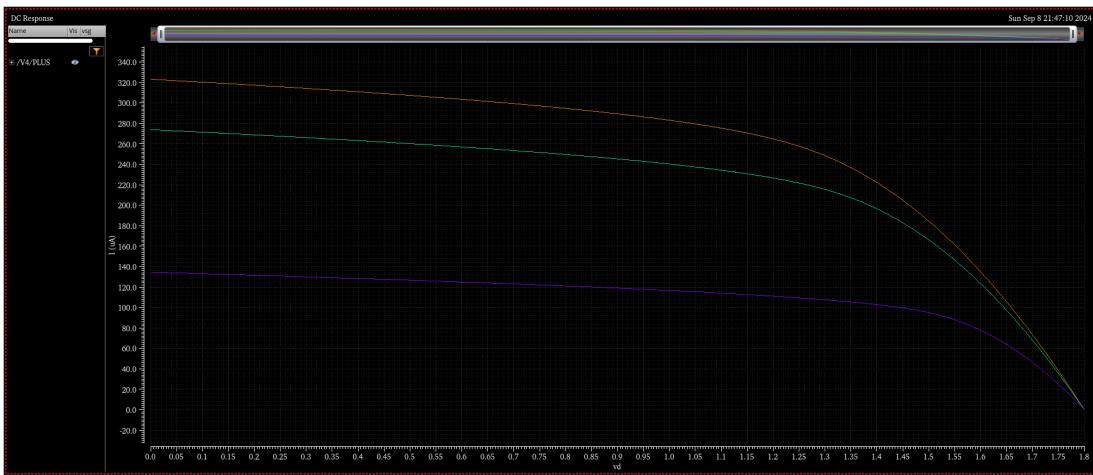


Fig. 11. ■ : $V_{GS} = 2V_T$; ■ : $V_{GS} = 3V_T$; ■ : $V_{GS} = V_{DD}$

5. 2) Given below is the plot of C_G vs V_{GS} for NMOS

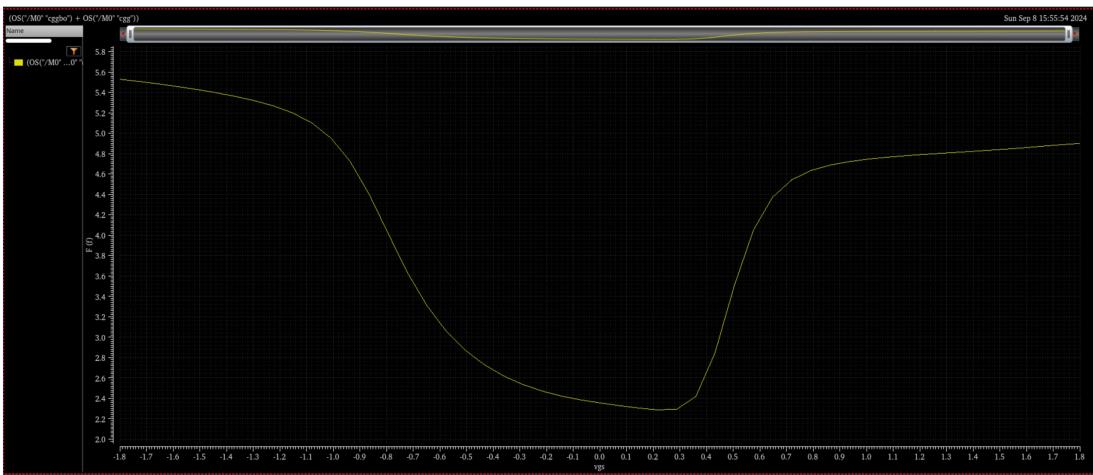


Fig. 12. C_G vs V_{GS} for NMOS; ■ : $C_{gg} + C_{ggbo}$

Given below is the plot of C_G vs V_{GS} for PMOS

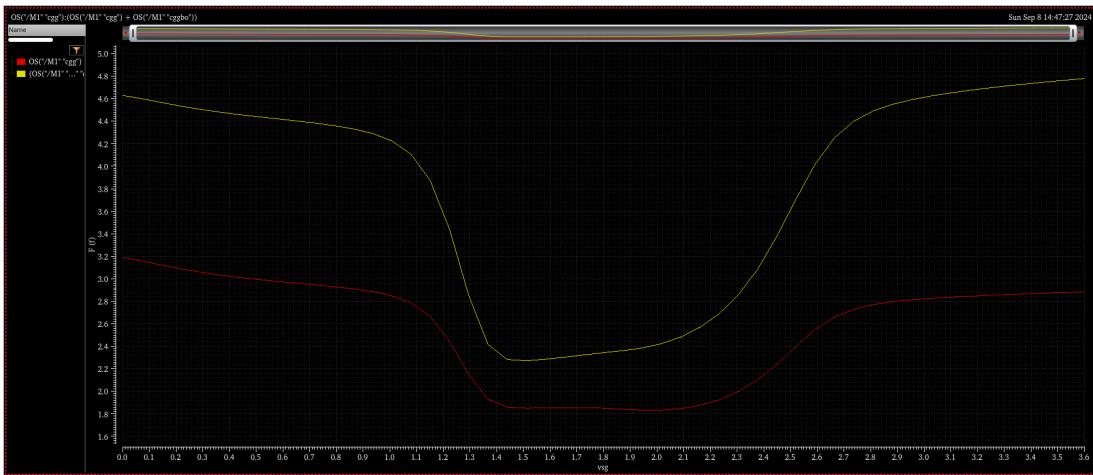


Fig. 13. C_G vs V_{GS} for PMOS; ■ : $C_{gg} + C_{ggbo}$, ■ : C_{gg}

5. 3) Given below is the plot of C_D vs V_{DS} for NMOS

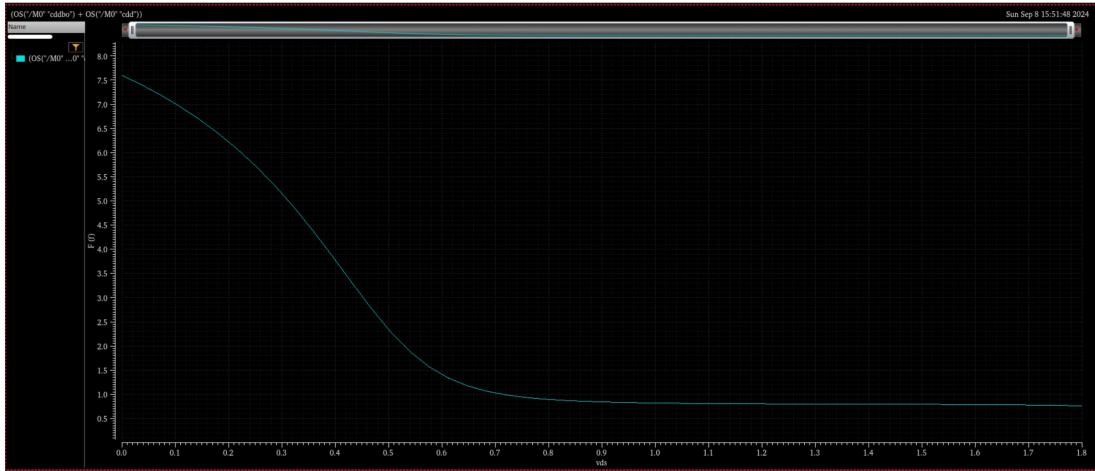


Fig. 14. C_D vs V_{DS} for NMOS; ■ : $C_{dd} + C_{ddbo}$

Given below is the plot of C_D vs V_{DS} for PMOS

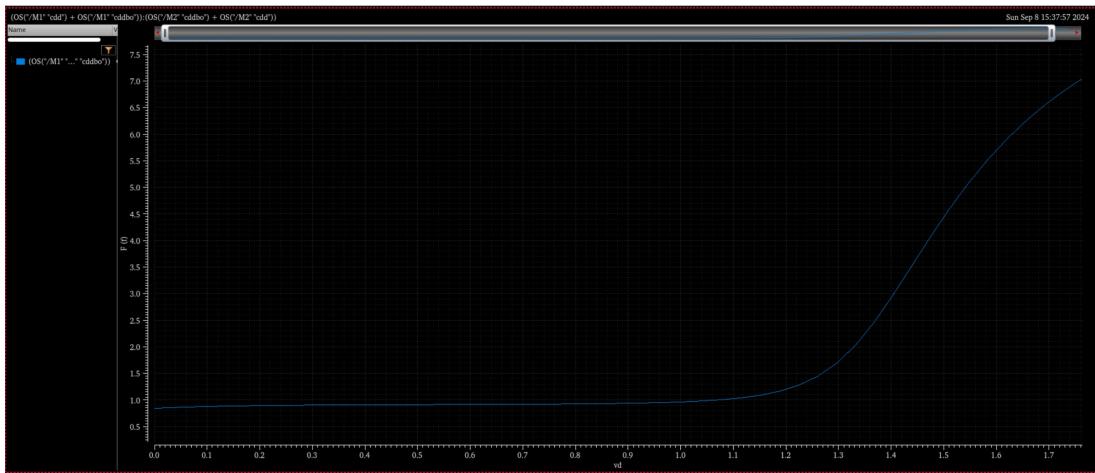


Fig. 15. C_D vs V_{DS} for PMOS; ■ : $C_{dd} + C_{ddbo}$