

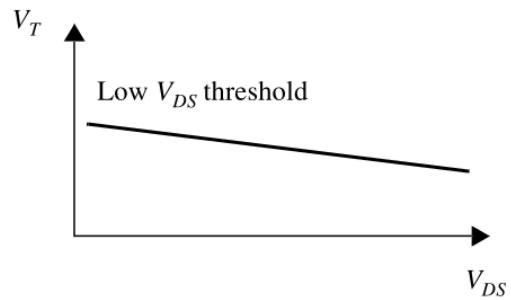
Assignment #1

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2. 2)



Fig. 1. V_T vs V_{DS}



(b) Drain-induced barrier lowering (for low L)

Fig. 2. Another figure

2. 3)

Following is the plot of $\frac{\partial I_D}{\partial V_{GS}}$ vs V_{GS} for NMOS (with log scale aswell)

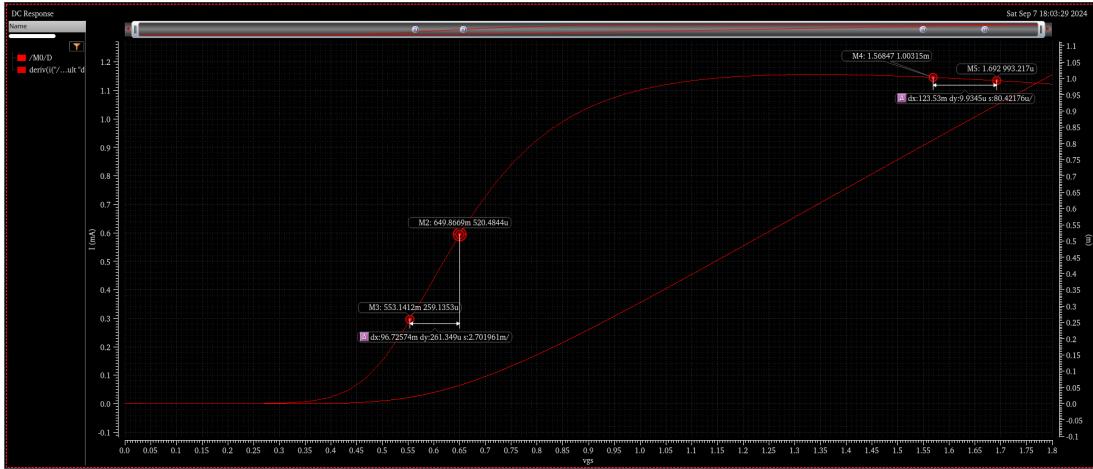


Fig. 3. $\frac{\partial I_D}{\partial V_{GS}}$

By extrapolating Linear and Quadratic region we observe that the boundary point for NMOS is at:
(0.827901V, 0.00103533A)

Following is the plot of $\frac{\partial I_D}{\partial V_{GS}}$ vs V_{GS} for PMOS

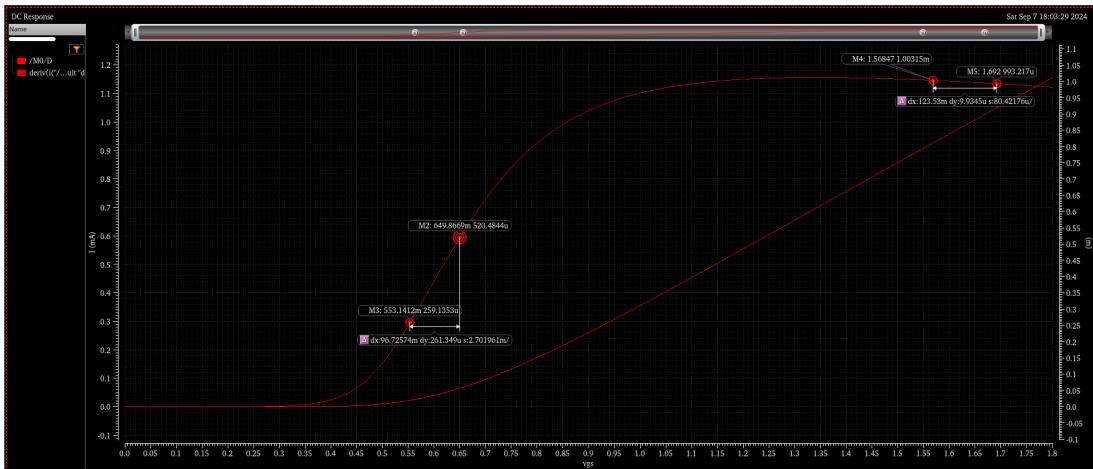


Fig. 4. $\frac{\partial I_D}{\partial V_{GS}}$

By extrapolating Linear and Quadratic region we observe that the boundary point for NMOS is at:
(0.827901V, 0.00103533A)

3(a) NMOS: The plots for I_D vs V_{DS} for $V_{GS} = \{2V_T, 3V_T, V_{DD}\}$ NMOS device:

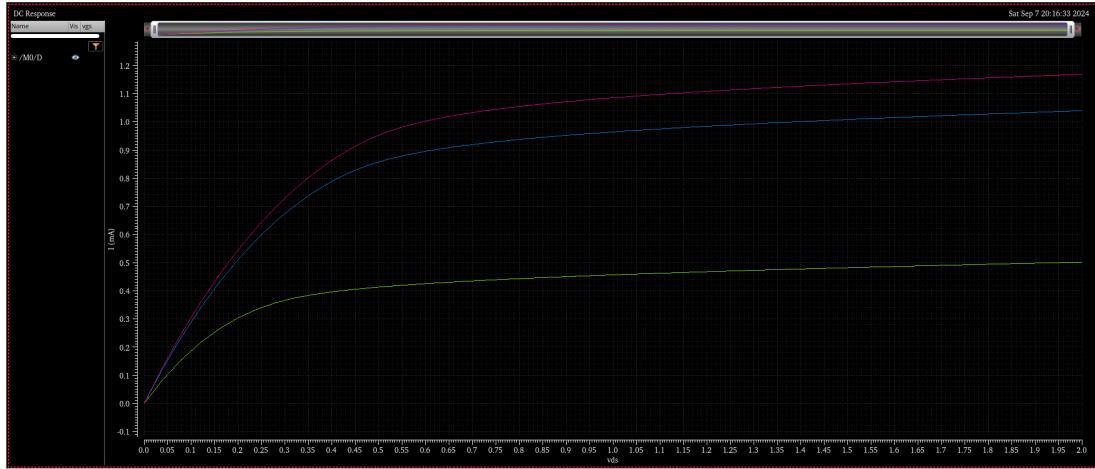


Fig. 5. █ : $V_{GS} = 2V_T$; █ : $V_{GS} = 3V_T$; █ : $V_{GS} = V_{DD}$

5. 2) Given below is the plot of C_G vs V_{GS} for NMOS

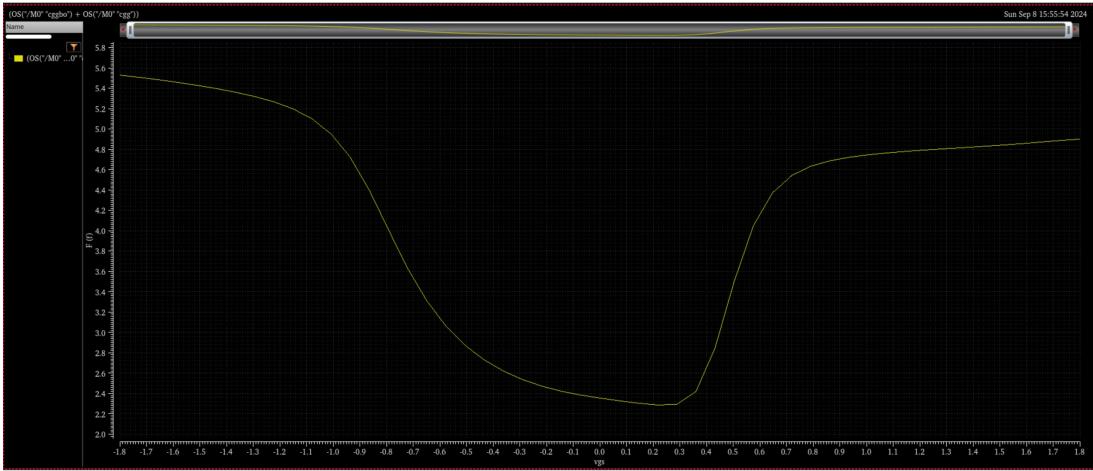


Fig. 6. C_G vs V_{GS} for NMOS; ■ : $C_{gg} + C_{ggb0}$

Given below is the plot of C_G vs V_{GS} for PMOS

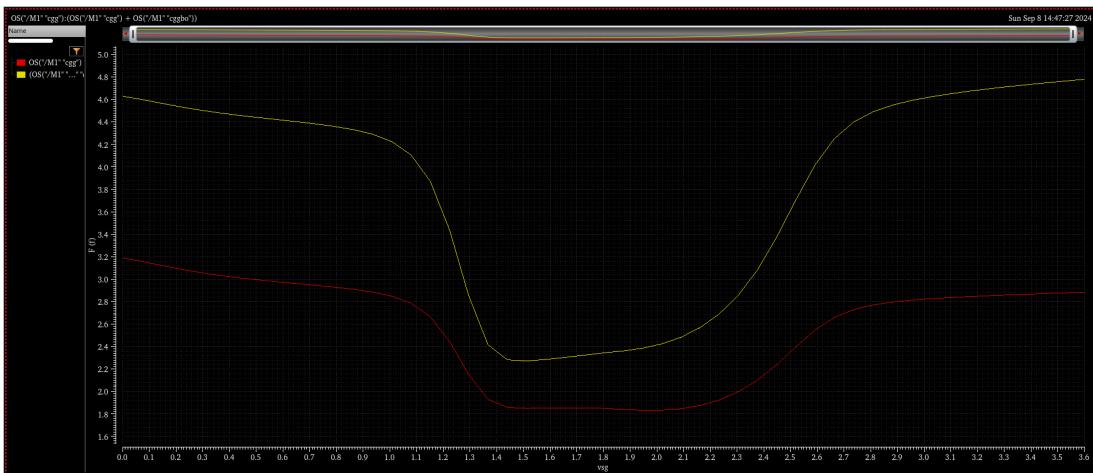


Fig. 7. C_G vs V_{GS} for PMOS; ■ : $C_{gg} + C_{ggb0}$, ■ : C_{gg}

5. 3) Given below is the plot of C_D vs V_{DS} for NMOS

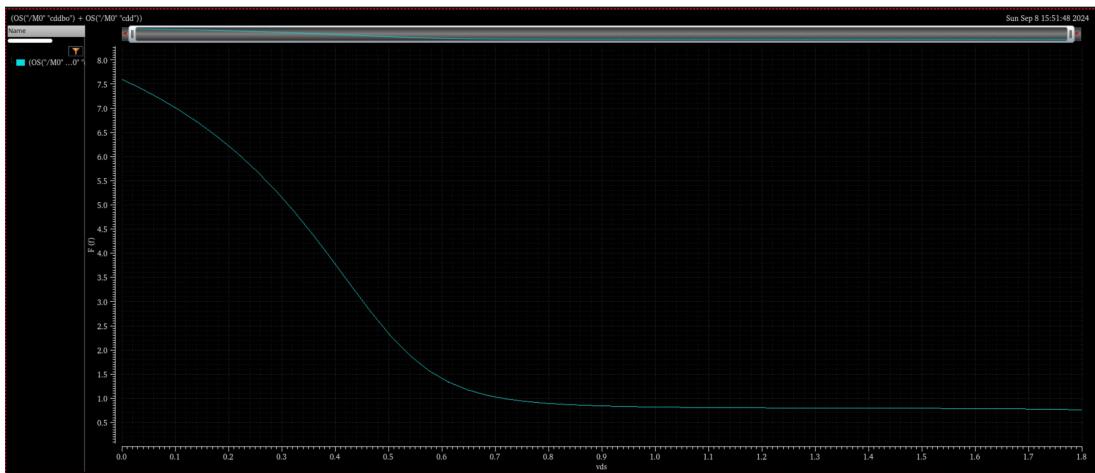


Fig. 8. C_D vs V_{DS} for NMOS; ■ : $C_{dd} + C_{ddbo}$

Given below is the plot of C_D vs V_{DS} for PMOS

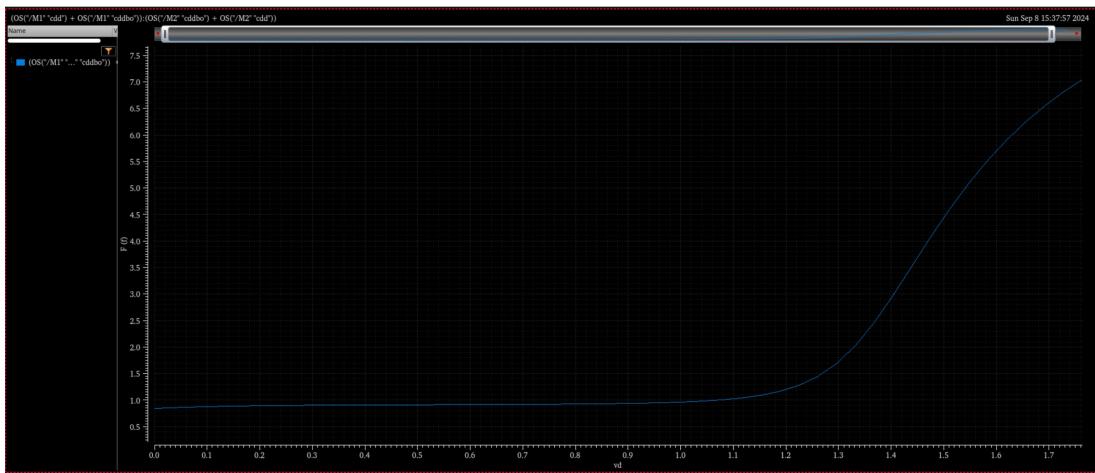


Fig. 9. C_D vs V_{DS} for PMOS; ■ : $C_{dd} + C_{ddbo}$