Description

The AT8236 is a DC brush motor driver capable of bi-directional motor control at peak currents of up to 6A. Using the current decay mode, the motor speed can be controlled by pulse-width modulation (PWM) of the input signal, and a low-power sleep mode is available.

The AT8236 integrates a synchronous rectification function to significantly reduce system power requirements.

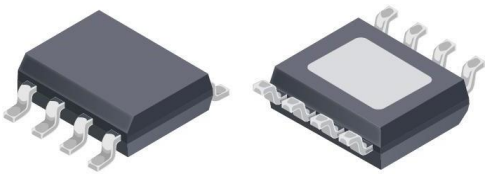
The internal protection functions include over-current protection, short-circuit protection, undervoltage lockout, and over-temperature protection.

The AT8236 offers an ESOP8 package with exposed pads for improved thermal performance and is lead-free to meet environmental standards.

Features

- Single Channel H-Bridge Motor Driver
- Wide voltage power supply, 5.5V-36V
- Low $R_{DS(ON)}$ resistance, 200mΩ (HS+LS)
- 6A peak drive output, 4A continuous drive output
- PWM control interface
- Supports low-power sleep mode

Package form



ESOP8

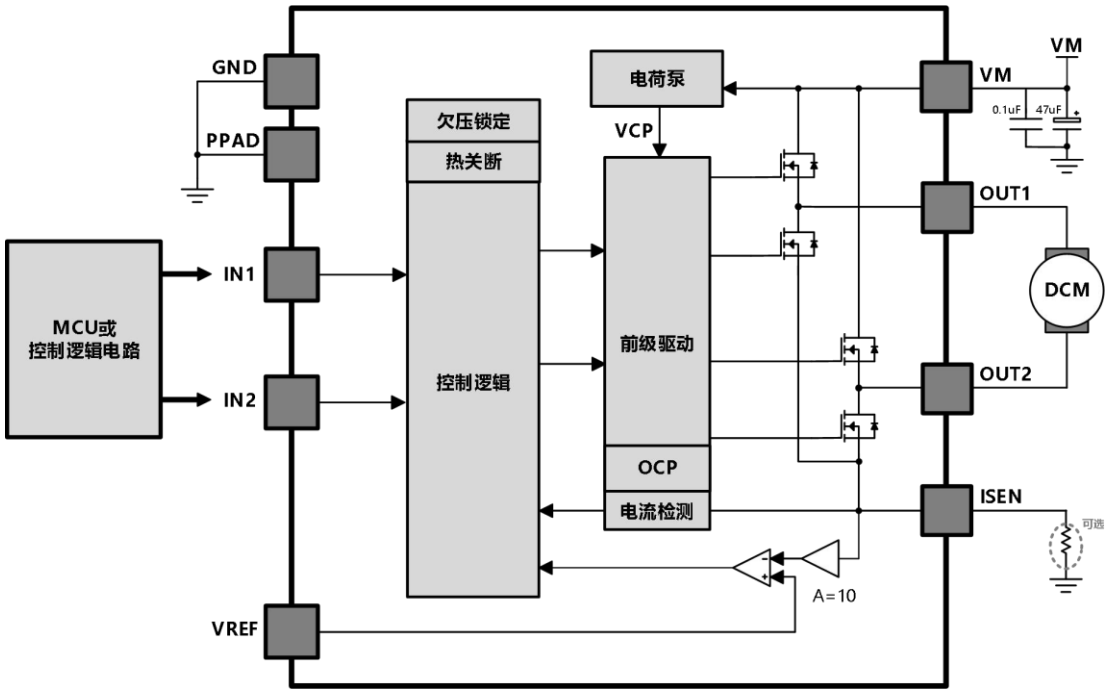
Applications

- Printers and office automation equipment
- Electrical
- Smart Home
- Industrial Control

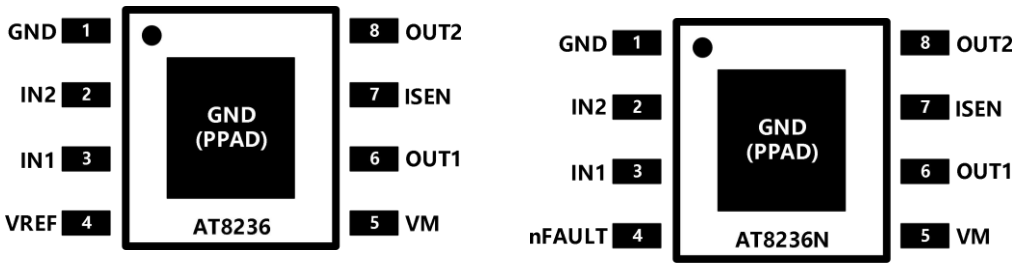
Model selection

Order Model	Package	Packaging Information
AT8236	ESOP8	Braided tape, 4000pcs/pan
AT8236N	ESOP8	Braided tape, 4000pcs/pan

Typical application schematic



Pin Definition



Pin List

Pin Name	Pin Number	Pin Definition	Peripheral Components and Connections
Power and Ground			
GND	1	Chip Land	GND pin and chip bare pad to power ground
PPAD	-		
VM	5	Chip Power	Chip power supply and motor power supply, need to do a good job of power filtering
Control Logic			
IN1	3	Logic input	Control H-bridge output state, built-in pull-down resistor
IN2	2		
VREF	4	Reference voltage input (8236)	Reference voltage input to set the peak drive current
nFAULT		Fault detection output (8236N)	Open-drain output, using external pull-up resistor. When overcurrent, overtemperature, or undervoltage, nFAULT will be pulled low
ISEN	7	H-bridge Check current input/ground	H-bridge current check terminal, connect current check resistor to ground, if no current limit is needed, ground directly
Power Output			
OUT1	6	H-bridge output 1	H-bridge output. Define the forward current as OUT1 → OUT2
OUT2	8	H-bridge output 2	

Circuit operating limit at $T_A = 25°C$

Parameters	Symbols	Conditions	Scope	Unit
Power Supplies	VM		-0.3 - 40	V
Peak Output Current	IPEAK		±6	A
Logic input voltage	VIN		-0.7 to 7	V
Sense Voltage	VSENSE		-0.3 to 0.5	V
Operating temperature	TA	Range S	-40 to 85	°C
Maximum junction temperature	T_J(max)		150	°C
Storage temperature	Tstg		-55 to 150	°C

Thermal resistance characteristics at $T_A = 25°C$

Heat meteri ng	ESOP 8PINS	Unit
θ_{JA} - Silicon core to environment thermal resistance coefficient(*)	35	°C/W

(*) The thermal resistance coefficients from the silicon core to the environment under natural convection conditions were obtained by simulating on a JEDEC standard high K-value board as specified in JESD51-7, under the following environmental conditions

described in JESD51-2a.

Recommended operating conditions at TA= 25°C

Parameters	Symbols	Minimum	Typical	Maximum	Unit
Power Supplies	VM	5.5	-	36	V
Continuous output current	IOUT	0	-	3	A
Peak output current	IPEAK	0	-	4.5	A
Logic input voltage	VIN	0	-	5.25	V
Logic input frequency	fPWM	0	-	100	kHZ
Reference Voltage	VREF	0.5	-	4	V

(*) When the chip is working with high current, the chip needs to be dissipated well.

Electrical characteristics at T_A = 25°C, V_M = 24 V

Parameters		Test conditions	Minimum	Typical	Maximum	Unit
Power supply						
IVM	VM Static operating current	f_{PWM} < 50 kHz	-	4.5	6	mA
IVMQ	VM Sleeping Current	IN1 = IN2 = 0 V	-	20	30	uA
VUVLO	VM undervoltage lockout value	VM Up	-	4.7	5.0	V
VHYS	VM undervoltage hysteresis		-	300	-	mV
Logic input						
VIL	Logic input low voltage		-	0.5	0.7	V
VIH	Logic input high voltage		1.5	-	5.25	V
VHYS	Logic input hysteresis		-	0.2	-	V
IIL	Logic input current_low level	V_{IN} = 0 V	-0.2	-	0.2	uA
IIH	Logic input current_high	V_{IN} = 3.3 V	-	33	100	uA
Rpd	Input internal pull-down resistor	Other	-	100	-	kΩ
tSLEEP	Delay in entering SLEEP state		-	0.7	1.0	ms
H Bridge FETs						
RDS(ON)	High-side + low-side FET resistance	I_O = 1A, T_J = 25°C	-	200	-	mΩ
IOFF	Output shutdown leakage current		-1	-	1	uA
Driver Circuit Timing and Current Configuration						
tOFF	Current decay time	Internal PWM fixed shutdown time	-	23	-	us
tR	Rise time	V_M =24V, 24Ω to GND, 20% to 80%	-	150	-	ns
tF	Descent time	V_M =24V, 24Ω to GND, 20% to 80%	-	150	-	ns
tDEAD	Dead time		-	250	-	ns
AISEN	ISEN Current Gain		-	10	-	V/V
tBLANK	Fade time		-	2.2	-	us
Protection Circuit						
IOCP	Overcurrent Threshold		6	7	10	A

TOCP	Overcurrent restart time		-	3	-	ms
TSD	Over Temperature Threshold	Knot temperature	140	150	160	℃
THYS	Overtemperature hysteresis		-	30	-	℃

Module Function Description

H-bridge control

The input pins IN1 and IN2 control the output state of the H-bridge. The following table shows the logical relationship between the inputs and outputs.

IN1	IN2	OUT1	OUT2	Function
0	0	Z	Z	Coasting, dormant
1	0	H	L	Positive
0	1	L	H	Reverse
1	1	L	L	Brakes

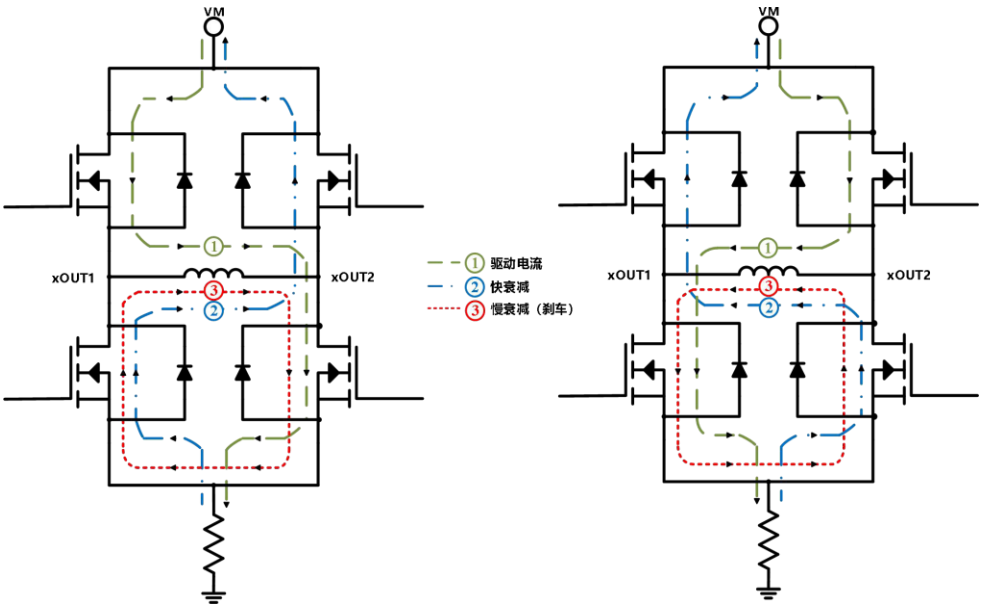
H-bridge control logic table

When using PWM control for the speed control function, the H-bridge can operate in two different states, fast decay or slow decay. In the fast decay mode, the H-bridge is disabled and the renewal current flows through the body diode; in the slow decay mode, both lower tubes of the output H-bridge are open.

IN1	IN2	Function
PWM	0	Positive rotation PWM, fast decay
1	PWM	Positive rotation PWM, slow decay
0	PWM	Inverted PWM, Fast Decay
PWM	1	Reverse PWM, slow decay

Function logic table

The figure below shows the current path in different drive and attenuation modes.



Drive and decay modes

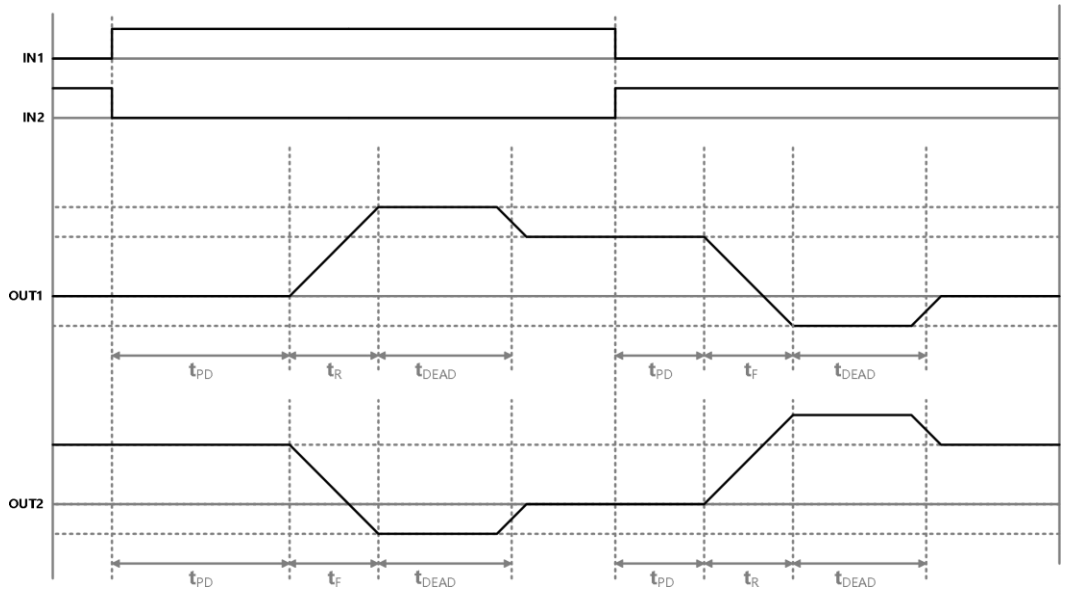
Current control

When an H-bridge is enabled, the current flowing through the corresponding bridge arm rises, and when the current reaches a set threshold, the driver output turns off until the next PWM cycle begins. Note that the voltage on the ISEN pin is ignored at the moment the H-bridge is enabled, and a fixed time elapses before the current detection circuit is enabled. This fading time is typically fixed at 2.2us. This fading time also determines the minimum PWM time when the operating current is decaying. The PWM target current is determined by the comparator comparing the voltage across the current sense resistor connected to the ISEN pin multiplied by a factor of 10 and a reference The reference voltage of the AT8236 is input through the VREF pin, while the AT8236N has an internal fixed $_{VREF}$ voltage of 3.3 V. The following equation calculates the target current for 100%.

$$I_{TRIP}(A) = \frac{V_{REF}(V)}{A_V R_{ISEN}(\Omega)} \quad \frac{V_{REF}(V)}{10\, R_{ISEN}(\Omega)}$$

Dead time

When the output goes from high to low, or from low to high, there is a dead time to prevent the upper and lower tubes from conducting at the same time. During the dead time, the output is a high resistance state. When the dead time needs to be measured on the output, it needs to be measured according to the current direction of the corresponding pin at that time. If the current is flowing out of the pin, the voltage at the output is one diode drop below the ground level; if the current is flowing into the pin, the voltage at the output is one diode drop above the supply voltage VM.



Time parame ters

Sleep mode

When IN1 and IN2 are both low and maintained for more than 1ms, the device will enter the hibernation mode, thus significantly reducing the power consumption of the device at idle. After entering sleep mode, the H-bridge of the device is disabled and the charge pump circuit stops operating. When IN1 or IN2 flips high and stays high for at least 5us, the chip will return to normal operation after a delay of about 1ms.

Overcurrent Protection (OCP)

When the current flowing through the output tube exceeds the overcurrent threshold, the chip output

turns OFF. After 3ms, the chip will try to restart and return to normal.

Over Temperature Protection (TSD)

If the junction temperature exceeds the safety limit threshold, the FET of the H-bridge is disabled. Once the junction temperature drops to a safe level, all operations automatically return to normal.

Under voltage lockout protection (UVLO)

If the voltage on the VM pin drops below the undervoltage lockout threshold, the output is disabled and the internal logic is reset. When the voltage on the VM rises to V_{UVLO} above, the circuit resumes normal operation.

PCB layout suggestions

The PCB should be overlaid with a large heatsink and the ground connection should have a wide ground overlay. In order to optimize the electrical and thermal parameters of the circuit, the chip should be directly attached to the heatsink.

For the power supply VM, an electrolytic capacitor of not less than 47uF should be connected for ground coupling, and the capacitor should be placed as close as possible to the device.

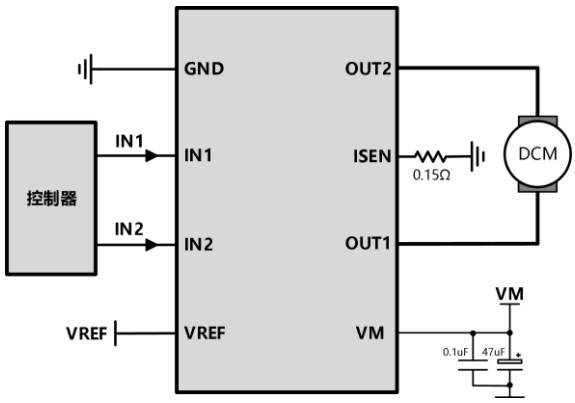
In order to avoid capacitive coupling problems caused by high-speed dv/dt conversion, the circuit cladding at the output of the driver circuit should be kept away from the cladding at the logic control input.

The logic control leads should be aligned with low impedance to reduce noise caused by thermal resistance.

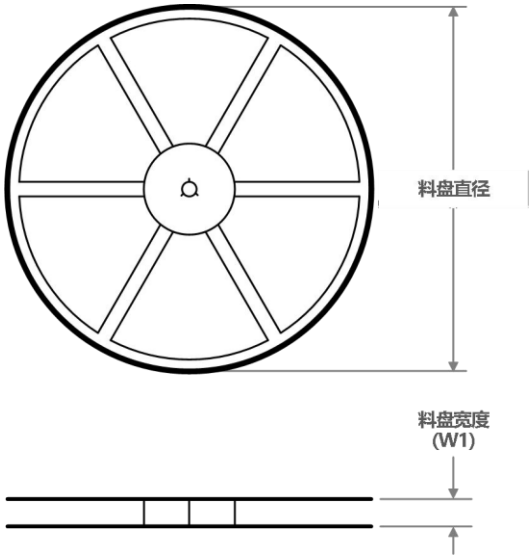
Typical application examples

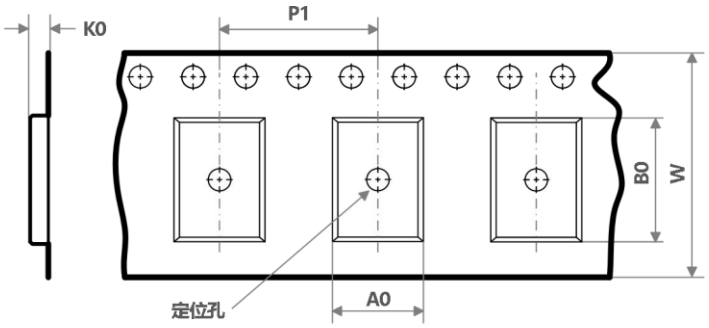
Examples of application schematics for specific operating conditions are given below.

VIN	24V
IOUT	2A
VREF	3.0V



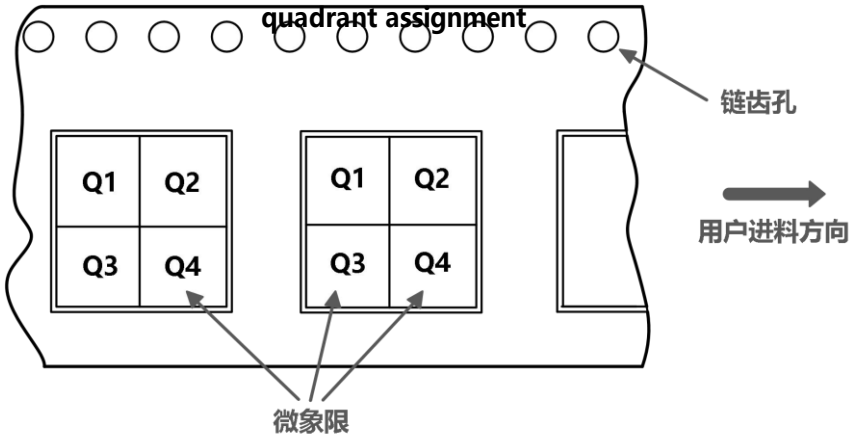
Taping material reel information





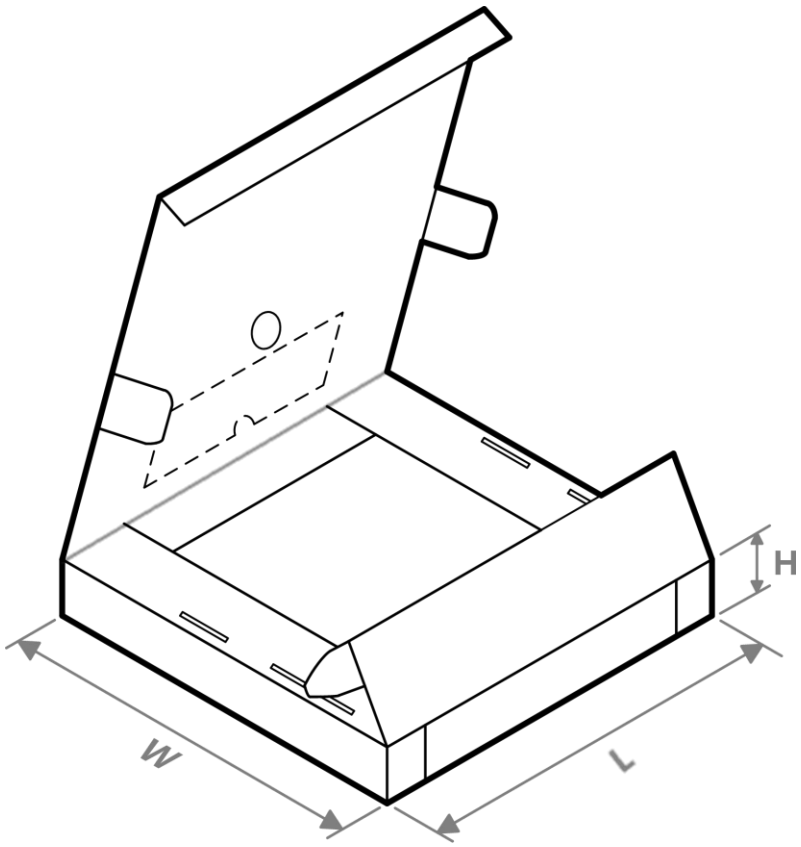
A0	Width of trough
B0	Tank length
K0	Thickness of trough
W	Overall width of carrier belt
P1	Distance between adjacent slot centers

Braiding PIN1 Azimuth quadrant assignment



Components	Package Type	Package identification	Number of Pins	SPQ	Diameter of material tray (mm)	Tray width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 quadrant
AT8236	ESOP	-	8	4000	330	12	6.55	5.2	2	8	12	Q1

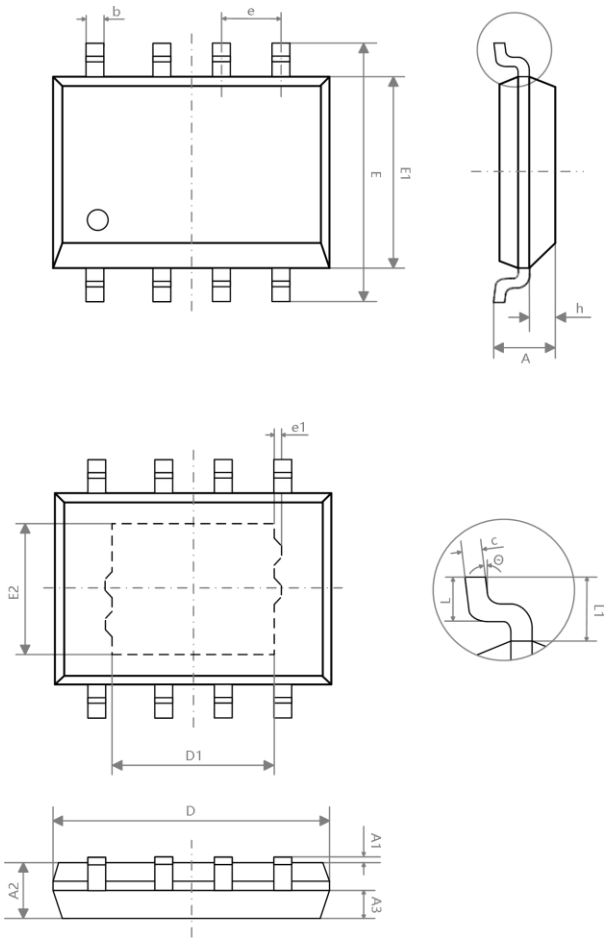
Taping reel package size



Components	Package Type	Package identification	Number of Pins	SPQ	Length(mm)	Width(mm)	Height(mm)
AT8236	ESOP	-	8	4000	400	343	60

Package Information

ESOP8



Symbols	mm(mm)		
	Minimum	Typical	Maximum
A	--	--	1.65
A1	0.05	--	0.15
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	--	0.47
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 (BSC)		
h	0.25	--	0.50
L	0.50	0.60	0.80
L1	1.05(REF)		
θ	0	--	8°
e1	0.10(REF)		
D1	3.10 (REF)		
E2	2.21 (REF)		