

# SN54HC164, SN74HC164 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

SCLS115B – DECEMBER 1982 – REVISED MAY 1997

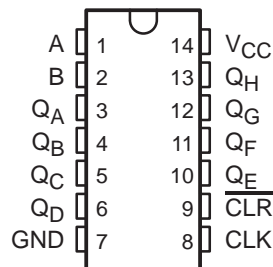
- AND-Gated (Enable/Disable) Serial Inputs
- Fully Buffered Clock and Serial Inputs
- Direct Clear
- Package Options Include Plastic Small-Outline (D) and Ceramic Flat (W) Packages, Ceramic Chip Carriers (FK), and Standard Plastic (N) and Ceramic (J) 300-mil DIPs

## description

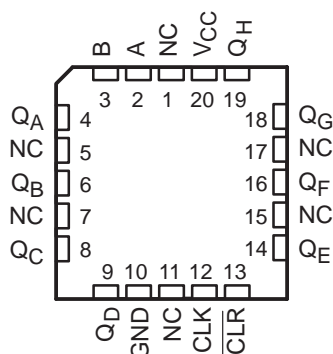
These 8-bit shift registers feature AND-gated serial inputs and an asynchronous clear ( $\overline{\text{CLR}}$ ) input. The gated serial (A and B) inputs permit complete control over incoming data; a low at either input inhibits entry of the new data and resets the first flip-flop to the low level at the next clock (CLK) pulse. A high-level input enables the other input, which then determines the state of the first flip-flop. Data at the serial inputs can be changed while CLK is high or low, provided the minimum setup time requirements are met. Clocking occurs on the low-to-high-level transition of CLK.

The SN54HC164 is characterized for operation over the full military temperature range of  $-55^{\circ}\text{C}$  to  $125^{\circ}\text{C}$ . The SN74HC164 is characterized for operation from  $-40^{\circ}\text{C}$  to  $85^{\circ}\text{C}$ .

SN54HC164 . . . J OR W PACKAGE  
SN74HC164 . . . D OR N PACKAGE  
(TOP VIEW)



SN54HC164 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

FUNCTION TABLE

INPUTS				OUTPUTS		
$\overline{\text{CLR}}$	CLK	A	B	$Q_A$	$Q_B \dots Q_H$	
L	X	X	X	L	L	L
H	L	X	X	$Q_{A0}$	$Q_{B0}$	$Q_{H0}$
H	$\uparrow$	H	H	H	$Q_{An}$	$Q_{Gn}$
H	$\uparrow$	L	X	L	$Q_{An}$	$Q_{Gn}$
H	$\uparrow$	X	L	L	$Q_{An}$	$Q_{Gn}$

$Q_{A0}$ ,  $Q_{B0}$ ,  $Q_{H0}$  = the level of  $Q_A$ ,  $Q_B$ , or  $Q_H$ , respectively, before the indicated steady-state input conditions were established

$Q_{An}$ ,  $Q_{Gn}$  = the level of  $Q_A$  or  $Q_G$  before the most recent  $\uparrow$  transition of CLK; indicates a 1-bit shift



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**TEXAS  
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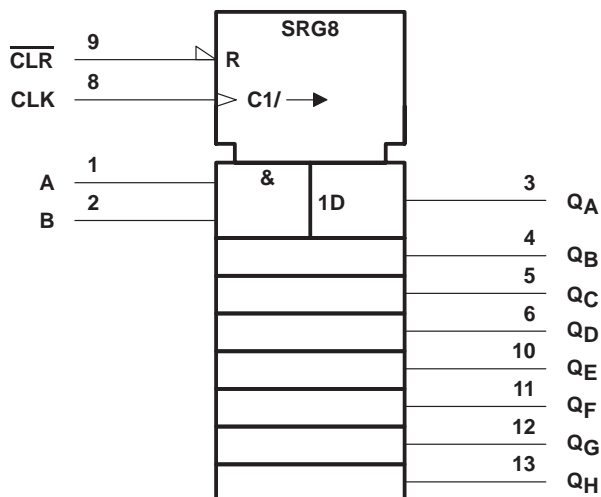
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# SN54HC164, SN74HC164

## 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

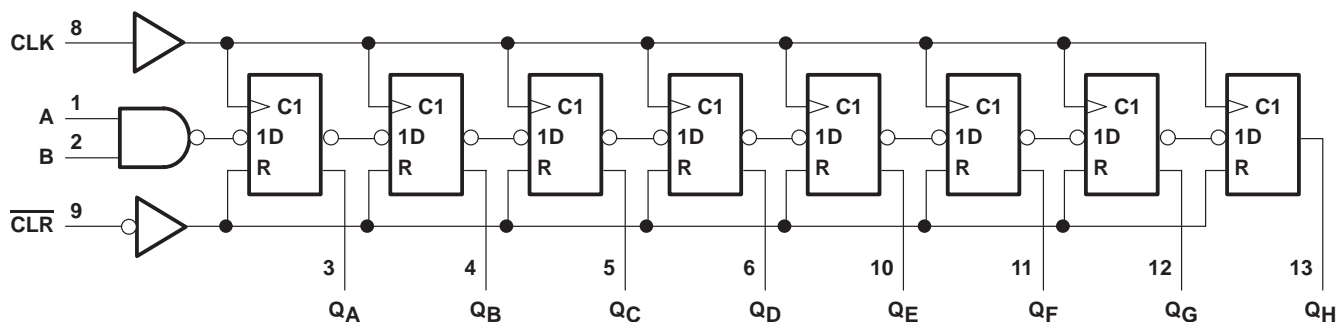
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### logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.  
Pin numbers shown are for the D, J, N, and W packages.

### logic diagram (positive logic)

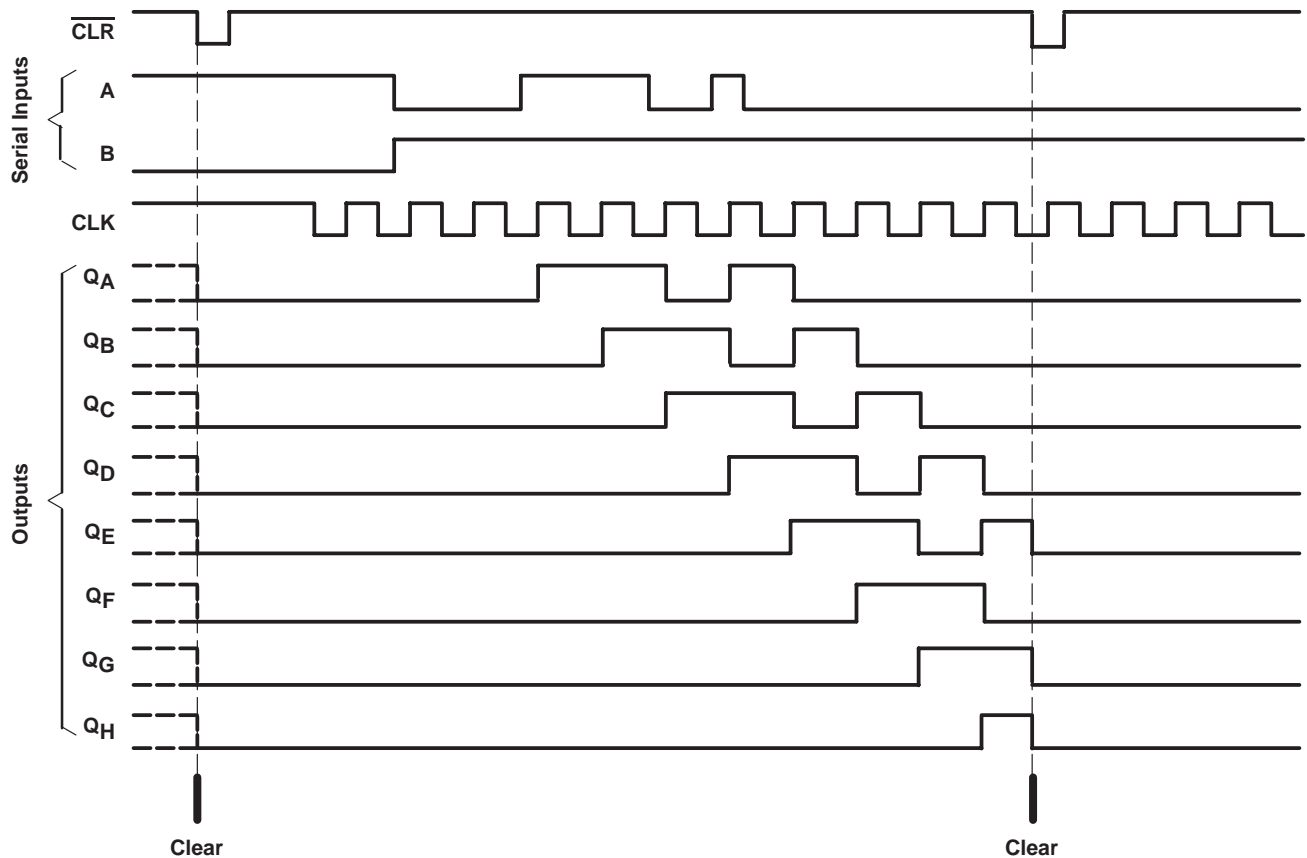


Pin numbers shown are for the D, J, N, and W packages.

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## typical clear, shift, and clear sequence



## absolute maximum ratings over operating free-air temperature range†

Supply voltage range, $V_{CC}$	–0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	127°C/W
N package	78°C/W
Storage temperature range, $T_{stg}$	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
  2. The package thermal impedance is calculated in accordance with JEDEC 51, except for through-hole packages, which use a trace length of zero.



# SN54HC164, SN74HC164

## 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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### recommended operating conditions

			SN54HC164			SN74HC164			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage		2	5	6	2	5	6	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5			1.5			V
		V <sub>CC</sub> = 4.5 V	3.15			3.15			
		V <sub>CC</sub> = 6 V	4.2			4.2			
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0			0			V
		V <sub>CC</sub> = 4.5 V	0			1.35			
		V <sub>CC</sub> = 6 V	0			1.8			
V <sub>I</sub>	Input voltage		0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
V <sub>O</sub>	Output voltage		0		V <sub>CC</sub>	0		V <sub>CC</sub>	V
t <sub>t</sub> <sup>†</sup>	Input transition (rise and fall) time	V <sub>CC</sub> = 2 V	0		1000	0		1000	ns
		V <sub>CC</sub> = 4.5 V	0		500	0		500	
		V <sub>CC</sub> = 6 V	0		400	0		400	
T <sub>A</sub>	Operating free-air temperature		−55		125	−40		85	°C

<sup>†</sup> If this device is used in the threshold region (from  $V_{IL\text{max}} = 0.5\text{ V}$  to  $V_{IH\text{min}} = 1.5\text{ V}$ ), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at  $t_t = 1000\text{ ns}$  and  $V_{CC} = 2\text{ V}$  does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.

### electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		$V_{CC}$	$T_A = 25^\circ\text{C}$			SN54HC164		SN74HC164		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
$V_{OH}$	$V_I = V_{IH}\text{ or }V_{IL}$	$I_{OH} = -20\text{ }\mu\text{A}$	2 V	1.9	1.998		1.9		1.9		V
			4.5 V	4.4	4.499		4.4		4.4		
			6 V	5.9	5.999		5.9		5.9		
		$I_{OH} = -4\text{ mA}$	4.5 V	3.98	4.3		3.7		3.84		
		$I_{OH} = -5.2\text{ mA}$	6 V	5.48	5.8		5.2		5.34		
$V_{OL}$	$V_I = V_{IH}\text{ or }V_{IL}$	$I_{OL} = 20\text{ }\mu\text{A}$	2 V		0.002	0.1		0.1		0.1	V
			4.5 V		0.001	0.1		0.1		0.1	
			6 V		0.001	0.1		0.1		0.1	
		$I_{OL} = 4\text{ mA}$	4.5 V		0.17	0.26		0.4		0.33	
		$I_{OL} = 5.2\text{ mA}$	6 V		0.15	0.26		0.4		0.33	
$I_I$	$V_I = V_{CC}\text{ or }0$		6 V		$\pm 0.1$	$\pm 100$		$\pm 1000$		$\pm 1000$	nA
$I_{CC}$	$V_I = V_{CC}\text{ or }0, I_O = 0$		6 V			8		160		80	$\mu\text{A}$
$C_i$			2 V to 6 V		3	10		10		10	pF

# SN54HC164, SN74HC164

## 8-BIT PARALLEL-OUT SERIAL SHIFT REGISTERS

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		SN54HC164		SN74HC164		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f <sub>clock</sub>	Clock frequency	2 V	0	6	0	4.2	0	5	MHz
		4.5 V	0	31	0	21	0	25	
		6 V	0	36	0	25	0	28	
t <sub>w</sub>	Pulse duration	CLR low	2 V	100	150		125		ns
			4.5 V	20	30		25		
			6 V	17	25		21		
	CLK high or low		2 V	80	120		100		
			4.5 V	16	24		20		
			6 V	14	20		18		
t <sub>su</sub>	Setup time before CLK↑	Data	2 V	100	150		125		ns
			4.5 V	20	30		25		
			6 V	17	25		21		
	CLR inactive		2 V	100	150		125		
			4.5 V	20	30		25		
			6 V	17	25		21		
t <sub>h</sub>	Hold time, data after CLK↑		2 V	5	5		5		ns
			4.5 V	5	5		5		
			6 V	5	5		5		

switching characteristics over recommended operating free-air temperature range, C<sub>L</sub> = 50 pF (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			SN54HC164		SN74HC164		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			2 V	6	10		4.2		5		MHz
			4.5 V	31	54		21		25		
			6 V	36	62		25		28		
t <sub>PHL</sub>	CLR	Any Q	2 V		140	205		295		255	ns
			4.5 V		28	41		59		51	
			6 V		24	35		51		46	
t <sub>pd</sub>	CLK	Any Q	2 V		115	175		265		220	
			4.5 V		23	35		53		44	
			6 V		20	30		45		38	
t <sub>t</sub>			2 V		38	75		110		95	ns
			4.5 V		8	15		22		19	
			6 V		6	13		19		16	

operating characteristics, T<sub>A</sub> = 25°C

PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load	135	pF

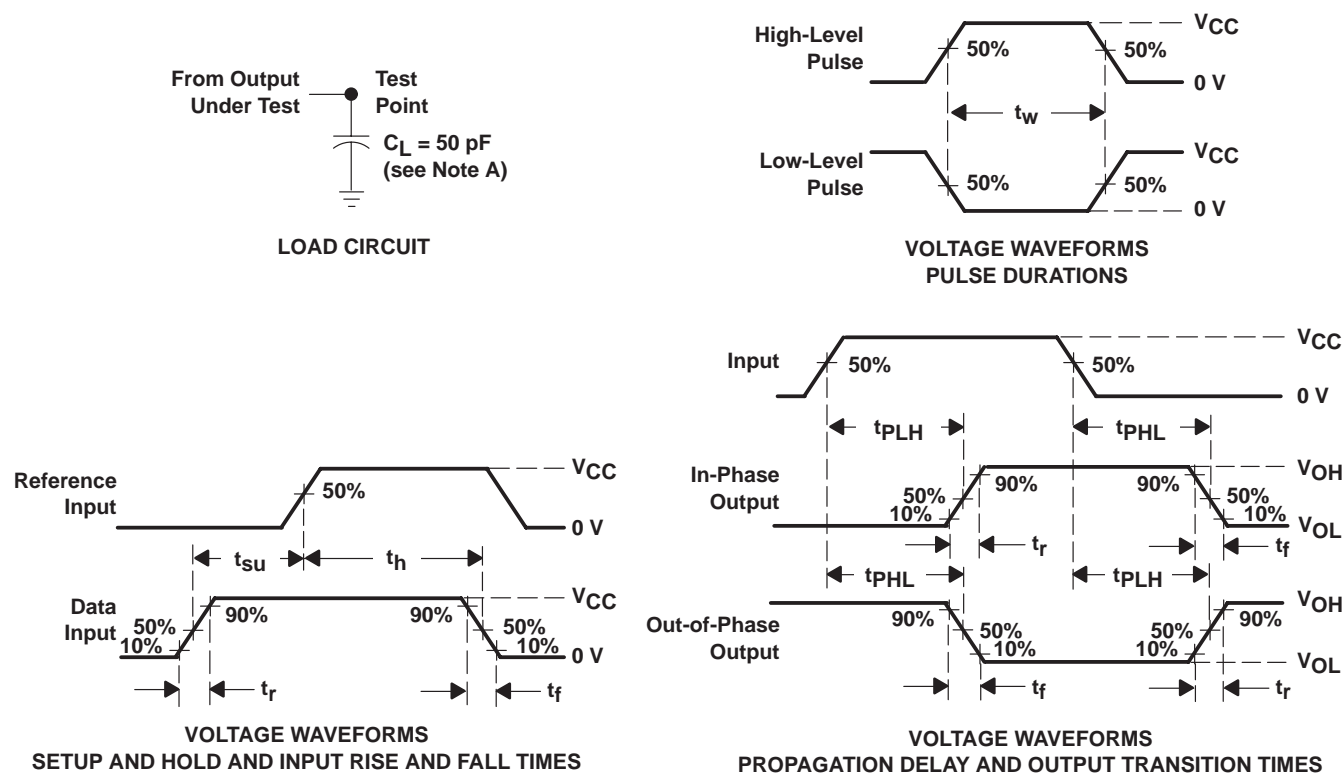


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### PARAMETER MEASUREMENT INFORMATION



- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms

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