# Giovanni Pollo

## Embedded System Engineering


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### INTRODUCTION

My interest and passion for scientific and technological subjects allowed me to obtain a grade of 101/110 in a three-year degree at the Politecnico di Torino and a grade of 110/110 cum Laude in the Master's Degree.
The experiences abroad formed me both under the cultural and relational aspects and have increased my independence and problem-solving ability.

### EDUCATION

#### Master's degree in Embedded Systems

Politecnico Di Torino | 2020 - 2023

#### Bachelor's degree in Electronic Engineering

Politecnico Di Torino | 2017 - 2020

### SKILLS

- Linux, Docker
- C, C++, Bash, LaTeX, VHDL, Verilog, CUDA, Python, HLS
- Visual Studio Code, Jetbrains Editors, Office Suite
- Digital Design, Hardware Design, FPGA
- Cybersecurity for Embedded Systems
- Neural Networks Accelerators

### CERTIFICATION

#### Cambridge C1 Advanced

Milan | 2016

#### Cambridge B2 First

Milan | 2015

### EXPERIENCE

#### Children's Supervisor

Astro Park Tallaght, Dublin| July 2017 - September 2017

- Improvements in the English language
- First approach to a work environment
- Ability to manage a group of people
- Deadlines

#### Study abroad

Joseph Chamberlain Sixth Form College, Birmingham | August 2016 - December 2016

- Improvements in the English language
- Get in touch with different cultures
- Deadlines
- Participation in many group project
- Ability to live abroad

### PROJECTS

#### DLX Microprocessor Design

Politecnico Di Torino | March 2021 - July 2021

- VHDL structural design
- Windowed register file
- Five Stages Pipeline
- Enhanced Booth's Multiplier
- Hazard detection

#### CUDA Video Streaming

Politecnico Di Torino | September 2021 - February 2022

- Fully functional on NVIDIA Jetson Nano board
- Maximum parallelism with threads and kernels
- Comparison between CPU and GPU performance
- Independent module for higher scalability

### THESIS

#### Resilience analysis of FPGA-based Dataflow accelerators

Politecnico Di Torino | June 2022 - April 2023

- Neural Network Accelerators
- Dataflow architecture
- HLS optimization
- Bit-Flips attack
- Analysis of the accuracy degradation in presence of hardware errors