Giorgos Vyronos

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giorgosvyronos | giorgos-vyronos
Python • C/C++ • GoLang • F#
giorgosvyronos.github.io

Education

MEng Electronic and Information Engineering **Sep 2019 - June 2023**
Imperial College London *London, UK*

- Expected Graduation Class: Second Class Upper Division (2:1)
- Year 4 Modules: Self-Organising Multi-Agent Systems, Hardware and Software Verification, Mathematics for Machine Learning, Deep Learning, System Performance Engineering, Distributed Algorithms
- Final Year Project:

Experience

System Development Engineer Intern | *Python* **Apr 2022 - Sep 2022**
Amazon.com *Dublin, Ireland*

- Member of the Intelligent Cloud Hosting Rendering Experience Team (ICON/IRX).
- Developed an automated auditing process to assess the compatibility of cloud environments using the x86 platform to the Arm-based Graviton platform.

Summer Internship Program | *Java, XML* **Jul 2020 - Aug 2020**
SignalGeneriX Ltd *Limassol, Cyprus*

- Focused on performing research on Image Recognition and on deploying a system for identifying and logging a citizen's temperature under COVID-19.
- Conducted first steps in developing an app for Image Processing and Recognition purposes (using Android Studio, Java and XML).

Academic Projects

Year 3 Coursework - Design a Digital System | SystemVerilog, Intel Quartus Prime **Jan 2022 — Mar 2022**

- Developed in a group of 2, a digital system design using Intel Quartus Prime to accelerate an application (arithmetic expression calculation) through reconfiguring the hardware of an FPGA.
- Designed a NIOS II processor on an FPGA using on-chip RAM and external memory.
- Extended design to provide support for floating point operations through software emulating blocks and through custom IP hardware blocks to be used as dedicated hardware blocks to compute the target expression.

Year 2 Spring Term Project - Information Processing System | Eclipse, Intel Quartus Prime **Feb 2021 — Mar 2021**

- Developed in a group of 6, a multiplayer racing game hosted on a server with multiple local FPGAs (DE10-lite) as nodes. The server was designed using NodeJS and Express.
- Steering data from the on-board accelerometer were locally processed and communicated to the server from each node. The data processing was designed using Eclipse. Server communication was established through Python and the Nios-II terminal.
- Information was then communicated back to each node to display current position on FPGA LEDs.

Year 2 Autumn Term Project - MIPS-compatible CPU | SystemVerilog, Intel Quartus Prime **Oct 2020 — Nov 2020**

- Member of a group of 5 people that developed a working synthesizeable MIPS-compatible CPU using SystemVerilog. This CPU interfaced with the world using a memory-mapped bus, which would gave it access to memory and other peripherals.
- The outcome of this Project was to produce a deliverable containing an implementation of the CPU, a test-bench and memory, and a data-sheet covering the overall CPU architecture and the test-bench testing implementation.

Leadership and Awards

Artillery Corporal **Jul 2018 — Sep 2019**
Cyprus National Guard *Limassol, Cyprus*

- In charge of managing strategic and confidential information at the 195^{th} Anti-Aircraft Artillery Battalion (195 MEA/AP) personnel office.
- Completed tactical training as an Assistant Operator of the OTHELLO anti-aircraft gunnery system.

Technical Skills

Programming Languages
Python, Swift, C, C++, HTML/CSS, JavaScript, MatLab, VHDL, SystemVerilog, GoLang, F#.

Developer Tools
VS Code, Git, Eclipse, Intel Quartus Prime, XCode, Jetbrains IntelliJ.

Technologies/Frameworks
Linux, MacOS, GitHub, MongoDB, LaTeX.