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# **G76S**

## **LoRa Wireless**

# **Communication Module**

**Date: Sep. 21th, 2017**

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## 1. General Description

The G76S integrates ARM Cortex®-M0+ (32-bit RISC core operating at a 32MHz frequency) MCU with LoRa™ modulation that provides ultra-long range spread spectrum communication and high interference immunity whilst minimizing current consumption.

G76S can achieve a sensitivity of over -148 dBm. The high sensitivity combined with the integrated +19.5 dBm power amplifier yields industry leading link budget making it optimal for any low data rate application requiring range or robustness. LoRa™ also provides significant advantages in both blocking and selectivity over conventional modulation techniques, solving the traditional design compromise between range, interference immunity and energy consumption.

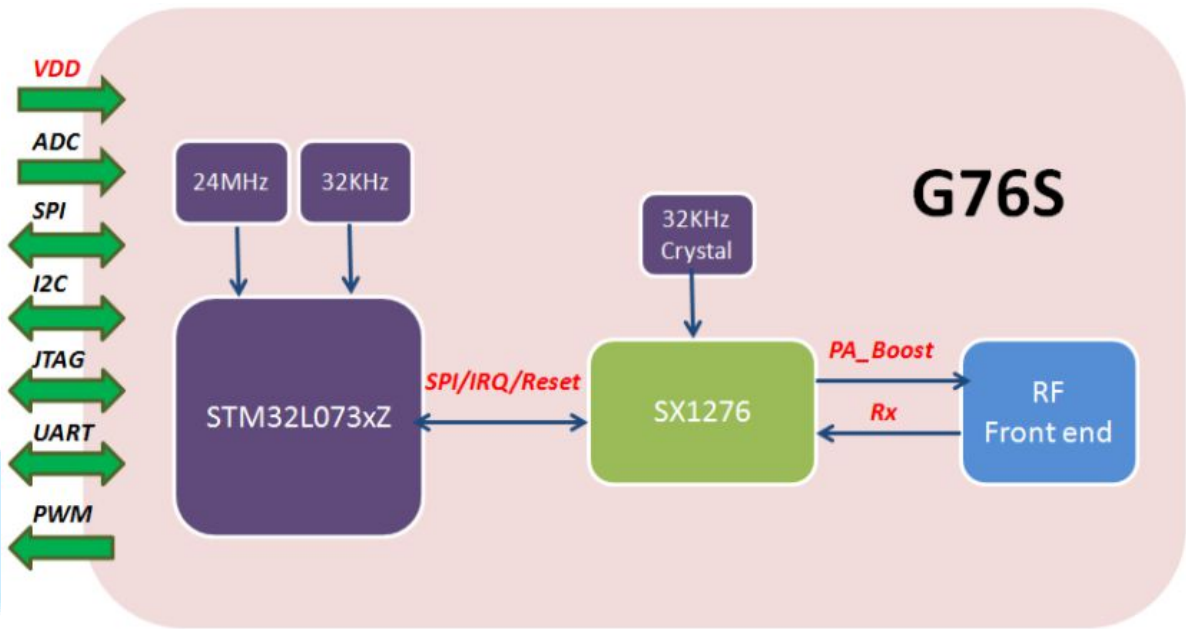
### Features

- Small footprint : 13 mm x 11 mm x 1.1 mm
- LoRa™ Modem
- +19.5 dBm constant RF output vs. V supply
- Programmable bit rate up to 37500 bps
- High sensitivity: down to -148 dBm
- Excellent blocking immunity
- Preamble detection
- Automatic RF Sense and CAD with ultra-fast AFC
- Payload up to 242 bytes with CRC \* [Note](#)
- Embedded memories (up to 192 Kbytes of Flash memory and 20 Kbytes of RAM)

**Note: LoRa WAN FW mode: payload up to 242 Byte; GIOT FW mode: payload up to 51 Byte while SF is between 7~9.**

## 1-1 Block Diagram

A simplified block diagram of the G76S module is depicted in the figure below.



## 1-2 Product Version

The features of G76S is detailed in the following table:

Part Number	Frequency Range	Spreading Factor	Bandwidth (KHz)	Effective Bitrate (bps)	Est. Sensitivity ( dBm )
G76S	863~870 MHz &902~928 MHz	6 - 12	62.5 - 500	146 - 37500	-109 to -139*

**Note:** LORA setting SF=12, BW=62.5k, Long-Range Mode, highest LNA gain, *LnaBoost* for Band 1.

## 1-3 Specification

Model Name	G76S
Product Description	LoRa Wireless Communication Module
Host Interface	UART
<b>Operation Conditions</b>	
Temperature	<ul style="list-style-type: none"> <li>■ Storage : -50°C ~ +105°C</li> <li>■ Operating : -40°C ~ +85°C</li> </ul>
Humidity	<ul style="list-style-type: none"> <li>■ Operating : 10 ~ 95% (Non-Condensing)</li> <li>■ Storage : 5 ~ 95% (Non-Condensing)</li> </ul>
Dimension	13 mm x 11 mm x 1.1 mm
Package	LGA type

## 2. Electrical Characteristics

### 2-1 Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD33	Supply Voltage	-0.3		3.9	V
V <sub>IN</sub>	Input voltage on digital pins	-0.3		3.9	V
P <sub>mr</sub>	RF Input Level			+10	dBm

## 2-2 Recommended Operating Range

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD33	Supply Voltage	2.0	3.3	3.6	V
ML	RF Input Level			+10	dBm

## 2-3 Power Consumption Characteristics

Symbol	Parameter	Conditions	Typ.	Max.	Unit
IDDSL	Supply current in Sleep mode		5		uA
IDDST	Supply current in Standby mode	Crystal oscillator enabled	9	9.6	mA
IDDR	Supply current in Receive mode		17.5		mA
IDDT	Supply current in Transmit mode with impedance matching	RFOP = +19.5 dBm RFOP = +17 dBm RFOP = +13 dBm RFOP = + 7 dBm	127 82 65 49		mA

**Note:** Power consumption measured @3.3V.



## 2-4 RF Characteristics

The table below gives the electrical specifications for the transceiver operating with LoRa™ modulation. Following conditions apply unless otherwise specified:

- Supply voltage = 3.3 V.
- Temperature = 25° C.
- Frequency range: 863~870 MHz & 902~928 MHz\*[Note](#)
- Bandwidth (BW) = 125 kHz.
- Spreading Factor (SF) = 12.
- Error Correction Code (EC) = 4/5.
- Packet Error Rate (PER)= 1%
- CRC on payload enabled.
- Output power = 19.5 dBm in transmission.
- Preamble Length = 12 symbols (programmed register PreambleLength=8)
- With matched impedances

**Note:** The frequency band could be configured within the range based on regulations stipulated in different countries.

LoRa Transmitter (Conductive)					
Item	Condition	Min.	Typ.	Max.	Unit
Tx Power Level	PA_BOOST pin	18.0	19.5	21.0	dBm
LoRa Receiver (Conductive)					
Item	Condition	Min.	Typ.	Max.	Unit
RFS_L62_HF  (Long-Range Mode, highest LNA gain, LNA boost, 62.5 kHz bandwidth)	SF = 6		-119		dBm
	SF = 7		-114		dBm
	SF = 8		-127		dBm
	SF = 12		-137		dBm
RFS_L500_HF  (Long-Range Mode, highest LNA gain, LNA boost, 500 kHz)	SF = 6		-109		dBm
	SF = 7		-114		dBm
	SF = 8		-117		dBm

bandwidth)	SF = 9		-120		dBm
	SF = 10		-123		dBm
	SF = 11		-126		dBm
	SF = 12		-128		dBm

## 2-5 Digital Characteristics

### 2-5.1 DC characteristics

#### Input voltage levels

Symbol	Description	Conditions	Min	Typ.	Max	Unit
VIH	I/O input high level voltage	NRST	0.7xVDD33	-	-	V
		BOOT0	0.7xVDD33	-	-	V
		GPIO	0.7xVDD33	-	-	V
VIL	I/O input low level voltage	NRST	-	-	0.3xVDD33	V
		BOOT0	-	-	0.14xVDD33	V
		GPIO	-	-	0.3xVDD33	V
R <sub>PU</sub>	Weak pull-up Equivalent resistor	V <sub>IN</sub> = GND	30	45	60	K Ω
R <sub>PD</sub>	Weak pull-down Equivalent resistor	V <sub>IN</sub> = VDD33	30	45	60	K Ω



## Output voltage levels

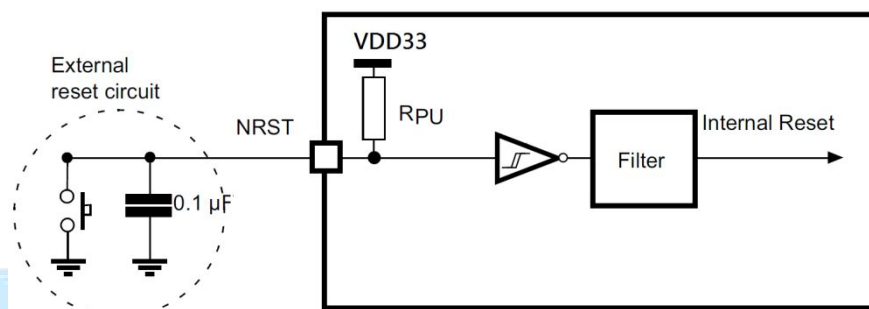
Symbol	Description	Conditions	Min	Max	Unit
$V_{OL}$	Output low level voltage for an I/O pin	CMOS port / IIO = +8 mA $2.7\text{ V} \leq V_{DD33} \leq 3.6\text{ V}$	-	0.4	V
$V_{OH}$	Output high level voltage for an I/O pin		$V_{DD33}-0.4$	-	
$V_{OL}$	Output low level voltage for an I/O pin	TTL port / IIO = + 8 mA $2.7\text{ V} \leq V_{DD33} \leq 3.6\text{ V}$	-	0.4	
$V_{OH}$	Output high level voltage for an I/O pin	TTL port / IIO = - 6 mA $2.7\text{ V} \leq V_{DD33} \leq 3.6\text{ V}$	2.4	-	
$V_{OL}$	Output low level voltage for an I/O pin	IIO = +15 mA $2.7\text{ V} \leq V_{DD33} \leq 3.6\text{ V}$	-	1.3	
$V_{OH}$	Output high level voltage for an I/O pin	IIO = -15 mA $2.7\text{ V} \leq V_{DD33} \leq 3.6\text{ V}$	$V_{DD33}-1.3$	-	
$V_{OL}$	Output low level voltage for an I/O pin	IIO = +4 mA $1.65\text{ V} \leq V_{DD33} \leq 3.6\text{ V}$	-	0.45	
$V_{OH}$	Output high level voltage for an I/O pin	IIO = +4 mA $1.65\text{ V} \leq V_{DD33} \leq 3.6\text{ V}$	$V_{DD33}-0.45$	-	

## 2-5.2 NRST pin characteristics

The NRST pin input driver uses CMOS technology.

It is connected to a permanent pull-up resistor ( $R_{PU}$ ).

The following figure is recommended NRST pin protection circuit against parasitic resets.



Symbol	Description	Conditions	Min	Typ.	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage		VSS		0.8	V
$V_{IH(NRST)}$	NRST input high level voltage		1.4		VDD33	V
$V_{OL(NRST)}$	NRST output low level voltage	$I_{OL} = 2\text{mA}$ $2.7\text{V} < \text{VDD33} < 3.6\text{V}$			0.4	V
$V_{OL(NRST)}$	NRST output low level voltage	$I_{OL} = 1.5\text{mA}$ $1.65\text{V} < \text{VDD33} < 3.6\text{V}$			0.4	V
$V_{hys(NRST)}$	NRST schmitt trigger voltage hysteresis			10% VDD33		mV
$R_{PU}$	Weak pull-up Equivalent resistor	$V_{IN} = \text{GND}$	30	45	60	K $\Omega$
$V_F$	NRST Input filtered pulse				50	nS
$V_{NF}$	NRST Input not filtered pulse	$\text{VDD33} > 2.7\text{V}$		350		nS

## 2-5.3 UART Interface Parameters

Baud Rate = 9600 bps  
Data Bits = 8 bits  
Stop Bits = 1 bit  
Parity Check = None  
Flow Control = None

## 3. Pin Definition

### 3-1 Pin Assignment

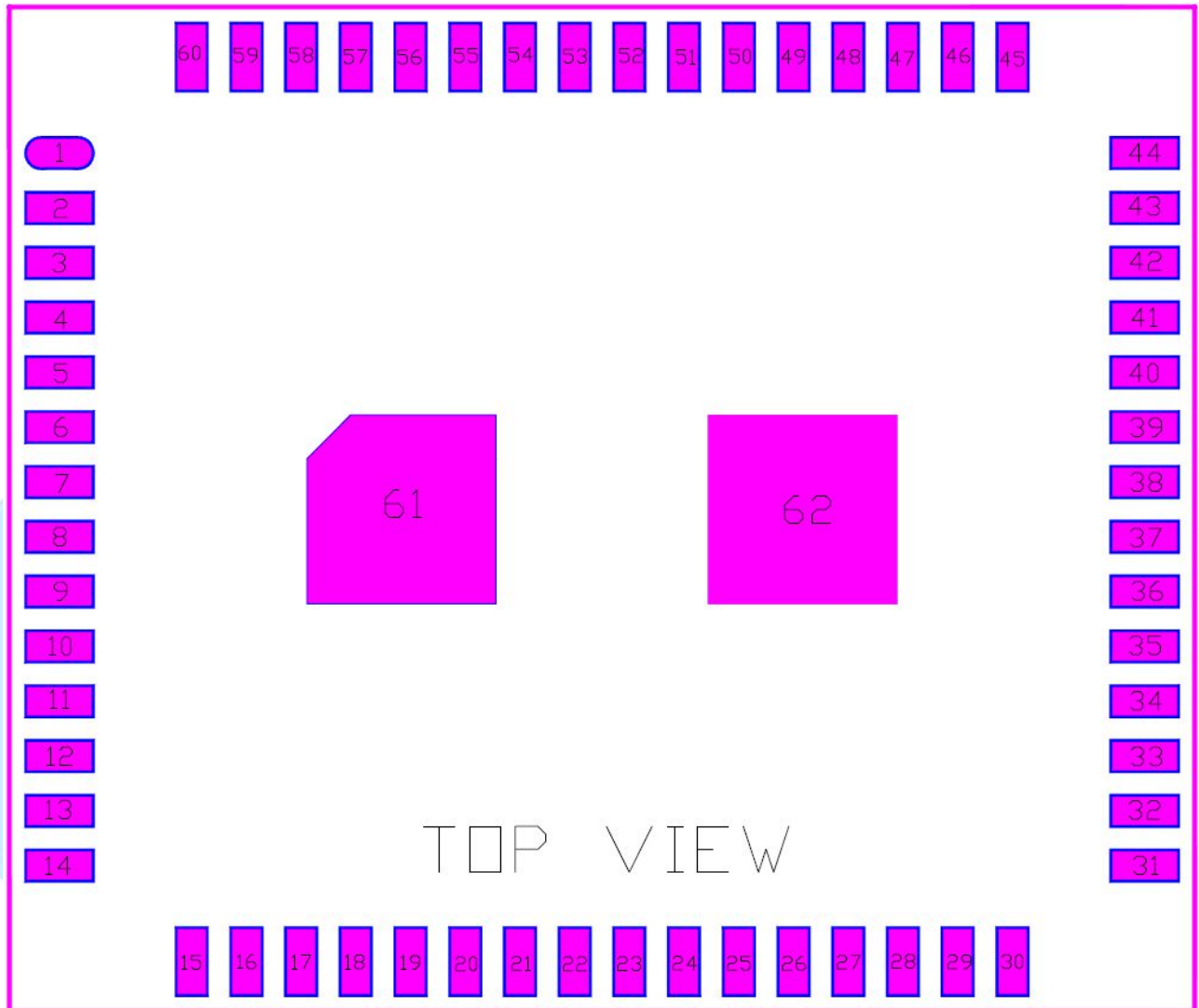
The SiP module will conform to the following pin map, shown in the following diagram (top view)

Pin	Definition	I/O	Description
1	NC		
2	GND		Ground pin
3	GND		Ground pin
4	PC0	I/O	MCU pin name: PC0
5	PC1	I/O	MCU pin name: PC1
6	PC2	I/O	MCU pin name: PC2
7	PC3	I/O	MCU pin name: PC3
8	NC		
9	NC		
10	NC		
11	NC		
12	NRST		Hardware reset pin
13	PA0	I/O	MCU pin name: PA0

14	GND		Ground pin
15	GND		Ground pin
16	PA2	I/O	MCU pin name: PA2
17	PA3	I/O	MCU pin name: PA3
18	PA4_SPI1_NSS	I/O	MCU pin name: PA4
19	PA5_SPI1_SCK	I/O	MCU pin name: PA5
20	PA6_SPI1_MISO	I/O	MCU pin name: PA6
21	PA7_SPI1_MOSI	I/O	MCU pin name: PA7
22	PC4	I/O	MCU pin name: PC4
23	PC5	I/O	MCU pin name: PC5
24	PB0_IO_INT1	I/O	MCU pin name: PB0
25	PB1_IO_INT2	I/O	MCU pin name: PB1
26	PC6	I/O	MCU pin name: PC6
27	PC7	I/O	MCU pin name: PC7
28	PC8	I/O	MCU pin name: PC8
29	PC9	I/O	MCU pin name: PC9
30	RXTX/RFMOD	O	Control signal from SX1276, which connects to internal RF switch at the same time.
31	GND		Ground pin
32	GND		Ground pin
33	RF_ANT	I/O	RF I/O
34	GND		Ground pin
35	GND		Ground pin
36	PA1_RF_FEM_CPS	I/O	MCU pin name: PA1
37	GND		Ground pin
38	NC		

39	GND		Ground pin
40	NC		
41	GND		Ground pin
42	NC		
43	VDD33		Power Supply
44	VDD33		Power Supply
45	PA8_USART1_CK	I/O	MCU pin name: PA8
46	PA10_USART1_RX	I/O	MCU pin name: PA10(UART)
47	PA9_USART1_TX	I/O	MCU pin name: PA9(UART)
48	PA11_USART1_CTS	I/O	MCU pin name: PA11
49	PA12_USART1_RTS	I/O	MCU pin name: PA12
50	PA13_SWDIO		Serial wire (SWD) debug interface
51	PA14_SWCLK		Serial wire (SWD) debug interface
52	PC10	I/O	MCU pin name: PC10
53	PC11	I/O	MCU pin name: PC11
54	PC12	I/O	MCU pin name: PC12
55	PD2	I/O	MCU pin name: PD2
56	PB5	I/O	MCU pin name: PB5
57	PB6_SCL	I/O	MCU pin name: PB6
58	PB7_SDA	I/O	MCU pin name: PB7
59	BOOT0	I	Boot mode selection pin
60	PB8_IO_LED_FCT	I/O	MCU pin name: PB8
61	GND		Ground Pin
62	GND		Ground Pin

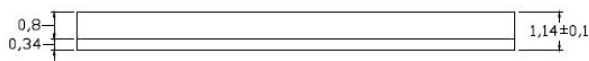
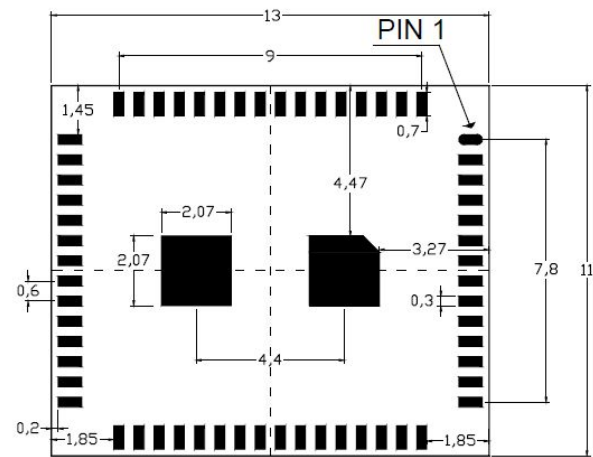
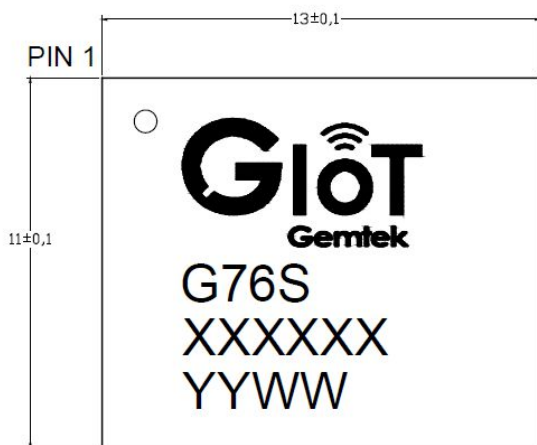
**\*Note: All unused IO pins should be kept floating.**





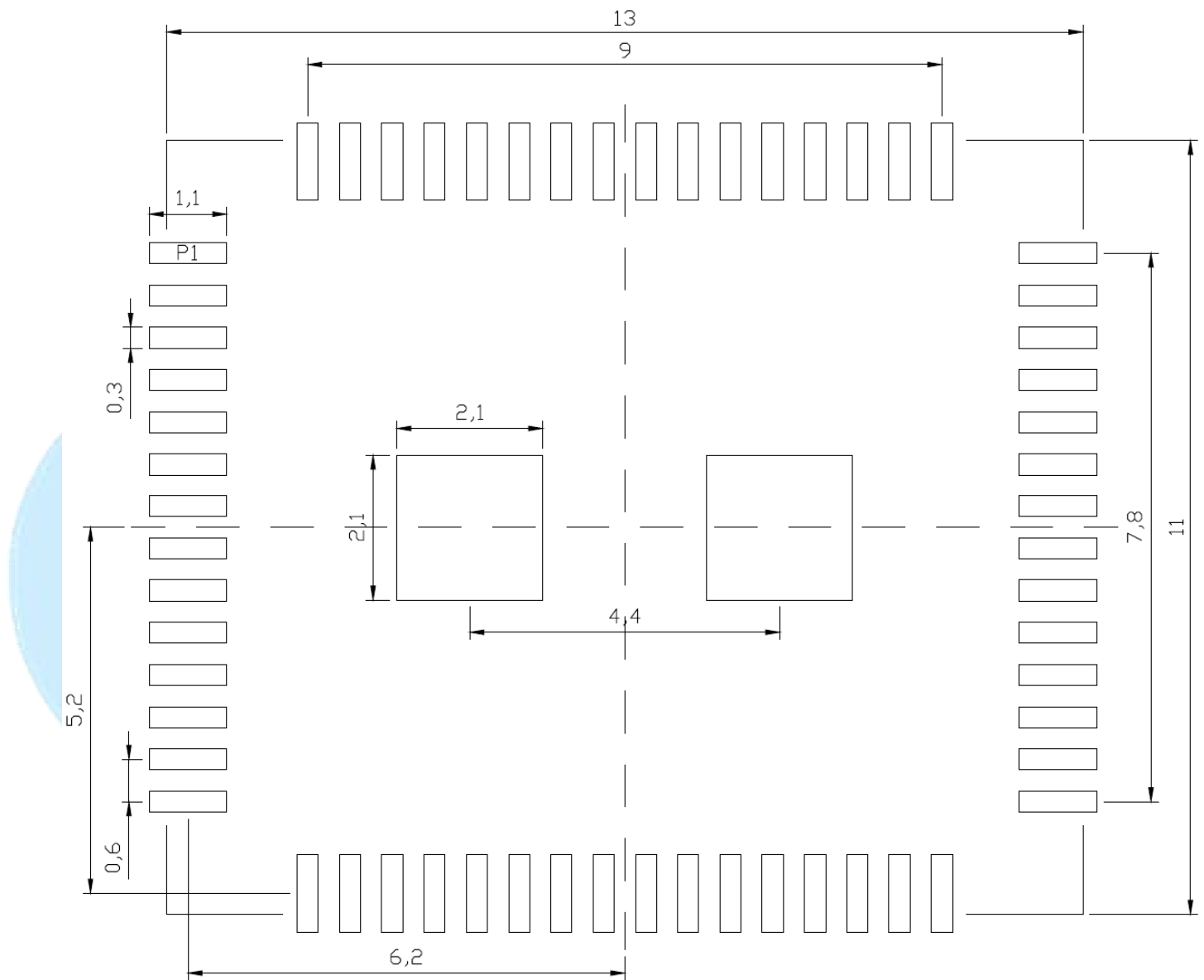
## 4. Mechanical Dimension

Unit: mm



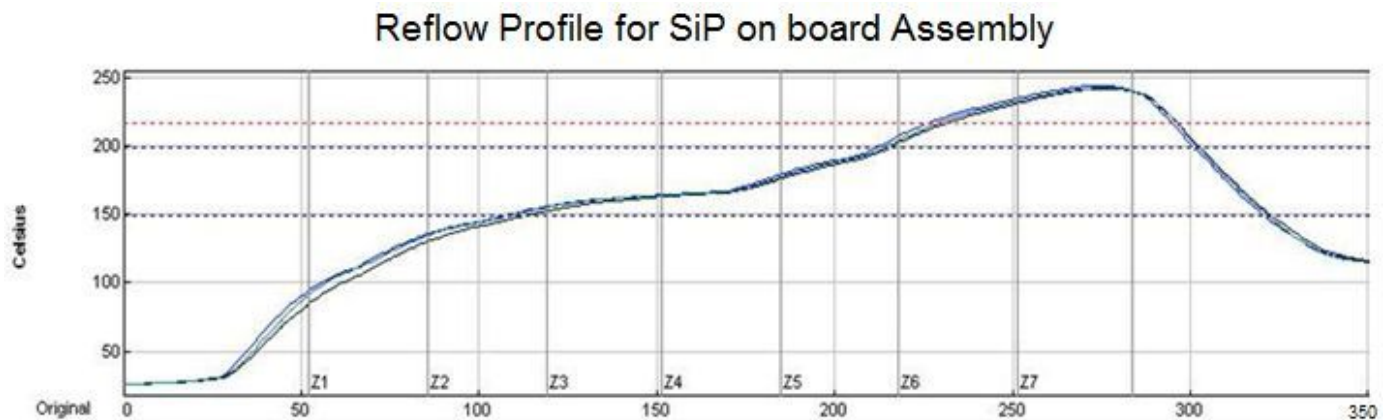
## 4-2 Recommended Footprint

Unit: mm



TOP View

## 5. Recommended Reflow Profile



<b>Preheat time</b>	<b>150°C—200°C : 105+/-15sec</b>
<b>Dwell time</b>	<b>Over 220°C : 70+5/-10 sec</b>
<b>Peak Temp</b>	<b>240 +10/-5°C</b>
<b>Ramp Up/Down Rate</b>	<b>Up: 3 +0/-2 °C / sec Down: 2 +0/-1°C / sec</b>

## 6. SiP Module Preparation

### 6-1 Handling

Handling the module must wear the anti-static wrist strap to avoid ESD damage. After each module is aligned and tested, it should be transported and stored with anti-static tray and packing. This protective package must remain in a suitable environment until the module is assembled and soldered onto the main board.

## 6-2 SMT Preparation

1. Estimated shelf life in sealed bag: 6 months at  $<40^{\circ}\text{C}$  and  $<90\%$  relative humidity (RH).
2. Peak package body temperature:  $250^{\circ}\text{C}$ .
3. After opening the bag, devices that will be due to undergo reflow soldering or other high temperature process must:
  - A. Be mounted within: 168 hours of factory conditions  $<30^{\circ}\text{C}/60\%\text{RH}$ .
  - B. Be stored at  $\leq 10\%\text{RH}$  with  $\text{N}_2$  flow box.
4. Devices may require baking before mounting, if:
  - A. Package bag was not kept in a vacuum environment after opening.
  - B. Humidity Indicator Card is  $>10\%$  when read at  $23\pm 5^{\circ}\text{C}$ .
  - C. Exposed at 3A condition over 8 hours or Exposed at 3B condition over 24 hours.
5. If baking is required, devices may need to be baked for 12 hours at  $125\pm 5^{\circ}\text{C}$ .

## 7. Package Information

### 7-1 Product Making

Figure 1 below details the standard product marking for all Gemtek products. Cross reference to the applicable line number and table for a full detail of all the variables.

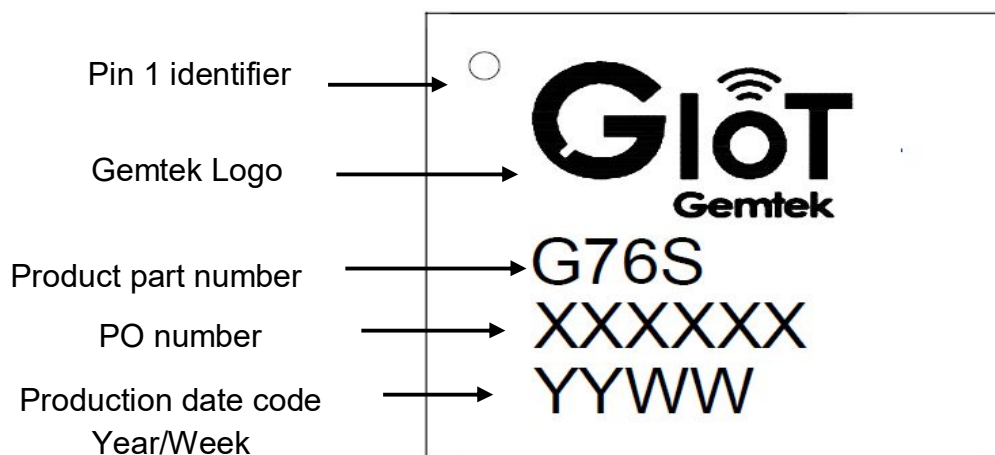


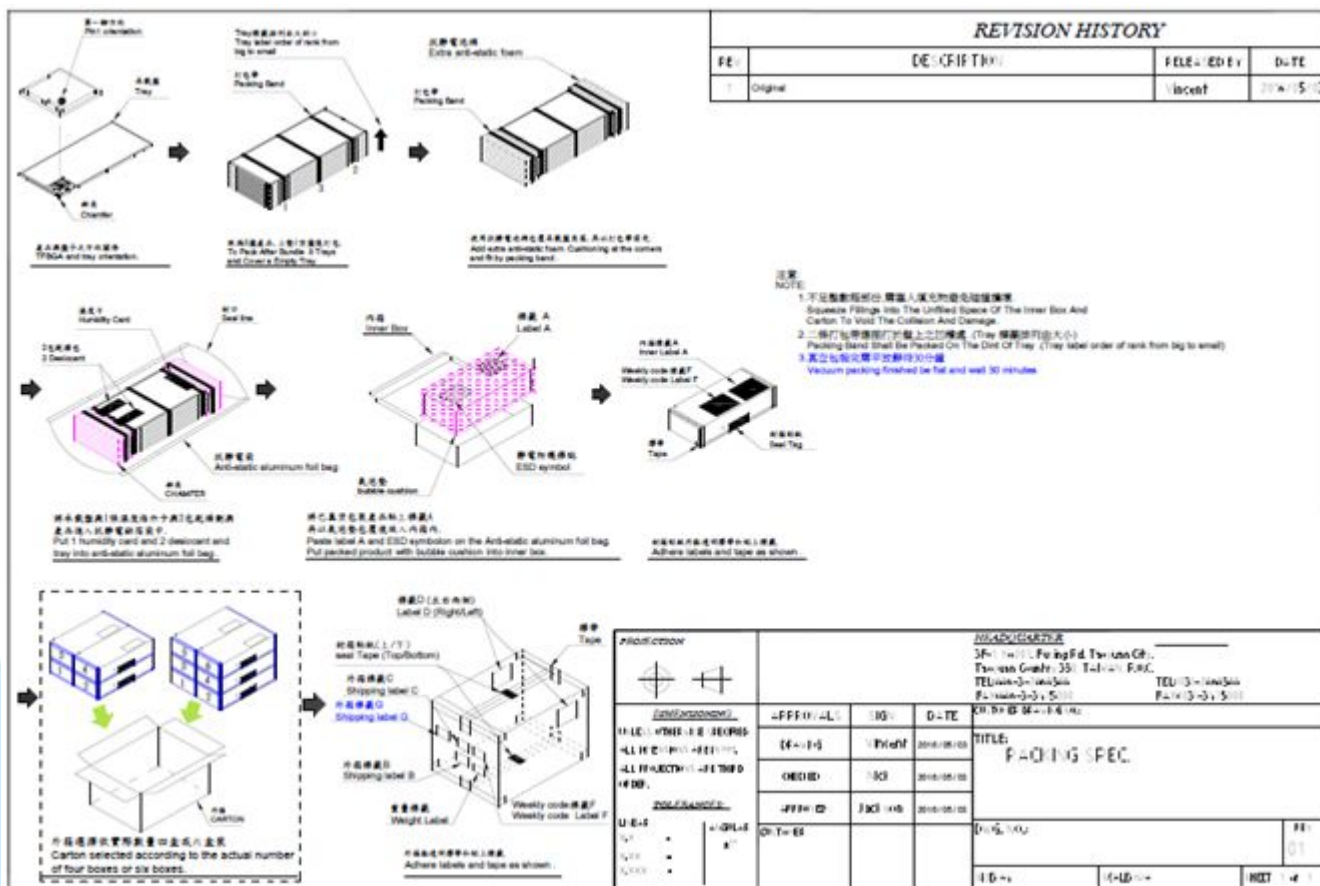
Figure 1 Standard Product Marking Diagram- TOP

VIEW





## 7-3 Packing Information



## 7-4 Humidity Indicator Card



**Indicates 指示點:**

10%,20%,30,40%,50%,60% relative humidity  
10%,20%,30,40%,50%,60% 相對濕度

**Color Change 顏色變化:**  
**Brown (Dry) ---> Blue (Wet)**  
**棕色 (乾燥) ---> 藍色 (潮溼)**