Gemtek
Wireless Broadband Anywhere

Document Number	QW_01_0012.001

G78S
LoRa Wireless Communication Module

Date: Oct 11th, 2016

Modification History

Date	Change log	Author	Revision
10/31/2016	Update specification values	Cory	0.1

Table of Contents

1. General Description

The G78S integrates ARM Cortex®-M0+ (32-bit RISC core operating at a 32MHz frequency) MCU with LoRa™ modulation that provides ultra-long range spread spectrum communication and high interference immunity whilst minimizing current consumption.

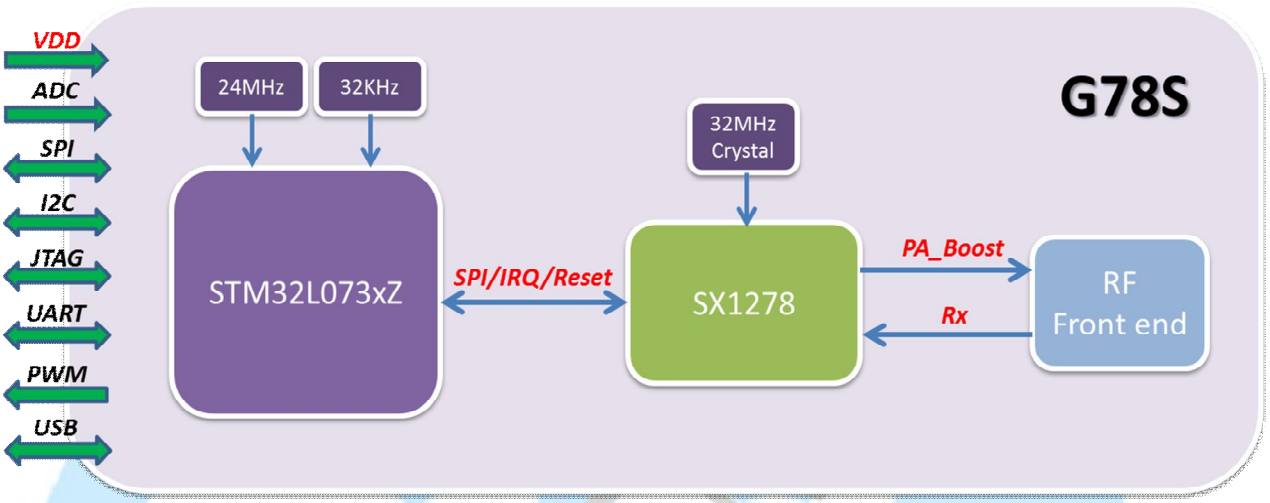
G78S can achieve a sensitivity of over -148 dBm. The high sensitivity combined with the integrated +20 dBm power amplifier yields industry leading link budget making it optimal for any low data rate application requiring range or robustness. LoRa™ also provides significant advantages in both blocking and selectivity over conventional modulation techniques, solving the traditional design compromise between range, interference immunity and energy consumption.

Feature

- Small footprint：13 mm x 11 mm x 1.1 mm
- LoRa™ Modem
- +20 dBm constant RF output vs. V supply
- Programmable bit rate up to 37500 bps
- High sensitivity: down to -148 dBm
- Excellent blocking immunity
- Preamble detection
- Automatic RF Sense and CAD with ultra-fast AFC
- Payload up to 128 bytes with CRC
- Embedded memories (up to 192 Kbytes of Flash memory and 20 Kbytes of RAM)

1-1 Block Diagram

A simplified block diagram of the G78S module is depicted in the figure below.



1-2 Product Version

The features of G78S is detailed in the following table

Part Number	Frequency Range	Spreading Factor	Bandwidth (K Hz)	Effective Bitrate (bps)	Est. Sensitivity (dBm)
G78S	470 MHz	6 - 12	62.5 - 500	146 - 38500	-109 to -138*

Note: * LORA setting SF=12, BW=62.5k, Long-Range Mode, highest LNA gain, *LnaBoost* for Band 1.

1-3 Specification

Model Name	G78S
Product Description	LoRa Wireless Communication Module
Host Interface	UART
Operation Conditions	
Temperature	■ Storage：-50℃ ~ +105℃ ■ Operating：-40℃ ~ +85℃

Humidity	■ Operating：10 ~ 95% (Non-Condensing) ■ Storage：5 ~ 95% (Non-Condensing)
Dimension	13 mm x 11 mm x 1.1 mm
Package	LGA type

2. Electrical Characteristics

2-1. Absolute Maximum Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD33	Supply Voltage	-0.3		3.9	V
V_{IN}	Input voltage on digital pins	-0.3		3.9	V
Pmr	RF Input Level			+10	dBm

2-2. Recommended Operating Range

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD33	Supply Voltage	2.0	3.3	3.6	V
ML	RF Input Level			+10	dBm

2-3. Power Consumption Characteristics

Symbol	Parameter	Conditions	Typ.	Max.	Unit
IDDSL	Supply current in Sleep mode		TBD		uA

IDDST	Supply current in Standby mode	Crystal oscillator enabled	9	9.8	mA
IDDR	Supply current in Receive mode		17.7		mA
IDDT	Supply current in Transmit mode with impedance matching	RFOP = +20 dBm RFOP = +17 dBm RFOP = +13 dBm RFOP = + 7 dBm	128 83 64.5 48		mA

2-4. RF Characteristics

The table below gives the electrical specifications for the transceiver operating with LoRa™ modulation. Following conditions apply unless otherwise specified:

- Supply voltage = 3.3 V.
- Temperature = 25° C.
- Frequency bands: 470 MHz
- Bandwidth (BW) = 125 kHz.
- Spreading Factor (SF) = 12.
- Error Correction Code (EC) = 4/6.
- Packet Error Rate (PER)= 1%
- CRC on payload enabled.
- Output power = 13 dBm in transmission.
- Payload length = 64 bytes.
- Preamble Length = 12 symbols (programmed register PreambleLength=8)
- With matched impedances

LoRa Transmitter (Conductive)					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Frequency Range	Band2		480		MHz
Tx Power Level	PA_BOOST pin	18.0	19.5	21.0	dBm

LoRa Receiver (Conductive)					
Item	**Condition**	**Min.**	**Typ.**	**Max.**	**Unit**
Frequency Range	Band2		480		MHz
RFS_L62_LF (Long-Range Mode, highest LNA gain, 62.5 kHz bandwidth)	SF = 11		-135		dBm
	SF = 12		-138		dBm
RFS_L500_LF (Long-Range Mode, highest LNA gain, 500 kHz bandwidth)	SF = 6		-110		dBm
	SF = 7		-116		dBm
	SF = 8		-119		dBm
	SF = 9		-122		dBm
	SF = 10		-125		dBm
	SF = 11		-127		dBm
	SF = 12		-128		dBm

2-5. Digital Characteristics

2-5-1. DC characteristics

Input voltage levels

Symbol	Description	Conditions	Min	Typ.	Max	Unit
VIH	I/O input high level voltage	NRST	0.7xVDD33	-	-	V
		BOOT0	0.7xVDD33	-	-	V
		GPIO	0.7xVDD33	-	-	V
VIL	I/O input low level voltage	NRST	-	-	0.3xVDD33	V
		BOOT0	-	-	0.14xVDD33	V

		GPIO	-	-	0.3xVDD33	V
R_{PU}	Weak pull-up Equivalent resistor	V_{IN} = GND	30	45	60	K Ω
R_{PD}	Weak pull-down Equivalent resistor	V_{IN} =VDD33	30	45	60	K Ω

Output voltage levels

Symbol	Description	Conditions	Min	Max	Unit
V_{OL}	Output low level voltage for an I/O pin	CMOS port / IIO = +8 mA 2.7 V≦VDD33≦3.6 V	-	0.4	V
V_{OH}	Output high level voltage for an I/O pin		VDD33-0.4	-	
V_{OL}	Output low level voltage for an I/O pin	TTL port / IIO =+ 8 mA 2.7 V≦VDD33≦3.6 V	-	0.4	
V_{OH}	Output high level voltage for an I/O pin	TTL port / IIO =- 6 mA 2.7 V≦VDD33≦3.6 V	2.4	-	
V_{OL}	Output low level voltage for an I/O pin	IIO = +15 mA 2.7 V≦VDD33≦3.6 V	-	1.3	
V_{OH}	Output high level voltage for an I/O pin	IIO = -15 mA 2.7 V≦VDD33≦3.6 V	VDD33-1.3	-	
V_{OL}	Output low level voltage for	IIO = +4 mA	-	0.45	

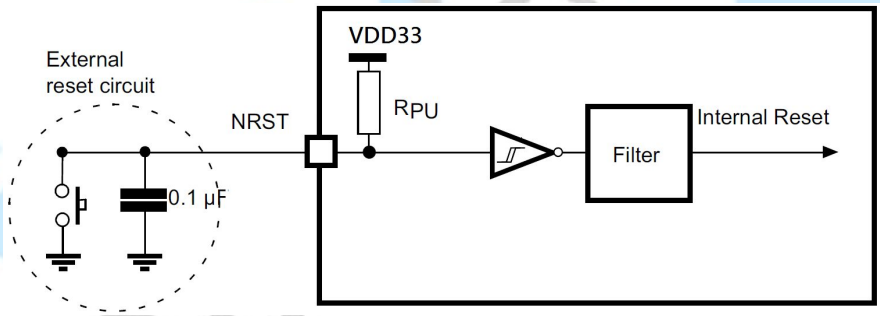
	an I/O pin	1.65 V≦VDD33≦3.6 V			
V_{OH}	Output high level voltage for an I/O pin	IIO = +4 mA 1.65 V≦VDD33≦3.6 V	VDD33-0.45	-	

2-5-2. NRST pin characteristics

The NRST pin input driver uses CMOS technology.

It is connected to a permanent pull-up resistor (R_{PU}).

The following figure is recommended NRST pin protection circuit against parasitic resets.



Symbol	Description	Conditions	Min	Typ.	Max	Unit
$V_{IL(NRST)}$	NRST input low level voltage		VSS		0.8	V
$V_{IH(NRST)}$	NRST input high level voltage		1.4		VDD33	V
$V_{OL(NRST)}$	NRST output low level voltage	I_{OL} = 2mA 2.7V < VDD33 < 3.6V			0.4	V
$V_{OL(NRST)}$	NRST output low level voltage	I_{OL} = 1.5mA 1.65V < VDD33 <			0.4	V

$V_{hys(NRST)}$	NRST schmitt trigger voltage hysteresis			10% VDD33		mV
R_{PU}	Weak pull-up Equivalent resistor	V_{IN} = GND	30	45	60	K Ω
V_F	NRST Input filtered pulse				50	nS
V_{NF}	NRST Input not filtered pulse	VDD33 > 2.7 V		350		nS

2-5-3. UART Interface Parameters

Baud Rate = 9600 bps
Data Bits = 8 bits
Stop Bits = 1 bit
Parity Check = None
Flow Control = None

3. Pin Definition

3-1. Pin Assignment

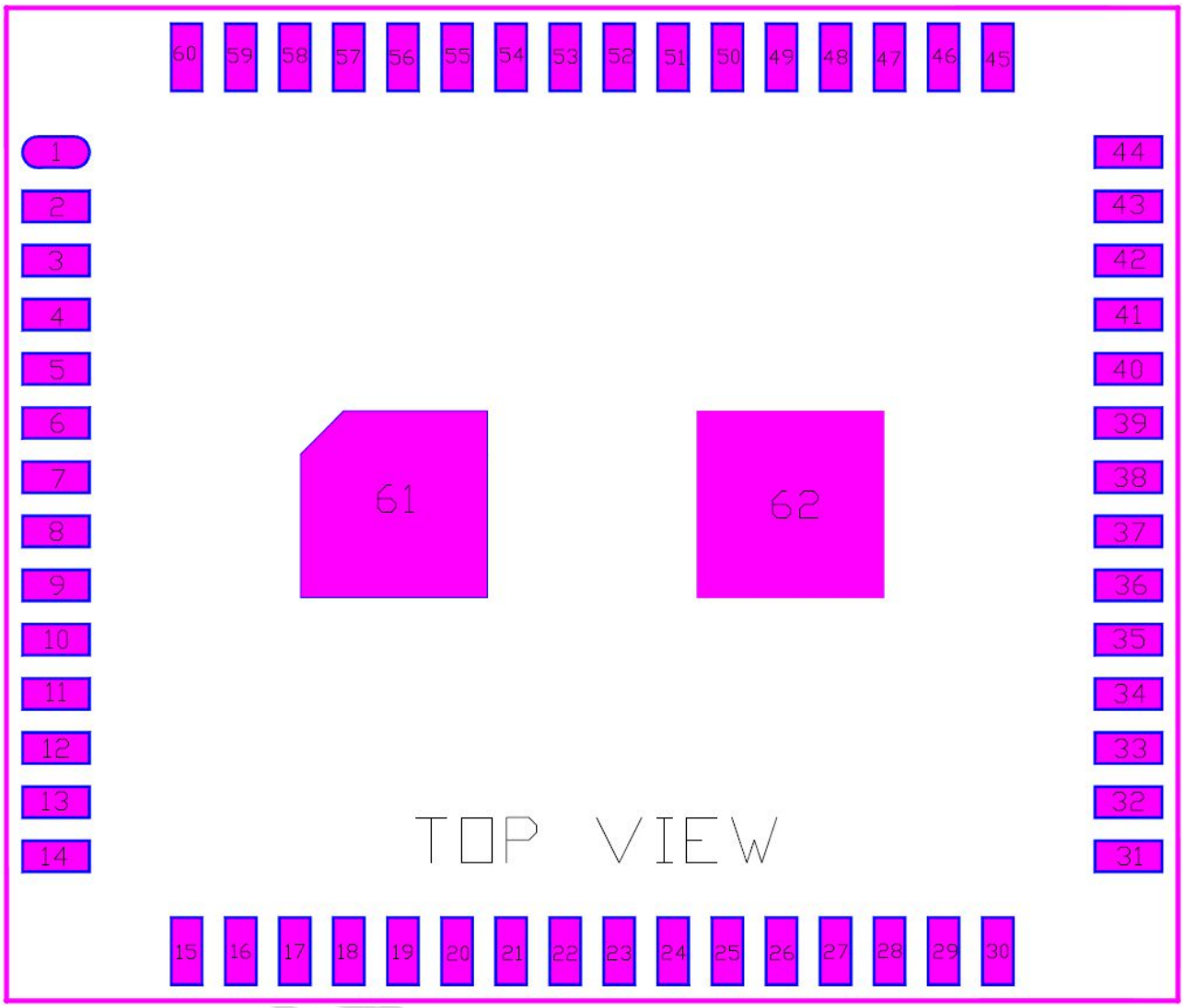
The SiP module will conform to the following pin map, shown in the following diagram (top view)

Pin	Definition	I/O	Description
1	NC		
2	GND		Ground pin
3	GND		Ground pin
4	PC0	I/O	MCU pin name: PC0
5	PC1	I/O	MCU pin name: PC1
6	PC2	I/O	MCU pin name: PC2

7	PC3	I/O	MCU pin name: PC3
8	NC		
9	NC		
10	NC		
11	NC		
12	NRST		Hardware reset pin
13	PA0	I/O	MCU pin name: PA0
14	GND		Ground pin
15	GND		Ground pin
16	PA2_TXD_A	I/O	MCU pin name: PA2
17	PA3_RXD_A	I/O	MCU pin name: PA3
18	PA4_SPI1_NSS	I/O	MCU pin name: PA4
19	PA5_SPI1_SCK	I/O	MCU pin name: PA5
20	PA6_SPI1_MISO	I/O	MCU pin name: PA6
21	PA7_SPI1_MOSI	I/O	MCU pin name: PA7
22	PC4	I/O	MCU pin name: PC4
23	PC5	I/O	MCU pin name: PC5
24	PB0_IO_INT1	I/O	MCU pin name: PB0
25	PB1_IO_INT2	I/O	MCU pin name: PB1
26	PC6	I/O	MCU pin name: PC6
27	PC7	I/O	MCU pin name: PC7
28	PC8	I/O	MCU pin name: PC8
29	PC9	I/O	MCU pin name: PC9
30	RXTX/RFMOD	O	Control signal from SX1278, which connects to internal RF switch at the same time.

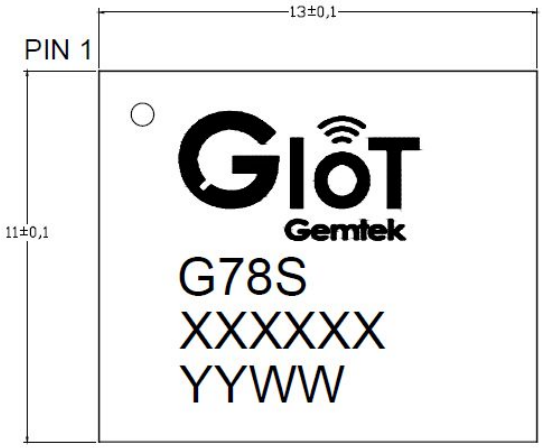
31	GND		Ground pin
32	GND		Ground pin
33	RF_ANT	I/O	RF I/O
34	GND		Ground pin
35	GND		Ground pin
36	PA1_RF_FEM_CPS	I/O	MCU pin name: PA1
38	GND		Ground pin
38	NC		
39	GND		Ground pin
40	NC		
41	GND		Ground pin
42	NC		
43	VDD33		Power Supply
44	VDD33		Power Supply
45	PA8_USART1_CK	I/O	MCU pin name: PA8
46	PA10_USART1_RX	I/O	MCU pin name: PA10
47	PA9_USART1_TX	I/O	MCU pin name: PA9
48	PA11_USART1_CTS	I/O	MCU pin name: PA11
49	PA12_USART1_RTS	I/O	MCU pin name: PA12
50	PA13_SWDIO		Serial wire (SWD) debug interface
51	PA14_SWCLK		Serial wire (SWD) debug interface
52	PC10	I/O	MCU pin name: PC10

53	PC11	I/O	MCU pin name: PC11
54	PC12	I/O	MCU pin name: PC12
55	PD2	I/O	MCU pin name: PD2
56	PB5	I/O	MCU pin name: PB5
57	PB6_SCL	I/O	MCU pin name: PB6
58	PB7_SDA	I/O	MCU pin name: PB7
59	BOOT0	I	Boot mode selection pin
60	PB8_IO_LED_FCT	I/O	MCU pin name: PB8
61	GND		Ground Pin
62	GND		Ground Pin

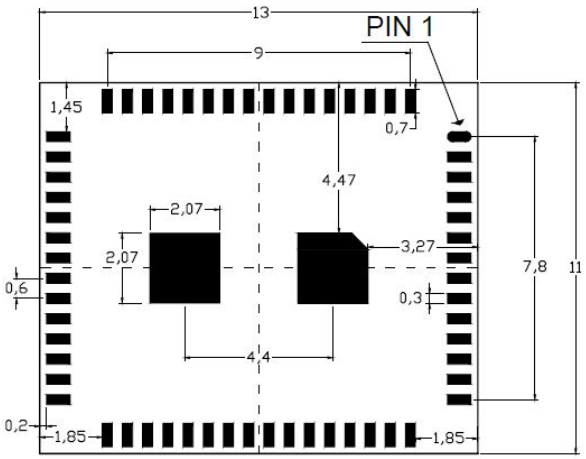


4. Mechanical Dimension

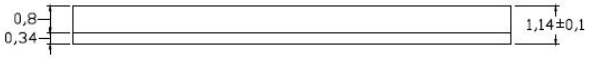
Unit: mm



TOP VIEW



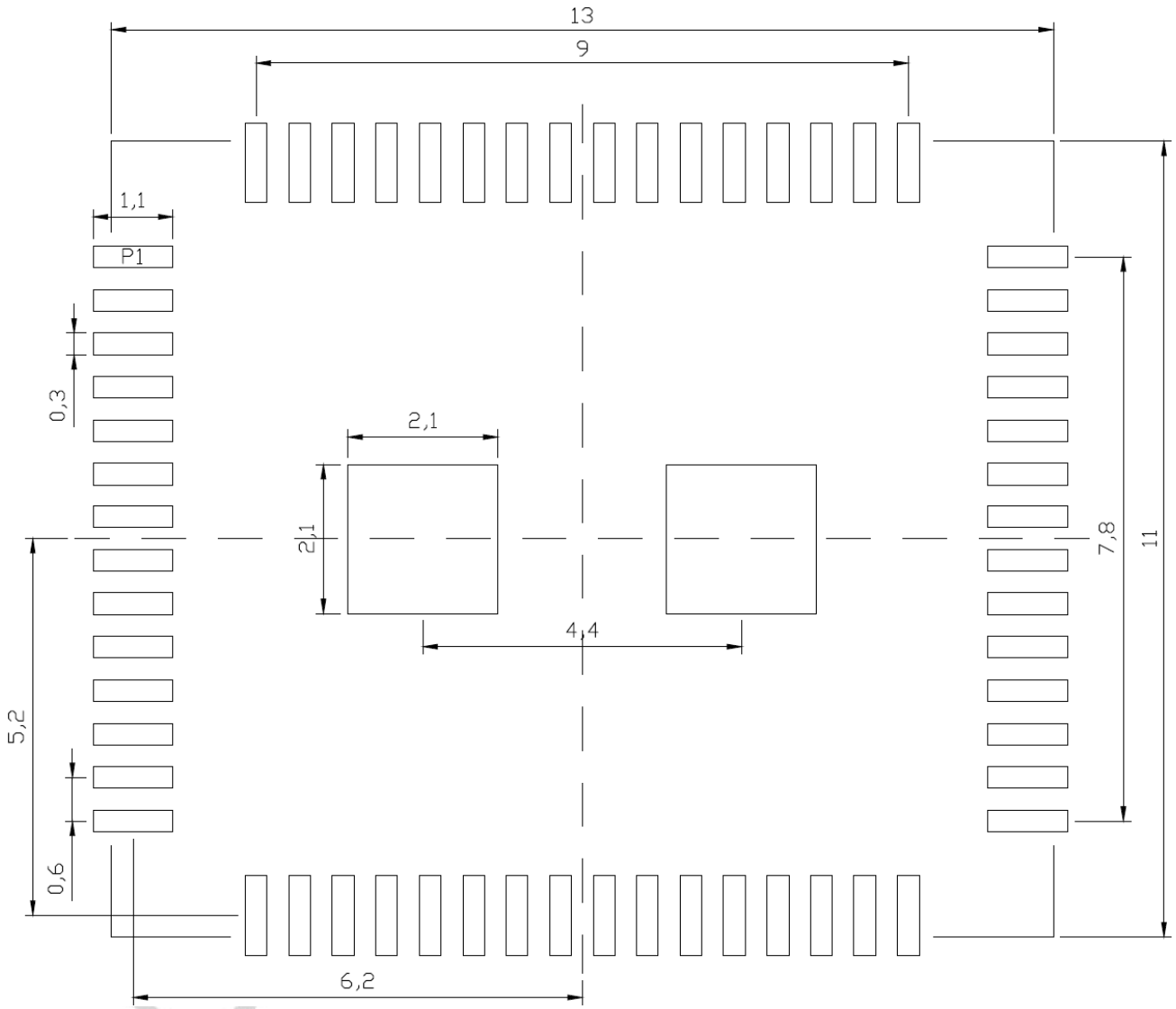
BOTTOM VIEW



SIDE VIEW

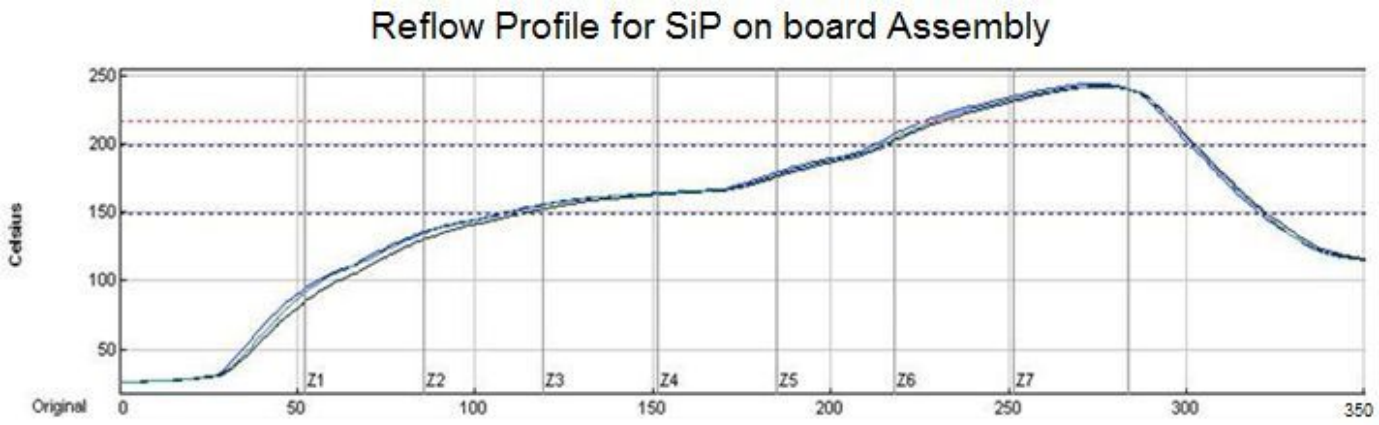
4-1 Recommended Footprint

Unit: mm



TOP View

5. Recommended Reflow Profile



Preheat time	150℃—200℃: 105+/-15sec
Dwell time	Over 220℃: 70+5/-10 sec
Peak Temp	240 +10/-5℃
Ramp Up/Down Rate	Up: 3 +0/-2 ℃/ sec Down: 2 +0/-1℃/ sec

6. SiP Module Preparation

6-1. Handling

Handling the module must wear the anti-static wrist strap to avoid ESD damage. After each module is aligned and tested, it should be transport and storage with anti -static tray and packing. This protective package must be remained in suitable environment until the module is assembled and soldered onto the main board.

6-2. SMT Preparation

1. Calculated shelf life in sealed bag: 6 months at<40℃ and <90% relative humidity (RH).
2. Peak package body temperature: 250℃.
3. After bag was opened, devices that will be subjected to reflow solder or other high temperature process must.
   A. Mounted within: 168 hours of factory conditions<30℃/60%RH.
   B. Stored at≦10%RH with N2 flow box.
4. Devices require baking, before mounting, if:
   A. Package bag does not keep in vacuumed while first time open.
   B. Humidity Indicator Card is >10% when read at 23±5℃.
   C. Expose at 3A condition over 8 hours or Expose at 3B condition over 24 hours.
5. If baking is required, devices may be baked for 12 hours at 125±5℃.

7. Package Information

7-1. Product Marking

Figure 1 below details the standard product marking for all Gemtek products. Cross reference to the applicable line number and table for a full detail of all the variables.

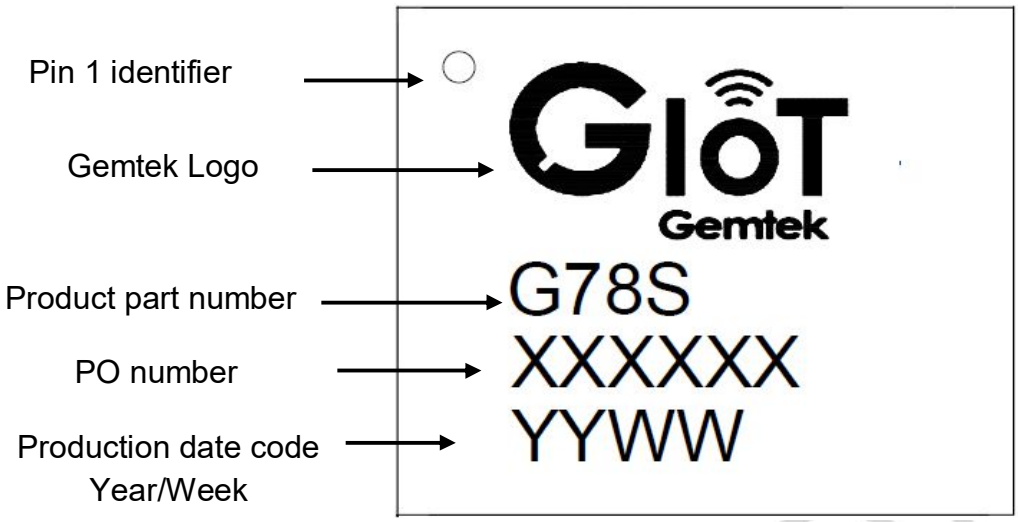
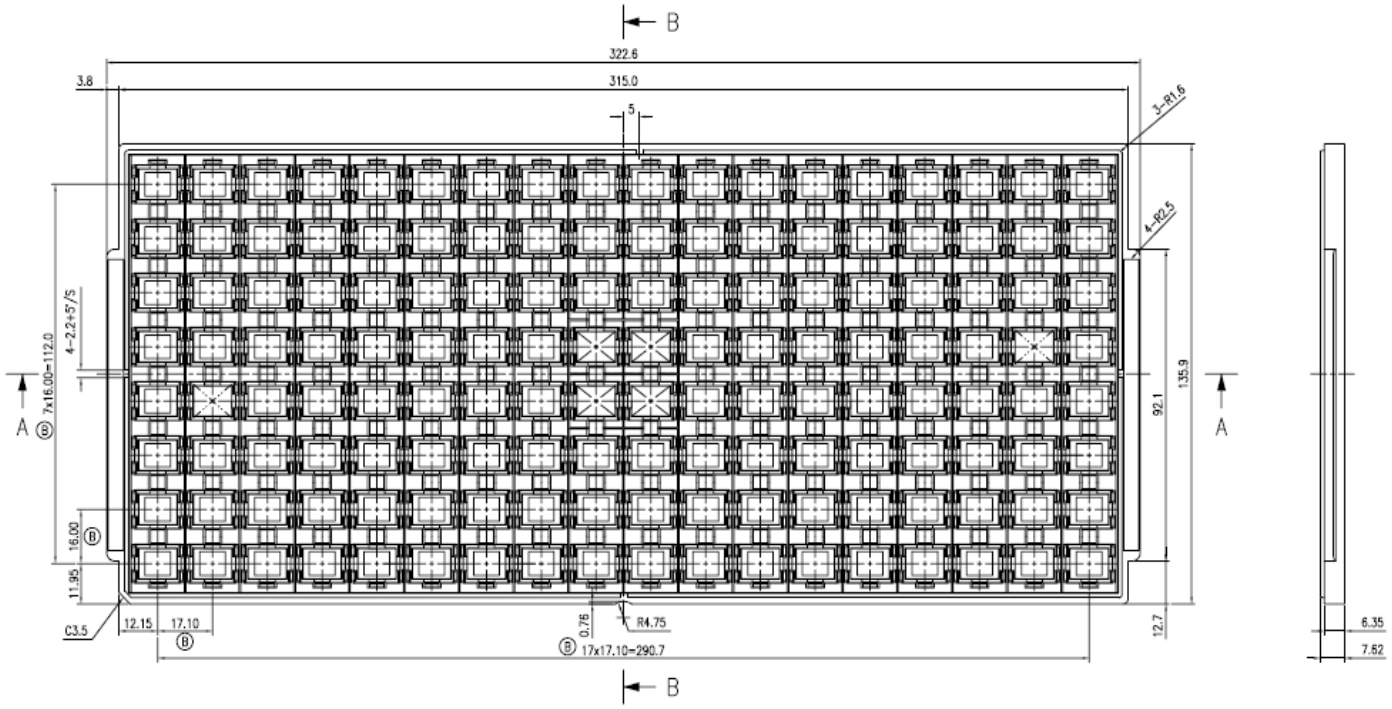
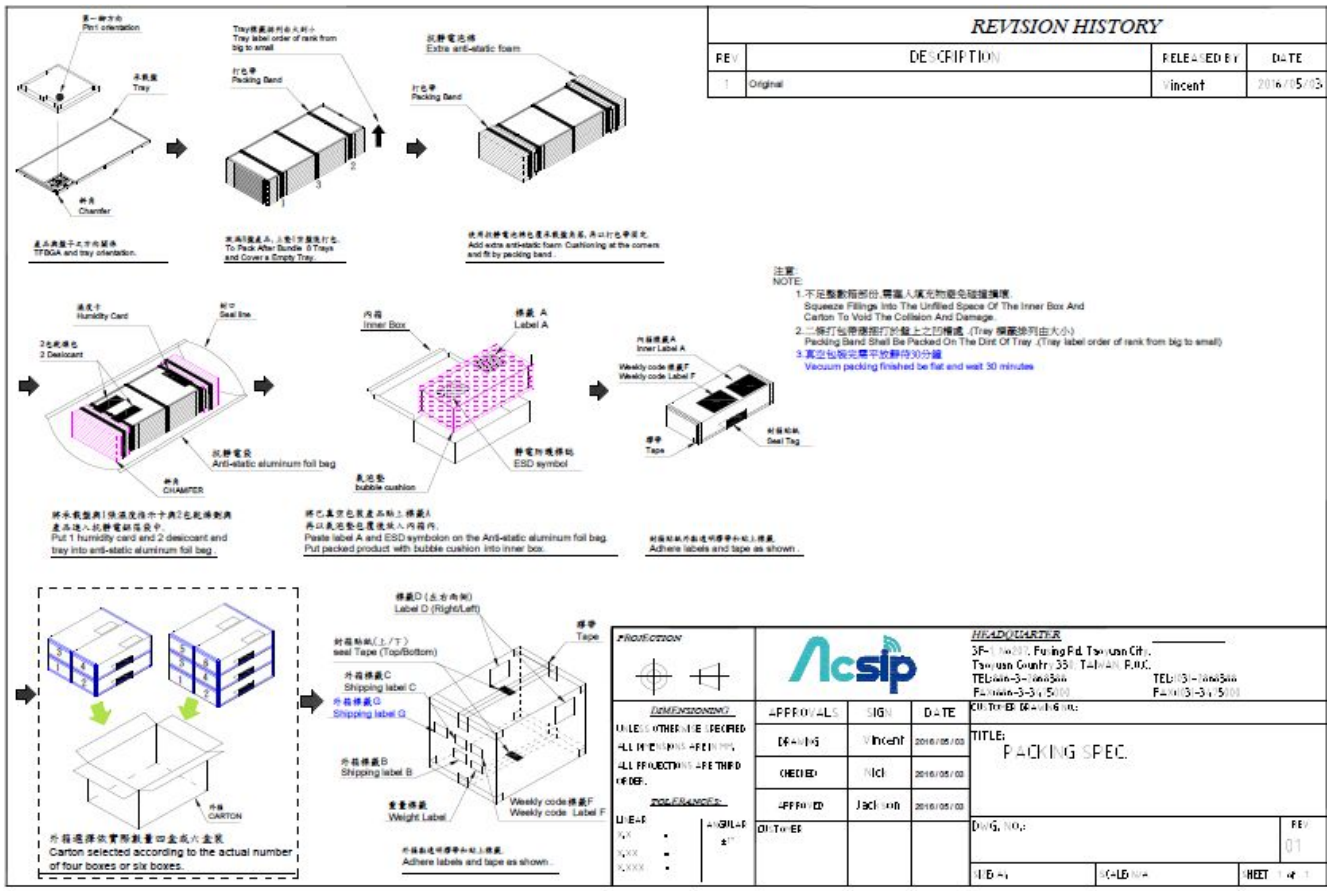


Figure 1 Standard Product Marking Diagram- TOP VIEW

7-2. Tray Dimension



7-3. Packing Information



7-4. Humidity Indicator Card

Dry Wet

Indicates 指示點:
10%,20%,30,40%,50%,60% relative humidity
10%,20%,30,40%,50%,60% 相對濕度

Color Change 顏色變化:
Brown (Dry) ---> Blue (Wet)
棕色 (乾燥) ---> 藍色 (潮溼)