This document is for the sole use of Giovanni Ferreira of Aluno



# **Course Prerequisites**

Before taking this course, you need to have:

- Basic computer literacy you must know how to use a shell and editor of your choice and navigate the file system.
- A basic understanding of digital hardware design and verification.
- Knowledge of a procedural programming language will facilitate your learning experience.

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# **Course Objectives**

In this course, you:

- Use fundamental Verilog language constructs required for design, verification and logic synthesis.
- Analyze and ensure that Verilog designs meet the requirements for synthesis.
- Compare mismatches that can happen between pre-synthesis and post-synthesis simulation and the process of synthesis.
- Debug digital designs by developing Verilog test environments of significant capability and complexity.
- Apply system tasks and functions to verify digital designs using the Xcelium™ Simulator.

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## **Course Agenda**

#### Day 1

- Describing Verilog Applications
  - Lab: Exploring the VeriRISC CPU Design
- Verilog Introduction
  - Lab: Modeling an Address Multiplexor
- Choosing Between Verilog Data Types
  - Lab: Modeling a Data Driver
- Using Verilog Operators
  - Lab: Modeling the Arithmetic Logic Unit

#### Day 2

- Making Procedural Statements
- Lab: Modeling a Controller
- Using Blocking and Nonblocking Assignments
  - Lab: Modeling a Generic Register
- Using Continuous and Procedural Assignments
  - Lab: Modeling a Single-Bidirectional-Port Memory
- Understanding the Simulation Cycle
  - Lab: Modeling a Generic Counter
- Using Functions and Tasks
  - Lab: Modeling the Counter Using Functions
  - Lab: Modeling the Memory Test Block Using Tasks
- Directing the Compiler
  - Lab: Verifying the VeriRISC CPU Design

#### Day 3

- Introducing the Process of Synthesis
  - Lab: Exploring the Synthesis Process
- Coding RTL for Synthesis
  - Lab: Using a Component Library
- Designing Finite State Machines
  - Lab: Coding State Machines in Multiple Styles
- Avoiding Simulation Mismatches
- Managing the RTL Coding Process
- Managing the Logic Synthesis Process
- Coding and Synthesizing an Example Verilog Design
  Lab: Coding a Serial-to-Parallel Interface Receiver

#### Day 4

- Using Verification Constructs
  - Resolving a Deadlocked System
- Coding Design Behavioral Algorithmically
- Using System Tasks and System Functions
- Adding System Tasks and System Functions to a Beverage Dispenser Design
- Generating Test Stimulus
  - Verifying a Serial Interface Receiver
- Developing a Testbench
  - Testing a VeriRISC CPU Model
- Example Verilog Testbench
  - Developing a Script-Driven Testbench Using Verilog 1995
  - Developing a Script-Driven Testbench Using Verilog 2001

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## **Software and Licenses**

For the software and licenses used in the labs for this course, go to:

https://www.cadence.com/en\_US/home/training/all-courses/82110.html

If there is additional information regarding the specific software, it is detailed in the lab document and/or the README file of the database provided with this course.

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  - Stand apart from your peers





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### How do I register to take the exam?

 Log in to our <u>Learning Management System</u>, click on the course in your transcript, and go to the Content tab to locate the exam.

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# **Icons Used in This Class**



Best Practice



Language Syntax



Concept/ Glossary

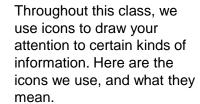


Frequently Asked Questions / Quiz





Error Message







Quick Reference







Lab List

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