Module 25

Course Conclusions

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This page does not contain notes.

What This Training Covered

You can now appropriately and effectively utilize fundamental Verilog constructs for Design and Verification.

Topics

- Introduction
- Fundamentals
- Value set and data types
- Operators
- Procedural statements
- Compiler directives
- Simulation cycle
- Logic synthesis introduction
- Coding RTL for synthesis
- Avoiding simulation mismatches
- Designing finite-state machines
- Verification constructs
- Functions and Tasks
- System tasks and system Functions
- Testbench development and application

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You can now start developing Verilog testbenches. Although Verilog is primarily a hardware design language, it does have nontrivial testbench capability and the year 2001 update significantly increased those capabilities. Verification personnel have developed very powerful testbenches over the more than two decade life of Verilog, starting long before it became a standard.

Any verification team you work with will almost undoubtedly have their own conventions you need to follow. What this module therefore presented was the “nuts and bolts”, i.e., the basics of Verilog design verification. You should consider this to be only the beginning of your learning.

Additional Resources

Standards

- IEEE Std 1364™-2005 Verilog Hardware Description Language
- IEEE Std 1364.1™-2002 Verilog RTL Synthesis

Cadence Documentation

- Verilog-XL Reference

Internet Community

- Accellera
- EDA.ORG
- FAQ: Comp.lang.verilog
- Verilog DOT COM

Publications

- Moorby, Philip R., and Donald E. Thomas. *The Verilog Hardware Description Language*. Springer Science+Business Media, 2002.

Here are some additional resources to help you with your Verilog projects:

- The IEEE Std 1364-2005 Verilog Hardware Description Language Reference Manual defines the Verilog language. This standard is unfortunately not free.
- The Cadence Verilog-XL Reference documents the Verilog language that it accepts. The Verilog language standard has diverged only slightly. This document is free to licensed users of the Cadence digital simulation tools.
- These are some of the most obvious internet resources. Many alternative internet resources are also available.
- The author lists this book in tribute to Verilog founder Philip Moorby. Many alternative books are also available.