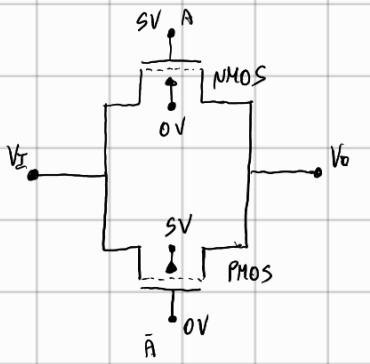
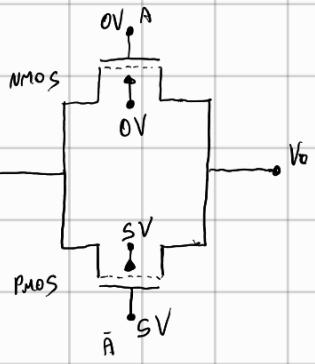


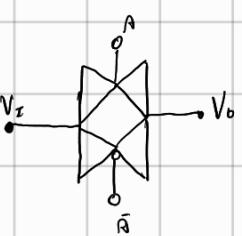
# ① PORTA DI TRASMISSIONE CMOS



STATO ON

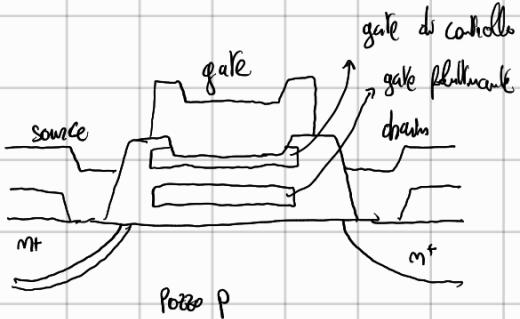


STATO OFF

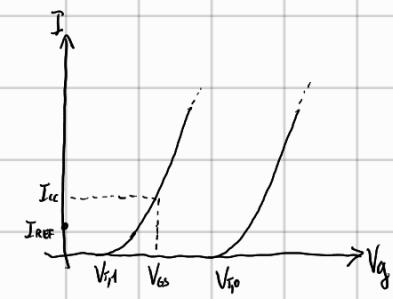


SCHEMA CIRCUITALE

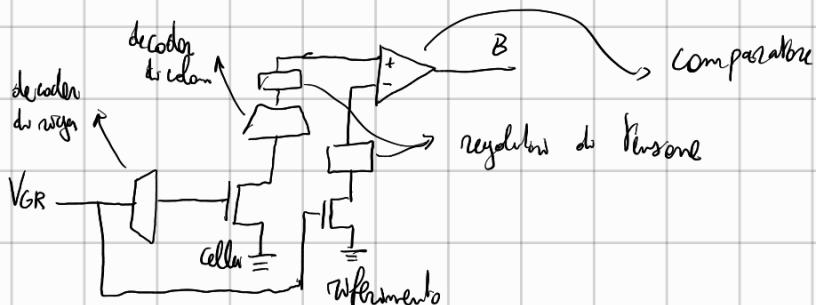
# ② CELLA DI MEMORIA FLASH



(A) SCHEMA CELLA

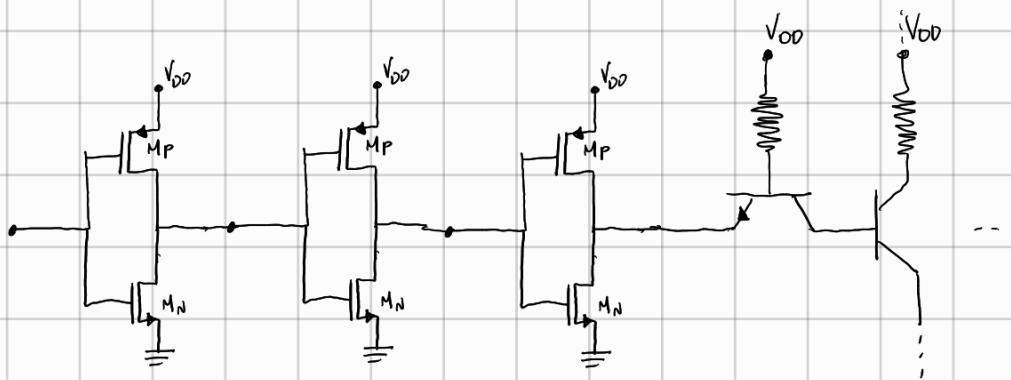


(B) SCHEMA MEMORIZZAZIONE INFO



(C) SCHEMA SISTEMA DI INTERROGAZIONE

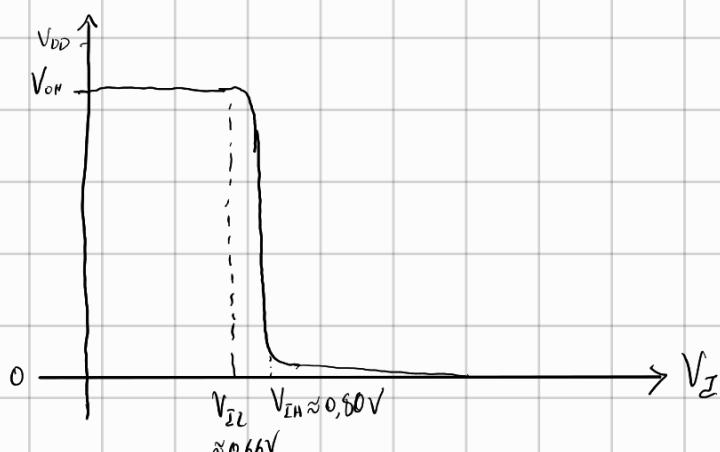
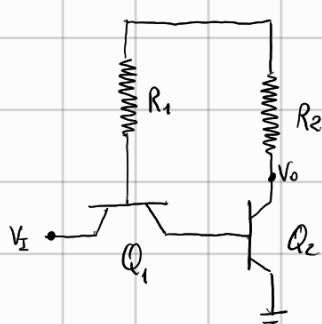
### ③ SCHEMA INTERFAZIAMENTO CMOS-TTL



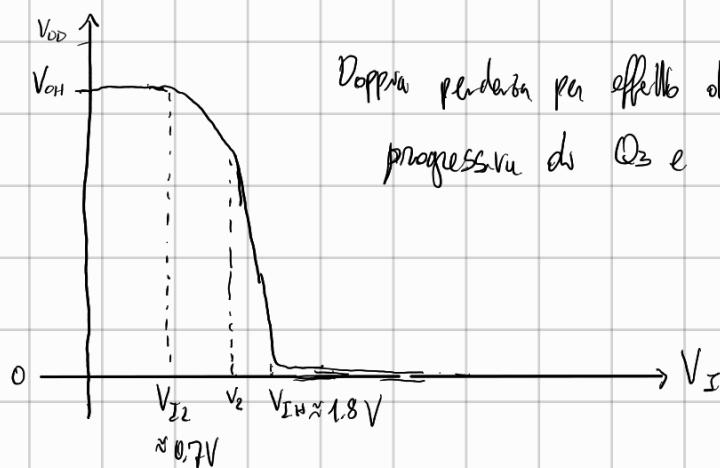
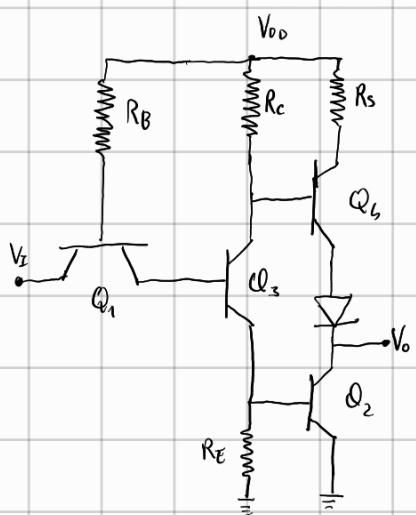
### ④ INVERTITORE NMOS A SVUOTAMENTO [BLANK]

### ⑤ PORTA TTL

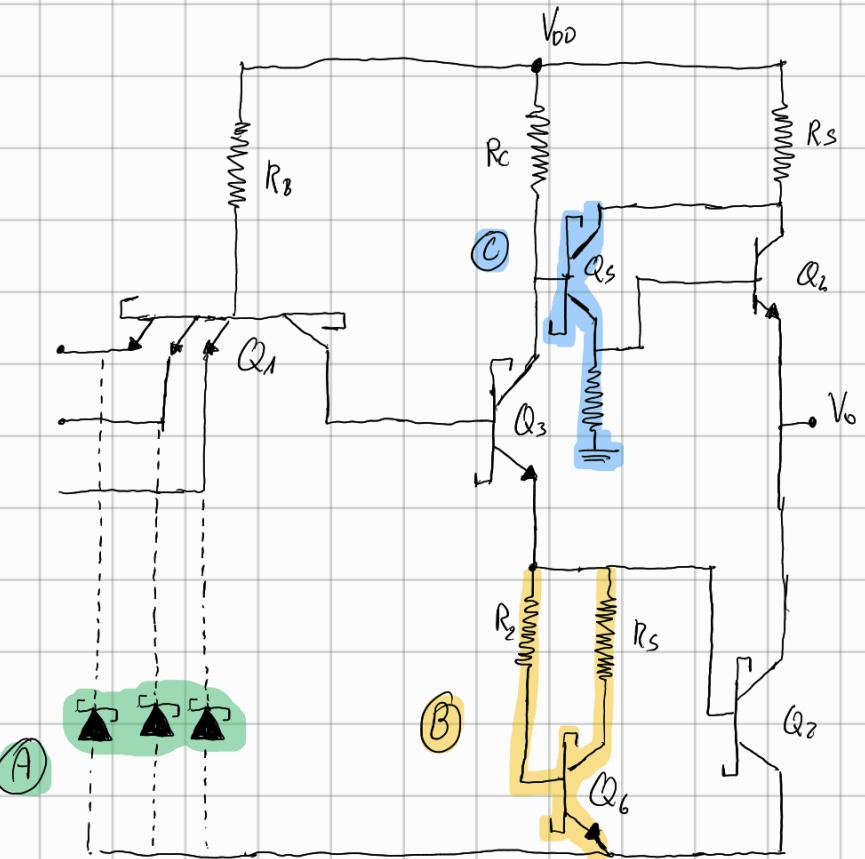
TTL elementare :



TTL Standard:



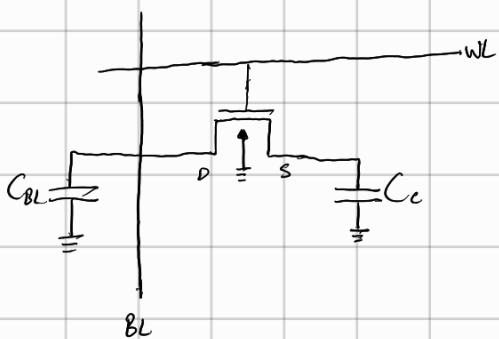
Quando si accende  $Q_3$ , la sua corrente di collettore fa abbassare leggermente la  $V_o$ . All'accensione di  $Q_2$  si ha una discesa molto più rapida.



(C) SCHEMA TTL SHOTTKY VELOCE

(6) FUNZIONI LOGICHE CMOS [BLANK]

(7) CELLE DI MEMORIA DINAMICHE (1-T)

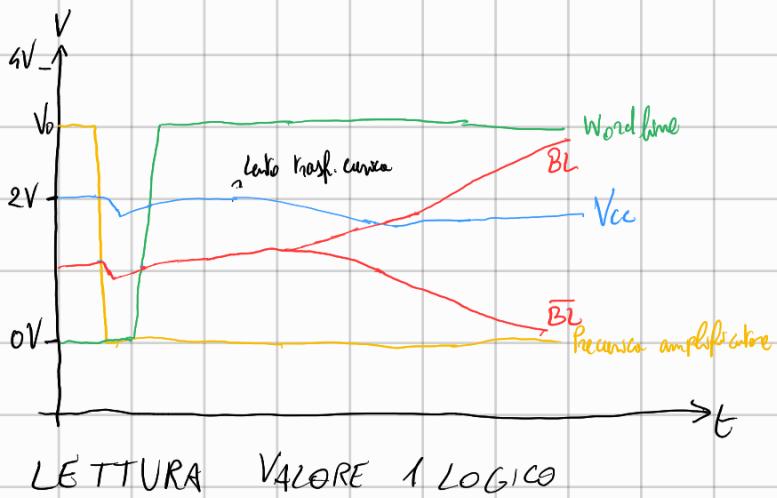


(A) SCHEMA CELLA

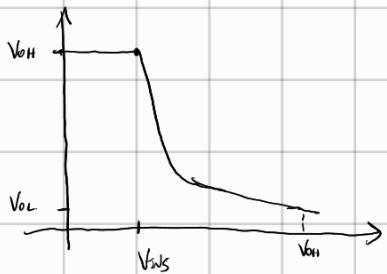
(B) FORMULA RIDISTRIBUZIONE CARICA

$$\Delta V_t = V_f - V_{BL} = \frac{V_c - V_{BL}}{\frac{C_{BL}}{C_c} + 1}$$

### ⑦ SCHEMA RIDISTRIBUZIONE + GRAFICO

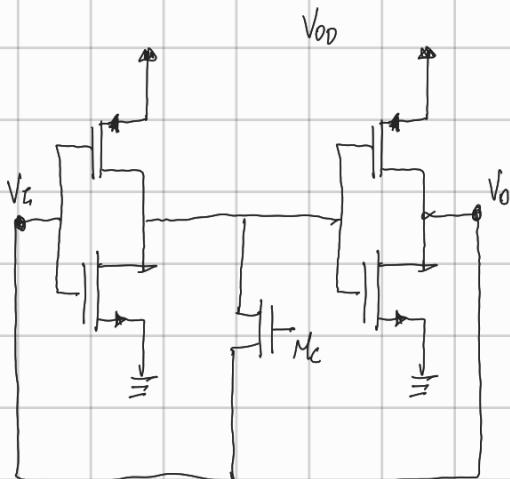


### ⑧ INVERTORI NMOS IN SATURAZIONE



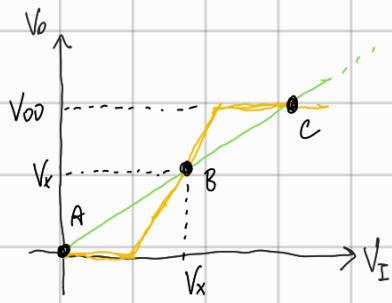
(A) CARATTERISTICA DI TRANSFERIMENTO

### ⑨ AMPLIFICATORE DI LETTURA

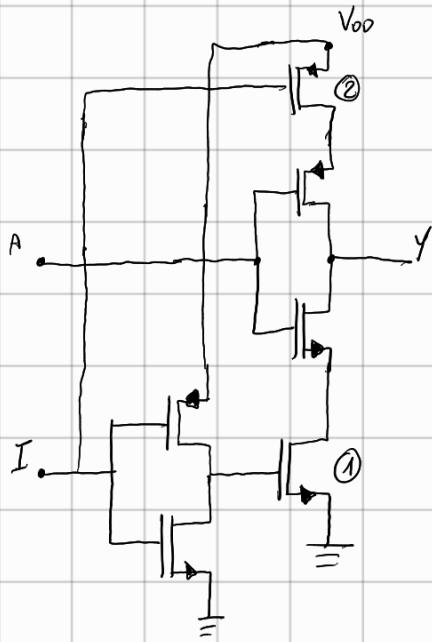


(A) SCHEMA CMOS

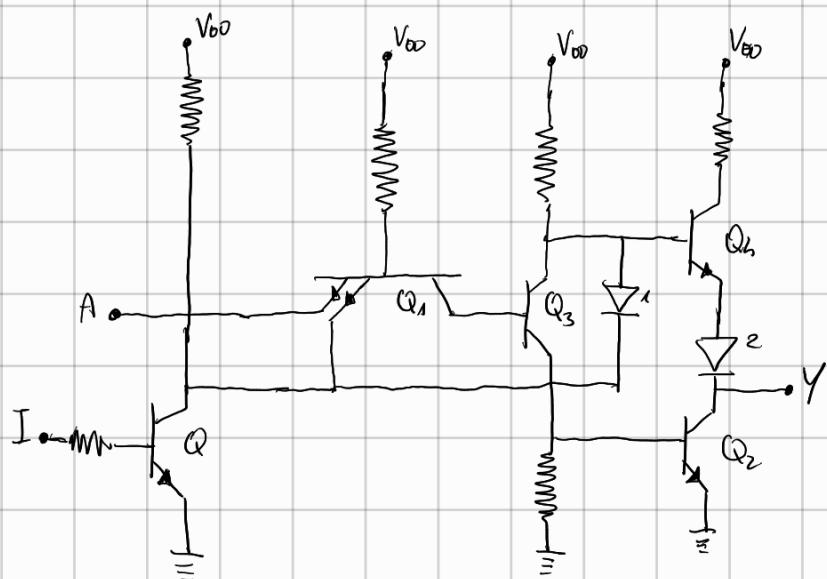
(B) GRAFICO DI FUNZIONAMENTO



⑩ PORTE TRISTATE

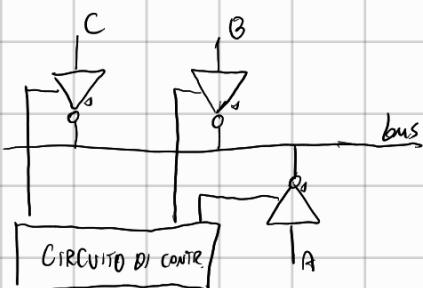


(A) CMOS



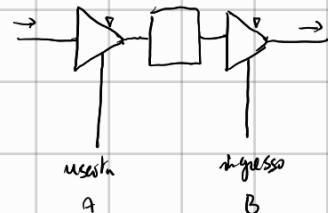
(B) TTL

APPLICAZIONI



(A) BUS

(B) BUFFER BIDIREZIONALE

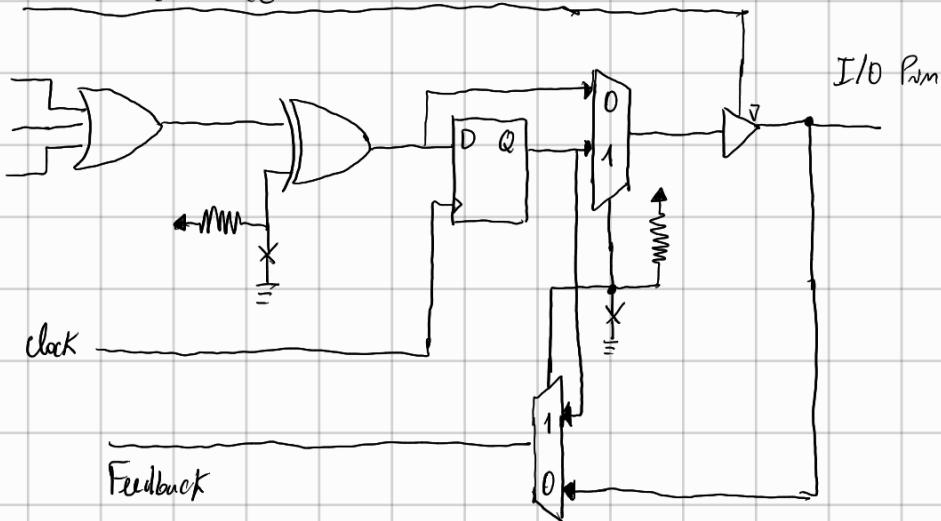


(C) TERMINALE I/O

## 11 MACROCELLE DI USCITA

### SCHEMA COMPLETO

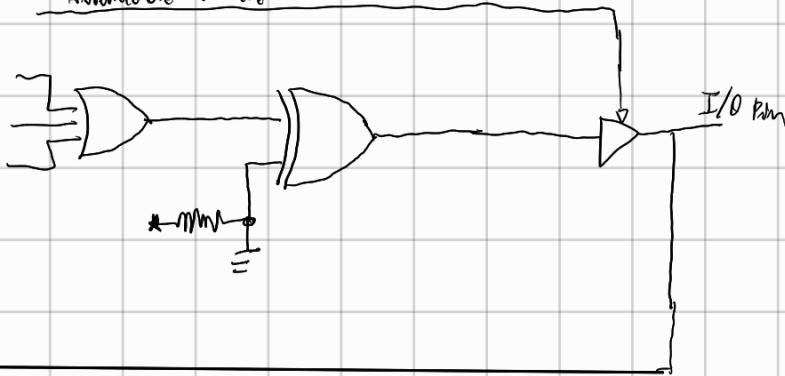
Abilitazione Twstate



### MODALITÀ COMBINATORIA

Abilitazione Twstate

MUX impostato su uscita 0

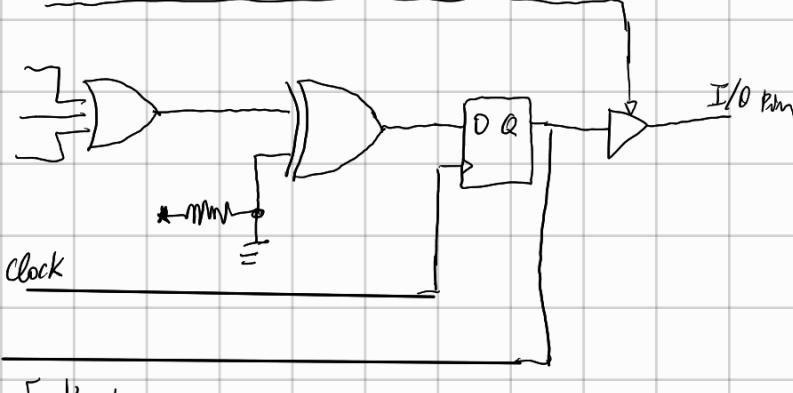


Feedback

### MODALITÀ SEQUENZIALE

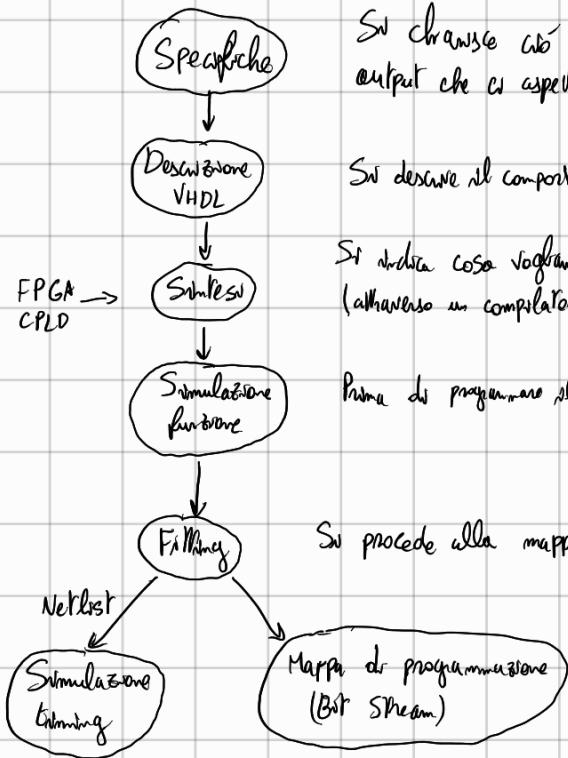
Abilitazione Twstate

MUX impostato su uscita 1



Feedback

## 12 SISTEMI LOGICI COMPLESSI



Si descrive ciò che deve fare il nostro sistema logico, gli input che deve ricevere e gli output che ci aspettiamo.

Si descrive il comportamento con una sintassi astratta che viene poi interpretata durante la sintesi.

Si indica cosa vogliamo programmare e viene interpretata la descrizione fornita nel passaggio precedente (attraverso un compilatore).

Prima di programmare il circuito, la funzione viene simulata per confermare il comportamento che ci aspettiamo.

Si procede alla mappatura dello schema sul circuito.

Viene eseguita una

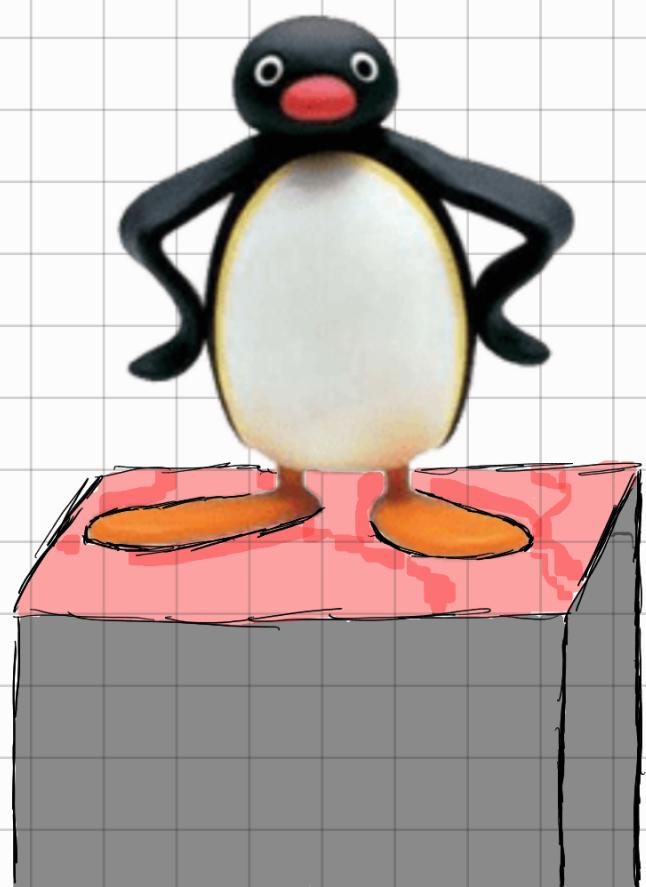
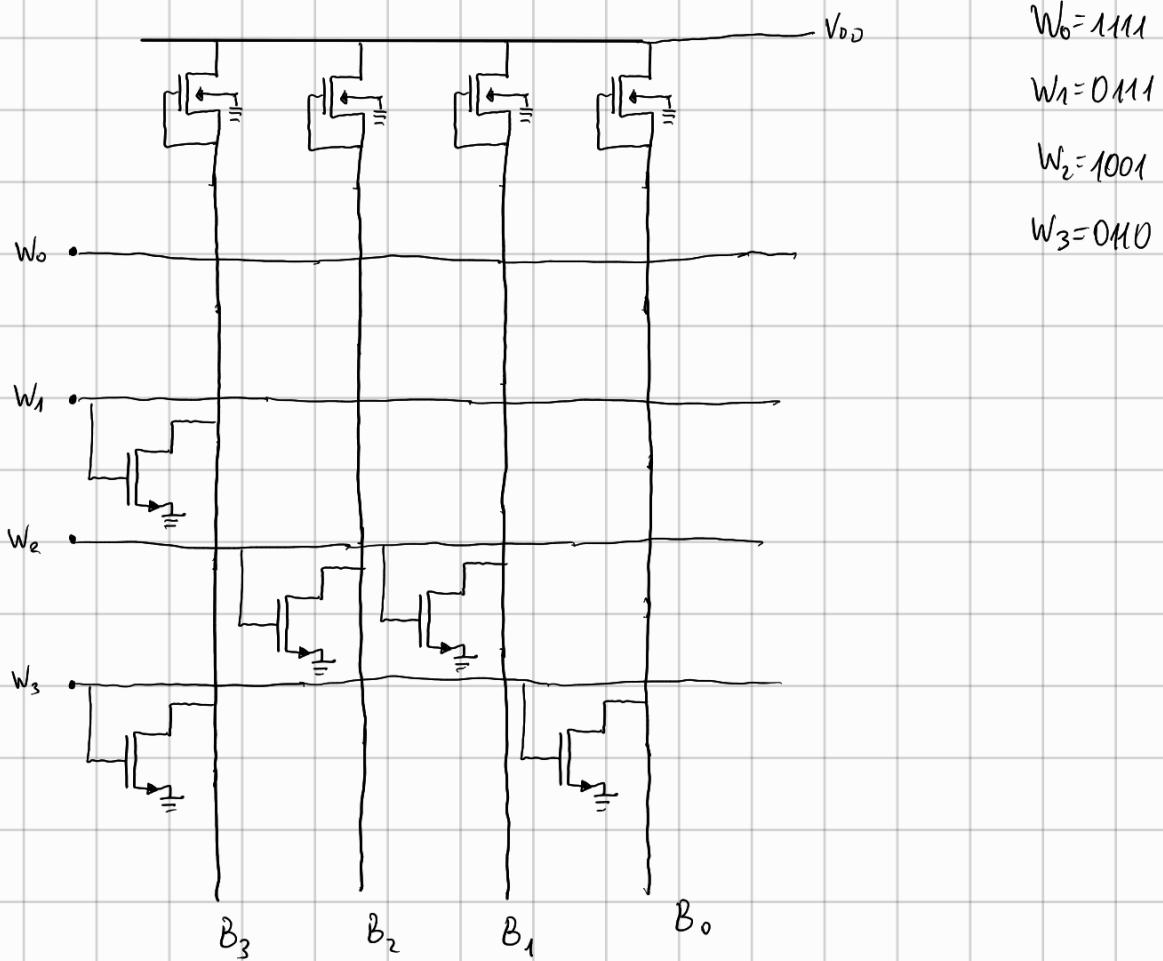
Simulazione del timing prima

della scrittura dell'ivra

Viene generato lo stream e gli interruttori programmabili sono

selezionati al valore richiesto della funzione logica.

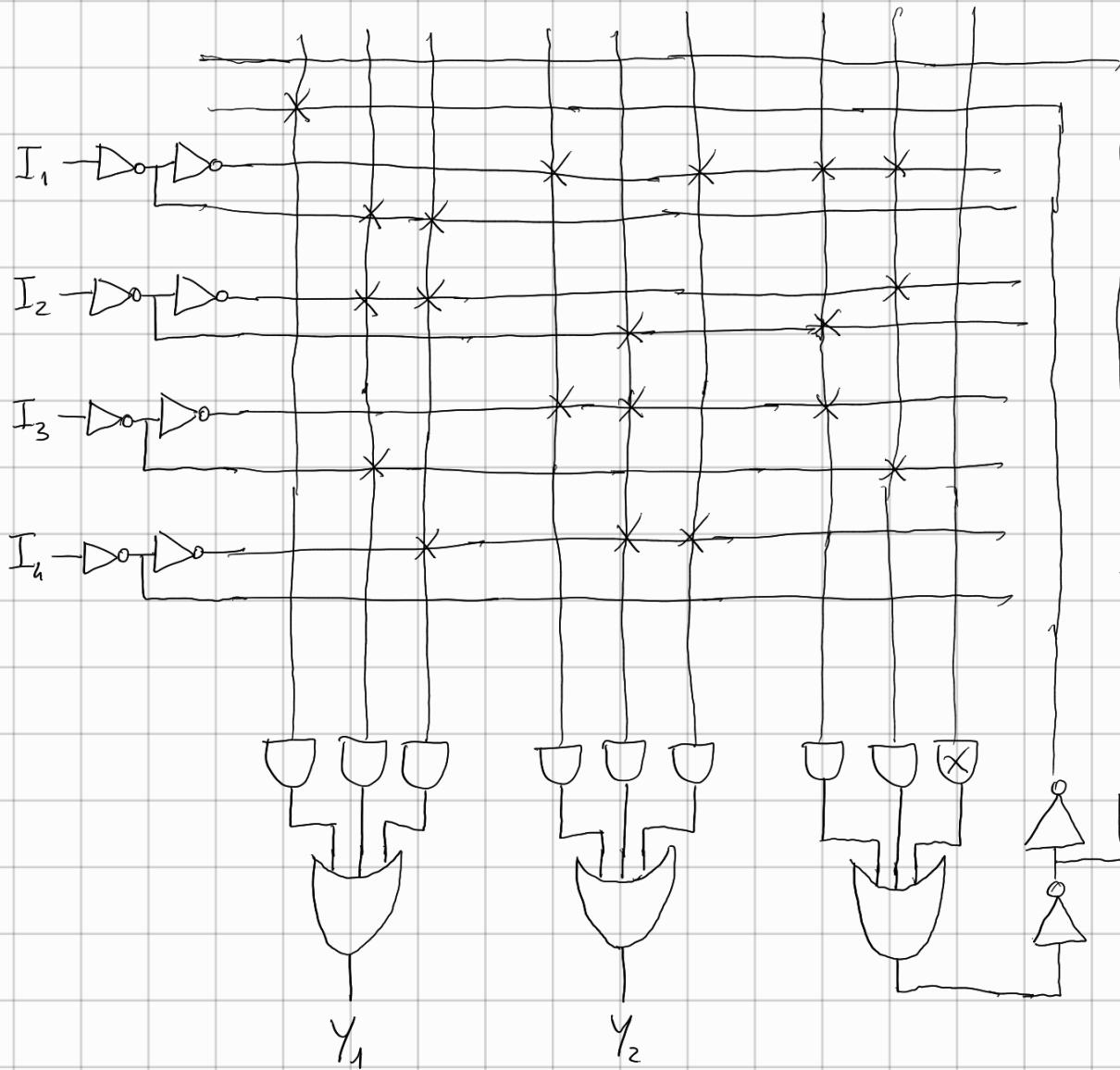
(13) MEMORIE ROM NMOS



## ⑭ DISPOSITIVI PAL

$$Y_1 = I_1 \bar{I}_2 I_3 + I_1 I_2 \bar{I}_3 + \bar{I}_1 I_2 \bar{I}_3 + \bar{I}_1 I_2 I_4$$

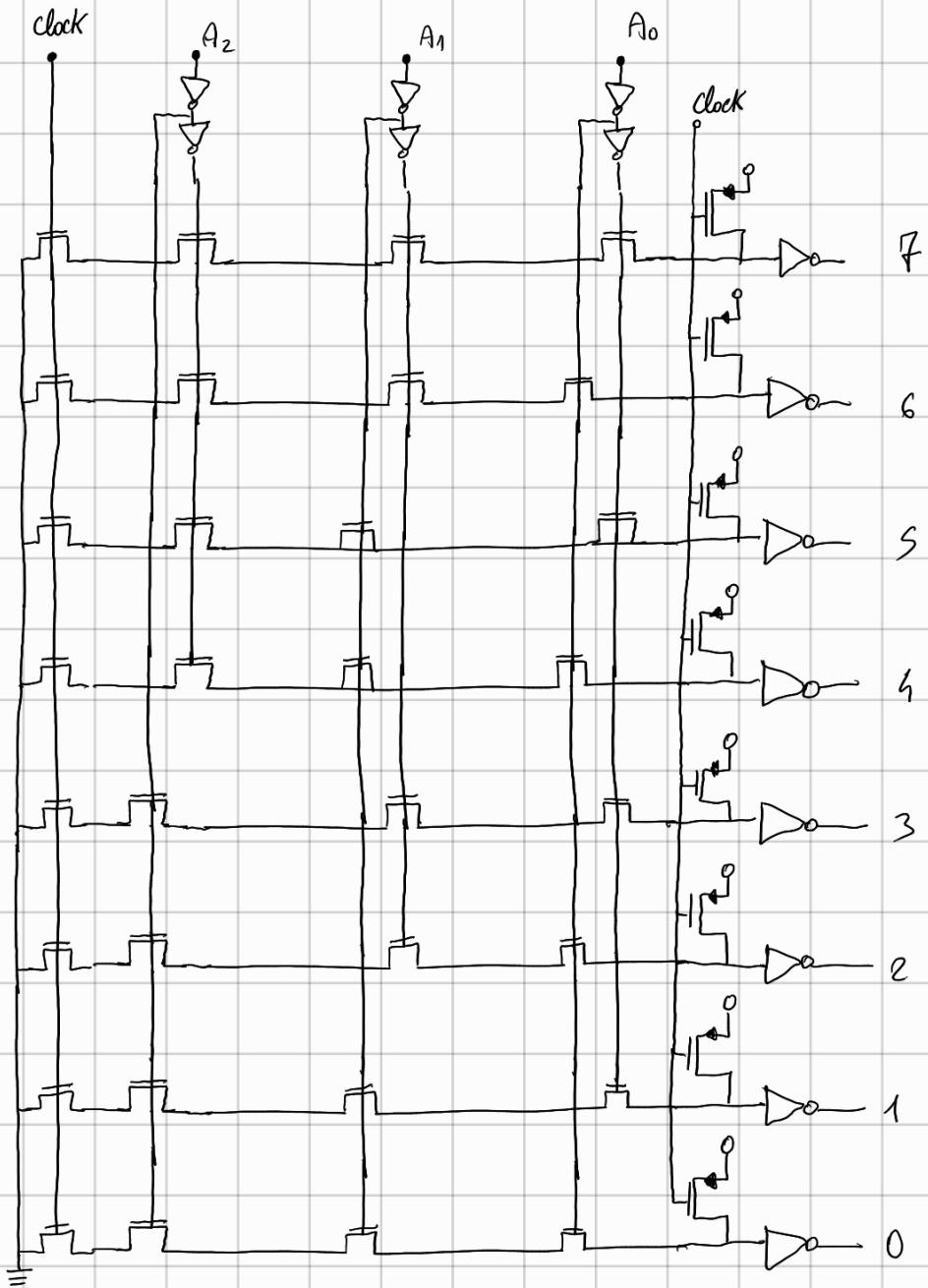
$$Y_2 = I_1 I_3 + \bar{I}_2 \bar{I}_3 I_4 + I_1 I_4$$



$$Y_3 = I_1 \bar{I}_2 I_3 + I_1 I_2 \bar{I}_3$$

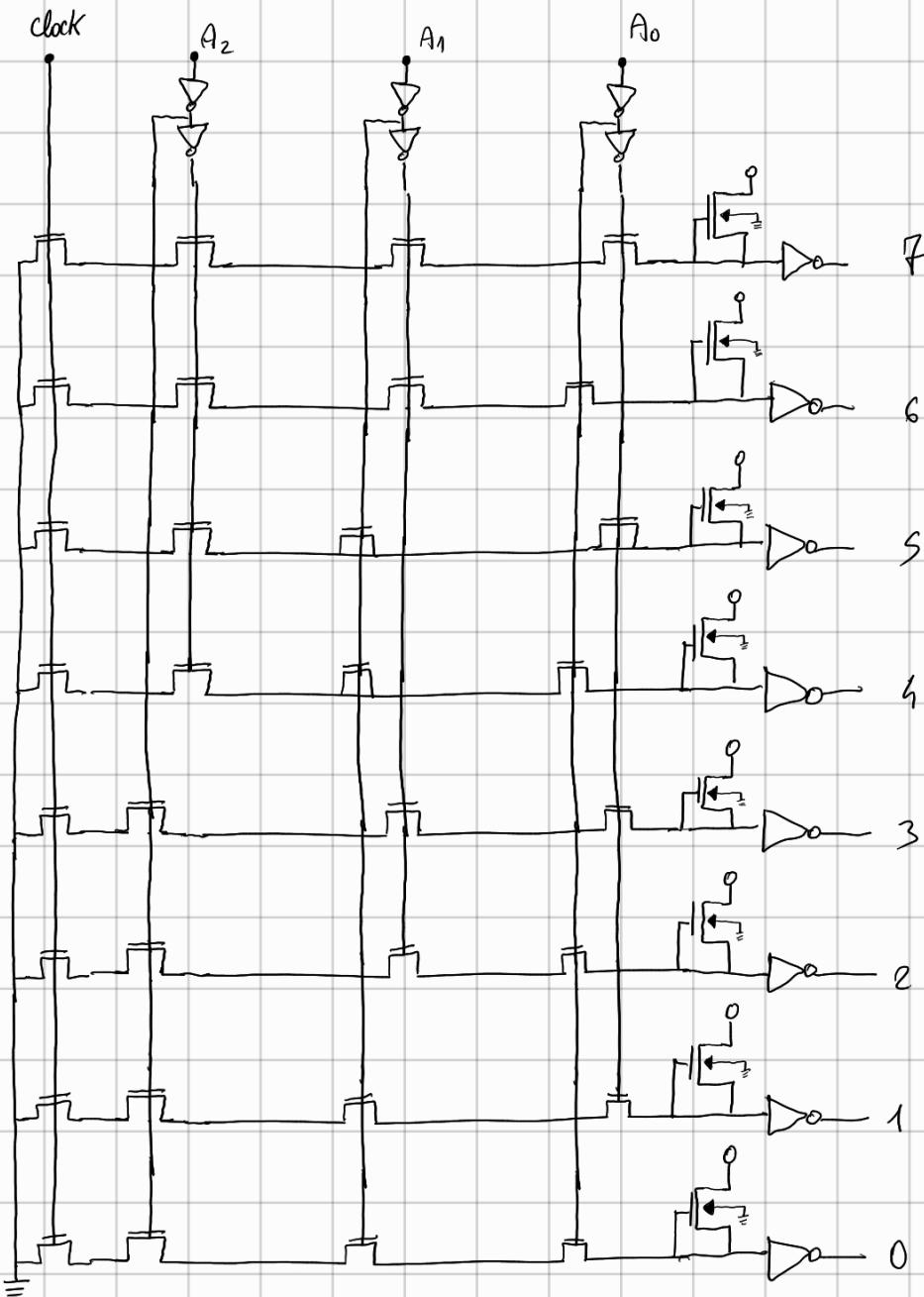
(15) DECODIFICATORE A 3 BIT

[CMOS]



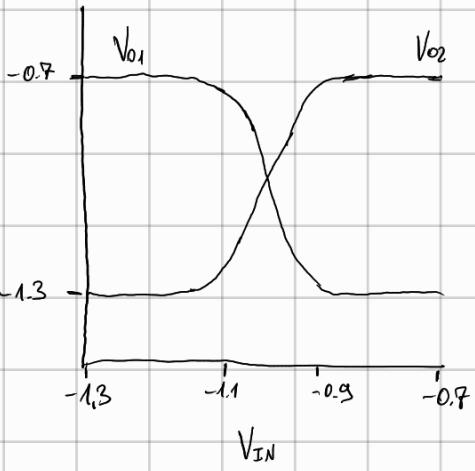
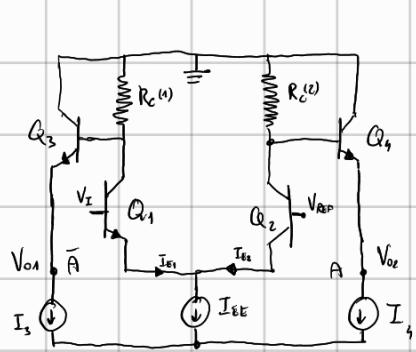
[N MOS]

(Non confermato, ma dovrebbe essere così).



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## INVERTITORE ECL



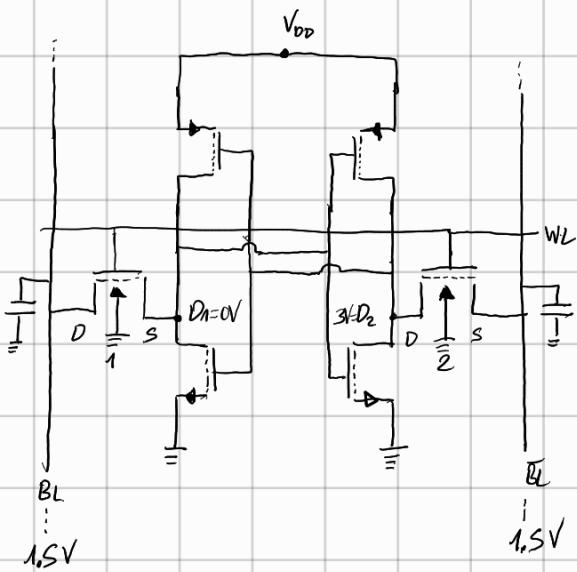
Ⓐ SCHEMA CIRCUITALE

Ⓑ CARATT. DI TRASFERIMENTO

● Uscita invertente  
● Uscita non invertente

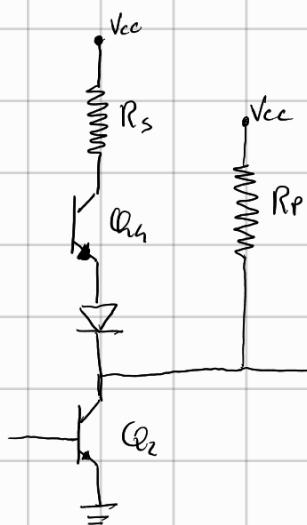
Ⓒ SCHEMA PROBLEMI USCITA INVERTENTE

(17) RAM CMOS G-T



(A) SCHEMA LETTURA 0

(18) INTERFACCIAZIONO TTL-CMOS



(A) SCHEMA INTERFACCIAZIONO

(19) FUNZIONI LOGICHE NMOS [BLANK]