Investigation of Rounding on Performance of Square GAA NW

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***Abstract*—A square shaped gate-all-around nanowire (GAA NW) was simulated using Sentaurus Device Editor (SDE) and its performance was assessed. The square GAA NW has mediocre performance that would need other compensation methods to improve. This paper aims to present our findings for a simulated square shaped GAA NW and our investigation into methods to improve its performance.**

I. Introduction

There is an interest in GAA NW because of its potential in further scaling of sub-micro electronic devices[1]. In this study, the performance of a GAA NW with a square cross-section is investigated. A 3D model of the square GAA NW was created using Sentaurus SDE, with dimensions of the square at 25nm for its length and width. A 1.2nm layer of Hafnium Dioxide (HFO_2) was deposited around the channel and lastly a thin layer of titanium nitride was coated over the channel. Fig.1 shows the GAA NW fabricated using SDE.

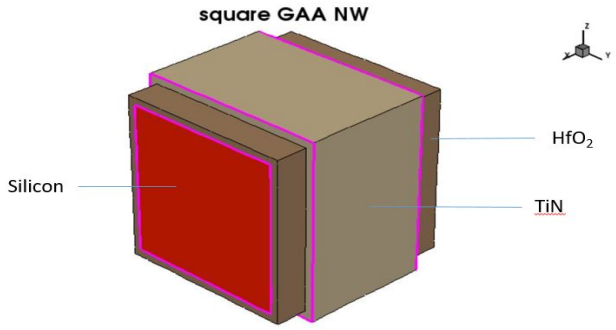


Fig. 1: 3D Model of Square GAA NW

The drain and source were doped with Arsenic (As) at a concentration of $10^{20}cm^{-3}$, creating a highly doped drain region. The channel was doped with Boron (B) at a concentration of $10^{15}cm^{-3}$.

In the subsequent sections, this paper seeks to investigate different changes that could be made to improve the performance of this square GAA NW. The device simulated as in Fig 1 is the reference device on which all other investigations will be performed.

II. Performance of Initial GAA NW

The performance of the GAA NW was assessed using the following performance parameters.

- Maximum Transconductance (g_m)
- Linear Threshold Voltage (V_{th}^{lin})
- Saturation Threshold Voltage (V_{th}^{sat})
- Drain Induced Barrier Lowering (DIBL)
- Sub-Threshold Swing (S)
- Output Conductance (g_d)
- On-Off Current Ratio

Sentaurus is very powerful and capable of producing models of the required GAA NW to very high degrees of accuracy. However, greater accuracy will inevitably lead to longer runtime. Therefore, various methods were explored to strike an acceptable compromise between accuracy and runtime.

A. Effects of Mesh

One factor which was taken into account when the model was fabricated in Sentaurus was the amount of meshing in the GAA NW. A finer or increased meshing would imply greater accuracy of the device simulated but would also increase run time exponentially. Since there was a tight time constraint in this project, a compromise had to be reached. Therefore, two simulations at different meshing levels ((2nm, 1nm) and (1nm, 0.5nm)) were conducted to determine a suitable mesh.

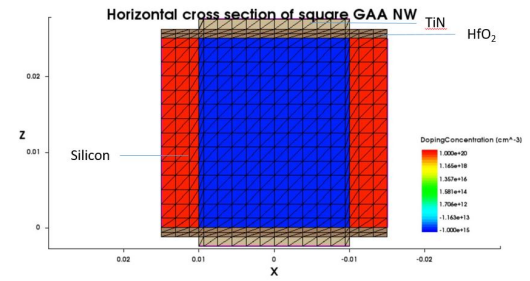
Fig.2 shows the difference in meshing between the two GAA NW.

I-V characteristics of the 2 simulations were extracted to compute performance parameters as shown in table I.

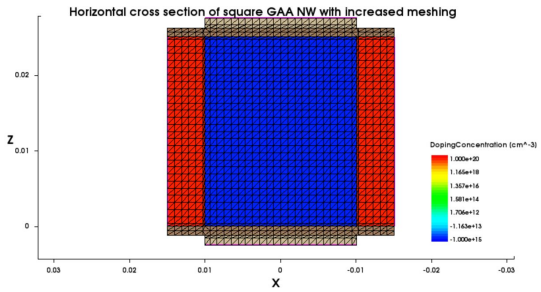
TABLE I: Performance Parameters of GAA NW With Different Mesh Sizes

Parameter	Normal Mesh	Increased Mesh
Maximum Transconductance (S)	8.33x10 $^{-5}$	6.87x10 $^{-5}$
Linear Threshold Voltage (V)	0.501	0.485
Saturation Threshold Voltage (V)	0.315	0.293
DIBL (mV/V)	125	130
Sub-Threshold Swing (mV/dec)	271	286
Output Conductance (S)	2.20x10^{-4}	2.20x10^{-4}
On-Off Current Ratio	4.97x10^{2}	4.65x10^{2}

Comparing the values in table I, it can be seen that there is not much disparity between the values. The opportunity cost of a



(a) Normal Mesh Size (2nm, 1nm)



(b) Increased Mesh Size (1nm, 0.5nm)

Fig. 2: Variation in mesh

much larger run time outweighed any potential improvements in accuracy. Therefore, for all future simulations, the normal mesh size (2nm, 1nm) was used.

An additional difference which was implemented in subsequent fabrications was the absence of the gate material. Having the gate in the model prolongs the running of Sentaurus, and in interest of time, the gate was removed.

On that same note, the gate was accounted for in SDevice command file, allowing the results to be calculated as though a gate were present, hence the results calculated in Sentaurus were still accurate.

With reference to the column of values for normal mesh in table 1, it can be seen that this GAA NW had inferior performance. The DIBL and sub-threshold swing obtained were unacceptably high whereas the on-off current ratio was a mere 497, a far cry from the expected on-off current ratios in the 10^6 range. Therefore, the subsequent sections will explore compensation methods to improve the GAA NW.

III. Theoretical Analysis of Compensation Methods to Improve GAA NW

With aid from research and literature, it has been understood that an issue greatly faced in the square GAA NW is the introduction of corner effects.[2]

When a sharp corner exist in a device such as FinFET or square GAA NW, the proximity of two adjacent gates leads to charge sharing at the corners, leading to premature inversion. Independent channels are formed beneath the corner with different threshold voltages, resulting in higher off-leakage currents which are not well-controlled by the gate. These phenomena are known as corner effects.[3]

The sharp edges in the square GAA NW has caused various I-V characteristic changes, which subsequently leads to a decrease in performance of NW.[4]

Another perspective to view corner effects is that corner effect implies the presence of a parasitic capacitance which is affecting the NW's performance.[5]

Methods to attenuate the corner effects were taken, such as rounding of corners, under-lapping of gate in SDE and wider drain.

A. Lateral Gate Underlap

To combat corner effects, a technique known as "Square gate all around MOSFET with gate underlap" is proposed by Sharma and Chaudhury[5].

This technique models the oxide as a parallel capacitor, with the silicon channel on one side and gate material on the other. Fig.3b) shows the model.

If the gate width is reduced on each side of the GAA NW by W', the length of the upper plate of the parallel plate capacitor is effectively being reduced by the same amount.

Using Gauss Law, the capacitance per unit area of the unequal parallel plate section can be found as:

$$C = \frac{\epsilon_{ox} \cos\theta_i}{t_{ox}}$$

where

$$\theta_i = \tan^{-1}\left(\frac{w'}{t_{ox}}\right)$$

t_{ox} being the thickness of the oxide layer (1.2nm in this report).

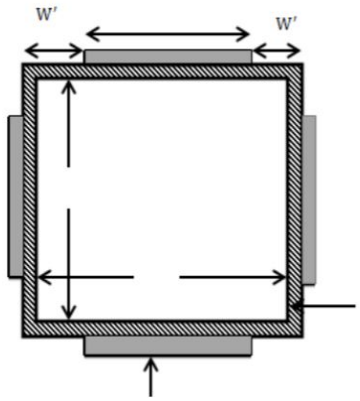
The capacitance in the unequal parallel plate region is reduced by a factor of $cos\theta_i$. At the edge of the top plate, which is the gate layer, electric fields will be fringing and the electric field magnitude in the corners will be reduced.

The depletion charge at the corners is therefore less than that generated directly beneath the gate material. Charge sharing contributions between two sides of the square GAA NW is reduced and there will be less electrostatic coupling.

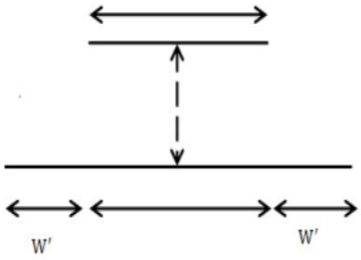
This leads to an increase in threshold voltage and this minimises the effects of premature inversion at the corners, reducing off leakage currents and therefore greatly improving on-off current ratios.

With the theoretical justifications, a simulation of the underlap gate technique was carried out and the results are presented

in the following section.



(a) schematic of GAA NW with underlap gate



(b) Parallel gate capacitor with unequal plate dimensions

Fig. 3: GAA NW with underlap gate from [5]

B. Rounding of Corners

As mentioned in the earlier part of the section, the reason for a mediocre performance of a square shaped GAA NW is due to its geometry.

The removal of the sharp edges could potentially reduce the magnitude of corner effects, improving the NW performance. Rounding of square GAA NW would be simulated and tested in Sentaurus, to compare the NW performance.

C. Widening of Drain

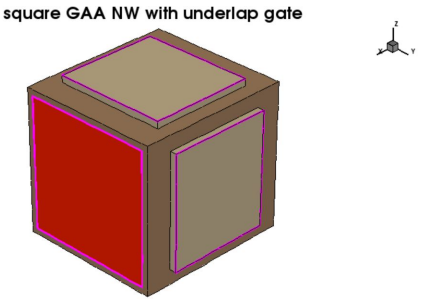
Widening of drain reduces the magnitude of gate induced drain leakage (GIDL). Presence of leakage current is due to presence of a large longitudinal electric field. [6]

Widening of drain supresses the electric field, resulting in a lower GIDL, which consequently results in a better performing GAA NW.

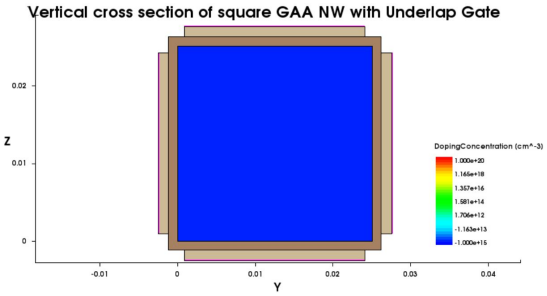
IV. Experimental Results

The methods mentioned in section IV were implemented in Sentaurus, and the performance parameters were once again extracted to assess its performance.

A. Lateral Gate Underlap



(a) GAA NW with underlap gate



(b) Cross section of GAA NW with underlap gate

Fig. 4: GAA NW with underlap gate

Table III shows the performance parameter of the base case and under-lapped GAA NW.

TABLE II: Performance Parameters of GAA NW with Under-Lapped Gates

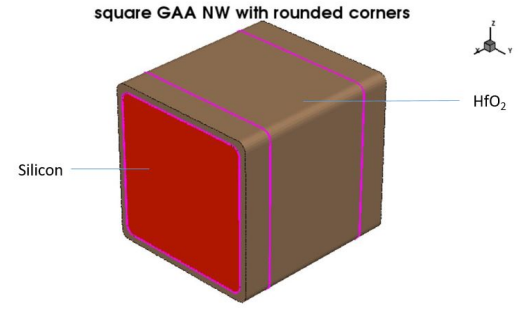
Parameter	Base Case	Under-lapped
Maximum Transconductance (S)	$8.33\text{x}10^{-5}$	$8.01\text{x}10^{-5}$
Linear Threshold Voltage (V)	0.501	0.498
Saturation Threshold Voltage (V)	0.315	0.308
DIBL (mV/V)	125	128
Sub-Threshold Swing (mV/dec)	271	272
Output Conductance (S)	$2.20\text{x}10^{-4}$	$1.95\text{x}10^{-4}$
On-Off Current Ratio	$4.97\text{x}10^{2}$	$1.18\text{x}10^{5}$

A comparison in table III shows a much better performance in the on-off current ratio, having a remarkable increase of 1000 fold.

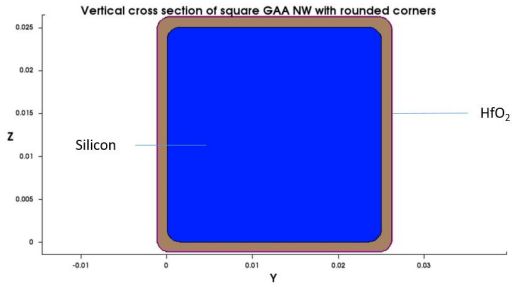
Despite the improvement in on-off current ratio, the other parameters were computed to be about the same values as the base case. This shows that under-lapping of gates has reduced the leakage current, which leads to a higher current ratio, but did not help much in other parameters such as DIBL.

B. Rounding of Corners

In SDE, the corners were rounded via the fillet function in Sentaurus. Adding a fillet essentially replaces the corners of our square cross-section with a quadrant of defined radius. The fillet radius was increased to 1nm for this simulation. Fig.3 shows the fabricated model of the GAA NW. The performance parameters were obtained and compared to that in Fig.2a).



(a) Rounded GAA NW



(b) Cross section of Rounded GAA NW
Fig. 5: Rounded with fillet radius of 1nm

Comparison of the values in table IV shows a slight improvement in the NW performance, having a 10 fold increase of on-off current ratio.

Overall, the other performance parameters did not show much improvement in performance, having a relatively large DIBL of 125mV/V, which is still undesirable for a GAA NW.

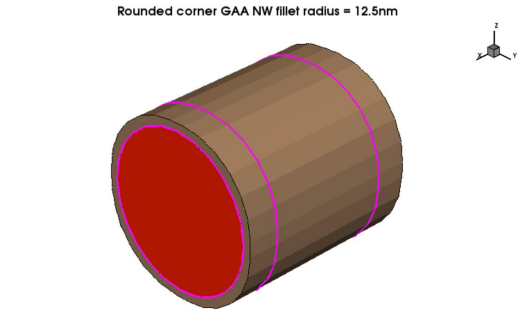
TABLE III: Performance Parameters of GAA NW with Rounded Corners

Parameter	Base Case	Rounded
Maximum Transconductance (S)	$8.33x10^{-5}$	$6.71x10^{-5}$
Linear Threshold Voltage (V)	0.501	0.321
Saturation Threshold Voltage (V)	0.315	0.130
DIBL (mV/V)	125	128
Sub-Threshold Swing (mV/dec)	271	274
Output Conductance (S)	$2.20x10^{-4}$	$2.38x10^{-4}$
On-Off Current Ratio	$4.97x10^{2}$	$4.55x10^{3}$

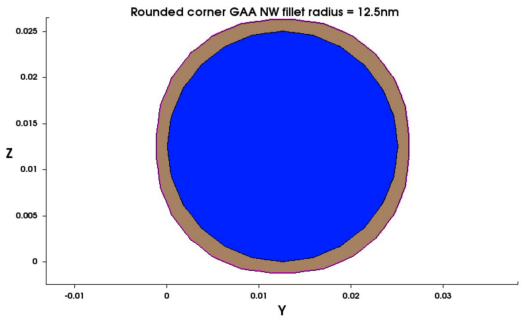
Despite theoretical justification that rounding of corners would improve our square GAA NW, the results showed otherwise. It would be premature to conclude that rounding of corners is ineffective. A plausible explanation is that the rounding of corners was not drastic enough to negate corner effects.

Therefore, to improve GAA NW performance, a larger degree of rounding will be needed and the logical conclusion would be the square cross-section ”evolving” to a circular cross-section.

The fillet radius, which controls the amount of rounding, was pushed to a much greater value in Sentaurus. The fillet radius was increased from 1nm to a value of 12.5nm, resulting in a rounded GAA NW as shown in Fig.6 .



(a) Rounded GAA NW



(b) Cross section of Rounded GAA NW
Fig. 6: Rounded with fillet radius of 12.5 nm

Table V shows the performance parameters of the more rounded GAA NW.

TABLE IV: Performance Parameters of GAA NW with more Rounded Corners

Parameter	Base Case	Rounded
Maximum Transconductance (S)	$8.33x10^{-5}$	$5.26x10^{-5}$
Linear Threshold Voltage (V)	0.501	0.323
Saturation Threshold Voltage (V)	0.315	0.137
DIBL (mV/V)	125	125
Sub-Threshold Swing (mV/dec)	271	179
Output Conductance (S)	$2.20x10^{-4}$	$2.03x10^{-4}$
On-Off Current Ratio	$4.97x10^{2}$	$3.97x10^{3}$

With reference to Fig.6 it can be seen that at a high fillet radius, the square GA NW is essentially a circle GAA NW.

Looking at table V, it can still be seen that there were improvements in the subthreshold swing, but the DIBL is still not up to expectations, still having a value larger than 100mV/V despite the changes made.

This leads to a conclusion that the rounding of the NW had boosted the NW’s performance, however more remains to be done to bring the DIBL to an acceptable range.

C. Widening of Drain

The last method which was implemented to reduce corner effects is the widening of drain. The dimensions of the drain was increased in SDE, creating a wider drain to attenuate the corner effects.

Fig.7 shows the cross section of the GAA NW with extended drain, and it can be seen that the drain is increased to 7.5nm instead of the earlier 5nm as seen in previous models.

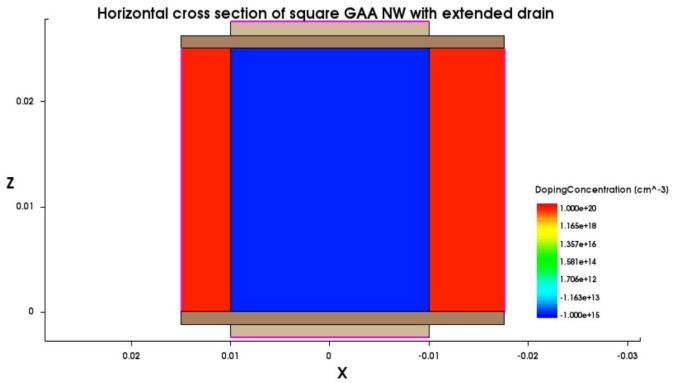


Fig. 7: 3D Model of Square GAA NW with widened drain

Table VI shows the performance parameter of a GAA NW with widened drain.

TABLE V: Performance Parameters of GAA NW with more widened drain

Parameter	Base Case	Widened Drain
Maximum Transconductance (S)	$8.33\text{x}10^{-5}$	$7.47\text{x}10^{-5}$
Linear Threshold Voltage (V)	0.501	0.500
Saturation Threshold Voltage (V)	0.315	0.315
DIBL (mV/V)	125	124
Sub-Threshold Swing (mV/dec)	271	266
Output Conductance (S)	$2.20\text{x}10^{-4}$	$2.17\text{x}10^{-4}$
On-Off Current Ratio	$4.97\text{x}10^{2}$	$5.82\text{x}10^{3}$

Unfortunately, the improvement in performance is not as significant as expected. The effect might be more significant on FinFETs due to the presence of a substrate, which is absent in a nanowire.

V. Next approach

Analyzing the performance parameters, it can be concluded that performance of a square GAA NW is not on par with the performance of a cylindrical GAA NW.

This has been supported by values in tables IV and V, where it has shown that a rounded square GAA NW has a better performance than a regular square GAA NW.

Papers and literature has also affirmed that a rounded square GAA NW, which is essentially a cylindrical GAA NW, has better performance.[7]

Despite the better performance, the cylindrical shaped NW requires further optimisation as the DIBL is still at a value larger than 100mV/dec.

With more research done, a possible explanation as to a high DIBL despite the change in shape of GAA NW could be due to the presence of a large surface area in the NW.

This leads to a new approach taken, where reduction of surface area of GAA NW is implemented in Sentaurus, and performance is once again analyzed.

VI. Reducing Surface Area of cylindrical GAA NW

With the knowledge that a cylindrical GAA NW has a better performance, further assessments of how surface area affects the NW's performance would be performed on cylindrical GAA.

A similar approach was taken in SDE to fabricate a cylindrical shaped NW with a simple change of settings in the drawing tool.

The first model which was fabricated is a circle with radius of 10nm. Comparing with the initial square created in Fig.1, which has an area of 625nm^2, the area of the circle has now shrunk to 314nm^2.

The performance parameters of cylindrical GAA NW with radius of 10nm shown in table VII.

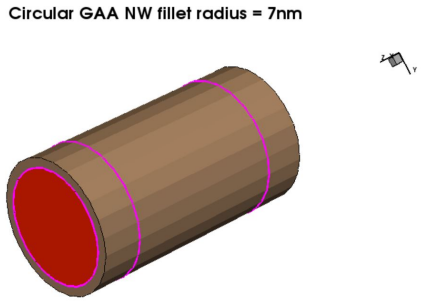
TABLE VI: Performance Parameters of Cylindrical GAA NW with radius of 10nm

Parameter	Base Case	Cylindrical with radius 10nm
Maximum Transconductance (S)	$8.33\text{x}10^{-5}$	$4.28\text{x}10^{-5}$
Linear Threshold Voltage (V)	0.501	0.335
Saturation Threshold Voltage (V)	0.315	0.212
DIBL (mV/V)	125	82.3
Sub-Threshold Swing (mV/dec)	271	79
Output Conductance (S)	$2.20\text{x}10^{-4}$	$1.45\text{x}10^{-4}$
On-Off Current Ratio	$4.97\text{x}10^{2}$	$2.71\text{x}10^{4}$

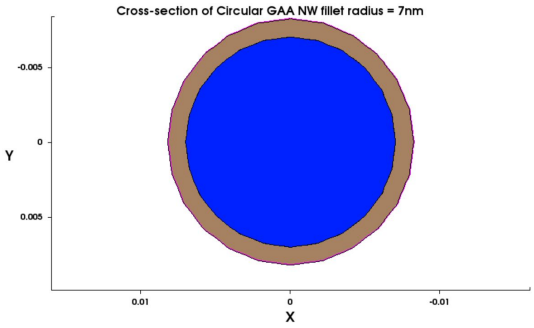
Comparison across values in table VII has shown that there is a great improvement in all aspects of its performance. DIBL and sub-threshold swing both at a value smaller than 100. The on-off current ratio has also shown a 100 times improvement from the base case.

To further investigate the hypothesis that surface area of the NW has an inversely proportional relationship to its performance parameter, the area of the cylindrical GAA NW has been reduced further to an area of 154nm^2.

Fig.8 shows the cross-section as well as the whole cylindrical GAA NW.



(a) Rounded GAA NW



(b) Cross section of Rounded GAA NW

Fig. 8: Cylindrical GAA NW with radius of 7nm

Performance parameters are once again computed and shown in table VII.

TABLE VII: Performance Parameters of Cylindrical GAA NW with varying radius

Parameter	**Radius 7nm**	**Radius 10nm**
Maximum Transconductance (S)	2.66x10 $^{-5}$	4.28x10 $^{-5}$
Linear Threshold Voltage (V)	0.341	0.335
Saturation Threshold Voltage (V)	0.273	0.212
DIBL (mV/V)	45.2	82.3
Sub-Threshold Swing (mV/dec)	65.1	79.0
Output Conductance (S)	8.07x10^{-5}	1.45x10^{-4}
On-Off Current Ratio	3.97x10^{6}	2.71x10^{4}

The values in table VIII has affirmed the hypothesis as it can be seen that a cylindrical GAA NW with a smaller radius has shown much greater performance overall.

VII. Conclusion

Through research and simulations, it can be seen that a square GAA NW has a worse performance when compared to that of a cylindrical GAA NW.

A plausible factor is due to the larger magnitude of corner effects being present in the square GAA NW than in a cylindrical GAA NW.

Secondly, it can also be concluded that when the area is reduced, the performance has drastically improved. This shows that a NW with smaller surface area with smoother edges would be a better performing NW. However, smaller nanowires may be more expensive to manufacture. Thus, this represents an engineering tradeoff that the industry has to consider.

Table IX shows the final comparison made, between the initial square GAA NW with an area of 625nm^2 and the cylindrical GAA NW with an area of 154nm^2 .

TABLE VIII: Performance Parameters of GAA NW With Different Geometry and Area

Parameter	**Square(625nm$_2$)**	**Cylindrical(154nm$_2$)**
Maximum Transconductance (S)	8.33x10 $^{-5}$	2.66 $^{-5}$
Linear Threshold Voltage (V)	0.501	0.341
Saturation Threshold Voltage (V)	0.315	0.273
DIBL (mV/V)	125	45.2
Sub-Threshold Swing (mV/dec)	271	65.1
Output Conductance (S)	2.20x10^{-4}	8.07x10^{-5}
On-Off Current Ratio	4.97x10^{2}	3.97x10^{6}

The performance parameters have shown vast improvements:

- Maximum Transconductance (g_m) has decreased by 3.13 times
- Linear Threshold Voltage (V_{th}^{lin}) has decreased by 0.16v
- Saturation Threshold Voltage (V_{th}^{sat}) has decreased by 0.042v
- Drain Induced Barrier Lowering (DIBL) has decreased by 2.77 times
- Sub-Threshold Swing (S) has decreased by 4.16 times
- Output Conductance (g_d) has decreased by 2.73 times
- On-Off Current Ratio has increased by 7990 times

With the aid of the list as well as the table, a final conclusion pertaining to the performance of a NW can be made. The conclusion is that a rounded GAA NW with a smaller surface area would give the highest level of performance, and GAA NW with other geometries woudl be more proned to corner effects when scaling is performed.

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