Mitigation of Short Channel Effects in MOSFETS and Investigation of Short Gate Width Effects

Yaohua Zhang, Zhi Kai Pong, Yi Song Ng

I. Abstract

A reduction of gate length of a MOSFET to 150 nm has inevitably introduced various adverse effects on MOSFET performance. These effects are termed as short channel effects (SCE). In the first part of this report, various measures to rectify these effects were implemented in TCAD Sentaurus and analysed. The performance parameters were computed and compared against pre-optimised values to ensure that the short channel MOSFET's performance has improved. In the second part, a 3D model of a MOSFET was created and alterations of its gate width simulated. These changes will degrade its performance, and the effects of these changes will be investigated in greater detail.

II. Introduction on Parameters

Downscaling MOSFET is beneficial for transistor performance in terms of operation speed and power consumption, but also leads to many unintended effects, generally termed short channel effects(SCE). [1]

SCE affects many performance parameters, including the threshold voltage due to charge sharing and drain induced barrier lowering (DIBL) which could eventually lead to MOSFET breakdown. Therefore, the aim of this assignment is to optimise the performance of the MOSFET by reducing the impact of SCEs.

Before discussing in greater details on how the various parameters were used to assess the performance of the MOSFET, this section serves as an introduction to each parameter and explains why they are important in quantifying SCEs.

A. Maximum Transconductance (g_m)

The transconductance is given by the expression $g_m = \frac{dI_{DS}}{dV_{DS}}$. It indicates how well the gate controls the drain current. Ideally this value should be constant in the linear region, but in reality the high field effects and weak inversion currents at high and low V_{GS} respectively cause changes in g_m . [2]

In the middle of linear region, g_m will attain a maximum value when it is not affected by either of the aforementioned effects, and g_m^{max} is used to calculate the Linear Threshold Voltage. g_m^{max} is also of interest to analogue electronic engineers as it is a key parameter in calculating small-signal voltage gain and other quantities.

B. Linear Threshold Voltage (V_{th}^{lin})

The threshold voltage is the value of V_{GS} where the MOSFET is considered turned on. In this report, the linear region is defined at $V_{DS} = 0.01V$. It was calculated by extrapolating the slope of the $I_D - V_G$ transfer characteristics at the value where g_m^{max} was attained.

C. Saturation Threshold Voltage (V_{th}^{sat})

The saturation region is defined at $V_{DS} = 1.5V$. In short channel MOSFETs, the threshold voltage of the saturation region will have a significant shift compared to that of the linear region, and this is measured by DIBL, which will be explained in section II.D.

The saturation threshold voltage was calculated by first taking the square root of I_{DS} and extrapolating the slope of this curve to find its horizontal intercept. This is because in the saturation region, the current is proportional to the square of $V_{GS} - V_{th}$.

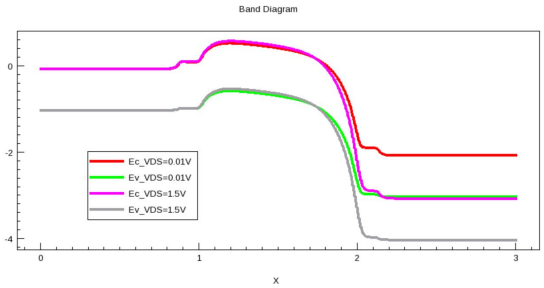
D. Drain Induced Barrier Lowering (DIBL)

DIBL is given by the formula of: $DIBL = \frac{|V_{th}^{lin} - V_{th}^{sat}|}{V_{DS}^{sat} - V_{DS}^{lin}}$. The equation shows that DIBL is proportional to the shift in threshold voltage in linear and saturation regions. [2, p. 271-272]

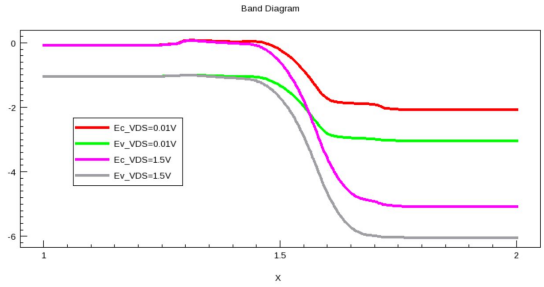
In short channel MOSFETs, V_{DS} causes the drain depletion layer to expand into the channel, leading to charge sharing and the lowering of potential barrier. One of main goals of mitigating SCEs is to reduce the DIBL.

In Fig. 1[1], it can be observed that the applied drain voltage in the long gate length MOSFET did not have a significant effect on the potential barrier. However, in the short gate length MOSFET, the drain depletion layer leads to a significant DIBL when a high V_{DS} was applied.

[1]Plots of Energy Band Diagrams have units of μm on X axis and eV on Y axis



(a) Energy band diagram of MOSFET with gate length = 1μm at V_{DS} = 0.01V and 1.5V



(b) Energy band diagram of MOSFET with gate length = 150nm at V_{DS} = 0.01V and 1.5V

Fig. 1: Comparison of DIBL in long and short gate length MOSFETs

E. Sub-Threshold Swing (S)

Sub-threshold swing is a measurement of the switching-off characteristic. A smaller sub-threshold swing indicates a better performance, but it should be noted that under room temperature sub-threshold swing has a minimum theoretical limit of approximately 60mV/dec. [3]

It was calculated as the reciprocal of the maximum value of $\frac{dLogI_{DS}}{dV_{GS}}$ in the saturation region. [2, p. 207-208]

F. Output Conductance (g_d)

Output conductance is defined as the derivative $\frac{dI_{DS}}{dV_{DS}}$ in saturation. [2, p. 403-404] Ideally, this value should be constant. However, in reality this is not the case. In the saturation region, channel pinch-off occurs and the effective channel length decreases as a function of the applied drain voltage, leading to a non-zero output conductance. This is also known as channel length modulation. [4]

G. On-Off Current Ratio

SCEs introduce more leakage currents in the MOSFET, leading to non-zero currents even when the device is switched off. The on-off current ratio in saturation region is therefore an important benchmark of how well the off current is controlled. In this report, the on voltages are defined as $V_{on} = V_{DD} = V_{DS}$ for enhancement mode MOSFETs, and $V_{on} = V_{DD} + 2V_{th}$ for depletion mode MOSFETs, whereas the off voltages are 0V and $2V_{th}$ for enhancement and depletion mode MOSFETs respectively.

III. Performance of Short Channel MOSFET

In an earlier simulation where a long channel MOSFET of gate length 1 μm was reduced to 150 nm, many undesirable characteristics of its performance were observed. Fig 2 [2] shows a diagram of the initial short channel MOSFET after only reducing the gate length.

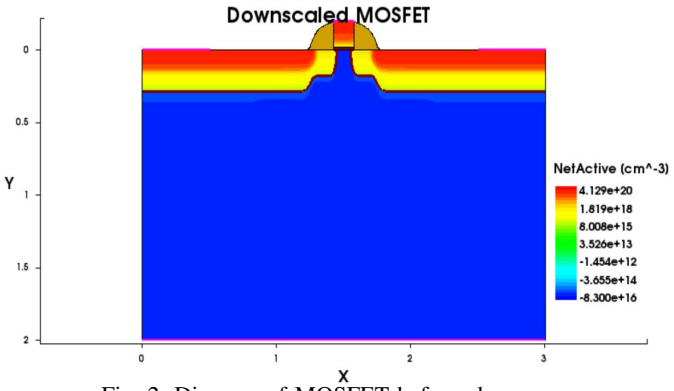


Fig. 2: Diagram of MOSFET before changes

Table I gives the values of the MOSFET performance parameters after the length of gate has been reduced.

TABLE I: Performance Parameters of Short Channel MOSFET

Maximum Transconductance (S)	5.06×10^{-6}
Linear Threshold Voltage (V)	0.118
Saturation Threshold Voltage (V)	-1.09
DIBL (mV/V)	814
Sub-Threshold Swing (mV/dec)	508
Output Conductance (S)	4.25×10^{-5}
On-Off Current Ratio	5.06×10^{7}

It can be seen that the performance parameters are not desirable and the reason is due to SCEs which are caused by shrinking of gate length.

SCEs are the result of a shift in the threshold voltage, which in turn would cause performance parameters to vary. This is due to calculations of performance parameters requiring the threshold voltages in both linear and saturation.

In subsequent sections, measures to alleviate SCEs were investigated. The performance parameters calculated earlier will be computed again for each method implemented, to prove that these methods has attenuated the SCEs.

A. Reducing dimensions of MOSFET

For the MOSFET which optimisation would be tested on, alterations were made from Fig 2. Fig 3 shows those modifications being made, where the MOSFET has been reduced in size in both width and depth of MOSFET. This modification has been made to allow processes in Sentaurus to run at a faster pace.

[2] Plots of MOSFETS have units of μm on X and Y axes

The MOSFET has been reduced from a width of 3 μm to 1 μm and the depth has been reduced from 2 μm to 0.5 μm.

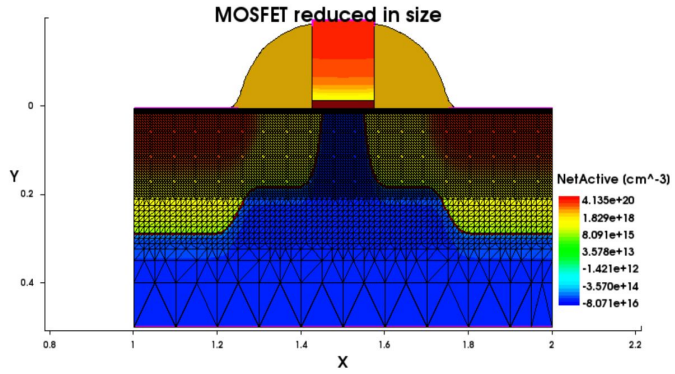


Fig. 3: Diagram of MOSFET with meshing after reducing dimensions

Table II illustrates the performance of the dimension-reduced MOSFET.

TABLE II: Performance Parameters of Short Channel MOSFET after alterations to dimension

Maximum Transconductance (S)	5.16x10 $^{-6}$
Linear Threshold Voltage (V)	0.120
Saturation Threshold Voltage (V)	-1.09
DIBL (mV/V)	814
Sub-Threshold Swing (mV/dec)	508
Output Conductance (S)	4.22x10^{-5}
On-Off Current Ratio	5.61x10^{7}

Comparing table II to table I, it can be observed that the values in table II has not varied much from that of table I. This shows that alteration of dimensions of this MOSFET did not affect its performance. These values in table II would be the basis of comparison for subsequent parameters obtained after the measures had been implemented.

IV. Testing of Individual Methods to Reduce SCE's

In literature, various ways to attenuate SCEs had been introduced, and these methods were implemented to improve the performance of the short channel MOSFET.

The methods tested were as follows:

- Thinning Of Oxide Layer
- Reducing Junction Depth
- Increase in Substrate Doping

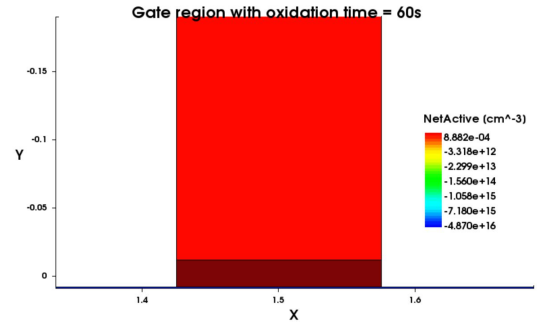
The explanation as to how each method works in reducing SCEs will be explained in the subsections. The performance parameters were computed for each method used to determine which gave the best improvement in performance.

A. Thinning of Oxide Layer

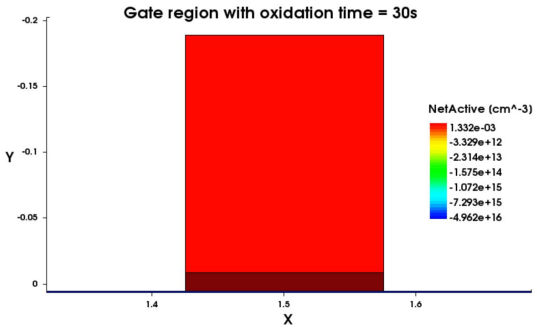
With a reduction in gate length, there will be an increase in control of drain over gate. This shortcoming can be rectified by increasing the oxide capacitance, since the oxide capacitance is calculated as $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ [2, p. 70].

Therefore, reducing the oxide thickness will greatly increase oxide capacitance. An increase in oxide capacitance will result in a better control of the MOSFET. [5] This will eventually lead to SCEs being reduced.

In Sentaurus, an approach taken for thinning of oxide layer was to reduce oxidation time in the code. An initial oxidation time of 60s was used and it had been reduced to 30s to thin the oxide with the resultant MOSFET assessed on its performance.



(a) Oxide thickness with oxidation time of 60s



(b) Oxide thickness with oxidation time of 30s

Fig. 4: Reduction in Oxide Thickness

Performance parameters of MOSFET after a reduction in oxide layer thickness are seen in table III.

TABLE III: Performance Parameters of Short Channel MOSFET after reducing thickness of oxide

Maximum Transconductance (S)	6.58x10 $^{-6}$
Linear Threshold Voltage (V)	0.0741
Saturation Threshold Voltage (V)	-0.825
DIBL(mV/V)	603
Sub-Threshold Swing (mV/dec)	425
Output Conductance (S)	3.91x10^{-5}
On-Off Current Ratio	7.29x10^{7}

Comparing the values in table III and table II, it can be seen that a notable change is the drop of DIBL. After thinning the oxide layer, DIBL had decreased from 814mV/V to 603mV/V, showing remarkable improvement. The other parameters had also improved, proving that thinning the oxide layer had alleviated some SCEs.

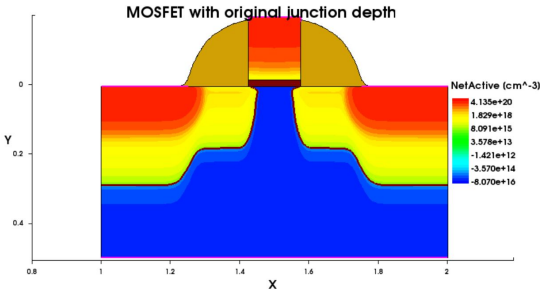
Despite the large improvement of DIBL, there was still much to work on as a value of 603mV/V was considerably large. This suggested a combination of methods to get a better performing MOSFET.

B. Reducing Junction Depth

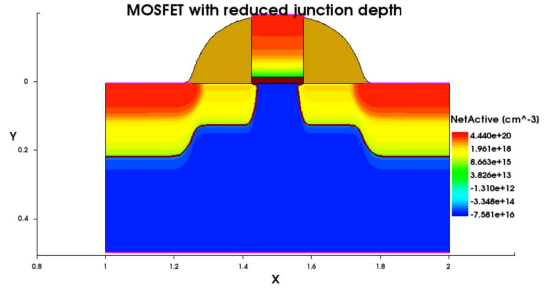
An alternative approach is reduction of junction depth. This reduces short channel effects by decreasing the amount of charge sharing. As charge will be shared across Ohmic regions and the gate depletion region over the depth of doping, reducing junction depth reduces the amount of charge sharing. [6]

Charge sharing is more prominent in short channel MOSFETS as the source and drain are closer to each other. Thus, depletion widths are closer to each other, causing effects of charge sharing to influence the threshold voltage more in short channel MOSFET.

To simulate a reduced junction depth in Sentaurus, the lowly doped drain(LDD) implantation energy as well as highly doped drain (HDD) implantation energy were reduced from 15keV to 9keV and 70keV to 60keV respectively. Fig 5 a) and b) show the difference between the junction depth after it had been reduced.



(a) Original Junction Depth



(b) Reduced Junction Depth

Fig. 5: Reduction in Junction Depth

However, when a simulation of only reducing the depth was run, the MOSFET did not fare much better than before. A plausible reason could be an increased contact resistance which reduced the output current flow.

This reduced current flow would therefore lead to undesirable parameter values. Table IV shows the performance parameters of the MOSFET after only reducing junction depth.

TABLE IV: Performance Parameters of Short Channel MOSFET after reducing junction depth

Maximum Transconductance (S)	3.61×10^{-6}
Linear Threshold Voltage (V)	0.686
Saturation Threshold Voltage (V)	-0.538
DIBL (mV/V)	822
Sub-Threshold Swing (mV/dec)	314
Output Conductance (S)	3.56×10^{-5}
On-Off Current Ratio	1.99×10^{8}

A suggested solution would be to elevate the source and drain since elevation has controlled the lateral diffusion of the highly doped regions. [7] The source and drain were elevated by depositing silicon after spacer formation. In Sentaurus SProcess, this was achieved by using the command `deposit Silicon type=fill coord=-0.1`.

Fig 6 shows the MOSFET with reduced junction depth and elevated source and drain.

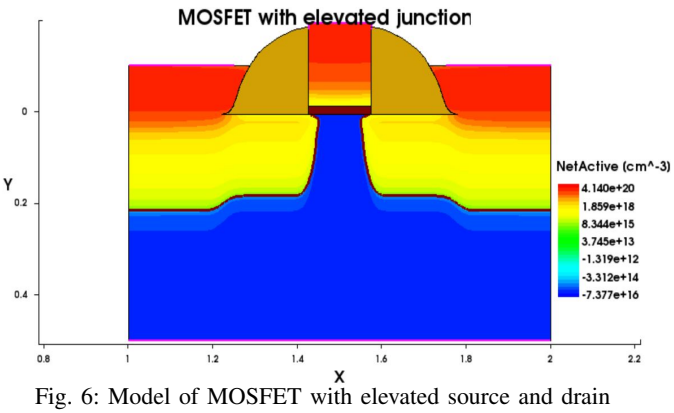


Fig. 6: Model of MOSFET with elevated source and drain

Table V shows the performance parameters after the source and drain had been elevated, showing much better performance compared to in table IV.

TABLE V: Performance Parameters of Short Channel MOSFET after reducing junction depth with elevation of source and drain

Maximum Transconductance (S)	3.06×10^{-6}
Linear Threshold Voltage (V)	0.351
Saturation Threshold Voltage (V)	-0.513
DIBL (mV/V)	580
Sub-Threshold Swing (mV/dec)	301
Output Conductance (S)	3.11×10^{-5}
On-Off Current Ratio	2.36×10^{8}

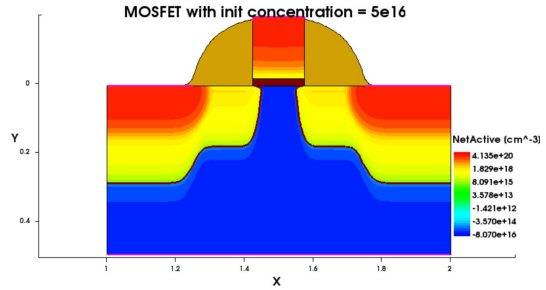
Looking at the values in table V, it can be seen that there was a marked improvement in the on-off current ratio, being 10 times larger than that in table II. The other parameters have also shown improvement but they were not as notable as that of the on-off current ratio.

However, a similar conclusion as in III.A can be made, which is despite the improvement, the MOSFET is still not fully optimised, and additional measures are required.

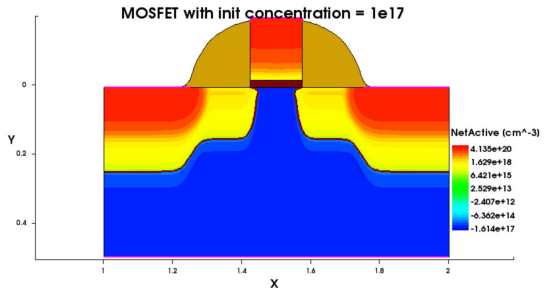
C. Increasing Substrate Doping

Increase in doping density reduces the width of the depletion region because the total charge remains the same under the same applied voltage. This reduces the influence of the drain on the channel, which is a primary cause of SCEs [8].

To assess this factor, doping of MOSFET increased from $5x10^{16}cm^{-3}$ to $1x10^{17}cm^{-3}$ in Sentaurus . Fig 7 a) and b) show models of MOSFET that had its doping concentration varied.



(a) Original Doping Concentration



(b) Increased Doping Concentration

Fig. 7: Increase in Doping

The performance parameters are shown in table VI , where it can be seen that performance of the MOSFET has improved.

TABLE VI: Performance Parameters of Short Channel MOSFET with increase in doping

Maximum Transconductance (S)	$4.37x10^{-6}$
Linear Threshold Voltage (V)	0.467
Saturation Threshold Voltage (V)	-0.190
DIBL (mV/V)	441
Sub-Threshold Swing (mV/dec)	218
Output Conductance (S)	$3.01x10^{-5}$
On-Off Current Ratio	$4.07x10^{7}$

Looking at the values across table VI, it was noticed that there was an increase in threshold voltage. There was also a notable decrease in the DIBL, reducing from 814mV/V to 441mV/V. The sub-threshold swing also greatly reduced to 218mv/dec.

Elevation of the source and drain was required when the doping had increased as the shortcomings mentioned in III.B were present as the substrate doping was increased.

TABLE VII: Performance Parameters of Short Channel MOSFET with increase in doping with elevated source and drain

Maximum Transconductance (S)	$4.03x10^{-6}$
Linear Threshold Voltage (V)	0.449
Saturation Threshold Voltage (V)	-0.186
DIBL (mV/V)	426
Sub-Threshold Swing (mV/dec)	211
Output Conductance (S)	$2.51x10^{-5}$
On-Off Current Ratio	$3.19x10^{7}$

With elevation, it can be seen that the performance parameters have improved when it was compared to that presented in table VI. There was an overall improvement in parameters such as the DIBL and sub-threshold swing despite a minute decrease in the on-off current ratio.

V. Summary of Each Method

The notable improvements in the performance parameters of each method are seen in the following list.

- Thinning Of Oxide Layer lead to the best improvement in DIBL
- Reducing Junction Depth increased on-off current ratio
- Increase in Substrate Doping also greatly reduced DIBL

VI. Investigating Effects when Methods are Combined

It can be concluded from Section IV that some SCEs had been significantly reduced when the methods were implemented separately. However, there is still room for improvement.

The subsequent step was to analyse the effects on SCEs if a combination of methods were used. The performance parameters of the MOSFET were computed to determine if the methods complemented or opposed each other.

Three combinations were simulated:

- Thinning of oxide and reducing junction depth
- Thinning of oxide and increasing substrate doping
- Thinning of oxide, increasing substrate doping, reducing junction depth

A particular combination (increasing substrate doping, reducing junction depth) was not simulated because thinning of oxide yielded the best results so it would be ineffective to run a simulation without thinning oxide.

A. Thinning of Oxide and Reducing Junction Depth

A similar Sentaurus code was run with slight changes to the input parameters such as the oxidation time being at 20s instead of 30s, and the LDD implantation energy and HDD implantation energy being at 13keV and 60keV respectively instead of 9keV and 40keV.

Table VIII shows the performance parameters of the MOSFET after these values were updated.

TABLE VIII: Performance Parameters of Short Channel MOSFET after reducing junction depth and thinning of oxide against the individual methods of reducing junction depth and thinning of oxide layer

Parameter	**C1** [3]	**R**[4]	**T**[5]
Maximum Transconductance (S)	5.79x10 $^{-6}$	3.06x10 $^{-6}$	6.58x10 $^{-6}$
Linear Threshold Voltage (V)	0.0997	0.351	0.0741
Saturation Threshold Voltage (V)	-0.433	-0.513	-0.843
DIBL (mV/V)	357	580	603
Sub-Threshold Swing (mV/dec)	273	301	425
Output Conductance (S)	2.93x10^{-5}	3.11x10^{-5}	3.91x10^{-5}
On-Off Current Ratio	1.11x10^{8}	2.36x10^{8}	7.29x10^{7}

With reference to table VIII, it can be seen that the MOSFET performance had greatly improved, with all values showing an improvement compared to when these methods were implemented separately.

It can also be seen that both DIBL and on-off current ratio had shown remarkable improvement from the values obtained in table II. This shows that the methods complement each other.

B. Thinning of Oxide and Increase in Substrate Doping

This method was executed in Sentaurus with the oxidation time reduced to 20s, and the doping increased from 5x10$^{16}cm^{-3}$ to 1x10$^{17}cm^{-3}$. Table VIII shows the performance parameters of the MOSFET obtained when these two methods were implemented jointly. Table IX shows the parameters of the short channel MOSFET with increased doping and thinning of oxide layer.

TABLE IX: Performance Parameters of Short Channel MOSFET after increase in doping and thinning of oxide against the individual methods

Parameter	**C2**[6]	**I**[7]	**T**[5]
Maximum Transconductance (S)	5.82x10 $^{-6}$	4.37x10 $^{-6}$	6.58x10 $^{-6}$
Linear Threshold Voltage (V)	0.264	0.467	0.0741
Saturation Threshold Voltage (V)	-0.113	-0.190	-0.843
DIBL (mV/V)	253	441	603
Sub-Threshold Swing (mV/dec)	153	218	425
Output Conductance (S)	2.09x10^{-5}	3.01x10^{-5}	3.91x10^{-5}
On-Off Current Ratio	2.84x10^{7}	4.07x10^{7}	7.29x10^{7}

This MOSFET has shown remarkable improvement across the board of all parameters, mainly in DIBL, reducing from an initial value of 814 mV/V to 253 mV/V.

It has a relatively low output conductance, being the only method that produced a value with an order of magnitude of 10^{-6}. This method produced a reduced sub-threshold swing which is a desirable property of a MOSFET.

[3]C1:Reducing of junction depth and thinning of oxide
[4]R:Reducing junction depth
[5]T:Thinning of oxide
[6]C2: Increase in doping and thinning of oxide

C. Thinning of Oxide, Reducing Junction Depth and Increase Substrate Doping

With the parameters computed in section IV.A and IV.B, it is safe to say that when two methods are combined together, the short channel effects has been mitigated to a large extent. A final level of assessment would be to combine all three methods and compare the performances of the MOSFETs.

Table X shows the comparisons in the table as the combination were varied.

TABLE X: Performance Parameters of Short Channel MOSFET after all methods implemented compared against when 2 methods are implemented

Parameter	**C1**[3]	**C2**[6]	**C3**[7]
Maximum Transconductance (S)	5.79x10^{-6}	5.82x10 $^{-6}$	4.77x10 $^{-6}$
Linear Threshold Voltage (V)	0.0997	0.264	0.358
Saturation Threshold Voltage (V)	-0.433	-0.113	-0.059
DIBL (mV/V)	357	253	280
Sub-Threshold Swing (mV/dec)	273	153	145
Output Conductance(S)	2.93x10^{-5}	2.09x10^{-5}	2.01x10^{-5}
On-Off Current Ratio	1.11x10^{8}	2.84x10^{7}	1.28x10^{7}

Looking at table X, it can be seen that the DIBL is not as low as in method IV.B, as well as a much lower on-off current ratio. This shows that the combination of all three methods yielded an inferior MOSFET than that in IV.B.

VII. Comparison Among Methods

C2(increasing in doping and thinning of oxide) is better than C1(reducing of junction depth and thinning of oxide). A combination of two methods had boosted MOSFET performance. However, when three methods were implemented jointly, it performed slightly worse than the MOSFET done in Section IV.B.

VIII. Final Design Choice

After taking into consideration the time constraint of this assignment, a more doped version of the MOSFET in Section IV.B was simulated. The doping was increased from 1x10$^{17}cm^{-3}$ to 4x10$^{17}cm^{-3}$. This new MOSFET turned out to be the most optimised.

A. Performance Parameters

Table XI shows the performance parameters of the most optimised MOSFET against the initial short channel MOSFET, and the table clearly shows the vast improvements the MOSFET had in terms of its performance.

[7]C3: Combination of all 3 methods

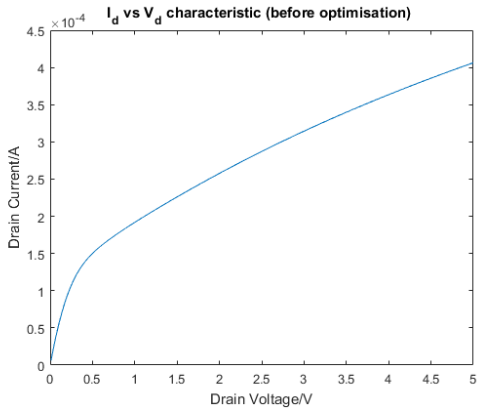
TABLE XI: Performance Parameters of most Optimised Short Channel MOSFET against initial short channel MOSFET

Parameter	**Optimised MOSFET**	**Initial**
Maximum Transconductance (S)	3.63x10 $^{-6}$	5.16x10 $^{-6}$
Linear Threshold Voltage (V)	1.25	0.120
Saturation Threshold Voltage (V)	1.00	-1.09
DIBL (mV/V)	162	814
Sub-Threshold Swing (mV/dec)	119	508
Output Conductance (S)	3.81x10^{-6}	4.22x10^{-5}
On-Off Current Ratio	8.16x10^{9}	5.61x10^{7}

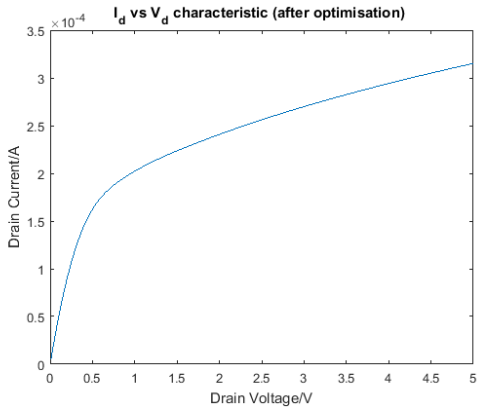
A list shows the factor by which each performance parameter has changed.

- Maximum Transconductance decreased by a factor of 1.42
- Linear Threshold Voltage increased by 1.13V
- Saturation Threshold Voltage increased by 2.09V
- DIBL decreased by a factor of 5.02
- Sub-Threshold Swing decreased by a factor of 4.27
- Output Conductance decreased by a factor of 11.1
- On-off current ratio increased by a factor of 14.5

Overall, it has shown the greatest improvements in all of its performance parameters. Achieving the lowest DIBL of 162 mV/V, as well as the highest on-off current ratio, made this MOSFET the most optimised MOSFET that has been obtained through simulations.



(a) I_D vs V_D before optimization



(b) I_D vs V_D after optimization

Fig. 8: I_D vs V_D graphs

B. I/V Characteristics

Studying I/V characteristics gave a qualitative analysis of the MOSFET performance. The graphs obtained would highlight a change in a certain performance parameter, as the performance parameters are obtained via calculations from I/V characteristics. Plotting I/V characteristics provide a clear and powerful way of analysing MOSFET performance.

1) Output characteristics

The I_D vs V_D characteristics are studied in this subsection. Plots of I_D vs V_D are seen in Fig 8 a) and b) .

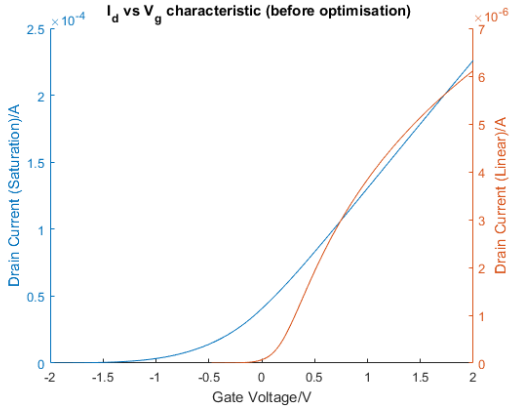
The linear and saturation regions are plotted on the same graph, making analysis of I/V characteristics more convenient. Linear region is from 0V-0.5V (the steepest part), saturation region occurs after 0.5V-5V.

From the I_D vs V_D plots, it can be seen that the slope is gentler in Fig 8 b) than in a) in the saturation region. The output conductance is calculated as $g_d = \frac{\partial I_D}{\partial V_D}$, thus one would expect a lower output conductance in the better MOSFET, and this is corroborated by values from table XI.

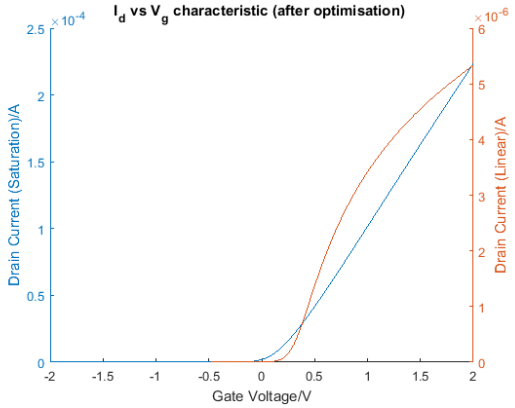
2) Transfer characteristics

Similarly, a study of I_D vs V_G is made, and Fig 9 shows the I_D vs V_G characteristics of the MOSFET before and after optimisation. The I_D vs V_G characteristics are more interesting to study, as most of the calculation of the parameters involved usage of I_D vs V_G characteristics.

The plots in red represents the I_D vs V_G behaviour in the linear region and the plots in blue represents the I_D vs V_G in the saturation region.

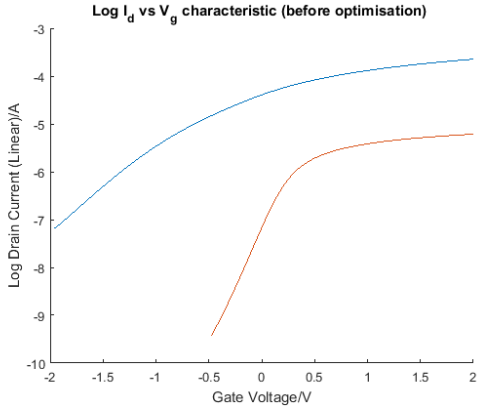


(a) I_D vs V_G before optimization

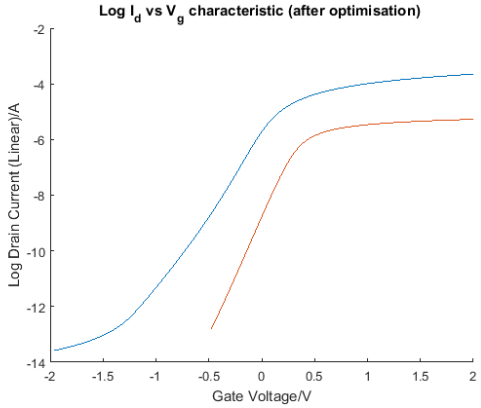


(b) I_D vs V_G after optimization

Fig. 9: I_D vs V_G graphs



(a) I_D vs V_G before optimization



(b) I_D vs V_G after optimization

Fig. 10: I_D vs V_G graphs

The gradient of the red slope in Fig 9 b) is steeper than that in Fig 9 a). This difference in gradient shows a difference in the transconductance.

3) $log(I_D)$ vs V_G

Lastly, a method of assessing performance from the I/V graphs would be to plot the $\log(I_{DS})$ vs V_{GS} graph.

A comparison made between the red and blue plot in each sub-figure would explain the variance in DIBL. The DIBL can be observed as the gap between the red and the blue plots in each sub-figure.

Comparing the two sub-figures, it can be seen that the optimised MOSFET has a smaller DIBL than that of the initial MOSFET.

C. Physics Model

In Sentaurus SDevice, users can define what physics model to use in their simulations. It is therefore crucial to ensure that the correct model is used or else the simulated device performance may not be realistic. An investigation was therefore carried out to verify whether some models were necessary, or they could be modified to reduce running time of simulations.

Two simulations with same device parameters were simulated, one with `HighFieldSaturation` and one without. The output characteristics of the MOSFET are presented in Fig. 11.

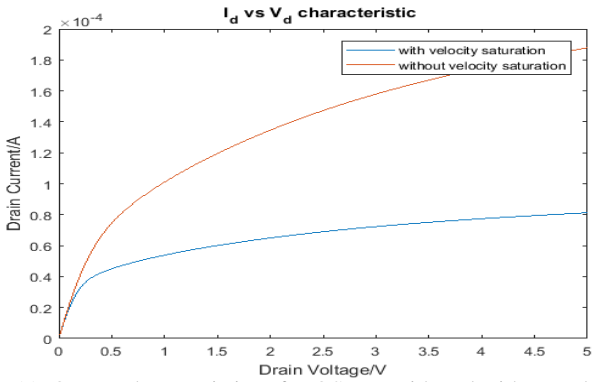


Fig. 11: Output characteristics of MOSFET with and without velocity saturation model

There is a significant difference in the output characteristics of the two simulations. This suggests that velocity saturation is a crucial effect with regard to SCEs, and it must be taken into consideration in order to obtain realistic results. Without velocity saturation, the drain current is limited by pinch-off instead, and onset of saturation will occur at a higher V_{GS}. The drain current will also reach a higher value in the saturation region.

Another set of simulations was carried out, one with and one without the `Hydrodynamic` model. It was observed that the output and transfer characteristics are virtually the same. This seemingly suggests that the Hydrodynamic model is not necessary for simulation purposes in this report.

The `Hydrodynamic` model takes into account of carrier temperatures, whereas the default model only considers Drift-Diffusion behaviour. In this report, temperature changes were not considered, therefore this could be the reason `Hydrodynamic` model is unnecessary. The `Drift-Diffusion` model could replace the `Hydrodynamic` model to reduce the running time because it is less computationally expensive.

IX. 3D Modelling

In this section, a 3D model was created in Sentaurus. In the earlier sections, there were discussions on SCEs. For this part, narrow channel width effects would be looked into. Physical properties of the MOSFET would change with a reduction in gate width, and the effects of narrowing the width would be studied in greater detail.

A. Short Channel Optimised MOSFET

The MOSFET that had been chosen for 3D Modelling was the MOSFET with increased substrate doping and thinned oxide layer.

Unfortunately, the most optimised MOSFET was not used, as the doping used in this MOSFET was from that of a previous result in section VI.B, when substrate doping was at $1\text{x}10^{17}cm^{-3}$ instead of $4\text{x}10^{17}cm^{-3}$. This is due to a lack of time as simulations for 3D modelling have a long running time, and there was insufficient time to run a 3D model analysis after the final optimised MOSFET was created.

Nevertheless, an analysis based off results obtained when the gate width was reduced would still be made in this section.

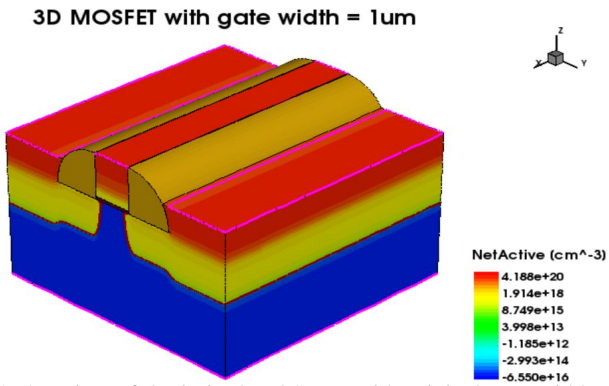


Fig. 12: 3D view of Optimised MOSFET with original gate width

Table XII shows the performance parameters of the 3D model MOSFET.

TABLE XII: Performance Parameters of 3D Model before reducing of gate width

Maximum Transconductance (S)	$5.82\text{x}10^{-6}$
Linear Threshold Voltage (V)	0.264
Saturation Threshold Voltage (V)	-0.113
DIBL (mV/V)	253
Sub-Threshold Swing (mV/dec)	153
Output Conductance (S)	$2.09\text{x}10^{-5}$
On-Off Current Ratio	$2.84\text{x}10^{7}$

B. Effects of reducing width of gate of MOSFET

In Sentaurus SProcess, this was achieved by adding z-coordinates to all appropriate commands, effectively turning the 2D planar MOSFET into a 3D MOSFET. However, this massively increased the running time for both SProcess and SDevice simulations. The 2D MOSFET had 40000 edges for the mesh, whereas the 3D MOSFET had more than 300000 edges.

Using the linear region transfer and output characteristics as a basis for comparison, each experiement of 2D MOSFETs took at most 1 hour to complete, whereas the 3D MOSFETs required more than 15 hours. These numbers show that the 3D MOSFET simulation is much more time consuming and computationally costly than 2D MOSFET. Therefore, using 2D simulations to investigate MOSFET characteristics is preferred when the 3rd dimension does not need to be taken into account.

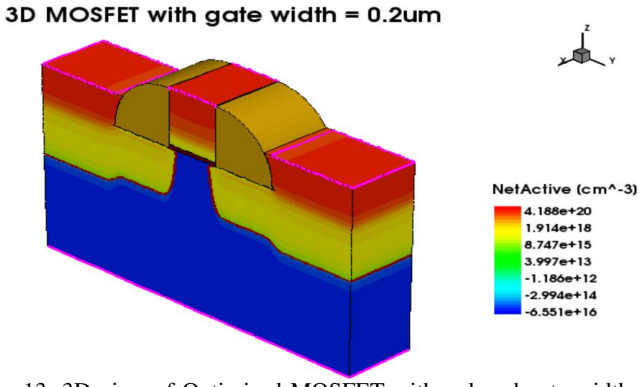


Fig. 13: 3D view of Optimised MOSFET with reduced gate width

Table XII shows the performance parameters of the 3D model MOSFET.

TABLE XIII: Performance Parameters of 3D Model before reducing of gate width

Maximum Transconductance (S)	$1.20x10^{-6}$
Linear Threshold Voltage (V)	0.0987
Saturation Threshold Voltage (V)	-0.548
DIBL (mV/V)	434
Sub-Threshold Swing (mV/dec)	316
Output Conductance (S)	$6.25x10^{-6}$
On-Off Current Ratio	$3.79x10^{8}$

C. Performance after change of gate width

With comparisons made between tables XII and XIII, it can be concluded that a narrowing of gate width has also introduced effects which affected MOSFET performance.

There was an overall drop in performance of MOSFET as shown in the following list.

- Maximum Transconductance decreased by a factor of 4.85
- Linear Threshold Voltage decreased by 0.165V
- Saturation Threshold Voltage decreased by 0.435V
- DIBL increased by a factor of 1.72
- Sub-Threshold Swing increased by a factor of 2.07
- Output Conductance decreased by a factor of 3.34
- On-off current ratio decreased by a factor of 13.3

It can be seen that narrow width effects also adversely affected MOSFET performance, with a significant reduction in threshold voltages. This is further corroborated by L. Akers' theoretical and experimental research into the narrow width effect. [9]

X. Conclusion

Having performed a collection of simulations on Sentaurus to test methods to alleviate SCEs , it is justified to claim that a short channel MOSFET's performance might not differ as much as a long channel MOSFET if the right methods were used to alleviate the SCEs.

With a combination of two methods of thinning of oxide layer and increasing substrate doping, the MOSFET has greatly improved from its initial phase and with more research and testing, it is plausible for the short channel MOSFET to have a better performance than a long channel MOSFET.

TCAD Sentarus is a very powerful software that could simulate device characteristics very well, but it also requires a lot of computational power and simulations take a long time to complete. Given more time, more investigations can be carried out to potentially further improve the short channel MOSFET.

Firstly, more combinations of the methods outlined in the report can be tested and pushed to the limit. In particular, thinning the oxide further could improve the performance further, but precision is also needed before it is pushed too far and introduces too much leakage current.

Secondly, other methods could also be tested, for example halo implants under the LDD and retrograde doping under the channel. [10] These methods are introduced in literature, and are potentially needed to further improve the MOSFET performance.

References

[1] A. Chaudhry and M. J. Kumar. *Controlling short-channel effects in deep-submicron SOI MOSFETs for improved reliability: a review.* in IEEE Transactions on Device and Materials Reliability, vol. 4, no. 1, pp. 99-109, March 2004.

[2] Y. Tsividis and C. McAndrew. *Operation and Modeling of the MOS Transistor.* 3rd ed. New York: Oxford University Press, 2011.

[3] Cheung, Kin. *On the 60 mV/dec @300 K limit for MOSFET subthreshold swing. International Symposium on VLSI Technology, Systems, and Applications, Proceedings* 10.1109/VTSA.2010.5488941.

[4] K.Y. Lim, X. Zhou. *An analytical effective channel-length modulation model for velocity overshoot in submicron MOSFETs based on energy-balance formulation* Microelectronics Reliability,Volume 42, Issue 12,2002,Pages 1857-1864,ISSN 0026-2714.

[5] A. Valletta, P. Gaucci, L. Mariucci, A. Pecora, M. Cuscunà, L. Maiolo, G. Fortunato, S. D. Brotherton *Role of gate oxide thickness in controlling short channel effects in polycrystalline silicon thin film transistors* Applied Physics Letters, vol. 95, pp. 303-308, Dec 2013.

[6] Lizhe Tan, Octavian Buiu, Stephen Hall, Enrico Gili, Takashi Uchino, Peter Ashburn *The influence of junction depth on short channel effects in vertical sidewall MOSFETs, Solid-State Electronics*Volume 52, Issue 7,2008,Pages 1002-1007,ISSN 0038-1101.

[7] S. Yamakawa *Drivability improvement on deep-submicron MOSFETs by elevation of source/drain regions* n IEEE Electron Device Letters, vol. 20, no. 7, pp. 366-368, July 1999. doi: 10.1109/55.772378

[8] K. Roy, S. Mukhopadhyay and H. Mahmoodi-Meimand *Leakage current mechanisms and leakage reduction techniques in deep-submicrometer CMOS circuits* in Proceedings of the IEEE, vol. 91, no. 2, pp. 305-327, Feb. 2003.

[9] L. A. Akers *The inverse-narrow-width effect* in IEEE Electron Device Letters, vol. 7, no. 7, pp. 419-421, July 1986

[10] Anu Tonk *Short Channel Effects in Conventional MOSFETs and their Suppression* International Journal of Engineering Research and General Science Volume 4, Issue 3, May-June, 2016 ISSN 2091-2730.