MC33774A

18-cell battery-cell controller IC

Rev. 1 — 15 June 2023

Product data sheet
CONFIDENTIAL

1 General description

The MC33774A is a lithium-ion battery-cell controller IC designed for automotive applications, such as hybrid electric vehicles (HEV) and electric vehicles (EV). It can be used in industrial applications, such as energy storage systems (ESS) and uninterruptible power supply (UPS) systems. The device measures differential high-precision cell voltages, as well as temperatures. Additionally, the device provides an extensive set of passive cell voltage balancing features to equalize the individual cell voltages across the battery stack. The device offers a serial peripheral interface (SPI) and an isolated daisy chain interface for communication with the host MCU. The MC33774A offers increased safety level and a low bill of materials cost.

2 Features and benefits

- AEC-Q100 grade 1 qualified: -40 °C to +125 °C ambient temperature range
- ISO 26262 ASIL D support for cell voltage and cell temperature measurements from the host microcontroller unit (MCU) to the cell
- Cell voltage measurement
  - 4 to 18 cells per device
  - Supports bus bars voltage measurement with -3 V to +5 V input voltage
  - 16-bit resolution and ±1 mV typical measurement accuracy with ultra low long-term drift
  - Integrated configurable digital filter
- External temperature and auxiliary voltage measurements
  - One analog input for absolute measurement, 5 V input range
  - Eight analog inputs configurable as absolute or ratiometric, 5 V input range
  - 16-bit resolution and ±5 mV typical measurement accuracy
  - Integrated configurable digital filter
- Internal measurement
  - Two redundant internal temperature sensors
  - Supply voltages
  - External transistor current
- Cell voltage balancing
  - 18 internal balancing field effect transistors (FET), up to 150 mA average with 0.5 Ω R_{DSon} per channel (typ.)
  - Support for simultaneous passive balancing of all channels with automatic odd/even sequence
  - Global balancing timeout timer
  - Timer controlled balancing with individual timers with 10 s resolution and up to 45 h duration
  - Voltage controlled balancing with global and individual undervoltage thresholds
  - Temperature controlled balancing; if balancing resistors or the IC are in overtemperature, balancing is interrupted
  - Configurable pulse width modulation (PWM) duty cycle balancing
  - Automatic pause of balancing during measurement with configurable filter settling time
  - Configurable delay of the start of balancing after transition to sleep
  - Automatic discharge of the battery pack (emergency discharge)
  - Constant current cell balancing to compensate the balancing current variation because of cell voltage variation
- I^2C-bus master interface to control external devices, for example, EEPROMs and security ICs
- Configurable alarm output
- Cyclic wake-up to monitor the pack and the balancing function during sleep.
- Capability to wake up the host MCU via daisy chain in case of a fault event.
- Host interface supporting SPI or isolated daisy chain communication (TPL3)
  - 2 Mbit/s data rate for TPL interface
  - 4 Mbit/s data rate for SPI interface
- TPL3 daisy chain communication supports
  - Two-wire daisy chain with capacitive or inductive isolation
  - Protocol supporting up to six daisy chains and 62 nodes per chain
- Unique device ID with dynamic addressing
- Operation modes
  - Active mode FP (12 mA typ.)
  - Sleep mode LP (60 µA typ.)
  - Deep Sleep mode ULP (15 µA typ.)

3 Applications

Automotive:

- (Plug-in) hybrid electric vehicle battery management system
- Electric vehicle battery management system

Industrial:

- Stationary ESS
- UPS systems

4 Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
MC33774ATA1	LQFP64	Plastic, thermal enhanced low profile quad flat package; 64 terminals; 0.50 mm pitch; 10 x 10 x 1.4 mm body	SOT1510-2

4.1 Ordering options

Table 2. Part numbers

Type number	Description
MC33774ATA1	TPL interface

5 Block diagram

Figure 1 shows the general architecture of the MC33774A.

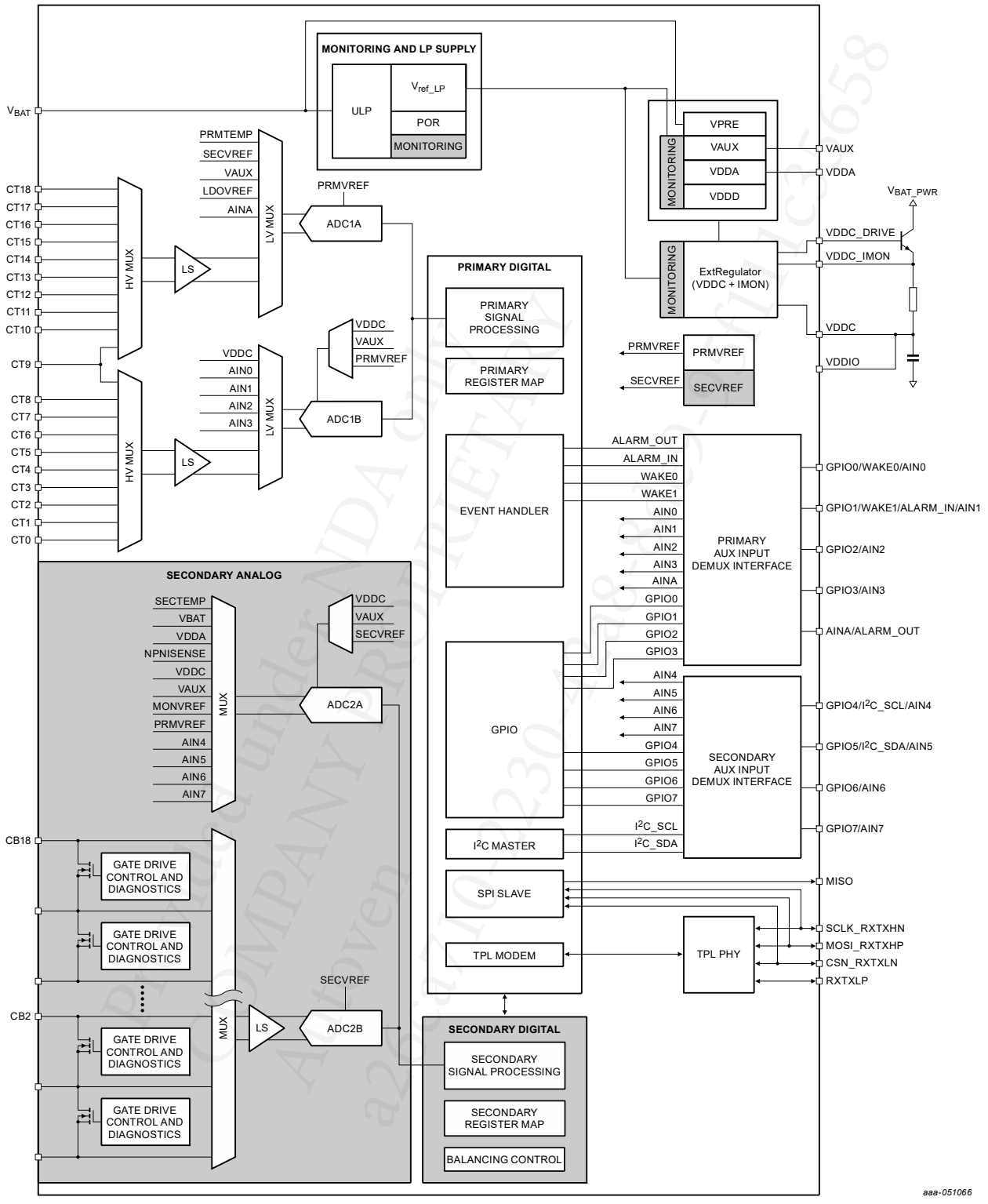


Figure 1. Simplified internal block diagram

6 Pinning information

6.1 Pinout diagram

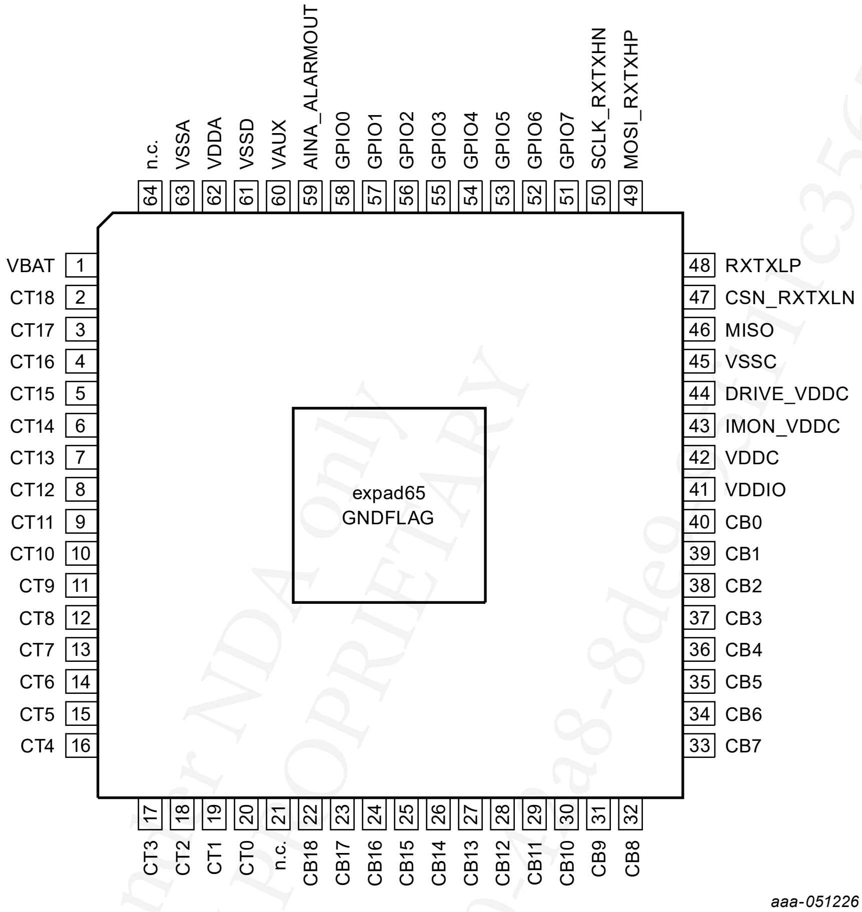


Figure 2. Pinout

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VBAT	1	Supply input of the product.
CT18	2	Cell terminal 18 input.
CT17	3	Cell terminal 17 input.
CT16	4	Cell terminal 16 input.
CT15	5	Cell terminal 15 input.
CT14	6	Cell terminal 14 input.
CT13	7	Cell terminal 13 input.
CT12	8	Cell terminal 12 input.
CT11	9	Cell terminal 11 input.
CT10	10	Cell terminal 10 input.

Table 3. Pin description*...continued*

Symbol	Pin	Description
CT9	11	Cell terminal 9 input.
CT8	12	Cell terminal 8 input.
CT7	13	Cell terminal 7 input.
CT6	14	Cell terminal 6 input.
CT5	15	Cell terminal 5 input.
CT4	16	Cell terminal 4 input.
CT3	17	Cell terminal 3 input.
CT2	18	Cell terminal 2 input.
CT1	19	Cell terminal 1 input.
CT0	20	Cell terminal 0 input.
n.c.	21	Not connected.
CB18	22	1. Secondary cell terminal 18 input 2. High input for cell 17 balancing
CB17	23	1. Secondary cell terminal 17 input 2. Low input for cell 17 balancing 3. High input for cell 16 balancing
CB16	24	1. Secondary cell terminal 16 input 2. Low input for cell 16 balancing 3. High input for cell 15 balancing
CB15	25	1. Secondary cell terminal 15 input 2. Low input for cell 15 balancing 3. High input for cell 14 balancing
CB14	26	1. Secondary cell terminal 14 input 2. Low input for cell 14 balancing 3. High input for cell 13 balancing
CB13	27	1. Secondary cell terminal 13 input 2. Low input for cell 13 balancing 3. High input for cell 12 balancing
CB12	28	1. Secondary cell terminal 12 input 2. Low input for cell 12 balancing 3. High input for cell 11 balancing
CB11	29	1. Secondary cell terminal 11 input 2. Low input for cell 11 balancing 3. High input for cell 10 balancing
CB10	30	1. Secondary cell terminal 10 input 2. Low input for cell 10 balancing 3. High input for cell 9 balancing
CB9	31	1. Secondary cell terminal 9 input 2. Low input for cell 9 balancing 3. High input for cell 8 balancing
CB8	32	1. Secondary cell terminal 8 input 2. Low input for cell 8 balancing 3. High input for cell 7 balancing
CB7	33	1. Secondary cell terminal 7 input 2. Low input for cell 7 balancing 3. High input for cell 6 balancing

Table 3. Pin description*...continued*

Symbol	Pin	Description
CB6	34	1. Secondary cell terminal 6 input 2. Low input for cell 6 balancing 3. High input for cell 5 balancing
CB5	35	1. Secondary cell terminal 5 input 2. Low input for cell 5 balancing 3. High input for cell 4 balancing
CB4	36	1. Secondary cell terminal 4 input 2. Low input for cell 4 balancing 3. High input for cell 3 balancing
CB3	37	1. Secondary cell terminal 3 input 2. Low input for cell 3 balancing 3. High input for cell 2 balancing
CB2	38	1. Secondary cell terminal 2 input 2. Low input for cell 2 balancing 3. High input for cell 1 balancing
CB1	39	1. Secondary cell terminal 1 input 2. Low input for cell 1 balancing 3. High input for cell 0 balancing
CB0	40	1. Secondary cell terminal 0 input 2. Low input for cell 0 balancing
VDDIO	41	External VDDIO supply input.
VDDC	42	External VDDC supply input.
IMON_VDDC	43	External NPN monitoring input.
DRIVE_VDDC	44	External NPN base output.
VSSC	45	VDDIO and VDDC ground reference.
MISO	46	SPI slave data output to master.
CSN_RXTXLN	47	1. SPI chip select input from master 2. TPLRX negative input from lower node 3. TPLTX negative output to lower node
RXTXLP	48	1. TPLRX positive input from lower node 2. TPLTX positive output to lower node
MOSI_RXTXHP	49	1. SPI slave data input from master 2. TPLRX positive input from upper node 3. TPLTX positive output to upper node
SCLK_RXTXHN	50	1. SPI clock input from master 2. TPLRX negative input from upper node 3. TPLTX negative output to upper node
GPIO7	51	1. Analog input AIN7 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN7 for absolute measurement 3. General-purpose input 7 4. General-purpose output 7
GPIO6	52	1. Analog input AIN6 for ratiometric measurement to VAUX / VDDC 2. Analog input AIN6 for absolute measurement 3. General-purpose input 6 4. General-purpose output 6
GPIO5	53	1. Analog input AIN5 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN5 for absolute measurement 3. General Purpose Input 5

Table 3. Pin description*...continued*

Symbol	Pin	Description
		4. General Purpose Output 5 5. I2CSDA
GPIO4	54	1. Analog input AIN4 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN4 for absolute measurement 3. General-purpose input 4 4. General-purpose output 4 5. I2CSCL
GPIO3	55	1. Analog input AIN3 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN3 for absolute measurement 3. General-purpose input 3 4. General-purpose output 3
GPIO2	56	1. Analog input AIN2 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN2 for absolute measurement 3. General-purpose input 2 4. General-purpose output 2
GPIO1	57	1. Analog input AIN1 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN1 for absolute measurement 3. General-purpose input 1 4. General-purpose output 1 5. Wake-up input 1 6. Alarm input
GPIO0	58	1. Analog input AIN0 for ratiometric measurement to VAUX/VDDC 2. Analog input AIN0 for absolute measurement 3. General-purpose input 0 4. General-purpose output 0 5. Wake-up input 0
AINA_ALARMOUT	59	1. Analog input AINA for absolute measurement 2. Alarm output
VAUX	60	Supply output for external sensors.
VSSD	61	Digital ground.
VDDA	62	Internal analog supply.
VSSA	63	Analog ground.
n.c.	64	Not connected.
GNDFLAG	Expad 65	Grounded exposed pad.

7 Functional description

The MC33774A is a lithium-ion battery-cell controller IC designed for automotive applications. The key functions of the MC33774A are shown in Figure 3.

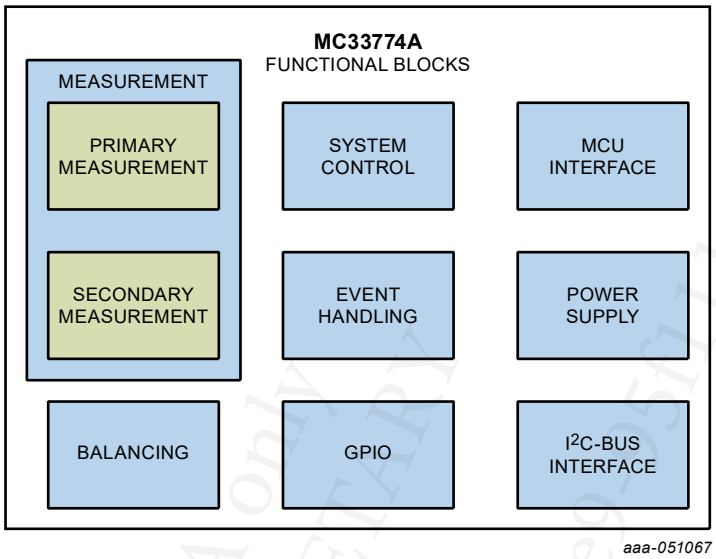


Figure 3. MC33774A key functions

The System control block defines the operational state and the basic configuration of the device.

The Event handling block configures the behavior of the device as response to events such as faults, wake-up, and alarms.

The Power supply section contains information about the power supply of the IC and the external supplies the MC33774A offers.

The MC33774A can measure and balance up to 18 battery cells. The measurement block, containing the primary and secondary measurements, is described in Section 7.4. Section 7.5 contains information about the cell balancing functionality.

The MC33774A provides eight general-purpose input/output (GPIO) pins. The GPIO ports can be used for several purposes, such as interrupt pins or to implement an I^2C-bus interface. See Section 7.6 for details about the GPIO pins and Section 7.8 for details on the I^2C-bus interface.

Communication between the superior control unit and the MC33774A is established via TPL or SPI by the microcontroller interface.

7.1 System control

The system control function block controls the operating modes of the device and, along with the operation mode, the availability of the various supply voltages described in Section 7.3.

7.1.1 Operation modes

The device offers four different operation modes.

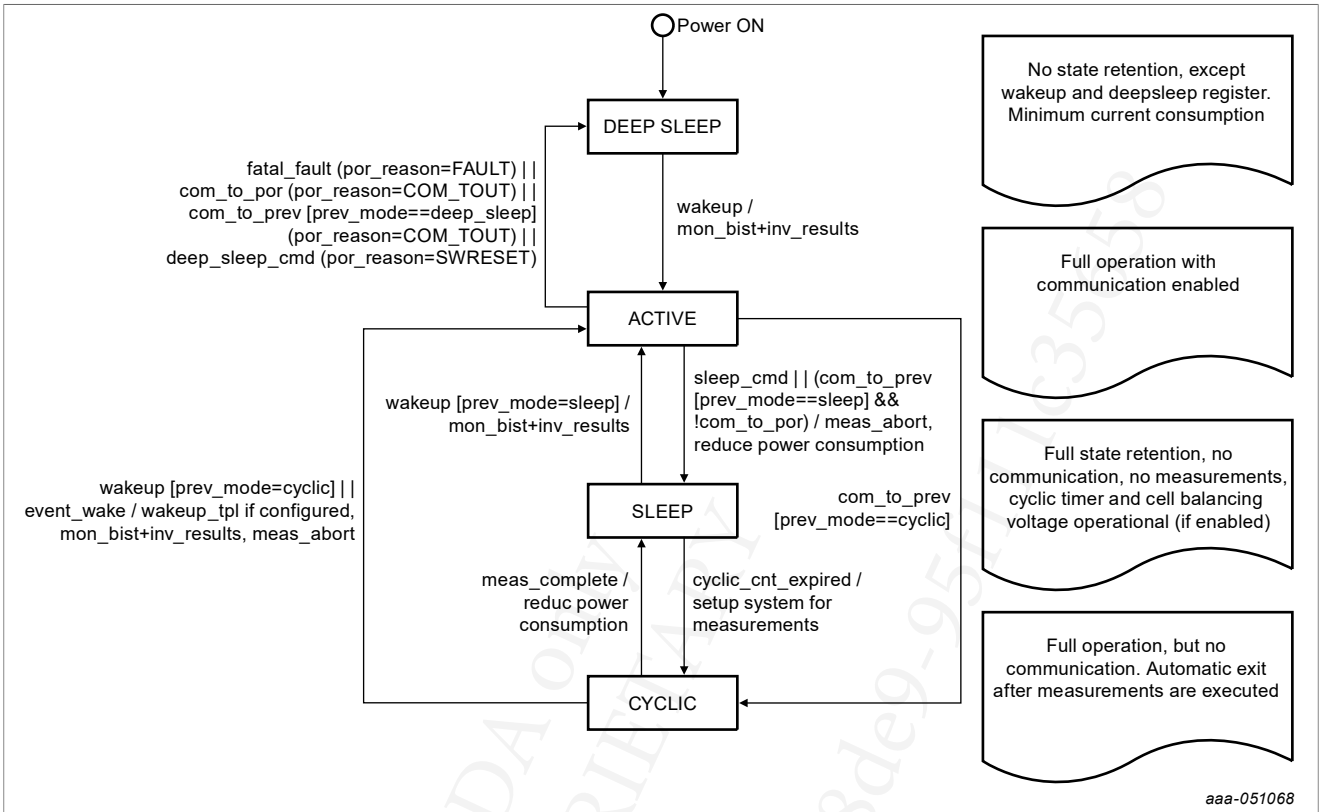


Figure 4. Overview of operation modes FSM

Table 4. Explanation of symbols

Name	Documentation
meas_abort	Abort measurement if currently ongoing.
wakeup_tpl	Send TPL wake-up frame.
reset	Reset and initialize IC.
mon_bist + inv_results	Run supply monitor BIST and set all measurement result registers to invalid.
com_to_por	Communication timeout occurred and timeout reaction is configured to POR.
com_to_prev	Communication timeout occurred and timeout reaction is configured to transition back to previous mode.
cyclic_cnt_expired	Cyclic wake-up counter has expired.
event_wake	An event configured for wake-up occurred: internal events configurable for wake-up (for example, OV/UV events) or configurable external wake-up sources (for example, GPIO wake-up pin).
fatal_fault	A fatal internal fault occurred or an internal event that is configured to trigger a POR occurred.
sleep_cmd	SW command to transition to sleep (SYS_MODE register).
deep_sleep_cmd	SW command to transition to deep sleep (SYS_MODE register).
wakeup	Wake-up event on the MCU interface detected.
prev_mode	Previous mode before transition.
por_reason	SYS_POR_REASON register.

Table 4. Explanation of symbols*...continued*

Name	Documentation
meas_complete	Measurement cycle completed.

Each operation mode has different features and power consumptions associated with it.

Table 5. Operation modes

Operation mode	Behavior	Application usage
Deep sleep (ULP)	Device is off; activation possible only via communication.	Storage mode and default mode after reset.
Sleep (LP)	Low-power operation mode.	Inactive mode, for example, parking of the vehicle; cell balancing possible.
Active	All functions enabled; full performance of device.	Monitoring of the battery.
Cyclic	Device switches automatically between Sleep mode and Active mode.	Balancing while parking of a vehicle.

7.1.1.1 Deep Sleep mode

In Deep Sleep mode, the device is offering the lowest current consumption. Deep Sleep mode is entered automatically after a power-on reset. The device remains in Deep Sleep mode until it detects bus activity. Other wake-up sources are disabled. The deep sleep storage data registers (SYS_DS_STORAGE0 and SYS_DS_STORAGE1) retain their current information. The register FEH_POR_REASON contains the information about the reason for entering Deep Sleep mode. All other registers are reset.

Setting the bit field SYS_MODE.TARGETMODE to DEEPSLEEP (14h) initiates the transition to Deep Sleep mode. This bit field must be set with a message that accesses only the SYS_MODE.TARGETMODE register.

Note: *Single-register access is achieved by setting DATALEN to 00b. See Section 7.9.1.1 for details.*

7.1.1.2 Sleep mode

In Sleep mode, the current consumption is very low. The device monitors the wake-up sources, but does not perform ADC conversions. Balancing is possible in Sleep mode. The register content of the cell balancing registers, the system control registers, the event handling registers, and the primary measurement register remain valid. All other registers are reset. With the SYS_CYC_WAKEUP_CFG register set to 0000h, the MC33774A remains in Sleep mode until a transition to active mode is initiated. With SYS_CYC_WAKEUP_CFG register set to a value other than 0000h the device automatically changes between sleep and cyclic mode.

The sequence to enter Sleep mode in a controlled way is:

1. Read undervoltage and overvoltage status bits to confirm system integrity.
2. Disable the measurement (measurement results are invalidated).
3. Read undervoltage and overvoltage status bits and discard the results.
4. Read FEH_WAKEUP_REASON to ensure no wake-up events are pending.
5. Send go-to-sleep command.

Setting the bit field SYS_MODE.TARGETMODE to SLEEP (0Ah) initiates the transition to Sleep mode. This bit field must be set with a message that accesses only the SYS_MODE.TARGETMODE register.

Note: *Single-register access is achieved by setting DATALEN to 00b. See Section 7.9.1.1 for details.*

7.1.1.3 Active mode

In Active mode, the device is fully operational. When entering Active mode, all measurement results are invalidated. A BIST is executed when entering into Active mode to check the integrity of the device.

7.1.1.4 Cyclic mode

Cyclic mode is entered via Sleep mode with SYS_CYC_WAKEUP_CFG register set to a value other than 0000h. The device automatically transitions between cyclic and sleep states. In the cyclic state, MC33774A executes one periodic measurement (Section 7.4.3.1) and evaluates the results for undervoltage and overvoltage conditions. After the evaluation, it either returns to Sleep mode or wakes up if any of the configured wake-up events (Section 7.2.2) has been detected. The bit field SYS_CYC_WAKEUP_CFG.PERIOD configures the cycle time.

Note: *The MC33774A manages the MEASEN bit in Cyclic mode automatically.*

7.1.2 System control features

7.1.2.1 System configuration CRC

The MC33774A contains many configuration registers. All of these registers can be read to verify the device configuration. The MC33774A calculates a cyclic redundancy check (CRC) across the content of the configuration registers. The MCU can use this CRC value to validate the integrity of the configuration. The CRC is recalculated whenever a register covered by the CRC is written or the CRC value is read.

The system configuration CRC covers the SYS_COM_CFG, SYS_COM_TO_CFG, SYS_SUPPLY_CFG, SYS_CYC_WAKEUP_CFG, and SYS_TPL_CFG register.

The used polynomial is: D175h (+1) = $X^{16} + X^{15} + X^{13} + X^9 + X^7 + X^6 + X^5 + X^3 + X^1 + 1$.

Note: *The CRC value depends on the configuration of the device and is therefore application dependent.*

Note: *The polynomial used here is different to the polynomial used for communication.*

Application usage: Check integrity of the system configuration.

7.1.2.2 Communication, communication timeout configuration, and TPL configuration

The register SYS_COM_CFG contains the daisy chain and device address of the device, as well as the overall number of devices in the daisy chain.

The register SYS_COM_TO_CFG configures the communication timeout of the device.

The register SYS_TPL_CFG configures the wake-up compatibility, termination, and response properties of the TPL ports.

The configuration applied here is used by the microcontroller interface. For a detailed description, see Section 7.9.

7.1.2.3 Supply configuration

VDDC and VAUX are intended to supply the GPIO ports and sensor networks. The bits VDDCCYC and VAUXCYC in the SYS_SUPPLY_CFG register control the state of the VDDC and VAUX supplies in Cyclic mode. The bit VAUXACT controls the state of VAUX in Active mode.

The bit CURMATCH enables the supply current matching feature of the MC33774A. When the feature is enabled, the current consumption of the MC33774A is within $\Delta I_{BAT(FP)}$.

7.1.2.4 System mode and interval for cyclic measurements

The registers SYS_MODE and SYS_CYC_WAKEUP_CFG control the operation mode of the device and the interval for the cyclic measurements.

Application usage: State control and monitoring of the system voltages, for example, during balancing in Sleep mode.

7.1.2.5 Clock synchronization

With the register SYNCCNT, it is possible to adjust the internal clock of the MC33774A.

Application usage: Synchronize measurement timing between multiple MC33774A devices.

7.1.2.6 System version

The SYS_VERSION register provides information about the revision of the silicon.

Table 6. System version identification

TYPE	FREV	MREV	Silicon state
03h	2h	1h	B silicon
Others			Reserved for future usage

Application usage: Identification of silicon revision.

7.1.2.7 Software interface information

The MC33774A does not contain software, but provides some information about the compatibility between the register definitions of different product variants. The SYS_PROD_VER register allows a fast assessment whether software generated for a specific product version can be used for other product versions.

Table 7. Software interface information

Major	Minor	Patch	Silicon state
2h	0h	0h	B silicon

7.1.2.8 Unique device ID

The registers SYS_UID_LOW, SYS_UID_MID, and SYS_UID_HIGH provide together a unique identification value for each MC33774A.

Application usage: Identification of ICs for system integrity checks and tracking.

7.1.2.9 Deep sleep storage data

The registers SYS_DS_STORAGE0 and SYS_DS_STORAGE1 provide 32-bit data storage. The bits are not used by the MC33774A and are free to be used in the overall application. The MC33774A never clears the content of these registers. However, when the supply voltage for the MC33774A is removed, the content of the register is lost. The register is not initialized at restart of the IC and may show any value.

Application usage: Storage of tracking data; storage of current class for contactor relays.

7.1.3 System control registers

All registers related to the system control are listed here. Details to the registers and the bit fields are explained in the register map chapter.

Table 8. Register overview: System_Control_Registers

Address	Name	Access	Reset	Description
0h	SYS_CFG_CRC	R	0h	system configuration CRC
1h	SYS_COM_CFG	R/W	200h	communication initialization
2h	SYS_COM_TO_CFG	R/W	1Eh	system communication timeout
3h	SYS_SUPPLY_CFG	R/W	8003h	supply configuration
4h	SYS_MODE	R/W	1400h	system mode
5h	SYS_CYC_WAKEUP_CFG	R/W	0h	interval for cyclic measurements
6h	SYS_TPL_CFG	R/W	10h	TPL configuration
8h	SYS_CLK_SYNC_CTRL	R/W	0h	clock Synchronization
10h	SYS_VERSION	R	320h	device silicon identifier
11h	SYS_UID_LOW	R	0h	unique device ID lower part
12h	SYS_UID_MID	R	0h	unique device ID middle part
13h	SYS_UID_HIGH	R	0h	unique device ID higher part
14h	SYS_PROD_VER	R	200h	software interface related version of the product
80h	SYS_DS_STORAGE0	R/W	0h	deep sleep storage data 0; the value is stored in the ULP domain
81h	SYS_DS_STORAGE1	R/W	0h	deep sleep storage data 1; the value is stored in the ULP domain

7.2 Event handling

The event handling block configures the reaction of the device when events or faults occur.

During regular operation of the device, events can occur. Events are items, such as wake-up or alarm signals. Events can cause a wake-up and/or an activation of the alarm output.

The term "fault" is used for events that should not occur during regular operation. Faults indicate a malfunction of the system, such as missing supply voltages. For faults, it can be selected to create a power-on reset (POR) or create a fault event. If nothing is selected, the fault is only reported.

Figure 5 shows the principle structure of the fault and event handling in the system.

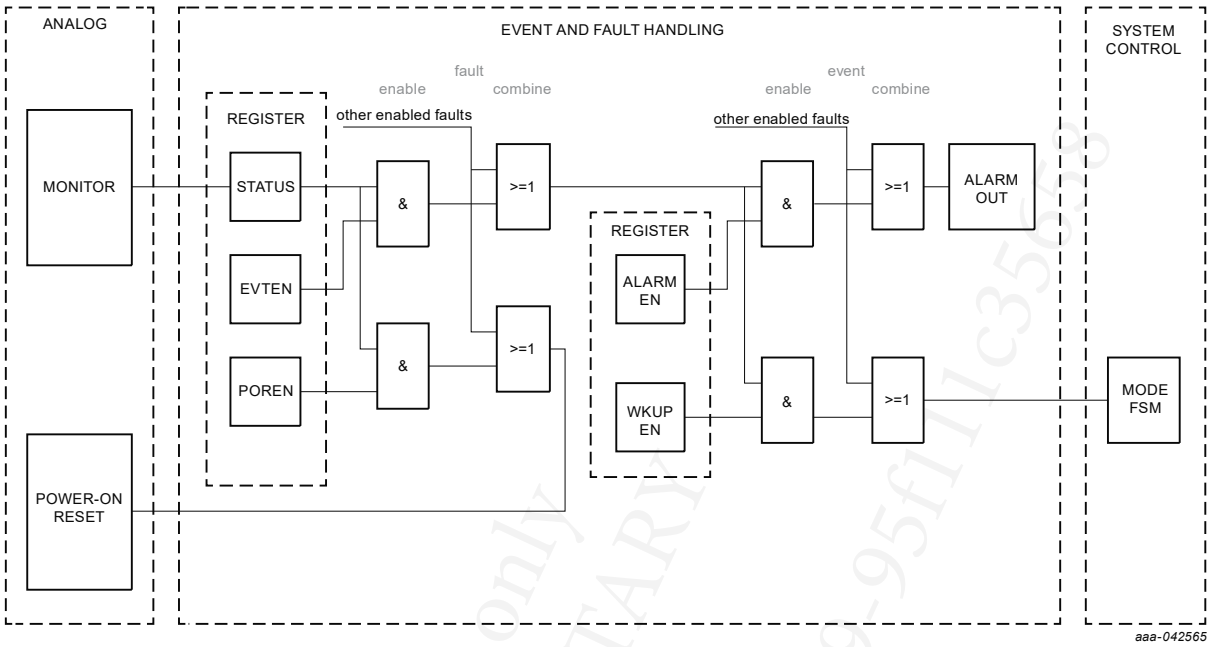


Figure 5. Event handling

7.2.1 Faults

The MC33774A monitors the system for faults. The monitoring is done via dedicated hardware instances and independent of the measurement block. Some faults are critical for the correct operation of the device. These faults (VDDDLPPERMUV, VBATUV, VDDCOC, VDDDOV, VDDDUV, VDDDLPUV, OTEMPSHUTDOWN, PRMCLK, SECCLK, SLEEPOSC, and LOGICERR) trigger a POR.

Once a fault is detected, the corresponding fault bit is set. Individual faults are grouped into supply, analog, communication, and measurement-related faults allowing a quick overview. Register FEH_GRP_FLT_STAT provides the overview based on the fault group. The fault registers (FEH_SUPPLY_FLT_STAT0, FEH_SUPPLY_FLT_STAT1, FEH_ANA_FLT_STAT, FEH_COM_FLT_STAT, and FEH_MEAS_FLT_STAT) signal the specific fault. For each fault, it can be selected that the MC33774A directly issues a POR, and/or generates a system fault event (SYSFLTEVT). If nothing is selected, the device reports the fault and continues operation.

Table 9. Overview of faults

Faults	Fault description	Forced POR	Fault group	Monitoring condition	Covered by BIST	Effects and comments
VDDDLPPERMUV	Undervoltage on internal supply for low-power operation.	Yes	SUPPLYFLT	All modes	No	
VBATOV	Overvoltage condition on pin VBAT (external supply for IC).	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST	• Disabling of balancing • Incorrect ADC results for VBAT • Disables AFECP leading to AFECPUV • Invalidation of SYNC measurement results in SECM
VBATLV	Low-voltage condition on pin VBAT (external supply for IC).	Yes, in case automatic discharge is on; selectable	SUPPLYFLT	Active and Cyclic modes; Sleep mode if balancing is enabled	No	Generates wake event in case balancing is Active and FEH_

Table 9. Overview of faults*...continued*

Faults	Fault description	Forced POR	Fault group	Monitoring condition	Covered by BIST	Effects and comments
		in case automatis discharge is off				WAKEUP_CFG0. SYSFLTEV is set
VBATUV	Undervoltage condition on pin VBAT (external supply for IC).	Yes	SUPPLYFLT		No	
VDDCOV	Overvoltage condition on VDDC (supply for GPIO pins and TPL interface).	Selectable	SUPPLYFLT	Active mode and Cyclic mode when VDDCCYC = 1	Manual BIST	Invalidation of APP results in case VDDC is used for ratiometric results
VDDCUV	Undervoltage condition on VDDC (supply for GPIO pins and TPL interface).	Selectable	SUPPLYFLT	Active mode and Cyclic mode when VDDCCYC = 1	Manual BIST	Invalidation of APP results in case VDDC is used for ratiometric results
VDDCOC	Overcurrent condition on VDDC.	Yes	SUPPLYFLT	Active mode and Cyclic mode when VDDCCYC = 1	No	
VDDCHC	High current condition on VDDC.	Selectable	SUPPLYFLT	Active mode and Cyclic mode when VDDCCYC = 1	No	
VAUXOV	Overvoltage condition on VAUX (supply for external circuit).	Selectable	SUPPLYFLT	Active mode when VAUXACT = 1 and Cyclic mode when VAUXCYC = 1	Manual BIST	Invalidation of APP results in case VAUX is used for ratiometric results
VAUXUV	Undervoltage condition on VAUX (supply for external circuit).	Selectable	SUPPLYFLT	Active mode when VAUXACT = 1 and Cyclic mode when VAUXCYC = 1	Manual BIST	Invalidation of APP results in case VAUX is used for ratiometric results
VDDIOOV	Overvoltage condition on VDDIO (supply for SPI and I2C-bus).	Selectable	SUPPLYFLT	Active and Cyclic modes	No	
VDDIOUV	Undervoltage condition on VDDIO (supply for SPI and I2C-bus).	Selectable	SUPPLYFLT	Active and Cyclic modes	No	
VDDDOV	Overvoltage condition on VDDD (internal digital supply).	Yes	SUPPLYFLT	Active, Cyclic, and Sleep modes	No	
VDDDUV	Undervoltage condition on VDDD (internal digital supply).	Yes	SUPPLYFLT	Active, Cyclic, and Sleep modes	No	
VDDDLPUV	Undervoltage on internal supply for low-power operation.	Yes	SUPPLYFLT	Active and Cyclic modes	No	
VDDAOV	Overvoltage condition on VDDA	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST and manual BIST	Invalidation of SYNC measurement results in SECM

Table 9. Overview of faults*...continued*

Faults	Fault description	Forced POR	Fault group	Monitoring condition	Covered by BIST	Effects and comments
	(internal analog supply).					
VDDAUV	Undervoltage condition on VDDA.	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST and manual BIST	Invalidation of SYNC measurement results in SECM
VPREOV	Overvoltage condition on VPRE (supply of the IC).	Selectable	SUPPLYFLT	Active and Cyclic modes	No	
VPREUV	Undervoltage condition on VPRE (supply of the IC).	Selectable	SUPPLYFLT	Active and Cyclic modes	No	
VPREREFSOV	Overvoltage condition on VPR EREFS (supply for IC reference).	Selectable	SUPPLYFLT	Active and Cyclic modes	No	
VPREREFSUV	Undervoltage condition on VPR EREFS (supply for IC reference).	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST and manual BIST	
VANAOV	Overvoltage condition on VANA.	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST and manual BIST	Invalidation of SYNC measurement results in SECM
VANAUV	Undervoltage condition on VANA.	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST and manual BIST	Invalidation of SYNC measurement results in SECM
AFECPOV	Overvoltage condition on AFECP.	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST and manual BIST	Invalidation of SYNC measurement results in SECM
AFECPUV	Undervoltage condition on AFECP.	Selectable	SUPPLYFLT	Active and Cyclic modes	Start-up BIST and manual BIST	• Invalidation of SYNC measurement results in SECM • AFECPUV can only be cleared if VBATOV is cleared.
OTEMPSHUT DOWN	Too high junction temperature.	Yes	ANAFLT	Active and Cyclic modes	No	
MONBIST	BIST monitor failure.	No	ANAFLT	On entering Active mode; during manual BIST		
PRMCLK	Primary clock monitor failure.	Yes	ANAFLT	Active and Cyclic modes	No	Invalidation of SYNC measurement results in SECM
SECCLK	Secondary clock monitor failure.	Yes	ANAFLT	Active mode when SECM_CFG. MEASEN = 1	No	Invalidation of SYNC measurement results in SECM
SLEEPOSC	Low frequency oscillator failure.	Yes	ANAFLT	Active, Cyclic, and Sleep modes	No	
FUSEERR	Corrected single bit error in fuses.	No	ANAFLT	Active, Cyclic, and Sleep modes	No	
BALERR	Balancing switch fault.	No	ANAFLT	Active and Cyclic; in Sleep mode, BALERR is detected but wake is only issued in	No	

Table 9. Overview of faults*...continued*

Faults	Fault description	Forced POR	Fault group	Monitoring condition	Covered by BIST	Effects and comments
				Cyclic and Active mode		
FRAMEERR	Communication frame error.	No	COMFLT	Active mode	No	
CRCERR	Communication CRC error.	No	COMFLT	Active mode	No	
COMTO	Communication timeout.	Selectable	COMFLT	Active mode	No	
COMERRORS	> 255 communication errors.	Selectable	COMFLT	Active mode	No	
PRIMCALCRCFLT	Primary calibration CRC error.	No	MEASFLT	On entering Active or Cyclic mode; start of a synchronous measurement	No	Invalidation of SYNC measurement results in SECM
SECCALCCRCFLT	Secondary calibration CRC error.	No	MEASFLT	On entering Active or Cyclic mode; start of a synchronous measurement	No	Invalidation of SYNC measurement results in SECM
LOGICERR	EDC error.	Yes	MEASFLT	Active, Cyclic, and Sleep modes	No	
SYNCMEASFLT	Synchronous measurement error.	No	MEASFLT	During synchronous measurements	No	Invalidation of SYNC measurement results in SECM

Application usage: Check for faults in the system.

7.2.2 Events

Events are situations that occur during the normal operation of the product. Events include various system faults, balancing ready, voltage checks based on measured data, and so on. Events can be used to trigger a wake-up or can be output via the alarm output signal.

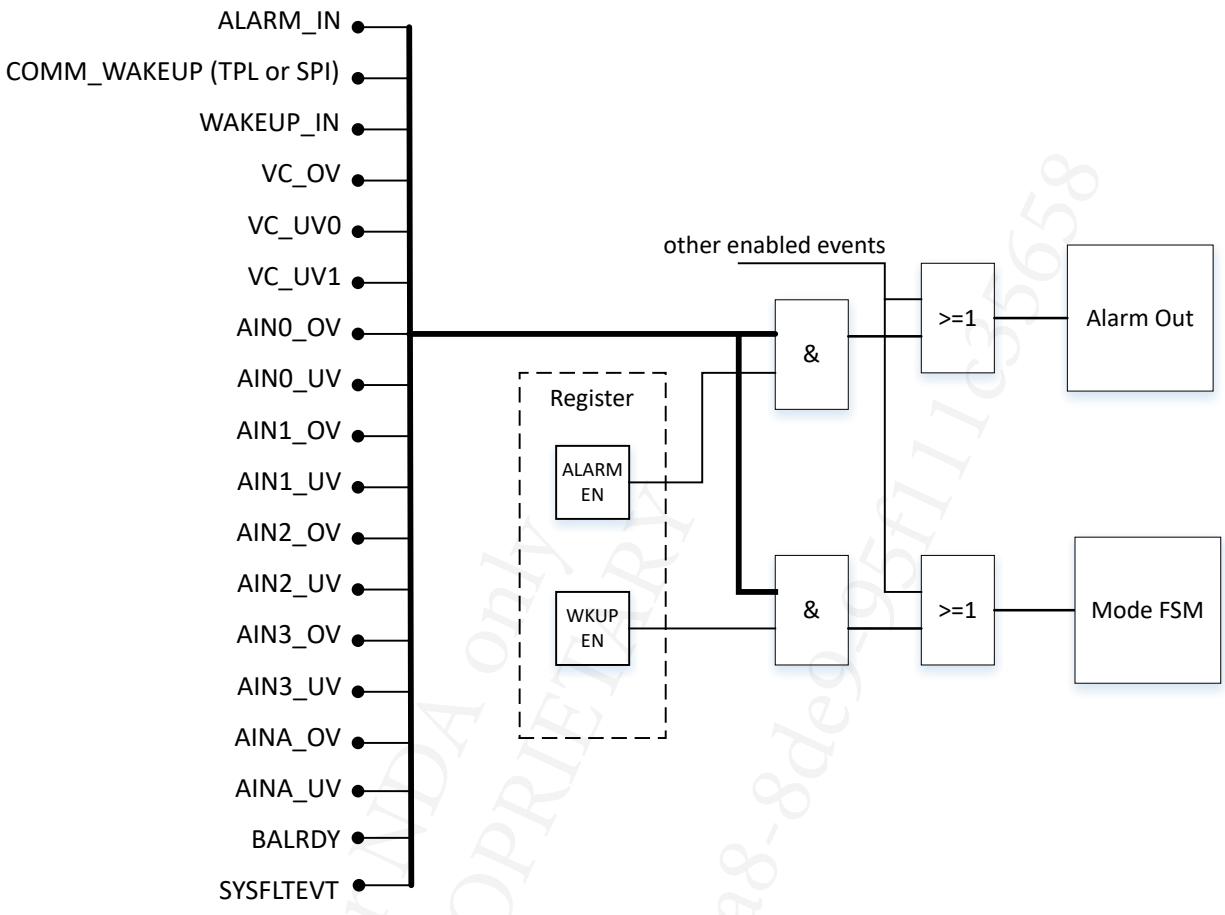


Figure 6. Event propagation

The register FEH_ALARM_CFG (Section 12.1.17) configures which events generate an alarm.

Registers FEH_WAKEUP_CFG0 and FEH_WAKEUP_CFG1 (Section 12.1.22) do configure which events generate a wake-up. The wake-up initiates state transition as described in operation modes and initiates wake-up commands as described in Section 7.9.2.

Table 10. Overview of events

Events	Event description
ALARM_IN	Alarm detection on alarm input pins
COMM_WAKEUP (TPL or SPI)	Wake-up via communication
WAKEUP_IN	Wake-up via wake-up input
VC_OV	Cell voltage on one of the cells enabled in PRMM_VC_OV_UV_CFG measured to be higher than PRMM_VC_OV_TH_CFG
VC_UV0	Cell voltage on one of the cells enabled in PRMM_VC_OV_UV_CFG measured to be lower than PRMM_VC_UV0_TH_CFG
VC_UV1	Cell voltage on one of the cells enabled in PRMM_VC_OV_UV_CFG measured to be lower than PRMM_VC_UV1_TH_CFG
AIN0_OV	Voltage at pin AIN0 measured to be above PRMM_AIN0_OV_TH_CFG
AIN0_UV	Voltage at pin AIN0 measured to be below PRMM_AIN0_UV_TH_CFG
AIN1_OV	Voltage at pin AIN1 measured to be above PRMM_AIN1_OV_TH_CFG

Table 10. Overview of events*...continued*

Events	Event description
AIN1_UV	Voltage at pin AIN1 measured to be below PRMM_AIN1_UV_TH_CFG
AIN2_OV	Voltage at pin AIN2 measured to be above PRMM_AIN2_OV_TH_CFG
AIN2_UV	Voltage at pin AIN2 measured to be below PRMM_AIN2_UV_TH_CFG
AIN3_OV	Voltage at pin AIN3 measured to be above PRMM_AIN3_OV_TH_CFG
AIN3_UV	Voltage at pin AIN3 measured to be below PRMM_AIN3_UV_TH_CFG
AINA_OV	Voltage at pin AINA measured to be below PRMM_AINA_OV_TH_CFG
AINA_UV	Voltage at pin AINA measured to be below PRMM_AINA_UV_TH_CFG
BALRDY	Balancing activity finished; bit BALRDY is set
SYSFAULT	Occurrence of a fault (see Table 9) that: 1. Does not result in a POR. 2. Is enabled.

Application usage: Notification of MCU about events.

7.2.3 Alarm output

The MC33774A offers an alarm output on AINA_ALARMOUT pin. The alarm output is only available in Active mode. The register FEH_ALARM_CFG defines the configuration. The configuration options are Active HIGH, Active LOW, or Heartbeat mode. In Heartbeat mode, the MC33774A provides a pattern with a fixed high time and a selectable low time.

Application usage: Notification of MCU about events. Heartbeat mode is also used for checking of integrity of the alarm line.

7.2.4 Alarm input

The MC33774A offers an alarm input on GPIO1 pin. The register FEH_ALARM_CFG defines the configuration. The configuration options are Active HIGH, Active LOW, or Heartbeat mode. In Heartbeat mode, the MC33774A expects a pattern with a fixed high time and a selectable low time. The bit FEH_ALARM_CFG.ALARMINHBINV allows inverting the expected pattern. The device is then expecting a fixed low time and a selectable high time.

Application usage: Forwarding of events. Heartbeat mode is also used for checking of integrity of the alarm line.

7.2.5 Built-in self-test (BIST)

The MC33774A has two BIST methods implemented. The start-up BIST is executed automatically each time the device is entering into Active mode. The manual BIST is started when the bit FEH_MON_BIST_CTRL.STARTBIST is set. FEH_MON_BIST_CTRL.BISTCRC reflects the CRC result of the last BIST. This information shows a completion of the BIST. The individual results of the BIST can be read in the register FEH_MON_BIST_RES. The covered faults of the BIST are shown in Table 9.

Note: *Execution of the BIST is manipulating the inputs to the measurements of the MC33774A. The execution of the BIST results in erratic measurements and triggers system faults. During the execution of the start-up BIST, the system faults are masked. No masking is applied during the manual BIST. The MC33774A reacts to the faults introduced during the manual BIST in the same way as in normal operation. As per the configuration of the device, invalidation of the measurement result, an activation of the fault and alarm outputs, or a POR is initiated. Measurement results that have been acquired while the BIST was Active must be discarded.*

Application usage: Functionality check of monitoring instances.

7.2.6 Event handling configuration CRC

The MC33774A contains many configuration registers. For validation of the correctness of the configuration of the device, all configuration registers can be read. The MC33774A is calculating a CRC across the content of the configuration registers. The MCU can use this CRC value to validate the integrity of the configuration. The CRC is recalculated whenever a register covered by the CRC is written or the CRC value is read.

The event handling CRC covers the FEH_ALARM_CFG, FEH_ALARM_OUT_CFG0, FEH_ALARM_OUT_CFG1 , FEH_WAKEUP_CFG0, FEH_WAKEUP_CFG1, FEH_SUPPLY_FLT_POR_CFG0, FEH_SUPPLY_FLT_POR_CFG1, FEH_ANA_FLT_POR_CFG, FEH_COM_FLT_POR_CFG, FEH_SUPPLY_FLT_EVT_CFG0, FEH_SUPPLY_FLT_EVT_CFG1, FEH_ANA_FLT_EVT_CFG, FEH_COM_FLT_EVT_CFG, and FEH_MEAS_FLT_EVT_CFG register.

The used polynomial is: D175h (+1) = $X^{16} + X^{15} + X^{13} + X^9 + X^7 + X^6 + X^5 + X^3 + X^1 + 1$.

Note: *The CRC value depends on the configuration of the device and is therefore application dependent.*

Note: *The polynomial used here is different to the polynomial used for communication.*

Application usage: Check of integrity of the system configuration.

7.2.7 Last POR reason

The register FEH_POR_REASON provides information about the reason of the last POR. The error code for the various reasons is listed in the FEH_POR_REASON register.

A POR may not always be initiated by a single source, but by an event that causes multiple reasons to occur simultaneously. In case supplies are affected, the integrity of the FEH_POR_REASON may also be affected. Because of this reason, the content of the FEH_POR_REASON should only be considered as an indication and so used only for debugging purposes.

Application usage: Debugging information.

7.2.8 Event handling registers

All registers related to the event handling are listed here. Details of registers and the bit fields are explained in the register map chapter.

Table 11. Register overview: Event_Handling_Registers

Address	Name	Access	Reset	Description
400h	FEH_CFG_CRC	R	0h	configuration CRC
401h	FEH_ALARM_CFG	R/W	0h	general alarm configuration
402h	FEH_ALARM_OUT_CFG0	R/W	0h	alarm output source selection
403h	FEH_ALARM_OUT_CFG1	R/W	0h	alarm output source selection
404h	FEH_ALARM_OUT_REASON0	R	0h	alarm output reason
405h	FEH_ALARM_OUT_REASON1	R	0h	alarm output reason
408h	FEH_WAKEUP_CFG0	R/W	0h	wake up source configuration
409h	FEH_WAKEUP_CFG1	R/W	0h	wake up source configuration
40Ah	FEH_WAKEUP_REASON0	R	0h	wake up reason register
40Bh	FEH_WAKEUP_REASON1	R	0h	wake up reason register
410h	FEH_MON_BIST_CTRL	R/W	0h	monitor BIST control register

Table 11. Register overview: Event_Handling_Registers...*continued*

Address	Name	Access	Reset	Description
411h	FEH_MON_BIST_RES	R	FFh	monitor BIST result register; value changes at start-up, if everything is fine to 0000h
41Eh	FEH_ACC_ERR	R	0h	access error status register
41Fh	FEH_GRP_FLT_STAT	R	0h	main system fault status register; this register holds one bit per fault group. For each fault group a separate status register exists. The bit here is cleared if all its sources are cleared.
420h	FEH_SUPPLY_FLT_STAT0	R/W	0h	supply fault status register 0 (these monitors are part of the BIST)
421h	FEH_SUPPLY_FLT_STAT1	R/W	0h	supply fault status register 1 (these monitors are not part of the BIST)
422h	FEH_ANA_FLT_STAT	R/W	0h	analog fault status register
423h	FEH_COM_FLT_STAT	R/W	0h	communication fault status register
424h	FEH_MEAS_FLT_STAT	R/W	0h	other fault status register
428h	FEH_SUPPLY_FLT_POR_CFG0	R/W	0h	supply fault POR selection 0
429h	FEH_SUPPLY_FLT_POR_CFG1	R/W	0h	supply fault POR selection 1
42Ah	reserved	R	0h	analog fault POR selection
42Bh	FEH_COM_FLT_POR_CFG	R/W	8h	communication fault POR enable register
430h	FEH_SUPPLY_FLT_EVT_CFG0	R/W	0h	supply fault event selection register 0
431h	FEH_SUPPLY_FLT_EVT_CFG1	R/W	0h	supply fault event selection register 1
432h	FEH_ANA_FLT_EVT_CFG	R/W	0h	analog fault event enable register
433h	FEH_COM_FLT_EVT_CFG	R/W	0h	communication fault event enable register
434h	FEH_MEAS_FLT_EVT_CFG	R/W	0h	measurement fault event enable register
480h	FEH_POR_REASON	R	0h	power-on reset reason. The value is stored in the ULP domain.

7.3 Power supply

The power supply block provides all voltages that are required internally, as well as the voltages provided externally. In addition, it monitors the voltages for overvoltage and undervoltage.

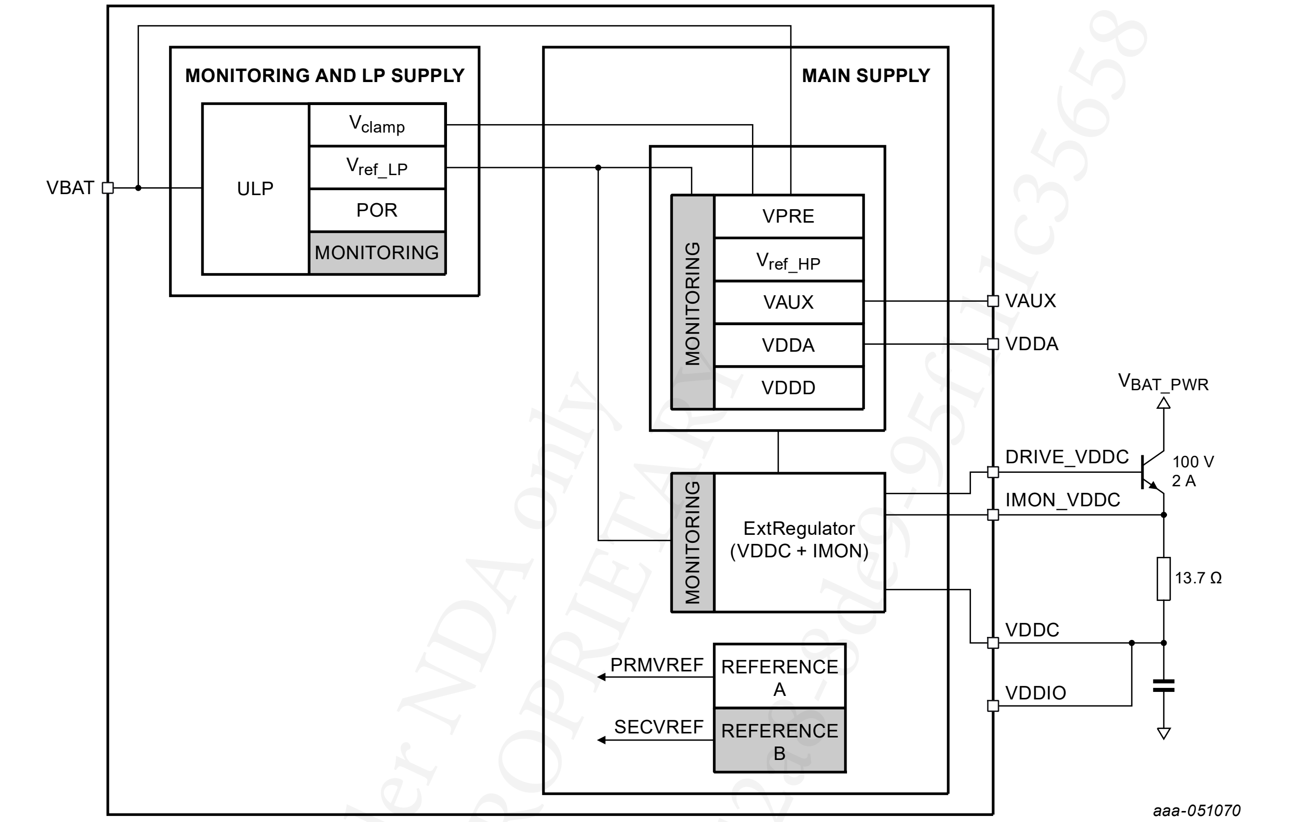


Figure 7. Power supply diagram

7.3.1 Overview

Table 12 gives an overview of the supplies, the intended usage, the source, and the diagnostic information for this supply.

Table 12. Supply overview

Supply	Intended usage	Source	Diagnostics
VBAT	External supply for IC	External	1. Overvoltage and undervoltage 2. Analog voltage measurement
VPRE	Supply of the IC	VBAT	Overvoltage
VPREREF	Supply for IC references	VBAT	Undervoltage and overvoltage
VAUX	Supply for external circuits	VPRE	1. Undervoltage and overvoltage 2. Analog voltage measurement
VDDC	Supply for GPIO pins and TPL interface	External	1. Undervoltage and overvoltage 2. Analog current measurement 3. High current and overcurrent 4. Analog voltage measurement

Table 12. Supply overview*...continued*

Supply	Intended usage	Source	Diagnostics
VDDIO	Supply for SPI and I^2C-bus	External or VDDC	Undervoltage and overvoltage
Internal: RevLDO	Reference for supplies	VPRE	Analog voltage measurement
Internal: VDDA	Internal analog supply	VPRE	1. Undervoltage and overvoltage 2. Analog voltage measurement
Internal: VDDD	Internal digital supply	VPRE	Undervoltage and overvoltage (forces power-on reset, info can be read in FEH_POR_REASON.SOURCE)
Internal: RefA	Reference voltage for ADC1	VPREREF	Analog voltage measurement
Internal: RefB	Reference voltage for ADC2	VPREREF	Analog voltage measurement
Internal: RevMON	Supply monitoring	VPREREF	Analog voltage measurement
Internal: VANA	Internal analog supply	VPRE	Undervoltage and overvoltage
Internal: IBIAS	Internal reference current	VPRE	Undercurrent and overcurrent
Internal: AFE charge pump	Internal analog supply	VPRE	Undervoltage and overvoltage

Table 13 gives an overview of the availability of the supplies in the various operation modes.

Table 13. Availability of supplies vs. operation modes

Supply	Active mode	Cyclic mode	Sleep mode	Deep sleep mode
VDDC	Available	Available if VDDCCYC = 1	Off	Off
VAUX	Available if VAUXACT = 1	Available if VAUXCYC = 1	Off	Off

7.3.2 VPRE

VPRE is a preregulated supply voltage. VPRE is generated out of the VBAT voltage. Most of the supply voltages, reference voltages, and reference currents are derived from VPRE. A detailed overview is given in Table 12.

7.3.3 VAUX

VAUX is intended to supply external analog circuits, such as resistor and negative temperature coefficient (NTC) networks.

VAUX can also be used as reference voltage for the ADC converter in case ratiometric measurements are needed. See Section 7.4 for more details.

7.3.4 VDDC

VDDC is used for the GPIO pins and the TPL communication. VDDC can also be used as supply for VDDIO and external analog circuits, and as reference voltage for the ADC converter in case ratiometric measurements are needed. To limit the power dissipation inside the IC, VDDC is generated via an external transistor. See Section 7.4 for more details.

7.3.5 VDDIO

VDDIO is an input voltage of the MC33774A. VDDIO can be supplied by a 5 V supply, such as VDDC, or via an external 3.3 V regulator. VDDIO is used for SPI and I^2C-bus interface.

7.3.6 Others

VDDA, VDDD, RefA, RefB, VANA, IBIAS, and analog front-end (AFE) are internal voltages or currents. They do not have a direct connection to a pin of the IC. For functional safety reasons, the device monitors these voltages or currents.

7.4 Measurement

The MC33774A offers a primary and a secondary measurement chain. The two chains are independent from each other. The measurement operations of the two measurement chains can be synchronized.

7.4.1 Functional diagram

Figure 8 and Figure 9 show the functional diagrams of the measurement blocks.

7.4.1.1 Primary measurement

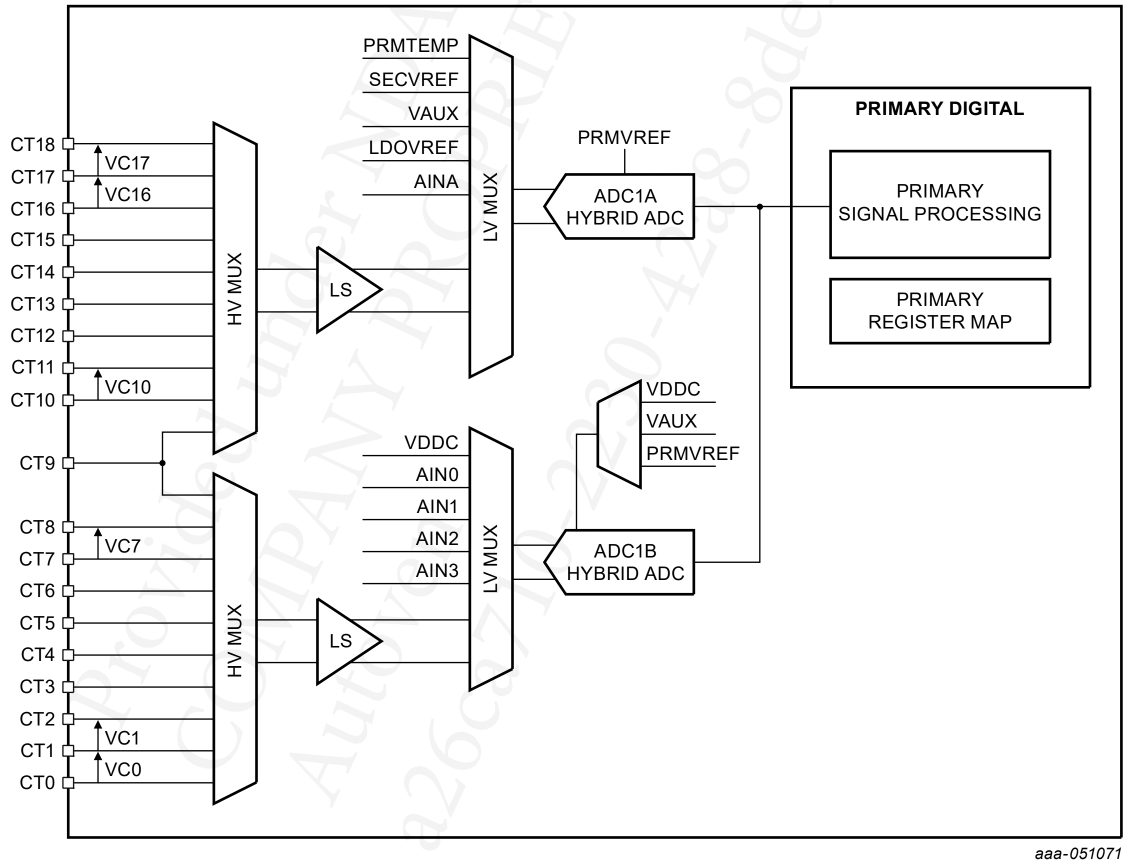


Figure 8. Functional diagram for primary measurement

7.4.1.2 Secondary measurement

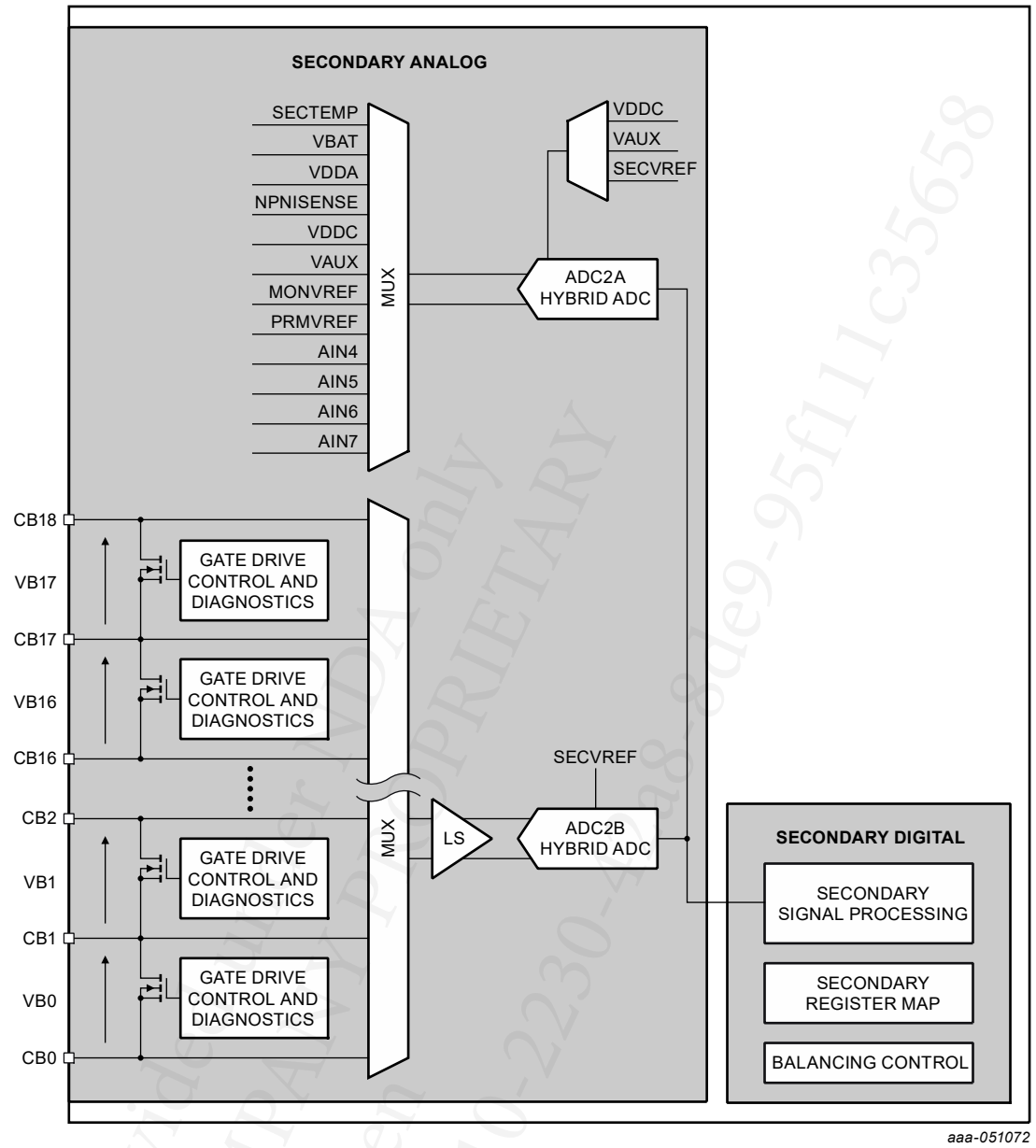


Figure 9. Functional diagram for secondary measurement

7.4.2 Functional description

The MC33774A offers a primary and a secondary measurement chain. The primary measurement chain is using the registers listed in the Primary Measurement Registers block. The secondary measurement chain is using the registers listed in the Secondary Measurement Registers block. The two register blocks are independent of each other. The two chains are independent from each other.

The event handling block monitors the synchronicity between the primary and secondary measurements. See Section 7.2 for details on the event handling block.

The registers block All Measurement Registers is writing simultaneously into the primary and the secondary measurement registers. This mechanism provides a comfortable way of ensuring the measurement configuration registers are set simultaneously for the primary and secondary measurement chain. A read back of the All Measurement Registers is not possible. The MC33774A returns 0000h as data in case one of the All Measurement Registers is read.

7.4.2.1 Measurement sequence

To achieve a high sampling rate, the primary measurement chain has two ADCs.

ADC1A measures:

- The primary IC temperature (PRMTEMP)
- The cell voltages 9 to 17 (VC9 to VC17)
- The auxiliary supply (VAUX)
- The voltage reference for the secondary measurement chain (SECVREF)
- The analog input AINA
- The voltage reference for the internal power supplies (LDOVREF)

ADC1B measures:

- The supply voltage for GPIO and the TPL interface (VDDC)
- The cell voltages 0 to 8 (VC0 to VC8)
- The analog inputs 0 to 3 (AIN0 to AIN3)

The primary measurement chain measures all signals cyclically. Once an ADC conversion is completed, the next signal is measured. After all 14 signals are measured once, the scan is completed and the next measurement cycle starts (Figure 10).

The secondary measurement chain has two ADCs.

ADC2A measures:

- The secondary IC temperature (SECTEMP)
- The battery supply (VBAT)
- The analog supply voltage (VDDA)
- The current in the external NPN (NPNISENSE)
- The supply voltage for GPIO and the TPL interface (VDDC)
- The auxiliary supply (VAUX)
- The reference for the primary measurement chain (PRMVREF)
- The reference (MONVREF)
- The analog inputs 4 to 7 (AIN4 to AIN7)

ADC2A measures cyclically, like ADC1A and ADC1B. After all 14 channels are measured once, the scan is completed and the next cycle starts.

ADC2B measures the cell voltages via the balancing pins (VB0 to VB17). As the cell balancing pins do not have an external antialiasing filter, ADC2B uses an internal antialiasing filter. The sampling scheme of the MC33774A implements appropriate settling times for the internal antialiasing filter. ADC2B measures one signal several times before it switches to the next signal. In a synchronous measurement cycle, the signal is measured for SECM_PER_CTRL.PERLEN × 14 × $t_{s(meas)}$. In a fast VB measurement cycle, each signal is measured for 28 × $t_{s(meas)}$.

Disabling measurements has no influence on the sequence for ADC1A, ADC1A, and ADC2A. ADC2B skips cells that are disabled.

Note: *PRMM_PER_CTRL.PERLEN and SECM_PER_CTRL.PERLEN must be set to the same value.*

Note: *SECVREF is available when secondary measurement is enabled. PRMVREF is available when primary measurement is enabled.*

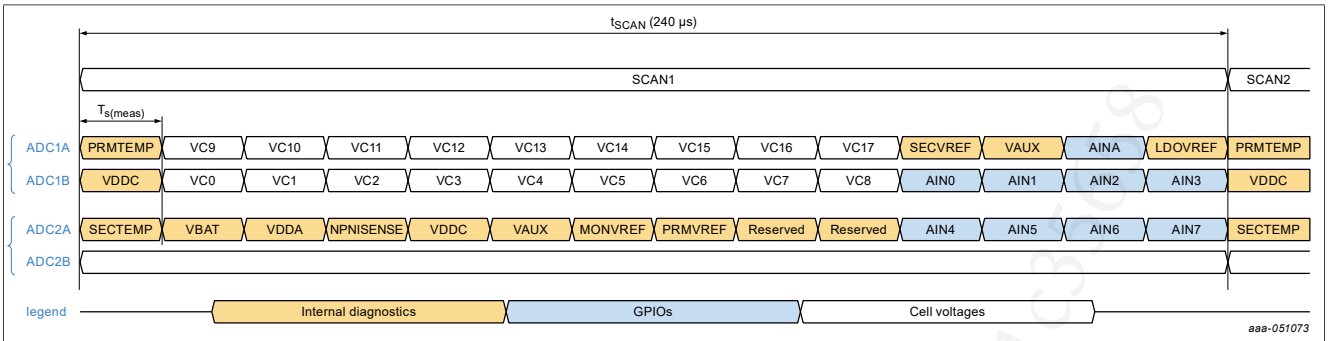


Figure 10. Measurement scan timing

The result of a single scan cycle as shown in Figure 10 is not directly available. The MC33774A makes the averaged value over multiple scan cycles available.

7.4.2.2 Measurement configuration

The registers PRMM_VC_CFG, PRMM_AIN_CFG, PRMM_VBUF_CFG, SECM_VBUF_CFG, SECM_VB_CFG, and SECM_AIN_CFG configure the measurements that are enabled. Disabling signals measured by ADC1A, ADC1B, or ADC2A does not influence the measurement timing. Signals measured by ADC2B are only measured when enabled. Disabled channels are skipped.

The registers PRMM_AIN_CFG and SECM_AIN_CFG contain the bitfields RATIOMETRICAIN0 to RATIOMETRICAIN7. These bits configure the measurement of the pins AIN0 to AIN7. Options are:

- Absolute regarding SECVREF or PRMVREF.
- Ratiometric to VAUX.
- Ratiometric to VDDC.

The bits FLTAPPINV in PRMM_AIN_CFG and SECM_AIN_CFG force an automatic invalidation of the application timed measurement results once a measurement fault (see Section 7.4.4) is detected.

7.4.2.3 Measurement configuration CRC

The MC33774A contains many configuration registers. For validation of the correctness of the configuration of the device, all configuration registers can be read. The MC33774A calculates a CRC across the content of the configuration registers. The MCU can use this CRC value to validate the integrity of the configuration. The CRC is recalculated whenever a register covered by the CRC is written or the CRC value is read.

PRMM_CFG_CRC contains the CRC value for the registers PRMM_CFG, PRMM_PER_CTRL, PRMM_VC_CFG0, PRMM_VC_CFG1, PRMM_AIN_CFG, PRMM_VBUF_CFG, PRMM_VC_OV_UV_CFG0, PRMM_VC_OV_UV_CFG1, PRMM_VC_OV_TH_CFG, PRMM_VC_UV0_TH_CFG, PRMM_VC_UV1_TH_CFG, PRMM_AIN0_OV_TH_CFG, PRMM_AIN1_OV_TH_CFG, PRMM_AIN2_OV_TH_CFG, PRMM_AIN3_OV_TH_CFG, PRMM_AINA_OV_TH_CFG, PRMM_AIN0_UV_TH_CFG, PRMM_AIN1_UV_TH_CFG, PRMM_AIN2_UV_TH_CFG, PRMM_AIN3_UV_TH_CFG, PRMM_AINA_UV_TH_CFG.

SECM_CFG_CRC contains the CRC value of the registers SECM_CFG, SECM_PER_CTRL, SECM_VB_CFG, SECM_AIN_CFG, and SECM_VBUF_CFG.

The used polynomial is: D175h (+1) = $X^{16} + X^{15} + X^{13} + X^9 + X^7 + X^6 + X^5 + X^3 + X^1 + 1$.

Note: *The CRC value depends on the configuration of the device and is therefore application dependent.*

Note: *The polynomial used here is different to the polynomial used for communication.*

Application usage: Check of integrity of the system configuration.

7.4.2.4 Undervoltage and overvoltage checks

The MC33774A performs an undervoltage and overvoltage check after each periodic measurement. For the cell terminals voltages, this check is optional. Register PRMM_VC_OV_UV_CFG configures which of the cell voltages take part in the undervoltage and overvoltage comparison. The register PRMM_VC_OV_TH_CFG contains the overvoltage threshold to be used for the comparison. The results of the comparisons are available in the PRMM_VC_OV_FLT_STAT register.

The register PRMM_VC_UV0_TH_CFG contains the threshold used for cell undervoltage-based balancing as described in the Section 7.5.3.2. The results of the comparison can be read in the PRMM_VC_UV0_FLT_STAT register.

The register PRMM_VC_UV1_TH_CFG contains the threshold used for global undervoltage-based balancing as described in the Section 7.5.3.3. The results of the comparison can be read in the PRMM_VC_UV1_FLT_STAT register.

The registers PRMM_AIN0_OV_TH_CFG to PRMM_AIN3_OV_TH_CFG and PRMM_AINA_OV_TH_CFG and PRMM_AIN0_UV_TH_CFG to PRMM_AIN3_UV_TH_CFG and PRMM_AINA_UV_TH_CFG contain the undervoltage and overvoltage thresholds for AIN0 to AIN3 and AINA. The results of the comparison can be read in the PRMM_AIN_OV_FLT_STAT and PRMM_AIN_UV_FLT_STAT registers. The thresholds set by these registers are also used for the Section 7.5.3.6 .

The MC33774A performs the undervoltage and overvoltage comparison together. In some cases, it can be of interest to compare only to one of the thresholds. Configuring not used thresholds to the invalid code (8000h) prevents setting the corresponding undervoltage or overvoltage bits.

7.4.2.5 Measurement data format

The MC33774A provides the measurement results as 16-bit two's complement. Code 8000h represents invalid data (see Section 7.4.4). Clamping is signaled when the measured value is out of the measurement range of the MC33774A. Code 7FFFh indicates the value is clamped positively. Code 8001h indicates a negative clamping.

Measurements that have only a positive measurement range, for instance all GPIO measurements, are still provided as 16-bit two's complement.

Table 14. Measurement data representation

Code	Value	Example for PRMM_APP_VC0
7FFFh	Positive clamped value	Positive clamping occurred; cell voltage above measurement range
7FFEh	maximum positive value = 32766[1]	32766 × LSB × $V_{meas(res)}$ = 5.05 V
0001h	+1	+1 LSB × $V_{meas(res)}$ = 154 µV
0000h	0	0 V
FFFFh	−1	−1 LSB × $V_{meas(res)}$ = −154 µV
8002h	Maximum negative value = −32765[1]	−32765 × LSB × $V_{meas(res)}$ = −5.05 V
8001h	Negative clamped value	Negative clamping occurred; cell voltage below measurement range
8000h	Invalid	Measurement is invalidated, for example, fewer than 16 scans

[1] Saturation may occur before maximum value is reached (see Section 7.4.2.6).

7.4.2.6 Measurement saturation, resolution, and references

Table 15 lists the measurement location and the reference potential for the individual measurements of the MC33774A . The table also lists the resolution of the measurements and, when applicable, the saturation values. If a single ADC conversion is outside the saturation limits, the measurement result register for this measurement indicates clamping. If the value is below the lower saturation limit, the negative clamping value (8001h) is used. If the value is above the upper saturation limit, the positive clamping value (7FFFh) is used.

Table 15. Measurements and references

Measurement	Measurement location	Reference potential	Conversion formula (typ.)	Saturation
Cell terminal measurement VC(X); X = 0 to 17	CT(X+1)	CT(X)	154 µV × result register value	Positive saturation at 7FF7h Negative saturation at 8008h
Cell voltage at balancing pins VB(X); X = 0 to 17	CB(X+1)	CB(X)	154 µV × result register value	Positive saturation at 7FF7h negative saturation at B2D9h
AIN(X); X = 0 to 7, A	AIN(X)	AINX_VSSA	154 µV × result register value (for absolute measurement) 3.05176 m% × result register value (for ratiometric measurement)	positive saturation at 7FF7h Negative saturation at FEEEh
VDDA	VDDA	VSSA	154 µV × result register value	Not applicable
VBAT	VBAT	VSSA	3.128 mV × result register value	Not applicable
PRMTEMP	Internal	Internal	32.4 mK × result register value (to get result in Kelvin) 32.4 mK × result register value - 273.15 (to get result in °C)	Not applicable
SECTEMP	Internal	Internal	32.4 mK × result register value (to get result in Kelvin) 32.4 mK × result register value - 273.15 (to get result in °C)	Not applicable
VAUX	VAUX	ADC1A: AINX_GND ADC2A: VSSA	308 µV × result register value (for absolute measurement)	Not applicable
VDDC	VDDC	ADC1A: AINX_GND ADC2A: VSSA	308 µV × result register value	Not applicable
NPNISENSE	VDDC_IMON	VDDC	7.69 µV × result register value	Not applicable

Table 15. Measurements and references*...continued*

Measurement	Measurement location	Reference potential	Conversion formula (typ.)	Saturation
PRMVREF	Internal	Internal	38.452 µV × result register value	Not applicable
SECVREF	Internal	Internal	38.452 µV × result register value-	Not applicable

7.4.3 Measurement modes

The MC33774A allows four main measurement modes:

- Periodic measurements
- Application timed continuous measurements
- Synchronized measurements of VC and VB terminals
- Fast VB measurements

The synchronized and fast VB measurements are mutually exclusive, all measurements can run in parallel with each other. When measurements run in parallel, one ADC conversion result is used for all active measurement modes. Figure 11 shows the measurement location for the cell voltages and the result registers where the cell voltage data are stored. Figure 11 also shows the conditions that trigger the storing of the ADC result to the result register sets. Based on this, one ADC conversion result for a cell terminal voltage can be used for the periodic, the application and the synchronous measurements. Not all inputs have all register sets. For instance the cell balancing voltages have only a set for the synchronous results.

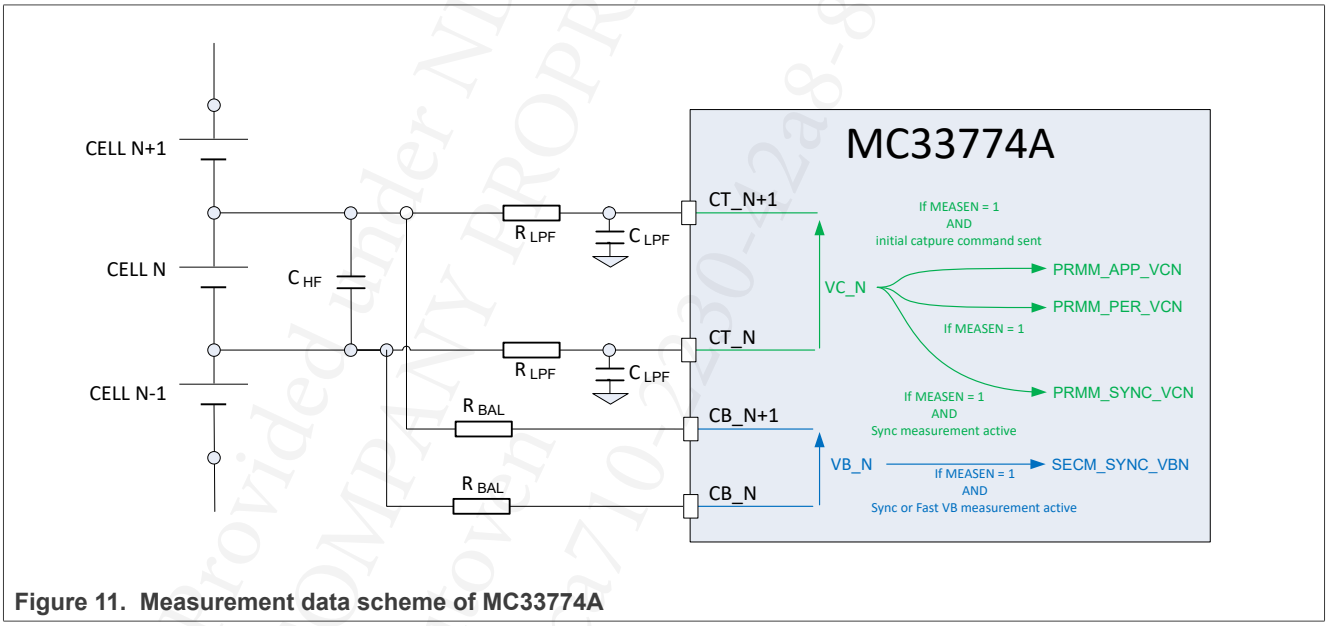


Figure 11. Measurement data scheme of MC33774A

Table 16 shows the key characteristics of the measurement modes.

Table 16. Overview of measurement modes

Measurement	Measurement frequency	Averaging interval	Result update	Start condition	Applies to
Periodic	$f_{PER} = \frac{1}{14 \times t_{s(meas)}} = \text{approx. } 4.2 \text{ kHz}$	defined by bit field PERLEN (primary: 16 to 511 measurements)	periodically depending on PERCTRL	continuous measurement (as soon as MEASEN is set 1)	ADC1A, ADC1B, and ADC2A
Application timed continuous	$f_{APP} = \frac{1}{14 \times t_{s(meas)}} = \text{approx. } 4.2 \text{ kHz}$	defined by capture command (16 to 65535 measurements)	after capture command (PRMM_APP_CTRL[5:0] and SECM_APP_CTRL[9:6])	continuous measurement (as soon as MEASEN is set 1 and first capture command for the signal is received)	ADC1A, ADC1B, and ADC2A
Synchronized	$f_{SYNC\_PRMM} = \frac{1}{14 \times t_{s(meas)}} = \text{approx. } 4.2 \text{ kHz}$ $f_{SYNC\_SECM} = \frac{1}{t_{s(meas)}} = \text{approx. } 59 \text{ kHz}$	defined by bit field PERLEN (primary: 16 to 511 measurements) (secondary: must use same time interval as primary)	after measurement is finished	start of a synchronous measurement cycle[1]	ADC1A, ADC1B, ADC2A, and ADC2B
Fast VB	$f_{fast\ VB} = \frac{1}{t_{s(meas)}} = \text{approx. } 59 \text{ kHz}$	$28 \times t_{s(meas)}$	after measurement is finished	start of a fast VB measurement (SECM_SYNC_CTRL.FASTFB)	ADC2B

[1] Set PRMM_SYNC_CTRL.SYNCCYC and SECM_SYNC_CTRL.SYNCCYC simultaneously via writing to ALLM_SYNC_CTRL.SYNCCYC.

7.4.3.1 Periodic measurement

In Periodic Measurement mode, a configurable number of samples is taken and an averaged result is stored. The number of measurement cycles is defined in PRMM_PER_CTRL.PERLEN and SECM_PER_CTRL.PERLEN. Once the device has performed the configured number of measurements for a signal, the result is checked for undervoltage or overvoltage conditions (see Undervoltage and overvoltage checks). Once the device has completed the configured number of the measurements for all signals, the averaged results are stored in the periodic measurement result registers. Based on this implementation, the undervoltage and overvoltage flags are updated before the measurement results are available.

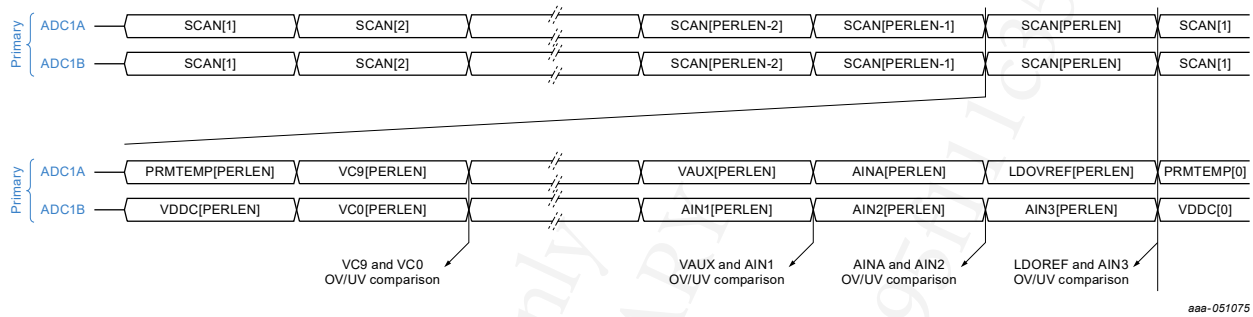


Figure 12. Example: Periodic measurement cycle with PERLEN cycles

The update of the periodic result registers (PRMM_PER_NUM to PRMM_PER_ LDOVREF and SECM_PER_NUM to SECM_PER_NPNISENSE) is done based on the bit field PRMM_PER_CTRL.PERCTRL and SECM_PER_CTRL.PERCTRL. When PERCTRL is set to auto, the result registers contain the latest generated results. Setting PERCTRL to ONCE initiates one update. After the update, the result registers are frozen. This mechanism allows reading of time aligned measurement data across multiple devices. PRMM_PER_NUM and SECM_PER_NUM contain the number of the periodic cycle in which the primary periodic results have been created, the other registers contain the measurement results.

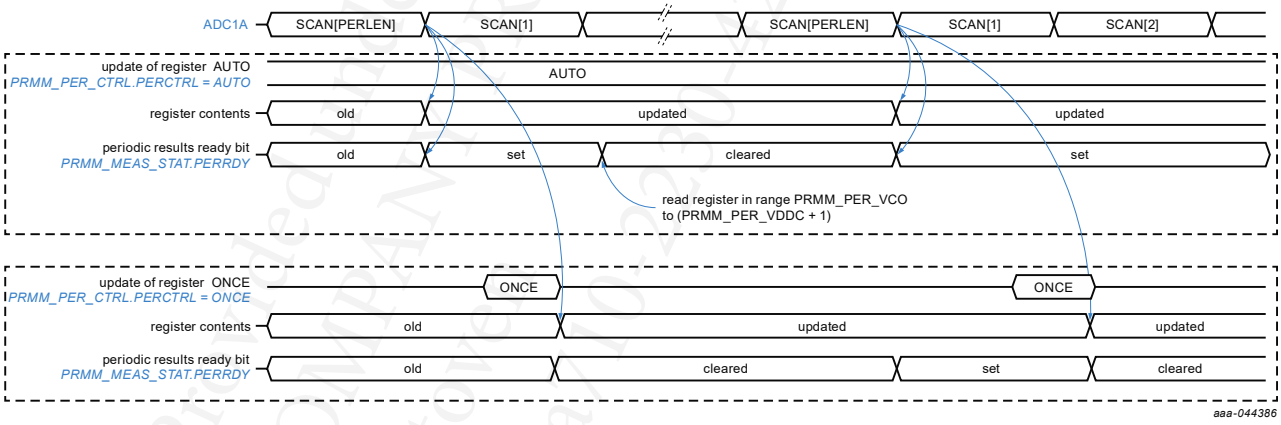


Figure 13. Update of periodic result register based on PERCTRL

Application usage: Measurement over a fixed time period; used for all undervoltage and overvoltage checks.

Note: *PRMM_PER_CTRL and SECM_PER_CTRL must have the same setting. ALLM_PER_CTRL sets PRMM_PER_CTRL and SECM_PER_CTRL simultaneously.*

7.4.3.2 Application timed measurement

The application timed measurement averages the measurement results between two capture commands. The time between the capture commands is up to the application, but must allow minimum 16 scan cycles and maximum 65534 scan cycles. If a capture is shorter than 16 measurements or longer than 65535 measurements, the results registers are set to invalid. A capture command means writing of PRMM_APP_CTRL[5:0] and/or SECM_APP_CTRL[9:6] with logic 1. The measurement results are made available in the application result registers (PRMM_APP_VC_CNT to PRMM_APP_AIN3 and SECM_APP_AIN4 to SECM_APP_AIN7). Register PRMM_APP_VC_CNT contains the number of cell voltage measurements performed within the last VC capture cycle. The other register contains the measured voltages. Bits PRMM_MEAS_STAT[5:0] and SECM_MEAS_STAT[3:0] signal that more than 16 measurements have been performed, which indicates that a new capture can be initiated.

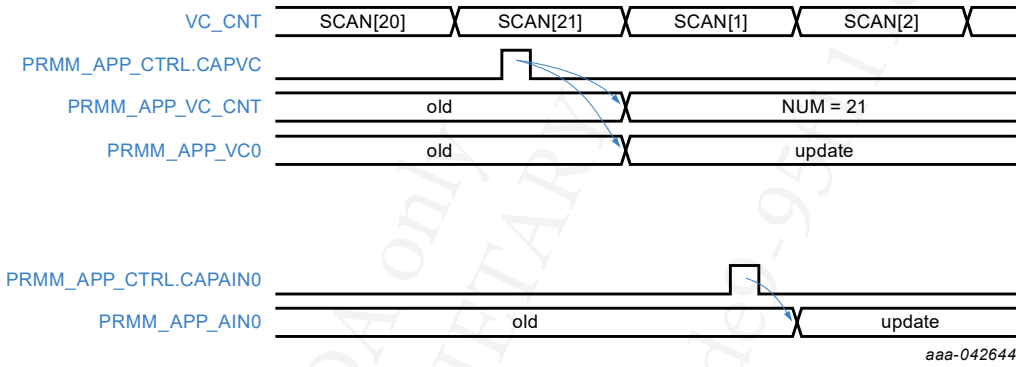


Figure 14. Example: Application timed measurement

Application usage: Measurement over an MCU controlled time period.

7.4.3.3 Synchronized measurement

The synchronized measurement is a measurement of the primary and secondary voltages. The synchronized measurement is initiated by setting the bits PRMM_SYNC_CTRL.SYNCCYC and SECM_SYNC_CTRL.SYNCCYC. To ensure synchronous measurements, the bits must be set simultaneously. The bit ALLM_SYNC_CTRL.SYNCCYC can be used to set the PRMM_SYNC_CTRL.SYNCCYC and SECM_SYNC_CTRL.SYNCCYC simultaneously.

The synchronous measurement cycle starts with the next periodic measurement. ADC2B measures the cells continuously until the number of samples for one period is reached. ADC1A and ADC1B operate as usual. When ADC2B has completed the measurement for VB17, all the synchronous measurement result registers are updated. The secondary measurement registers are populated with the average results of ADC2B for the individual cells. The primary measurement registers are populated with the average results of ADC1A/ADC1B while ADC2B has measured the same cell. The bits PRMM_MEAS_STAT.SYNCRDY and SECM_MEAS_STAT.SYNCRDY signal the completion of the measurement.

The results of the synchronized measurement are available in the registers PRMM_SYNC_NUM to PRMM_SYNC_VC17 and SECM_SYNC_NUM to SECM_SYNC_VB17. PRMM_SYNC_NUM and SECM_SYNC_NUM contain the number of the synchronous cycle in which the synchronous results have been created, the other registers contain the measured voltages.

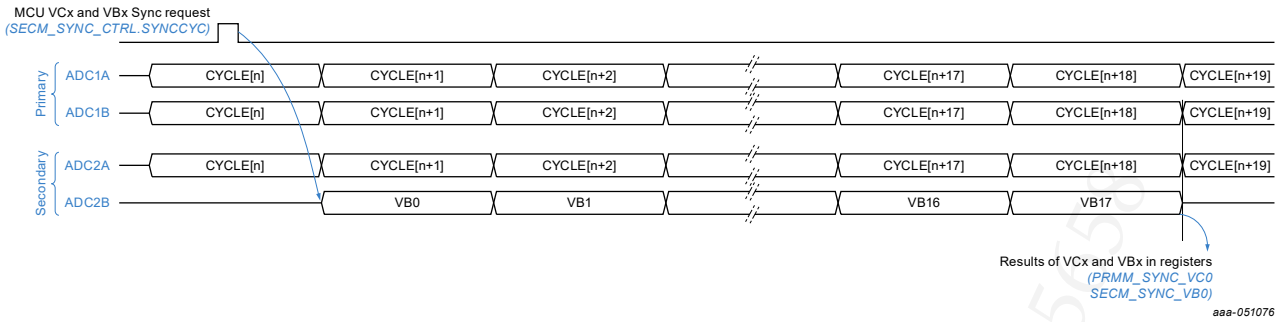


Figure 15. Synchronized measurement cycle with 18 cells active

ADC2B skips cells that are disabled during a synchronized or fast VB measurement.

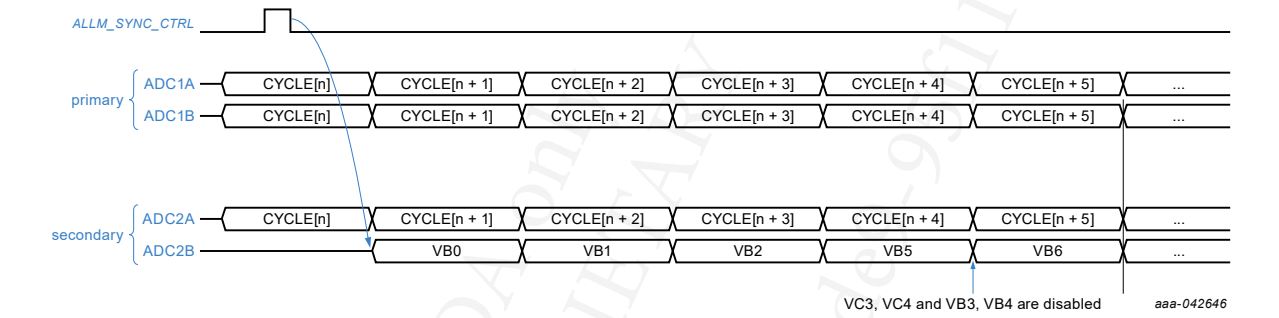


Figure 16. Synchronized measurement cycle with cell 3 and cell 4 disabled

Application usage: Independent time synchronized measurement of the cell voltage.

7.4.3.4 Fast VB measurement

The fast VB measurement is a measurement of the VBx voltages. The fast VB measurement is initiated by setting the bit SECM_SYNC_CTRL.FASTVB. ADC2B measures each enabled VBx voltage for 28 × $t_{s(meas)}$. A fast VB measurement is started latest with the second scan cycle after the bit ALLM_SYNC_CTRL.FASTVB is set. The bit SECM_MEAS_STAT.FASTVBRDY signals the completion of the measurement. The averaged results for each channel are available in the registers SECM_SYNC_VB0 to SECM_SYNC_VB17.

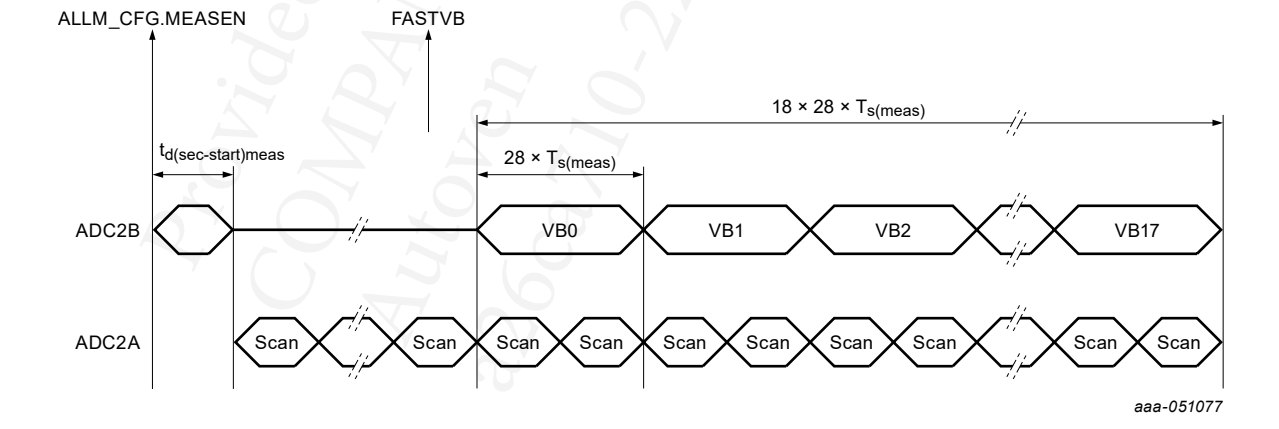


Figure 17. Fast VB measurement cycle

Application usage: Check of the connectivity of VB terminals and open load detection.

7.4.4 Invalidation of measurement results

The MC33774A invalidates the measurement results in order to avoid usage of old or corrupted data. The code 8000h represents invalid data (see Measurement data format). Table 17 gives an overview of the events and the result registers that are invalidated.

Table 17. Invalidation of measurement results

Event	Invalidated results	Comment
Transition into Active mode.	Primary and secondary measurement results.	
Read of a measurement register.	Register that was read.	The result is always invalidated, independently, of the communication success of the register to the MCU.
Faults leading to result invalidation	Secondary synchronous measurement results (registers SECM_SYNC_VB0 to SECM_SYNC_VB17).	All primary results, the secondary periodic, and secondary application results are not invalidated.
Faults leading to result invalidation with PRMM_AIN_CFG.FLTAPPINV set to 1.	Application measurement results of AIN0 to AIN3 and AINA (registers PRMM_APP_AIN0 to PRMM_APP_AIN3 and PRMM_APP_AINA).	Periodic results are not invalidated.
Faults leading to result invalidation with SECM_AIN_CFG.FLTAPPINV set to 1.	Application measurement results of AIN4 to AIN7 (registers SECM_APP_AIN4 to SECM_APP_AIN7).	Periodic results are not invalidated.
Receiving of a capture command before 16 scans are performed.	Application measurements with fewer than 16 scans.	PRMM_APP_VC_CNT shows the actual number of scans performed.
Receiving of a capture command after 65535 scans are performed.	Application measurements with more than 65535 scans.	PRMM_APP_VC_CNT shows FFFFh.
Disabling of the measurement.	Primary and secondary measurement results.	

There are various sources that can lead to an erratic measurement. The fault events leading to a result invalidation are shown in Figure 18.

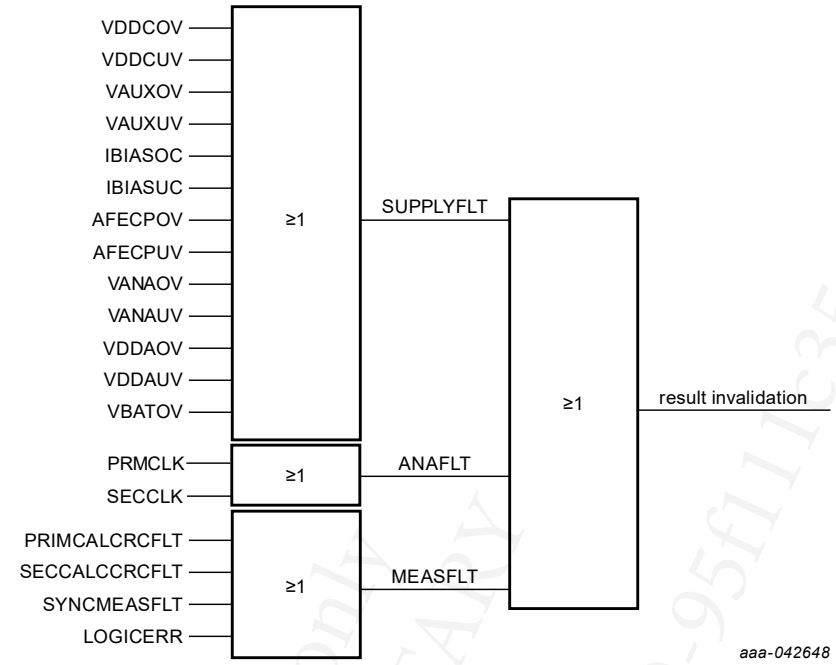


Figure 18. Result invalidation event

Note: *Figure 18 shows only the supply faults that can cause an invalidation of the results. All faults leading to a supply fault are shown in Table 9.*

Note: *VAUXUV, VAUXOV, VDDCUV, and VDDCOV only cause an invalidation of the results if they are used as references for the measurement.*

7.4.5 Pausing of balancing

In a typical battery management system (BMS), each battery cell terminal is connected with a single wire to the application circuit of the MC33774A (see Figure 54). An active cell balancing leads to voltage drop at the connectors and wirings. The voltage drop creates an undesired offset in the voltages measured by the MC33774A. To allow an accurate measurement, the MC33774A provides the option to pause the balancing. To allow the external filters to settle to their steady state value, the measurement after start of a pause can be delayed.

The bit fields PRMM_CFG.BALPAUSELEN and SECM_CFG.BALPAUSELEN control the length of the pause before the measurement is started. In order to avoid generation of a SYNCMEASFLT, PRMM_CFG.BALPAUSELEN, and SECM_CFG.BALPAUSELEN must be set to the same value.

The bits PRMM_CFG.BALPAUSECYCMODEN and SECM_CFG.BALPAUSECYCMODEN force a balancing pause during the measurement and a pause after transitioning from Sleep to Cyclic mode and the start of the first measurement in Cyclic mode.

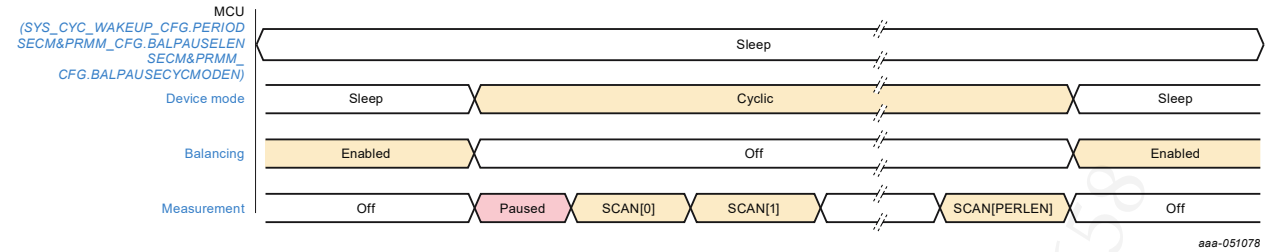


Figure 19. Pause when entering Cyclic mode

The bits PRMM_SYNC_CTRL.PAUSEBAL and SECM_SYNC_CTRL.PAUSEBAL allow forcing a pause for a synchronized measurement (Section 7.4.3.3) or a Fast VB measurement (Section 7.4.3.4).

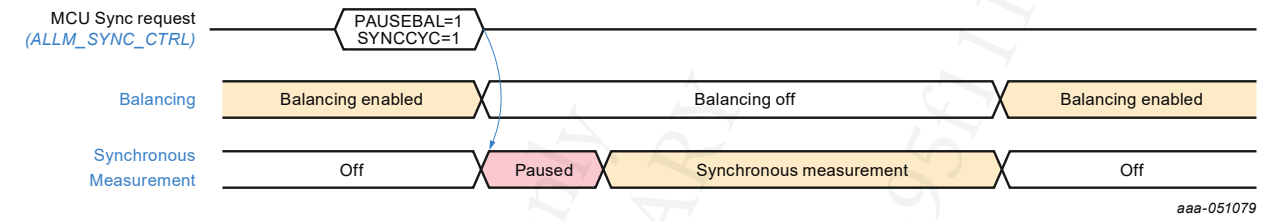


Figure 20. Pause when executing a synchronous measurement

The bits PRMM_APP_CTRL.PAUSEBAL and SECM_SYNC_APP_CTRL.PAUSEBAL allow forcing a pause for an application timed measurement (Section 7.4.3.2).

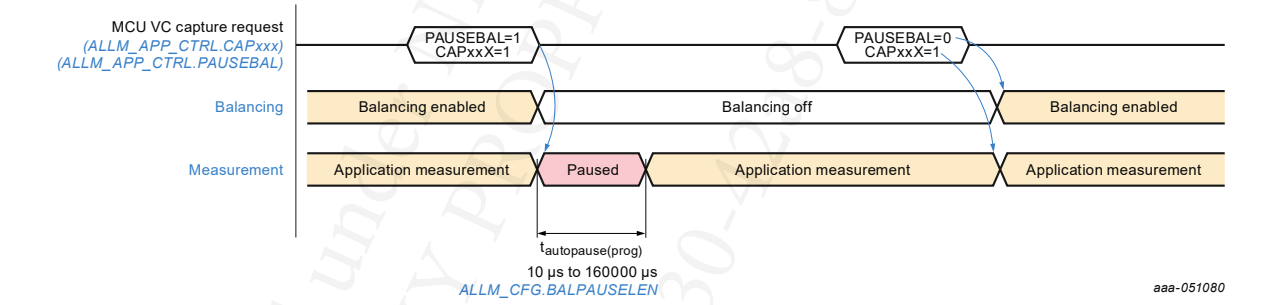


Figure 21. Pause when executing an application timed measurement

In case one or more measurements with balancing are triggered, the IC keeps the balancing paused until the last measurement sequence is completed. If a different measurement pauses the balancing already, the new measurement is directly started without a pause.

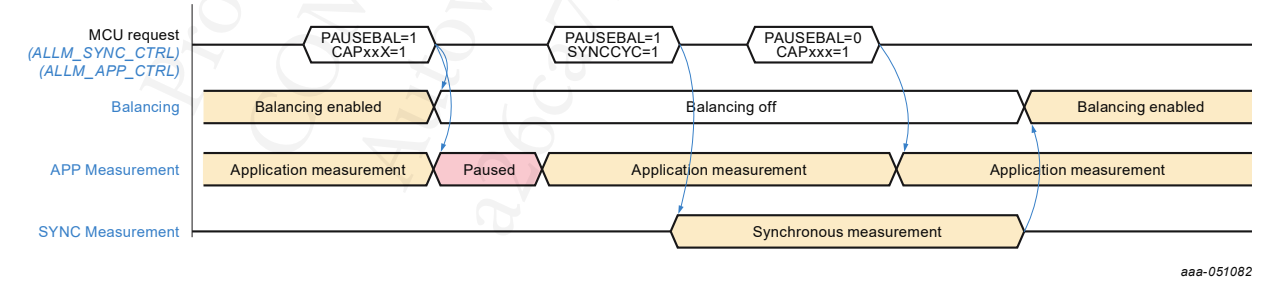


Figure 22. Multiple pause sources

Note: *Keep the configuration for primary and secondary measurements identical to avoid triggering a SYNCMEASFLT. The usage of the ALLM_xxx registers ensures primary and secondary measurements are set identical.*

7.4.6 Registers for primary measurement

All registers related to the primary measurement are listed here. Details to the registers and the bitfields are explained in the register map chapter.

Table 18. Register overview: Primary_Measurement_Registers

Address	Name	Access	Reset	Description
1800h	PRMM_CFG	R/W	0h	general measurement control
1801h	PRMM_APP_CTRL	R/W	7C00h	application measurement control
1802h	PRMM_PER_CTRL	R/W	10h	periodic measurement control
1803h	PRMM_SYNC_CTRL	W	0h	synchronous measurement control
1808h	PRMM_VC_CFG0	R/W	0h	cell voltage measurement enable
1809h	PRMM_VC_CFG1	R/W	0h	cell voltage measurement enable
180Ah	PRMM_AIN_CFG	R/W	20h	AINx measurement enables
180Bh	PRMM_AIN_OL_CFG	R/W	0h	AINx open-load detection enable
180Ch	PRMM_VBUF_CFG	R/W	3h	voltage buffer enable
1810h	PRMM_VC_OV_UV_CFG0	R/W	0h	cell voltage over-voltage and under-voltage check enable
1811h	PRMM_VC_OV_UV_CFG1	R/W	0h	cell voltage over-voltage and under-voltage check enable
1812h	PRMM_VC_OV_TH_CFG	R/W	7FFFh	upper comparator limit for VC0 to VC17
1813h	PRMM_VC_UV0_TH_CFG	R/W	0h	lower comparator limit 0 for VC0 to VC17
1814h	PRMM_VC_UV1_TH_CFG	R/W	0h	lower comparator limit 1 for VC0 to VC17
1815h	PRMM_AIN0_OV_TH_CFG	R/W	7FFFh	upper comparator limit for AIN0
1816h	PRMM_AIN1_OV_TH_CFG	R/W	7FFFh	upper comparator limit for AIN1
1817h	PRMM_AIN2_OV_TH_CFG	R/W	7FFFh	upper comparator limit for AIN2
1818h	PRMM_AIN3_OV_TH_CFG	R/W	7FFFh	upper comparator limit for AIN3
1819h	PRMM_AINA_OV_TH_CFG	R/W	7FFFh	upper comparator limit for AINA
181Ah	PRMM_AIN0_UV_TH_CFG	R/W	8001h	lower comparator limit for AIN0
181Bh	PRMM_AIN1_UV_TH_CFG	R/W	8001h	lower comparator limit for AIN1
181Ch	PRMM_AIN2_UV_TH_CFG	R/W	8001h	lower comparator limit for AIN2
181Dh	PRMM_AIN3_UV_TH_CFG	R/W	8001h	lower comparator limit for AIN3
181Eh	PRMM_AINA_UV_TH_CFG	R/W	8001h	lower comparator limit for AINA
1820h	PRMM_CAL_CRC	R/W	0h	CRC over calibration data
1821h	PRMM_CFG_CRC	R	0h	CRC over configuration values
1822h	PRMM_VC_OV_FLT_STAT0	R	0h	cell voltage over-voltage status
1823h	PRMM_VC_OV_FLT_STAT1	R	0h	cell voltage over-voltage status
1824h	PRMM_VC_UV0_FLT_STAT0	R	0h	cell voltage under-voltage status regarding limit 0
1825h	PRMM_VC_UV0_FLT_STAT1	R	0h	cell voltage under-voltage status regarding limit 0
1826h	PRMM_VC_UV1_FLT_STAT0	R	0h	cell voltage under-voltage status regarding limit 1
1827h	PRMM_VC_UV1_FLT_STAT1	R	0h	cell voltage under-voltage status regarding limit 1

Table 18. Register overview: Primary_Measurement_Registers...*continued*

Address	Name	Access	Reset	Description
1828h	PRMM_AIN_OV_FLT_STAT	R	0h	AINx over-voltage status
1829h	PRMM_AIN_UV_FLT_STAT	R	0h	AINx under-voltage status
183Eh	PRMM_MEAS_STAT	R	0h	measurement status
183Fh	PRMM_APP_VC_CNT	R	0h	application measurement VC sample count number
1840h	PRMM_APP_VC0	R	8000h	application measurement result cell 0
1841h	PRMM_APP_VC1	R	8000h	application measurement result cell 1
1842h	PRMM_APP_VC2	R	8000h	application measurement result cell 2
1843h	PRMM_APP_VC3	R	8000h	application measurement result cell 3
1844h	PRMM_APP_VC4	R	8000h	application measurement result cell 4
1845h	PRMM_APP_VC5	R	8000h	application measurement result cell 5
1846h	PRMM_APP_VC6	R	8000h	application measurement result cell 6
1847h	PRMM_APP_VC7	R	8000h	application measurement result cell 7
1848h	PRMM_APP_VC8	R	8000h	application measurement result cell 8
1849h	PRMM_APP_VC9	R	8000h	application measurement result cell 9
184Ah	PRMM_APP_VC10	R	8000h	application measurement result cell 10
184Bh	PRMM_APP_VC11	R	8000h	application measurement result cell 11
184Ch	PRMM_APP_VC12	R	8000h	application measurement result cell 12
184Dh	PRMM_APP_VC13	R	8000h	application measurement result cell 13
184Eh	PRMM_APP_VC14	R	8000h	application measurement result cell 14
184Fh	PRMM_APP_VC15	R	8000h	application measurement result cell 15
1850h	PRMM_APP_VC16	R	8000h	application measurement result cell 16
1851h	PRMM_APP_VC17	R	8000h	application measurement result cell 17
1852h	PRMM_APP_AINA	R	8000h	application measurement result AINA
1853h	PRMM_APP_AIN0	R	8000h	application measurement result AIN0
1854h	PRMM_APP_AIN1	R	8000h	application measurement result AIN1
1855h	PRMM_APP_AIN2	R	8000h	application measurement result AIN2
1856h	PRMM_APP_AIN3	R	8000h	application measurement result AIN3
185Fh	PRMM_PER_NUM	R	0h	measurement period number of the primary periodic results
1860h	PRMM_PER_VC0	R	8000h	periodic measurement result cell 0
1861h	PRMM_PER_VC1	R	8000h	periodic measurement result cell 1
1862h	PRMM_PER_VC2	R	8000h	periodic measurement result cell 2
1863h	PRMM_PER_VC3	R	8000h	periodic measurement result cell 3
1864h	PRMM_PER_VC4	R	8000h	periodic measurement result cell 4
1865h	PRMM_PER_VC5	R	8000h	periodic measurement result cell 5
1866h	PRMM_PER_VC6	R	8000h	periodic measurement result cell 6
1867h	PRMM_PER_VC7	R	8000h	periodic measurement result cell 7
1868h	PRMM_PER_VC8	R	8000h	periodic measurement result cell 8
1869h	PRMM_PER_VC9	R	8000h	periodic measurement result cell 9
186Ah	PRMM_PER_VC10	R	8000h	periodic measurement result cell 10

Table 18. Register overview: Primary_Measurement_Registers*...continued*

Address	Name	Access	Reset	Description
186Bh	PRMM_PER_VC11	R	8000h	periodic measurement result cell 11
186Ch	PRMM_PER_VC12	R	8000h	periodic measurement result cell 12
186Dh	PRMM_PER_VC13	R	8000h	periodic measurement result cell 13
186Eh	PRMM_PER_VC14	R	8000h	periodic measurement result cell 14
186Fh	PRMM_PER_VC15	R	8000h	periodic measurement result cell 15
1870h	PRMM_PER_VC16	R	8000h	periodic measurement result cell 16
1871h	PRMM_PER_VC17	R	8000h	periodic measurement result cell 17
1872h	PRMM_PER_AINA	R	8000h	periodic measurement result AINA
1873h	PRMM_PER_AIN0	R	8000h	periodic measurement result AIN0
1874h	PRMM_PER_AIN1	R	8000h	periodic measurement result AIN1
1875h	PRMM_PER_AIN2	R	8000h	periodic measurement result AIN2
1876h	PRMM_PER_AIN3	R	8000h	periodic measurement result AIN3
1877h	PRMM_PER_PRMTEMP	R	8000h	periodic measurement result primary device temperature
1878h	PRMM_PER_SECVREF	R	8000h	periodic measurement result secondary voltage reference
1879h	PRMM_PER_VAUX	R	8000h	periodic measurement result auxiliary supply voltage
187Ah	PRMM_PER_VDDC	R	8000h	periodic measurement result VDDC
187Fh	PRMM_SYNC_NUM	R	0h	measurement period number of the synchronous results.
1880h	PRMM_SYNC_VC0	R	8000h	synchronous measurement result cell 0
1881h	PRMM_SYNC_VC1	R	8000h	synchronous measurement result cell 1
1882h	PRMM_SYNC_VC2	R	8000h	synchronous measurement result cell 2
1883h	PRMM_SYNC_VC3	R	8000h	synchronous measurement result cell 3
1884h	PRMM_SYNC_VC4	R	8000h	synchronous measurement result cell 4
1885h	PRMM_SYNC_VC5	R	8000h	synchronous measurement result cell 5
1886h	PRMM_SYNC_VC6	R	8000h	synchronous measurement result cell 6
1887h	PRMM_SYNC_VC7	R	8000h	synchronous measurement result cell 7
1888h	PRMM_SYNC_VC8	R	8000h	synchronous measurement result cell 8
1889h	PRMM_SYNC_VC9	R	8000h	synchronous measurement result cell 9
188Ah	PRMM_SYNC_VC10	R	8000h	synchronous measurement result cell 10
188Bh	PRMM_SYNC_VC11	R	8000h	synchronous measurement result cell 11
188Ch	PRMM_SYNC_VC12	R	8000h	synchronous measurement result cell 12
188Dh	PRMM_SYNC_VC13	R	8000h	synchronous measurement result cell 13
188Eh	PRMM_SYNC_VC14	R	8000h	synchronous measurement result cell 14
188Fh	PRMM_SYNC_VC15	R	8000h	synchronous measurement result cell 15
1890h	PRMM_SYNC_VC16	R	8000h	synchronous measurement result cell 16
1891h	PRMM_SYNC_VC17	R	8000h	synchronous measurement result cell 17

7.4.7 Registers for secondary measurement

All registers related to the secondary measurement are listed here. Details to the registers and the bitfields are explained in the register map chapter.

Table 19. Register overview: Secondary_Measurement_Registers

Address	Name	Access	Reset	Description
1C00h	SECM_CFG	R/W	0h	general measurement control
1C01h	SECM_APP_CTRL	W	0h	application measurement control
1C02h	SECM_PER_CTRL	R/W	10h	periodic measurement control
1C03h	SECM_SYNC_CTRL	R/W	7C00h	synchronous measurement control
1C08h	SECM_VB_CFG0	R/W	0h	balance voltage measurement enable
1C09h	SECM_VB_CFG1	R/W	0h	balance voltage measurement enable
1C0Ah	SECM_AIN_CFG	R/W	80h	measurement enables for extra channel
1C0Bh	SECM_AIN_OL_CFG	R/W	0h	AINx open-load detection enable
1C0Ch	SECM_VBUF_CFG	R/W	3h	voltage buffer enable
1C20h	SECM_CAL_CRC	R/W	0h	CRC over calibration data
1C21h	SECM_CFG_CRC	R	0h	CRC over configuration values
1C3Eh	SECM_MEAS_STAT	R	0h	measurement status
1C53h	SECM_APP_AIN4	R	8000h	application measurement result AIN4
1C54h	SECM_APP_AIN5	R	8000h	application measurement result AIN5
1C55h	SECM_APP_AIN6	R	8000h	application measurement result AIN6
1C56h	SECM_APP_AIN7	R	8000h	application measurement result AIN7
1C5Fh	SECM_PER_NUM	R	0h	measurement period number of the secondary periodic results
1C73h	SECM_PER_AIN4	R	8000h	periodic measurement result AIN4
1C74h	SECM_PER_AIN5	R	8000h	periodic measurement result AIN5
1C75h	SECM_PER_AIN6	R	8000h	periodic measurement result AIN6
1C76h	SECM_PER_AIN7	R	8000h	periodic measurement result AIN7
1C77h	SECM_PER_SECTEMP	R	8000h	periodic measurement result secondary device temperature
1C78h	SECM_PER_PRMVREF	R	8000h	periodic measurement result primary voltage reference
1C79h	SECM_PER_VAUX	R	8000h	periodic measurement result auxiliary supply voltage
1C7Ah	SECM_PER_VBAT	R	8000h	periodic measurement result VBAT
1C7Bh	SECM_PER_VDDA	R	8000h	periodic measurement result VDDA
1C7Ch	SECM_PER_VDDC	R	8000h	periodic measurement result VDDC
1C7Eh	SECM_PER_NPNISENSE	R	8000h	periodic measurement result NPN current sensor
1C7Fh	SECM_SYNC_NUM	R	0h	measurement number of the secondary synchronous results
1C80h	SECM_SYNC_VB0	R	8000h	synchronous measurement result from balancing pins cell 0.
1C81h	SECM_SYNC_VB1	R	8000h	synchronous measurement result from balancing pins cell 1

Table 19. Register overview: Secondary_Measurement_Registers...*continued*

Address	Name	Access	Reset	Description
1C82h	SECM_SYNC_VB2	R	8000h	synchronous measurement result from balancing pins cell 2
1C83h	SECM_SYNC_VB3	R	8000h	synchronous measurement result from balancing pins cell 3
1C84h	SECM_SYNC_VB4	R	8000h	synchronous measurement result from balancing pins cell 4
1C85h	SECM_SYNC_VB5	R	8000h	synchronous measurement result from balancing pins cell 5
1C86h	SECM_SYNC_VB6	R	8000h	synchronous measurement result from balancing pins cell 6
1C87h	SECM_SYNC_VB7	R	8000h	synchronous measurement result from balancing pins cell 7
1C88h	SECM_SYNC_VB8	R	8000h	synchronous measurement result from balancing pins cell 8
1C89h	SECM_SYNC_VB9	R	8000h	synchronous measurement result from balancing pins cell 9
1C8Ah	SECM_SYNC_VB10	R	8000h	synchronous measurement result from balancing pins cell 10
1C8Bh	SECM_SYNC_VB11	R	8000h	synchronous measurement result from balancing pins cell 11
1C8Ch	SECM_SYNC_VB12	R	8000h	synchronous measurement result from balancing pins cell 12
1C8Dh	SECM_SYNC_VB13	R	8000h	synchronous measurement result from balancing pins cell 13
1C8Eh	SECM_SYNC_VB14	R	8000h	synchronous measurement result from balancing pins cell 14
1C8Fh	SECM_SYNC_VB15	R	8000h	synchronous measurement result from balancing pins cell 15
1C90h	SECM_SYNC_VB16	R	8000h	synchronous measurement result from balancing pins cell 16
1C91h	SECM_SYNC_VB17	R	8000h	synchronous measurement result from balancing pins cell 17

7.4.8 Registers for all measurement

The registers block All Measurement Registers is writing simultaneously into the primary and the secondary measurement registers. This mechanism provides a comfortable way of ensuring the measurement configuration registers are set simultaneously for the primary and secondary measurement chain. A read back of the All Measurement Registers is not possible. The MC33774A returns 0000h as data in case one of the All Measurement Registers is read.

Table 20. Register overview: All_Measurement_Registers

Address	Name	Access	Reset	Description
1400h	ALLM_CFG	W	0h	general measurement control
1401h	ALLM_APP_CTRL	W	7C00h	application measurement control
1402h	ALLM_PER_CTRL	W	10h	periodic measurement control
1403h	ALLM_SYNC_CTRL	W	7C00h	synchronous measurement control
1408h	ALLM_VCVB_CFG0	W	0h	cell voltage measurement enable

Table 20. Register overview: All_Measurement_Registers*...continued*

Address	Name	Access	Reset	Description
1409h	ALLM_VCVB_CFG1	W	0h	cell voltage measurement enable

7.5 Cell balancing

The cell voltage-balancing function allows discharging individual cells based on external resistors and PWM modulated currents controlled by the MC33774. A constant current mode-balancing feature permits to limit the current variation due to the cell voltage. Because of the balancing structure, the balancing switches are enabled alternatively depending of their position on the module (odd/even). Different PWM duty cycle can be used to define the average current. The internal switches can be controlled by individual balancing timers and/or by the cell voltage. Additionally, the balancing process can be interrupted based on an external temperature sensor in order to manage the heat dissipation of the balancing resistors.

7.5.1 Functions

The MC33774A allows two main balancing modes:

- Timer-based balancing
- Cell voltage-based balancing

Combining of balancing modes is possible.

Other balancing functions enhance the balancing functionality.

- Global balancing timeout
- Global cell undervoltage-based balancing
- Temperature modulated balancing
- Junction temperature balancing protection
- Constant current balancing
- Pre-balancing timer
- PWM
- Auto pause
- Emergency discharge
- Analog switch monitoring

7.5.1.1 Cell balancing diagram

The cell-balancing circuit uses two back-to-back MOSFET transistors for each cell to support negative cell voltages.

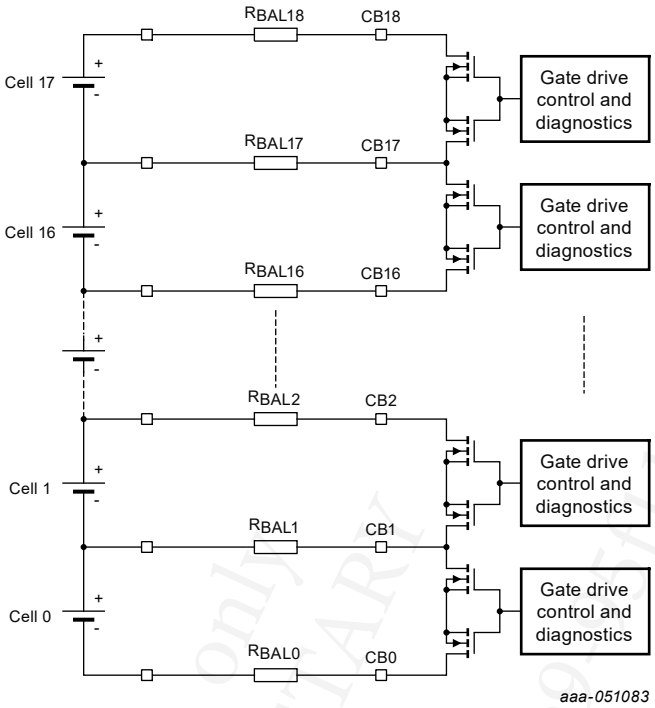


Figure 23. Cell balancing diagram

7.5.2 Functional diagram

Figure 24 shows the functional diagram of the balancing functionality.

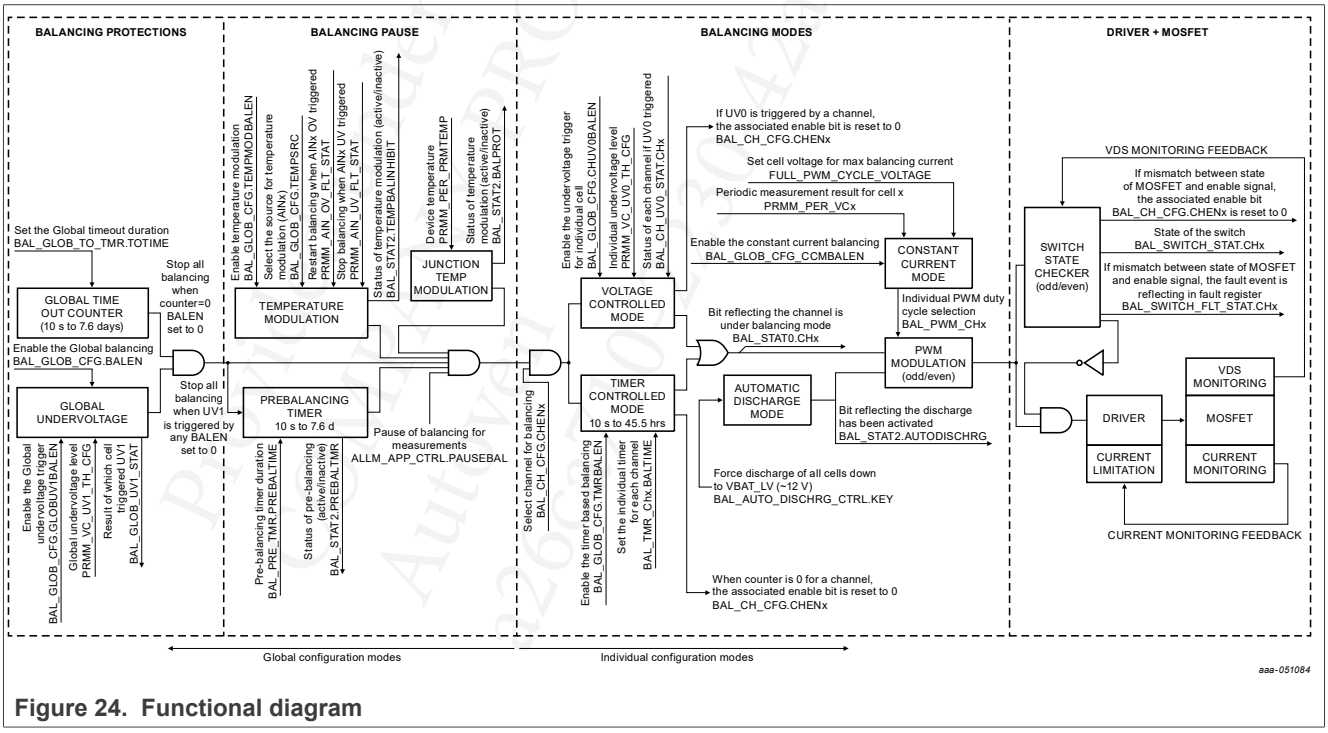


Figure 24. Functional diagram

7.5.3 Functional description

During balancing, odd and even balance MOSFET banks are alternatively enabled at the fixed frequency $f_{PWM(bal)}$. The following are descriptions of the different balancing modes.

7.5.3.1 Timer-based balancing

The timer-based balancing allows a time-controlled discharge of the cells. The discharge time for the cells can be set individually for the channels. Individual discharge time is set by writing into the registers BAL_TMR_CH0 to BAL_TMR_CH17. Writing into BAL_TMR_CH_ALL sets all registers BAL_TMR_CH0 to BAL_TMR_CH17 simultaneously. If the timer-based balancing is active, the balancing timer counter counts down every 10 seconds. Once the timer for a cell expires, the balancing action for this cell stops.

To enable timer-based balancing, the bits BAL_GLOB_CFG.BALEN and BAL_GLOB_CFG.TMRBALEN must be logic 1. BAL_GLOB_TO_TMR.TOTIME must be non-zero.

The timer-based balancing can be combined with the other balancing functions. The other enabled balancing functions can cause an interruption of the balancing activity. During the interruption, the balancing timer of the affected channel does not decrement.

Application usage: Timer-based balancing is a state-of-the-art way for cell balancing.

7.5.3.2 Cell undervoltage based balancing

The cell voltage-balancing function allows discharging of a cell until the cell reaches the undervoltage threshold set in PRMM_VC_UV0_TH_CFG. For the monitoring of the cell voltage, the primary measurement chain is used.

To enable cell undervoltage-based balancing, the bits BAL_GLOB_CFG.BALEN and BAL_GLOB_CFG.CHUV0BALEN must be logic 1. BAL_GLOB_TO_TMR.TOTIME must be non-zero.

The cell undervoltage-based balancing can be combined with the other balancing functions. Other enabled balancing functions can cause an interruption or complete stop of the balancing activity.

Application usage: Cell undervoltage-based balancing is a new way for cell balancing. It discharges the cells to the BAL_CH_UV0 threshold.

Note: *The cyclic measurement must be active to allow cell voltage-measurement updates. If cyclic measurements are disabled, the balancing continues until the global balancing timeout function stops the discharge.*

7.5.3.3 Global undervoltage based balancing

The global undervoltage-balancing function allows discharging of a cell until one cell reaches the undervoltage threshold PRMM_VC_UV1_TH_CFG. For the monitoring of the cell voltages, the primary measurement chain is used.

To enable global undervoltage-based balancing, the bits BAL_GLOB_CFG.BALEN and BAL_GLOB_CFG.GLOBUV1BALEN must be logic 1. BAL_GLOB_TO_TMR.TOTIME must be non-zero.

The global undervoltage-based balancing can be combined with the other balancing functions. Other enabled balancing functions can cause an interruption or complete stop of the balancing activity.

Application usage: Global undervoltage-based balancing is a protection feature to avoid deep discharge of cells because of current consumption of the IC during balancing.

Note: *The cyclic measurement must be active to allow cell voltage-measurement updates. If cyclic measurements are disabled, the balancing continues until the global balancing timeout function stops the discharge.*

7.5.3.4 Global balancing timeout

The global-balancing timeout timer is used to configure the maximum balancing time for all balancing activities.The counter counts down every 10 seconds as soon as its value is non-zero, independent of any other conditions. Once the timer expires, the balancing switches are switched OFF. The bit BAL_GLOB_CFG.BALEN is set to logic 0. The global-balancing timeout timer and the balancing timers for the individual channels use independent clock sources. In case balancing actions are intended, the global-balancing timeout should be set long enough to allow the needed balancing activities.

Application usage: Global timeout is protection feature to avoid deep discharge.

7.5.3.5 Pre-balancing timer

The pre-balancing timer BAL_PRE_TMR allows delaying or pausing of the balancing activity. The counter decrements as soon as bit BAL_GLOB_CFG.BALEN is set logic 1. Once the counter is expired, the balancing activity is enabled. The pre-balancing timer holds the timers for the timer-based balancing. The pre-balancing timer has no impact on the global balancing timeout.

Application usage: The pre-balancing timer can be set to allow a cooldown of the system before the balancing activity is started.

7.5.3.6 Temperature-modulated balancing

The temperature-modulated balancing is an add-on to the other balancing functions. It cannot be used standalone. This mode is activated when BAL_GLOB_CFG.TEMPMODBALEN is set to 1.The source of the temperature-modulated balancing can be selected with BAL_GLOB_CFG.TEMPSRC. Only AIN0 to AIN3 can be used. The temperature-modulated balancing works with a two-point approach. The balancing is stopped once the selected analog-input pin falls below the lower comparator limit (register PRMM_AIN0_UV_TH_CFG to PRMM_AIN3_UV_TH_CFG). If timer-based balancing is active, the balancing timers are on hold as well. The global balancing timeout timer continues. Once the selected analog input pin exceeds the upper comparator limit (register PRMM_AIN0_OV_TH_CFG to PRMM_AIN3_OV_TH_CFG), the balancing activity is started again. The cell balancing timers decrement again.

Application usage: Temperature-modulated balancing allows thermal management during balancing.

Note: *The cyclic measurement must be active to allow updates of the AIN pin measurements. If cyclic measurements are disabled, the balancing is not modulated.*

Note: *After balancing activity is started again, a short balancing pause between the next balancing mosfet banks transition can occur.*

7.5.3.7 PWM for balancing

The PWM for balancing allows operating the activated analog balancing switch in PWM mode. The PWM duty cycle is controlled with registers BAL_PWM_CH0 to BAL_PWM_CH17 and can be set from 0 to 100 % by 0.39 % step.

Note: *If the PWM period is updated when the cell balancing is activated, in some cases, the PWM period can be 1 ms less than the programmed period. This effect is permanent until a new PWM period is set.*

Application usage: PWM for balancing allows thermal management during balancing.

7.5.3.8 Constant current cell balancing

The Constant Current Cell Balancing mode allows to balance with a constant current based on a fixed balancing resistor and a changing cell voltage. The Constant Current mode balancing feature permits to have less variation of the balancing current versus cell voltage. It adapts automatically the PWM duty cycle of the

activated balancing channels based on their primary periodic measurement results. This mode is activated when BAL_GLOB_CFG.CCMBALEN is set to 1.

As the balancing current depends on the external balancing resistor, to keep a constant balancing current, a configurable full PWM cycle voltage register (register FULL_PWM_CYCLE_VOLTAGE) sets the minimum cell voltage on which the balancing is operating at the maximum current (100 % ON in respective odd or even sequence). The PWM duty cycle can be calculated from the following equation ⟦PWM⟧_DutyCycle=V_(Cell_min) / V_Cell.

BAL_PWM_CH0 to BAL_PWM_CH17 registers are automatically updated with the last duty cycle calculated by the device.

Application usage: PWM for balancing allows constant current during balancing.

7.5.3.9 Analog balancing switch monitoring

The analog balancing switch does the actual switching of the balancing current. It is implemented for each channel. Each switch has a current limitation circuit. Each switch is monitored for the correct status when the switch is enabled for monitoring (BAL_SWITCH_MON_CFG) and the balancing is enabled (BAL_GLOB_CFG.BALEN = 1).

A violation of the status is detected when the voltage across the corresponding CB pins is:

- Above the output fault detection voltage threshold, when the switch shall be closed
- Below the output fault detection voltage threshold, when the switch shall be open

Note: *Connectivity of the CB pins is checked via the cell balancing terminal pulldown resistors in the measurement block (see Section 7.7.2).*

Application usage: Execution and monitoring of balancing activities.

7.5.3.10 Junction temperature balancing protection

The Junction Temperature Balancing mode is an additional protection to avoid the risk of over temperature on the die during balancing sequence. It cannot be deactivated. It is enabled when balancing operation is enabled.

Balancing of all cells are interrupted when the internal IC primary junction temperature measurement is above the junction temperature upper threshold for cell balancing thermal protection. If timer-based balancing is active, the balancing timers are on hold as well. The individual balancing timers will resume automatically when the internal IC primary junction temperature measurement has decreased by the junction temperature hysteresis for cell balancing thermal protection and the cell balancing timers decrement again.

The pause does not affect the global balancing timeout timer.

7.5.3.11 Auto pause

The auto pause feature is implemented as part of the measurement function. The cell balancing function receives the pause signal, which temporarily inhibits the cell balancing. The balancing function holds the individual balancing timer. The pause does not influence the global timeout timer.

Application usage: The auto pause feature is used to avoid influence of the balancing activity on the secondary cell voltage measurement.

Note: *Prior triggering an automatic discharge:*

- *Temperature modulated balancing should be deactivated: BAL_GLOB_CFG.TEMPMODBALEN set to 0*
- *Ongoing balancing pause should be stopped (PAUSEBAL = 0)*
- *Automatic discharge functionality shoud not be used when Ta > 105 °C*

7.5.3.12 Automatic discharge

The automatic discharge functionality allows an emergency discharge of the cells. The discharge is started by writing the enable key (DEADh) into register BAL_AUTO_DISCHRG_CTRL. Once the automatic discharge is enabled, the balancing switches are turned on with 100 % duty cycle. The discharge is stopped by writing the disable key (2152h) into register BAL_AUTO_DISCHRG_CTRL or when a supply low-voltage condition occurs.

The automatic discharge is the only balancing feature that can be active in case the BAL_GLOB_CFG.BALEN is logic 0. Automatic discharge is independent of the temperature modulation. The global balancing timeout has no influence on the automatic discharge, but when the automatic discharge is active, the global balancing timeout timer is on hold. In case an overvoltage condition on VBAT is present during auto discharge, the automatic discharge is put on hold. The global balancing timeout timer is resuming from hold. Clearing of the overvoltage error flag (FEH_SUPPLY_FLT_STAT0.VBATOV) enables the auto discharge again. The global balancing timeout timer is again put on hold.

In case a switch error on a balancing switch is detected, the affected channel is turned off.

7.5.4 Cell balancing process

7.5.4.1 Start of balancing

The bit BAL_GLOB_CFG.BALEN is the global enabling bit for the balancing circuit. All balancing related functions, including diagnostics are only active if the bit is set to logic 1.

7.5.4.2 Balancing operation

During balancing in Active mode, the MC33774A is operating the same way as without balancing. Once the balancing activity of a channel is completed, the individual balancing enable bit BAL_CH_CFG.CHEN0 to CHEN17 for this channel is cleared.

When the cyclic wake-up function is used, the MC33774A enters into Cyclic mode at the selected set time interval. In Cyclic mode, one periodic measurement is performed. The measurement results are used for the voltage- and temperature-based balancing functionality.

7.5.4.3 Completion of balancing

When all individual balancing enable bits BAL_CH_CFG.CHEN0 to BAL_CH_CFG.CHEN17 are cleared, the balancing activity is finished. The bit BAL_GLOB_CFG.BALEN is reset and the bit BAL_STAT1.RDY is set to logic 1.

The following conditions clear the balancing enable bits:

- Global balancing timer is expired
- Timer-based balancing is activated and all activated individual balancing timers are expired
- Global undervoltage based balancing is activated and one activated cell has reached the global undervoltage threshold
- Cell undervoltage based balancing is activated and all activated cells have reached the undervoltage threshold

Note: *The MC33774A does not report the reason for clearing the individual enable bits.*

7.5.5 Cell balancing diagnostics

The MC33774A provides diagnostic to monitor the integrity of the balancing operation. Connectivity of the CB pins is checked via the cell balancing terminal pulldown resistors in the measurement block (see Section 7.7.2).

7.5.5.1 Switch status monitoring

Registers BAL_SWITCH_STAT0 and BAL_SWITCH_STAT1 provide for each switch the status (open or closed).

7.5.5.2 Analog balancing switch monitoring

The analog balancing switch monitoring does the monitoring of each individual switch. Registers BAL_SWITCH_FLT_STAT0 and BAL_SWITCH_FLT_STAT1 provide, for each switch, a fault indication. Any deviation of the physical state of the balancing circuit from the intended one is considered as a fault.

Each switch is monitored for the correct status, overcurrent, and open-load detection circuit with a separate enable.

Application usage: Execution and monitoring of balancing activities.

7.5.6 Cell balancing registers

All registers related to the cell balancing are listed here. Details on the registers and the bit fields are explained in the register map chapter.

Table 21. Register overview: Balancing_Registers

Address	Name	Access	Reset	Description
1000h	BAL_GLOB_CFG	R/W	0h	The global balancing configuration register is used to configure the balancing modes.
1001h	BAL_GLOB_TO_TMR	R/W	0h	The Global Balancing timeout timer register is used to configure the maximum balancing time for all balancing activities to make sure that in case of fault the balancing switches are switched OFF.
1002h	BAL_CH_CFG0	R/W	0h	balancing channel individual enable channel 0 - 15
1003h	BAL_CH_CFG1	R/W	0h	balancing channel individual enable channel 16 - 17
1004h	BAL_PRE_TMR	R/W	0h	pre-balancing timer
1005h	BAL_AUTO_DISCHRG_CTRL	R/W	2152h	emergency discharge enable
1006h	BAL_SWITCH_MON_CFG0	R/W	FFFFh	balancing switch monitoring enable
1007h	BAL_SWITCH_MON_CFG1	R/W	3h	balancing switch monitoring enable
1008h	FULL_PWM_CYCLE_VOLTAGE	R/W	0h	full PWM cycle voltage
1009h	BAL_CH_UV0_STAT0	R	0h	channel under-voltage balancing status channel 0 - 15
100Ah	BAL_CH_UV0_STAT1	R	0h	channel under-voltage balancing status channel 16 - 17
100Bh	BAL_GLOB_UV1_STAT0	R	0h	global under-voltage balancing status channel 0 - 15
100Ch	BAL_GLOB_UV1_STAT1	R	0h	global under-voltage balancing status channel 16 - 17
100Dh	BAL_STAT0	R	0h	logical balancing channel status channel 0 - 15
100Eh	BAL_STAT1	R	0h	logical balancing channel status channel 16 - 17
100Fh	BAL_STAT2	R	0h	balancing status
1010h	BAL_SWITCH_STAT0	R	0h	physical balancing channel status channel 0 - 15
1011h	BAL_SWITCH_STAT1	R	0h	physical balancing channel status channel 16 - 17

Table 21. Register overview: Balancing_Registers...*continued*

Address	Name	Access	Reset	Description
1012h	BAL_SWITCH_FLT_STAT0	R	0h	balancing switch fault channel 0 - 15
1013h	BAL_SWITCH_FLT_STAT1	R	0h	balancing switch fault channel 16 - 17
101Fh	BAL_TMR_CH_ALL	W	0h	virtual register, writes in parallel into BAL_TMR_CH0 up to BAL_TMR_CH17
1020h	BAL_TMR_CH0	R/W	0h	balancing timer channel 0
1021h	BAL_TMR_CH1	R/W	0h	balancing timer channel 1
1022h	BAL_TMR_CH2	R/W	0h	balancing timer channel 2
1023h	BAL_TMR_CH3	R/W	0h	balancing timer channel 3
1024h	BAL_TMR_CH4	R/W	0h	balancing timer channel 4
1025h	BAL_TMR_CH5	R/W	0h	balancing timer channel 5
1026h	BAL_TMR_CH6	R/W	0h	balancing timer channel 6
1027h	BAL_TMR_CH7	R/W	0h	balancing timer channel 7
1028h	BAL_TMR_CH8	R/W	0h	balancing timer channel 8
1029h	BAL_TMR_CH9	R/W	0h	balancing timer channel 9
102Ah	BAL_TMR_CH10	R/W	0h	balancing timer channel 10
102Bh	BAL_TMR_CH11	R/W	0h	balancing timer channel 11
102Ch	BAL_TMR_CH12	R/W	0h	balancing timer channel 12
102Dh	BAL_TMR_CH13	R/W	0h	balancing timer channel 13
102Eh	BAL_TMR_CH14	R/W	0h	balancing timer channel 14
102Fh	BAL_TMR_CH15	R/W	0h	balancing timer channel 15
1030h	BAL_TMR_CH16	R/W	0h	balancing timer channel 16
1031h	BAL_TMR_CH17	R/W	0h	balancing timer channel 17
1032h	BAL_PWM_CH_ALL	W	FFh	virtual register, writes in parallel into BAL_PWM_CH0 up to BAL_PWM_CH17
1033h	BAL_PWM_CH0	R/W	FFh	balancing PWM channel 0
1034h	BAL_PWM_CH1	R/W	FFh	balancing PWM channel 1
1035h	BAL_PWM_CH2	R/W	FFh	balancing PWM channel 2
1036h	BAL_PWM_CH3	R/W	FFh	balancing PWM channel 3
1037h	BAL_PWM_CH4	R/W	FFh	balancing PWM channel 4
1038h	BAL_PWM_CH5	R/W	FFh	balancing PWM channel 5
1039h	BAL_PWM_CH6	R/W	FFh	balancing PWM channel 6
103Ah	BAL_PWM_CH7	R/W	FFh	balancing PWM channel 7
103Bh	BAL_PWM_CH8	R/W	FFh	balancing PWM channel 8
103Ch	BAL_PWM_CH9	R/W	FFh	balancing PWM channel 9
103Dh	BAL_PWM_CH10	R/W	FFh	balancing PWM channel 10
103Eh	BAL_PWM_CH11	R/W	FFh	balancing PWM channel 11
103Fh	BAL_PWM_CH12	R/W	FFh	balancing PWM channel 12
1040h	BAL_PWM_CH13	R/W	FFh	balancing PWM channel 13
1041h	BAL_PWM_CH14	R/W	FFh	balancing PWM channel 14
1042h	BAL_PWM_CH15	R/W	FFh	balancing PWM channel 15
1043h	BAL_PWM_CH16	R/W	FFh	balancing PWM channel 16

Table 21. Register overview: Balancing_Registers*...continued*

Address	Name	Access	Reset	Description
1044h	BAL_PWM_CH17	R/W	FFh	balancing PWM channel 17

7.5.7 Balancing related registers

The most important registers related to the balancing function and the related content are shown in Table 22.

Table 22. Balancing related registers

Register	Content
PRMM_AIN0_OV_TH_CFG (Section 12.1.147)	upper comparator limit for AIN0
PRMM_AIN1_OV_TH_CFG (Section 12.1.148)	upper comparator limit for AIN1
PRMM_AIN2_OV_TH_CFG (Section 12.1.149)	upper comparator limit for AIN2
PRMM_AIN3_OV_TH_CFG (Section 12.1.150)	upper comparator limit for AIN3
PRMM_AIN0_UV_TH_CFG (Section 12.1.152)	lower comparator limit for AIN0
PRMM_AIN1_UV_TH_CFG (Section 12.1.153)	lower comparator limit for AIN1
PRMM_AIN2_UV_TH_CFG (Section 12.1.154)	lower comparator limit for AIN2
PRMM_AIN3_UV_TH_CFG (Section 12.1.155)	lower comparator limit for AIN3
PRMM_VC_UV1_TH_CFG (Section 12.1.146)	lower comparator limit 1 for VC0 to VC17
PRMM_VC_UV0_TH_CFG (Section 12.1.145)	lower comparator limit 0 for VC0 to VC17

7.6 GPIO pins

The GPIO pins allow a flexible usage for specific application functions. The functionalities offered by the GPIOs are:

- Analog input for auxiliary (ratiometric) measurements (all GPIO pins)
- Analog input for auxiliary (absolute) measurements (all GPIO pins and AINA pin)
- General-purpose inputs (all GPIO pins)
- General-purpose outputs (all GPIO pins)
- Wake input (GPIO0 and GPIO1)
- Alarm input (GPIO1)
- Alarm output (AINA)
- I^2C-bus master interface (GPIO4 and GPIO5)

Each pin offers several functionalities. Table 23 shows an overview of the pins and the functions.

Table 23. GPIO functions

Pin	Function
GPIO0	1. Analog input AIN0 for ratiometric measurement to VAUX or VDDC 2. Analog input AIN0 for absolute measurement 3. General-purpose input 0 4. General-purpose output 0 5. Wake-up input 0
GPIO1	1. Analog input AIN1 for ratiometric measurement to VAUX or VDDC 2. Analog input AIN1 for absolute measurement 3. General-purpose input 1 4. General-purpose output 1

Table 23. GPIO functions*...continued*

Pin	Function
	5. Wake-up input 1 6. Alarm input
GPIO2	1. Analog input AIN2 for ratiometric measurement to VAUX or VDDC 2. Analog input AIN2 for absolute measurement 3. General-purpose input 2 4. General-purpose output 2
GPIO3	1. Analog input AIN3 for ratiometric measurement to VAUX or VDDC 2. Analog input AIN3 for absolute measurement 3. General-purpose input 3 4. General-purpose output 3
GPIO4	1. Analog input AIN4 for ratiometric measurement to VAUX or VDDC 2. Analog input AIN4 for absolute measurement 3. General-purpose input 4 4. General-purpose output 4 5. I^{2}C-bus SCL
GPIO5	1. Analog input AIN5 for ratiometric measurement to VAUX or VDDC 2. Analog input AIN5 for absolute measurement 3. General-purpose input 5 4. General-purpose output 5 5. I^{2}C-bus SDA
GPIO6	1. Analog input AIN6 for ratiometric measurement to VAUX or VDDC 2. Analog input AIN6 for absolute measurement 3. General-purpose input 6 4. General-purpose output 6
GPIO7	1. Analog input AIN7 for ratiometric measurement to VAUX or VDDC 2. Analog input AIN7 for absolute measurement 3. General-purpose input 7 4. General-purpose output 7
AINA	1. Analog input AINA for absolute measurement 2. Alarm output

Configuring a special function (wake, alarm, I^{2}C-bus) sets the configuration of the GPIO pin automatically for this functionality. More than one function can be selected.

When a pin is configured as analog input, an external low-pass filter is mandatory. If no external low-pass filter is present, the analog measurement functionality must be disabled. Configuring I^{2}C-bus functionality and general-purpose output functionality results in I^{2}C-bus functionality. General-purpose output settings are ignored in this case.

7.6.1 Analog input

The primary measurement chain measures the voltage at GPIO0 to GPIO3 and AINA.

The secondary measurement chain measures the voltage at GPIO4 to GPIO7.

Note: *During cyclic measurement of the MC33774A, only the primary measurement chain is active. GPIO4 to GPIO7 cannot be monitored in cyclic mode.*

Note: *The leakage current of $I_{L(GPIO)}$ is for GPIO2 to GPIO7 only guaranteed if VDDC is available. If GPIO2 and GPIO3 shall be measured in cyclic mode, VDDC must be enabled (set bit SYS_SUPPLY_CFG.VDDCCYC to logic 1).*

Details on the measurement functionality are in the measurement section.

Application usage: Analog voltage measurements for various functions, such as temperature-based balancing (GPIO0 to GPIO3), voltage measurements, and independent voltage measurements.

7.6.2 I²C-bus master interface

GPIO4 and GPIO5 offer an I²C-bus master interface.

Details on the I²C-bus master interface functionality are in the I²C-bus interface section.

Application usage: Communication to other components [for example: external EEPROM, near-field communication (NFC)].

7.6.3 General-purpose input

All GPIO pins offer a general-purpose input functionality.

The bits GPIO_CFG0.INPEN0 to GPIO_CFG0.INPEN7 enable the pin for input. The bits GPIO_IN.IN0 to GPIO_IN.IN7 reflect the status of the pin. The bits GPIO_IN.HIGHDET0 to GPIO_IN.HIGHDET7 provide the info whether a high level was present at the pin since the last read command.

Application usage: Reading of digital input signals.

7.6.4 General-purpose output

All GPIO pins offer a general-purpose output functionality.

The bits GPIO_CFG0.OUTEN0 to GPIO_CFG0.OUTEN7 enable the pin for output. The bits GPIO_CFG1.ODEN0 to GPIO_CFG1.ODEN7 configure the output pin for open-drain configuration. The bits GPIO_OUT.OUT0 to GPIO_OUT.OUT7 set the state for the output.

Application usage: Driving of digital outputs signals.

7.6.5 Wake input

GPIO0 and GPIO1 offer a wake-up input functionality. FEH_WAKEUP_CFG0.WAKEUPIN configures GPIO0 as wake-up input. FEH_WAKEUP_CFG0.ALARMIN configures GPIO1 as wake-up input.

Note: *GPIO0 expects an active HIGH signal. GPIO1 can be configured for acting on active HIGH, active LOW, or heartbeat signals.*

Application usage: Wake-up of the system on external triggers.

7.6.6 Alarm input

GPIO1 offers an alarm input functionality. FEH_ALARM_CFG.ALARMIN configures GPIO1 as alarm input. See Section 7.2 on how to use the alarm input event.

Note: *An alarm reported in FEH_ALARM_OUT_REASON0.ALARMIN should be re-checked by the pack controller. To such purpose, the pack controller may clear the flag (set it to 0) to check if the error is reconfirmed.*

Application usage: Wake-up of the system by alarms.

7.6.7 GPIO registers

All registers related to the GPIOs are listed here. Details to the registers and the bit fields are explained in the register map chapter.

Table 24. Register overview: GPIO_Registers

Address	Name	Access	Reset	Description
800h	GPIO_CFG0	R/W	0h	GPIO configuration 0
801h	GPIO_CFG1	R/W	0h	GPIO configuration 1
802h	GPIO_OUT	R/W	0h	GPIO output
804h	GPIO_IN	R	0h	GPIO input

7.7 Diagnostics

The MC33774A provides diagnostic options to validate the integrity of the measurement chain.

7.7.1 Cell-terminal pulldown resistors (CTx pins)

The MC33774A allows turning on a pulldown resistor between two adjacent cell terminal pins.

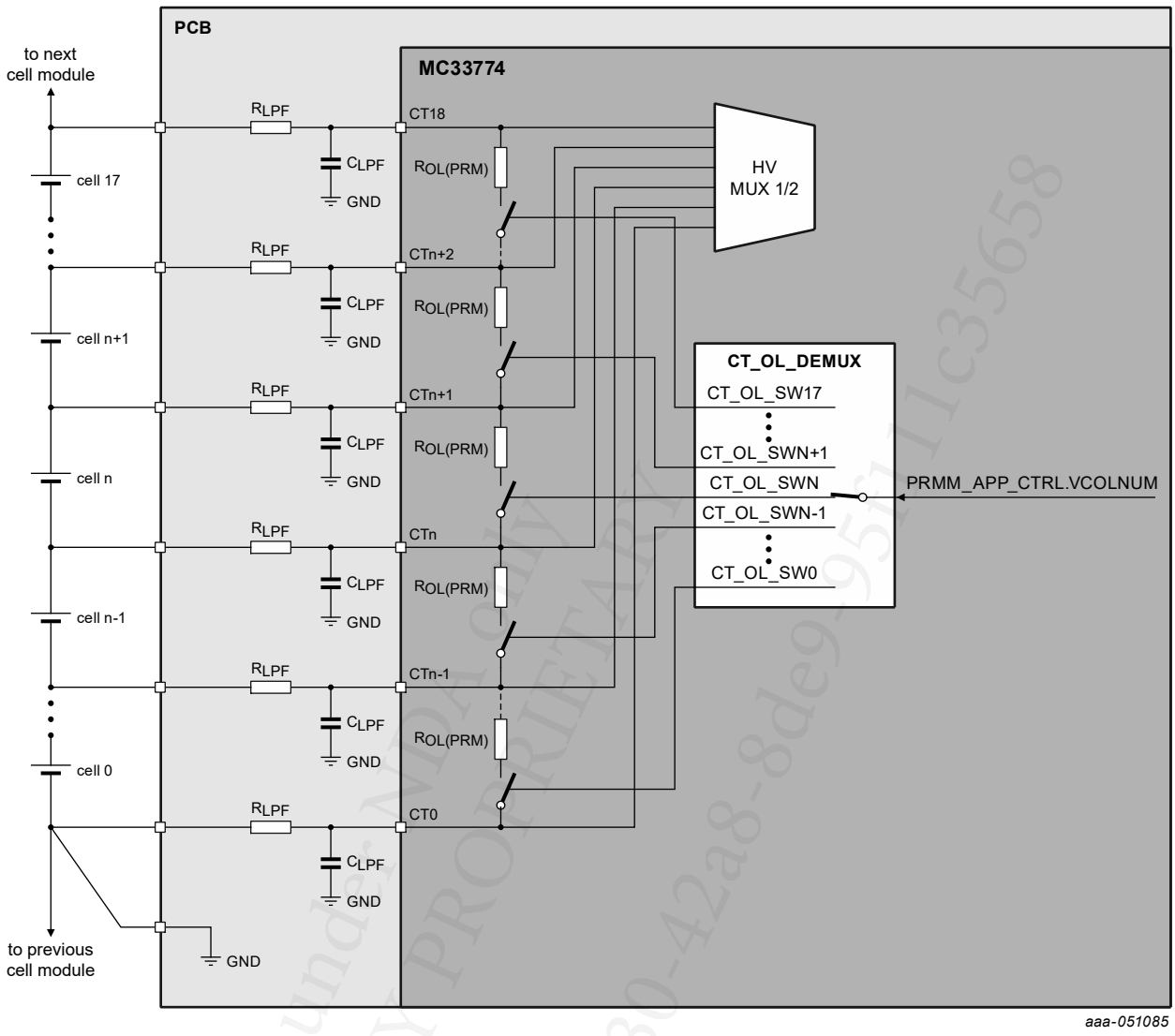


Figure 25. Cell terminal pulldown resistors

PRMM_APP_CTRL.VCOLNUM selects which switch is closed. Maximum one switch closes at one moment in time.

Application usage: Monitoring of the cell terminal connectivity and testing of the multiplexer functionality.

7.7.2 Cell-balancing terminal pulldown resistors (CBx pins)

The MC33774A allows turning on a pulldown resistor network between two adjacent cell-balancing terminal pins.

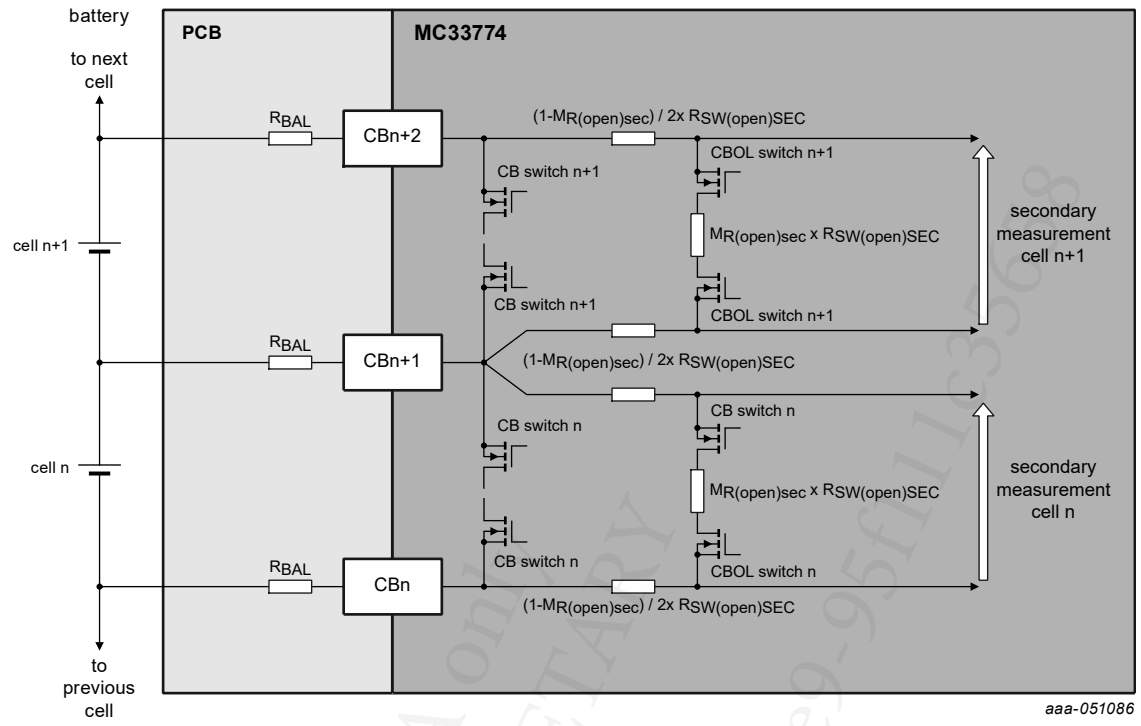


Figure 26. Cell balancing terminal pulldown resistors

SECM_SYNC_CTRL.VBOLNUM selects which switch is closed. Possible options are:

- One selected switch is closed (SECM_SYNC_CTRL.VBOLNUM is set to 0d to 17d)
- The MC33774A closes the switch for the channel ADC2B is measuring (SECM_SYNC_CTRL.VBOLNUM is set to 30d = 1Eh)
- No switch is closed (SECM_SYNC_CTRL.VBOLNUM is set to 1Fh)

Maximum one switch closes at one moment in time.

Application usage: Monitoring of the cell balancing terminal connectivity and testing of the multiplexer functionality.

7.7.3 AINx terminal pulldown resistors (AINx pins)

The MC33774A allows turning on a pulldown resistor for each individual analog input pin to GND.

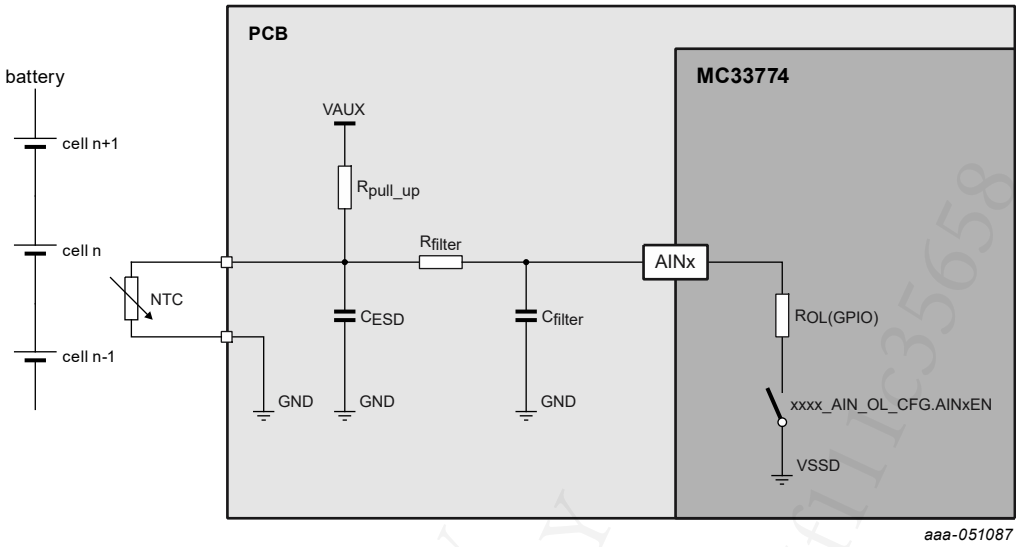


Figure 27. Cell terminal pulldown resistors

PRMM_AIN_OL_CFG.AIN0EN to PRMM_AIN_OL_CFG.AIN3EN and PRMM_AIN_OL_CFG_AINAEN control the OL_DETECT_SW for AIN0 to AIN3 and AINA.

SECM_AIN_OL_CFG.AIN4EN to SECM_AIN_OL_CFG.AIN7EN control the OL_DETECT_SW for AIN4 to AIN7.

Application usage: Monitoring of the connectivity of the AIN pins and testing of the multiplexer functionality.

7.7.4 Calibration CRCs

The MC33774A is calibrated at the end of the device production line. The calibration data is protected by a CRC. In case the register PRMM_CAL_CRC or SECM_CAL_CRC contains the value BEEFh, the calibration data is intact. If a different value is returned, the calibration data may be corrupted. Performance of devices with corrupted calibration data must not be trusted. The bit PRIMCALCRCFLT is signaling that a fault on the primary calibration data is detected. The bit SECCALCCRCFLT is signaling a fault on the secondary calibration data. Both error bits result in a result invalidation trigger (Figure 18).

Note: *Even when the MC33774A provides error bits for the calibration CRC faults, the MCU must check the PRMM_CAL_CRC and SECM_CAL_CRC register content as well.*

Application usage: Check of integrity of the calibration.

7.7.5 Measurement status bits

The registers PRMM_MEAS_STAT and SECM_MEAS_STAT contain several status bits. The bits MEASFLT, ANAFLT, and SUPPLYFLT signal faults that lead to invalidation of the measurement results (see Section 7.4.4). The bit COMFLT has no direct influence on the measurement, but is included in the registers as important diagnostic information.

The bits SYNCRDY and PERRDY signal that the new synchronized measurement results (see Section 7.4.4) or the new periodic measurement results (see Section 7.4.3.3) are available. The bits APPRDYVC, APPRDYAIN0 to APPRDYAIN7, and APPRDYAINA signal that new application timed measurement results can be requested (see Section 7.4.3.1).

Application usage: Monitoring of the measurement chains.

7.7.6 Synchronization monitoring

The purpose of a synchronous measurement is to measure with the primary and secondary measurement chain the same input at the same moment in time. To ensure that the measurements are performed at the same moment in time, the MC33774A monitors the synchronicity of the measurement chains during a synchronous measurement cycle. In case a deviation is detected, the bit SYNCMEASFLT is set. Reasons for deviations could be that the values of PRMM_PER_CTRL.PERLEN and SECM_PER_CTRL.PERLEN are unequal, the PRMM_SYNC_CTRL.SYNCCYC and SECM_SYNC_CTRL.SYNCCYC are not set simultaneously. Also differences in the enabled cells in the PRMM_VC_CFG and SECM_VB_CFG result in a SYNCMEASFLT.

Application usage: Ensure synchronicity of the measurement chains during a synchronous measurement cycle.

7.8 I²C-bus interface

The I²C-bus block allows communication to other components on the printed-circuit board (PCB) (for example: EEPROM, NFC). The device acts as I²C-bus master. The I²C-bus master module creates I²C-bus transactions as configured via the microcontroller interface. The MC33774A executes the I²C-bus transaction autonomously. An ongoing transaction has no impact on other blocks and can be executed parallel to any other task of the MC33774A.

The I²C-bus interface is compliant to NXP UM10204 for I²C-bus operation in Standard mode. The interface also supports Fast mode and Fast mode plus.

Transactions with a length below 14 bytes (including the device address) can be set up in one communication frame. If longer transactions are needed, the I²C-bus is held until the next part of the transaction has been set up. The I²C-bus offers various diagnostic information to allow a monitoring of the I²C-bus from the application microcontroller.

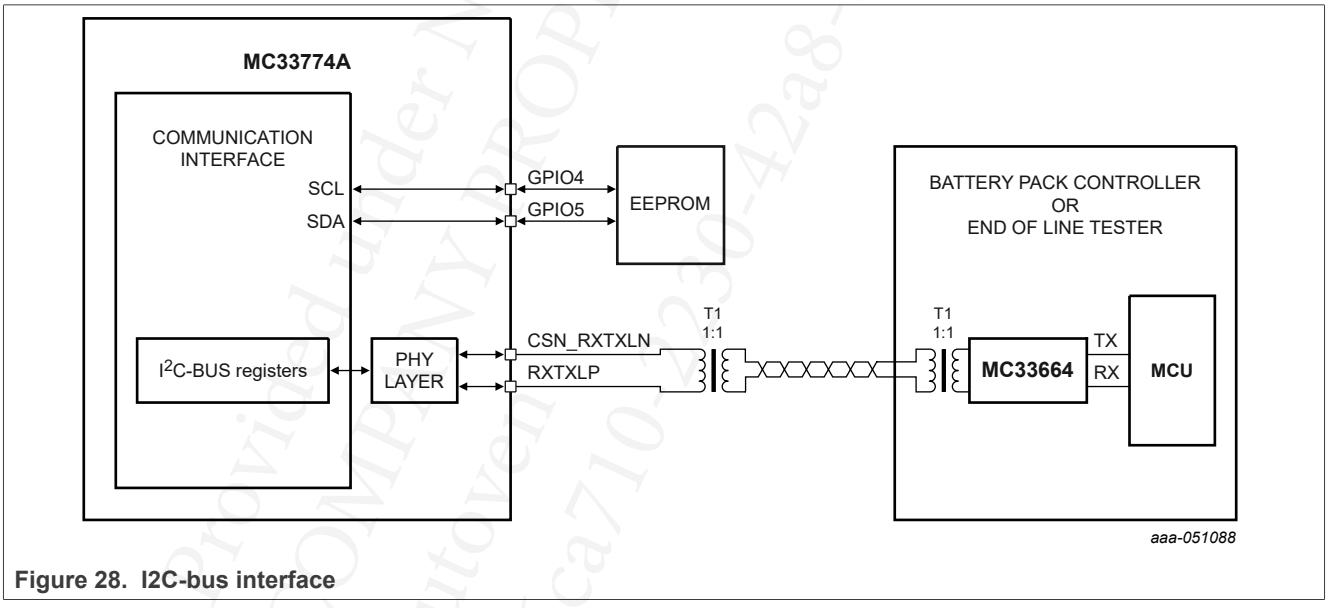


Figure 28. I2C-bus interface

Register I2C_CFG allows enabling and disabling of the interface and setting the I²C-bus clock frequency. Register I2C_CTRL initiates I²C-bus communication. Register I2C_STAT provides the status information of the interface. The data registers (I2C_DATA0 to I2C_DATA17) contain the actual data to be transmitted. After a read operation, the data read on the I²C-bus is stored in the data registers.

To ensure that all I²C-bus transitions are correct, it must be avoid sending the MC33774A to Sleep mode while a transaction is pending.

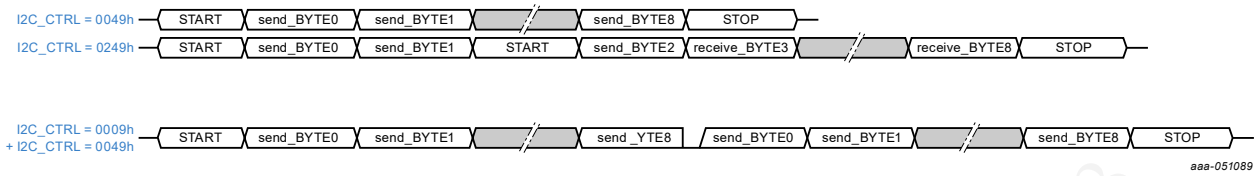


Figure 29. I2C-bus communication examples

Figure 29 shows some possible I^2C-bus transactions. The first line is a write command. The second line is a write with a switch to read. The third transaction shows a long sequence using two I^2C-bus transactions. Direct read commands, without using the switch to read function, are supported, as well. NXP UM10204 provides details about the I^2C-bus.

7.8.1 I^2C-bus registers

All registers related to the I^2C-bus interface are listed here. Details to the registers and the bitfields are explained in the register map chapter.

Table 25. Register overview: I2C_Registers

Address	Name	Access	Reset	Description
C00h	I2C_CFG	R/W	0h	I2C configuration
C01h	I2C_CTRL	R/W	0h	I2C control
C02h	I2C_STAT	R	0h	I2C status
C04h	I2C_DATA0	R/W	0h	I2C data register 0
C05h	I2C_DATA1	R/W	0h	I2C data register 1
C06h	I2C_DATA2	R/W	0h	I2C data register 2
C07h	I2C_DATA3	R/W	0h	I2C data register 3
C08h	I2C_DATA4	R/W	0h	I2C data register 4
C09h	I2C_DATA5	R/W	0h	I2C data register 5
C0Ah	I2C_DATA6	R/W	0h	I2C data register 6
C0Bh	I2C_DATA7	R/W	0h	I2C data register 7
C0Ch	I2C_DATA8	R/W	0h	I2C data register 8
C0Dh	I2C_DATA9	R/W	0h	I2C data register 9
C0Eh	I2C_DATA10	R/W	0h	I2C data register 10
C0Fh	I2C_DATA11	R/W	0h	I2C data register 11
C10h	I2C_DATA12	R/W	0h	I2C data register 12
C11h	I2C_DATA13	R/W	0h	I2C data register 13
C12h	I2C_DATA14	R/W	0h	I2C data register 14
C13h	I2C_DATA15	R/W	0h	I2C data register 15
C14h	I2C_DATA16	R/W	0h	I2C data register 16
C15h	I2C_DATA17	R/W	0h	I2C data register 17

7.9 Microcontroller interface

The microcontroller interface facilitates the communication between the microcontroller and the MC33774A. The interface is based on registers and exchanges data, for example, the voltage measurements, GPIO pin status information.

The microcontroller interface features:

- Single master - multiple slave communication
- Flexible or fixed frame length options (64-, 80-, 96-, and 112-bit frames)

Communication is done via SPI or TPL. The frame format for SPI and TPL communication is equivalent.

7.9.1 TPL3 message format

Command and response frames are exchanged primarily between a single master and a single slave. Broadcast commands can be transmitted from one master to multiple slaves. The purpose of the command and response transactions is to read and write to registers within the MC33774A register map.

The MC33774A uses TPL3 protocol, which supports messages with a length of 64 bits, 80 bits, 96 bits, and 112 bits. The dynamic message-length feature reduces the number of transactions for read/write of consecutive registers.

The MC33774A defines a set of fields that constitute the message format.

7.9.1.1 TPL3 message structure

The device supports dynamic message length.

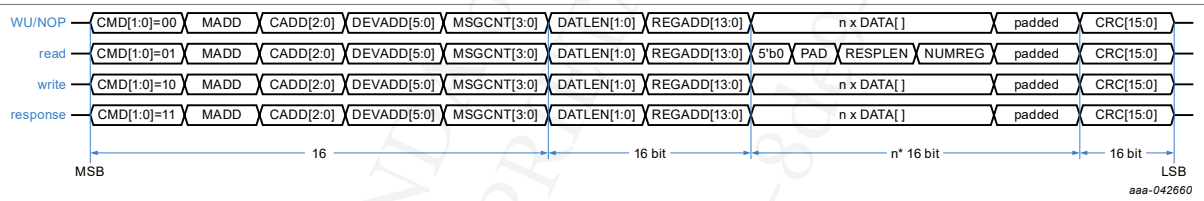


Figure 30. TPL3 message structure

The symbols used in the messages are listed in Table 26.

Because of the padding option, the number of register data provided in the data fields do not have to match with the message length. The data used for padding is used for CRC calculation, but has otherwise no effect. If a message contains fewer data fields than specified by DATALEN[1:0], the communication frame is discarded.

Table 26. Symbol description

Symbol	Value	Description
CMD[1:0]		Operation to be performed
	00	Wake-up message or no operation (NOP)[1]
	01	Read request message
	10	Write request message
	11	Response message
MADD		Indicates the address of the master transmitting
	0	Master 0 (also used by MC33774A in all response messages)
	1	Master 1
CADD[2:0]		Daisy chain address
	0	Reserved for future usage
	1	Daisy chain 1
	2	Daisy chain 2
	3	Daisy chain 3

Table 26. Symbol description...*continued*

Symbol	Value	Description
	4	Daisy chain 4
	5	Daisy chain 5
	6	Daisy chain 6
	7	All daisy chains
DEVADD[5:0]		Device address in the daisy chain
	0	Unenumerated device
	1 to 62	Device address
	63	All devices
MSGCNT[3:0]		Each MC33774A has a local message counter which is incremented after a message was sent. The counter rolls over to 0.
	0 to 15	Response message: current message counter value other messages: ignored by the MC33774A
DATLEN[1:0][2]		Number of valid data fields in the message
	0	DATA0 is valid
	1	DATA0 and DATA 1 are valid
	2	DATA0, and DATA1 and DATA2 are valid
	3	All four data fields are valid
REGADD[13:0]		Indicates the start address of the register access
	0 to 16383	Register addressed
0 0000b reserved (only for read commands)		This field is reserved and must have the value 0.
PAD[3] (only for read commands)	0	No padding used in response frames
	1	Padding is used in response frames
RESPLEN[1:0] (only for read commands)		Number of registers to be transferred in one response frame. If RESPLEN is greater than the number of registers to be transmitted, the device adapts the response length to fit the number of registers.
	0	Response length is one register
	1	Response length is two registers
	2	Response length is three registers
	3	Response length is four registers
NUMREG[7:0] (only for read commands)		Number of total registers requested
	0	One register
	1 to 255	Number of total registers requested = NUMREG + 1
DATA0[15:0]		Data to be transferred
DATA1[15:0]		Data to be transferred
DATA2[15:0]		Data to be transferred
DATA3[15:0]		Data to be transferred
Padded	0000h	Optional padding of message
CRC[15:0]		CRC value

[1] Differentiation for wake-up message and NOP messages is described in chapter Section 7.9.1.4.1.
[2] Read commands with DATALEN ≠ 0 are accepted, but only DATA0 is used.
[3] See Section 7.9.1.3.

7.9.1.2 Message CRC generation

The master and slaves calculate a 16-bit CRC on the entire message using the processes detailed in this section. The CRC is calculated using the polynomial $X^{16} + X^{13} + X^{12} + X^{11} + X^{10} + X^8 + X^6 + X^5 + X^2 + 1$ (identified by 3D65h - MSB first notation) with a seed value of 0000h. The seed value represents the initial status of the CRC calculation.

Note: *In Koopman notation, the polynomial corresponds to 9EB2h.*

Table 27. CRC parameters

Description	Value
CRC result width	16 bits
Polynomial (MSB-first notation)	3D65h
Polynomial (Koopman notation)	9EB2h
Seed	0000h

Procedure for CRC encoding (transmission)

The part of the message being encoded are bits from MSB to bit 16, bits 15 to 0 are reserved for CRC result.

1. Calculate the CRC over the message bits MSB to bit 16 using the given polynomial, and the seed as initial value.
2. Once the CRC is calculated, append it at the end of the message, and the message can be transmitted.

Table 28. CRC calculation examples

Message bits MSB to 16	CRC, 16 bit	Frame
1FFF FFFF FFEEh	7EF4h	1FFF FFFF FFEE 7EF4h
9FF0 1403 7C01h	D0C2h	9FF0 1403 7C01 D0C2h
4410 187F 070Eh	9434h	4410 187F 070E 9434h

Procedure for CRC check (reception)

Calculate the CRC over all bits of the received message (including CRC) using the given polynomial, and the seed as initial value.

- If the result is 00h, the CRC is correct. The MC33774A processes the message.
- If the result is different than 00h, the CRC is incorrect. The MC33774A discards the message, sets the CRCERR fault bit in the FEH_COM_FLT_STAT register, and increments the COMERRCNT.

Note: *The bit COMFLT signals the occurrence of communication faults, as well.*

Table 29. CRC check examples

Frame	CRC check result, 16 bit
01FF 0000 FFEE 948Eh	0000h
9FF0 1403 7C01 D0C2h	0000h
4410 187F 070E 9434h	0000h
C418 9009 0000 0000 0000 10F9h	0000h

7.9.1.3 Multiread responses with padding

The TPL3 protocol offers the option to request multiple consecutive registers with one read request message. The symbol RESPLEN[1:0] defines the number of registers to be transferred in one message. The symbol NUMREG[7:0] defines the number of registers that are requested. To transfer the requested number of

registers, the MC33774A sends as many messages with DATALEN[1:0] = RESPLEN[1:0] as needed. If the last message has less data to transfer than specified in RESPLEN[1:0], the device sends in the last message only the remaining register data.

The symbol PAD configures the length of this last message. With PAD set to logic 0, the length of the last message is adapted to match the number of registers to be transferred. With PAD set to logic 1, the last message is padded with 0000h to match the requested message length (as indicated by RESPLEN). If the message is a response to an access error, the padding is done with 8000h instead.

Note: *DATALEN is indicating the length of the message including the padded data.*

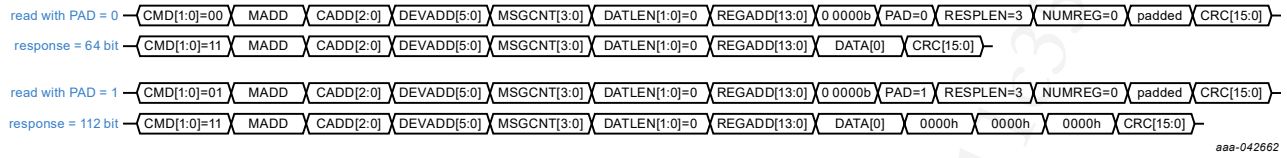


Figure 31. TPL3 response with and without padding

7.9.1.4 TPL wake-up commands

The MC33774A wakes up by any kind of bus activity; a dedicated wake message is needed. In order to wake all TPL3 devices connected, the TPL3 communication features a special command to wake up the system. In order to allow compatibility with TPL2 devices such as MC33664, the MC33774A can also be configured to initiate an MC33664-compatible wake command.

7.9.1.4.1 TPL3 wake-up message

NOP messages do not cause a reaction of the MC33774A. The only exception to this behavior is the wake-up message. The wake-up message is a 64-bit NOP message with DATA[0] = FFEEh sent to all devices (DEVADD[5:0] = 11 1111b). The daisy chain address (CADD[2:0]), master address (MADD), data length (DATLEN), and the message counter (MSGCNT[3:0]) are ignored.

Figure 32. Wake-up message for MC33774A

Once the device receives the wake-up message as explained above, the device initiates a wake-up of the system. For details of the system wake-up, see Section 7.9.2.3.

Note: *The system wake-up is initiated only once after entering active mode. The second wake-up message after entering active mode is treated as a regular NOP command.*

The wake-up message sent by the MC33774A is shown in Figure 33.

Figure 33. Wake-up message sent by MC33774A (WAKEUPCOMP = MC33774A)

7.9.1.4.2 Wake-up compatibility for MC33664

The MC33664 uses a different wake-up message than the MC33774A. To ensure compatibility with the MC33664, the MC33774A supports the generation of MC33664-compatible wake-up messages. The bits SYS_TPL_CFG.WAKEUPCOMP[1:0] set the wake-up message type for each TPL port. One port can be configured to MC33664 compatibility.

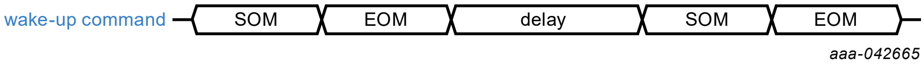


Figure 34. Wake-up message used by MC33664

Figure 34 shows the sequence sent by the MC33774A. The sequence consists of a two messages: a start of message (SOM) symbol and an end of message (EOM) symbol. The messages are separated by a delay.

7.9.2 TPL3 interface

High-speed differential isolated communication is achieved by using transformers or capacitors. The MC33774A offers two TPL ports to allow a daisy-chain communication of multiple devices. In one daisy chain, up to 62 nodes can be logically addressed via the device address. Device address 0d (DADD[5:0] or DEVADD[5:0] = 00 0000b) is reserved for network initialization. Device address 63d (DADD[5:0] or DEVADD[5:0]= 11 1111b) is reserved for broadcast messages.

7.9.2.1 TPL communication symbols

The TPL uses four pulse-encoded symbols for communication. The four symbols are shown in Figure 35 to Figure 38. The transformer driver generates SOM and EOM symbols. They always occur at the start and end of the communication message, respectively. Data pulses are used to transfer the actual information.

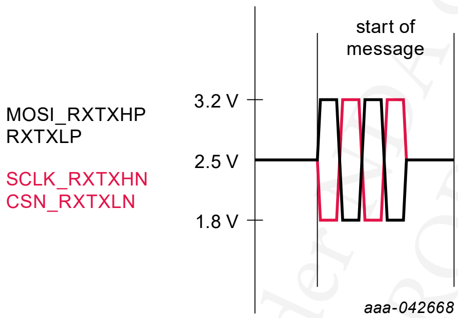


Figure 35. SOM

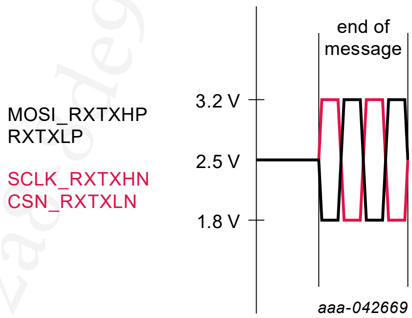


Figure 36. EOM

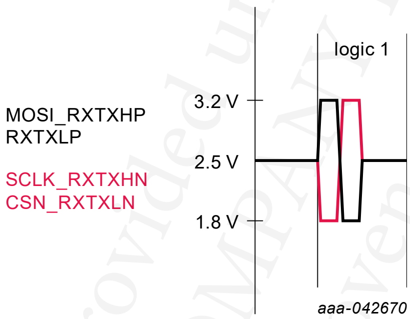


Figure 37. Logic 1

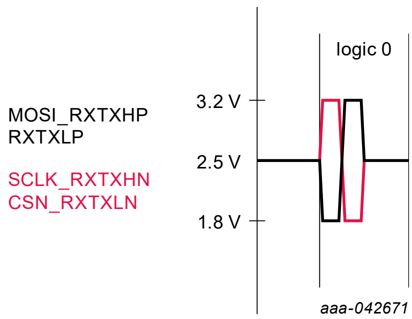


Figure 38. Logic 0

Figure 39 shows a typical TPL communication frame.

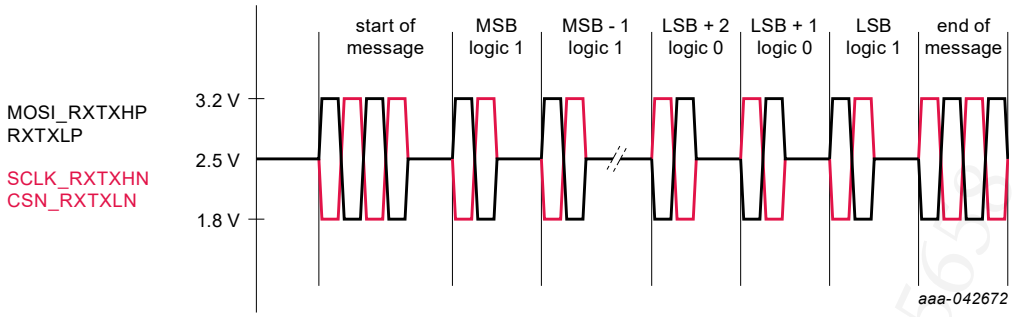


Figure 39. Example frame with content 11 to 001

7.9.2.2 TPL daisy-chain communication

The TPL communication is done in a daisy-chain configuration.

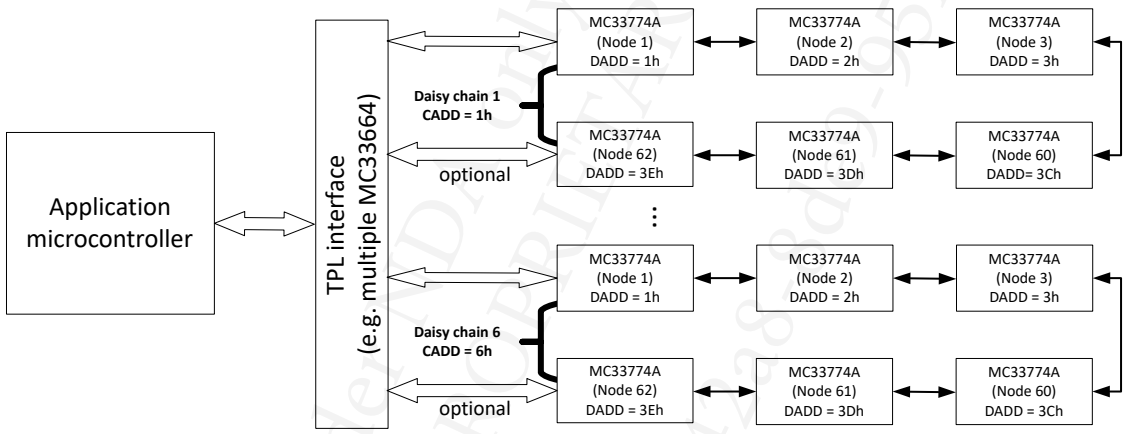


Figure 40. Setup for multiple TPL daisy chains

During communication, each device is checking the device address field in the communication messages. Devices react only to commands that are addressed to them (DEVADD of message is equal to DADD of the device, or broadcast messages). The MC33774A is not decoding the CADD field, but uses the CADD in all response messages. CADD = 0h must be reserved for future usage.

7.9.2.2.1 Communication methodology

The TPL communication physical layer does not offer any collision avoidance mechanism. On the higher communication layers, some mechanisms are implemented.

- The MC33774A ignores read commands to all devices (DEVADD[5:0] = 63) since the responses would cause bus collisions
- The MC33774A delays the start of sending of response messages in case the bus is busy. Messages received while a response is pending are ignored.

Otherwise, it is the task of the communication master to ensure that no collisions happen. If collisions occur, it is the task of the communication master to re-establish proper communication.

Write commands to the MC33774A do not generate a response message. Read commands sent by the master may generate a single response or multiple responses depending on the parameters used in the read request. The message size and start register are identified in the read command sent by the master.

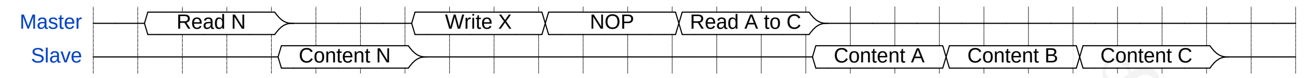


Figure 41. Bus traffic example

7.9.2.2.2 Message processing and compensation of forward delays

Each message received by the MC33774A is checked for integrity after reception. Valid messages for an individual device (DEVADD[5:0] = 0 to 3Eh) are executed within the delay time between two messages ($t_{d(req)MCU}$). The execution of write messages for all devices (DEVADD[5:0] = 3Fh) is delayed. The delay is calculated based on:

- The device address (SYS_COM_CFG.DADD)
- The number of nodes in the daisy chain (SYS_COM_CFG.NUMNODES)
- The direction of the communication (MADD of the communication message)
- The average forward delay

Table 30. Equation used for delay if MADD = 0

$$t_{delay} = (\mathrm{NUMNODES} - \mathrm{DADD}) \times t_{d(Fd)}$$

Table 31. Equation used for delay if MADD = 1

$$t_{delay} = (\mathrm{DADD} - 1) \times t_{d(Fd)}$$

Note: *Read messages for all devices are ignored as they would cause bus collisions.*

Compensating the forward delays allows all devices to execute global write commands at nearly the same moment in time.

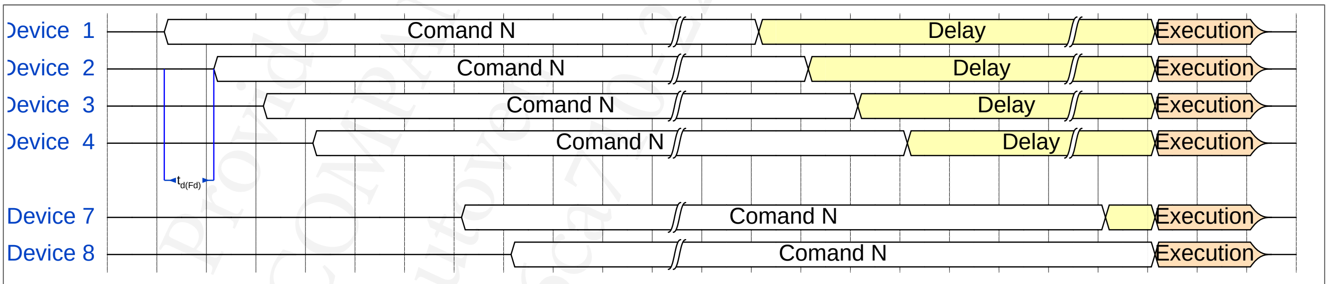


Figure 42. Compensation of forward delays with MADD = 1 and NUMNODES = 8

Note: *For proper operation of the forward delay compensation:*

- *The SYS_COM_CFG.NUMNODES must be set correctly in all devices*
- *If NUMNODES - DADD < 0, then the device considers* $t_{delay} = 0$
- *The devices must be enumerated in incrementing order when MADD = 1 is used and in decrementing order when MADD = 0 is used*

Note: *During the delay time, it is forbidden to send new messages to the MC33774A.*

Application usage: Synchronized start and end of measurements.

7.9.2.2.3 Device address and enumeration of devices

After power-up or Deep Sleep mode, the MC33774A starts with DADD = 0. To allow forwarding of messages and therefore enable communication toward a complete daisy chain, the DADD has to be assigned. This process is called enumeration.

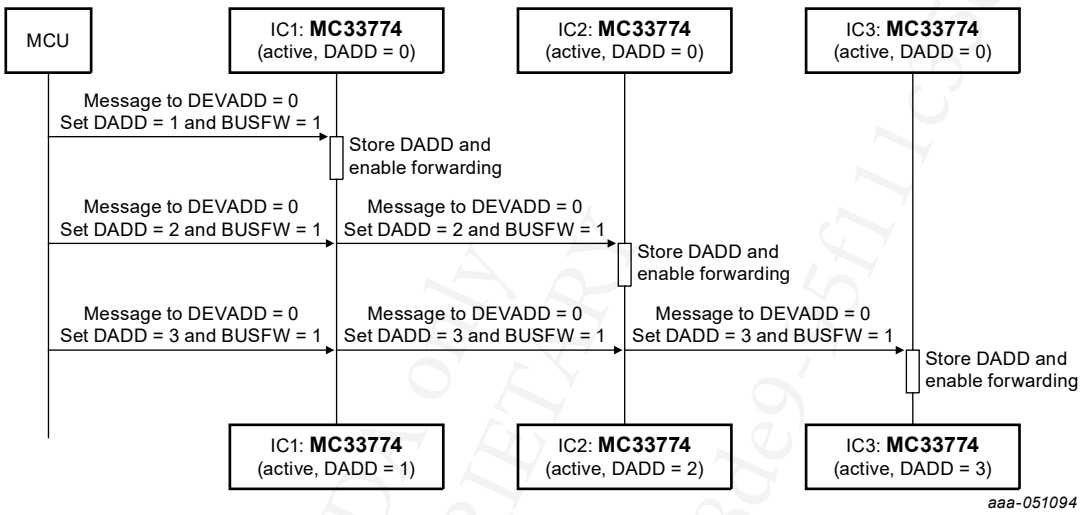


Figure 43. Enumeration process

An unenumerated device (DADD = 0) does not forward any communication. This behavior allows setting the device address for each device in the daisy chain based on the position in the daisy chain. An enumerated device (DADD ≠ 0) with enabled bus forwarding (bit SYS_COM_CFG.BUSFW) forwards any communication received on one TPL port to the other TPL port. This behavior allows communication from upper nodes to lower nodes and lower nodes to upper nodes. All devices in a daisy chain receive any communication sent by the application microcontroller.

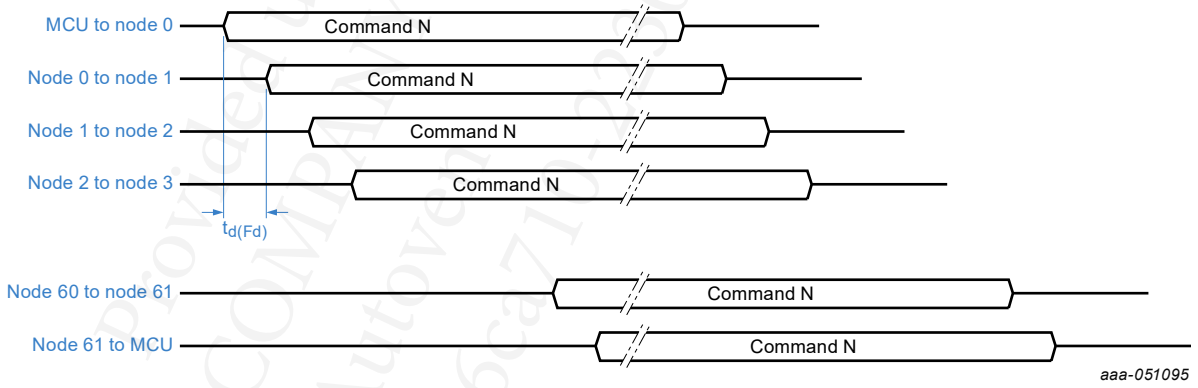


Figure 44. Communication example MCU to MC33774A

Responses to read commands are transmitted at both TPL interfaces. Figure 45 shows a response assuming that command N in Figure 44 was a read command for node 2.

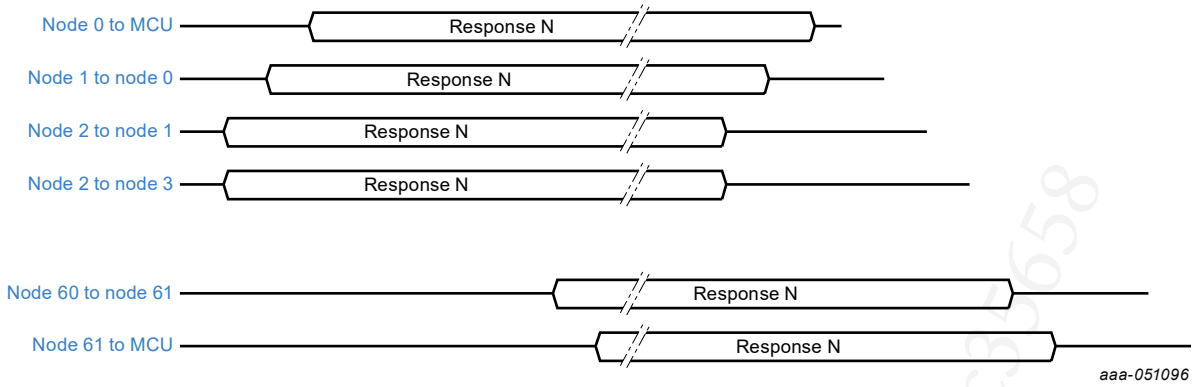


Figure 45. Communication example response to read request for node 2

7.9.2.3 Wake-up by TPL communication

The MC33774A contains bus wake-up capability. An MC33774A can wake up other devices, and other devices can wake up the MC33774A. If the MC33774A detects a wake-up condition and the wake-up is enabled, the device initiates a wake-up pulse sequence on the bus.

7.9.2.3.1 Wake-up of MC33774A

The MC33774A wakes up once there is any communication on the TPL bus.

7.9.2.3.1.1 Wake-up with enumerated devices (DADD[5:0] ≠ 0 and BUSFW = 1) using device wake-up messages

The first wake-up message or bus activity initiates a transition to Active mode. In Active mode, an enumerated MC33774A with BUSFW = 1 forwards any message. The second wake-up message transmitted by the MCU is forwarded to the next MC33774A in the daisy chain. The first MC33774A has now received two wake-up messages. It automatically sends one additional wake-up message toward the second MC33774A.

The second MC33774A in the daisy chain receives one forwarded wake-up message plus the generated message and acts in the same way as the first MC33774A. This behavior wakes the entire daisy chain. Figure 46 illustrates this behavior.

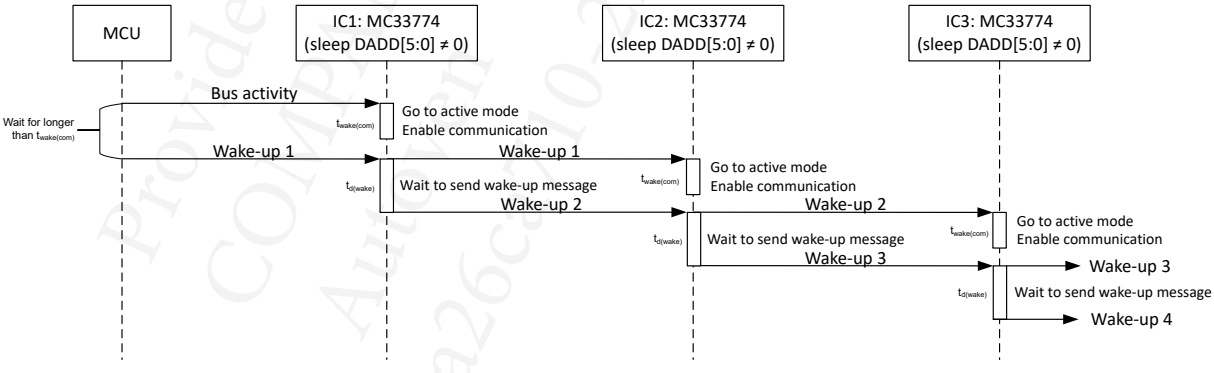


Figure 46. System wake-up with enumerated devices

Note: *The wake-up message used here is the one defined in Section 7.9.1.4.1.*

***Note:** Reception of a valid message during the wait time between the wake-up messages ($t_{d(wake)}$) stops the wake-up process.*

7.9.2.3.1.2 Wake-up with unenumerated devices (DADD[5:0] = 0) using device wake-up messages

An unenumerated MC33774A does not forward communication. The microcontroller can communicate only with the physically first IC of the daisy chain. Assigning a daisy chain address (DADD ≠ 0) and enabling the bus forwarding (BUSFW = 1) enables communication with the first and second IC. Continuing this process allows assigning unique addresses to all devices in the daisy chain based on their physical position in the daisy chain.

The first wake-up message or bus activity initiates a transition to Active mode. In Active mode, an unenumerated MC33774A does not forward messages. The second wake-up message transmitted by the MCU is not forwarded to the next MC33774A in the daisy chain. To wake up the entire daisy chain, the unenumerated MC33774A automatically sends two wake-up messages toward the second MC33774A.

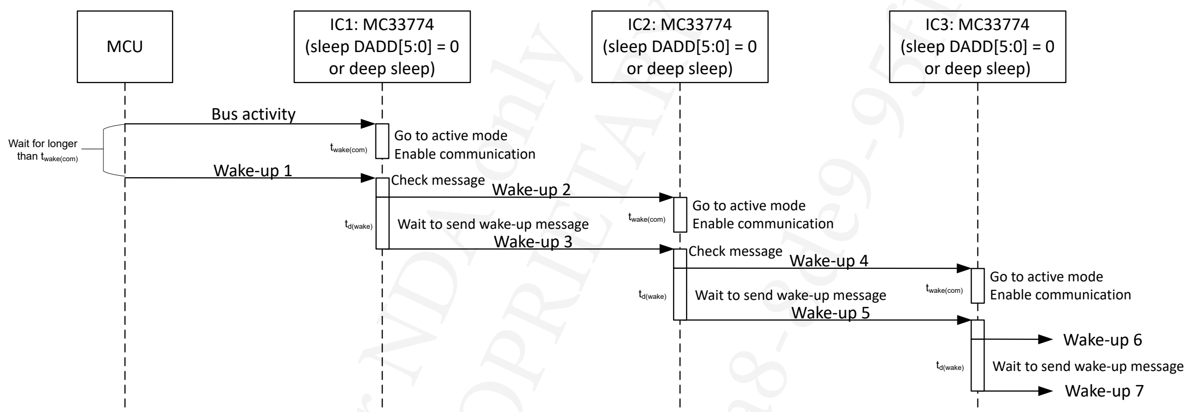


Figure 47. System wake-up with unenumerated devices

***Note:** The wake-up message used here is the one defined in Section 7.9.1.4.1.*

***Note:** Reception of a valid message during the wait time between the wake-up messages ($t_{d(wake)}$) stops the wake-up process.*

7.9.2.3.1.3 Wake-up with regular communication

The usage of wake-up messages as described in Section 7.9.2.3.1.1 and Section 7.9.2.3.1.2 automatically ensures the wake-up of the whole daisy chain. It is also possible to wake the system without usage of dedicated wake-up messages.

With start of bus activity, the first device in the chain starts to wake up. Once the device has completed the transition to Active mode, the device can receive and send messages. If the device is enumerated and the bus forwarding is enabled, the device forwards the communication. The resulting bus activity wakes up the next device in the daisy chain.

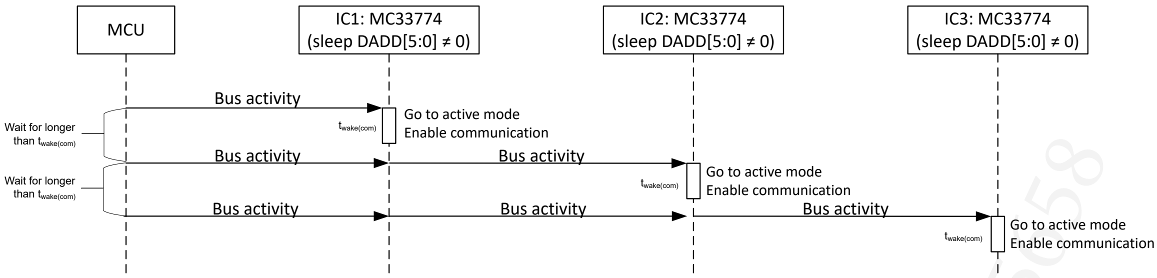


Figure 48. Wake-up without wake-up messages for enumerated devices (DADD[5:0] ≠ 0)

The concept of wake-up by communication can also be combined with the enumeration process.

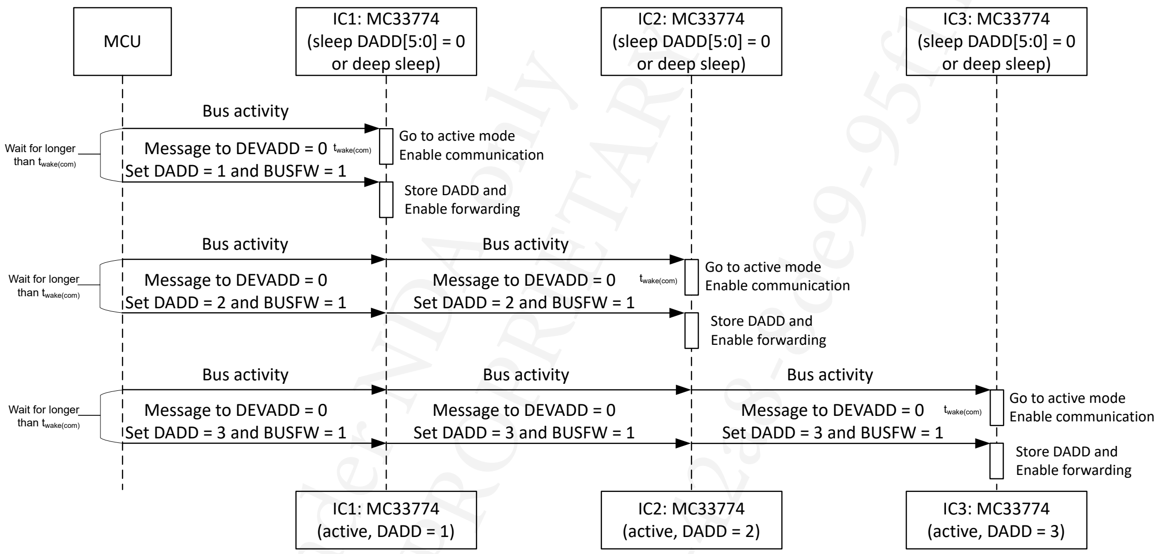


Figure 49. Wake-up and enumeration without wake-up messages for unenumerated devices (DADD[5:0] = 0)

7.9.3 SPI interface

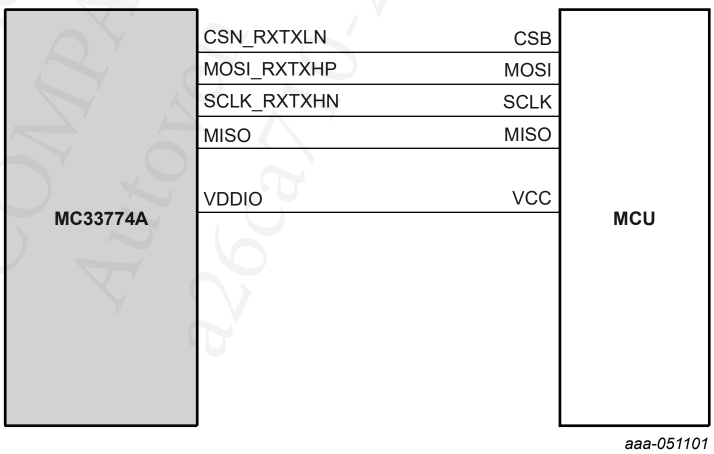


Figure 50. SPI connection

The SPI input signal levels to the MC33774A operate at 5.0 V logic levels but are 3.3 V compatible.

The VDDIO pin can be connected to the VDDC pin to get 5.0 V SPI output signal levels. To get 3.3 V SPI outuput signal levels, the VDDIO pin should be connected to an external 3.3 V supply.

The MC33774A SPI is a standard SPI with a chip select (CSN_RXTXLN), clock (SCLK_RXTXHN), master input slave output (MISO), and master output slave input (MOSI) (MOSI_RXTXHP). The shifting of the data follows a first in first out (FIFO) order, with both input and output words transferring the most significant bit (MSB) first. The microcontroller controls all SPI communication to the MC33774A.

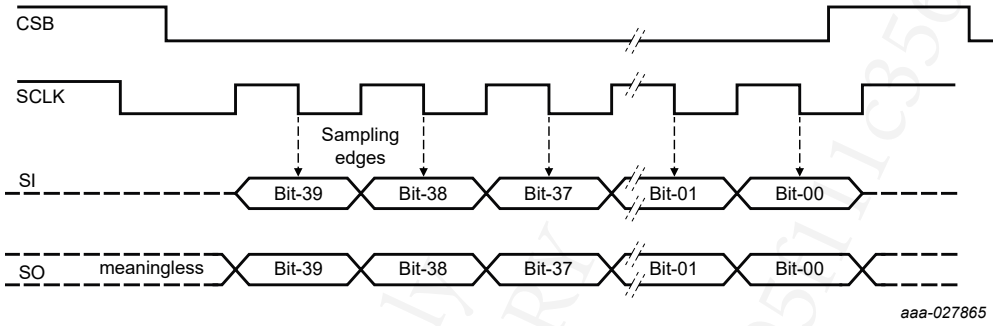


Figure 51. SPI transmission

The MC33774A decodes the SPI message with the rising edge of the chip select (CSN_RXTXLN) pin. The clock polarity is active HIGH (idles LOW). The rising edge on SCLK changes data bits, with the falling edge data bits are sampled (valid). The MC33774A responds to a received command with the next transmission.

The MC33774A accepts read requests for more registers than the actual data length. NOP messages allow the device to send pending data. If the device has no data anymore to send, it responds with all remaining bits logic 0. Other commands than NOP commands cancel the transmission of pending data. To write commands, the device responds with all bits logic 0.

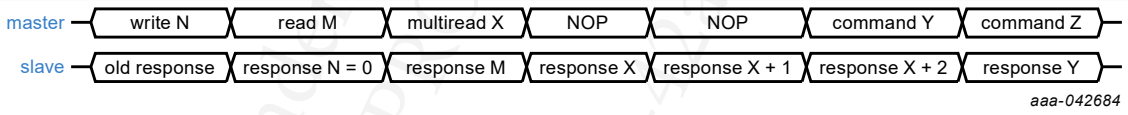


Figure 52. Bus traffic example

Change of the data length of the SPI frames is allowed. However, the user must ensure that pending responses fit the SPI frame length. Otherwise, a response frame error is generated.

7.9.4 Microcontroller interface monitoring

The microcontroller interface facilitates several diagnostics and monitoring functionalities. They are explained in the following sections.

7.9.4.1 Communication error counter

If any communication issue (FRAMEERR, CRCERR, RSPLENERR) is detected, the communication error counter FEH_COM_FLT_STAT.COMERRCNT increases by one. A write to the FEH_COM_FLT_STAT.COMERRCNT with any data unequal to 00h resets the counter.

7.9.4.2 Error counter overflow

In case the communication error counter is maxed out, the communication error counter stays at the maximum value, and the bit FEH_COM_FLT_STAT.ERRCNTOF is set. A write to the bit with logic 1 clears the FEH_COM_FLT_STAT.ERRCNTOF bit.

Application usage: An error counter overflow can be used to trigger a power-on reset of the device.

7.9.4.3 Response errors

Response errors can only occur when the MC33774A is used with SPI communication. In case the length of an SPI frame does not match the length of the response frame to be transmitted, the CRC bit field is not at the end of the message. This error is signaled with the bit FEH_COM_FLT_STAT.RSPLENERR and FEH_COM_FLT_STAT.COMERRCNT is increased. A write to the bit with logic 1 clears the FEH_COM_FLT_STAT.RSPLENERR bit.

7.9.4.4 Communication timeout

In case the device does not receive or transmit a valid message for a time longer than set in SYS_COM_TO_CFG.COMTO a communication timeout error is generated. The bit FEH_COM_FLT_STAT.COMTO is set and FEH_COM_FLT_STAT.COMERRCNT is increased. The further reaction of the MC33774A depends on the configuration in the event handling. A write to the bit with logic 1 clears the FEH_COM_FLT_STAT.COMTO bit.

The bit field SYS_COM_TO_CFG.COMTODISABLE allows disabling the communication timeout. Disabling of the communication timeout is only allowed for development purposes.

7.9.4.5 CRC error

The MC33774A checks all messages it receives for a correct CRC. In case the device detects an invalid CRC for the received message a CRC error is generated. The bit FEH_COM_FLT_STAT.CRCERR is set and FEH_COM_FLT_STAT.COMERRCNT is increased. A write to the bit with logic 1 clears the FEH_COM_FLT_STAT.CRCERR bit.

7.9.4.6 Frame error

The MC33774A checks all messages for a valid frame length. Frames with 64 bit, 80 bit, 96 bit, and 112 bit are accepted. In case the device detects an invalid frame a frame error is generated. The bit FEH_COM_FLT_STAT.FRAMEERR is set and FEH_COM_FLT_STAT.COMERRCNT is increased. A write to the bit with logic 1 clears the FEH_COM_FLT_STAT.FRAMEERR bit.

7.9.4.7 Access error

An access error is detected when a non-existing register is accessed. For the access, it does not matter if it is read or write. Write into read only, or read of write-only registers do not trigger an access error. If an access error occurs for a read request, the device responds with a regular response frame. REGADD[13:0] contains the error indicator 3FFFh. DATA[0] contains the address where the access error was triggered. Bit 15 and bit 14 of DATA[0] are set to 00b. Data padding for access errors is done with 8000h instead of 0000h.

If the access error occurs within a response message to a multiread command, the device provides the readable content until the frame is sent, in which the access error occurs. The frame with the access error contains in DATA[0] the address in which the error occurred. Subsequent frames contain in DATA[0] the address that this frame would use. Access error frames are sent, independent whether the frame would use accessible or non-accessible content, until the requested number of messages is sent. Figure 53 shows the behavior of the MC33774A in case an access error occurs during a multiread command.

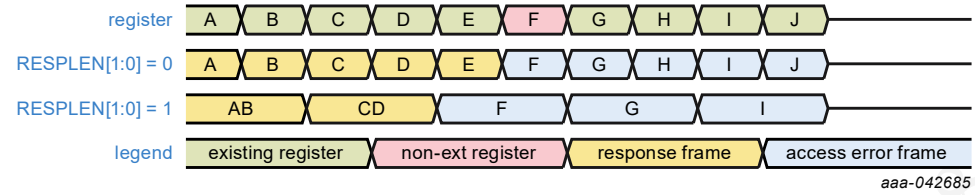


Figure 53. Access error

The register FEH_ACC_ERR contains information about the type of the last access error and the register addressed during this access.

Note: *An access error does not increment the communication error counter.*

7.9.4.8 Response of the device to communication errors

When an error in the communication to the MC33774A is detected (FRAMEERR, CRCERR, RSPLENERR), the message is discarded. The MC33774A does not send a response to this command.

7.9.5 Microcontroller interface related registers

The most important registers for the microcontroller interface and the related content are shown in Table 32.

Table 32. Microcontroller interface related registers

Register	Content
FEH_COM_FLT_EVT_CFG (Section 12.1.41)	communication faults events
FEH_COM_FLT_POR_CFG (Section 12.1.37)	reset due to communication faults
FEH_COM_FLT_STAT (Section 12.1.33)	communication errors
SYS_COM_TO_CFG (Section 12.1.3)	communication timeout configuration
SYS_COM_CFG (Section 12.1.2)	communication configuration

8 Limiting values

Table 33. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{BAT}	VBAT voltage		-0.3	-	84	V
$V_{i(CTn)}$	Cell terminal input voltage (CTn) (n=0 to 15)		-0.3	-	(n+1) * 5	V
$V_{i(CTn)}$	Cell terminal input voltage (CTn) (n=16 to 18)		-0.3	-	84	V
$V_{dif(CT)}$	Cell terminal input differential voltage		-5	-	10	V
$I_{i(CTn)}$	cell terminal input current	open load detection disabled	-500	-	500	nA
$V_{i(CBn)}$	Cell terminal balance input voltage (CBn) (n=0 to 15)		-0.3	-	(n+1) * 5	V
$V_{i(CBn)}$	Cell terminal balance input voltage (CBn) (n=16 to 18)		-0.3	-	84	V
$V_{i(dif)bal}$	balancing input differential voltage		-4.5	-	12.5	V
$I_{i(bal)}$	input current on balancing pins		-	-	330	mA
V_{DDA}	VDDA voltage		-0.3	-	1.65	V
V_{DDC}	VDDC voltage		-0.3	-	5.5	V
V_{DDIO}	VDDIO voltage		-0.3	-	5.5	V
V_{AUX}	VAUX voltage		-0.3	-	4	V
V_{GPIOx}	GPIOx voltage		-0.3	-	VDDC + 0.5	V
V_{AINA}	AINA and $ALARM_{OUT}$ voltage		-0.3	-	VDDC + 0.5	V
$V_{bus(TPL)}$	voltage on TPL communication bus pins	Relative to VSSC	-27	-	40	V
$V_{i(IMONVDDC)}$	input voltage on IMON_VDDC pin		-0.3	-	7	V
$V_{i(DRIVEVDDC)}$	input voltage on DRIVE_VDDC pin		-0.3	-	7	V
Thermal maximum ratings						
T_j	junction temperature		-40	-	165	°C
T_{stg}	storage temperature		-55	-	150	°C
$T_{reflow(peak)}$	peak package reflow temperature	Pin soldering temperature limit is for 30 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause a malfunction or permanent damage to the device.	-	-	260	°C
ESD ratings						
V_{ESD1}	electrostatic discharge voltage	At any pin; human body model (HBM): according to AEC-Q100-002 (100 pF, 1.5 kΩ)	−2	-	+2	kV
V_{ESD2}	electrostatic discharge voltage	At pin VBAT, CTx, CBx, VDDIO, VDDC, CSN_RXTXLN, RXTXLP,	−4	-	+4	kV

Table 33. Limiting values...*continued*

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
		MOSI_RXTXHP, SCLK_ RXTXHN, GPIOx, AINA_ ALARMOUT, VAUX, ; HBM: according to AEC-Q100-002 (100 pF, 1.5 kΩ); against all GNDs shorted together				
V_{ESD3}	electrostatic discharge voltage	At all pins; charged device model (CDM): according to AEC-Q100-011 (field induced charge; 4 pF)	−500	-	+500	V
V_{ESD4}	electrostatic discharge voltage	At corner pins; CDM: according to AEC-Q100-011 (field induced charge; 4 pF)	−750	-	+750	V
V_{ESD5}	electrostatic discharge voltage	At pin VBAT, CTx, CBx, VDDIO, VDDC, VSSC, CSN_ RXTXLN, RXTXLP, MOSI_ RXTXHP, SCLK_RXTXHN, GPIOx, AIINA_ALARMOUT, VAUX, VSSA, GNDFLAG; according to IEC 61000-4-2, unpowered (150 pF, 330 Ω) with recommended ESD capacitors as in section application information - with floating ground	−8	-	+8	kV
V_{ESD6}	electrostatic discharge voltage	At pin VBAT, CTx, CBx, VDDIO, VDDC, VSSC, CSN_RXTXLN, RXTXLP, MOSI_RXTXHP, SCLK_RXTXHN, GPIOx, AIINA_ ALARMOUT, VAUX, VSSA, GNDFLAG; according to ISO-10605, unpowered (150 pF, 330 Ω) with recommended ESD capacitors as in section application information - with ground referenced	−8	-	+8	kV
V_{ESD7}	electrostatic discharge voltage	At pin VBAT, CTx, CBx, VDDIO, VDDC, VSSC, CSN_RXTXLN, RXTXLP, MOSI_RXTXHP, SCLK_RXTXHN, GPIOx, AIINA_ ALARMOUT, VAUX, VSSA, GNDFLAG; according to ISO-10605, unpowered (150 p F, 2 kΩ) with recommended ESD capacitors as in section application information - with ground referenced	−8	-	+8	kV
V_{ESD8}	electrostatic discharge voltage	At pin VBAT, CTx, CBx, VDDIO, VDDC, VSSC, CSN_RXTXLN, RXTXLP, MOSI_RXTXHP, SCLK_RXTXHN, GPIOx, AIINA_ALARMOUT, VAUX, VSSA, GNDFLAG; according to ISO-10605, powered (330 p F, 2 kΩ) with recommended ESD capacitors as in section application information - with ground referenced	−8	-	+8	kV

9 Thermal characteristics

Table 34. Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Rth_{ja}	Junction to ambient natural convection four layer board (2s2p)	Ta = -40 .. 125°C	-	-	27	K/W
Rth_{jc}	Junction to case bottom (exposed pad)	Ta = -40 .. 125°C	-	-	1	K/W

10 Characteristics

Table 35. Characteristics

Vbat = 9 V to 81 V; Ta= -40 °C to +125 °C; Tj = -40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat= 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VBAT						
V_{BAT}	VBAT operating range		9	-	81	V
$V_{BAT(th)uv}$	VBAT undervoltage threshold		7	8	9	V
$V_{BAT(th)lv}$	VBAT low-voltage (LV) threshold	FP and FPC modes and LP mode with cell balancing	10.5	12	13.5	V
$V_{BAT(th)ov}$	VBAT overvoltage threshold		81	-	83	V
$\Delta V_{max1(VBAT\text{-}upperCT)}$	Maximum voltage difference 1 between battery supply voltage and pin CT18 or highest CTn	V_{bat} = 35 V to maximum supply voltage	-2.1	-	2.5	V
$\Delta V_{max2(VBAT\text{-}upperCT)}$	Maximum voltage difference between battery supply voltage and pin CT18 or highest CTn	V_{bat} = 9 V +1.5 V to 35 V	-1.5	-	2	V
Current consumption						
$I_{BAT(ULP)}$	IBAT current in deep Sleep mode	T_j up to 125 °C	-	-	19	µA
$I_{BAT(LP)}$	IBAT current in Sleep mode	T_j = -40°C to 125°C balancing disabled	-	-	115	µA
$\sigma_{IBAT(nom)}$	Nominal current variance of IBAT	Sleep mode without cell balancing.IC at the same temperature.same device configuration.	-	-	10	µA
$I_{BAT(add)LP}$	Additional IBAT current in Sleep mode due to balancing	Sleep mode with balancing enabled	-	-	2.9	mA
$I_{BAT(FP)}$	Full Power mode current consumption measuring all cell voltages and auxiliary inputs.	Ta = -40 °C to 125 °C No external load. No cell balancing. No communication.	-	-	14.9	mA
$I_{BAT(FPC)2}$	Cyclic mode current consumption measuring all cell voltages, primary auxiliary inputs, and module voltage.	Ta = -40 °C to 125 °C No secondary measurement No balancing No external current consumption. No communication.	-	-	12.3	mA
$I_{BATCB(FPC)}$	IBAT additional current in Active or Cyclic mode	All cell balancing enabled.	-	-	700	uA
$\Delta I_{BAT(FP)}$	IC to IC operating current imbalance	Ta = -40 °C to 125 °C, Vbat = 45 V, Ta and Vbat are the same for both ICs, Active mode / all ADCs running No balancing operation. No communication. No external load	-	-	400	µA
VDDA						
V_{DDA}	VDDA voltage		1.5	1.55	1.6	V
$I_{lim(VDDA)}$	Current limit of VDDA		-	-	12	mA
$t_{startup(VDDA)}$	VDDA startup time	Cload=100 nF	-	-	50	µs
$V_{DDA(th)uv}$	VDDA undervoltage threshold		1.36	1.4	1.44	V
$V_{DDA(th)ov}$	VDDA overvoltage threshold		1.65	1.7	1.75	V
VAUX						

Table 35. Characteristics*...continued*

Vbat = 9 V to 81 V; Ta= -40 °C to +125 °C; Tj = -40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat= 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{AUX}	VAUX output voltage		3.19	3.3	3.41	V
I_{VAUX}	VAUX external current capability		-	-	5	mA
$I_{lim(VAUX)}$	Current limit of VAUX		-	-	12	mA
$t_{startup(VAUX)}$	VAUX startup time	1 KΩ load,100 nF ext cap	-	-	200	µs
$V_{AUX(th)uv}$	VAUX undervoltage threshold		2.88	3.0	3.12	V
$V_{AUX(th)ov}$	VAUX overvoltage threshold		3.5	3.65	3.8	V
VDDC						
V_{DDC}	VDDC output voltage		4.85	5.0	5.15	V
I_{VDDC}	External VDDC current drive capability	Ta = –40 °C to 125 °C	-	-	15	mA
$t_{startup(VDDC)}$	Startup time of VDDC	14 Ω sense resistor 5 mA load and 470 nF capacitor	-	-	400	µs
$I_{out(DRIVE\_VDDC)}$	Driver output current (base current)		-60	-	300	uA
$V_{DDC(th)uv}$	VDDC undervoltage threshold		4.51	4.65	4.79	V
$V_{DDC(th)ov}$	VDDC overvoltage threshold		5.2	5.35	5.5	V
$V_{sense(VDDC)hc}$	Sense voltage of VDDC high current event		167	190	213	mV
$V_{trig(VDDC)oc}$	Trigger voltage of VDDC overcurrent event		264	300	336	mV
VDDIO						
$V_{DDIO(th)uv}$	VDDIO undervoltage threshold		2.96	3.03	3.1	V
$V_{DDIO(th)ov}$	VDDIO overvoltage threshold		5.25	5.375	5.5	V
Internal temperature measurement						
$T_{j(meas)}$	IC temperature measurement range		-45	-	155	°C
$\Delta T_{j(meas)}$	IC temperature measurement error	Range to be measured is -40 °C to 150 °C	-3	-	3	°C
Overtemperature protection						
$T_{sd(th)}$	Shutdown temperature threshold	Of VPRE regulator	160	-	175	°C
Mode switching						
$t_{wake(com)}$	Maximum wake-up to communication time	Measured from start of wake-event.	-	-	2.4	ms
$t_{sw(act-Sleep)}$	Switching time from Active mode to Sleep mode		-	-	0.3	ms
$t_{sw(act-deepsleep)}$	Switching time from Active mode to deep Sleep mode		-	-	0.3	ms
$t_{sw(act-cyc)}$	Switching time from Active mode to Cyclic mode		-	-	0.3	ms
$t_{wait(cyc-soc)}$	Waiting time between entering in Cyclic mode and start of conversation		5	-	-	ms
$t_{sw(cyc-act)}$	Switching time from Cyclic mode to Active mode		-	-	0.8	ms

Table 35. Characteristics*...continued*

Vbat = 9 V to 81 V; Ta= -40 °C to +125 °C; Tj = -40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat= 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{sw(cyc-sleep)}$	Switching time from Cyclic mode to Sleep mode	After completion of the measurement.	-	-	0.3	ms
$t_{sw(sleep-act)}$	Switching time from Sleep mode to Active mode		-	-	2.1	ms
$t_{sw(sleep-cyc)}$	Switching time from Sleep mode to Cyclic mode		-	-	1.6	ms
$t_{startup(deepsleep-act)}$	Start-up time from Deep Sleep mode to Active mode		-	-	2.1	ms
$t_{wake(cyc)res}$	Cyclic mode wake-up time resolution		93	100	107	ms
$\alpha_{wake(cyc)}$	Cyclic mode wake-up time accuracy		-7	-	7	%
$t_{max(Cwu)}$	Maximum Cyclic mode wake-up timer period		6094	6553	7012	s
BIST						
$t_{check(fr)BIST}$	Frame check time for BIST	from setting FEH_MON_BIST_ CTRL.STARTBIST until final results available	-	-	500	µs
Measurement resolution						
$V_{meas(res)VBAT}$	Measured voltage resolution		-	3.128	-	mV/LSB
$V_{meas(res)}$	Measured voltage resolution		-	154	-	µV/LSB
$T_{meas(res)}$	Primary and secondary measured temperature resolution		-	32.4	-	mK/LSB
$V_{meas(res)(supply)}$	Supply voltage measurement resolution (VAUX, VDDC)		-	308	-	uV/LSB
$V_{meas(res)(vdda)}$	Supply voltage measurement resolution (VDDA)		-	154	-	uV/LSB
VREF limits						
$N_{limit(VREF)}$	Limits for reference voltages during fault-free operation	PRMM_PER_SECVREF and SECM_PER_PRMVREF	6577h	-	65A9h	LSB
Cell terminal leakage						
$I_{L(absdyn)}$	Dynamic absolute leakage current	absolute cell voltage measurement pin current leakage during measurement sequenceCBautopause =10ms	-130	-	130	nA
$I_{L(difdyn)}$	Dynamic differential leakage current	differential cell voltage measurement pin current leakage during measurement sequenceCBautopause = 10ms	-25	-	25	nA
Cell voltage measurement accuracy for primary measurement - begin of life						
$V_{err(meas)(LPF1)}$	Measurement error voltage (LFP1)	VC_x = 0 V to 3.7 V; T_j = −40 °C to +105 °C	-1	-	1	mV
$V_{err(meas)(LFP2)}$	Measurement error voltage (LFP2)	VC_x = 0 V to 3.7 V; T_j = −40 °C to +125 °C	-1.2	-	1.2	mV
$V_{err(meas)(NMC1)}$	Measurement error voltage (NMC1)	VC_x = 0 V to 4.5 V; T_j = −40 °C to +105 °C	-1.3	-	1.3	mV

Table 35. Characteristics*...continued*

Vbat = 9 V to 81 V; Ta= -40 °C to +125 °C; Tj = -40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat= 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{err(meas)(NMC2)}$	Measurement error voltage (NMC2)	VC_x = 0 V to 4.5 V; T_j = −40 °C to +125 °C	-1.5	-	1.5	mV
$V_{err(meas)(FULL1)}$	Measurement error voltage (FULL1)	VC_x = −3 V to +5 V; T_j = −40 °C to +150 °C	-7	-	7	mV
$V_{err(meas)(FUL1B)}$	Measurement error voltage (FULL1B)	VC_x = −5 V to −3 V; T_j = −40 °C to +150 °C	−12	-	12	mV
Cell voltage measurement accuracy for primary measurement - end of life						
$V_{err(meas)(LFP3)}$	Measurement error voltage (LFP3)	VC_x = 0 V to 3.7 V; T_j = −40 °C to +125 °C	−1.5	-	1.5	mV
$V_{err(meas)(NMC3)}$	Measurement error voltage (NMC3)	VC_x = 0 V to 4.5 V; T_j = −40 °C to +125 °C	−2.0	-	2.0	mV
$V_{err(meas)(FULL2)}$	Measurement error voltage (FULL2)	VC_x = −3 V to +5 V; T_j = −40 °C to +150 °C	−10	-	10	mV
Cell voltage measurement accuracy for secondary measurement - begin of life						
$V_{err(meas)(LFP4)}$	Measurement error voltage (LFP4)	VB_x = 0 V to 3.7 V; T_j = −40 °C to +105 °C	-1.7	-	1.7	mV
$V_{err(meas)(LFP5)}$	Measurement error voltage (LFP5)	VB_x = 0 V to 3.7 V; T_j = −40 °C to +125 °C	-4	-	4	mV
$V_{err(meas)(NMC4)}$	Measurement error voltage (NMC4)	VB_x = 0 V to 4.5 V; T_j = −40 °C to +105 °C	-2	-	2	mV
$V_{err(meas)(NMC5)}$	Measurement error voltage (NMC5)	VB_x = 0 V to 4.5 V; T_j = −40 °C to +125 °C	-4.5	-	4.5	mV
$V_{err(meas)(FULL3)}$	Measurement error voltage (FULL3)	VB_x = −3 V to +5 V; T_j = −40 °C to +150 °C	-7	-	7	mV
Cell voltage measurement accuracy for secondary measurement - end of life						
$V_{err(meas)(LFP7)}$	Measurement error voltage (LFP7)	VB_x = 0 V to 3.7 V; Tj = −40 °C to +105 °C	-2.7	-	2.7	mV
$V_{err(meas)(LFP6)}$	Measurement error voltage (LFP6)	VB_x = 0 V to 3.7 V; T_j = −40 °C to +125 °C	−5	-	5	mV
$V_{err(meas)(NMC7)}$	Measurement error voltage (NMC7)	VBx = 0 V to 4.5 V; Tj = −40 °C to +105 °C	-3	-	3	mV
$V_{err(meas)(NMC6)}$	Measurement error voltage (NMC6)	VB_x = 0 V to 4.5 V; T_j = −40 °C to +125 °C	−5.5	-	5.5	mV
$V_{err(meas)(FULL4)}$	Measurement error voltage (FULL4)	VB_x = −3 V to +5 V; T_j = −40 °C to +150 °C	−10	-	10	mV
Cell terminal noise						
$V_{n(meas)}$	Measurement noise voltage	sampling period = 16 scansT_j = 150 °C	-	-	300	μVRMS
Cell terminal open load detection						
$R_{open(prm)}$	Primary open load resistance		6.8	-	13.2	kΩ
$R_{sw(open)sec}$	Secondary cell voltage open-load mechanism switched impedance		13.8	-	26.2	kΩ
$M_{ratio(open)sec}$	Ratio between VBx measurement and actual voltage at VBx pin	CBOL switch closed; VC > 1.5 V	93.6	-	94.1	%

Table 35. Characteristics*...continued*

Vbat = 9 V to 81 V; Ta= -40 °C to +125 °C; Tj = -40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat= 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Measurement acquisition						
$N_{s(PI)}$	Number of periodic integrator samples		16	-	511	
$N_{s(AI)}$	Number of application integrator samples		16	-	65534	
Measurement timing						
$t_{appmeas}$	Application measurement time	application result availability after capture command	-	-	265	µs
$t_{d(prm-start)meas}$	Delay time from global primary measurement enable to measurement start		-	-	100	µs
$t_{d(sec-start)meas}$	Delay time from secondary measurement enable to measurement start		-	-	100	µs
$t_{autopause(prog)}$	Programmable autopause time		10	-	160000	µs
$t_{autopause(acc)}$	Autopause timer accuracy		-5	-	5	%
$t_{autopause(res)}$	Autopause time resolution		-	10	-	µs
$T_{s(meas)}$	Measurement sampling period		16.15	17	17.85	µs
$t_{sync(meas)}$	Measurement synchronization time	from any cell to any cell	129.2	136	142.8	µs
VBAT measurement accuracy						
$V_{I(acc)VBAT}$	Measured voltage minimum accuracy	Tj = -40 °C to 115 °C, VBAT >= 17 V at pin VBAT (wo Rvbat)	-50	-	50	mV
$\Delta V_{I(meas)VBAT}$	Measured Voltage Max Relative Error	Tj = -40 °C to 115 °C, VBAT >= 17 V at pin VBAT (wo Rvbat)	-	-	0.3	%
VBAT measurement noise						
$V_{n(VBAT)(RMS)}$	Measurement noise	Sampling period = 16 scan samples, Tj = 150 °C	-	-	10	mVrms
Balancing						
I_{bal}	Balancing current	T_j =-40°C to 150°C, R_{bal} = 10 to 450 Ω,no external load current, 50% duty cycle max	0	-	300	mA
$I_{lim(bal)}$	Balancing current limit	Tj = -40°C to 150°C	310	-	800	mA
$R_{sw(bal)}$	Balancing switch resistance	T_j = -40°C to 150°CV_{bat} = 9 V to 81V, 4 to 18 cells	-	-	1.1	Ω
$V_{th(fault)Bal}$	Output fault detection voltage threshold	T_j = -40 °C to +150 °C	0.25	-	0.65	V
$I_{L(CBx)}$	CBx leakage current	Tj= -40...85°C,0<VCBx+1 - VCBx<5,ULP mode	-500	-	500	nA
$I_{L(CBx)}$	CBx leakage current	Tj= -40...150°C,0<VCBx +1 - VCBx<5,ULP and LP mode,Balancing disabled	-2	-	2	µA
$I_{L(CBx)3}$	CBx input leakage current	Tj = -40 °C...150 °C,-3<VCBx+1 - VCBx<5,All modes,Balancing disabled	-10	-	10	µA

Table 35. Characteristics...*continued*

Vbat = 9 V to 81 V; Ta= -40 °C to +125 °C; Tj = -40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat= 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$T_{th(act)otp}$	overtemperature protection activation threshold	threshold for primary temperature measurement to stop balancing	-	3254h	-	LSB
$T_{th(rel)otp}$	overtemperature protection release threshold	threshold for primary temperature measurement to restart balancing	-	3010h	-	LSB
Balancing timings						
$t_{r(bal)}$	Balancing rise time	T_j = -40 °C to +150 °CR_{bal} = 5 Ω	1	-	100	µs
$t_{f(bal)}$	Balancing fall time	T_j = -40°C to 150°C, R_{bal} = 15 Ω,from last $bal_{chcfg.chenx}$ bit falling edge or $bal_{globcfg.balen}$ bit falling edge, no fatal fault	1	-	100	µs
$t_{d(bal)}$	Balancing delay time	T_j = -40 °C to +150 °CRBal = 5 Ω	-	-	150	µs
$t_{gbal(max)}$	Maximum global balancing time		609475,5	655350	701224.5	s
$t_{gbal(res)}$	Global balancing time resolution		-	-	10	s
$t_{gbal(acc)}$	Global balancing time accuracy	T_j = -40°C to +150°C	-7%	-	7%	
$t_{gprebal(max)}$	Maximum global pre-balancing time		609475	655350	701225	s
$t_{gprebal(res)}$	Global pre-balancing time resolution		-	-	10	s
$t_{gprebal(acc)}$	Global pre-balancing time accuracy		-7%	-	7%	
$t_{ibal(max)}$	Maximum individual balancing time		163830	-	-	s
$t_{ibal(res)}$	Individual balancing time resolution		-	-	10	s
$t_{ibal(acc)}$	Individual balancing time accuracy	T_j = -40°C to + 150°C [1]	-7% of (programmed period – 10 s)	-	7% of (programmed period – 10 s)	
δ_{PWM}	Pulse width modulation (PWM) duty cycle		0	-	100	%
$\delta_{PWM(res)}$	Pulse width modulation (PWM) duty cycle resolution		$1/2^8$	-	-	%
$f_{PWM(bal)}$	Pulse width modulation (PWM) balancing frequency		-	2	-	Hz
Analog inputs						
$V_{meas(aux)(abs)}$	Auxiliary input measured voltage (absolute value)		0	-	5	V
$V_{meas(ratiom)VAUX}$	Auxiliary input measured voltage (ratiometric value)	VAUX voltage used by external circuitry connected to AINx pins	0	-	VAUX * 0.975	V
$V_{meas(ratiom)VDDC}$	Auxiliary input measured voltage (ratiometric value)	VDDC voltage used by external circuitry connected to AINx pins	0	-	V_{VDDC} * 0.975	V
$E_{G(abs)1}$	Absolute gain error 1	T_j = -40 °C to +115 °C	-0.15	-	0.15	%
$E_{G(abs)2}$	Absolute gain error 2	T_j = -40 °C to +150 °C	-0.2	-	0.2	%
$V_{err(offset)(abs)}$	Absolute offset error voltage	T_j = -40 °C to +150 °C	-3	-	3	mV

Table 35. Characteristics...*continued*

Vbat = 9 V to 81 V; Ta= -40 °C to +125 °C; Tj = -40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat= 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$E_{T(meas)ratiom1}$	Ratiometric measurement total error 1	T_j = -40 °C to +115 °C	-0.006 - 0.15% * V_{AINx}	-	0.006 + 0.15% * V_{AINx}	V
$E_{T(meas)ratiom2}$	Ratiometric measurement total error 2	T_j = -40 °C to +150 °C	-0.006 - 0.25% * V_{AINx}	-	0.006 + 0.25% * V_{AINx}	V
$V_{n(meas)RMS}$	RMS measurement noise voltage	Sampling period = 16 scan samples,Tj = 150degC	-	-	350	µV
$V_{meas(res)(abs)}$	Measured voltage resolution	Absolute measurement (absolute reference voltage)	-	154	-	µV/LSB
$V_{meas(res)(ratiom)}$	Measured voltage resolution	Ratiometric measurement (VAUX or VDDC)	-	3.05176 x 10^{-3}	-	% / LSB
GPIO						
$V_{OH(GPIO)}$	Output logic high voltage on GPIO pins	I_{GPIO} = 1 mA Including routing and all GPIOs / I^2C driving at the same time.	V_{VDDC} - 0.4V	-	V_{VDDC}	-
$V_{OL(GPIO)}$	Output logic low voltage on GPIO pins	I_{GPIO} = 1 mA Including routing and all GPIOs / I^2C driving at the same time.	-	-	0.4	V
$I_{OH(tot)GPIO}$	Total HIGH-level output current on GPIO pins		-	-	8	mA
$I_{OL(tot)GPIO}$	Total LOW-level output current on GPIO pins		-	-	20	mA
$V_{IL(GPIO)}$	Input logic low voltage on GPIO pins		-	-	0.8	V
$V_{IH(GPIO)}$	Input logic high voltage on GPIO pins		2.0	-	-	V
$V_{hys(GPIO)}$	Input hysteresis voltage on GPIO pins		0.15	-	1.0	V
$V_{IL(wake)GPIO}$	Input logic low wake-up voltage on GPIO pins		-	-	0.8	V
$V_{IH(wake)GPIO}$	Input logic high wake-up voltage on GPIO pins		2.5	-	-	V
$V_{hys(wake)GPIO}$	Input hysteresis wake-up voltage on GPIO pins		0.03	-	1.2	V
$t_{deglitch(GPIO)}$	Deglitch time on GPIO pins (not for wake up and alarm)		3.81	-	5.6	µs
$I_{L(GPIO)}$	Leakage current on GPIO pins	GPIO0 and GPIO1	-	-	100	nA
$I_{L(GPIO)}$	Leakage current on GPIO pins	GPIO2 to GPIO7, VDDC Active.	-	-	100	nA
GPIO Diagnostics						
$R_{OL(GPIO)}$	GPIO openload diagnostic resistance		6.8	10	13.2	kΩ
Wake pin						
$t_{deglitch(GPIO0)wake}$	Wake-up time of deglitch function on pin GPIO0		50	80	100	µs
ALARM						

Table 35. Characteristics...*continued*

Vbat = 9 V to 81 V; Ta= -40 °C to +125 °C; Tj = -40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat= 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{alarm(deglitch)GPIO1}$	Alarm time of deglitch filter on GPIO1 pin		93	-	118.27	µs
$t_{heartbeat(IH)}$	Heartbeat input high time	if ALARMINHBINV = 0, then heartbeat input high time; if ALA RMINHBINV = 1, then heartbeat input low time	360	-	640	µs
$t_{heartbeat(IL)}$	Heartbeat input low time	ALARMINHB = T_{500u}	360	-	640	µs
$t_{heartbeat(IL)}$	Heartbeat input low time	ALARMINHB = T_{1ms}	830	-	1180	µs
$t_{heartbeat(IL)}$	Heartbeat input low time	ALARMINHB = T_{10ms}	9240	-	10860	µs
$t_{heartbeat(IL)}$	Heartbeat input low time	ALARMINHB = T_{100ms}	93350	-	107630	µs
$I_{O(source)alarm}$	Alarm line output source current	V_{VDDIO} = $V_{VDDC}$$V_{ALARM_OUT}$ = V_{VDDIO} - 0.8 V	2	-	-	mA
$I_{O(sink)alarm}$	Alarm line output sink current	V_{ALARM_OUT} = 0.8 V	2	-	-	mA
$I_{O(source)alarm}$	Alarm line output source current	V_{VDDIO} = V_{VDDC} V_{ALARM_OUT} = -0.4 V	1	-	-	mA
$I_{O(sink)alarm}$	Alarm line output sink current	V_{VDDIO} = $V_{VDDC}$$V_{ALRM_OUT}$ = 0.4 V	1	-	-	mA
$t_{heartbeat(OH)}$	Heartbeat output high time		460	-	540	µs
$t_{heartbeat(OL)}$	Heartbeat output low time	ALARMOUTHB = T_{500us}	460	-	540	µs
$t_{heartbeat(OL)}$	Heartbeat output low time	ALARMOUTHB=T_{1ms}	930	-	1080	µs
$t_{heartbeat(OL)}$	Heartbeat output low time	ALARMOUTHB=T_{10ms}	9340	-	10760	µs
$t_{heartbeat(OL)}$	Heartbeat output low time	ALARMOUTHB=T_{100ms}	93450	-	107530	µs
I^2C-bus interface						
$t_{to(I2C-bus)}$	I^2C-bus timeout time		35	-	55	µs
$V_{IL(I2C-bus)}$	I^2C-bus input logic low voltage		-	-	0.3 * V_{VDDIO}	V
$V_{IH(I2C-bus)}$	I^2C-bus input logic low voltage		0.7 * V_{VDDIO}	-	-	V
$V_{hys(I2C-bus)}$	I^2C-bus input hysteresis voltage		0.05 * V_{VDDIO}	-	-	V
$I_{I(I2C-bus)}$	Input current on I^2C pins	Only with VDDC/VDDIO ON.	-10	-	+10	µA
$C_{i(I2C-bus)}$	Input capacitance on I^2C pins		-	-	10	pF
$V_{OL(I2C-bus)}$	I^2C-bus output logic low voltage	$I_{OL\_I2C=}$ 5 mA, Including routing and all GPIOs / I2C driving at the same time.	-	-	0.4	V
$t_{f(o)I2C-bus}$	I^2C-bus output fall time from $V_{IH(min)}$ to $V_{IL(max)}$		0	-	120	ns
f_{SCL}	SCL clock frequency	bit $I2C_{CFG.CLKSEL}$ = 1 no clock stretching	0	-	100	kHZ
$t_{HD;STA}$	Hold time (repeated) START condition		4.0	-	-	µs
t_{LOW}	LOW period of the SCL clock std. mode		4.7	-	-	µs
t_{HIGH}	HIGH period of the SCL clock std. mode		4.0	-	-	µs

Table 35. Characteristics*...continued*

Vbat = 9 V to 81 V; Ta= -40 °C to +125 °C; Tj = -40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat= 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{LOW}	LOW period of the SCL clock fast mode		1.3	-	-	µs
t_{HIGH}	HIGH period of the SCL clock fast mode		0.6	-	-	µs
$t_{SU;STA}$	Set-up time for a repeated START condition		4.7	-	-	µs
$t_{SU;DAT}$	Data set-up time		250	-	-	ns
$t_{SU;STO}$	Set-up time for STOP condition		4.0	-	-	µs
C_{bus}	Capacitive load for each bus line		-	-	100	pF
$t_{VD;DAT}$	Data valid time std. mode		-	-	3.45	µs
$t_{VD;ACK}$	Data valid acknowledge time std. mode		-	-	3.45	µs
$t_{VD;DAT}$	Data valid time fast mode		-	-	0.9	µs
$t_{VD;ACK}$	Data valid acknowledge time fast mode		-	-	0.9	µs
Communication timings						
$t_{d(rec\text{-}trans)}$	Time between request received by the device and response transmitted		1.3	-	8	µs
$t_{d(TPL)}$	Time between two consecutive response message frames transmitted by the product		1.3	-	2.8	µs
$t_{to(EOM)}$	Time for end of message timeout	SOM symbol to EOM symbol	250	-	300	µs
$t_{d(req)MCU}$	Time between two requests transmitted by MCU		1.3	-	-	µs
$t_{d(Fd)}$	Forward delay time	Time required by a message to propagate from one port of the device to the other port of the same device; the delay is measured between SOM to SOM	-	0.5	1.7	µs
$t_{d(wake)}$	Time between two consecutive wake-up messages.		3	-	4	ms
$R_{data(TPL)}$	TPL data rate		1.9	-	2.1	Mbit/s
Communication timeout						
$t_{to(com)res}$	Communication time-out resolution		9.5	10	10.5	ms
$t_{to(com)min}$	Minimal communication time-out time		9.5	10	10.5	ms
$t_{to(com)max}$	Maximum communication time-out time		2422.5	2550	2677.5	ms
Communication (TPL)						
$I_{VDDC(TPL)wait}$	TPL current on VDDC, device in waiting state	2 RX ON,No TX	-	-	1.4	mA
$I_{VDDC(TPL)forward}$	TPL current on VDDC, device in forward state	1 RX ON,1 TX ON(TX averaged on bit period)	-	-	9.2	mA

Table 35. Characteristics*...continued*

Vbat = 9 V to 81 V; Ta= -40 °C to +125 °C; Tj = -40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat= 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$I_{VDDC(TPL)respond}$	TPL current on VDDC, device in responding state	NO RX, 2 TX ON(TX averaged on bit period)	-	-	17	mA
$V_{th(sleep-wake)dif}$	Differential receiver threshold voltage in deep Sleep mode or in Sleep mode to wake-up		1.15	-	-	V
$V_{th(full}$ power)dif	Differential receiver threshold voltage	Active mode $rising_{edge}$	0.48	-	0.68	V
$V_{hys(RX)dif}$	Differential receiver hysteresis voltage		70	-	130	mV
$V_{o(peak)dif}$	Differential peak output voltage	R_{ldiff} = 120 ΩV_{VDDC} > 4.85V V_{VDDC} < 5.15V	1.1	-	2.2	V
$R_{term(act)}$	Termination resistance in Active mode	IC configured in TPL mode and not in sleep states	85	120	175	Ω
$R_{term(sleep)}$	Termination resistance in sleep mode	In SPI mode and in deep sleep and sleep states	20	-	100	kΩ
Communication (SPI)						
$V_{IL(SPI)}$	SPI input low voltage on MOSI, CSN, SCLK pins		-	-	0.8	V
$V_{IH(SPI)}$	SPI input high voltage on MOSI, CSN, SCLK pins		2.0	-	VDDIO + 0.3	V
$V_{hys(SPI)}$	SPI input hysteresis voltage on MOSI, CSN, SCLK pins		30	-	600	mV
$V_{IH(wake)CSN}$	SPI input logic high wake-up voltage on CSN pin		2.5	-	-	V
$V_{IL(wake)CSN}$	SPI input logic low wake-up voltage on CSN pin		-	-	0.8	V
$V_{hys(wake)CSN}$	SPI input hysteresis wake-up voltage on CSN pin		30	-	1200	mV
$V_{OL(SPI)}$	SPI output logic low voltage on MISO pin	2 mA	-	-	0.4	V
$V_{OH(SPI)}$	SPI output logic high voltage on MISO pin	-2 mA	VDDIO - 0.4	-	-	V
f_{SPI}	SPI output logic high voltage on MISO pin		-	-	4.2	MHz
$t_{en(MISO)}$	MISO enable time		0	-	40	ns
$t_{dis(MISO)}$	MISO disable time		0	-	40	ns
$t_{v(data)MISO}$	MISO data valid after rising edge of SCLK		0	-	45	ns
$t_{d(data)transfer}$	Sequential data transfer delay time		1	-	-	µs
t_{SCLKH}	SCLK high time		90	-	-	ns
t_{SCLKL}	SCLK low time		90	-	-	ns
$t_{FALLSPI}$	SCLK, CSN, and MOSI fall time		-	-	15	ns
$t_{RISESPI}$	SCLK, CSN and MOSI rise time		-	-	15	ns
$t_{SETUPSPI}$	MOSI to SCLK falling edge setup time		20	-	-	ns

Table 35. Characteristics...*continued*

Vbat = 9 V to 81 V; Ta= -40 °C to +125 °C; Tj = -40 °C to +150 °C; all voltages are defined with respect to ground; positive currents flow into the IC. Typical values are given at Vbat= 72 V; Ta = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{HOLDSPI}$	MOSI to SCLK falling edge hold time		20	-	-	ns
CSN_{LEAD}	CSN lead time		100	-	-	ns
CSN_{LAG}	CSN lag time		100	-	-	ns
$SCLK_{SBL}$	SCLK stable before CSN low		40	-	-	ns
$SCLK_{SBH}$	SCLK stable after CSN high		40	-	-	ns
$t_{low(wake)}$	Minimum CSN low time before rising edge for wake-up		12	-	-	us

[1] Using balancing pause (PAUSEBAL) may impact the balancing time accuracy.

11 Application information

Figure 54 provides an application example for the MC33774A in a typical 18-cell battery application.

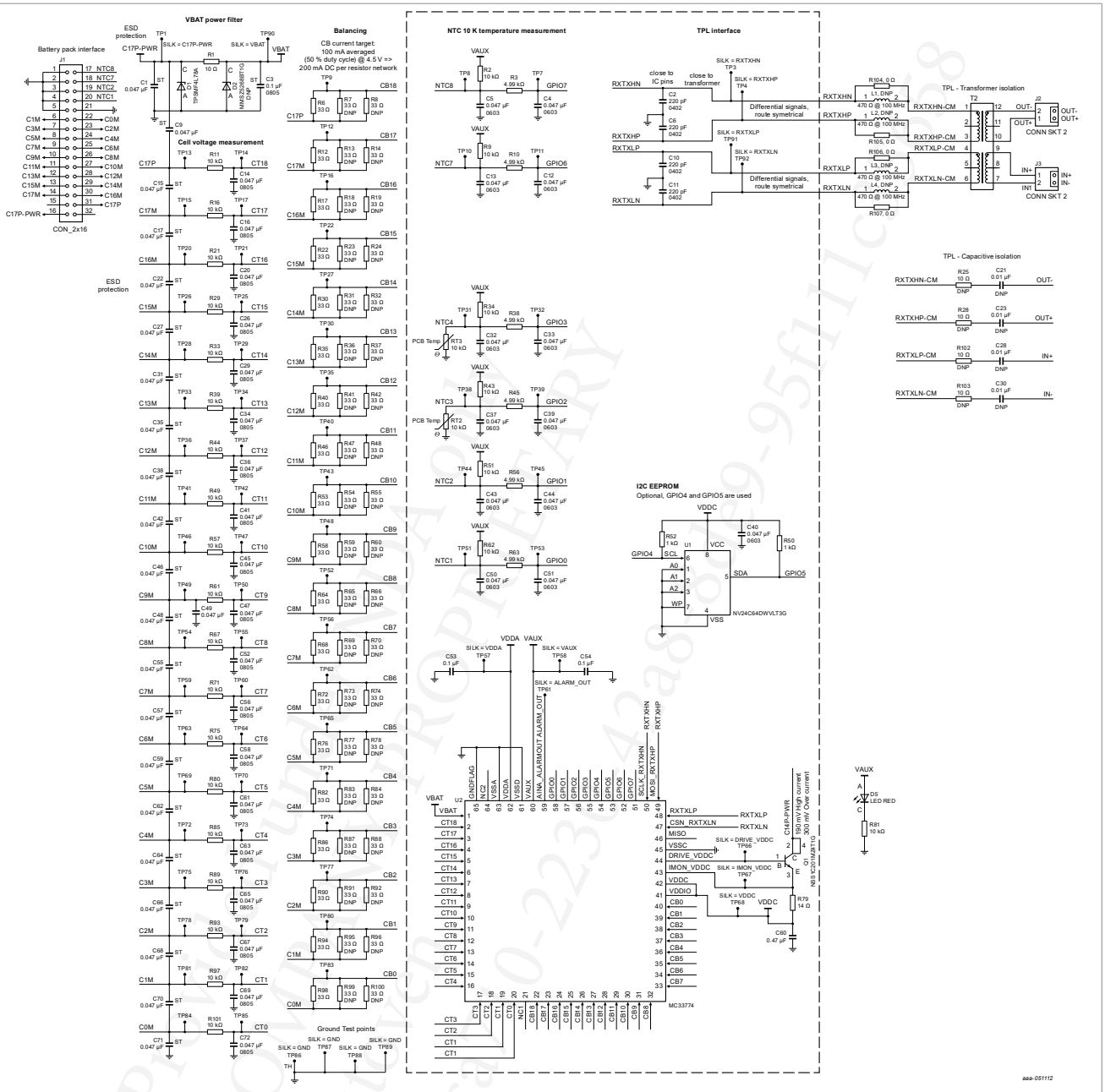


Figure 54. Typical application

11.1 Typical applications

11.1.1 External components

This section provides information about recommended external components and how to select them.

11.1.1.1 Power supplies

The recommended schematic to supply the MC33774A and enable voltages is described in Figure 55.

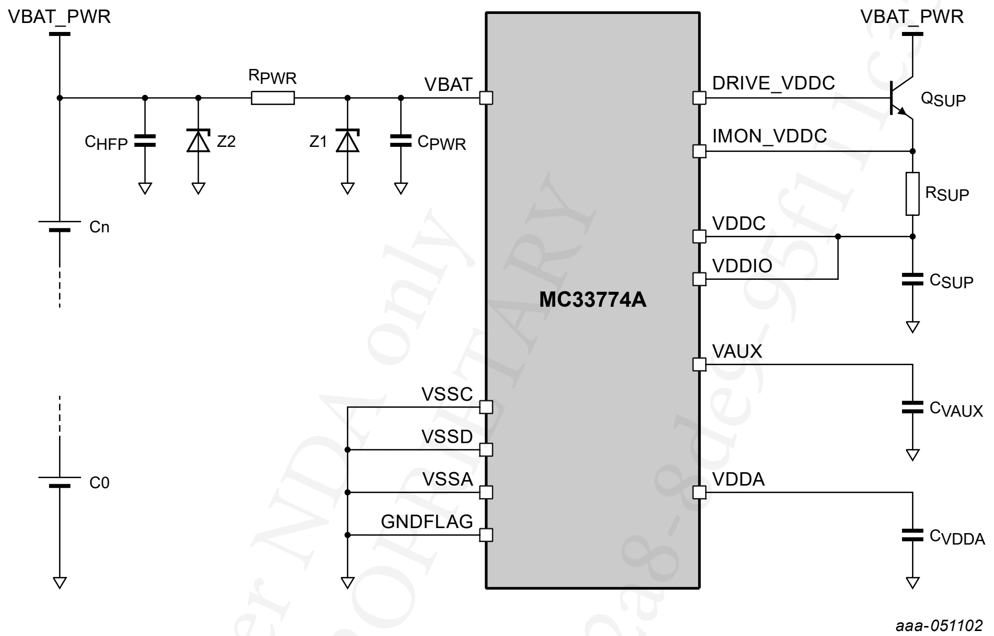


Figure 55. Supplies connection

The component values and comments are described in Table 36.

Table 36. Supply components

ID	Value	Units	Comment
C_{HFP}	0.047	μF	100 V capacitor; should not be changed to sustain ESD and hotplug.
R_{PWR}	10 / 0.1W	Ω	do not exceed to avoid excessive voltage drop between VBAT and CT18; Combined with C_{PWR} to filter noise above 160 kHz.
C_{PWR}	0.1	μF	100 V capacitor; should not be changed.
Z2			Optional: To sustain negative iso pulses; TPSMF4L78A or equivalent.
Z1			Optional: Overvoltage protection; use MMSZ5268BT1G or equivalent.
Q_{SUP}			Ballast NPN transistor; use NSS1C201MZ4T1G or equivalent; (Key parameters: Vce0 min = 100 V, Beta min = 50, Icb0 < 50 μA).
R_{SUP}	14	Ω	Optimal value for VDDC current sourcing and monitoring in TPL applications.
C_{SUP}	0.47	μF	25 V capacitor, should not be changed.
C_{VAUX}	0.1	μF	25 V capacitor, should not be changed.
C_{VDDA}	0.1	μF	25 V capacitor, should not be changed.

11.1.1.2 Cell terminal filters

Figure 56 shows the recommended cell terminal connections first order low-pass filters, cell balancing connections, and ESD protection capacitors.

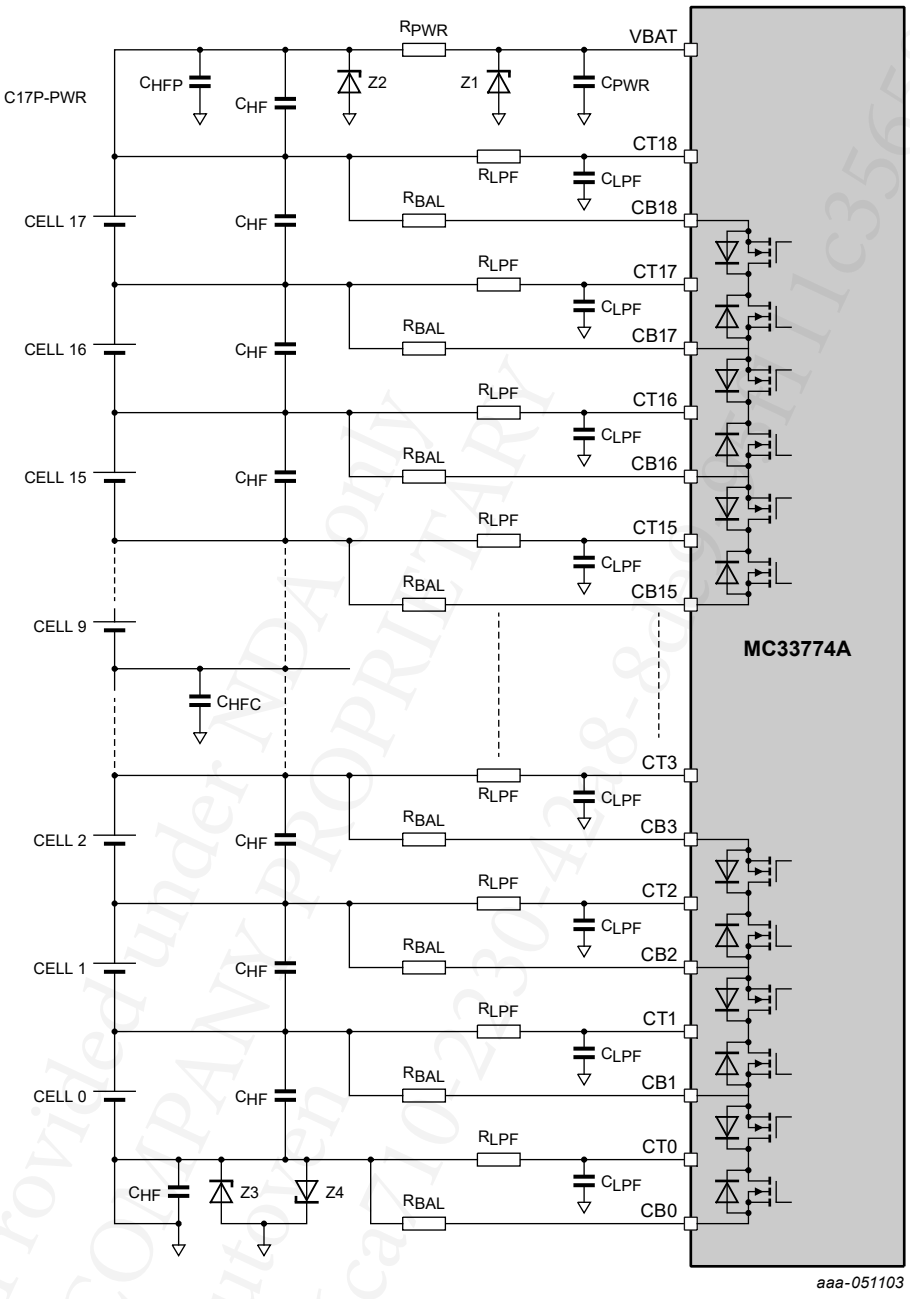


Figure 56. Cell terminal connections

The component values and comments are described in the table Table 37

Table 37. Cell terminal connection component values

ID	Value	Units	Comments
C_{HF}	0.047	µF	25 V capacitor; should not be changed to sustain ESD
C_{HFC}	0.047	µF	optional: 100 V common mode capacitor on Cell9M to improve EMC performances
R_{LPF}	10	kΩ	Should not be changed; Antialiasing filtering with C_{LPF} : fcut : 338 Hz (ten times below 4 kHz internal ADC sampling)
C_{LPF}	0.047	µF	100 V capacitor; should not be changed
R_{BAL}	X	Ω	Any value is possible if following cell balance current limits are not exceeded: 9 mA > I > 300 mA peak (Vcellmax / (2 x Rbal))
Z3, Z4			optional: Schottky diodes to improve EMC performances - for example, MBR0250LT1G

11.1.1.3 External cell balancing

External cell balancings can be implemented with external transistors to increase the total balancing current or shift the power dissipation out of the device toward external cell-balancing resistors. For one cell-balancing channel switched on, the total balancing current will be the sum of the currents through the internal (through 2xRbal) and external (through Rbalext) transistors. NMOS, PMOS, and BJT can be used in a similar way.

Figure 57 shows the principle of such implementation with an NMOSFET (Q) as external cell balancing transistor. The NMOSFET is switched on synchronously with the internal cell-balancing switches, when the voltage drop across Rbal reaches the NMOSFET Vgs threshold of the NMOSFET.

The maximum Vgs voltage equals Vcell/2. Low Vgs NMOSFET should be selected to ensure a good saturation at the desired current. The selected NMOSFET should be capable for the required cell balancing current, power dissipation, and also capable sustaining negative Vgs voltage when the adjacent cell-balancing channel is on.

The behavior is fully transparent for the application and does not require any specific software adaptation.

The user is in charge of selecting and validating the external transistors type, characteristics, external balancing resistors, and additional components to protect the transistor against electrical overstresses (for example, hotplug), depending on the user's application requirements.

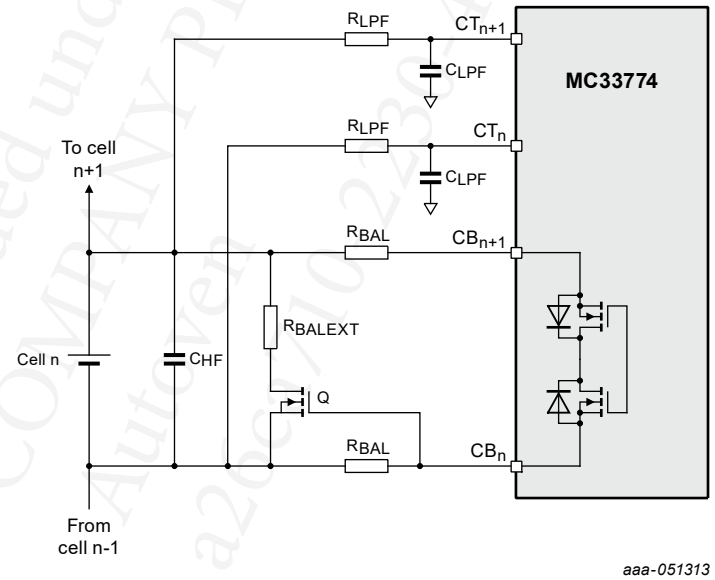


Figure 57. External cell balancing

11.1.1.4 Temperature channels

Figure 58 shows configuration of AINx inputs configured as temperature measurements

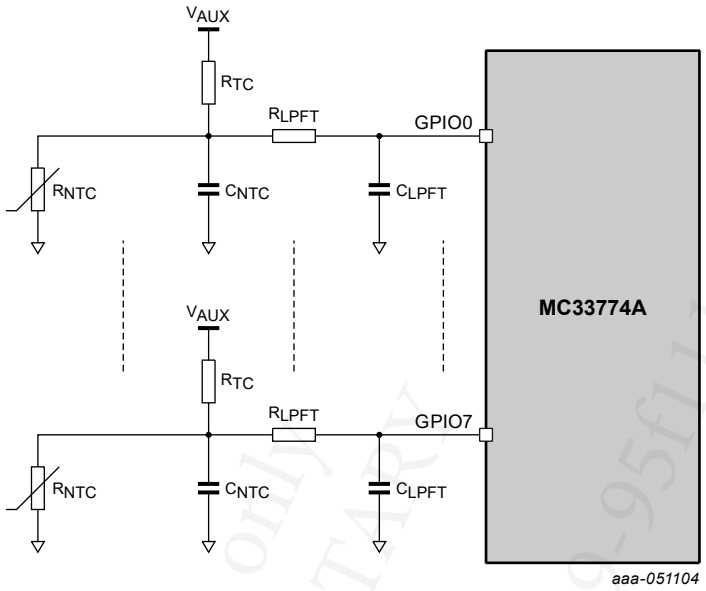


Figure 58. temperature measurements

Table 38. AiNx filter components for temperature measurements

ID	Value	Units	Comments
R_{TC}	10	kΩ	Optimal for R_{NTC} = 10 kΩ; If changed, see C_{LPFT}.
R_{NTC}	10	kΩ	Nominal value resistance is given at 25 °C.
C_{NTC}	0.047	µF	Optional: ESD protection for off board NTC.
R_{LPFT}	5	kΩ	Should not be changed for NTC = 10 kΩ to get Fcut around 330 Hz with C_{LPFT} and keep timing margin for cyclic acquisitions.
C_{LPFT}	0.047	µF	Should not be changed for NTC = 10 kΩ.

11.1.1.5 Alarm signal daisy chain

Figure 59 shows the connection of the alarm daisy chain signal between two battery-cell controllers

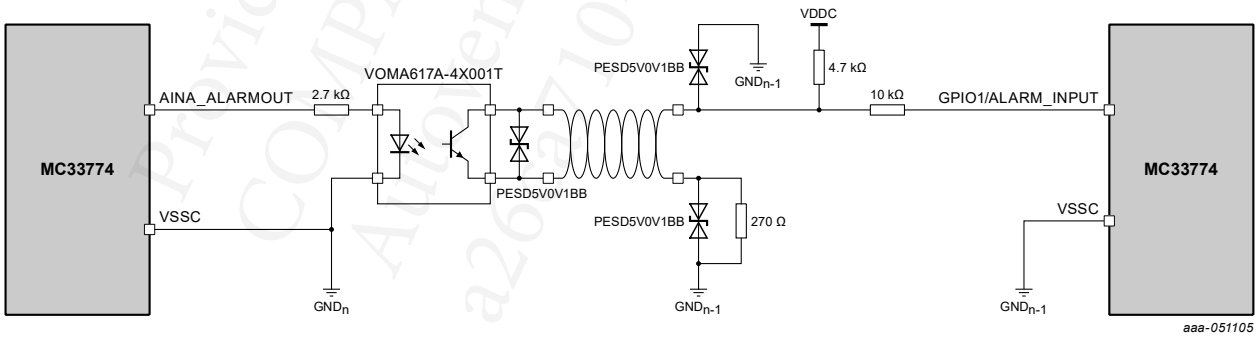


Figure 59. Alarm daisy chain

11.1.1.6 Isolated communication interface

High-speed differential isolated communication is achieved by using transformers or capacitors.

Note: *For hardware compatibility with future MC33774A versions, it is mandatory to add split termination component placeholders between respectively:*

- *Pin 49 MOSI_RXTXHP and pin 50 SCLK_RXTXHN.*
- *Pin 47 CSN_RXTXLN and pin 48 RXTXLP.*

A split termination consists of two resistors Rterm (indicative value 180 ohms) in series and one capacitor Cterm (indicative value 10 nF) placed between the Common mode point and ground.

It is important to note that for MC33774ATA1 version with SYS_VERSION[FREV] = 2h, these components should not be populated.

11.1.1.6.1 Distributed applications

11.1.1.6.1.1 Transformer isolation

Figure 60 shows the recommended application schematic with transformer isolation in a distributed system.

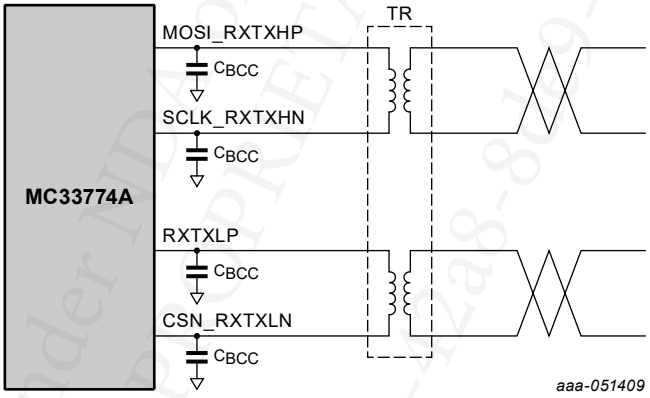


Figure 60. Inductive isolation between nodes

11.1.1.6.1.2 Capacitive isolation

Figure 61 shows the recommended application schematic for capacitive isolation, between nodes, in a distributed system.

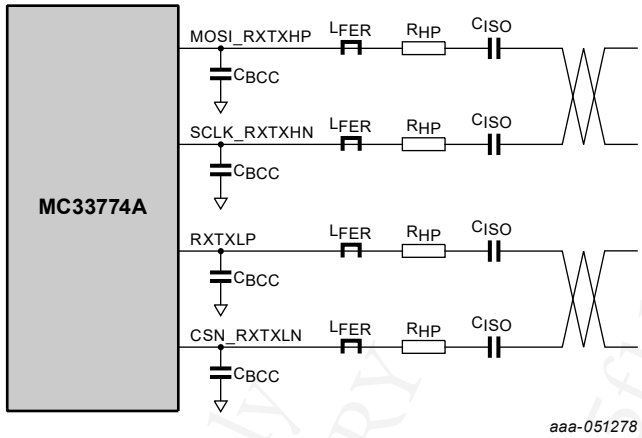


Figure 61. Capacitive isolation between nodes

11.1.1.6.1.3 Component values

Table 39. Component values

ID	Value	Units	Comments
C_{BCC}	220	pF	Common mode capacitors.
R_{HP}	10	Ω	Series resistance for hotplug robustness.
C_{ISO}	0.01	µF	Isolation capacitors.
L_{FER}	470	Ω	Optional: Ferrite bead - MMZ1608Q471
TR	1:1		1 x dual channel 1:1 transformer (example: Pulse Electronic HM2118/HM2168) or 2 x single channel transformers (example: Pulse Electronic TC102M, HM2119, HM2106/HM2166, TDK P303506-A1-52) - no center taps required - no common mode chokes required - Insertion Loss: -1 dB max - OCL 60 µH min

11.1.1.6.2 Centralized applications

11.1.1.6.2.1 Transformer isolation

Transformer isolation shows the recommended schematic when using transformers in a centralized application.

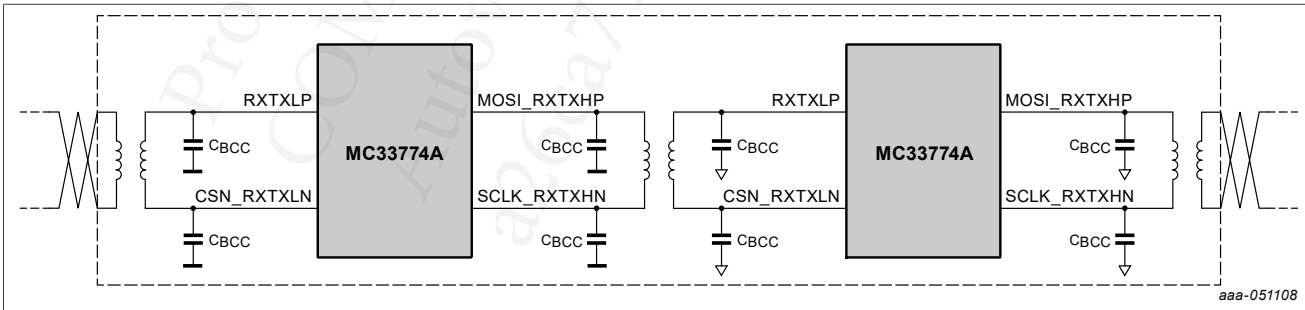


Figure 62. Transformator isolation

11.1.1.6.2.2 Capacitive isolation

Figure 63 shows the recommended schematic when using capacitors in a centralized application.

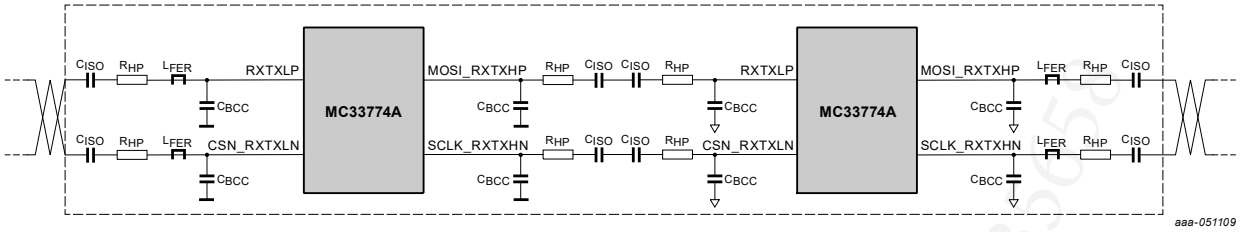


Figure 63. Capacitive isolation

11.1.1.6.2.3 Transformer and capacitive isolation

Figure 64 shows the recommended schematic when using capacitors in a centralized application.

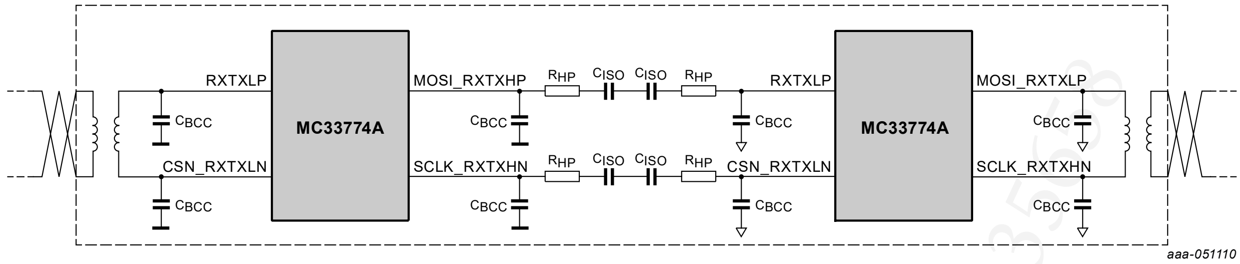


Figure 64. Transformer and capacitive isolation

11.1.1.6.2.4 Component values

Table 40. Component values

ID	Value	Units	Comments
C_{BCC}	220	pF	Common mode capacitors.
R_{HP}	10	Ω	Series resistance for hotplug robustness.
C_{ISO}	0.01	µF	Isolation capacitors.
L_{FER}	470	Ω	Optional: ferrite bead - MMZ1608Q471
TR			Single 1:1 channel transformer: (example: Pulse Electronic TC102M, HM2119, HM2106/ HM2166, TDK P303506-A1-51) - no center taps required - no Common mode chokes required - Insertion Loss: -1 dB max - OCL 60 µH min

11.1.2 Cell and bus bar connections on CT/CB terminals

The cells are connected to the CT pins starting from the lower position. Unused CT pins remain on the upper CT pins and can be connected to the next lower CT pin without need of external components. Unused CB pins connection follows the same connection strategy as for unused CT pins.

Unused CT pins with complete low pass filter can be connected to the next lower CT pins through a connector.

Bus bars are considered as cells and can be connected to CT pins to allow bus bar voltage measurement through primary measurement chain and to CB pins for secondary measurement. Two cells minimum should separate two bus bars.

Positions for cell connection, bus bars connection, and voltages are summarized in the Figure 65.

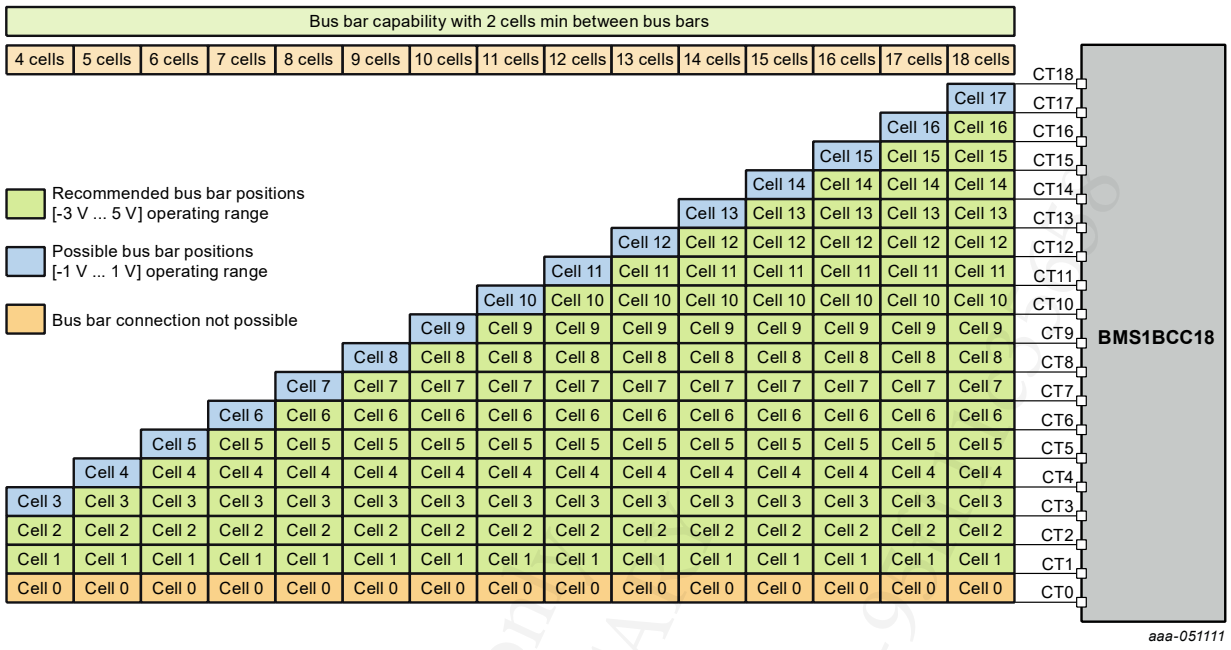


Figure 65. Cell connections

12 Register map

Table 41. MC33774A register map

Start address	End address	Range	Function
00001C00h	00001FFFh	00000400h	secondary measurement
00001800h	00001BFFh	00000400h	primary measurement
00001400h	000017FFh	00000400h	all measurements
00001000h	000013FFh	00000400h	cell balancing registers
00000C00h	00000FFFh	00000400h	I^2C-bus interface
00000800h	00000BFFh	00000400h	GPIO
00000400h	000007FFh	00000400h	event handling
00000000h	000003FFh	00000400h	system control

12.1 Register description

Table 42. Register overview: System_Control_Registers

Address	Name	Access	Reset	Description
0h	SYS_CFG_CRC	R	0h	system configuration CRC
1h	SYS_COM_CFG	R/W	200h	communication initialization
2h	SYS_COM_TO_CFG	R/W	1Eh	system communication timeout
3h	SYS_SUPPLY_CFG	R/W	8003h	supply configuration
4h	SYS_MODE	R/W	1400h	system mode
5h	SYS_CYC_WAKEUP_CFG	R/W	0h	interval for cyclic measurements
6h	SYS_TPL_CFG	R/W	10h	TPL configuration
8h	SYS_CLK_SYNC_CTRL	R/W	0h	clock Synchronization
10h	SYS_VERSION	R	320h	device silicon identifier
11h	SYS_UID_LOW	R	0h	unique device ID lower part
12h	SYS_UID_MID	R	0h	unique device ID middle part
13h	SYS_UID_HIGH	R	0h	unique device ID higher part
14h	SYS_PROD_VER	R	200h	software interface related version of the product
80h	SYS_DS_STORAGE0	R/W	0h	deep sleep storage data 0; the value is stored in the ULP domain
81h	SYS_DS_STORAGE1	R/W	0h	deep sleep storage data 1; the value is stored in the ULP domain

Table 43. Register overview: Event_Handling_Registers

Address	Name	Access	Reset	Description
400h	FEH_CFG_CRC	R	0h	configuration CRC
401h	FEH_ALARM_CFG	R/W	0h	general alarm configuration
402h	FEH_ALARM_OUT_CFG0	R/W	0h	alarm output source selection
403h	FEH_ALARM_OUT_CFG1	R/W	0h	alarm output source selection
404h	FEH_ALARM_OUT_REASON0	R	0h	alarm output reason

Table 43. Register overview: Event_Handling_Registers...*continued*

Address	Name	Access	Reset	Description
405h	FEH_ALARM_OUT_REASON1	R	0h	alarm output reason
408h	FEH_WAKEUP_CFG0	R/W	0h	wake up source configuration
409h	FEH_WAKEUP_CFG1	R/W	0h	wake up source configuration
40Ah	FEH_WAKEUP_REASON0	R	0h	wake up reason register
40Bh	FEH_WAKEUP_REASON1	R	0h	wake up reason register
410h	FEH_MON_BIST_CTRL	R/W	0h	monitor BIST control register
411h	FEH_MON_BIST_RES	R	FFh	monitor BIST result register; value changes at start-up, if everything is fine to 0000h
41Eh	FEH_ACC_ERR	R	0h	access error status register
41Fh	FEH_GRP_FLT_STAT	R	0h	main system fault status register; this register holds one bit per fault group. For each fault group a separate status register exists. The bit here is cleared if all its sources are cleared.
420h	FEH_SUPPLY_FLT_STAT0	R/W	0h	supply fault status register 0 (these monitors are part of the BIST)
421h	FEH_SUPPLY_FLT_STAT1	R/W	0h	supply fault status register 1 (these monitors are not part of the BIST)
422h	FEH_ANA_FLT_STAT	R/W	0h	analog fault status register
423h	FEH_COM_FLT_STAT	R/W	0h	communication fault status register
424h	FEH_MEAS_FLT_STAT	R/W	0h	other fault status register
428h	FEH_SUPPLY_FLT_POR_CFG0	R/W	0h	supply fault POR selection 0
429h	FEH_SUPPLY_FLT_POR_CFG1	R/W	0h	supply fault POR selection 1
42Ah	reserved	R	0h	analog fault POR selection
42Bh	FEH_COM_FLT_POR_CFG	R/W	8h	communication fault POR enable register
430h	FEH_SUPPLY_FLT_EVT_CFG0	R/W	0h	supply fault event selection register 0
431h	FEH_SUPPLY_FLT_EVT_CFG1	R/W	0h	supply fault event selection register 1
432h	FEH_ANA_FLT_EVT_CFG	R/W	0h	analog fault event enable register
433h	FEH_COM_FLT_EVT_CFG	R/W	0h	communication fault event enable register
434h	FEH_MEAS_FLT_EVT_CFG	R/W	0h	measurement fault event enable register
480h	FEH_POR_REASON	R	0h	power-on reset reason. The value is stored in the ULP domain.

Table 44. Register overview: GPIO_Registers

Address	Name	Access	Reset	Description
800h	GPIO_CFG0	R/W	0h	GPIO configuration 0
801h	GPIO_CFG1	R/W	0h	GPIO configuration 1
802h	GPIO_OUT	R/W	0h	GPIO output
804h	GPIO_IN	R	0h	GPIO input

Table 45. Register overview: I2C_Registers

Address	Name	Access	Reset	Description
C00h	I2C_CFG	R/W	0h	I2C configuration
C01h	I2C_CTRL	R/W	0h	I2C control
C02h	I2C_STAT	R	0h	I2C status
C04h	I2C_DATA0	R/W	0h	I2C data register 0
C05h	I2C_DATA1	R/W	0h	I2C data register 1
C06h	I2C_DATA2	R/W	0h	I2C data register 2
C07h	I2C_DATA3	R/W	0h	I2C data register 3
C08h	I2C_DATA4	R/W	0h	I2C data register 4
C09h	I2C_DATA5	R/W	0h	I2C data register 5
C0Ah	I2C_DATA6	R/W	0h	I2C data register 6
C0Bh	I2C_DATA7	R/W	0h	I2C data register 7
C0Ch	I2C_DATA8	R/W	0h	I2C data register 8
C0Dh	I2C_DATA9	R/W	0h	I2C data register 9
C0Eh	I2C_DATA10	R/W	0h	I2C data register 10
C0Fh	I2C_DATA11	R/W	0h	I2C data register 11
C10h	I2C_DATA12	R/W	0h	I2C data register 12
C11h	I2C_DATA13	R/W	0h	I2C data register 13
C12h	I2C_DATA14	R/W	0h	I2C data register 14
C13h	I2C_DATA15	R/W	0h	I2C data register 15
C14h	I2C_DATA16	R/W	0h	I2C data register 16
C15h	I2C_DATA17	R/W	0h	I2C data register 17

Table 46. Register overview: Balancing_Registers

Address	Name	Access	Reset	Description
1000h	BAL_GLOB_CFG	R/W	0h	The global balancing configuration register is used to configure the balancing modes.
1001h	BAL_GLOB_TO_TMR	R/W	0h	The Global Balancing timeout timer register is used to configure the maximum balancing time for all balancing activities to make sure that in case of fault the balancing switches are switched OFF.
1002h	BAL_CH_CFG0	R/W	0h	balancing channel individual enable channel 0 - 15
1003h	BAL_CH_CFG1	R/W	0h	balancing channel individual enable channel 16 - 17
1004h	BAL_PRE_TMR	R/W	0h	pre-balancing timer
1005h	BAL_AUTO_DISCHRG_CTRL	R/W	2152h	emergency discharge enable
1006h	BAL_SWITCH_MON_CFG0	R/W	FFFFh	balancing switch monitoring enable
1007h	BAL_SWITCH_MON_CFG1	R/W	3h	balancing switch monitoring enable
1008h	FULL_PWM_CYCLE_VOLTAGE	R/W	0h	full PWM cycle voltage
1009h	BAL_CH_UV0_STAT0	R	0h	channel under-voltage balancing status channel 0 - 15

Table 46. Register overview: Balancing_Registers...*continued*

Address	Name	Access	Reset	Description
100Ah	BAL_CH_UV0_STAT1	R	0h	channel under-voltage balancing status channel 16 - 17
100Bh	BAL_GLOB_UV1_STAT0	R	0h	global under-voltage balancing status channel 0 - 15
100Ch	BAL_GLOB_UV1_STAT1	R	0h	global under-voltage balancing status channel 16 - 17
100Dh	BAL_STAT0	R	0h	logical balancing channel status channel 0 - 15
100Eh	BAL_STAT1	R	0h	logical balancing channel status channel 16 - 17
100Fh	BAL_STAT2	R	0h	balancing status
1010h	BAL_SWITCH_STAT0	R	0h	physical balancing channel status channel 0 - 15
1011h	BAL_SWITCH_STAT1	R	0h	physical balancing channel status channel 16 - 17
1012h	BAL_SWITCH_FLT_STAT0	R	0h	balancing switch fault channel 0 - 15
1013h	BAL_SWITCH_FLT_STAT1	R	0h	balancing switch fault channel 16 - 17
101Fh	BAL_TMR_CH_ALL	W	0h	virtual register, writes in parallel into BAL_TMR_CH0 up to BAL_TMR_CH17
1020h	BAL_TMR_CH0	R/W	0h	balancing timer channel 0
1021h	BAL_TMR_CH1	R/W	0h	balancing timer channel 1
1022h	BAL_TMR_CH2	R/W	0h	balancing timer channel 2
1023h	BAL_TMR_CH3	R/W	0h	balancing timer channel 3
1024h	BAL_TMR_CH4	R/W	0h	balancing timer channel 4
1025h	BAL_TMR_CH5	R/W	0h	balancing timer channel 5
1026h	BAL_TMR_CH6	R/W	0h	balancing timer channel 6
1027h	BAL_TMR_CH7	R/W	0h	balancing timer channel 7
1028h	BAL_TMR_CH8	R/W	0h	balancing timer channel 8
1029h	BAL_TMR_CH9	R/W	0h	balancing timer channel 9
102Ah	BAL_TMR_CH10	R/W	0h	balancing timer channel 10
102Bh	BAL_TMR_CH11	R/W	0h	balancing timer channel 11
102Ch	BAL_TMR_CH12	R/W	0h	balancing timer channel 12
102Dh	BAL_TMR_CH13	R/W	0h	balancing timer channel 13
102Eh	BAL_TMR_CH14	R/W	0h	balancing timer channel 14
102Fh	BAL_TMR_CH15	R/W	0h	balancing timer channel 15
1030h	BAL_TMR_CH16	R/W	0h	balancing timer channel 16
1031h	BAL_TMR_CH17	R/W	0h	balancing timer channel 17
1032h	BAL_PWM_CH_ALL	W	FFh	virtual register, writes in parallel into BAL_PWM_CH0 up to BAL_PWM_CH17
1033h	BAL_PWM_CH0	R/W	FFh	balancing PWM channel 0
1034h	BAL_PWM_CH1	R/W	FFh	balancing PWM channel 1
1035h	BAL_PWM_CH2	R/W	FFh	balancing PWM channel 2
1036h	BAL_PWM_CH3	R/W	FFh	balancing PWM channel 3
1037h	BAL_PWM_CH4	R/W	FFh	balancing PWM channel 4
1038h	BAL_PWM_CH5	R/W	FFh	balancing PWM channel 5
1039h	BAL_PWM_CH6	R/W	FFh	balancing PWM channel 6

Table 46. Register overview: Balancing_Registers...*continued*

Address	Name	Access	Reset	Description
103Ah	BAL_PWM_CH7	R/W	FFh	balancing PWM channel 7
103Bh	BAL_PWM_CH8	R/W	FFh	balancing PWM channel 8
103Ch	BAL_PWM_CH9	R/W	FFh	balancing PWM channel 9
103Dh	BAL_PWM_CH10	R/W	FFh	balancing PWM channel 10
103Eh	BAL_PWM_CH11	R/W	FFh	balancing PWM channel 11
103Fh	BAL_PWM_CH12	R/W	FFh	balancing PWM channel 12
1040h	BAL_PWM_CH13	R/W	FFh	balancing PWM channel 13
1041h	BAL_PWM_CH14	R/W	FFh	balancing PWM channel 14
1042h	BAL_PWM_CH15	R/W	FFh	balancing PWM channel 15
1043h	BAL_PWM_CH16	R/W	FFh	balancing PWM channel 16
1044h	BAL_PWM_CH17	R/W	FFh	balancing PWM channel 17

Table 47. Register overview: All_Measurement_Registers

Address	Name	Access	Reset	Description
1400h	ALLM_CFG	W	0h	general measurement control
1401h	ALLM_APP_CTRL	W	7C00h	application measurement control
1402h	ALLM_PER_CTRL	W	10h	periodic measurement control
1403h	ALLM_SYNC_CTRL	W	7C00h	synchronous measurement control
1408h	ALLM_VCVB_CFG0	W	0h	cell voltage measurement enable
1409h	ALLM_VCVB_CFG1	W	0h	cell voltage measurement enable

Table 48. Register overview: Primary_Measurement_Registers

Address	Name	Access	Reset	Description
1800h	PRMM_CFG	R/W	0h	general measurement control
1801h	PRMM_APP_CTRL	R/W	7C00h	application measurement control
1802h	PRMM_PER_CTRL	R/W	10h	periodic measurement control
1803h	PRMM_SYNC_CTRL	W	0h	synchronous measurement control
1808h	PRMM_VC_CFG0	R/W	0h	cell voltage measurement enable
1809h	PRMM_VC_CFG1	R/W	0h	cell voltage measurement enable
180Ah	PRMM_AIN_CFG	R/W	20h	AINx measurement enables
180Bh	PRMM_AIN_OL_CFG	R/W	0h	AINx open-load detection enable
180Ch	PRMM_VBUF_CFG	R/W	3h	voltage buffer enable
1810h	PRMM_VC_OV_UV_CFG0	R/W	0h	cell voltage over-voltage and under-voltage check enable
1811h	PRMM_VC_OV_UV_CFG1	R/W	0h	cell voltage over-voltage and under-voltage check enable
1812h	PRMM_VC_OV_TH_CFG	R/W	7FFFh	upper comparator limit for VC0 to VC17
1813h	PRMM_VC_UV0_TH_CFG	R/W	0h	lower comparator limit 0 for VC0 to VC17
1814h	PRMM_VC_UV1_TH_CFG	R/W	0h	lower comparator limit 1 for VC0 to VC17

Table 48. Register overview: Primary_Measurement_Registers...*continued*

Address	Name	Access	Reset	Description
1815h	PRMM_AIN0_OV_TH_CFG	R/W	7FFFh	upper comparator limit for AIN0
1816h	PRMM_AIN1_OV_TH_CFG	R/W	7FFFh	upper comparator limit for AIN1
1817h	PRMM_AIN2_OV_TH_CFG	R/W	7FFFh	upper comparator limit for AIN2
1818h	PRMM_AIN3_OV_TH_CFG	R/W	7FFFh	upper comparator limit for AIN3
1819h	PRMM_AINA_OV_TH_CFG	R/W	7FFFh	upper comparator limit for AINA
181Ah	PRMM_AIN0_UV_TH_CFG	R/W	8001h	lower comparator limit for AIN0
181Bh	PRMM_AIN1_UV_TH_CFG	R/W	8001h	lower comparator limit for AIN1
181Ch	PRMM_AIN2_UV_TH_CFG	R/W	8001h	lower comparator limit for AIN2
181Dh	PRMM_AIN3_UV_TH_CFG	R/W	8001h	lower comparator limit for AIN3
181Eh	PRMM_AINA_UV_TH_CFG	R/W	8001h	lower comparator limit for AINA
1820h	PRMM_CAL_CRC	R/W	0h	CRC over calibration data
1821h	PRMM_CFG_CRC	R	0h	CRC over configuration values
1822h	PRMM_VC_OV_FLT_STAT0	R	0h	cell voltage over-voltage status
1823h	PRMM_VC_OV_FLT_STAT1	R	0h	cell voltage over-voltage status
1824h	PRMM_VC_UV0_FLT_STAT0	R	0h	cell voltage under-voltage status regarding limit 0
1825h	PRMM_VC_UV0_FLT_STAT1	R	0h	cell voltage under-voltage status regarding limit 0
1826h	PRMM_VC_UV1_FLT_STAT0	R	0h	cell voltage under-voltage status regarding limit 1
1827h	PRMM_VC_UV1_FLT_STAT1	R	0h	cell voltage under-voltage status regarding limit 1
1828h	PRMM_AIN_OV_FLT_STAT	R	0h	AINx over-voltage status
1829h	PRMM_AIN_UV_FLT_STAT	R	0h	AINx under-voltage status
183Eh	PRMM_MEAS_STAT	R	0h	measurement status
183Fh	PRMM_APP_VC_CNT	R	0h	application measurement VC sample count number
1840h	PRMM_APP_VC0	R	8000h	application measurement result cell 0
1841h	PRMM_APP_VC1	R	8000h	application measurement result cell 1
1842h	PRMM_APP_VC2	R	8000h	application measurement result cell 2
1843h	PRMM_APP_VC3	R	8000h	application measurement result cell 3
1844h	PRMM_APP_VC4	R	8000h	application measurement result cell 4
1845h	PRMM_APP_VC5	R	8000h	application measurement result cell 5
1846h	PRMM_APP_VC6	R	8000h	application measurement result cell 6
1847h	PRMM_APP_VC7	R	8000h	application measurement result cell 7
1848h	PRMM_APP_VC8	R	8000h	application measurement result cell 8
1849h	PRMM_APP_VC9	R	8000h	application measurement result cell 9
184Ah	PRMM_APP_VC10	R	8000h	application measurement result cell 10
184Bh	PRMM_APP_VC11	R	8000h	application measurement result cell 11
184Ch	PRMM_APP_VC12	R	8000h	application measurement result cell 12
184Dh	PRMM_APP_VC13	R	8000h	application measurement result cell 13
184Eh	PRMM_APP_VC14	R	8000h	application measurement result cell 14
184Fh	PRMM_APP_VC15	R	8000h	application measurement result cell 15
1850h	PRMM_APP_VC16	R	8000h	application measurement result cell 16
1851h	PRMM_APP_VC17	R	8000h	application measurement result cell 17

Table 48. Register overview: Primary_Measurement_Registers...*continued*

Address	Name	Access	Reset	Description
1852h	PRMM_APP_AINA	R	8000h	application measurement result AINA
1853h	PRMM_APP_AIN0	R	8000h	application measurement result AIN0
1854h	PRMM_APP_AIN1	R	8000h	application measurement result AIN1
1855h	PRMM_APP_AIN2	R	8000h	application measurement result AIN2
1856h	PRMM_APP_AIN3	R	8000h	application measurement result AIN3
185Fh	PRMM_PER_NUM	R	0h	measurement period number of the primary periodic results
1860h	PRMM_PER_VC0	R	8000h	periodic measurement result cell 0
1861h	PRMM_PER_VC1	R	8000h	periodic measurement result cell 1
1862h	PRMM_PER_VC2	R	8000h	periodic measurement result cell 2
1863h	PRMM_PER_VC3	R	8000h	periodic measurement result cell 3
1864h	PRMM_PER_VC4	R	8000h	periodic measurement result cell 4
1865h	PRMM_PER_VC5	R	8000h	periodic measurement result cell 5
1866h	PRMM_PER_VC6	R	8000h	periodic measurement result cell 6
1867h	PRMM_PER_VC7	R	8000h	periodic measurement result cell 7
1868h	PRMM_PER_VC8	R	8000h	periodic measurement result cell 8
1869h	PRMM_PER_VC9	R	8000h	periodic measurement result cell 9
186Ah	PRMM_PER_VC10	R	8000h	periodic measurement result cell 10
186Bh	PRMM_PER_VC11	R	8000h	periodic measurement result cell 11
186Ch	PRMM_PER_VC12	R	8000h	periodic measurement result cell 12
186Dh	PRMM_PER_VC13	R	8000h	periodic measurement result cell 13
186Eh	PRMM_PER_VC14	R	8000h	periodic measurement result cell 14
186Fh	PRMM_PER_VC15	R	8000h	periodic measurement result cell 15
1870h	PRMM_PER_VC16	R	8000h	periodic measurement result cell 16
1871h	PRMM_PER_VC17	R	8000h	periodic measurement result cell 17
1872h	PRMM_PER_AINA	R	8000h	periodic measurement result AINA
1873h	PRMM_PER_AIN0	R	8000h	periodic measurement result AIN0
1874h	PRMM_PER_AIN1	R	8000h	periodic measurement result AIN1
1875h	PRMM_PER_AIN2	R	8000h	periodic measurement result AIN2
1876h	PRMM_PER_AIN3	R	8000h	periodic measurement result AIN3
1877h	PRMM_PER_PRMTEMP	R	8000h	periodic measurement result primary device temperature
1878h	PRMM_PER_SECVREF	R	8000h	periodic measurement result secondary voltage reference
1879h	PRMM_PER_VAUX	R	8000h	periodic measurement result auxiliary supply voltage
187Ah	PRMM_PER_VDDC	R	8000h	periodic measurement result VDDC
187Fh	PRMM_SYNC_NUM	R	0h	measurement period number of the synchronous results.
1880h	PRMM_SYNC_VC0	R	8000h	synchronous measurement result cell 0
1881h	PRMM_SYNC_VC1	R	8000h	synchronous measurement result cell 1
1882h	PRMM_SYNC_VC2	R	8000h	synchronous measurement result cell 2

Table 48. Register overview: Primary_Measurement_Registers...*continued*

Address	Name	Access	Reset	Description
1883h	PRMM_SYNC_VC3	R	8000h	synchronous measurement result cell 3
1884h	PRMM_SYNC_VC4	R	8000h	synchronous measurement result cell 4
1885h	PRMM_SYNC_VC5	R	8000h	synchronous measurement result cell 5
1886h	PRMM_SYNC_VC6	R	8000h	synchronous measurement result cell 6
1887h	PRMM_SYNC_VC7	R	8000h	synchronous measurement result cell 7
1888h	PRMM_SYNC_VC8	R	8000h	synchronous measurement result cell 8
1889h	PRMM_SYNC_VC9	R	8000h	synchronous measurement result cell 9
188Ah	PRMM_SYNC_VC10	R	8000h	synchronous measurement result cell 10
188Bh	PRMM_SYNC_VC11	R	8000h	synchronous measurement result cell 11
188Ch	PRMM_SYNC_VC12	R	8000h	synchronous measurement result cell 12
188Dh	PRMM_SYNC_VC13	R	8000h	synchronous measurement result cell 13
188Eh	PRMM_SYNC_VC14	R	8000h	synchronous measurement result cell 14
188Fh	PRMM_SYNC_VC15	R	8000h	synchronous measurement result cell 15
1890h	PRMM_SYNC_VC16	R	8000h	synchronous measurement result cell 16
1891h	PRMM_SYNC_VC17	R	8000h	synchronous measurement result cell 17

Table 49. Register overview: Secondary_Measurement_Registers

Address	Name	Access	Reset	Description
1C00h	SECM_CFG	R/W	0h	general measurement control
1C01h	SECM_APP_CTRL	W	0h	application measurement control
1C02h	SECM_PER_CTRL	R/W	10h	periodic measurement control
1C03h	SECM_SYNC_CTRL	R/W	7C00h	synchronous measurement control
1C08h	SECM_VB_CFG0	R/W	0h	balance voltage measurement enable
1C09h	SECM_VB_CFG1	R/W	0h	balance voltage measurement enable
1C0Ah	SECM_AIN_CFG	R/W	80h	measurement enables for extra channel
1C0Bh	SECM_AIN_OL_CFG	R/W	0h	AINx open-load detection enable
1C0Ch	SECM_VBUF_CFG	R/W	3h	voltage buffer enable
1C20h	SECM_CAL_CRC	R/W	0h	CRC over calibration data
1C21h	SECM_CFG_CRC	R	0h	CRC over configuration values
1C3Eh	SECM_MEAS_STAT	R	0h	measurement status
1C53h	SECM_APP_AIN4	R	8000h	application measurement result AIN4
1C54h	SECM_APP_AIN5	R	8000h	application measurement result AIN5
1C55h	SECM_APP_AIN6	R	8000h	application measurement result AIN6
1C56h	SECM_APP_AIN7	R	8000h	application measurement result AIN7
1C5Fh	SECM_PER_NUM	R	0h	measurement period number of the secondary periodic results
1C73h	SECM_PER_AIN4	R	8000h	periodic measurement result AIN4
1C74h	SECM_PER_AIN5	R	8000h	periodic measurement result AIN5
1C75h	SECM_PER_AIN6	R	8000h	periodic measurement result AIN6
1C76h	SECM_PER_AIN7	R	8000h	periodic measurement result AIN7

Table 49. Register overview: Secondary_Measurement_Registers*...continued*

Address	Name	Access	Reset	Description
1C77h	SECM_PER_SECTEMP	R	8000h	periodic measurement result secondary device temperature
1C78h	SECM_PER_PRMVREF	R	8000h	periodic measurement result primary voltage reference
1C79h	SECM_PER_VAUX	R	8000h	periodic measurement result auxiliary supply voltage
1C7Ah	SECM_PER_VBAT	R	8000h	periodic measurement result VBAT
1C7Bh	SECM_PER_VDDA	R	8000h	periodic measurement result VDDA
1C7Ch	SECM_PER_VDDC	R	8000h	periodic measurement result VDDC
1C7Eh	SECM_PER_NPNISENSE	R	8000h	periodic measurement result NPN current sensor
1C7Fh	SECM_SYNC_NUM	R	0h	measurement number of the secondary synchronous results
1C80h	SECM_SYNC_VB0	R	8000h	synchronous measurement result from balancing pins cell 0.
1C81h	SECM_SYNC_VB1	R	8000h	synchronous measurement result from balancing pins cell 1
1C82h	SECM_SYNC_VB2	R	8000h	synchronous measurement result from balancing pins cell 2
1C83h	SECM_SYNC_VB3	R	8000h	synchronous measurement result from balancing pins cell 3
1C84h	SECM_SYNC_VB4	R	8000h	synchronous measurement result from balancing pins cell 4
1C85h	SECM_SYNC_VB5	R	8000h	synchronous measurement result from balancing pins cell 5
1C86h	SECM_SYNC_VB6	R	8000h	synchronous measurement result from balancing pins cell 6
1C87h	SECM_SYNC_VB7	R	8000h	synchronous measurement result from balancing pins cell 7
1C88h	SECM_SYNC_VB8	R	8000h	synchronous measurement result from balancing pins cell 8
1C89h	SECM_SYNC_VB9	R	8000h	synchronous measurement result from balancing pins cell 9
1C8Ah	SECM_SYNC_VB10	R	8000h	synchronous measurement result from balancing pins cell 10
1C8Bh	SECM_SYNC_VB11	R	8000h	synchronous measurement result from balancing pins cell 11
1C8Ch	SECM_SYNC_VB12	R	8000h	synchronous measurement result from balancing pins cell 12
1C8Dh	SECM_SYNC_VB13	R	8000h	synchronous measurement result from balancing pins cell 13
1C8Eh	SECM_SYNC_VB14	R	8000h	synchronous measurement result from balancing pins cell 14
1C8Fh	SECM_SYNC_VB15	R	8000h	synchronous measurement result from balancing pins cell 15
1C90h	SECM_SYNC_VB16	R	8000h	synchronous measurement result from balancing pins cell 16
1C91h	SECM_SYNC_VB17	R	8000h	synchronous measurement result from balancing pins cell 17

12.1.1 SYS_CFG_CRC register

System configuration CRC

Table 50. SYS_CFG_CRC register - system configuration CRC (address 0h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CRC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 51. SYS_CFG_CRC register - system configuration CRC (address 0h)

Bit	Symbol	Access	Value	Description
15:0	CRC	R	0h	This CRC value is recalculated with any write to a covered register and with any read to this register. The updated CRC value is available latest 100 µs after the last write. The CRC value is application specific and must be re-calculated by the MCU. The used polynomial is: D175h (+1) = $X^{16} + X^{15} + X^{13} + X^9 + X^7 + X^6 + X^5 + X^3 + X^1 + 1$. Following registers are included: SYS_COM_CFG, SYS_COM_TO_CFG, SYS_SUPPLY_CFG, SYS_CYC_WAKEUP_CFG, SYS_TPL_CFG.

12.1.2 SYS_COM_CFG register

Communication initialization

Table 52. SYS_COM_CFG register - communication initialization (address 1h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	NUMNODES						BUSFW	CADD
Reset	0	0	0	0	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CADD		DADD					
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 53. SYS_COM_CFG register - communication initialization (address 1h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:10	NUMNODES	R/W	0h	Number of nodes in the daisy chain. Difference of NUMNODES and DADD defines the wait time for global write commands.
9	BUSFW	R/W		Bus forwarding
			0	DISABLED (read-write) Disabled
			1*	ENABLED (read-write) Enabled if DADD is unequal 00h
8:6	CADD	R/W		Defines the daisy chain address **CADD** = chain address CADD is only used for responses to a all chain read request.

Table 53. SYS_COM_CFG register - communication initialization (address 1h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			000*	RESERVED (read-write) Reserved for future usage
			111	GLOBAL (read-write) Reserved for global write commands
5:0	DADD	R/W		Defines the device address **DADD** = device address
			00h*	UNENUMERATED (read-write) Device is unenumerated; bus forwarding is disabled.
			3Fh	GLOBAL (read-write) Used for global read and write commands

12.1.3 SYS_COM_TO_CFG register

System communication timeout

Table 54. SYS_COM_TO_CFG register - system communication timeout (address 2h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	COMTODISABLE								COMTO							
Reset	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 55. SYS_COM_TO_CFG register - system communication timeout (address 2h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	COMTODISABLE	R/W		Communication timeout disable. Only intended for software development activities. Must never be used in release software.
			00h*	DEFAULT (read-write) Communication timeout enabled
			5Ah	DISABLED (read-write) Communication timeout disabled
7:0	COMTO	R/W		Communication timeout time **COMTO** * 10 milliseconds A value of 0 is treated as 10 ms.
			00h	T_MIN (read-write) 10 ms
			01h	T_10m (read-write) 10 ms
			1Eh*	T_300m (read-write) 300 ms
			FFh	T_MAX (read-write) 2550 ms

12.1.4 SYS_SUPPLY_CFG register

Supply configuration

Table 56. SYS_SUPPLY_CFG register - supply configuration (address 3h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	CURMATCH	reserved						
Reset	1	0	0	0	0	0	0	0
Access	R/W	R	R	R	R	R	R	R

Table 56. SYS_SUPPLY_CFG register - supply configuration (address 3h) bit allocation*...continued*

Bit	7	6	5	4	3	2	1	0
Symbol	reserved					VDDCCYC	VAUXCYC	VAUXACT
Reset	0	0	0	0	0	0	1	1
Access	R	R	R	R	R	R/W	R/W	R/W

Table 57. SYS_SUPPLY_CFG register - supply configuration (address 3h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	CURMATCH	R/W		Enable IC supply current matching in active mode.
			0	DISABLED (read-write) Supply current matching is disabled
			1*	ENABLED (read-write) Supply current matching is enabled
14:3	reserved	R	0h	This read-only field is reserved and always has the value 0.
2	VDDCCYC	R/W		Enable VDDC in cyclic mode.
			0*	DISABLED (read-write) VDDC is disabled in cyclic mode
			1	ENABLED (read-write) VDDC is enabled in cyclic mode
1	VAUXCYC	R/W		Enable VAUX in cyclic mode.
			0	DISABLED (read-write) VAUX is disabled in cyclic mode
			1*	ENABLED (read-write) VAUX is enabled in cyclic mode
0	VAUXACT	R/W		Enable VAUX in active mode.
			0	DISABLED (read-write) VAUX is disabled in active mode
			1*	ENABLED (read-write) VAUX is enabled in active mode

12.1.5 SYS_MODE register

System mode

Table 58. SYS_MODE register - system mode (address 4h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved			PREVMODE					reserved			TARGETMODE				
Reset	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	W	W	W	W	W

Table 59. SYS_MODE register - system mode (address 4h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:13	reserved	R	0h	This read-only field is reserved and always has the value 0.
12:8	PREVMODE	R		Previous mode. **Other** values as stated are invalid.
			0Ah	SLEEP (read) Sleep mode
			14h*	DEEPSLEEP (read) Deep sleep mode
			1Fh	CYCLIC (read) Cyclic mode

Table 59. SYS_MODE register - system mode (address 4h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7:5	reserved	R	0h	This read-only field is reserved and always has the value 0.
4:0	TARGETMODE	W	0h	Target mode. The mode transition starts immediately after writing. **Other** values as stated are ignored.
			0Ah	SLEEP (write) Sleep mode
			14h	DEEPSLEEP (write) Deep sleep mode

12.1.6 SYS_CYC_WAKEUP_CFG register

Interval for cyclic measurements

Table 60. SYS_CYC_WAKEUP_CFG register - interval for cyclic measurements (address 5h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	PERIOD															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 61. SYS_CYC_WAKEUP_CFG register - interval for cyclic measurements (address 5h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:0	PERIOD	R/W		Time between two cyclic wake-up events. **PERIOD** * 100 milliseconds
			0000h*	DISABLED (read-write) Cyclic wakeup disabled
			0001h	PERIOD (read-write) PERIOD * 100 ms
			FFFFh	PERIOD_MAX (read-write) Maximum period time = 6553500 ms = approximately 1.8 h

12.1.7 SYS_TPL_CFG register

TPL configuration

Table 62. SYS_TPL_CFG register - TPL configuration. (address 6h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved		RESPCFG		TXTERMH	TXTERML	WAKEUPCOMP	
Reset	0	0	0	1	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 63. SYS_TPL_CFG register - TPL configuration. (address 6h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:6	reserved	R	0h	This read-only field is reserved and always has the value 0.
5:4	RESPCFG	R/W		Response interface
			00	SAME (read-write) Responses are only transmitted on the receiving port.
			01*	BOTH (read-write) Responses are transmitted on both ports if DADD is unequal 00h.
			10	OPPOSITE (read-write) Responses are transmitted on the opposite port of the receiving port.
			11	RESERVED (read-write) Reserved, do not use. For now same as BOTH.
3	TXTERMH	R/W		Termination active while transmit for the higher TPL port. (Pin 49 and pin 50)
			0*	DISABLED (read-write) Disabled; termination is inactive during transmit. Required for normal TPL operation.
			1	ENABLED (read-write) Enabled; termination is active during transmit. Only needed at final daisy-chain node to have equal power consumption.
2	TXTERML	R/W		Termination active while transmit for the lower TPL port. (Pin 47 and pin 48)
			0*	DISABLED (read-write) Disabled; termination is inactive during transmit. Required for normal TPL operation.
			1	ENABLED (read-write) Enabled; termination is active during transmit. Only needed at final daisy-chain node to have equal power consumption.
1:0	WAKEUPCOMP	R/W		Defines compatibility for the MC33664 wake-up by the Daisy Chain. Undefined values are treated as HIGHER.
			00*	DEFAULT (read-write) Wake-up signal on both ports is compatible to MC33775 and MC33774.
			01	LOWER (read-write) Wake-up signal on lower TPL port is compatible to MC33664. The other port is compatible to MC33775 and MC33774.
			10	HIGHER (read-write) Wake-up signal on higher TPL port is compatible to MC33664. The other port is compatible to MC33775 and MC33774.

12.1.8 SYS_CLK_SYNC_CTRL register

Clock synchronization

Table 64. SYS_CLK_SYNC_CTRL register - clock Synchronization (address 8h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	SYNCCNT															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 65. SYS_CLK_SYNC_CTRL register - clock Synchronization (address 8h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:0	SYNCCNT	R/W		Synchronization counter value: Writing a 0000h resets the counter with no adjustment. For other values it is checked if the internal counter value is higher, in which case the oscillator frequency is decreased. If it is lower the internal oscillator frequency is increased. Reading the value returns the current internal counter value. 1 LSB = 10 µs.
			0000h*	RESET (read-write) Counter is reset with no adjustment.
			0001h	ADJUST (read-write) 10 µs

12.1.9 SYS_VERSION register

Device silicon identifier

Table 66. SYS_VERSION register - device silicon identifier (address 10h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	TYPE								FREV				MREV			
Reset	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	1
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 67. SYS_VERSION register - device silicon identifier (address 10h)

Bit	Symbol	Access	Value	Description
15:8	TYPE	R	3h	Type identifier. Development samples might show a different value.
7:4	FREV	R	2h	Full mask revision ID
3:0	MREV	R	1h	Metal revision ID

12.1.10 SYS_UID_LOW register

Unique device ID lower part

Table 68. SYS_UID_LOW register - unique device ID lower part (address 11h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LOW															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 69. SYS_UID_LOW register - unique device ID lower part (address 11h)

Bit	Symbol	Access	Value	Description
15:0	LOW	R	0h	Lower part of unique device ID

12.1.11 SYS_UID_MID register

Unique device ID middle part

Table 70. SYS_UID_MID register - unique device ID middle part (address 12h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	MID															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 71. SYS_UID_MID register - unique device ID middle part (address 12h)

Bit	Symbol	Access	Value	Description
15:0	MID	R	0h	Middle part of unique device ID

12.1.12 SYS_UID_HIGH register

Unique device ID higher part

Table 72. SYS_UID_HIGH register - unique device ID higher part (address 13h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	HIGH															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 73. SYS_UID_HIGH register - unique device ID higher part (address 13h)

Bit	Symbol	Access	Value	Description
15:0	HIGH	R	0h	Higher part of unique device ID

12.1.13 SYS_PROD_VER register

Software interface related version of the product

Table 74. SYS_PROD_VER register - software interface related version of the product (address 14h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved				MAJOR				MINOR				PATCH			
Reset	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 75. SYS_PROD_VER register - software interface related version of the product (address 14h)

Bit	Symbol	Access	Value	Description
15:12	reserved	R	0h	This read-only field is reserved and always has the value 0.
11:8	MAJOR	R	2h	Major Revision: Software interface change, register-map or registers changed. Non-compatible with previous versions. (Auto SAR nomenclature)
7:4	MINOR	R	0h	Minor Revision: Software interface change, for example improvement or extension which is covered by additional registers or transparent to the software. Existing software

Table 75. SYS_PROD_VER register - software interface related version of the product (address 14h)...*continued*

Bit	Symbol	Access	Value	Description
				is compatible but may not use new features. (AutoSAR nomenclature).
3:0	PATCH	R	0h	Patch: Patch with no software interface change. (AutoSAR nomenclature)

12.1.14 SYS_DS_STORAGE0 register

Deep sleep storage data 0; the value is stored in the ULP domain

Table 76. SYS_DS_STORAGE0 register - Deep Sleep Storage Data0. (address 80h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	DATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 77. SYS_DS_STORAGE0 register - Deep Sleep Storage Data0. (address 80h)

Bit	Symbol	Access	Value	Description
15:0	DATA	R/W	0h	Deep Sleep surviving data; this register has no reset. This register allows to store application data and has no influence on the device.

12.1.15 SYS_DS_STORAGE1 register

Deep sleep storage data 1; the value is stored in the ULP domain

Table 78. SYS_DS_STORAGE1 register - Deep Sleep Storage Data1. (address 81h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	DATA															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 79. SYS_DS_STORAGE1 register - Deep Sleep Storage Data1. (address 81h)

Bit	Symbol	Access	Value	Description
15:0	DATA	R/W	0h	Deep Sleep surviving data; this register has no reset. This register allows to store application data and has no influence on the device.

12.1.16 FEH_CFG_CRC register

Configuration CRC

Table 80. FEH_CFG_CRC register - configuration CRC (address 400h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CRC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 81. FEH_CFG_CRC register - configuration CRC (address 400h)

Bit	Symbol	Access	Value	Description
15:0	CRC	R	0h	This CRC value is recalculated with any transition into Active mode, with any write to a covered register and with any read to this register. The updated CRC value is available latest 100 μs after the last write. The CRC value is application specific and must be re-calculated by the MCU. The used polynomial is: D175h (+1) = $X^{16} + X^{15} + X^{13} + X^{9} + X^{7} + X^{6} + X^{5} + X^{3} + X^{1} + 1$. Following registers are included: FEH_ALARM_CFG, FEH_ ALARM_OUT_CFG0, FEH_ALARM_OUT_CFG1, FEH_ WAKEUP_CFG0, FEH_WAKEUP_CFG1, FEH_SUPPLY_FLT_ POR_CFG0, FEH_SUPPLY_FLT_POR_CFG1, FEH_ANA_ FLT_POR_CFG, FEH_COM_FLT_POR_CFG, FEH_SUPPLY_ FLT_EVT_CFG0, FEH_SUPPLY_FLT_EVT_CFG1, FEH_ANA_ FLT_EVT_CFG, FEH_COM_FLT_EVT_CFG, FEH_MEAS_FLT_ EVT_CFG.

12.1.17 FEH_ALARM_CFG register

General alarm configuration

Table 82. FEH_ALARM_CFG register - general alarm configuration (address 401h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							ALARMI NHBINV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	ALARMOUTHB		ALARMOUT		ALARMINHB		ALARMIN	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 83. FEH_ALARM_CFG register - general alarm configuration (address 401h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:9	reserved	R	0h	This read-only field is reserved and always has the value 0.
8	ALARMINHBINV	R/W		Inverted heartbeat input
			0*	DISABLED (read-write) Normal heartbeat (LOW with HIGH pulses) input used
			1	ENABLED (read-write) Inverted heartbeat (HIGH with LOW pulses) input used
7:6	ALARMOUTHB	R/W		Output heartbeat low time setting
			00*	T_500u (read-write) 500 us
			01	T_1ms (read-write) 1 ms
			10	T_10ms (read-write) 10 ms
			11	T_100ms (read-write) 100 ms
5:4	ALARMOUT	R/W		Enable alarm output
			00*	DISABLED (read-write) disabled. Alarm output is high impedance.

Table 83. FEH_ALARM_CFG register - general alarm configuration (address 401h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			01	HIGH_ACTIVE (read-write) high active
			10	LOW_ACTIVE (read-write) low active
			11	HEARTBEAT (read-write) heartbeat configuration
3:2	ALARMINHB	R/W		Input heartbeat low time setting
			00*	T_500u (read-write) 500 us
			01	T_1ms (read-write) 1 ms
			10	T_10ms (read-write) 10 ms
			11	T_100ms (read-write) 100 ms
1:0	ALARMIN	R/W		Enable alarm input Enabling the alarm input automatically enables the digital receiver for the Alarm input pin.
			00*	DISABLED (read-write) Alarm input is disabled
			01	HIGH_ACTIVE (read-write) Alarm input is enabled, high active
			10	LOW_ACTIVE (read-write) Alarm input is enabled, low active
			11	HEARTBEAT (read-write) Alarm input is enabled, heartbeat configuration

12.1.18 FEH_ALARM_OUT_CFG0 register

Alarm output source selection

Table 84. FEH_ALARM_OUT_CFG0 register - alarm output source selection (address 402h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved	SYSFLTEVT	BALRDY	WAKEUPIN	ALARMIN	AIN3UV	AIN3OV	AIN2UV
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	AIN2OV	AIN1UV	AIN1OV	AIN0UV	AIN0OV	VCUV1	VCUV0	VCOV
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 85. FEH_ALARM_OUT_CFG0 register - alarm output source selection (address 402h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	reserved	R	0h	This read-only field is reserved and always has the value 0.
14	SYSFLTEVT	R/W		Enable output on alarm output for a detected and selected system fault.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
13	BALRDY	R/W		Enable output on alarm output for cell voltage balancing ready.
			0*	DISABLED (read-write) disabled

Table 85. FEH_ALARM_OUT_CFG0 register - alarm output source selection (address 402h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			1	ENABLED (read-write) enabled
12	WAKEUPIN	R/W		Enable output on detected wakeup input. Enabling this bit automatically enables the digital receiver for the wakeup input pin.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
11	ALARMIN	R/W		Enable output on alarm output for detected alarm input.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
10	AIN3UV	R/W		Enable output on alarm output for AIN3_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
9	AIN3OV	R/W		Enable output on alarm output for AIN3_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
8	AIN2UV	R/W		Enable output on alarm output for AIN2_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
7	AIN2OV	R/W		Enable output on alarm output for AIN2_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
6	AIN1UV	R/W		Enable output on alarm output for AIN1_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
5	AIN1OV	R/W		Enable output on alarm output for AIN1_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
4	AIN0UV	R/W		Enable output on alarm output for AIN0_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
3	AIN0OV	R/W		Enable output on alarm output for AIN0_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
2	VCUV1	R/W		Enable output on alarm output for VC_UV1.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
1	VCUV0	R/W		Enable output on alarm output for VC_UV0.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
0	VCOV	R/W		Enable output on alarm output for VC_OV.

Table 85. FEH_ALARM_OUT_CFG0 register - alarm output source selection (address 402h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled

12.1.19 FEH_ALARM_OUT_CFG1 register

Alarm output source selection

Table 86. FEH_ALARM_OUT_CFG1 register - alarm output source selection (address 403h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							BALPROT
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						AINAUV	AINAOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 87. FEH_ALARM_OUT_CFG1 register - alarm output source selection (address 403h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:9	reserved	R	0h	This read-only field is reserved and always has the value 0.
8	BALPROT	R/W		Enable output on alarm output for detected balancing protection
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
7:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	AINAUV	R/W		Enable output on alarm output for AINA_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
0	AINAOV	R/W		Enable output on alarm output for AINA_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled

12.1.20 FEH_ALARM_OUT_REASON0 register

Alarm output reason

Table 88. FEH_ALARM_OUT_REASON0 register - alarm output reason (address 404h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved	SYSFLTEVT	BALRDY	WAKEUPIN	ALARMIN	AIN3UV	AIN3OV	AIN2UV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 88. FEH_ALARM_OUT_REASON0 register - alarm output reason (address 404h) bit allocation*...continued*

Bit	7	6	5	4	3	2	1	0
Symbol	AIN2OV	AIN1UV	AIN1OV	AIN0UV	AIN0OV	VCUV1	VCUV0	VCOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 89. FEH_ALARM_OUT_REASON0 register - alarm output reason (address 404h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	reserved	R	0h	This read-only field is reserved and always has the value 0.
14	SYSFLTEVT	R		Detected system fault. Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by detected system fault
			1	ALARM (read) Alarm caused by detected system fault
13	BALRDY	R		Cell voltage balancing ready Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by cell voltage balancing ready
			1	ALARM (read) Alarm caused by cell voltage balancing ready
12	WAKEUPIN	R		Detected wakeup input Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by detected wakeup input
			1	ALARM (read) Alarm caused by detected wakeup input
11	ALARMIN	R		Detected alarm input Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by detected alarm input
			1	ALARM (read) Alarm caused by detected alarm input
10	AIN3UV	R		AIN3_UV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN3_UV
			1	ALARM (read) Alarm caused by AIN3_UV
9	AIN3OV	R		AIN3_OV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN3_OV
			1	ALARM (read) Alarm caused by AIN3_OV
8	AIN2UV	R		AIN2_UV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN2_UV
			1	ALARM (read) Alarm caused by AIN2_UV
7	AIN2OV	R		AIN2_OV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN2_OV
			1	ALARM (read) Alarm caused by AIN2_OV
6	AIN1UV	R		AIN1_UV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN1_UV
			1	ALARM (read) Alarm caused by AIN1_UV
5	AIN1OV	R		AIN1_OV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN1_OV

Table 89. FEH_ALARM_OUT_REASON0 register - alarm output reason (address 404h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			1	ALARM (read) Alarm caused by AIN1_OV
4	AIN0UV	R		AIN0_UV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN0_UV
			1	ALARM (read) Alarm caused by AIN0_UV
3	AIN0OV	R		AIN0_OV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by AIN0_OV
			1	ALARM (read) Alarm caused by AIN0_OV
2	VCUV1	R		VC_UV1 Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by VC_UV1
			1	ALARM (read) Alarm caused by VC_UV1
1	VCUV0	R		VC_UV0 Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by VC_UV0
			1	ALARM (read) Alarm caused by VC_UV0
0	VCOV	R		VC_OV Read clears bit.
			0*	NO_ALARM (read) Alarm not caused by VC_OV
			1	ALARM (read) Alarm caused by VC_OV

12.1.21 FEH_ALARM_OUT_REASON1 register

Alarm output reason

Table 90. FEH_ALARM_OUT_REASON1 register - alarm output reason (address 405h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							BALPROT
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						AINAUV	AINAOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 91. FEH_ALARM_OUT_REASON1 register - alarm output reason (address 405h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:9	reserved	R	0h	This read-only field is reserved and always has the value 0.
8	BALPROT	R		Balancing protection detection Read clears bit.
			0*	NO_WAKE (read) Alarm not caused by detected Balancing protection
			1	WAKE_UP (read) Alarm caused by detected Balancing protection
7:2	reserved	R	0h	This read-only field is reserved and always has the value 0.

Table 91. FEH_ALARM_OUT_REASON1 register - alarm output reason (address 405h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
1	AINAUV	R		AINA_UV Read clears bit.
			0*	NO_WAKE (read) Alarm not caused by AINA_UV
			1	WAKE_UP (read) Alarm caused by AINA_UV
0	AINAOV	R		AINA_OV Read clears bit.
			0*	NO_WAKE (read) Alarm not caused by AINA_OV
			1	WAKE_UP (read) Alarm caused by AINA_OV

12.1.22 FEH_WAKEUP_CFG0 register

Wake-up source configuration

Table 92. FEH_WAKEUP_CFG0 register - wake-up source configuration (address 408h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	TPLWAKEUP	SYSFLTEVT	BALRDY	WAKEUPIN	ALARMIN	AIN3UV	AIN3OV	AIN2UV
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	AIN2OV	AIN1UV	AIN1OV	AIN0UV	AIN0OV	VCUV1	VCUV0	VCOV
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 93. FEH_WAKEUP_CFG0 register - wake up source configuration (address 408h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	TPLWAKEUP	R/W		Wake TPL
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled. Device sends wake-up frames on TPL if wake-up reason was other than communication
14	SYSFLTEVT	R/W		Enable wakeup on a detected system fault.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
13	BALRDY	R/W		Enable wakeup on cell voltage balancing ready.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
12	WAKEUPIN	R/W		Enable wakeup on detected wakeup input. Enabling this bit automatically enables the digital receiver for wake-up input 0.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
11	ALARMIN	R/W		Enable wakeup on detected alarm input
			0*	DISABLED (read-write) disabled

Table 93. FEH_WAKEUP_CFG0 register - wake up source configuration (address 408h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			1	ENABLED (read-write) enabled
10	AIN3UV	R/W		Enable wakeup on AIN3_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
9	AIN3OV	R/W		Enable wakeup on AIN3_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
8	AIN2UV	R/W		Enable wakeup on AIN2_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
7	AIN2OV	R/W		Enable wakeup on AIN2_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
6	AIN1UV	R/W		Enable wakeup on AIN1_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
5	AIN1OV	R/W		Enable wakeup on AIN1_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
4	AIN0UV	R/W		Enable wakeup on AIN0_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
3	AIN0OV	R/W		Enable wakeup on AIN0_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
2	VCUV1	R/W		Enable wakeup on VC_UV1.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
1	VCUV0	R/W		Enable wakeup on VC_UV0.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
0	VCOV	R/W		Enable wakeup on VC_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled

12.1.23 FEH_WAKEUP_CFG1 register

Wake-up source configuration

Table 94. FEH_WAKEUP_CFG1 register - wake-up source configuration (address 409h) bit allocation

Bit	15	14	13	12	11	10	9	8

Table 94. FEH_WAKEUP_CFG1 register - wake-up source configuration (address 409h) bit allocation*...continued*

Symbol	reserved							BALPROT
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						AINAUV	AINAOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 95. FEH_WAKEUP_CFG1 register - wake up source configuration (address 409h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:9	reserved	R	0h	This read-only field is reserved and always has the value 0.
8	BALPROT	R/W		Enable wakeup on detected balancing protection
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
7:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	AINAUV	R/W		Enable wakeup on AINA_UV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled
0	AINAOV	R/W		Enable wakeup on AINA_OV.
			0*	DISABLED (read-write) disabled
			1	ENABLED (read-write) enabled

12.1.24 FEH_WAKEUP_REASON0 register

Wake-up reason register

Table 96. FEH_WAKEUP_REASON0 register - wake-up reason register (address 40Ah) bit allocation

Bit	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**
Symbol	COMM	SYSFLTEVT	BALRDY	WAKEUPIN	ALARMIN	AIN3UV	AIN3OV	AIN2UV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	AIN2OV	AIN1UV	AIN1OV	AIN0UV	AIN0OV	VCUV1	VCUV0	VCOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 97. FEH_WAKEUP_REASON0 register - wake up reason register (address 40Ah)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	COMM	R		Communication detected Read clears bit.

Table 97. FEH_WAKEUP_REASON0 register - wake up reason register (address 40Ah)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	NO_WAKE (read) Wakeup not caused by detected communication
			1	WAKE_UP (read) Wakeup caused by detected communication
14	SYSFLTEVT	R		Detected system fault. Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by detected system fault
			1	WAKE_UP (read) Wakeup caused by detected system fault
13	BALRDY	R		Cell voltage balancing ready Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by cell voltage balancing ready
			1	WAKE_UP (read) Wakeup caused by cell voltage balancing ready
12	WAKEUPIN	R		Detected wakeup input Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by detected wakeup input
			1	WAKE_UP (read) Wakeup caused by detected wakeup input
11	ALARMIN	R		Detected alarm input Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by detected Wakeup input
			1	WAKE_UP (read) Wakeup caused by detected Wakeup input
10	AIN3UV	R		AIN3_UV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN3_UV
			1	WAKE_UP (read) Wakeup caused by AIN3_UV
9	AIN3OV	R		AIN3_OV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN3_OV
			1	WAKE_UP (read) Wakeup caused by AIN3_OV
8	AIN2UV	R		AIN2_UV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN2_UV
			1	WAKE_UP (read) Wakeup caused by AIN2_UV
7	AIN2OV	R		AIN2_OV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN2_OV
			1	WAKE_UP (read) Wakeup caused by AIN2_OV
6	AIN1UV	R		AIN1_UV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN1_UV
			1	WAKE_UP (read) Wakeup caused by AIN1_UV
5	AIN1OV	R		AIN1_OV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN1_OV
			1	WAKE_UP (read) Wakeup caused by AIN1_OV
4	AIN0UV	R		AIN0_UV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN0_UV

Table 97. FEH_WAKEUP_REASON0 register - wake up reason register (address 40Ah)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			1	WAKE_UP (read) Wakeup caused by AIN0_UV
3	AIN0OV	R		AIN0_OV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AIN0_OV
			1	WAKE_UP (read) Wakeup caused by AIN0_OV
2	VCUV1	R		VC_UV1 Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by VC_UV1
			1	WAKE_UP (read) Wakeup caused by VC_UV1
1	VCUV0	R		VC_UV0 Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by VC_UV0
			1	WAKE_UP (read) Wakeup caused by VC_UV0
0	VCOV	R		VC_OV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by VC_OV
			1	WAKE_UP (read) Wakeup caused by VC_OV

12.1.25 FEH_WAKEUP_REASON1 register

Wake-up reason register

Table 98. FEH_WAKEUP_REASON1 register - wake-up reason register (address 40Bh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							BALPROT
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						AINAUV	AINAOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 99. FEH_WAKEUP_REASON1 register - wake up reason register (address 40Bh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:9	reserved	R	0h	This read-only field is reserved and always has the value 0.
8	BALPROT	R		Balancing protection detection Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by detected Balancing protection
			1	WAKE_UP (read) Wakeup caused by detected Balancing protection
7:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	AINAUV	R		AIN0_UV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AINA_UV
			1	WAKE_UP (read) Wakeup caused by AINA_UV

Table 99. FEH_WAKEUP_REASON1 register - wake up reason register (address 40Bh)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
0	AINAOV	R		AINA_OV Read clears bit.
			0*	NO_WAKE (read) Wakeup not caused by AINA_OV
			1	WAKE_UP (read) Wakeup caused by AINA_OV

12.1.26 FEH_MON_BIST_CTRL register

Monitor BIST control register

Table 100. FEH_MON_BIST_CTRL register - monitor BIST control register (address 410h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	BISTCRC							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BISTCRC							STARTBIST
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	W

Table 101. FEH_MON_BIST_CTRL register - monitor BIST control register (address 410h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:1	BISTCRC	R/W	0h	CRC of the sequential BIST results. The value is different for the automatic BIST after start-up and a manual started BIST, as more monitors are then included. If the resulting CRC differs from the defined values, the BIST was not executed correctly.
			10B7h	STARTUP (read-write) Value 10B7h represents correct CRC value for start-up BIST
			4E3Dh	MAN_NO_VAUX (read-write) Value 4E3Dh represents the correct CRC value for a manual started BIST if VAUX is not enabled
			7742h	MANUAL (read-write) Value 7742h represents correct CRC value for manual started BIST
0	STARTBIST	W		Start BIST of all supply monitors, including VAUXOV, VAUXUV, VDDCOV and VDDCUV, which are not run at start-up. If the BIST is executed while measurements are running, some created secondary measurement results might be invalid. Read as zero.
			0*	NO_START (write) Do not start BIST
			0*	STATUS (read) Read as zero.
			1	START (write) Start BIST

12.1.27 FEH_MON_BIST_RES register

Monitor BIST result register; value changes at start up, if everything is fine to 0000h

Table 102. FEH_MON_BIST_RES register - Monitor BIST result register (address 411h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved				VDDCUV	VDDCOV	VAUXUV	VAUXOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	VPRERE FSUV	AFECPUV	AFECPOV	VANAUV	VANAOV	VDDAUV	VDDAOV	VBATOV
Reset	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R

Table 103. FEH_MON_BIST_RES register - Monitor BIST result register (address 411h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:12	reserved	R	0h	This read-only field is reserved and always has the value 0.
11	VDDCUV	R		VDDC Supply under-voltage BIST failed. Not part of start-up BIST, only executed for manual BIST execution.
			0*	PASS (read) BIST passed
			1	FAIL (read) BIST failed
10	VDDCOV	R		VDDC Supply over-voltage BIST failed. Not part of start-up BIST, only executed for manual BIST execution.
			0*	PASS (read) BIST passed
			1	FAIL (read) BIST failed
9	VAUXUV	R		VAUX Supply under-voltage BIST failed. Not part of start-up BIST, only executed for manual BIST execution.
			0*	PASS (read) BIST passed
			1	FAIL (read) BIST failed
8	VAUXOV	R		VAUX Supply over-voltage BIST failed. Not part of start-up BIST, only executed for manual BIST execution.
			0*	PASS (read) BIST passed
			1	FAIL (read) BIST failed
7	VPREREFSUV	R		VPREREFSUV Supply under-voltage BIST failed.
			0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed
6	AFECPUV	R		Analog Frontend Charge Pump under-voltage BIST failed.
			0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed
5	AFECPOV	R		Analog Frontend Charge Pump over-voltage BIST failed.
			0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed
4	VANAUV	R		VANA under-voltage BIST failed.
			0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed

Table 103. FEH_MON_BIST_RES register - Monitor BIST result register (address 411h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
3	VANAOV	R		VANA over-voltage BIST failed.
			0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed
2	VDDAUV	R		VDDA Supply under-voltage BIST failed.
			0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed
1	VDDAOV	R		VDDA Supply over-voltage BIST failed.
			0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed
0	VBATOV	R		VBAT Supply over-voltage BIST failed.
			0	PASS (read) BIST passed
			1*	FAIL (read) BIST failed

12.1.28 FEH_ACC_ERR register

Access error status register

Table 104. FEH_ACC_ERR register - access error status register (address 41Eh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	ERRSTAT	ERRACC	ERRADD					
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	ERRADD							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 105. FEH_ACC_ERR register - access error status register (address 41Eh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	ERRSTAT	R		Access error status Read clears bit.
			0*	NO_ERROR (read) No error occurred
			1	ERROR (read) Access error has occurred
14	ERRACC	R		Access type of the last access error Read clears bit.
			0*	READ (read) Last error occurred during a read access
			1	WRITE (read) Last error occurred during a write access
13:0	ERRADD	R	0h	Address of the last access which created an access error Read clears bits.

12.1.29 FEH_GRP_FLT_STAT register

Main system fault status register; this register holds one bit per fault group. For each fault group a separate status register exists. The bit here is cleared if all its sources are cleared.

Table 106. FEH_GRP_FLT_STAT register - Main system fault status register (address 41Fh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved				MEASFLT	COMFLT	ANAFLT	SUPPLYFLT
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 107. FEH_GRP_FLT_STAT register - Main system fault status register (address 41Fh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:4	reserved	R	0h	This read-only field is reserved and always has the value 0.
3	MEASFLT	R		Measurement fault status
			0*	NO_ERROR (read) No measurement fault detected
			1	ERROR (read) Measurement fault detected
2	COMFLT	R		Communication fault status
			0*	NO_ERROR (read) No communication fault detected
			1	ERROR (read) Communication fault detected.
1	ANAFLT	R		Analog fault status
			0*	NO_ERROR (read) No analog fault detected
			1	ERROR (read) Analog fault detected
0	SUPPLYFLT	R		Internal/external supply fault status
			0*	NO_ERROR (read) No supply error detected
			1	ERROR (read) Supply error detected

12.1.30 FEH_SUPPLY_FLT_STAT0 register

Supply fault status register 0 (these monitors are part of the BIST)

Table 108. FEH_SUPPLY_FLT_STAT0 register - Supply fault status register 0 (address 420h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved				VDDCUV	VDDCOV	VAUXUV	VAUXOV
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	VPRERE FSUV	AFECPUV	AFECPOV	VANAUV	VANAOV	VDDAUV	VDDAOV	VBATOV
Reset	0	0	0	0	0	0	0	0

Table 108. FEH_SUPPLY_FLT_STAT0 register - Supply fault status register 0 (address 420h) bit allocation*...continued*

Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 109. FEH_SUPPLY_FLT_STAT0 register - Supply fault status register 0 (address 420h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:12	reserved	R	0h	This read-only field is reserved and always has the value 0.
11	VDDCUV	R/W		VDDC Supply under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No VDDC Supply under-voltage detected.
			1	UV (read-write) VDDC Supply under-voltage detected.
10	VDDCOV	R/W		VDDC Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VDDC Supply over-voltage detected.
			1	OV (read-write) VDDC Supply over-voltage detected.
9	VAUXUV	R/W		VAUX Supply under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No VAUX Supply under-voltage detected.
			1	UV (read-write) VAUX Supply under-voltage detected.
8	VAUXOV	R/W		VAUX Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VAUX Supply over-voltage detected.
			1	OV (read-write) VAUX Supply over-voltage detected.
7	VPREREFSUV	R/W		VPREREFS Supply under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No VPREREFS Supply under-voltage detected.
			1	UV (read-write) VPREREFS Supply under-voltage detected.
6	AFECPUV	R/W		AFE Charge Pump under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No AFE Charge Pump under-voltage detected.
			1	UV (read-write) AFE Charge Pump under-voltage detected.
5	AFECPOV	R/W		AFE Charge Pump over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No AFE Charge Pump over-voltage detected.
			1	OV (read-write) AFE Charge Pump over-voltage detected.
4	VANAUV	R/W		VANA Supply under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No VANA Supply under-voltage detected.
			1	UV (read-write) VANA Supply under-voltage detected.
3	VANAOV	R/W		VANA Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VANA Supply over-voltage detected.
			1	OV (read-write) VANA Supply over-voltage detected.
2	VDDAUV	R/W		VDDA Supply under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No VDDA Supply under-voltage detected.

Table 109. FEH_SUPPLY_FLT_STAT0 register - Supply fault status register 0 (address 420h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			1	UV (read-write) VDDA Supply under-voltage detected.
1	VDDAOV	R/W		VDDA Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VDDA Supply over-voltage detected.
			1	OV (read-write) VDDA Supply over-voltage detected.
0	VBATOV	R/W		VBAT Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VBAT Supply over-voltage detected.
			1	OV (read-write) VBAT Supply over-voltage detected.

12.1.31 FEH_SUPPLY_FLT_STAT1 register

Supply fault status register 1 (these monitors are not part of the BIST)

Table 110. FEH_SUPPLY_FLT_STAT1 register - Supply fault status register 1 (address 421h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved	VPREUV	VPREOV	VDDIOUV	VDDIOOV	VDDCHC	VPRERE FSOV	VBATLV
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 111. FEH_SUPPLY_FLT_STAT1 register - Supply fault status register 1 (address 421h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:7	reserved	R	0h	This read-only field is reserved and always has the value 0.
6	VPREUV	R/W		VPRE Supply under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No VPRE Supply under-voltage detected.
			1	UV (read-write) VPRE Supply under-voltage detected.
5	VPREOV	R/W		VPRE Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VPRE Supply over-voltage detected.
			1	OV (read-write) VPRE Supply over-voltage detected.
4	VDDIOUV	R/W		VDDIO Supply under-voltage fault. Write 1 clears bit.
			0*	NO_UV (read-write) No VDDIO Supply under-voltage detected.
			1	UV (read-write) VDDIO Supply under-voltage detected.
3	VDDIOOV	R/W		VDDIO Supply over-voltage fault. Write 1 clears bit.

Table 111. FEH_SUPPLY_FLT_STAT1 register - Supply fault status register 1 (address 421h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	NO_OV (read-write) No VDDIO Supply over-voltage detected.
			1	OV (read-write) VDDIO Supply over-voltage detected.
2	VDDCHC	R/W		VDDC high-current fault. Write 1 clears bit.
			0*	NO_HC (read-write) No VDDC high-current detected.
			1	HC (read-write) VDDC high-current detected.
1	VPREREFSOV	R/W		VPREREFS Supply over-voltage fault. Write 1 clears bit.
			0*	NO_OV (read-write) No VPREREFS Supply over-voltage detected.
			1	OV (read-write) VPREREFS Supply over-voltage detected.
0	VBATLV	R/W		VBAT Supply low-voltage fault. Write 1 clears bit.
			0*	NO_LV (read-write) No VBAT Supply low-voltage detected.
			1	LV (read-write) VBAT Supply low-voltage detected.

12.1.32 FEH_ANA_FLT_STAT register

Analog fault status register

Table 112. FEH_ANA_FLT_STAT register - analog fault status register (address 422h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						BALFLT	MONBIST
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 113. FEH_ANA_FLT_STAT register - analog fault status register (address 422h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	BALFLT	R/W		Cell balance function fault. Write 1 clears bit.
			0*	NO_FLT (read-write) No cell balancing fault detected
			1	FAULT (read-write) Cell balancing fault detected
0	MONBIST	R/W		Monitor BIST failure fault. Write 1 clears bit.
			0*	NO_FLT (read-write) No monitor BIST failure detected.
			1	FAILURE (read-write) Monitor BIST failure detected.

12.1.33 FEH_COM_FLT_STAT register

Communication fault status register

Table 114. FEH_COM_FLT_STAT register - communication fault status register (address 423h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	COMERRCNT							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved			RSPLENERR	COMTO	ERRCNTOF	CRCERR	FRAMEERR
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W

Table 115. FEH_COM_FLT_STAT register - communication fault status register (address 423h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	COMERRCNT	R/W		Number of communication errors (frame errors, CRC errors) since last clear, counter saturates at 0xFF. Write with any data unequal 0 clears the counter. The counter value is preserved during Sleep mode. Write 1 clears bits. Write 1 clears bits.
			00h*	NO_ERROR (read-write) No communication error occurred
			01h	CNT (read-write) CNT errors occurred
			FFh	MAX (read-write) Maximum communication error counter = 255 communication errors occurred.
7:5	reserved	R	0h	This read-only field is reserved and always has the value 0.
4	RSPLENERR	R/W		Response length error Write 1 clears bit.
			0*	NO_ERROR (read-write) No response length error occurred
			1	ERROR (read-write) The number of SPI clocks did not fit to the length of a requested response
3	COMTO	R/W		Communication timeout fault status Write 1 clears bit.
			0*	NO_TIMEOUT (read-write) No communication timeout has happened.
			1	TIMEMOUT (read-write) Communication timeout has happened.
2	ERRCNTOF	R/W		Communication error counter overflow Write 1 clears bit.
			0*	NO_MAX (read-write) Communication error counter has not reached max value.
			1	MAX (read-write) Communication error counter has reached max value.
1	CRCERR	R/W		Communication CRC error Write 1 clears bit.
			0*	NO_ERROR (read-write) No communication CRC error detected.
			1	ERROR (read-write) Communication CRC error detected.
0	FRAMEERR	R/W		Communication frame error (Wrong number of bits or bit-length error) Write 1 clears bit.
			0*	NO_ERROR (read-write) No communication frame error detected.
			1	ERROR (read-write) Communication frame error detected.

12.1.34 FEH_MEAS_FLT_STAT register

Other fault status register

Table 116. FEH_MEAS_FLT_STAT register - other fault status register (address 424h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved					SYNCMEASFLT	SECCALCRCFLT	PRIMCALCRCFLT
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W

Table 117. FEH_MEAS_FLT_STAT register - other fault status register (address 424h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:3	reserved	R	0h	This read-only field is reserved and always has the value 0.
2	SYNCMEASFLT	R/W		Synchronization fault between the measurement units Write 1 clears bit.
			0*	NO_FLT (read-write) No synchronization fault between the measurement units for a Sync cycle has been detected..
			1	FAULT (read-write) Synchronization fault between the measurement units for a Sync cycle has been detected..
1	SECCALCRCFLT	R/W		A fault in the secondary measurement chain calibration data Write 1 clears bit.
			0*	NO_FLT (read-write) No fault in secondary measurement chain calibration data detected.
			1	FAULT (read-write) A fault in the secondary measurement chain calibration data has been detected.
0	PRIMCALCRCFLT	R/W		A fault in the primary measurement chain calibration data Write 1 clears bit.
			0*	NO_FLT (read-write) No fault in primary measurement chain calibration data detected.
			1	FAULT (read-write) A fault in the primary measurement chain calibration data has been detected.

12.1.35 FEH_SUPPLY_FLT_POR_CFG0 register

Supply fault POR selection 0

Table 118. FEH_SUPPLY_FLT_POR_CFG0 register - supply fault POR selection 0 (address 428h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved				VDDCUVEN	VDDCOVEN	VAUXUVEN	VAUXOVEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W

Table 118. FEH_SUPPLY_FLT_POR_CFG0 register - supply fault POR selection 0 (address 428h) bit allocation*...continued*

Bit	7	6	5	4	3	2	1	0
Symbol	VPREREFSUVEN	AFECPUVEN	AFECPOVEN	VANAUVEN	VANAOVEN	VDDAUVEN	VDDAOVEN	VBATOVEN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 119. FEH_SUPPLY_FLT_POR_CFG0 register - supply fault POR selection 0 (address 428h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:12	reserved	R	0h	This read-only field is reserved and always has the value 0.
11	VDDCUVEN	R/W		POR on VDDC under-voltage fault.
			0*	NO_POR (read-write) No POR in case of VDDC under-voltage
			1	POR (read-write) VDDC under-voltage error leads to POR
10	VDDCOVEN	R/W		POR on VDDC over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VDDC over-voltage
			1	POR (read-write) VDDC over-voltage error leads to POR
9	VAUXUVEN	R/W		POR on VAUX under-voltage fault.
			0*	NO_POR (read-write) No POR in case of VAUX supply under-voltage
			1	POR (read-write) VAUX supply under-voltage error leads to POR
8	VAUXOVEN	R/W		POR on VAUX over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VAUX supply over-voltage
			1	POR (read-write) VAUX supply over-voltage error leads to POR
7	VPREREFSUVEN	R/W		POR on VPREREFS Supply under-voltage fault.
			0*	NO_POR (read-write) No POR in case of VPREREFS supply under-voltage
			1	POR (read-write) VPREREFS supply under-voltage error leads to POR
6	AFECPUVEN	R/W		POR on AFE Charge Pump under-voltage fault.
			0*	NO_POR (read-write) No POR in case of AFE Charge Pump under-voltage
			1	POR (read-write) AFE Charge Pump under-voltage error leads to POR
5	AFECPOVEN	R/W		POR on AFE Charge Pump over-voltage fault.
			0*	NO_POR (read-write) No POR in case of AFE Charge Pump over-voltage
			1	POR (read-write) AFE Charge Pump over-voltage error leads to POR
4	VANAUVEN	R/W		POR on VANA Supply under-voltage fault.

Table 119. FEH_SUPPLY_FLT_POR_CFG0 register - supply fault POR selection 0 (address 428h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	NO_POR (read-write) No POR in case of VANA supply under-voltage
			1	POR (read-write) VANA supply under-voltage error leads to POR
3	VANAOVEN	R/W		POR on VANA Supply over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VANA supply over-voltage
			1	POR (read-write) VANA supply over-voltage error leads to POR
2	VDDAUVEN	R/W		POR on VDDA Supply under-voltage fault.
			0*	NO_POR (read-write) No POR in case of VDDA supply under-voltage
			1	POR (read-write) VDDA supply under-voltage error leads to POR
1	VDDAOVEN	R/W		POR on VDDA Supply over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VDDA supply over-voltage
			1	POR (read-write) VDDA supply over-voltage error leads to POR
0	VBATOVEN	R/W		POR on VBAT Supply over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VBAT supply over-voltage
			1	POR (read-write) VBAT supply over-voltage error leads to POR

12.1.36 FEH_SUPPLY_FLT_POR_CFG1 register

Supply fault POR selection 1

Table 120. FEH_SUPPLY_FLT_POR_CFG1 register - supply fault POR selection 1 (address 429h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved	VPREUVEN	VPREOVEN	VDDIOUVEN	VDDIOOVEN	VDDCHCEN	VPRERE FSOVEN	VBATLVEN
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 121. FEH_SUPPLY_FLT_POR_CFG1 register - supply fault POR selection 1 (address 429h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:7	reserved	R	0h	This read-only field is reserved and always has the value 0.
6	VPREUVEN	R/W		POR on VPRE Supply under-voltage fault.
			0*	NO_POR (read-write) No POR in case of VPRE supply under-voltage
			1	POR (read-write) VPRE supply under-voltage error leads to POR
5	VPREOVEN	R/W		POR on VPRE Supply over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VPRE over-voltage
			1	POR (read-write) VPRE over-voltage error leads to POR
4	VDDIOUVEN	R/W		POR on VDDIO Supply under-voltage fault.
			0*	NO_POR (read-write) No POR in case of VDDIO supply under-voltage
			1	POR (read-write) VDDIO supply under-voltage error leads to POR
3	VDDIOOVEN	R/W		POR on VDDIO Supply over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VDDIO supply over-voltage
			1	POR (read-write) VDDIO supply over-voltage error leads to POR
2	VDDCHCEN	R/W		POR on VDDC high-current fault.
			0*	NO_POR (read-write) No POR in case of VDDC high-current
			1	POR (read-write) VDDC high-current error leads to POR
1	VPREREFSOVEN	R/W		POR on VPREREFS Supply over-voltage fault.
			0*	NO_POR (read-write) No POR in case of VPREREFS over-voltage
			1	POR (read-write) VPREREFS over-voltage error leads to POR
0	VBATLVEN	R/W		POR on VBAT Supply low-voltage fault.
			0*	NO_POR (read-write) No POR in case of VBAT supply low-voltage
			1	POR (read-write) VBAT supply low-voltage error leads to POR

12.1.37 FEH_COM_FLT_POR_CFG register

Communication fault POR enable register

Table 122. FEH_COM_FLT_POR_CFG register - communication fault POR enable register (address 42Bh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Table 122. FEH_COM_FLT_POR_CFG register - communication fault POR enable register (address 42Bh) bit allocation*...continued*

Symbol	reserved				COMTOEN	ERRCNT OFEN	reserved	
Reset	0	0	0	0	1	0	0	0
Access	R	R	R	R	R/W	R/W	R	R

Table 123. FEH_COM_FLT_POR_CFG register - communication fault POR enable register (address 42Bh)
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:4	reserved	R	0h	This read-only field is reserved and always has the value 0.
3	COMTOEN	R/W		Create a POR if a communication timeout happens.
			0	PREV_MOD (read-write) Device fallbacks to prev. Mode in case of communication timeout
			1*	POR (read-write) POR in case of communication timeout
2	ERRCNTOFEN	R/W		Communication error counter max value leads to POR
			0*	NO_POR (read-write) Communication error counter has reached max value.
			1	POR (read-write) Communication error counter max value leads to POR
1:0	reserved	R	0h	This read-only field is reserved and always has the value 0.

12.1.38 FEH_SUPPLY_FLT_EVT_CFG0 register

Supply fault event selection register 0

Table 124. FEH_SUPPLY_FLT_EVT_CFG0 register - supply fault event selection register 0 (address 430h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved				VDDCUVEN	VDDCOVEN	VAUXUVEN	VAUXOVEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	VPRERE FSUVEN	AFECPUVEN	AFECPOVEN	VANAUVEN	VANAOVEN	VDDAUVEN	VDDAOVEN	VBATOVEN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 125. FEH_SUPPLY_FLT_EVT_CFG0 register - supply fault event selection register 0 (address 430h)
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:12	reserved	R	0h	This read-only field is reserved and always has the value 0.
11	VDDCUVEN	R/W		Event on VDDC under-voltage fault.
			0*	NO_EV (read-write) No event on VDDC under-voltage fault.
			1	EVENT (read-write) Event on VDDC under-voltage fault.

Table 125. FEH_SUPPLY_FLT_EVT_CFG0 register - supply fault event selection register 0 (address 430h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
10	VDDCOVEN	R/W		Event on VDDC over-voltage fault.
			0*	NO_EV (read-write) No event on VDDC over-voltage fault.
			1	EVENT (read-write) Event on VDDC over-voltage fault.
9	VAUXUVEN	R/W		Event on VAUX under-voltage fault.
			0*	NO_EV (read-write) No event on VAUX under-voltage fault.
			1	EVENT (read-write) Event on VAUX under-voltage fault.
8	VAUXOVEN	R/W		Event on VAUX over-voltage fault.
			0*	NO_EV (read-write) No event on VAUX over-voltage fault.
			1	EVENT (read-write) Event on VAUX over-voltage fault.
7	VPREREFSUVEN	R/W		Event on VPREREFS Supply under-voltage fault.
			0*	NO_EV (read-write) No event on VPREREFS Supply under-voltage fault.
			1	EVENT (read-write) Event on VPREREFS Supply under-voltage fault.
6	AFECPUVEN	R/W		Event on AFE Charge Pump under-voltage fault.
			0*	NO_EV (read-write) No event on AFE Charge Pump under-voltage fault.
			1	EVENT (read-write) Event on AFE Charge Pump under-voltage fault.
5	AFECPOVEN	R/W		Event on AFE Charge Pump over-voltage fault.
			0*	NO_EV (read-write) No event on AFE Charge Pump over-voltage fault.
			1	EVENT (read-write) Event on AFE Charge Pump over-voltage fault.
4	VANAUVEN	R/W		Event on VANA Supply under-voltage fault.
			0*	NO_EV (read-write) No event on VANA Supply under-voltage fault.
			1	EVENT (read-write) Event on VANA Supply under-voltage fault.
3	VANAOVEN	R/W		Event on VANA Supply over-voltage fault.
			0*	NO_EV (read-write) No event on VANA Supply over-voltage fault.
			1	EVENT (read-write) Event on VANA Supply over-voltage fault.
2	VDDAUVEN	R/W		Event on VDDA Supply under-voltage fault.
			0*	NO_EV (read-write) No event on VDDA Supply under-voltage fault.
			1	EVENT (read-write) Event on VDDA Supply under-voltage fault.
1	VDDAOVEN	R/W		Event on VDDA Supply over-voltage fault.
			0*	NO_EV (read-write) No event on VDDA Supply over-voltage fault.
			1	EVENT (read-write) Event on VDDA Supply over-voltage fault.

Table 125. FEH_SUPPLY_FLT_EVT_CFG0 register - supply fault event selection register 0 (address 430h)...*continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
0	VBATOVEN	R/W		Event on VBAT Supply over-voltage fault.
			0*	NO_EV (read-write) No event on VBAT Supply over-voltage fault.
			1	EVENT (read-write) Event on VBAT Supply over-voltage fault.

12.1.39 FEH_SUPPLY_FLT_EVT_CFG1 register

Supply fault event selection register 1

Table 126. FEH_SUPPLY_FLT_EVT_CFG1 register - supply fault event selection register 1 (address 431h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved	VPREUVEN	VPREOVEN	VDDIOUVEN	VDDIOOVEN	VDDCHCEN	VPRERE FSOVEN	VBATLVEN
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 127. FEH_SUPPLY_FLT_EVT_CFG1 register - supply fault event selection register 1 (address 431h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:7	reserved	R	0h	This read-only field is reserved and always has the value 0.
6	VPREUVEN	R/W		Event on VPRE Supply under-voltage fault.
			0*	NO_EV (read-write) No event on VPRE Supply under-voltage fault.
			1	EVENT (read-write) Event on VPRE Supply under-voltage fault.
5	VPREOVEN	R/W		Event on VPRE Supply over-voltage fault.
			0*	NO_EV (read-write) No event on VPRE Supply over-voltage fault.
			1	EVENT (read-write) Event on VPRE Supply over-voltage fault.
4	VDDIOUVEN	R/W		Event on VDDIO Supply under-voltage fault.
			0*	NO_EV (read-write) No event on VDDIO Supply under-voltage fault.
			1	EVENT (read-write) Event on VDDIO Supply under-voltage fault.
3	VDDIOOVEN	R/W		Event on VDDIO Supply over-voltage fault.
			0*	NO_EV (read-write) No event on VDDIO Supply over-voltage fault.

Table 127. FEH_SUPPLY_FLT_EVT_CFG1 register - supply fault event selection register 1 (address 431h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			1	EVENT (read-write) Event on VDDIO Supply over-voltage fault.
2	VDDCHCEN	R/W		Event on VDDC high-current fault.
			0*	NO_EV (read-write) No event on VDDC high-current fault.
			1	EVENT (read-write) Event on VDDC high-current fault.
1	VPREREFSOVEN	R/W		Event on VPREREFS Supply over-voltage fault.
			0*	NO_EV (read-write) No event on VPREREFS Supply over-voltage fault.
			1	EVENT (read-write) Event on VPREREFS Supply over-voltage fault.
0	VBATLVEN	R/W		Event on VBAT Supply low-voltage fault.
			0*	NO_EV (read-write) No event on VBAT Supply low-voltage fault.
			1	EVENT (read-write) Event on VBAT Supply low-voltage fault.

12.1.40 FEH_ANA_FLT_EVT_CFG register

Analog fault event enable register

Table 128. FEH_ANA_FLT_EVT_CFG register - analog fault event enable register (address 432h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						BALFLTEN	MONBISTEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 129. FEH_ANA_FLT_EVT_CFG register - analog fault event enable register (address 432h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	BALFLTEN	R/W		Event on cell balance function fault.
			0*	NO_EV (read-write) No event on cell balance function fault.
			1	EVENT (read-write) Event on cell balance function fault.
0	MONBISTEN	R/W		Event on Monitor BIST fault.
			0*	NO_EV (read-write) No event on Monitor BIST fault.
			1	EVENT (read-write) Event on Monitor BIST fault.

12.1.41 FEH_COM_FLT_EVT_CFG register

Communication fault event enable register

Table 130. FEH_COM_FLT_EVT_CFG register - communication fault event enable register (address 433h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved			RSPLEN ERREN	reserved	ERRCNT OFEN	CRCERREN	FRAMEE RREN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R	R/W	R/W	R/W

Table 131. FEH_COM_FLT_EVT_CFG register - communication fault event enable register (address 433h)
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:5	reserved	R	0h	This read-only field is reserved and always has the value 0.
4	RSPLENERREN	R/W		Event on number of SPI clocks did not fit to the length of a requested response
			0*	NO_EV (read-write) No event on number of SPI clocks did not fit to the length of a requested response
			1	EVENT (read-write) Event on number of SPI clocks did not fit to the length of a requested response
3	reserved	R	0h	This read-only field is reserved and always has the value 0.
2	ERRCNTOFEN	R/W		Event on communication error counter has reached max value.
			0*	NO_EV (read-write) No event on communication error counter has reached max value.
			1	EVENT (read-write) Event on communication error counter has reached max value.
1	CRCERREN	R/W		Event on communication CRC error detected.
			0*	NO_EV (read-write) No event on communication CRC error detected.
			1	EVENT (read-write) Event on communication CRC error detected.
0	FRAMEERREN	R/W		Event on communication error detected. Wrong number of bits, bit-length error.
			0*	NO_EV (read-write) No event on communication error detected.
			1	EVENT (read-write) Event on communication error detected.

12.1.42 FEH_MEAS_FLT_EVT_CFG register

Measurement fault event enable register

Table 132. FEH_MEAS_FLT_EVT_CFG register - measurement fault event enable register (address 434h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved					SYNCMEASFLTEN	SECCALCRCFLTEN	PRIMCALCRCFLTEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W

Table 133. FEH_MEAS_FLT_EVT_CFG register - measurement fault event enable register (address 434h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:3	reserved	R	0h	This read-only field is reserved and always has the value 0.
2	SYNCMEASFLTEN	R/W		Event on synchronization fault between the measurement units for a Sync cycle.
			0*	NO_EV (read-write) No event on synchronization fault.
			1	EVENT (read-write) Event on synchronization fault.
1	SECCALCRCFLTEN	R/W		Event on secondary calibration CRC fault.
			0*	NO_EV (read-write) No event on secondary calibration CRC fault.
			1	EVENT (read-write) Event on secondary calibration CRC fault.
0	PRIMCALCRCFLTEN	R/W		Event on primary calibration CRC fault.
			0*	NO_EV (read-write) No event on primary calibration CRC fault.
			1	EVENT (read-write) Event on primary calibration CRC fault.

12.1.43 FEH_POR_REASON register

Power-on reset reason. The value is stored in the ULP domain.

Table 134. FEH_POR_REASON register - power on reset reason (address 480h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved						SOURCE									
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 135. FEH_POR_REASON register - power on reset reason (address 480h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:10	reserved	R	0h	This read-only field is reserved and always has the value 0.

Table 135. FEH_POR_REASON register - power on reset reason (address 480h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
9:0	SOURCE	R		Reason for POR. POR sources are binary coded and protected by an EDC. **Other** values as shown below represent errors in EDC.
			000h*	VDDDLPPERMUV (read) POR caused by VDDDLP PERMUV
			00Fh	VDDDLPUV (read) POR caused by VDDDLPUV
			04Eh	VDDDUV (read) POR caused by VDDDUV
			083h	VBATLV (read) POR caused by VBATLV
			08Ch	VDDIOUV (read) POR caused by VDDIOUV
			0BFh	SWRESET (read) POR caused by software Deep Sleep request
			0C2h	VBATOV (read) POR caused by VBATOV
			0CDh	VDDDOV (read) POR caused by VDDDOV
			105h	VDDCOV (read) POR caused by VDDCOV
			10Ah	VAUXUV (read) POR caused by VAUXUV
			144h	VBATUV (read) POR caused by VBATUV
			14Bh	VDDIOOV (read) POR caused by VDDIOOV
			186h	VDDCUV (read) POR caused by VDDCUV
			189h	VAUXOV (read) POR caused by VAUXOV
			1C7h	VDDCOC (read) POR caused by VDDCOC
			1C8h	VDDCHC (read) POR caused by VDDCHC
			211h	VDDAUV (read) POR caused by VDDAUV
			21Eh	SLEEPOSC (read) POR caused by SLEEPOSC
			222h	VPREUV (read) POR caused by VPREUV
			250h	VDDAOV (read) POR caused by VDDAOV
			25Fh	COMTO (read) POR caused by COMTO
			292h	VPREOV (read) POR caused by VPREOV
			29Dh	SECCLK (read) POR caused by SECCLK
			2A1h	LOGICERR (read) POR caused by LOGICERR
			2D3h	VPREREFSOV (read) POR caused by VPREREFSOV
			2DCh	PRMCLK (read) POR caused by PRMCLK
			2E0h	COMERRORS (read) POR caused by COMERRORS
			314h	VPREREFSUV (read) POR caused by VPREREFSUV
			31Bh	OTEMPSHUTDOWN (read) POR caused by OTEMPSHUT DOWN
			355h	VANAOV (read) POR caused by VANAOV
			397h	AFECPOV (read) POR caused by AFECPOV
			398h	AFECPUV (read) POR caused by AFECPUV
			3D6h	VANAUV (read) POR caused by VANAUV

12.1.44 GPIO_CFG0 register

GPIO configuration 0

Table 136. GPIO_CFG0 register - GPIO configuration 0 (address 800h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	OUTEN7	OUTEN6	OUTEN5	OUTEN4	OUTEN3	OUTEN2	OUTEN1	OUTEN0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	INPEN7	INPEN6	INPEN5	INPEN4	INPEN3	INPEN2	INPEN1	INPEN0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 137. GPIO_CFG0 register - GPIO configuration 0 (address 800h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	OUTEN7	R/W		Enable the output of the GPIO7.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
14	OUTEN6	R/W		Enable the output of the GPIO6.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
13	OUTEN5	R/W		Enable the output of the GPIO5.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
12	OUTEN4	R/W		Enable the output of the GPIO4.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
11	OUTEN3	R/W		Enable the output of the GPIO3.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
10	OUTEN2	R/W		Enable the output of the GPIO2.

Table 137. GPIO_CFG0 register - GPIO configuration 0 (address 800h) *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
9	OUTEN1	R/W		Enable the output of the GPIO1.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
8	OUTEN0	R/W		Enable the output of the GPIO0.
			0*	DISABLED (read-write) Output is disabled
			1	ENABLED (read-write) Output is enabled. If an analog measurement function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in this bit.
7	INPEN7	R/W		Enable the input for GPIO7. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled
6	INPEN6	R/W		Enable the input for GPIO6. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled
5	INPEN5	R/W		Enable the input for GPIO5. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled
4	INPEN4	R/W		Enable the input for GPIO4. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled
3	INPEN3	R/W		Enable the input for GPIO3. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled
2	INPEN2	R/W		Enable the input for GPIO2. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled

Table 137. GPIO_CFG0 register - GPIO configuration 0 (address 800h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
1	INPEN1	R/W		Enable the input for GPIO1. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled
0	INPEN0	R/W		Enable the input for GPIO0. If a special function requires digital input, the according receiver is enabled automatically. This is not reflected in this bit.
			0*	DISABLED (read-write) Input is disabled
			1	ENABLED (read-write) Input is enabled

12.1.45 GPIO_CFG1 register

GPIO configuration 1

Table 138. GPIO_CFG1 register - GPIO configuration 1 (address 801h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	ODEN7	ODEN6	ODEN5	ODEN4	ODEN3	ODEN2	ODEN1	ODEN0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 139. GPIO_CFG1 register - GPIO configuration 1 (address 801h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7	ODEN7	R/W		Open Drain enable, GPIO7.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled
6	ODEN6	R/W		Open Drain enable, GPIO6.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled
5	ODEN5	R/W		Open Drain enable, GPIO5.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled
4	ODEN4	R/W		Open Drain enable, GPIO4.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled

Table 139. GPIO_CFG1 register - GPIO configuration 1 (address 801h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
3	ODEN3	R/W		Open Drain enable, GPIO3.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled
2	ODEN2	R/W		Open Drain enable, GPIO2.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled
1	ODEN1	R/W		Open Drain enable, GPIO1.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled
0	ODEN0	R/W		Open Drain enable, GPIO0.
			0*	DISABLED (read-write) Open Drain disabled
			1	ENABLED (read-write) Open Drain enabled

12.1.46 GPIO_OUT register

GPIO output

Table 140. GPIO_OUT register - GPIO output (address 802h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	OUT7	OUT6	OUT5	OUT4	OUT3	OUT2	OUT1	OUT0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 141. GPIO_OUT register - GPIO output (address 802h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7	OUT7	R/W		Set the output level of the gpio function for GPIO7.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high
6	OUT6	R/W		Set the output level of the gpio function for GPIO6.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high
5	OUT5	R/W		Set the output level of the gpio function for GPIO5.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high

Table 141. GPIO_OUT register - GPIO output (address 802h) *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
4	OUT4	R/W		Set the output level of the gpio function for GPIO4.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high
3	OUT3	R/W		Set the output level of the gpio function for GPIO3.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high
2	OUT2	R/W		Set the output level of the gpio function for GPIO2.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high
1	OUT1	R/W		Set the output level of the gpio function for GPIO1.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high
0	OUT0	R/W		Set the output level of the gpio function for GPIO0.
			0*	LOW (read-write) GPIO is low
			1	HIGH (read-write) GPIO is high

12.1.47 GPIO_IN register

GPIO input

Table 142. GPIO_IN register - GPIO input (address 804h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	HIGHDET7	HIGHDET6	HIGHDET5	HIGHDET4	HIGHDET3	HIGHDET2	HIGHDET1	HIGHDET0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	IN7	IN6	IN5	IN4	IN3	IN2	IN1	IN0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 143. GPIO_IN register - GPIO input (address 804h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	HIGHDET7	R		High value on GPIO7. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
14	HIGHDET6	R		High value on GPIO6. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
13	HIGHDET5	R		High value on GPIO5. Read clears bit.

Table 143. GPIO_IN register - GPIO input (address 804h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
12	HIGHDET4	R		High value on GPIO4. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
11	HIGHDET3	R		High value on GPIO3. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
10	HIGHDET2	R		High value on GPIO2. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
9	HIGHDET1	R		High value on GPIO1. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
8	HIGHDET0	R		High value on GPIO0. Read clears bit.
			0*	NO_HIGH (read) No high level observed
			1	HIGH (read) High level observed.
7	IN7	R		Read the level of the gpio function of GPIO7.
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high
6	IN6	R		Read the level of the gpio function of GPIO6.
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high
5	IN5	R		Read the level of the gpio function of GPIO5.
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high
4	IN4	R		Read the level of the gpio function of GPIO4.
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high
3	IN3	R		Read the level of the gpio function of GPIO3.
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high
2	IN2	R		Read the level of the gpio function of GPIO2.
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high
1	IN1	R		Read the level of the gpio function of GPIO1.
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high
0	IN0	R		Read the level of the gpio function of GPIO0.

Table 143. GPIO_IN register - GPIO input (address 804h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	LOW (read) GPIO is low
			1	HIGH (read) GPIO is high

12.1.48 I2C_CFG register

I2C configuration

Table 144. I2C_CFG register - I2C configuration (address C00h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved					CLKSEL		EN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W

Table 145. I2C_CFG register - I2C configuration (address C00h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:3	reserved	R	0h	This read-only field is reserved and always has the value 0.
2:1	CLKSEL	R/W		I^2C-bus clock selection
			00*	F_100k (read-write) Clock is 100 kHz
			01	F_400k (read-write) Clock is 400 kHz
			10	F_1000k (read-write) Clock is 1000 kHz
			11	RESERVED (read-write) Reserved. Do not use.
0	EN	R/W		Enable I^2C-bus interface. If the I^2C-bus interface is disabled while it is active, a stop condition is created and the bus is released. When enabling this bit the GPIO to which the I^2C-bus lines are connected are switched to the I^2C-bus function (input receiver active and open-drain output function).
			0*	DISABLED (read-write) Interface disabled
			1	ENABLED (read-write) Interface enabled

12.1.49 I2C_CTRL register

I2C control

Table 146. I2C_CTRL register - I2C control (address C01h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved		RDAFTER					
Reset	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 146. I2C_CTRL register - I2C control (address C01h) bit allocation*...continued*

Bit	7	6	5	4	3	2	1	0
Symbol	reserved	STPAFTER	START					
Reset	0	0	0	0	0	0	0	0
Access	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 147. I2C_CTRL register - I2C control (address C01h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:8	RDAFTER	R/W		Switch to read after **RDAFTER** bytes. Repeats the start condition after byte **RDAFTER**.
			00h*	NO_READ (read-write) No switch to read.
			01h	READ_1 (read-write) Switch to read after 1 byte
			24h	READ_36 (read-write) Switch to read after 36 bytes
			25h	RESERVED (read-write) Reserved. Do not use.
7	reserved	R	0h	This read-only field is reserved and always has the value 0.
6	STPAFTER	R/W		Send a stop condition after the last byte.
			0*	NO_STOP (read-write) No stop condition sent after last byte
			1	STOP (read-write) Stop condition sent after last byte
5:0	START	R/W	0h	Starts the I^2C-bus transmission and sends **START** bytes (including Dev. Address to be transmitted/read).
			01h	SEND_1 (read-write) Send one byte
			24h	SEND_36 (read-write) Send 36 bytes
			25h	SEND_MAX (read-write) Send 36 bytes

12.1.50 I2C_STAT register

I2C status

Table 148. I2C_STAT register - I2C status (address C02h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved		LEN					
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved				ARBLOST	NACKRCV	ACTIVE	PENDING
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 149. I2C_STAT register - I2C status (address C02h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:8	LEN	R		**LEN** bytes transferred until NACK received.
			00h*	NACK_0 (read) No bytes transmitted until NACK was received
			01h	NACK_1 (read) 1 byte transmitted until NACK was received
			24h	NACK_36 (read) 36 bytes transmitted until NACK was received
			25h	RESERVED (read) Reserved. Not used.
7:4	reserved	R	0h	This read-only field is reserved and always has the value 0.
3	ARBLOST	R		Wrong data bit
			0*	NO_FLT (read) No wrong data bits detected
			1	FAULT (read) A wrong data bit was detected
2	NACKRCV	R		NACK received
			0*	NO_NACK (read) No NACK was received
			1	NACK (read) A NACK was received
1	ACTIVE	R		I^2C-bus execution pending
			0*	NO_TRX (read) No transaction is ongoing.
			1	TRX (read) A transaction is ongoing (no STOP condition so far), bus is held with SCL low
0	PENDING	R		I^2C-bus execution pending
			0*	NO_TRX (read) No transfer is in execution, data registers can be accessed
			1	TRX (read) A transfer is in execution, no access to the data registers is allowed

12.1.51 I2C_DATA0 register

I2C data register 0

Table 150. I2C_DATA0 register - I2C data register 0 (address C04h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE1								BYTE0							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 151. I2C_DATA0 register - I2C data register 0 (address C04h)

Bit	Symbol	Access	Value	Description
15:8	BYTE1	R/W	0h	I^2C-bus data byte 1 (for example data or sub address)
7:0	BYTE0	R/W	0h	I^2C-bus data byte 0 (for example device address)

12.1.52 I2C_DATA1 register

I2C data register 1

Table 152. I2C_DATA1 register - I2C data register 1 (address C05h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE3								BYTE2							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 153. I2C_DATA1 register - I2C data register 1 (address C05h)

Bit	Symbol	Access	Value	Description
15:8	BYTE3	R/W	0h	I^2C-bus data byte 3
7:0	BYTE2	R/W	0h	I^2C-bus data byte 2

12.1.53 I2C_DATA2 register

I2C data register 2

Table 154. I2C_DATA2 register - I2C data register 2 (address C06h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE5								BYTE4							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 155. I2C_DATA2 register - I2C data register 2 (address C06h)

Bit	Symbol	Access	Value	Description
15:8	BYTE5	R/W	0h	I^2C-bus data byte 5
7:0	BYTE4	R/W	0h	I^2C-bus data byte 4

12.1.54 I2C_DATA3 register

I2C data register 3

Table 156. I2C_DATA3 register - I2C data register 3 (address C07h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE7								BYTE6							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 157. I2C_DATA3 register - I2C data register 3 (address C07h)

Bit	Symbol	Access	Value	Description
15:8	BYTE7	R/W	0h	I^2C-bus data byte 7
7:0	BYTE6	R/W	0h	I^2C-bus data byte 6

Table 157. I2C_DATA3 register - I2C data register 3 (address C07h)*...continued*

Bit	Symbol	Access	Value	Description

12.1.55 I2C_DATA4 register

I2C data register 4

Table 158. I2C_DATA4 register - I2C data register 4 (address C08h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE9								BYTE8							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 159. I2C_DATA4 register - I2C data register 4 (address C08h)

Bit	Symbol	Access	Value	Description
15:8	BYTE9	R/W	0h	I^2C-bus data byte 9
7:0	BYTE8	R/W	0h	I^2C-bus data byte 8

12.1.56 I2C_DATA5 register

I2C data register 5

Table 160. I2C_DATA5 register - I2C data register 5 (address C09h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE11								BYTE10							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 161. I2C_DATA5 register - I2C data register 5 (address C09h)

Bit	Symbol	Access	Value	Description
15:8	BYTE11	R/W	0h	I^2C-bus data byte 11
7:0	BYTE10	R/W	0h	I^2C-bus data byte 10

12.1.57 I2C_DATA6 register

I2C data register 6

Table 162. I2C_DATA6 register - I2C data register 6 (address C0Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE13								BYTE12							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 163. I2C_DATA6 register - I2C data register 6 (address C0Ah)

Bit	Symbol	Access	Value	Description
15:8	BYTE13	R/W	0h	I^2C-bus data byte 13
7:0	BYTE12	R/W	0h	I^2C-bus data byte 12

12.1.58 I2C_DATA7 register

I2C data register 7

Table 164. I2C_DATA7 register - I2C data register 7 (address C0Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE15								BYTE14							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 165. I2C_DATA7 register - I2C data register 7 (address C0Bh)

Bit	Symbol	Access	Value	Description
15:8	BYTE15	R/W	0h	I^2C-bus data byte 15
7:0	BYTE14	R/W	0h	I^2C-bus data byte 14

12.1.59 I2C_DATA8 register

I2C data register 8

Table 166. I2C_DATA8 register - I2C data register 8 (address C0Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE17								BYTE16							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 167. I2C_DATA8 register - I2C data register 8 (address C0Ch)

Bit	Symbol	Access	Value	Description
15:8	BYTE17	R/W	0h	I^2C-bus data byte 17
7:0	BYTE16	R/W	0h	I^2C-bus data byte 16

12.1.60 I2C_DATA9 register

I2C data register 9

Table 168. I2C_DATA9 register - I2C data register 9 (address C0Dh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE19								BYTE18							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 169. I2C_DATA9 register - I2C data register 9 (address C0Dh)

Bit	Symbol	Access	Value	Description
15:8	BYTE19	R/W	0h	I^{2}C-bus data byte 19
7:0	BYTE18	R/W	0h	I^{2}C-bus data byte 18

12.1.61 I2C_DATA10 register

I2C data register 10

Table 170. I2C_DATA10 register - I2C data register 10 (address C0Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE21								BYTE20							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 171. I2C_DATA10 register - I2C data register 10 (address C0Eh)

Bit	Symbol	Access	Value	Description
15:8	BYTE21	R/W	0h	I^{2}C-bus data byte 21
7:0	BYTE20	R/W	0h	I^{2}C-bus data byte 20

12.1.62 I2C_DATA11 register

I2C data register 11

Table 172. I2C_DATA11 register - I2C data register 11 (address C0Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE23								BYTE22							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 173. I2C_DATA11 register - I2C data register 11 (address C0Fh)

Bit	Symbol	Access	Value	Description
15:8	BYTE23	R/W	0h	I^{2}C-bus data byte 23
7:0	BYTE22	R/W	0h	I^{2}C-bus data byte 22

12.1.63 I2C_DATA12 register

I2C data register 12

Table 174. I2C_DATA12 register - I2C data register 12 (address C10h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE25								BYTE24							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 175. I2C_DATA12 register - I2C data register 12 (address C10h)

Bit	Symbol	Access	Value	Description
15:8	BYTE25	R/W	0h	I^2C-bus data byte 25
7:0	BYTE24	R/W	0h	I^2C-bus data byte 24

12.1.64 I2C_DATA13 register

I2C data register 13

Table 176. I2C_DATA13 register - I2C data register 13 (address C11h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE27								BYTE26							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 177. I2C_DATA13 register - I2C data register 13 (address C11h)

Bit	Symbol	Access	Value	Description
15:8	BYTE27	R/W	0h	I^2C-bus data byte 27
7:0	BYTE26	R/W	0h	I^2C-bus data byte 26

12.1.65 I2C_DATA14 register

I2C data register 14

Table 178. I2C_DATA14 register - I2C data register 14 (address C12h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE29								BYTE28							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 179. I2C_DATA14 register - I2C data register 14 (address C12h)

Bit	Symbol	Access	Value	Description
15:8	BYTE29	R/W	0h	I^2C-bus data byte 29
7:0	BYTE28	R/W	0h	I^2C-bus data byte 28

12.1.66 I2C_DATA15 register

I2C data register 15

Table 180. I2C_DATA15 register - I2C data register 15 (address C13h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE31								BYTE30							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 181. I2C_DATA15 register - I2C data register 15 (address C13h)

Bit	Symbol	Access	Value	Description
15:8	BYTE31	R/W	0h	I^2C-bus data byte 31
7:0	BYTE30	R/W	0h	I^2C-bus data byte 30

12.1.67 I2C_DATA16 register

I2C data register 16

Table 182. I2C_DATA16 register - I2C data register 16 (address C14h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE33								BYTE32							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 183. I2C_DATA16 register - I2C data register 16 (address C14h)

Bit	Symbol	Access	Value	Description
15:8	BYTE33	R/W	0h	I^2C-bus data byte 33
7:0	BYTE32	R/W	0h	I^2C-bus data byte 32

12.1.68 I2C_DATA17 register

I2C data register 17

Table 184. I2C_DATA17 register - I2C data register 17 (address C15h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	BYTE35								BYTE34							
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 185. I2C_DATA17 register - I2C data register 17 (address C15h)

Bit	Symbol	Access	Value	Description
15:8	BYTE35	R/W	0h	I^2C-bus data byte 35
7:0	BYTE34	R/W	0h	I^2C-bus data byte 34

12.1.69 BAL_GLOB_CFG register

The global balancing configuration register is used to configure the balancing modes.

Table 186. BAL_GLOB_CFG register - Global Balancing Configuration (address 1000h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved					TEMPSRC		
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Table 186. BAL_GLOB_CFG register - Global Balancing Configuration (address 1000h) bit allocation...*continued*

Symbol	reserved		CCMBALEN	TEMPMO DBALEN	GLOBUV1 BALEN	CHUV0 BALEN	TMRBALEN	BALEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 187. BAL_GLOB_CFG register - Global Balancing Configuration (address 1000h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:11	reserved	R	0h	This read-only field is reserved and always has the value 0.
10:8	TEMPSRC	R/W		Selects the source channel (AINx) for temperature modulated balancing. The MSB is ignored.
			000*	AIN0 (read-write) Selects AIN0 as source for temperature measurement.
			001	AIN1 (read-write) Selects AIN1 as source for temperature measurement.
			010	AIN2 (read-write) Selects AIN2 as source for temperature measurement.
			011	AIN3 (read-write) Selects AIN3 as source for temperature measurement.
7:6	reserved	R	0h	This read-only field is reserved and always has the value 0.
5	CCMBALEN	R/W		Enables the constant current balancing. When active the product adapts automatically the PWM duty cycle of the activated balancing channels based on their primary periodic measurement results to limit the balancing current variation due to cell voltage variation.
			0*	NOCCM (read-write) Constant Current Balancing is not active.
			1	CCM (read-write) Constant Current Balancing is active.
4	TEMPMODBALEN	R/W		Enables the temperature modulated balancing. After an over-temperature condition the balancing is halted until an under-temperature condition is detected.
			0*	NOTEMPMOD (read-write) Balancing is not temperature modulated.
			1	TEMPMOD (read-write) Balancing is temperature modulated.
3	GLOBUV1BALEN	R/W		Enables the Global undervoltage based balancing feature.
			0*	INDEPENDENT (read-write) Balancing is independent of the global undervoltage threshold.
			1	STOP (read-write) Balancing for all cells stops once the global undervoltage threshold is reached by any cell.
2	CHUV0BALEN	R/W		Enables the voltage based balancing for the individual channel. Balancing stops once each individual channel reaches the under-voltage threshold.
			0*	INDEPENDENT (read-write) Balancing is independent of the cell undervoltage threshold.
			1	STOP (read-write) Balancing for the individual cells stops once the cell undervoltage threshold is reached.
1	TMRBALEN	R/W		Enables the timer based balancing feature. All channel individual counters are stopped if zero.

Table 187. BAL_GLOB_CFG register - Global Balancing Configuration (address 1000h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	INDEPENDENT (read-write) Balancing is independent of the cell balancing timer.
			1	STOP (read-write) Balancing for all cells will be stopped when cell balancing timer expires.
0	BALEN	R/W		Enables the balancing activity. This bit is cleared in case of a balancing timeout or if an enabled global under-voltage condition is reached. All channel individual counters are stopped if zero. The emergency discharge works without setting this bit.
			0*	DISABLED (read-write) Balancing is disabled.
			1	ENABLED (read-write) Balancing is enabled.

12.1.70 BAL_GLOB_TO_TMR register

The Global Balancing timeout timer register is used to configure the maximum balancing time for all balancing activities to make sure that in case of fault the balancing switches are switched OFF.

Table 188. BAL_GLOB_TO_TMR register - Global Balancing Timeout (address 1001h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	TOTIME															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 189. BAL_GLOB_TO_TMR register - Global Balancing Timeout (address 1001h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:0	TOTIME	R/W		Balancing timeout value, used for normal balancing. The value of this field represents the current counter value when read. The BAL_GLOB_CFG.BALEN is cleared when zero is reached. The counter saturates at zero. It counts down regardless of the balancing enable state as long as its value is non-zero. **TOTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is expired
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			FFFFh	MAX (read-write) Maximum balancing time = 655350 seconds = approximately 182 hours = approximately 7.6 days

12.1.71 BAL_CH_CFG0 register

Balancing channel individual enable channel 0 - 15

Table 190. BAL_CH_CFG0 register - balancing channel individual enable channel 0 - 15 (address 1002h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	CHEN15	CHEN14	CHEN13	CHEN12	CHEN11	CHEN10	CHEN9	CHEN8
Reset	0	0	0	0	0	0	0	0

Table 190. BAL_CH_CFG0 register - balancing channel individual enable channel 0 - 15 (address 1002h) bit allocation*...continued*

Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CHEN7	CHEN6	CHEN5	CHEN4	CHEN3	CHEN2	CHEN1	CHEN0
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 191. BAL_CH_CFG0 register - balancing channel individual enable channel 0 - 15 (address 1002h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	CHEN15	R/W		Enable balancing for channel 15. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 15 is disabled. The balancing timer for Channel 15 is stopped.
			1	ENABLED (read-write) Balancing for Channel 15 is enabled.
14	CHEN14	R/W		Enable balancing for channel 14. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 14 is disabled. The balancing timer for Channel 14 is stopped.
			1	ENABLED (read-write) Balancing for Channel 15 is enabled.
13	CHEN13	R/W		Enable balancing for channel 13. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 13 is disabled. The balancing timer for Channel 13 is stopped.
			1	ENABLED (read-write) Balancing for Channel 13 is enabled.
12	CHEN12	R/W		Enable balancing for channel 12. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 12 is disabled. The balancing timer for Channel 12 is stopped.
			1	ENABLED (read-write) Balancing for Channel 12 is enabled.
11	CHEN11	R/W		Enable balancing for channel 11. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer

Table 191. BAL_CH_CFG0 register - balancing channel individual enable channel 0 - 15 (address 1002h) *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	DISABLED (read-write) Balancing for Channel 11 is disabled. The balancing timer for Channel 11 is stopped.
			1	ENABLED (read-write) Balancing for Channel 11 is enabled.
10	CHEN10	R/W		Enable balancing for channel 10. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 10 is disabled. The balancing timer for Channel 10 is stopped.
			1	ENABLED (read-write) Balancing for Channel 10 is enabled.
9	CHEN9	R/W		Enable balancing for channel 9. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 9 is disabled. The balancing timer for Channel 9 is stopped.
			1	ENABLED (read-write) Balancing for Channel 9 is enabled.
8	CHEN8	R/W		Enable balancing for channel 8. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 8 is disabled. The balancing timer for Channel 8 is stopped.
			1	ENABLED (read-write) Balancing for Channel 8 is enabled.
7	CHEN7	R/W		Enable balancing for channel 7. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 7 is disabled. The balancing timer for Channel 7 is stopped.
			1	ENABLED (read-write) Balancing for Channel 7 is enabled.
6	CHEN6	R/W		Enable balancing for channel 6. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 6 is disabled. The balancing timer for Channel 6 is stopped.
			1	ENABLED (read-write) Balancing for Channel 6 is enabled.
5	CHEN5	R/W		Enable balancing for channel 5. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer

Table 191. BAL_CH_CFG0 register - balancing channel individual enable channel 0 - 15 (address 1002h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	DISABLED (read-write) Balancing for Channel 5 is disabled. The balancing timer for Channel 5 is stopped.
			1	ENABLED (read-write) Balancing for Channel 5 is enabled.
4	CHEN4	R/W		Enable balancing for channel 4. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 4 is disabled. The balancing timer for Channel 4 is stopped.
			1	ENABLED (read-write) Balancing for Channel 4 is enabled.
3	CHEN3	R/W		Enable balancing for channel 3. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 3 is disabled. The balancing timer for Channel 3 is stopped.
			1	ENABLED (read-write) Balancing for Channel 3 is enabled.
2	CHEN2	R/W		Enable balancing for channel 2. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 2 is disabled. The balancing timer for Channel 2 is stopped.
			1	ENABLED (read-write) Balancing for Channel 2 is enabled.
1	CHEN1	R/W		Enable balancing for channel 1. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 1 is disabled. The balancing timer for Channel 1 is stopped.
			1	ENABLED (read-write) Balancing for Channel 1 is enabled.
0	CHEN0	R/W		Enable balancing for channel 0. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 0 is disabled. The balancing timer for Channel 0 is stopped.
			1	ENABLED (read-write) Balancing for Channel 0 is enabled.

12.1.72 BAL_CH_CFG1 register

Balancing channel individual enable channel 16 - 17

Table 192. BAL_CH_CFG1 register - balancing channel individual enable channel 16 - 17 (address 1003h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						CHEN17	CHEN16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 193. BAL_CH_CFG1 register - balancing channel individual enable channel 16 - 17 (address 1003h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	CHEN17	R/W		Enable balancing for channel 17. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 17 is disabled. The balancing timer for Channel 17 is stopped.
			1	ENABLED (read-write) Balancing for Channel 17 is enabled.
0	CHEN16	R/W		Enable balancing for channel 16. The bit is cleared by the device in case of • a detected over-current condition • a enabled and detected under-voltage condition • a timeout of the channel timer
			0*	DISABLED (read-write) Balancing for Channel 16 is disabled. The balancing timer for Channel 16 is stopped.
			1	ENABLED (read-write) Balancing for Channel 16 is enabled.

12.1.73 BAL_PRE_TMR register

Pre-balancing timer

Table 194. BAL_PRE_TMR register - pre-balancing timer (address 1004h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	PREBALTIME															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 195. BAL_PRE_TMR register - pre-balancing timer (address 1004h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:0	PREBALTIME	R/W		Downcounter which runs if BALEN is set. Inhibits the balancing and holds the individual channel timer. The value of this field represents the current counter value when read. The counting saturates at 0 and activates the balancing. The BAL_GLOB_TO_TMR is not influenced by this timer. **PREBALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Pre-balancing time is expired.
			0001h	PREBAL (read-write) Pre-balancing time is set to PREBAL * 10 seconds
			FFFFh	MAX (read-write) Maximum pre-balancing time = 655350 seconds = approximately 182 hours = approximately 7.6 days

12.1.74 BAL_AUTO_DISCHRG_CTRL register

Emergency discharge enable

Table 196. BAL_AUTO_DISCHRG_CTRL register - emergency discharge enable (address 1005h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	KEY															
Reset	0	0	1	0	0	0	0	1	0	1	0	1	0	0	1	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 197. BAL_AUTO_DISCHRG_CTRL register - emergency discharge enable (address 1005h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:0	KEY	R/W		Key for enabling auto discharge. After enabling with **DEADh** the discharge will continue until disable key **2152h** is received. **Other** values will be ignored.
			0001h	OTHERS (read-write) Other values will be ignored.
			2152h*	DISABLED (read-write) Disable key for auto discharge.
			DEADh	ENABLED (read-write) Enable key for auto discharge.

12.1.75 BAL_SWITCH_MON_CFG0 register

Balancing switch monitoring enable

Table 198. BAL_SWITCH_MON_CFG0 register - balancing switch monitoring enable (address 1006h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	MONEN15	MONEN14	MONEN13	MONEN12	MONEN11	MONEN10	MONEN9	MONEN8
Reset	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Table 198. BAL_SWITCH_MON_CFG0 register - balancing switch monitoring enable (address 1006h) bit allocation*...continued*

Symbol	MONEN7	MONEN6	MONEN5	MONEN4	MONEN3	MONEN2	MONEN1	MONEN0
Reset	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 199. BAL_SWITCH_MON_CFG0 register - balancing switch monitoring enable (address 1006h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	MONEN15	R/W		Enable balancing switch monitoring for channel 15.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 15 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 15 is enabled.
14	MONEN14	R/W		Enable balancing switch monitoring for channel 14.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 14 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 14 is enabled.
13	MONEN13	R/W		Enable balancing switch monitoring for channel 13.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 13 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 13 is enabled.
12	MONEN12	R/W		Enable balancing switch monitoring for channel 12.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 12 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 12 is enabled.
11	MONEN11	R/W		Enable balancing switch monitoring for channel 11.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 11 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 11 is enabled.
10	MONEN10	R/W		Enable balancing switch monitoring for channel 10.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 10 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 10 is enabled.
9	MONEN9	R/W		Enable balancing switch monitoring for channel 9.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 9 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 9 is enabled.
8	MONEN8	R/W		Enable balancing switch monitoring for channel 8.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 8 is disabled.

Table 199. BAL_SWITCH_MON_CFG0 register - balancing switch monitoring enable (address 1006h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 8 is enabled.
7	MONEN7	R/W		Enable balancing switch monitoring for channel 7.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 7 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 7 is enabled.
6	MONEN6	R/W		Enable balancing switch monitoring for channel 6.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 6 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 6 is enabled.
5	MONEN5	R/W		Enable balancing switch monitoring for channel 5.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 5 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 5 is enabled.
4	MONEN4	R/W		Enable balancing switch monitoring for channel 4.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 4 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 4 is enabled.
3	MONEN3	R/W		Enable balancing switch monitoring for channel 3.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 3 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 3 is enabled.
2	MONEN2	R/W		Enable balancing switch monitoring for channel 2.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 2 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 2 is enabled.
1	MONEN1	R/W		Enable balancing switch monitoring for channel 1.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 1 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 1 is enabled.
0	MONEN0	R/W		Enable balancing switch monitoring for channel 0.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 0 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 0 is enabled.

12.1.76 BAL_SWITCH_MON_CFG1 register

Balancing switch monitoring enable

Table 200. BAL_SWITCH_MON_CFG1 register - balancing switch monitoring enable (address 1007h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						MONEN17	MONEN16
Reset	0	0	0	0	0	0	1	1
Access	R	R	R	R	R	R	R/W	R/W

Table 201. BAL_SWITCH_MON_CFG1 register - balancing switch monitoring enable (address 1007h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	MONEN17	R/W		Enable balancing switch monitoring for channel 17.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 17 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 17 is enabled.
0	MONEN16	R/W		Enable balancing switch monitoring for channel 16.
			0	DISABLED (read-write) Balancing switch monitoring for Channel 16 is disabled.
			1*	ENABLED (read-write) Balancing switch monitoring for Channel 16 is enabled.

12.1.77 FULL_PWM_CYCLE_VOLTAGE register

Full PWM cycle voltage

Table 202. FULL_PWM_CYCLE_VOLTAGE register - full PWM cycle voltage (address 1008h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	FULLPWM															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 203. FULL_PWM_CYCLE_VOLTAGE register - full PWM cycle voltage (address 1008h)

Bit	Symbol	Access	Value	Description
15:0	FULLPWM	R/W	0h	FULL PWM cycle voltage setting to set the cell voltage on which the balancing is operating at the maximum current.(ie : min operating cell voltage in the application) Setting format is the same than cell voltage measurement.

12.1.78 BAL_CH_UV0_STAT0 register

Channel undervoltage balancing status channel 0 - 15

Table 204. BAL_CH_UV0_STAT0 register - channel undervoltage balancing status channel 0 - 15 (address 1009h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 205. BAL_CH_UV0_STAT0 register - channel under-voltage balancing status channel 0 - 15 (address 1009h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	CH15	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 15. Read clears bit.
			0*	NOUV (read) Balancing of channel 15 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 15 was disabled due to under-voltage condition.
14	CH14	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 14. Read clears bit.
			0*	NOUV (read) Balancing of channel 14 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 14 was disabled due to under-voltage condition.
13	CH13	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 13. Read clears bit.
			0*	NOUV (read) Balancing of channel 13 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 13 was disabled due to under-voltage condition.
12	CH12	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 12. Read clears bit.
			0*	NOUV (read) Balancing of channel 12 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 12 was disabled due to under-voltage condition.
11	CH11	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 11. Read clears bit.
			0*	NOUV (read) Balancing of channel 11 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 11 was disabled due to under-voltage condition.
10	CH10	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 10. Read clears bit.

Table 205. BAL_CH_UV0_STAT0 register - channel under-voltage balancing status channel 0 - 15 (address 1009h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	NOUV (read) Balancing of channel 10 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 10 was disabled due to under-voltage condition.
9	CH9	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 9. Read clears bit.
			0*	NOUV (read) Balancing of channel 9 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 9 was disabled due to under-voltage condition.
8	CH8	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 8. Read clears bit.
			0*	NOUV (read) Balancing of channel 8 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 8 was disabled due to under-voltage condition.
7	CH7	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 7. Read clears bit.
			0*	NOUV (read) Balancing of channel 7 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 7 was disabled due to under-voltage condition.
6	CH6	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 6. Read clears bit.
			0*	NOUV (read) Balancing of channel 6 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 6 was disabled due to under-voltage condition.
5	CH5	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 5. Read clears bit.
			0*	NOUV (read) Balancing of channel 5 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 5 was disabled due to under-voltage condition.
4	CH4	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 4. Read clears bit.
			0*	NOUV (read) Balancing of channel 4 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 4 was disabled due to under-voltage condition.
3	CH3	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 3. Read clears bit.
			0*	NOUV (read) Balancing of channel 3 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 3 was disabled due to under-voltage condition.

Table 205. BAL_CH_UV0_STAT0 register - channel under-voltage balancing status channel 0 - 15 (address 1009h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
2	CH2	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 2. Read clears bit.
			0*	NOUV (read) Balancing of channel 2 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 2 was disabled due to under-voltage condition.
1	CH1	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 1. Read clears bit.
			0*	NOUV (read) Balancing of channel 1 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 1 was disabled due to under-voltage condition.
0	CH0	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 0. Read clears bit.
			0*	NOUV (read) Balancing of channel 0 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 0 was disabled due to under-voltage condition.

12.1.79 BAL_CH_UV0_STAT1 register

Channel undervoltage balancing status channel 16 - 17

Table 206. BAL_CH_UV0_STAT1 register - channel undervoltage balancing status channel 16 - 17 (address 100Ah) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						CH17	CH16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 207. BAL_CH_UV0_STAT1 register - channel under-voltage balancing status channel 16 - 17 (address 100Ah)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	CH17	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 17. Read clears bit.
			0*	NOUV (read) Balancing of channel 17 was not disabled due to under-voltage condition.

Table 207. BAL_CH_UV0_STAT1 register - channel under-voltage balancing status channel 16 - 17 (address 100Ah)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			1	UV (read) Balancing of channel 17 was disabled due to under-voltage condition.
0	CH16	R		Status bit, if a channel under-voltage condition was the reason for disabling individual balancing of channel 16. Read clears bit.
			0*	NOUV (read) Balancing of channel 16 was not disabled due to under-voltage condition.
			1	UV (read) Balancing of channel 16 was disabled due to under-voltage condition.

12.1.80 BAL_GLOB_UV1_STAT0 register

Global undervoltage balancing status channel 0 - 15

Table 208. BAL_GLOB_UV1_STAT0 register - global undervoltage balancing status channel 0 - 15 (address 100Bh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 209. BAL_GLOB_UV1_STAT0 register - global under-voltage balancing status channel 0 - 15 (address 100Bh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	CH15	R		Status bit, if a global under-voltage of channel 15 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 15.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 15.
14	CH14	R		Status bit, if a global under-voltage of channel 14 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 14.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 14.
13	CH13	R		Status bit, if a global under-voltage of channel 13 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 13.

Table 209. BAL_GLOB_UV1_STAT0 register - global under-voltage balancing status channel 0 - 15 (address 100Bh)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 13.
12	CH12	R		Status bit, if a global under-voltage of channel 12 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 12.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 12.
11	CH11	R		Status bit, if a global under-voltage of channel 11 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 11.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 11.
10	CH10	R		Status bit, if a global under-voltage of channel 10 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 10.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 10.
9	CH9	R		Status bit, if a global under-voltage of channel 9 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 9.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 9.
8	CH8	R		Status bit, if a global under-voltage of channel 8 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 8.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 8.
7	CH7	R		Status bit, if a global under-voltage of channel 7 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 7.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 7.
6	CH6	R		Status bit, if a global under-voltage of channel 6 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 6.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 6.
5	CH5	R		Status bit, if a global under-voltage of channel 5 condition was the reason for disabling the global balancing. Read clears bit.

Table 209. BAL_GLOB_UV1_STAT0 register - global under-voltage balancing status channel 0 - 15 (address 100Bh)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 5.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 5.
4	CH4	R		Status bit, if a global under-voltage of channel 4 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 4.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 4.
3	CH3	R		Status bit, if a global under-voltage of channel 3 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 3.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 3.
2	CH2	R		Status bit, if a global under-voltage of channel 2 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 2.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 2.
1	CH1	R		Status bit, if a global under-voltage of channel 1 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 1.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 1.
0	CH0	R		Status bit, if a global under-voltage of channel 0 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 0.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 0.

12.1.81 BAL_GLOB_UV1_STAT1 register

Global undervoltage balancing status channel 16 - 17

Table 210. BAL_GLOB_UV1_STAT1 register - global undervoltage balancing status channel 16 - 17 (address 100Ch) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Table 210. BAL_GLOB_UV1_STAT1 register - global undervoltage balancing status channel 16 - 17 (address 100Ch) bit allocation*...continued*

Symbol	reserved						CH17	CH16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 211. BAL_GLOB_UV1_STAT1 register - global under-voltage balancing status channel 16 - 17 (address 100Ch)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	CH17	R		Status bit, if a global under-voltage of channel 17 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 17.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 17.
0	CH16	R		Status bit, if a global under-voltage of channel 16 condition was the reason for disabling the global balancing. Read clears bit.
			0*	NOUV (read) Balancing was not disabled due to global under-voltage condition of channel 16.
			1	UV (read) Balancing was disabled due to global under-voltage condition of channel 16.

12.1.82 BAL_STAT0 register

Logical balancing channel status channel 0 - 15

Table 212. BAL_STAT0 register - logical balancing channel status channel 0 - 15 (address 100Dh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 213. BAL_STAT0 register - logical balancing channel status channel 0 - 15 (address 100Dh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	CH15	R		Balancing channel 15 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 15 inactive.
			1	ACTIVE (read) Balancing for channel 15 active.

Table 213. BAL_STAT0 register - logical balancing channel status channel 0 - 15 (address 100Dh) *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
14	CH14	R		Balancing channel 14 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 14 inactive.
			1	ACTIVE (read) Balancing for channel 14 active.
13	CH13	R		Balancing channel 13 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 13 inactive.
			1	ACTIVE (read) Balancing for channel 13 active.
12	CH12	R		Balancing channel 12 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 12 inactive.
			1	ACTIVE (read) Balancing for channel 12 active.
11	CH11	R		Balancing channel 11 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 11 inactive.
			1	ACTIVE (read) Balancing for channel 11 active.
10	CH10	R		Balancing channel 10 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 10 inactive.
			1	ACTIVE (read) Balancing for channel 10 active.
9	CH9	R		Balancing channel 9 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 9 inactive.
			1	ACTIVE (read) Balancing for channel 9 active.
8	CH8	R		Balancing channel 8 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 8 inactive.
			1	ACTIVE (read) Balancing for channel 8 active.
7	CH7	R		Balancing channel 7 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 7 inactive.
			1	ACTIVE (read) Balancing for channel 7 active.
6	CH6	R		Balancing channel 6 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 6 inactive.
			1	ACTIVE (read) Balancing for channel 6 active.
5	CH5	R		Balancing channel 5 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 5 inactive.
			1	ACTIVE (read) Balancing for channel 5 active.
4	CH4	R		Balancing channel 4 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 4 inactive.

Table 213. BAL_STAT0 register - logical balancing channel status channel 0 - 15 (address 100Dh)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			1	ACTIVE (read) Balancing for channel 4 active.
3	CH3	R		Balancing channel 3 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 3 inactive.
			1	ACTIVE (read) Balancing for channel 3 active.
2	CH2	R		Balancing channel 2 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 2 inactive.
			1	ACTIVE (read) Balancing for channel 2 active.
1	CH1	R		Balancing channel 1 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 1 inactive.
			1	ACTIVE (read) Balancing for channel 1 active.
0	CH0	R		Balancing channel 0 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 0 inactive.
			1	ACTIVE (read) Balancing for channel 0 active.

12.1.83 BAL_STAT1 register

Logical balancing channel status channel 16 - 17

Table 214. BAL_STAT1 register - logical balancing channel status channel 16 - 17 (address 100Eh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						CH17	CH16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 215. BAL_STAT1 register - logical balancing channel status channel 16 - 17 (address 100Eh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	CH17	R		Balancing channel 17 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 17 inactive.
			1	ACTIVE (read) Balancing for channel 17 active.

Table 215. BAL_STAT1 register - logical balancing channel status channel 16 - 17 (address 100Eh)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
0	CH16	R		Balancing channel 16 status (without PWM and odd/even switching)
			0*	INACTIVE (read) Balancing for channel 16 inactive.
			1	ACTIVE (read) Balancing for channel 16 active.

12.1.84 BAL_STAT2 register

Balancing status

Table 216. BAL_STAT2 register - balancing status (address 100Fh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	BALRDY	BALPRO TFLG	reserved					
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved				BALPROT	AUTODI SCHRG	TEMPBA LINHIBIT	PREBALTMR
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 217. BAL_STAT2 register - balancing status (address 100Fh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	BALRDY	R		The ready bit is set after the cell balancing operation is finished. Reasons for this are that the last BAL_CH_EN.CHx has been cleared by hardware or the BAL_GLOB_CFG.BALEN has been cleared by hardware. With setting of BAL_GLOB_CFG.BALEN this bit is cleared. Read clears bit.
			0*	ONGOING (read) Balancing operation in progress.
			1	FINISHED (read) Balancing operation finished.
14	BALPROTFLG	R		Balancing protection flag. This bit is set when the BALPROT is ACTIVE. Read clears bit.
			0*	NOOCCURENCE (read) Balancing protection was not active.
			1	OCCURRED (read) Balancing protection was active.
13:4	reserved	R	0h	This read-only field is reserved and always has the value 0.
3	BALPROT	R		Balancing protection status
			0*	INACTIVE (read) Balancing protection allows balancing.
			1	ACTIVE (read) Balancing protection inhibits balancing.
2	AUTODISCHRG	R		Auto discharge status
			0*	INACTIVE (read) Auto discharge inactive
			1	ACTIVE (read) Auto discharge active

Table 217. BAL_STAT2 register - balancing status (address 100Fh)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
1	TEMPBALINHIBIT	R		Temperature balancing status
			0*	INACTIVE (read) Temperature based balancing control allows balancing.
			1	ACTIVE (read) Temperature based balancing control inhibits balancing.
0	PREBALTMR	R		Pre-Balancing status
			0*	INACTIVE (read) No pre-balancing timer active.
			1	ACTIVE (read) Pre-balancing timer active (Balancing is inhibited).

12.1.85 BAL_SWITCH_STAT0 register

Physical balancing channel status channel 0 - 15

Table 218. BAL_SWITCH_STAT0 register - physical balancing channel status channel 0 - 15 (address 1010h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 219. BAL_SWITCH_STAT0 register - physical balancing channel status channel 0 - 15 (address 1010h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	CH15	R		Balancing FET status channel 15 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
14	CH14	R		Balancing FET status channel 14 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
13	CH13	R		Balancing FET status channel 13 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.

Table 219. BAL_SWITCH_STAT0 register - physical balancing channel status channel 0 - 15 (address 1010h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
12	CH12	R		Balancing FET status channel 12 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
11	CH11	R		Balancing FET status channel 11 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
10	CH10	R		Balancing FET status channel 10 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
9	CH9	R		Balancing FET status channel 9 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
8	CH8	R		Balancing FET status channel 8 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
7	CH7	R		Balancing FET status channel 7 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
6	CH6	R		Balancing FET status channel 6 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
5	CH5	R		Balancing FET status channel 5 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
4	CH4	R		Balancing FET status channel 4 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.

Table 219. BAL_SWITCH_STAT0 register - physical balancing channel status channel 0 - 15 (address 1010h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
3	CH3	R		Balancing FET status channel 3 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
2	CH2	R		Balancing FET status channel 2 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
1	CH1	R		Balancing FET status channel 1 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
0	CH0	R		Balancing FET status channel 0 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.

12.1.86 BAL_SWITCH_STAT1 register

Physical balancing channel status channel 16 - 17

Table 220. BAL_SWITCH_STAT1 register - physical balancing channel status channel 16 - 17 (address 1011h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						CH17	CH16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 221. BAL_SWITCH_STAT1 register - physical balancing channel status channel 16 - 17 (address 1011h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	CH17	R		Balancing FET status channel 17 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.

Table 221. BAL_SWITCH_STAT1 register - physical balancing channel status channel 16 - 17 (address 1011h)*...continued***

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.
0	CH16	R		Balancing FET status channel 16 This is the actual status (including odd/even activation and PWM duty cycle) from the switch monitor circuit.
			0*	OPEN (read) Balancing FET is open.
			1	CLOSED (read) Balancing FET is closed.

12.1.87 BAL_SWITCH_FLT_STAT0 register

balancing switch fault channel 0 - 15

Table 222. BAL_SWITCH_FLT_STAT0 register - balancing switch fault channel 0 - 15 (address 1012h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	CH15	CH14	CH13	CH12	CH11	CH10	CH9	CH8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CH7	CH6	CH5	CH4	CH3	CH2	CH1	CH0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 223. BAL_SWITCH_FLT_STAT0 register - balancing switch fault channel 0 - 15 (address 1012h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	CH15	R		Balancing switch fault channel 15. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
14	CH14	R		Balancing switch fault channel 14. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
13	CH13	R		Balancing switch fault channel 13. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.

Table 223. BAL_SWITCH_FLT_STAT0 register - balancing switch fault channel 0 - 15 (address 1012h) *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
12	CH12	R		Balancing switch fault channel 12. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
11	CH11	R		Balancing switch fault channel 11. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
10	CH10	R		Balancing switch fault channel 10. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
9	CH9	R		Balancing switch fault channel 9. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
8	CH8	R		Balancing switch fault channel 8. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
7	CH7	R		Balancing switch fault channel 7. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
6	CH6	R		Balancing switch fault channel 6. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
5	CH5	R		Balancing switch fault channel 5. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
4	CH4	R		Balancing switch fault channel 4. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.

Table 223. BAL_SWITCH_FLT_STAT0 register - balancing switch fault channel 0 - 15 (address 1012h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			1	FAULT (read) Wrong switch state has been detected.
3	CH3	R		Balancing switch fault channel 3. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
2	CH2	R		Balancing switch fault channel 2. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
1	CH1	R		Balancing switch fault channel 1. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
0	CH0	R		Balancing switch fault channel 0. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.

12.1.88 BAL_SWITCH_FLT_STAT1 register

balancing switch fault channel 16 - 17

Table 224. BAL_SWITCH_FLT_STAT1 register - balancing switch fault channel 16 - 17 (address 1013h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						CH17	CH16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 225. BAL_SWITCH_FLT_STAT1 register - balancing switch fault channel 16 - 17 (address 1013h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	CH17	R		Balancing switch fault channel 17. Physical state of the Balancing circuit has differed from the expected one. This could

Table 225. BAL_SWITCH_FLT_STAT1 register - balancing switch fault channel 16 - 17 (address 1013h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
				be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.
0	CH16	R		Balancing switch fault channel 16. Physical state of the Balancing circuit has differed from the expected one. This could be due to a broken switch, leakages or over current. Read clears bit.
			0*	NOFLT (read) No fault detected.
			1	FAULT (read) Wrong switch state has been detected.

12.1.89 BAL_TMR_CH_ALL register

virtual register, writes in parallel into BAL_TMR_CH0 up to BAL_TMR_CH17

Table 226. BAL_TMR_CH_ALL register - Virtual register, writes all BAL_TMR registers (address 101Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Table 227. BAL_TMR_CH_ALL register - Virtual register, writes all BAL_TMR registers (address 101Fh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	W	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	W		Sets the balancing time for all channels. **BALTIME** * 10 seconds
			0000h*	EXPIRED (write) Balancing time is set to 0.
			0001h	BALTIME (write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.90 BAL_TMR_CH0 register

balancing timer channel 0

Table 228. BAL_TMR_CH0 register - balancing timer channel 0 (address 1020h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 229. BAL_TMR_CH0 register - balancing timer channel 0 (address 1020h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 0. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.91 BAL_TMR_CH1 register

balancing timer channel 1

Table 230. BAL_TMR_CH1 register - balancing timer channel 1 (address 1021h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 231. BAL_TMR_CH1 register - balancing timer channel 1 (address 1021h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 1. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.92 BAL_TMR_CH2 register

balancing timer channel 2

Table 232. BAL_TMR_CH2 register - balancing timer channel 2 (address 1022h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													

Table 232. BAL_TMR_CH2 register - balancing timer channel 2 (address 1022h) bit allocation*...continued*

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 233. BAL_TMR_CH2 register - balancing timer channel 2 (address 1022h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 2. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.93 BAL_TMR_CH3 register

balancing timer channel 3

Table 234. BAL_TMR_CH3 register - balancing timer channel 3 (address 1023h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 235. BAL_TMR_CH3 register - balancing timer channel 3 (address 1023h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 3. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.94 BAL_TMR_CH4 register

balancing timer channel 4

Table 236. BAL_TMR_CH4 register - balancing timer channel 4 (address 1024h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 237. BAL_TMR_CH4 register - balancing timer channel 4 (address 1024h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 4. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.95 BAL_TMR_CH5 register

balancing timer channel 5

Table 238. BAL_TMR_CH5 register - balancing timer channel 5 (address 1025h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 239. BAL_TMR_CH5 register - balancing timer channel 5 (address 1025h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 5. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.

Table 239. BAL_TMR_CH5 register - balancing timer channel 5 (address 1025h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.96 BAL_TMR_CH6 register

balancing timer channel 6

Table 240. BAL_TMR_CH6 register - balancing timer channel 6 (address 1026h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 241. BAL_TMR_CH6 register - balancing timer channel 6 (address 1026h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 6. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.97 BAL_TMR_CH7 register

balancing timer channel 7

Table 242. BAL_TMR_CH7 register - balancing timer channel 7 (address 1027h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 243. BAL_TMR_CH7 register - balancing timer channel 7 (address 1027h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 7. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.98 BAL_TMR_CH8 register

balancing timer channel 8

Table 244. BAL_TMR_CH8 register - balancing timer channel 8 (address 1028h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 245. BAL_TMR_CH8 register - balancing timer channel 8 (address 1028h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 8. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.99 BAL_TMR_CH9 register

balancing timer channel 9

Table 246. BAL_TMR_CH9 register - balancing timer channel 9 (address 1029h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													

Table 246. BAL_TMR_CH9 register - balancing timer channel 9 (address 1029h) bit allocation*...continued*

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 247. BAL_TMR_CH9 register - balancing timer channel 9 (address 1029h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 9. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.100 BAL_TMR_CH10 register

balancing timer channel 10

Table 248. BAL_TMR_CH10 register - balancing timer channel 10 (address 102Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 249. BAL_TMR_CH10 register - balancing timer channel 10 (address 102Ah)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 10. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.101 BAL_TMR_CH11 register

balancing timer channel 11

Table 250. BAL_TMR_CH11 register - balancing timer channel 11 (address 102Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 251. BAL_TMR_CH11 register - balancing timer channel 11 (address 102Bh)
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 11. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.102 BAL_TMR_CH12 register

balancing timer channel 12

Table 252. BAL_TMR_CH12 register - balancing timer channel 12 (address 102Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 253. BAL_TMR_CH12 register - balancing timer channel 12 (address 102Ch)
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 12. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.

Table 253. BAL_TMR_CH12 register - balancing timer channel 12 (address 102Ch)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.103 BAL_TMR_CH13 register

balancing timer channel 13

Table 254. BAL_TMR_CH13 register - balancing timer channel 13 (address 102Dh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 255. BAL_TMR_CH13 register - balancing timer channel 13 (address 102Dh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 13. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.104 BAL_TMR_CH14 register

balancing timer channel 14

Table 256. BAL_TMR_CH14 register - balancing timer channel 14 (address 102Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 257. BAL_TMR_CH14 register - balancing timer channel 14 (address 102Eh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 14. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.105 BAL_TMR_CH15 register

balancing timer channel 15

Table 258. BAL_TMR_CH15 register - balancing timer channel 15 (address 102Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 259. BAL_TMR_CH15 register - balancing timer channel 15 (address 102Fh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 15. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	PWM0 (read-write) Balancing time is set to 0.
			0001h	PWM1 (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.106 BAL_TMR_CH16 register

balancing timer channel 16

Table 260. BAL_TMR_CH16 register - balancing timer channel 16 (address 1030h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													

Table 260. BAL_TMR_CH16 register - balancing timer channel 16 (address 1030h) bit allocation*...continued*

Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 261. BAL_TMR_CH16 register - balancing timer channel 16 (address 1030h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 16. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.107 BAL_TMR_CH17 register

balancing timer channel 17

Table 262. BAL_TMR_CH17 register - balancing timer channel 17 (address 1031h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved		BALTIME													
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 263. BAL_TMR_CH17 register - balancing timer channel 17 (address 1031h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	reserved	R	0h	This read-only field is reserved and always has the value 0.
13:0	BALTIME	R/W		Balancing time for channel 17. The value of this field represents the current counter value when read. The counting saturates at 0. If the value is zero, the balancing for this channel is stopped. The counting is only active if balancing is enabled, timer based balancing is enabled and the channel enable is set. **BALTIME** * 10 seconds
			0000h*	EXPIRED (read-write) Balancing time is set to 0.
			0001h	BALTIME (read-write) Balancing time is set to BALTIME * 10 seconds
			3FFFh	MAX (read-write) Sets maximum balancing time of 163830 seconds = approximately 45.5 hours.

12.1.108 BAL_PWM_CH_ALL register

virtual register, writes in parallel into BAL_PWM_CH0 up to BAL_PWM_CH17

Table 264. BAL_PWM_CH_ALL register - Virtual register, writes all BAL_PWM registers (address 1032h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Table 265. BAL_PWM_CH_ALL register - Virtual register, writes all BAL_PWM registers (address 1032h)
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	W	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	W		Sets the balancing PWM for all channels. **PWM** * 100/255%
			00h	DISABLED (write) PWM duty cycle set to 0.
			80h	PWM50 (write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (write) PWM duty cycle set to 100%.

12.1.109 BAL_PWM_CH0 register

Balancing PWM channel 0

Table 266. BAL_PWM_CH0 register - balancing PWM channel 0 (address 1033h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 267. BAL_PWM_CH0 register - balancing PWM channel 0 (address 1033h)
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 0. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.110 BAL_PWM_CH1 register

Balancing PWM channel 1

Table 268. BAL_PWM_CH1 register - balancing PWM channel 1 (address 1034h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 269. BAL_PWM_CH1 register - balancing PWM channel 1 (address 1034h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 1. **PWM** * 100/255%
			00h	DISABLED (read-write) .
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.111 BAL_PWM_CH2 register

Balancing PWM channel 2

Table 270. BAL_PWM_CH2 register - balancing PWM channel 2 (address 1035h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 271. BAL_PWM_CH2 register - balancing PWM channel 2 (address 1035h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 2. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.112 BAL_PWM_CH3 register

Balancing PWM channel 3

Table 272. BAL_PWM_CH3 register - balancing PWM channel 3 (address 1036h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							

Table 272. BAL_PWM_CH3 register - balancing PWM channel 3 (address 1036h) bit allocation*...continued*

Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 273. BAL_PWM_CH3 register - balancing PWM channel 3 (address 1036h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 3. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.113 BAL_PWM_CH4 register

balancing PWM channel 4

Table 274. BAL_PWM_CH4 register - balancing PWM channel 4 (address 1037h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 275. BAL_PWM_CH4 register - balancing PWM channel 4 (address 1037h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 4. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.114 BAL_PWM_CH5 register

Balancing PWM channel 5

Table 276. BAL_PWM_CH5 register - balancing PWM channel 5 (address 1038h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 277. BAL_PWM_CH5 register - balancing PWM channel 5 (address 1038h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 5. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.115 BAL_PWM_CH6 register

Balancing PWM channel 6

Table 278. BAL_PWM_CH6 register - balancing PWM channel 6 (address 1039h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 279. BAL_PWM_CH6 register - balancing PWM channel 6 (address 1039h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 6. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.116 BAL_PWM_CH7 register

Balancing PWM channel 7

Table 280. BAL_PWM_CH7 register - balancing PWM channel 7 (address 103Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 281. BAL_PWM_CH7 register - balancing PWM channel 7 (address 103Ah)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 7. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.117 BAL_PWM_CH8 register

Balancing PWM channel 8

Table 282. BAL_PWM_CH8 register - balancing PWM channel 8 (address 103Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 283. BAL_PWM_CH8 register - balancing PWM channel 8 (address 103Bh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 8. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.118 BAL_PWM_CH9 register

Balancing PWM channel 9

Table 284. BAL_PWM_CH9 register - balancing PWM channel 9 (address 103Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 285. BAL_PWM_CH9 register - balancing PWM channel 9 (address 103Ch)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 9. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.119 BAL_PWM_CH10 register

Balancing PWM channel 10

Table 286. BAL_PWM_CH10 register - balancing PWM channel 10 (address 103Dh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 287. BAL_PWM_CH10 register - balancing PWM channel 10 (address 103Dh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 10. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.120 BAL_PWM_CH11 register

Balancing PWM channel 11

Table 288. BAL_PWM_CH11 register - balancing PWM channel 11 (address 103Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 289. BAL_PWM_CH11 register - balancing PWM channel 11 (address 103Eh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 11. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.121 BAL_PWM_CH12 register

Balancing PWM channel 12

Table 290. BAL_PWM_CH12 register - balancing PWM channel 12 (address 103Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 291. BAL_PWM_CH12 register - balancing PWM channel 12 (address 103Fh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 12 **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.122 BAL_PWM_CH13 register

Balancing PWM channel 13

Table 292. BAL_PWM_CH13 register - balancing PWM channel 13 (address 1040h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 293. BAL_PWM_CH13 register - balancing PWM channel 13 (address 1040h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 13. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.123 BAL_PWM_CH14 register

Balancing PWM channel 14

Table 294. BAL_PWM_CH14 register - balancing PWM channel 14 (address 1041h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 295. BAL_PWM_CH14 register - balancing PWM channel 14 (address 1041h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 14. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.124 BAL_PWM_CH15 register

Balancing PWM channel 15

Table 296. BAL_PWM_CH15 register - balancing PWM channel 15 (address 1042h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 297. BAL_PWM_CH15 register - balancing PWM channel 15 (address 1042h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 15. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.125 BAL_PWM_CH16 register

Balancing PWM channel 16

Table 298. BAL_PWM_CH16 register - balancing PWM channel 16 (address 1043h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 299. BAL_PWM_CH16 register - balancing PWM channel 16 (address 1043h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 16. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.126 BAL_PWM_CH17 register

Balancing PWM channel 17

Table 300. BAL_PWM_CH17 register - balancing PWM channel 17 (address 1044h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	reserved								PWM							
Reset	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Access	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 301. BAL_PWM_CH17 register - balancing PWM channel 17 (address 1044h)
*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:8	reserved	R	0h	This read-only field is reserved and always has the value 0.
7:0	PWM	R/W		Balancing PWM for channel 17. **PWM** * 100/255%
			00h	DISABLED (read-write) PWM duty cycle set to 0.
			80h	PWM50 (read-write) PWM duty cycle set to 128/255 *100 %= 50%.
			FFh*	MAX (read-write) PWM duty cycle set to 100%.

12.1.127 ALLM_CFG register

General measurement control

Table 302. ALLM_CFG register - general measurement control (address 1400h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	BALPAUSELEN							
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BALPAUSELEN						BALPAUSECYCMODEN	MEASEN
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 303. ALLM_CFG register - general measurement control (address 1400h)

Bit	Symbol	Access	Value	Description
15:2	BALPAUSELEN	W	0h	Writes BALPAUSELEN for primary and secondary measurement.
1	BALPAUSECYCMODEN	W	0h	Writes BALPAUSECYCMODEN for primary and secondary measurement.
0	MEASEN	W	0h	Writes MEASEN for primary and secondary measurement.

12.1.128 ALLM_APP_CTRL register

Application measurement control

Table 304. ALLM_APP_CTRL register - application measurement control (address 1401h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PAUSEBAL	VCOLNUM					CAPAIN7	CAPAIN6
Reset	0	1	1	1	1	1	0	0
Access	W	W	W	W	W	W	W	W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CAPAIN5	CAPAIN4	CAPAIN3	CAPAIN2	CAPAIN1	CAPAIN0	CAPAINA	CAPVC
Reset	0	0	0	0	0	0	0	0

Table 304. ALLM_APP_CTRL register - application measurement control (address 1401h) bit allocation*...continued*

Access	W	W	W	W	W	W	W	W

Table 305. ALLM_APP_CTRL register - application measurement control (address 1401h)

Bit	Symbol	Access	Value	Description
15	PAUSEBAL	W	0h	Writes PAUSEBAL for primary and secondary measurement.
14:10	VCOLNUM	W	1Fh	Writes VCOLNUM for primary measurement, if CAPVC is set. No influence on secondary measurement.
9	CAPAIN7	W	0h	No influence on primary measurement as long as it is used without the PAUSEBAL bit. Writes CAPAIN7 for secondary measurement.
8	CAPAIN6	W	0h	No influence on primary measurement as long as it is used without the PAUSEBAL bit. Writes CAPAIN6 for secondary measurement.
7	CAPAIN5	W	0h	No influence on primary measurement as long as it is used without the PAUSEBAL bit. Writes CAPAIN5 for secondary measurement.
6	CAPAIN4	W	0h	No influence on primary measurement as long as it is used without the PAUSEBAL bit. Writes CAPAIN4 for secondary measurement.
5	CAPAIN3	W	0h	Writes CAPAIN3 for primary measurement. No influence on secondary measurement as long as it is used without the PAU SEBAL bit.
4	CAPAIN2	W	0h	Writes CAPAIN2 for primary measurement. No influence on secondary measurement as long as it is used without the PAU SEBAL bit.
3	CAPAIN1	W	0h	Writes CAPAIN1 for primary measurement. No influence on secondary measurement as long as it is used without the PAU SEBAL bit.
2	CAPAIN0	W	0h	Writes CAPAIN0 for primary measurement. No influence on secondary measurement as long as it is used without the PAU SEBAL bit.
1	CAPAINA	W	0h	Writes CAPAINA for primary measurement. No influence on secondary measurement as long as it is used without the PAU SEBAL bit.
0	CAPVC	W	0h	Writes CAPVC for primary measurement. No influence on secondary measurement as long as it is used without the PAU SEBAL bit.

12.1.129 ALLM_PER_CTRL register

periodic measurement control

Table 306. ALLM_PER_CTRL register - periodic measurement control (address 1402h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved			PERCTRL	reserved			PERLEN
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	PERLEN							
Reset	0	0	0	1	0	0	0	0

Table 306. ALLM_PER_CTRL register - periodic measurement control (address 1402h) bit allocation*...continued*

Access	W	W	W	W	W	W	W	W

Table 307. ALLM_PER_CTRL register - periodic measurement control (address 1402h)

Bit	Symbol	Access	Value	Description
15:13	reserved	W	0h	This read-only field is reserved and always has the value 0.
12	PERCTRL	W	0h	Writes PERCTRL for primary and secondary measurement.
11:9	reserved	W	0h	This read-only field is reserved and always has the value 0.
8:0	PERLEN	W	10h	Writes PERLEN for primary and secondary measurement.

12.1.130 ALLM_SYNC_CTRL register

Synchronous measurement control

Table 308. ALLM_SYNC_CTRL register - synchronous measurement control (address 1403h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PAUSEBAL	VBOLNUM					reserved	
Reset	0	1	1	1	1	1	0	0
Access	W	W	W	W	W	W	W	W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						FASTVB	SYNCCYC
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 309. ALLM_SYNC_CTRL register - synchronous measurement control (address 1403h)

Bit	Symbol	Access	Value	Description
15	PAUSEBAL	W	0h	Writes PAUSEBAL for primary and secondary measurement.
14:10	VBOLNUM	W	1Fh	No influence on primary measurement. Writes VBOLNUM for secondary measurement.
9:2	reserved	W	0h	This read-only field is reserved and always has the value 0.
1	FASTVB	W	0h	Dummy fast measurement cycle on primary measurement. Writes FASTVB for secondary measurement.
0	SYNCCYC	W	0h	Writes SYNCCYC for primary and secondary measurement.

12.1.131 ALLM_VCVB_CFG0 register

Cell voltage measurement enable

Table 310. ALLM_VCVB_CFG0 register - cell voltage measurement enable (address 1408h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	VCVB15EN	VCVB14EN	VCVB13EN	VCVB12EN	VCVB11EN	VCVB10EN	VCVB9EN	VCVB8EN
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Table 310. ALLM_VCVB_CFG0 register - cell voltage measurement enable (address 1408h) bit allocation...*continued*

Symbol	VCVB7EN	VCVB6EN	VCVB5EN	VCVB4EN	VCVB3EN	VCVB2EN	VCVB1EN	VCVB0EN
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 311. ALLM_VCVB_CFG0 register - cell voltage measurement enable (address 1408h)

Bit	Symbol	Access	Value	Description
15	VCVB15EN	W	0h	Writes VC15EN for primary and VB15EN secondary measurement.
14	VCVB14EN	W	0h	Writes VC14EN for primary and VB14EN secondary measurement.
13	VCVB13EN	W	0h	Writes VC13EN for primary and VB13EN secondary measurement.
12	VCVB12EN	W	0h	Writes VC12EN for primary and VB12EN secondary measurement.
11	VCVB11EN	W	0h	Writes VC11EN for primary and VB11EN secondary measurement.
10	VCVB10EN	W	0h	Writes VC10EN for primary and VB10EN secondary measurement.
9	VCVB9EN	W	0h	Writes VC9EN for primary and VB9EN secondary measurement.
8	VCVB8EN	W	0h	Writes VC8EN for primary and VB8EN secondary measurement.
7	VCVB7EN	W	0h	Writes VC7EN for primary and VB7EN secondary measurement.
6	VCVB6EN	W	0h	Writes VC6EN for primary and VB6EN secondary measurement.
5	VCVB5EN	W	0h	Writes VC5EN for primary and VB5EN secondary measurement.
4	VCVB4EN	W	0h	Writes VC4EN for primary and VB4EN secondary measurement.
3	VCVB3EN	W	0h	Writes VC3EN for primary and VB3EN secondary measurement.
2	VCVB2EN	W	0h	Writes VC2EN for primary and VB2EN secondary measurement.
1	VCVB1EN	W	0h	Writes VC1EN for primary and VB1EN secondary measurement.
0	VCVB0EN	W	0h	Writes VC0EN for primary and VB0EN secondary measurement.

12.1.132 ALLM_VCVB_CFG1 register

Cell voltage measurement enable

Table 312. ALLM_VCVB_CFG1 register - cell voltage measurement enable (address 1409h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						VCVB17EN	VCVB16EN
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 313. ALLM_VCVB_CFG1 register - cell voltage measurement enable (address 1409h)

Bit	Symbol	Access	Value	Description
15:2	reserved	W	0h	this read-only field is reserved and always has the value 0
1	VCVB17EN	W	0h	writes VC17EN for primary and VB17EN secondary measurement
0	VCVB16EN	W	0h	writes VC16EN for primary and VB16EN secondary measurement

12.1.133 PRMM_CFG register

General measurement control

Table 314. PRMM_CFG register - general measurement control (address 1800h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	BALPAUSELEN							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BALPAUSELEN						BALPAUSECYCMODEN	MEASEN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 315. PRMM_CFG register - general measurement control (address 1800h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	BALPAUSELEN	R/W		Pause time of balancing before measurement cycle is executed. An on-going balancing pause operation is not influenced by a change of this value. **BALPAUSELEN** * 10 µs
			0000h*	NO_PAUSE (read-write) No Pause.
			0001h	PAUSE_10u (read-write) Pause = 10 us
			3FFFh	MAX (read-write) Maximum pause = 163830 us = 163 ms
1	BALPAUSECYCMODEN	R/W		Enable balancing auto pause. This delays the start of measurements after entering Cyclic mode until the auto pause counter has elapsed.
			0*	DISABLED (read-write) Auto pause for balancing is disabled.
			1	ENABLED (read-write) Auto pause for balancing is enabled. Measurements are started when the auto pause counter is elapsed.
0	MEASEN	R/W		Enable the data acquisition. Setting this bit to zero initiates a result clear and invalidate action (this includes resetting all ready bits). This bit is cleared when entering Sleep mode. Cyclic measurements are always executed, regardless of the value of this bit. Balancing is not stopped automatically (if in Active mode), as it would be permanently inhibited while measurement is active. If balancing shall be paused, please do so via the balancing control.

Table 315. PRMM_CFG register - general measurement control (address 1800h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	DISABLED (read-write) Data acquisition disabled
			1	ENABLED (read-write) Data acquisition enabled

12.1.134 PRMM_APP_CTRL register

Application measurement control

Table 316. PRMM_APP_CTRL register - application measurement control (address 1801h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PAUSEBAL	VCOLNUM					CAPAIN7	CAPAIN6
Reset	0	1	1	1	1	1	0	0
Access	W	R/W	R/W	R/W	R/W	R/W	W	W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CAPAIN5	CAPAIN4	CAPAIN3	CAPAIN2	CAPAIN1	CAPAIN0	CAPAINA	CAPVC
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 317. PRMM_APP_CTRL register - application measurement control (address 1801h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	PAUSEBAL	W		Pause the balancing during this capture cycle. If balancing was not paused before, the start of data capture is delayed until the auto pause timer has elapsed. If no CAPxxx is set this bit is ignored.
			0*	NO_PAUSE (write) Continue with balancing.
			1	PAUSE (write) Pause the balancing during this capture cycle.
14:10	VCOLNUM	R/W		VC number for which the open-load detection is enabled. **0 to 17** channel for which the open-load detection is enabled. **18 to 30** reserved (no open-load detection mechanism is enabled). Writing this bitfield is only possible if CAPVC is set as well.
			1Fh*	DISABLED (read-write) Open-load detection is disabled
9	CAPAIN7	W		AIN7 is not part of the primary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
8	CAPAIN6	W		AIN6 is not part of the primary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.

Table 317. PRMM_APP_CTRL register - application measurement control (address 1801h) *...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
7	CAPAIN5	W		AIN5 is not part of the primary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
6	CAPAIN4	W		AIN4 is not part of the primary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
5	CAPAIN3	W		Capture command for AIN3. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
4	CAPAIN2	W		Capture command for AIN2. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
3	CAPAIN1	W		Capture command for AIN1. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
2	CAPAIN0	W		Capture command for AIN0. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
1	CAPAINA	W		Capture command for AINA. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
0	CAPVC	W		Capture the application measurement values of the cell terminal measurements. The values are now readable via the app_result register. This bit is only available in the primary measurement chain.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.

12.1.135 PRMM_PER_CTRL register

Periodic measurement control

Table 318. PRMM_PER_CTRL register - periodic measurement control (address 1802h) bit allocation

Bit	15	14	13	12	11	10	9	8

Table 318. PRMM_PER_CTRL register - periodic measurement control (address 1802h) bit allocation *...continued*

Symbol	reserved			PERCTRL	reserved			PERLEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R	R	R	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	PERLEN							
Reset	0	0	0	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 319. PRMM_PER_CTRL register - periodic measurement control (address 1802h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:13	reserved	R	0h	This read-only field is reserved and always has the value 0.
12	PERCTRL	R/W		Control the periodic result behavior.
			0*	AUTO (read-write) Periodic results are automatically updated
			1	ONCE (read-write) Periodic results are updated once with the last results. (each write updates the results).
11:9	reserved	R	0h	This read-only field is reserved and always has the value 0.
8:0	PERLEN	R/W		Number of measurements for one periodic measurement. The minimum is 16. Writing a value lower than 16 leads to a 16 in the register.
			010h*	PER_16 (read-write) minimum value = 16 measurements per period
			011h	PER_17 (read-write) 17 measurements per period
			1FFh	PER_MAX (read-write) maximum value = 511 measurements per period

12.1.136 PRMM_SYNC_CTRL register

Synchronous measurement control

Table 320. PRMM_SYNC_CTRL register - synchronous measurement control (address 1803h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PAUSEBAL	reserved						
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						FASTCYC	SYNCCYC
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 321. PRMM_SYNC_CTRL register - synchronous measurement control (address 1803h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	PAUSEBAL	W		Pause the balancing during this capture cycle. If balancing was not paused before, the start of data capture is delayed until the auto pause timer has elapsed. If no capture cycle is started this bit is ignored.
			0*	NO_PAUSE (write) Continue with balancing.
			1	PAUSE (write) Pause the balancing during this capture cycle.
14:2	reserved	W	0h	This read-only field is reserved and always has the value 0.
1	FASTCYC	W		Start of a dummy Fast measurement cycle. In this cycle nothing is actually measured and stored. The bit is only implemented to keep the balancing auto pause synchronous between primary and secondary measurement. If set together with SYNCCYC or during an active synchronous measurement cycle, this bit is ignored. Read as zero.
			0*	NO_FAST (write) No new start of a dummy fast measurement cycle.
			0*	STATUS (read) Read as zero.
			1	FAST (write) Start a new dummy fast measurement cycle.
0	SYNCCYC	W		Start a synchronous measurement cycle. In this cycle the CT and CB voltages are measured and stored as matching pairs. If no VC channel is enabled or if set during a running synchronous measurement cycle the set is ignored. Read as zero.
			0*	NO_START (write) No new start a synchronous measurement cycle.
			0*	STATUS (read) Read a zero
			1	START (write) Start a synchronous measurement cycle.

12.1.137 PRMM_VC_CFG0 register

Cell voltage measurement enable

Table 322. PRMM_VC_CFG0 register - cell voltage measurement enable (address 1808h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	VC15EN	VC14EN	VC13EN	VC12EN	VC11EN	VC10EN	VC9EN	VC8EN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	VC7EN	VC6EN	VC5EN	VC4EN	VC3EN	VC2EN	VC1EN	VC0EN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 323. PRMM_VC_CFG0 register - cell voltage measurement enable (address 1808h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	VC15EN	R/W		Enable measurement of cell voltage 15. Changes to this bit during active measurement can lead to undefined results.

Table 323. PRMM_VC_CFG0 register - cell voltage measurement enable (address 1808h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
14	VC14EN	R/W		Enable measurement of cell voltage 14. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
13	VC13EN	R/W		Enable measurement of cell voltage 13. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
12	VC12EN	R/W		Enable measurement of cell voltage 12. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
11	VC11EN	R/W		Enable measurement of cell voltage 11. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
10	VC10EN	R/W		Enable measurement of cell voltage 10. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
9	VC9EN	R/W		Enable measurement of cell voltage 9. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
8	VC8EN	R/W		Enable measurement of cell voltage 8. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
7	VC7EN	R/W		Enable measurement of cell voltage 7. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
6	VC6EN	R/W		Enable measurement of cell voltage 6. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
5	VC5EN	R/W		Enable measurement of cell voltage 5. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled

Table 323. PRMM_VC_CFG0 register - cell voltage measurement enable (address 1808h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
4	VC4EN	R/W		Enable measurement of cell voltage 4. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
3	VC3EN	R/W		Enable measurement of cell voltage 3. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
2	VC2EN	R/W		Enable measurement of cell voltage 2. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
1	VC1EN	R/W		Enable measurement of cell voltage 1. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
0	VC0EN	R/W		Enable measurement of cell voltage 0. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled

12.1.138 PRMM_VC_CFG1 register

Cell voltage measurement enable

Table 324. PRMM_VC_CFG1 register - cell voltage measurement enable (address 1809h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						VC17EN	VC16EN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 325. PRMM_VC_CFG1 register - cell voltage measurement enable (address 1809h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VC17EN	R/W		Enable measurement of cell voltage 17. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled

Table 325. PRMM_VC_CFG1 register - cell voltage measurement enable (address 1809h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			1	ENABLED (read-write) Measurement enabled
0	VC16EN	R/W		Enable measurement of cell voltage 16. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled

12.1.139 PRMM_AIN_CFG register

AINx measurement enables

Table 326. PRMM_AIN_CFG register - AINx measurement enables (address 180Ah) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	RATIOMETRICAIN3		RATIOMETRICAIN2		RATIOMETRICAIN1		RATIOMETRICAIN0	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved		FLTAPPINV	AINAEN	AIN3EN	AIN2EN	AIN1EN	AIN0EN
Reset	0	0	1	0	0	0	0	0
Access	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Table 327. PRMM_AIN_CFG register - AINx measurement enables (address 180Ah)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	RATIOMETRICAIN3	R/W		Reference selection for AIN3. Changes to these bits during active measurement can lead to undefined results.
			00*	PRMVREF (read-write) Absolute (PRMVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
13:12	RATIOMETRICAIN2	R/W		Reference selection for AIN2. Changes to these bits during active measurement can lead to undefined results.
			00*	PRMVREF (read-write) Absolute (PRMVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
11:10	RATIOMETRICAIN1	R/W		Reference selection for AIN1. Changes to these bits during active measurement can lead to undefined results.
			00*	PRMVREF (read-write) Absolute (PRMVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)

Table 327. PRMM_AIN_CFG register - AINx measurement enables (address 180Ah)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
9:8	RATIOMETRICAIN0	R/W		Reference selection for AIN0. Changes to these bits during active measurement can lead to undefined results.
			00*	PRMVREF (read-write) Absolute (PRMVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
7:6	reserved	R	0h	This read-only field is reserved and always has the value 0.
5	FLTAPPINV	R/W		Invalidate AINx application results in case of fault.
			0	VALID (read-write) AINx application results are not invalidated in case of a fault
			1*	INVALID (read-write) AINx application results are invalidated when a fault is detected.
4	AINAEN	R/W		Enable measurement of AINA. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
3	AIN3EN	R/W		Enable measurement of AIN3. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.
2	AIN2EN	R/W		Enable measurement of AIN2. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.
1	AIN1EN	R/W		Enable measurement of AIN1. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.
0	AIN0EN	R/W		Enable measurement of AIN0. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.

12.1.140 PRMM_AIN_OL_CFG register

AINx open-load detection enable

Table 328. PRMM_AIN_OL_CFG register - AINx open-load detection enable (address 180Bh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved			AINAEN	AIN3EN	AIN2EN	AIN1EN	AIN0EN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R/W	R/W	R/W	R/W

Table 329. PRMM_AIN_OL_CFG register - AINx open-load detection enable (address 180Bh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:5	reserved	R	0h	This read-only field is reserved and always has the value 0.
4	AINAEN	R/W		Open-load detection circuit for AINA
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.
3	AIN3EN	R/W		Open-load detection circuit for AIN3
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.
2	AIN2EN	R/W		Open-load detection circuit for AIN2
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.
1	AIN1EN	R/W		Open-load detection circuit for AIN1
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.
0	AIN0EN	R/W		Open-load detection circuit for AIN0
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.

12.1.141 PRMM_VBUF_CFG register

Voltage buffer enable

Table 330. PRMM_VBUF_CFG register - voltage buffer enable (address 180Ch) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						VDDCEN	VAUXEN
Reset	0	0	0	0	0	0	1	1
Access	R	R	R	R	R	R	R/W	R/W

Table 331. PRMM_VBUF_CFG register - voltage buffer enable (address 180Ch)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VDDCEN	R/W		Voltage buffer for primary VDDC measurement
			0	DISABLED (read-write) Voltage buffer for primary VDDC measurement is disabled.
			1*	ENABLED (read-write) Voltage buffer for primary VDDC measurement is enabled.
0	VAUXEN	R/W		Voltage buffer for primary VAUX measurement
			0	DISABLED (read-write) Voltage buffer for primary VAUX measurement is disabled.
			1*	ENABLED (read-write) Voltage buffer for primary VAUX measurement is enabled.

12.1.142 PRMM_VC_OV_UV_CFG0 register

Cell voltage overvoltage and undervoltage check enable

Table 332. PRMM_VC_OV_UV_CFG0 register - cell voltage over-voltage and under-voltage check enable (address 1810h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	VC15EN	VC14EN	VC13EN	VC12EN	VC11EN	VC10EN	VC9EN	VC8EN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	VC7EN	VC6EN	VC5EN	VC4EN	VC3EN	VC2EN	VC1EN	VC0EN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 333. PRMM_VC_OV_UV_CFG0 register - cell voltage over-voltage and under-voltage check enable (address 1810h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	VC15EN	R/W		Include VC15 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC15 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC15 is included in VC over-voltage and under-voltage checks.
14	VC14EN	R/W		Include VC14 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC14 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC14 is included in VC over-voltage and under-voltage checks.
13	VC13EN	R/W		Include VC13 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC13 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC13 is included in VC over-voltage and under-voltage checks.
12	VC12EN	R/W		Include VC12 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC12 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC12 is included in VC over-voltage and under-voltage checks.
11	VC11EN	R/W		Include VC11 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC11 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC11 is included in VC over-voltage and under-voltage checks.
10	VC10EN	R/W		Include VC10 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC10 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC10 is included in VC over-voltage and under-voltage checks.
9	VC9EN	R/W		Include VC9 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC9 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC9 is included in VC over-voltage and under-voltage checks.
8	VC8EN	R/W		Include VC8 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC8 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC8 is included in VC over-voltage and under-voltage checks.
7	VC7EN	R/W		Include VC7 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC7 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC7 is included in VC over-voltage and under-voltage checks.

Table 333. PRMM_VC_OV_UV_CFG0 register - cell voltage over-voltage and under-voltage check enable (address 1810h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
6	VC6EN	R/W		Include VC6 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC6 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC6 is included in VC over-voltage and under-voltage checks.
5	VC5EN	R/W		Include VC5 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC5 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC5 is included in VC over-voltage and under-voltage checks.
4	VC4EN	R/W		Include VC4 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC4 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC4 is included in VC over-voltage and under-voltage checks.
3	VC3EN	R/W		Include VC3 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC3 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC3 is included in VC over-voltage and under-voltage checks.
2	VC2EN	R/W		Include VC2 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC2 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC2 is included in VC over-voltage and under-voltage checks.
1	VC1EN	R/W		Include VC1 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC1 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC1 is included in VC over-voltage and under-voltage checks.
0	VC0EN	R/W		Include VC0 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC0 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC0 is included in VC over-voltage and under-voltage checks.

12.1.143 PRMM_VC_OV_UV_CFG1 register

Cell voltage over-voltage and under-voltage check enable

Table 334. PRMM_VC_OV_UV_CFG1 register - cell voltage over-voltage and under-voltage check enable (address 1811h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0

Table 334. PRMM_VC_OV_UV_CFG1 register - cell voltage over-voltage and under-voltage check enable (address 1811h) bit allocation*...continued*

Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						VC17EN	VC16EN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 335. PRMM_VC_OV_UV_CFG1 register - cell voltage over-voltage and under-voltage check enable (address 1811h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VC17EN	R/W		Include VC17 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC17 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC17 is included in VC over-voltage and under-voltage checks.
0	VC16EN	R/W		Include VC16 in VC over-voltage and under-voltage checks
			0*	NO_CHECK (read-write) VC16 is not included in VC over-voltage and under-voltage checks.
			1	UV_OV (read-write) VC16 is included in VC over-voltage and under-voltage checks.

12.1.144 PRMM_VC_OV_TH_CFG register

Upper comparator limit for VC0 to VC17

Table 336. PRMM_VC_OV_TH_CFG register - upper comparator limit for VC0 to VC17 (address 1812h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 337. PRMM_VC_OV_TH_CFG register - upper comparator limit for VC0 to VC17 (address 1812h)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	7FFFh	Limit value. If this limit is reached, the OV status is activated.

12.1.145 PRMM_VC_UV0_TH_CFG register

Lower comparator limit 0 for VC0 to VC17

Table 338. PRMM_VC_UV0_TH_CFG register - lower comparator limit 0 for VC0 to VC17 (address 1813h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 338. PRMM_VC_UV0_TH_CFG register - lower comparator limit 0 for VC0 to VC17 (address 1813h) bit allocation*...continued*

Symbol	LIMIT															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 339. PRMM_VC_UV0_TH_CFG register - lower comparator limit 0 for VC0 to VC17 (address 1813h)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	0h	Limit value. If this limit is reached, the channel individual UV status is activated. Note: This limit is used for the channel individual balancing disable.

12.1.146 PRMM_VC_UV1_TH_CFG register

Lower comparator limit 1 for VC0 to VC17

Table 340. PRMM_VC_UV1_TH_CFG register - lower comparator limit 1 for VC0 to VC17 (address 1814h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 341. PRMM_VC_UV1_TH_CFG register - lower comparator limit 1 for VC0 to VC17 (address 1814h)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	0h	Limit value. If this limit is reached, the global UV status is activated. Note: This limit is used for the global balancing disable.

12.1.147 PRMM_AIN0_OV_TH_CFG register

Upper comparator limit for AIN0

Table 342. PRMM_AIN0_OV_TH_CFG register - upper comparator limit for AIN0 (address 1815h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 343. PRMM_AIN0_OV_TH_CFG register - upper comparator limit for AIN0 (address 1815h)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	7FFFh	Limit value. If this limit is reached, the OV status is activated.

12.1.148 PRMM_AIN1_OV_TH_CFG register

Upper comparator limit for AIN1

Table 344. PRMM_AIN1_OV_TH_CFG register - upper comparator limit for AIN1 (address 1816h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 345. PRMM_AIN1_OV_TH_CFG register - upper comparator limit for AIN1 (address 1816h)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	7FFFh	Limit value. If this limit is reached, the OV status is activated.

12.1.149 PRMM_AIN2_OV_TH_CFG register

Upper comparator limit for AIN2

Table 346. PRMM_AIN2_OV_TH_CFG register - upper comparator limit for AIN2 (address 1817h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 347. PRMM_AIN2_OV_TH_CFG register - upper comparator limit for AIN2 (address 1817h)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	7FFFh	Limit value. If this limit is reached, the OV status is activated.

12.1.150 PRMM_AIN3_OV_TH_CFG register

Upper comparator limit for AIN3

Table 348. PRMM_AIN3_OV_TH_CFG register - upper comparator limit for AIN3 (address 1818h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 349. PRMM_AIN3_OV_TH_CFG register - upper comparator limit for AIN3 (address 1818h)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	7FFFh	Limit value. If this limit is reached, the OV status is activated.

12.1.151 PRMM_AINA_OV_TH_CFG register

Upper comparator limit for AINA

Table 350. PRMM_AINA_OV_TH_CFG register - upper comparator limit for AINA (address 1819h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 351. PRMM_AINA_OV_TH_CFG register - upper comparator limit for AINA (address 1819h)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	7FFFh	Limit value. If this limit is reached, the OV status is activated.

12.1.152 PRMM_AIN0_UV_TH_CFG register

Lower comparator limit for AIN0

Table 352. PRMM_AIN0_UV_TH_CFG register - lower comparator limit for AIN0 (address 181Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 353. PRMM_AIN0_UV_TH_CFG register - lower comparator limit for AIN0 (address 181Ah)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	8001h	Limit value. If this limit is reached, the UV status is activated.

12.1.153 PRMM_AIN1_UV_TH_CFG register

Lower comparator limit for AIN1

Table 354. PRMM_AIN1_UV_TH_CFG register - lower comparator limit for AIN1 (address 181Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 355. PRMM_AIN1_UV_TH_CFG register - lower comparator limit for AIN1 (address 181Bh)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	8001h	Limit value. If this limit is reached, the UV status is activated.

12.1.154 PRMM_AIN2_UV_TH_CFG register

Lower comparator limit for AIN2

Table 356. PRMM_AIN2_UV_TH_CFG register - lower comparator limit for AIN2 (address 181Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 357. PRMM_AIN2_UV_TH_CFG register - lower comparator limit for AIN2 (address 181Ch)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	8001h	Limit value. If this limit is reached, the UV status is activated.

12.1.155 PRMM_AIN3_UV_TH_CFG register

Lower comparator limit for AIN3

Table 358. PRMM_AIN3_UV_TH_CFG register - lower comparator limit for AIN3 (address 181Dh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 359. PRMM_AIN3_UV_TH_CFG register - lower comparator limit for AIN3 (address 181Dh)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	8001h	Limit value. If this limit is reached, the UV status is activated.

12.1.156 PRMM_AINA_UV_TH_CFG register

Lower comparator limit for AINA

Table 360. PRMM_AINA_UV_TH_CFG register - lower comparator limit for AINA (address 181Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	LIMIT															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 361. PRMM_AINA_UV_TH_CFG register - lower comparator limit for AINA (address 181Eh)

Bit	Symbol	Access	Value	Description
15:0	LIMIT	R/W	8001h	Limit value. If this limit is reached, the UV status is activated.

12.1.157 PRMM_CAL_CRC register

CRC over calibration data

Table 362. PRMM_CAL_CRC register - CRC over calibration data (address 1820h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CRC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 363. PRMM_CAL_CRC register - CRC over calibration data (address 1820h)

Bit	Symbol	Access	Value	Description
15:0	CRC	R/W	0h	CRC over calibration data. The CRC calculation runs automatically every time when a synchronous measurement cycle is started and when the calibration data is read from the NVM.
			BEEFh	CALIBCRC (read-write) The expected value of the calibration CRC.

12.1.158 PRMM_CFG_CRC register

CRC over configuration values

Table 364. PRMM_CFG_CRC register - CRC over configuration values (address 1821h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CRC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 365. PRMM_CFG_CRC register - CRC over configuration values (address 1821h)

Bit	Symbol	Access	Value	Description
15:0	CRC	R	0h	This CRC value is recalculated with any transition into Active mode, with any write to a covered register and with any read to this register. The updated CRC value is available latest 100 µs after the last write. The CRC value is application specific and must be re-calculated by the MCU. The used polynomial is: D175h (+1) = $X^{16} + X^{15} + X^{13} + X^{9} + X^{7} + X^{6} + X^{5} + X^{3} + X^{1} + 1$. Following registers are included: PRMM_CFG, PRMM_PER_CTRL, PRMM_VC_CFG0, PRMM_VC_CFG1, PRMM_AIN_CFG, PRMM_VBUF_CFG, PRMM_VC_OV_UV_CFG0, PRMM_VC_OV_UV_CFG1, PRMM_VC_OV_TH_CFG, PRMM_VC_UV0_TH_CFG, PRMM_VC_UV1_TH_CFG, PRMM_AIN0_OV_TH_CFG, PRMM_AIN1_OV_TH_CFG, PRMM_AIN2_OV_TH_CFG, PRMM_

Table 365. PRMM_CFG_CRC register - CRC over configuration values (address 1821h)

Bit	Symbol	Access	Value	Description
				AIN3_OV_TH_CFG, PRMM_AINA_OV_TH_CFG, PRMM_AIN0_UV_TH_CFG, PRMM_AIN1_UV_TH_CFG, PRMM_AIN2_UV_TH_CFG, PRMM_AIN3_UV_TH_CFG, PRMM_AINA_UV_TH_CFG.

12.1.159 PRMM_VC_OV_FLT_STAT0 register

Cell voltage over-voltage status

Table 366. PRMM_VC_OV_FLT_STAT0 register - cell voltage over-voltage status (address 1822h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	VC15	VC14	VC13	VC12	VC11	VC10	VC9	VC8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 367. PRMM_VC_OV_FLT_STAT0 register - cell voltage over-voltage status (address 1822h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	VC15	R		Over-voltage status VC15 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
14	VC14	R		Over-voltage status VC14 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
13	VC13	R		Over-voltage status VC13 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
12	VC12	R		Over-voltage status VC12 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
11	VC11	R		Over-voltage status VC11 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
10	VC10	R		Over-voltage status VC10 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
9	VC9	R		Over-voltage status VC9 Read clears bit.

Table 367. PRMM_VC_OV_FLT_STAT0 register - cell voltage over-voltage status (address 1822h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
8	VC8	R		Over-voltage status VC8 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
7	VC7	R		Over-voltage status VC7 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
6	VC6	R		Over-voltage status VC6 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
5	VC5	R		Over-voltage status VC5 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
4	VC4	R		Over-voltage status VC4 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
3	VC3	R		Over-voltage status VC3 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
2	VC2	R		Over-voltage status VC2 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
1	VC1	R		Over-voltage status VC1 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
0	VC0	R		Over-voltage status VC0 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected

12.1.160 PRMM_VC_OV_FLT_STAT1 register

Cell voltage over-voltage status

Table 368. PRMM_VC_OV_FLT_STAT1 register - cell voltage over-voltage status (address 1823h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Table 368. PRMM_VC_OV_FLT_STAT1 register - cell voltage over-voltage status (address 1823h) bit allocation*...continued*

Symbol	reserved						VC17	VC16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 369. PRMM_VC_OV_FLT_STAT1 register - cell voltage over-voltage status (address 1823h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VC17	R		Over-voltage status VC17 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
0	VC16	R		Over-voltage status VC16 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected

12.1.161 PRMM_VC_UV0_FLT_STAT0 register

Cell voltage under-voltage status regarding limit 0

Table 370. PRMM_VC_UV0_FLT_STAT0 register - cell voltage under-voltage status regarding limit 0 (address 1824h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	VC15	VC14	VC13	VC12	VC11	VC10	VC9	VC8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 371. PRMM_VC_UV0_FLT_STAT0 register - cell voltage under-voltage status regarding limit 0 (address 1824h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	VC15	R		Under-voltage status VC15 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
14	VC14	R		Under-voltage status VC14 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
13	VC13	R		Under-voltage status VC13 Read clears bit.

Table 371. PRMM_VC_UV0_FLT_STAT0 register - cell voltage under-voltage status regarding limit 0 (address 1824h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
12	VC12	R		Under-voltage status VC12 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
11	VC11	R		Under-voltage status VC11 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
10	VC10	R		Under-voltage status VC10 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
9	VC9	R		Under-voltage status VC9 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
8	VC8	R		Under-voltage status VC8 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
7	VC7	R		Under-voltage status VC7 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
6	VC6	R		Under-voltage status VC6 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
5	VC5	R		Under-voltage status VC5 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
4	VC4	R		Under-voltage status VC4 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
3	VC3	R		Under-voltage status VC3 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
2	VC2	R		Under-voltage status VC2 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
1	VC1	R		Under-voltage status VC1 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected

Table 371. PRMM_VC_UV0_FLT_STAT0 register - cell voltage under-voltage status regarding limit 0 (address 1824h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
0	VC0	R		Under-voltage status VC0 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected

12.1.162 PRMM_VC_UV0_FLT_STAT1 register

Cell voltage under-voltage status regarding limit 0

Table 372. PRMM_VC_UV0_FLT_STAT1 register - cell voltage under-voltage status regarding limit 0 (address 1825h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						VC17	VC16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 373. PRMM_VC_UV0_FLT_STAT1 register - cell voltage under-voltage status regarding limit 0 (address 1825h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VC17	R		Under-voltage status VC17 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
0	VC16	R		Under-voltage status VC16 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected

12.1.163 PRMM_VC_UV1_FLT_STAT0 register

Cell voltage under-voltage status regarding limit 1

Table 374. PRMM_VC_UV1_FLT_STAT0 register - cell voltage under-voltage status regarding limit 1 (address 1826h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	VC15	VC14	VC13	VC12	VC11	VC10	VC9	VC8
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Table 374. PRMM_VC_UV1_FLT_STAT0 register - cell voltage under-voltage status regarding limit 1 (address 1826h) bit allocation*...continued*

Symbol	VC7	VC6	VC5	VC4	VC3	VC2	VC1	VC0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 375. PRMM_VC_UV1_FLT_STAT0 register - cell voltage under-voltage status regarding limit 1 (address 1826h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	VC15	R		Under-voltage status VC15 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
14	VC14	R		Under-voltage status VC14 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
13	VC13	R		Under-voltage status VC13 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
12	VC12	R		Under-voltage status VC12 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
11	VC11	R		Under-voltage status VC11 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
10	VC10	R		Under-voltage status VC10 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
9	VC9	R		Under-voltage status VC9 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
8	VC8	R		Under-voltage status VC8 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
7	VC7	R		Under-voltage status VC7 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
6	VC6	R		Under-voltage status VC6 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
5	VC5	R		Under-voltage status VC5 Read clears bit.
			0*	NO_UV (read) No under-voltage detected

Table 375. PRMM_VC_UV1_FLT_STAT0 register - cell voltage under-voltage status regarding limit 1 (address 1826h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			1	UV (read) Under-voltage detected
4	VC4	R		Under-voltage status VC4 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
3	VC3	R		Under-voltage status VC3 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
2	VC2	R		Under-voltage status VC2 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
1	VC1	R		Under-voltage status VC1 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
0	VC0	R		Under-voltage status VC0 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected

12.1.164 PRMM_VC_UV1_FLT_STAT1 register

Cell voltage under-voltage status regarding limit 1

Table 376. PRMM_VC_UV1_FLT_STAT1 register - cell voltage under-voltage status regarding limit 1 (address 1827h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						VC17	VC16
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 377. PRMM_VC_UV1_FLT_STAT1 register - cell voltage under-voltage status regarding limit 1 (address 1827h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VC17	R		Under-voltage status VC17 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected

Table 377. PRMM_VC_UV1_FLT_STAT1 register - cell voltage under-voltage status regarding limit 1 (address 1827h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
0	VC16	R		Under-voltage status VC16 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected

12.1.165 PRMM_AIN_OV_FLT_STAT register

AINx over-voltage status

Table 378. PRMM_AIN_OV_FLT_STAT register - AINx over-voltage status (address 1828h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved			AINA	AIN3	AIN2	AIN1	AIN0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 379. PRMM_AIN_OV_FLT_STAT register - AINx over-voltage status (address 1828h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:5	reserved	R	0h	This read-only field is reserved and always has the value 0.
4	AINA	R		Over-voltage status AINA Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
3	AIN3	R		Over-voltage status AIN3 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
2	AIN2	R		Over-voltage status AIN2 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
1	AIN1	R		Over-voltage status AIN1 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected
0	AIN0	R		Over-voltage status AIN0 Read clears bit.
			0*	NO_OV (read) No over-voltage detected
			1	OV (read) Over-voltage detected

12.1.166 PRMM_AIN_UV_FLT_STAT register

AINx under-voltage status

Table 380. PRMM_AIN_UV_FLT_STAT register - AINx under-voltage status (address 1829h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved			AINA	AIN3	AIN2	AIN1	AIN0
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 381. PRMM_AIN_UV_FLT_STAT register - AINx under-voltage status (address 1829h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:5	reserved	R	0h	This read-only field is reserved and always has the value 0.
4	AINA	R		Under-voltage status AINA Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
3	AIN3	R		Under-voltage status AIN3 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
2	AIN2	R		Under-voltage status AIN2 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
1	AIN1	R		Under-voltage status AIN1 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected
0	AIN0	R		Under-voltage status AIN0 Read clears bit.
			0*	NO_UV (read) No under-voltage detected
			1	UV (read) Under-voltage detected

12.1.167 PRMM_MEAS_STAT register

Measurement status

Table 382. PRMM_MEAS_STAT register - measurement status (address 183Eh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	MEASFLT	COMFLT	ANAFLT	SUPPLYFLT	reserved		SYNCRDY	PERRDY
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**

Table 382. PRMM_MEAS_STAT register - measurement status (address 183Eh) bit allocation*...continued*

Symbol	reserved		APPRDYAIN3	APPRDYAIN2	APPRDYAIN1	APPRDYAIN0	APPRDYAINA	APPRDYVC
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 383. PRMM_MEAS_STAT register - measurement status (address 183Eh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	MEASFLT	R		Measurement fault status
			0*	NO_FLT (read) No measurement fault detected
			1	FAULT (read) Measurement fault detected
14	COMFLT	R		Communication fault status
			0*	NO_FLT (read) No communication fault detected
			1	FAULT (read) Communication fault detected.
13	ANAFLT	R		Analog fault status
			0*	NO_FLT (read) No analog fault detected
			1	FAULT (read) Analog fault detected
12	SUPPLYFLT	R		Internal/external supply fault status
			0*	NO_FLT (read) No supply error detected
			1	FAULT (read) Supply error detected
11:10	reserved	R	0h	This read-only field is reserved and always has the value 0.
9	SYNCRDY	R		Synchronous measurement data is ready for readout, the bit is cleared by a read into the safety result range.
			0*	NO_DATA (read) No data available
			1	DATA (read) Sample data available.
8	PERRDY	R		New periodic result data has been created (depending on the periodic update mode, they might need to be requested), the bit is cleared by a read to any register in the range PRMM_PER_VC0 to (PRMM_PER_VDDC + 1) if PRMM_PER_CTRL.PERCTRL is set to AUTO. If PRMM_PER_CTRL.PERCTRL is set to ONCE, a write to PRMM_PER_CTRL.PERCTRL == ONCE clears it.
			0*	NO_DATA (read) No data available
			1	DATA (read) Sample data available.
7:6	reserved	R	0h	This read-only field is reserved and always has the value 0.
5	APPRDYAIN3	R		A new AIN3 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
4	APPRDYAIN2	R		A new AIN2 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
3	APPRDYAIN1	R		A new AIN1 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)

Table 383. PRMM_MEAS_STAT register - measurement status (address 183Eh)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			1	DATA (read) Data can be captured (>=16 samples are captured).
2	APPRDYAIN0	R		A new AIN0 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
1	APPRDYAINA	R		A new AINA application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
0	APPRDYVC	R		A new VC application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).

12.1.168 PRMM_APP_VC_CNT register

Application measurement VC sample count number

Table 384. PRMM_APP_VC_CNT register - application measurement VC sample count number (address 183Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	NUM															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 385. PRMM_APP_VC_CNT register - application measurement VC sample count number (address 183Fh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:0	NUM	R		Number of samples used for Application result. Read clears bits.
			0000h*	LOW (read) Zero or insufficient samples, VC Application results are invalid.
			FFFFh	OVERRUN (read) Sample counter overrun, VC Application results are invalid.

12.1.169 PRMM_APP_VC0 register

Application measurement result cell 0

Table 386. PRMM_APP_VC0 register - application measurement result cell 0 (address 1840h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 386. PRMM_APP_VC0 register - application measurement result cell 0 (address 1840h) bit allocation*...continued*

Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 387. PRMM_APP_VC0 register - application measurement result cell 0 (address 1840h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 0 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.170 PRMM_APP_VC1 register

Application measurement result cell 1

Table 388. PRMM_APP_VC1 register - application measurement result cell 1 (address 1841h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 389. PRMM_APP_VC1 register - application measurement result cell 1 (address 1841h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 1 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.171 PRMM_APP_VC2 register

Application measurement result cell 2

Table 390. PRMM_APP_VC2 register - application measurement result cell 2 (address 1842h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 391. PRMM_APP_VC2 register - application measurement result cell 2 (address 1842h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 2 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.172 PRMM_APP_VC3 register

Application measurement result cell 3

Table 392. PRMM_APP_VC3 register - application measurement result cell 3 (address 1843h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 392. PRMM_APP_VC3 register - application measurement result cell 3 (address 1843h) bit allocation*...continued*

Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 393. PRMM_APP_VC3 register - application measurement result cell 3 (address 1843h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 3 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.173 PRMM_APP_VC4 register

Application measurement result cell 4

Table 394. PRMM_APP_VC4 register - application measurement result cell 4 (address 1844h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 395. PRMM_APP_VC4 register - application measurement result cell 4 (address 1844h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 4 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.174 PRMM_APP_VC5 register

Application measurement result cell 5

Table 396. PRMM_APP_VC5 register - application measurement result cell 5 (address 1845h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 397. PRMM_APP_VC5 register - application measurement result cell 5 (address 1845h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 5 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.175 PRMM_APP_VC6 register

Application measurement result cell 6

Table 398. PRMM_APP_VC6 register - application measurement result cell 6 (address 1846h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 399. PRMM_APP_VC6 register - application measurement result cell 6 (address 1846h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 6 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.176 PRMM_APP_VC7 register

Application measurement result cell 7

Table 400. PRMM_APP_VC7 register - application measurement result cell 7 (address 1847h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 401. PRMM_APP_VC7 register - application measurement result cell 7 (address 1847h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 7 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.177 PRMM_APP_VC8 register

Application measurement result cell 8

Table 402. PRMM_APP_VC8 register - application measurement result cell 8 (address 1848h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 403. PRMM_APP_VC8 register - application measurement result cell 8 (address 1848h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 8 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.178 PRMM_APP_VC9 register

Application measurement result cell 9

Table 404. PRMM_APP_VC9 register - application measurement result cell 9 (address 1849h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 405. PRMM_APP_VC9 register - application measurement result cell 9 (address 1849h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 9 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.179 PRMM_APP_VC10 register

Application measurement result cell 10

Table 406. PRMM_APP_VC10 register - application measurement result cell 10 (address 184Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 407. PRMM_APP_VC10 register - application measurement result cell 10 (address 184Ah)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 10 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.180 PRMM_APP_VC11 register

Application measurement result cell 11

Table 408. PRMM_APP_VC11 register - application measurement result cell 11 (address 184Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 409. PRMM_APP_VC11 register - application measurement result cell 11 (address 184Bh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 11 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.181 PRMM_APP_VC12 register

Application measurement result cell 12

Table 410. PRMM_APP_VC12 register - application measurement result cell 12 (address 184Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 411. PRMM_APP_VC12 register - application measurement result cell 12 (address 184Ch)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 12 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.182 PRMM_APP_VC13 register

Application measurement result cell 13

Table 412. PRMM_APP_VC13 register - application measurement result cell 13 (address 184Dh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 413. PRMM_APP_VC13 register - application measurement result cell 13 (address 184Dh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 13 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.183 PRMM_APP_VC14 register

Application measurement result cell 14

Table 414. PRMM_APP_VC14 register - application measurement result cell 14 (address 184Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															

Table 414. PRMM_APP_VC14 register - application measurement result cell 14 (address 184Eh) bit allocation*...continued*

Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 415. PRMM_APP_VC14 register - application measurement result cell 14 (address 184Eh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 14 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.184 PRMM_APP_VC15 register

Application measurement result cell 15

Table 416. PRMM_APP_VC15 register - application measurement result cell 15 (address 184Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 417. PRMM_APP_VC15 register - application measurement result cell 15 (address 184Fh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 15 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.185 PRMM_APP_VC16 register

Application measurement result cell 16

Table 418. PRMM_APP_VC16 register - application measurement result cell 16 (address 1850h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 419. PRMM_APP_VC16 register - application measurement result cell 16 (address 1850h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 16 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.186 PRMM_APP_VC17 register

Application measurement result cell 17

Table 420. PRMM_APP_VC17 register - application measurement result cell 17 (address 1851h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 421. PRMM_APP_VC17 register - application measurement result cell 17 (address 1851h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 17 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.187 PRMM_APP_AINA register

Application measurement result AINA

Table 422. PRMM_APP_AINA register - application measurement result AINA (address 1852h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 423. PRMM_APP_AINA register - application measurement result AINA (address 1852h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AINA at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.188 PRMM_APP_AIN0 register

Application measurement result AIN0

Table 424. PRMM_APP_AIN0 register - application measurement result AIN0 (address 1853h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 425. PRMM_APP_AIN0 register - application measurement result AIN0 (address 1853h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN0 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.189 PRMM_APP_AIN1 register

Application measurement result AIN1

Table 426. PRMM_APP_AIN1 register - application measurement result AIN1 (address 1854h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 427. PRMM_APP_AIN1 register - application measurement result AIN1 (address 1854h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN1 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.190 PRMM_APP_AIN2 register

Application measurement result AIN2

Table 428. PRMM_APP_AIN2 register - application measurement result AIN2 (address 1855h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 429. PRMM_APP_AIN2 register - application measurement result AIN2 (address 1855h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN2 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.191 PRMM_APP_AIN3 register

Application measurement result AIN3

Table 430. PRMM_APP_AIN3 register - application measurement result AIN3 (address 1856h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 431. PRMM_APP_AIN3 register - application measurement result AIN3 (address 1856h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN3 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.192 PRMM_PER_NUM register

Measurement period number of the primary periodic results

Table 432. PRMM_PER_NUM register - measurement period number of the primary periodic results (address 185Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	NUM															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 433. PRMM_PER_NUM register - measurement period number of the primary periodic results (address 185Fh)

Bit	Symbol	Access	Value	Description
15:0	NUM	R	0h	Number of the periodic cycle in which the primary periodic results have been created. The value is incremented for each periodic cycle executed. The counting wraps at its limit.

12.1.193 PRMM_PER_VC0 register

Periodic measurement result cell 0

Table 434. PRMM_PER_VC0 register - periodic measurement result cell 0 (address 1860h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 435. PRMM_PER_VC0 register - periodic measurement result cell 0 (address 1860h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 0 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.194 PRMM_PER_VC1 register

Periodic measurement result cell 1

Table 436. PRMM_PER_VC1 register - periodic measurement result cell 1 (address 1861h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 437. PRMM_PER_VC1 register - periodic measurement result cell 1 (address 1861h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 1 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.195 PRMM_PER_VC2 register

Periodic measurement result cell 2

Table 438. PRMM_PER_VC2 register - periodic measurement result cell 2 (address 1862h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 439. PRMM_PER_VC2 register - periodic measurement result cell 2 (address 1862h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 2 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.196 PRMM_PER_VC3 register

Periodic measurement result cell 3

Table 440. PRMM_PER_VC3 register - periodic measurement result cell 3 (address 1863h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 441. PRMM_PER_VC3 register - periodic measurement result cell 3 (address 1863h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 3 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.197 PRMM_PER_VC4 register

Periodic measurement result cell 4

Table 442. PRMM_PER_VC4 register - periodic measurement result cell 4 (address 1864h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 443. PRMM_PER_VC4 register - periodic measurement result cell 4 (address 1864h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 4 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.198 PRMM_PER_VC5 register

Periodic measurement result cell 5

Table 444. PRMM_PER_VC5 register - periodic measurement result cell 5 (address 1865h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 445. PRMM_PER_VC5 register - periodic measurement result cell 5 (address 1865h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 5 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.199 PRMM_PER_VC6 register

Periodic measurement result cell 6

Table 446. PRMM_PER_VC6 register - periodic measurement result cell 6 (address 1866h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 447. PRMM_PER_VC6 register - periodic measurement result cell 6 (address 1866h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 6 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.200 PRMM_PER_VC7 register

Periodic measurement result cell 7

Table 448. PRMM_PER_VC7 register - periodic measurement result cell 7 (address 1867h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 449. PRMM_PER_VC7 register - periodic measurement result cell 7 (address 1867h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 7 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.201 PRMM_PER_VC8 register

Periodic measurement result cell 8

Table 450. PRMM_PER_VC8 register - periodic measurement result cell 8 (address 1868h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 451. PRMM_PER_VC8 register - periodic measurement result cell 8 (address 1868h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 8 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.202 PRMM_PER_VC9 register

Periodic measurement result cell 9

Table 452. PRMM_PER_VC9 register - periodic measurement result cell 9 (address 1869h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 453. PRMM_PER_VC9 register - periodic measurement result cell 9 (address 1869h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 9 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.203 PRMM_PER_VC10 register

Periodic measurement result cell 10

Table 454. PRMM_PER_VC10 register - periodic measurement result cell 10 (address 186Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 455. PRMM_PER_VC10 register - periodic measurement result cell 10 (address 186Ah)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 10 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.204 PRMM_PER_VC11 register

Periodic measurement result cell 11

Table 456. PRMM_PER_VC11 register - periodic measurement result cell 11 (address 186Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 457. PRMM_PER_VC11 register - periodic measurement result cell 11 (address 186Bh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 11 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.205 PRMM_PER_VC12 register

Periodic measurement result cell 12

Table 458. PRMM_PER_VC12 register - periodic measurement result cell 12 (address 186Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 459. PRMM_PER_VC12 register - periodic measurement result cell 12 (address 186Ch)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 12 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.206 PRMM_PER_VC13 register

Periodic measurement result cell 13

Table 460. PRMM_PER_VC13 register - periodic measurement result cell 13 (address 186Dh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 461. PRMM_PER_VC13 register - periodic measurement result cell 13 (address 186Dh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 13 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.207 PRMM_PER_VC14 register

Periodic measurement result cell 14

Table 462. PRMM_PER_VC14 register - periodic measurement result cell 14 (address 186Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 463. PRMM_PER_VC14 register - periodic measurement result cell 14 (address 186Eh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 14 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.208 PRMM_PER_VC15 register

Periodic measurement result cell 15

Table 464. PRMM_PER_VC15 register - periodic measurement result cell 15 (address 186Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 465. PRMM_PER_VC15 register - periodic measurement result cell 15 (address 186Fh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 15 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.209 PRMM_PER_VC16 register

Periodic measurement result cell 16

Table 466. PRMM_PER_VC16 register - periodic measurement result cell 16 (address 1870h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 467. PRMM_PER_VC16 register - periodic measurement result cell 16 (address 1870h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 16 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.210 PRMM_PER_VC17 register

Periodic measurement result cell 17

Table 468. PRMM_PER_VC17 register - periodic measurement result cell 17 (address 1871h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 469. PRMM_PER_VC17 register - periodic measurement result cell 17 (address 1871h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 17 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.211 PRMM_PER_AINA register

Periodic measurement result AINA

Table 470. PRMM_PER_AINA register - periodic measurement result AINA (address 1872h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 471. PRMM_PER_AINA register - periodic measurement result AINA (address 1872h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AINA of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.212 PRMM_PER_AIN0 register

Periodic measurement result AIN0

Table 472. PRMM_PER_AIN0 register - periodic measurement result AIN0 (address 1873h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 473. PRMM_PER_AIN0 register - periodic measurement result AIN0 (address 1873h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN0 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.213 PRMM_PER_AIN1 register

Periodic measurement result AIN1

Table 474. PRMM_PER_AIN1 register - periodic measurement result AIN1 (address 1874h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 475. PRMM_PER_AIN1 register - periodic measurement result AIN1 (address 1874h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN1 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.214 PRMM_PER_AIN2 register

Periodic measurement result AIN2

Table 476. PRMM_PER_AIN2 register - periodic measurement result AIN2 (address 1875h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 477. PRMM_PER_AIN2 register - periodic measurement result AIN2 (address 1875h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN2 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.215 PRMM_PER_AIN3 register

Periodic measurement result AIN3

Table 478. PRMM_PER_AIN3 register - periodic measurement result AIN3 (address 1876h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 479. PRMM_PER_AIN3 register - periodic measurement result AIN3 (address 1876h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN3 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.216 PRMM_PER_PRMTEMP register

Periodic measurement result primary device temperature

Table 480. PRMM_PER_PRMTEMP register - periodic measurement result primary device temperature (address 1877h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 481. PRMM_PER_PRMTEMP register - periodic measurement result primary device temperature (address 1877h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured value of primary temperature sensor of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.217 PRMM_PER_SECVREF register

Periodic measurement result secondary voltage reference

Table 482. PRMM_PER_SECVREF register - periodic measurement result secondary voltage reference (address 1878h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 483. PRMM_PER_SECVREF register - periodic measurement result secondary voltage reference (address 1878h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of secondary reference voltage of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.218 PRMM_PER_VAUX register

Periodic measurement result auxiliary supply voltage

Table 484. PRMM_PER_VAUX register - periodic measurement result auxiliary supply voltage (address 1879h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 484. PRMM_PER_VAUX register - periodic measurement result auxiliary supply voltage (address 1879h) bit allocation*...continued*

Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 485. PRMM_PER_VAUX register - periodic measurement result auxiliary supply voltage (address 1879h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of VAUX of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.219 PRMM_PER_VDDC register

Periodic measurement result VDDC

Table 486. PRMM_PER_VDDC register - periodic measurement result VDDC (address 187Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 487. PRMM_PER_VDDC register - periodic measurement result VDDC (address 187Ah)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of VDDC of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.220 PRMM_SYNC_NUM register

Measurement period number of the synchronous results.

Table 488. PRMM_SYNC_NUM register - measurement period number of the synchronous results. (address 187Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	NUM															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 489. PRMM_SYNC_NUM register - measurement period number of the synchronous results. (address 187Fh)

Bit	Symbol	Access	Value	Description
15:0	NUM	R	0h	Number of the synchronous cycle in which the synchronous results have been created. The value is incremented for each synchronous cycle executed. The counting wraps at its limit.

12.1.221 PRMM_SYNC_VC0 register

Synchronous measurement result cell 0

Table 490. PRMM_SYNC_VC0 register - synchronous measurement result cell 0 (address 1880h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 491. PRMM_SYNC_VC0 register - synchronous measurement result cell 0 (address 1880h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 0 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.222 PRMM_SYNC_VC1 register

Synchronous measurement result cell 1

Table 492. PRMM_SYNC_VC1 register - synchronous measurement result cell 1 (address 1881h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 493. PRMM_SYNC_VC1 register - synchronous measurement result cell 1 (address 1881h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 1 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.223 PRMM_SYNC_VC2 register

Synchronous measurement result cell 2

Table 494. PRMM_SYNC_VC2 register - synchronous measurement result cell 2 (address 1882h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 495. PRMM_SYNC_VC2 register - synchronous measurement result cell 2 (address 1882h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 2 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.224 PRMM_SYNC_VC3 register

Synchronous measurement result cell 3

Table 496. PRMM_SYNC_VC3 register - synchronous measurement result cell 3 (address 1883h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 497. PRMM_SYNC_VC3 register - synchronous measurement result cell 3 (address 1883h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 3 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.225 PRMM_SYNC_VC4 register

Synchronous measurement result cell 4

Table 498. PRMM_SYNC_VC4 register - synchronous measurement result cell 4 (address 1884h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 499. PRMM_SYNC_VC4 register - synchronous measurement result cell 4 (address 1884h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 4 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.226 PRMM_SYNC_VC5 register

Synchronous measurement result cell 5

Table 500. PRMM_SYNC_VC5 register - synchronous measurement result cell 5 (address 1885h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															

Table 500. PRMM_SYNC_VC5 register - synchronous measurement result cell 5 (address 1885h) bit allocation*...continued*

Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 501. PRMM_SYNC_VC5 register - synchronous measurement result cell 5 (address 1885h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 5 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.227 PRMM_SYNC_VC6 register

Synchronous measurement result cell 6

Table 502. PRMM_SYNC_VC6 register - synchronous measurement result cell 6 (address 1886h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 503. PRMM_SYNC_VC6 register - synchronous measurement result cell 6 (address 1886h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 6 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.228 PRMM_SYNC_VC7 register

Synchronous measurement result cell 7

Table 504. PRMM_SYNC_VC7 register - synchronous measurement result cell 7 (address 1887h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 505. PRMM_SYNC_VC7 register - synchronous measurement result cell 7 (address 1887h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 7 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.229 PRMM_SYNC_VC8 register

Synchronous measurement result cell 8

Table 506. PRMM_SYNC_VC8 register - synchronous measurement result cell 8 (address 1888h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 507. PRMM_SYNC_VC8 register - synchronous measurement result cell 8 (address 1888h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 8 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.230 PRMM_SYNC_VC9 register

Synchronous measurement result cell 9

Table 508. PRMM_SYNC_VC9 register - synchronous measurement result cell 9 (address 1889h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 509. PRMM_SYNC_VC9 register - synchronous measurement result cell 9 (address 1889h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 9 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.231 PRMM_SYNC_VC10 register

Synchronous measurement result cell 10

Table 510. PRMM_SYNC_VC10 register - synchronous measurement result cell 10 (address 188Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 511. PRMM_SYNC_VC10 register - synchronous measurement result cell 10 (address 188Ah)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 10 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.232 PRMM_SYNC_VC11 register

Synchronous measurement result cell 11

Table 512. PRMM_SYNC_VC11 register - synchronous measurement result cell 11 (address 188Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 513. PRMM_SYNC_VC11 register - synchronous measurement result cell 11 (address 188Bh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 11 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.233 PRMM_SYNC_VC12 register

Synchronous measurement result cell 12

Table 514. PRMM_SYNC_VC12 register - synchronous measurement result cell 12 (address 188Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 515. PRMM_SYNC_VC12 register - synchronous measurement result cell 12 (address 188Ch)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 12 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.234 PRMM_SYNC_VC13 register

Synchronous measurement result cell 13

Table 516. PRMM_SYNC_VC13 register - synchronous measurement result cell 13 (address 188Dh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															

Table 516. PRMM_SYNC_VC13 register - synchronous measurement result cell 13 (address 188Dh) bit allocation*...continued*

Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 517. PRMM_SYNC_VC13 register - synchronous measurement result cell 13 (address 188Dh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 13 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.235 PRMM_SYNC_VC14 register

Synchronous measurement result cell 14

Table 518. PRMM_SYNC_VC14 register - synchronous measurement result cell 14 (address 188Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 519. PRMM_SYNC_VC14 register - synchronous measurement result cell 14 (address 188Eh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 14 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.236 PRMM_SYNC_VC15 register

Synchronous measurement result cell 15

Table 520. PRMM_SYNC_VC15 register - synchronous measurement result cell 15 (address 188Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 521. PRMM_SYNC_VC15 register - synchronous measurement result cell 15 (address 188Fh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 15 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.237 PRMM_SYNC_VC16 register

Synchronous measurement result cell 16

Table 522. PRMM_SYNC_VC16 register - synchronous measurement result cell 16 (address 1890h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 523. PRMM_SYNC_VC16 register - synchronous measurement result cell 16 (address 1890h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 16 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.238 PRMM_SYNC_VC17 register

Synchronous measurement result cell 17

Table 524. PRMM_SYNC_VC17 register - synchronous measurement result cell 17 (address 1891h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 525. PRMM_SYNC_VC17 register - synchronous measurement result cell 17 (address 1891h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 17 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.239 SECM_CFG register

General measurement control

Table 526. SECM_CFG register - general measurement control (address 1C00h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	BALPAUSELEN							
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	BALPAUSELEN						BALPAUSECYCMODEN	MEASEN
Reset	0	0	0	0	0	0	0	0

Table 526. SECM_CFG register - general measurement control (address 1C00h) bit allocation*...continued*

Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 527. SECM_CFG register - general measurement control (address 1C00h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	BALPAUSELEN	R/W		Pause time of balancing before measurement cycle is executed. An on-going balancing pause operation is not influenced by a change of this value. **BALPAUSELEN** * 10 µs
			0000h*	NO_PAUSE (read-write) No Pause.
			0001h	PAUSE_10u (read-write) Pause = 10 us
			3FFFh	MAX (read-write) Maximum pause = 163830 us = 163 ms
1	BALPAUSECYCMODEN	R/W		Enable balancing auto pause. This delays the start of measurements after entering Cyclic mode until the auto pause counter has elapsed. This field has no effect in secondary measurement.
			0*	DISABLED (read-write) auto pause for balancing is disabled.
			1	ENABLED (read-write) auto pause for balancing is enabled. Measurements are started when the auto pause counter is elapsed.
0	MEASEN	R/W		Enable the data acquisition. Setting this bit to zero initiates a result clear and invalidate action (this includes resetting all ready bits). This bit is cleared when entering Sleep mode. Cyclic measurements are always executed, regardless of the value of this bit. Balancing is not stopped automatically (if in Active mode), as it would be permanently inhibited while measurement is active. If balancing shall be paused, please do so via the balancing control.
			0*	DISABLED (read-write) Data acquisition disabled
			1	ENABLED (read-write) Data acquisition enabled

12.1.240 SECM_APP_CTRL register

Application measurement control

Table 528. SECM_APP_CTRL register - application measurement control (address 1C01h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PAUSEBAL	reserved					CAPAIN7	CAPAIN6
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	CAPAIN5	CAPAIN4	CAPAIN3	CAPAIN2	CAPAIN1	CAPAIN0	CAPAINA	CAPVC
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 529. SECM_APP_CTRL register - application measurement control (address 1C01h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	PAUSEBAL	W		Pause the balancing during this capture cycle. If balancing was not paused before, the start of data capture is delayed until the auto pause timer has elapsed. This field has no effect in secondary measurement.
			0*	NO_PAUSE (write) Continue with balancing.
			1	PAUSE (write) Pause the balancing during this capture cycle.
14:10	reserved	W	0h	This read-only field is reserved and always has the value 0.
9	CAPAIN7	W		Capture command for AIN7. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
8	CAPAIN6	W		Capture command for AIN6. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
7	CAPAIN5	W		Capture command for AIN5. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
6	CAPAIN4	W		Capture command for AIN4. When used in combination with PAUSEBAL, a pause of the balancing is forced.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
5	CAPAIN3	W		AIN3 is not part of the secondary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
4	CAPAIN2	W		AIN2 is not part of the secondary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
3	CAPAIN1	W		AIN1 is not part of the secondary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
2	CAPAIN0	W		AIN0 is not part of the secondary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.

Table 529. SECM_APP_CTRL register - application measurement control (address 1C01h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
1	CAPAINA	W		AINA is not part of the secondary measurement chain. Still, when used in combination with PAUSEBAL, a pause of the balancing is forced. The allows to keep the primary and secondary measurement chain synchronized.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.
0	CAPVC	W		Trigger the balancing auto pause if set in combination with the PAUSEBAL bit. Needed to keep primary and secondary measurement synchron when used via the ALLM access. In primary: Capture the application measurement value of the cell terminal measurements.
			0*	NO_CAP (write) Measurements are not captured.
			1	CAP (write) Measurements are captured.

12.1.241 SECM_PER_CTRL register

Periodic measurement control

Table 530. SECM_PER_CTRL register - periodic measurement control (address 1C02h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved			PERCTRL	reserved			PERLEN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R/W	R	R	R	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	PERLEN							
Reset	0	0	0	1	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 531. SECM_PER_CTRL register - periodic measurement control (address 1C02h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:13	reserved	R	0h	This read-only field is reserved and always has the value 0.
12	PERCTRL	R/W		Control the periodic result behavior.
			0*	AUTO (read-write) Periodic results are automatically updated
			1	ONCE (read-write) Periodic results are updated once with the last results. (each write updates the results).
11:9	reserved	R	0h	This read-only field is reserved and always has the value 0.
8:0	PERLEN	R/W		Number of measurements for one periodic measurement. The minimum is 16. Writing a value lower than 16 leads to a 16 in the register.

Table 531. SECM_PER_CTRL register - periodic measurement control (address 1C02h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			010h*	PER_16 (read-write) minimum value = 16 measurements per period
			011h	PER_17 (read-write) 17 measurements per period
			1FFh	PER_MAX (read-write) maximum value = 511 measurements per period

12.1.242 SECM_SYNC_CTRL register

Synchronous measurement control

Table 532. SECM_SYNC_CTRL register - synchronous measurement control (address 1C03h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	PAUSEBAL	VBOLNUM					reserved	
Reset	0	1	1	1	1	1	0	0
Access	W	R/W	R/W	R/W	R/W	R/W	W	W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						FASTVB	SYNCCYC
Reset	0	0	0	0	0	0	0	0
Access	W	W	W	W	W	W	W	W

Table 533. SECM_SYNC_CTRL register - synchronous measurement control (address 1C03h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	PAUSEBAL	W		Pause the balancing during this capture cycle. If balancing was not paused before, the start of data capture is delayed until the auto pause timer has elapsed. If no capture cycle is started this bit is ignored.
			0*	NO_PAUSE (write) Continue with balancing.
			1	PAUSE (write) Pause the balancing during this capture cycle.
14:10	VBOLNUM	R/W		VB number for which the open load detection is enabled. **0 to 17** channel for which the open load detection is enabled. **18 to 29** reserved (no open load detection mechanism is enabled) **30** the open load detection is enabled for the currently measured channel.
			1Fh*	DISABLED (read-write) Open-load detection is disabled
9:2	reserved	W	0h	This read-only field is reserved and always has the value 0.
1	FASTVB	W		Start a fast VB measurement cycle. The fast VB measurement is a measurement of the VBx voltages. The fast VB measurement is initiated by setting the bit SECM_SYNC_CTRL.FASTVB. ADC2B measures each enabled VBx voltage for $28 \times x \times t_{s(meas)}$. Read as zero.
			0*	NO_FAST (write) No new start of a fast VB measurement cycle.

Table 533. SECM_SYNC_CTRL register - synchronous measurement control (address 1C03h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	STATUS (read) Read as zero.
			1	FAST (write) Start a new fast VB measurement cycle.
0	SYNCCYC	W		Start a synchronous measurement cycle. In this cycle the CT and CB voltages are measured and stored as matching pairs. If no VB channel is enabled or if set during a running synchronous measurement cycle or a running Fast VB cycle, the set is ignored. Read as zero.
			0*	NO_START (write) No new start a synchronous measurement cycle.
			0*	STATUS (read) Read as zero.
			1	START (write) Start a synchronous measurement cycle.

12.1.243 SECM_VB_CFG0 register

Balance voltage measurement enable

Table 534. SECM_VB_CFG0 register - balance voltage measurement enable (address 1C08h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	VB15EN	VB14EN	VB13EN	VB12EN	VB11EN	VB10EN	VB9EN	VB8EN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	7	6	5	4	3	2	1	0
Symbol	VB7EN	VB6EN	VB5EN	VB4EN	VB3EN	VB2EN	VB1EN	VB0EN
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 535. SECM_VB_CFG0 register - balance voltage measurement enable (address 1C08h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	VB15EN	R/W		Enable measurement of balance voltage 15. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
14	VB14EN	R/W		Enable measurement of balance voltage 14. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
13	VB13EN	R/W		Enable measurement of balance voltage 13. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
12	VB12EN	R/W		Enable measurement of balance voltage 12. Changes to this bit during active measurement can lead to undefined results.

Table 535. SECM_VB_CFG0 register - balance voltage measurement enable (address 1C08h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
11	VB11EN	R/W		Enable measurement of balance voltage 11. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
10	VB10EN	R/W		Enable measurement of balance voltage 10. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
9	VB9EN	R/W		Enable measurement of balance voltage 9. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
8	VB8EN	R/W		Enable measurement of balance voltage 8. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
7	VB7EN	R/W		Enable measurement of balance voltage 7. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
6	VB6EN	R/W		Enable measurement of balance voltage 6. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
5	VB5EN	R/W		Enable measurement of balance voltage 5. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
4	VB4EN	R/W		Enable measurement of balance voltage 4. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
3	VB3EN	R/W		Enable measurement of balance voltage 3. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
2	VB2EN	R/W		Enable measurement of balance voltage 2. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled

Table 535. SECM_VB_CFG0 register - balance voltage measurement enable (address 1C08h)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
1	VB1EN	R/W		Enable measurement of balance voltage 1. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
0	VB0EN	R/W		Enable measurement of balance voltage 0. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled

12.1.244 SECM_VB_CFG1 register

Balance voltage measurement enable

Table 536. SECM_VB_CFG1 register - balance voltage measurement enable (address 1C09h) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						VB17EN	VB16EN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R/W	R/W

Table 537. SECM_VB_CFG1 register - balance voltage measurement enable (address 1C09h)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VB17EN	R/W		Enable measurement of balance voltage 17. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled
0	VB16EN	R/W		Enable measurement of balance voltage 16. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled

12.1.245 SECM_AIN_CFG register

Measurement enables for extra channel

Table 538. SECM_AIN_CFG register - measurement enables for extra channel (address 1C0Ah) bit allocation

Bit	15	14	13	12	11	10	9	8

Table 538. SECM_AIN_CFG register - measurement enables for extra channel (address 1C0Ah) bit allocation*...continued*

Symbol	RATIOMETRICAIN7		RATIOMETRICAIN6		RATIOMETRICAIN5		RATIOMETRICAIN4	
Reset	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	FLTAPPINV	reserved			AIN7EN	AIN6EN	AIN5EN	AIN4EN
Reset	1	0	0	0	0	0	0	0
Access	R/W	R	R	R	R/W	R/W	R/W	R/W

Table 539. SECM_AIN_CFG register - measurement enables for extra channel (address 1C0Ah)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:14	RATIOMETRICAIN7	R/W		Reference selection for AIN7. Changes to these bits during active measurement can lead to undefined results.
			00*	SECVREF (read-write) Absolute (SECVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
13:12	RATIOMETRICAIN6	R/W		Reference selection for AIN6. Changes to these bits during active measurement can lead to undefined results.
			00*	SECVREF (read-write) Absolute (SECVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
11:10	RATIOMETRICAIN5	R/W		Reference selection for AIN5. Changes to these bits during active measurement can lead to undefined results.
			00*	SECVREF (read-write) Absolute (SECVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
9:8	RATIOMETRICAIN4	R/W		Reference selection for AIN4. Changes to these bits during active measurement can lead to undefined results.
			00*	SECVREF (read-write) Absolute (SECVREF)
			01	RESERVED (read-write) reserved
			10	VAUX (read-write) Ratiometric (VAUX)
			11	VDDC (read-write) Ratiometric (VDDC)
7	FLTAPPINV	R/W		Invalidate AINx application results in case of fault.
			0	VALID (read-write) AINx application results are not invalidated in case of a fault
			1*	INVALID (read-write) AINx application results are invalidated when a fault is detected.
6:4	reserved	R	0h	This read-only field is reserved and always has the value 0.

Table 539. SECM_AIN_CFG register - measurement enables for extra channel (address 1C0Ah)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
3	AIN7EN	R/W		Enable measurement of AIN7. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.
2	AIN6EN	R/W		Enable measurement of AIN6. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.
1	AIN5EN	R/W		Enable measurement of AIN5. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.
0	AIN4EN	R/W		Enable measurement of AIN4. Changes to this bit during active measurement can lead to undefined results.
			0*	DISABLED (read-write) Measurement disabled
			1	ENABLED (read-write) Measurement enabled. If a GPIO output function is enabled on this GPIO, the GPIO output is automatically disabled. This is not reflected in the GPIO output enable bit.

12.1.246 SECM_AIN_OL_CFG register

AINx open-load detection enable

Table 540. SECM_AIN_OL_CFG register - AINx open-load detection enable (address 1C0Bh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved				AIN7EN	AIN6EN	AIN5EN	AIN4EN
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R/W	R/W	R/W	R/W

Table 541. SECM_AIN_OL_CFG register - AINx open-load detection enable (address 1C0Bh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:4	reserved	R	0h	This read-only field is reserved and always has the value 0.
3	AIN7EN	R/W		open-load detection circuit for AIN7
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.
2	AIN6EN	R/W		open-load detection circuit for AIN6
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.
1	AIN5EN	R/W		open-load detection circuit for AIN5
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.
0	AIN4EN	R/W		open-load detection circuit for AIN4
			0*	DISABLED (read-write) Disable the open-load detection circuit.
			1	ENABLED (read-write) Enable the open-load detection circuit.

12.1.247 SECM_VBUF_CFG register

Voltage buffer enable

Table 542. SECM_VBUF_CFG register - voltage buffer enable (address 1C0Ch) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	reserved							
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Symbol	reserved						VDDCEN	VAUXEN
Reset	0	0	0	0	0	0	1	1
Access	R	R	R	R	R	R	R/W	R/W

Table 543. SECM_VBUF_CFG register - voltage buffer enable (address 1C0Ch)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15:2	reserved	R	0h	This read-only field is reserved and always has the value 0.
1	VDDCEN	R/W		Enable the voltage buffer for secondary VDDC measurement.
			0	DISABLED (read-write) Voltage buffer for VDDC is disabled.
			1*	ENABLED (read-write) Voltage buffer for VDDC is enabled.

Table 543. SECM_VBUF_CFG register - voltage buffer enable (address 1C0Ch)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
0	VAUXEN	R/W		Enable the voltage buffer for secondary VAUX measurement.
			0	DISABLED (read-write) Voltage buffer for VAUX is disabled.
			1*	ENABLED (read-write) Voltage buffer for VAUX is enabled.

12.1.248 SECM_CAL_CRC register

CRC over calibration data

Table 544. SECM_CAL_CRC register - CRC over calibration data (address 1C20h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CRC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 545. SECM_CAL_CRC register - CRC over calibration data (address 1C20h)

Bit	Symbol	Access	Value	Description
15:0	CRC	R/W	0h	CRC over calibration data. The CRC calculation runs automatically every time when a synchronous measurement cycle is started and when the calibration data is read from the NVM.
			BEEFh	CALIBCRC (read-write) The expected value of the calibration CRC.

12.1.249 SECM_CFG_CRC register

CRC over configuration values

Table 546. SECM_CFG_CRC register - CRC over configuration values (address 1C21h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	CRC															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 547. SECM_CFG_CRC register - CRC over configuration values (address 1C21h)

Bit	Symbol	Access	Value	Description
15:0	CRC	R	0h	This CRC value is recalculated with any transition into Active mode, with any write to a covered register and with any read to this register. The updated CRC value is available latest 100 µs after the last write. The CRC value is application specific and must be re-calculated by the MCU. The used polynomial is: D175h (+1) = $X^{16} + X^{15} + X^{13} + X^{9} + X^{7} + X^{6} + X^{5} + X^{3} + X^{1} + 1$. Following registers are included: SECM_CFG, SECM_PER_CTRL, SECM_VB_CFG0, SECM_VB_CFG1, SECM_AIN_CFG, SECM_VBUF_CFG.

12.1.250 SECM_MEAS_STAT register

Measurement status

Table 548. SECM_MEAS_STAT register - measurement status (address 1C3Eh) bit allocation

Bit	15	14	13	12	11	10	9	8
Symbol	MEASFLT	COMFLT	ANAFLT	SUPPLYFLT	reserved	FASTVBRDY	SYNCRDY	PERRDY
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R
Bit	7	6	5	4	3	2	1	0
Symbol	reserved				APPRDYAIN7	APPRDYAIN6	APPRDYAIN5	APPRDYAIN4
Reset	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R

Table 549. SECM_MEAS_STAT register - measurement status (address 1C3Eh)

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
15	MEASFLT	R		Measurement fault status
			0*	NO_FLT (read) No measurement fault detected
			1	FAULT (read) Measurement fault detected
14	COMFLT	R		Communication fault status
			0*	NO_FLT (read) No communication fault detected
			1	FAULT (read) Communication fault detected.
13	ANAFLT	R		Analog fault status
			0*	NO_FLT (read) No analog fault detected
			1	FAULT (read) Analog fault detected
12	SUPPLYFLT	R		Internal/external supply fault status
			0*	NO_FLT (read) No supply error detected
			1	FAULT (read) Supply error detected
11	reserved	R	0h	This read-only field is reserved and always has the value 0.
10	FASTVBRDY	R		Fast VB measurement data is ready for readout, the bit is cleared by a read to any register in the range SECM_SYNC_VB0 to SECM_SYNC_VB17 or if a synchronous measurement cycle is completed.
			0*	NO_DATA (read) No data available
			1	DATA (read) Sample data available.
9	SYNCRDY	R		Synchronous measurement data is ready for readout, the bit is cleared by a read to any register in the range SECM_SYNC_VB0 to SECM_SYNC_VB17 or if a fast VB measurement cycle is completed.
			0*	NO_DATA (read) No data available
			1	DATA (read) Sample data available.
8	PERRDY	R		New periodic result data has been created (depending on the periodic update mode, they might need to be requested), the bit is cleared by a read to any register in the range SECM_PER_AIN4 to SECM_PER_NPNISENSE if SECM_PER_CTRL.

Table 549. SECM_MEAS_STAT register - measurement status (address 1C3Eh)*...continued*

*Legend: * reset value*

Bit	Symbol	Access	Value	Description
				PERCTRL is set to AUTO. If SECM_PER_CTRL.PERCTRL is set to ONCE, a write to SECM_PER_CTRL.PERCTRL == ONCE clears it.
			0*	NO_DATA (read) No data available
			1	DATA (read) Sample data available.
7:4	reserved	R	0h	This read-only field is reserved and always has the value 0.
3	APPRDYAIN7	R		A new AIN7 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
2	APPRDYAIN6	R		A new AIN6 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
1	APPRDYAIN5	R		A new AIN5 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).
0	APPRDYAIN4	R		A new AIN4 application result can be requested / captured.
			0*	NO_DATA (read) No data available (<16 sample)
			1	DATA (read) Data can be captured (>=16 samples are captured).

12.1.251 SECM_APP_AIN4 register

Application measurement result AIN4

Table 550. SECM_APP_AIN4 register - application measurement result AIN4 (address 1C53h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 551. SECM_APP_AIN4 register - application measurement result AIN4 (address 1C53h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN4 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.252 SECM_APP_AIN5 register

Application measurement result AIN5

Table 552. SECM_APP_AIN5 register - application measurement result AIN5 (address 1C54h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 552. SECM_APP_AIN5 register - application measurement result AIN5 (address 1C54h) bit allocation*...continued*

Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 553. SECM_APP_AIN5 register - application measurement result AIN5 (address 1C54h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN5 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.253 SECM_APP_AIN6 register

Application measurement result AIN6

Table 554. SECM_APP_AIN6 register - application measurement result AIN6 (address 1C55h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 555. SECM_APP_AIN6 register - application measurement result AIN6 (address 1C55h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN6 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.254 SECM_APP_AIN7 register

Application measurement result AIN7

Table 556. SECM_APP_AIN7 register - application measurement result AIN7 (address 1C56h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 557. SECM_APP_AIN7 register - application measurement result AIN7 (address 1C56h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN7 at the last application capture as signed integer. A read to this register sets its content to invalid (8000h).

12.1.255 SECM_PER_NUM register

Measurement period number of the secondary periodic results

Table 558. SECM_PER_NUM register - measurement period number of the secondary periodic results (address 1C5Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	NUM															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 559. SECM_PER_NUM register - measurement period number of the secondary periodic results (address 1C5Fh)

Bit	Symbol	Access	Value	Description
15:0	NUM	R	0h	Number of the periodic cycle in which the secondary periodic results have been created. The value is incremented for each periodic cycle executed. The counting wraps at its limit.

12.1.256 SECM_PER_AIN4 register

Periodic measurement result AIN4

Table 560. SECM_PER_AIN4 register - periodic measurement result AIN4 (address 1C73h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 561. SECM_PER_AIN4 register - periodic measurement result AIN4 (address 1C73h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN4 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.257 SECM_PER_AIN5 register

Periodic measurement result AIN5

Table 562. SECM_PER_AIN5 register - periodic measurement result AIN5 (address 1C74h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 563. SECM_PER_AIN5 register - periodic measurement result AIN5 (address 1C74h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN5 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.258 SECM_PER_AIN6 register

Periodic measurement result AIN6

Table 564. SECM_PER_AIN6 register - periodic measurement result AIN6 (address 1C75h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 565. SECM_PER_AIN6 register - periodic measurement result AIN6 (address 1C75h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN6 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.259 SECM_PER_AIN7 register

Periodic measurement result AIN7

Table 566. SECM_PER_AIN7 register - periodic measurement result AIN7 (address 1C76h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 567. SECM_PER_AIN7 register - periodic measurement result AIN7 (address 1C76h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of AIN7 of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.260 SECM_PER_SECTEMP register

Periodic measurement result secondary device temperature

Table 568. SECM_PER_SECTEMP register - periodic measurement result secondary device temperature (address 1C77h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 569. SECM_PER_SECTEMP register - periodic measurement result secondary device temperature (address 1C77h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured temperature of secondary temperature sensor of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.261 SECM_PER_PRMVREF register

Periodic measurement result primary voltage reference

Table 570. SECM_PER_PRMVREF register - periodic measurement result primary voltage reference (address 1C78h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 571. SECM_PER_PRMVREF register - periodic measurement result primary voltage reference (address 1C78h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of the primary voltage reference of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.262 SECM_PER_VAUX register

Periodic measurement result auxiliary supply voltage

Table 572. SECM_PER_VAUX register - periodic measurement result auxiliary supply voltage (address 1C79h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 573. SECM_PER_VAUX register - periodic measurement result auxiliary supply voltage (address 1C79h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of VAUX of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.263 SECM_PER_VBAT register

Periodic measurement result VBAT

Table 574. SECM_PER_VBAT register - periodic measurement result VBAT (address 1C7Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

Table 574. SECM_PER_VBAT register - periodic measurement result VBAT (address 1C7Ah) bit allocation*...continued*

Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 575. SECM_PER_VBAT register - periodic measurement result VBAT (address 1C7Ah)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of VBAT of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.264 SECM_PER_VDDA register

Periodic measurement result VDDA

Table 576. SECM_PER_VDDA register - periodic measurement result VDDA (address 1C7Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 577. SECM_PER_VDDA register - periodic measurement result VDDA (address 1C7Bh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of VDDA of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.265 SECM_PER_VDDC register

Periodic measurement result VDDC

Table 578. SECM_PER_VDDC register - periodic measurement result VDDC (address 1C7Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 579. SECM_PER_VDDC register - periodic measurement result VDDC (address 1C7Ch)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of VDDC of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.266 SECM_PER_NPNISENSE register

Periodic measurement result NPN current sensor

Table 580. SECM_PER_NPNISENSE register - periodic measurement result NPN current sensor (address 1C7Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 581. SECM_PER_NPNISENSE register - periodic measurement result NPN current sensor (address 1C7Eh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of NPN current sensor of the periodic cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.267 SECM_SYNC_NUM register

Measurement number of the secondary synchronous results

Table 582. SECM_SYNC_NUM register - measurement number of the secondary synchronous results (address 1C7Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	NUM															
Reset	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 583. SECM_SYNC_NUM register - measurement number of the secondary synchronous results (address 1C7Fh)

Bit	Symbol	Access	Value	Description
15:0	NUM	R	0h	Number of the synchronous cycle in which the secondary results have been created. The value is incremented for each synchronous cycle executed. The counting wraps at its limit. The value is not incremented for FASTVB cycle.

12.1.268 SECM_SYNC_VB0 register

Synchronous measurement result from balancing pins cell 0.

Table 584. SECM_SYNC_VB0 register - synchronous measurement result from balancing pins cell 0. (address 1C80h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 585. SECM_SYNC_VB0 register - synchronous measurement result from balancing pins cell 0. (address 1C80h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 0 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.269 SECM_SYNC_VB1 register

Synchronous measurement result from balancing pins cell 1

Table 586. SECM_SYNC_VB1 register - synchronous measurement result from balancing pins cell 1 (address 1C81h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 587. SECM_SYNC_VB1 register - synchronous measurement result from balancing pins cell 1 (address 1C81h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 1 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.270 SECM_SYNC_VB2 register

Synchronous measurement result from balancing pins cell 2

Table 588. SECM_SYNC_VB2 register - synchronous measurement result from balancing pins cell 2 (address 1C82h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 589. SECM_SYNC_VB2 register - synchronous measurement result from balancing pins cell 2 (address 1C82h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 2 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.271 SECM_SYNC_VB3 register

Synchronous measurement result from balancing pins cell 3

Table 590. SECM_SYNC_VB3 register - synchronous measurement result from balancing pins cell 3 (address 1C83h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 591. SECM_SYNC_VB3 register - synchronous measurement result from balancing pins cell 3 (address 1C83h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 3 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.272 SECM_SYNC_VB4 register

Synchronous measurement result from balancing pins cell 4

Table 592. SECM_SYNC_VB4 register - synchronous measurement result from balancing pins cell 4 (address 1C84h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 593. SECM_SYNC_VB4 register - synchronous measurement result from balancing pins cell 4 (address 1C84h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 4 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.273 SECM_SYNC_VB5 register

Synchronous measurement result from balancing pins cell 5

Table 594. SECM_SYNC_VB5 register - synchronous measurement result from balancing pins cell 5 (address 1C85h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 595. SECM_SYNC_VB5 register - synchronous measurement result from balancing pins cell 5 (address 1C85h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 5 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.274 SECM_SYNC_VB6 register

Synchronous measurement result from balancing pins cell 6

Table 596. SECM_SYNC_VB6 register - synchronous measurement result from balancing pins cell 6 (address 1C86h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 597. SECM_SYNC_VB6 register - synchronous measurement result from balancing pins cell 6 (address 1C86h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 6 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.275 SECM_SYNC_VB7 register

Synchronous measurement result from balancing pins cell 7

Table 598. SECM_SYNC_VB7 register - synchronous measurement result from balancing pins cell 7 (address 1C87h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 599. SECM_SYNC_VB7 register - synchronous measurement result from balancing pins cell 7 (address 1C87h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 7 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.276 SECM_SYNC_VB8 register

Synchronous measurement result from balancing pins cell 8

Table 600. SECM_SYNC_VB8 register - synchronous measurement result from balancing pins cell 8 (address 1C88h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 601. SECM_SYNC_VB8 register - synchronous measurement result from balancing pins cell 8 (address 1C88h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 8 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.277 SECM_SYNC_VB9 register

Synchronous measurement result from balancing pins cell 9

Table 602. SECM_SYNC_VB9 register - synchronous measurement result from balancing pins cell 9 (address 1C89h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 603. SECM_SYNC_VB9 register - synchronous measurement result from balancing pins cell 9 (address 1C89h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 9 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.278 SECM_SYNC_VB10 register

Synchronous measurement result from balancing pins cell 10

Table 604. SECM_SYNC_VB10 register - synchronous measurement result from balancing pins cell 10 (address 1C8Ah) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 605. SECM_SYNC_VB10 register - synchronous measurement result from balancing pins cell 10 (address 1C8Ah)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 10 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.279 SECM_SYNC_VB11 register

Synchronous measurement result from balancing pins cell 11

Table 606. SECM_SYNC_VB11 register - synchronous measurement result from balancing pins cell 11 (address 1C8Bh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 607. SECM_SYNC_VB11 register - synchronous measurement result from balancing pins cell 11 (address 1C8Bh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 11 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.280 SECM_SYNC_VB12 register

Synchronous measurement result from balancing pins cell 12

Table 608. SECM_SYNC_VB12 register - synchronous measurement result from balancing pins cell 12 (address 1C8Ch) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 609. SECM_SYNC_VB12 register - synchronous measurement result from balancing pins cell 12 (address 1C8Ch)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 12 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.281 SECM_SYNC_VB13 register

Synchronous measurement result from balancing pins cell 13

Table 610. SECM_SYNC_VB13 register - synchronous measurement result from balancing pins cell 13 (address 1C8Dh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 611. SECM_SYNC_VB13 register - synchronous measurement result from balancing pins cell 13 (address 1C8Dh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 13 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.282 SECM_SYNC_VB14 register

Synchronous measurement result from balancing pins cell 14

Table 612. SECM_SYNC_VB14 register - synchronous measurement result from balancing pins cell 14 (address 1C8Eh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 613. SECM_SYNC_VB14 register - synchronous measurement result from balancing pins cell 14 (address 1C8Eh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 14 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.283 SECM_SYNC_VB15 register

Synchronous measurement result from balancing pins cell 15

Table 614. SECM_SYNC_VB15 register - synchronous measurement result from balancing pins cell 15 (address 1C8Fh) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 615. SECM_SYNC_VB15 register - synchronous measurement result from balancing pins cell 15 (address 1C8Fh)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 15 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.284 SECM_SYNC_VB16 register

Synchronous measurement result from balancing pins cell 16

Table 616. SECM_SYNC_VB16 register - synchronous measurement result from balancing pins cell 16 (address 1C90h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Table 617. SECM_SYNC_VB16 register - synchronous measurement result from balancing pins cell 16 (address 1C90h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 16 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

12.1.285 SECM_SYNC_VB17 register

Synchronous measurement result from balancing pins cell 17

Table 618. SECM_SYNC_VB17 register - synchronous measurement result from balancing pins cell 17 (address 1C91h) bit allocation

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	VALUE															
Reset	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Access	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

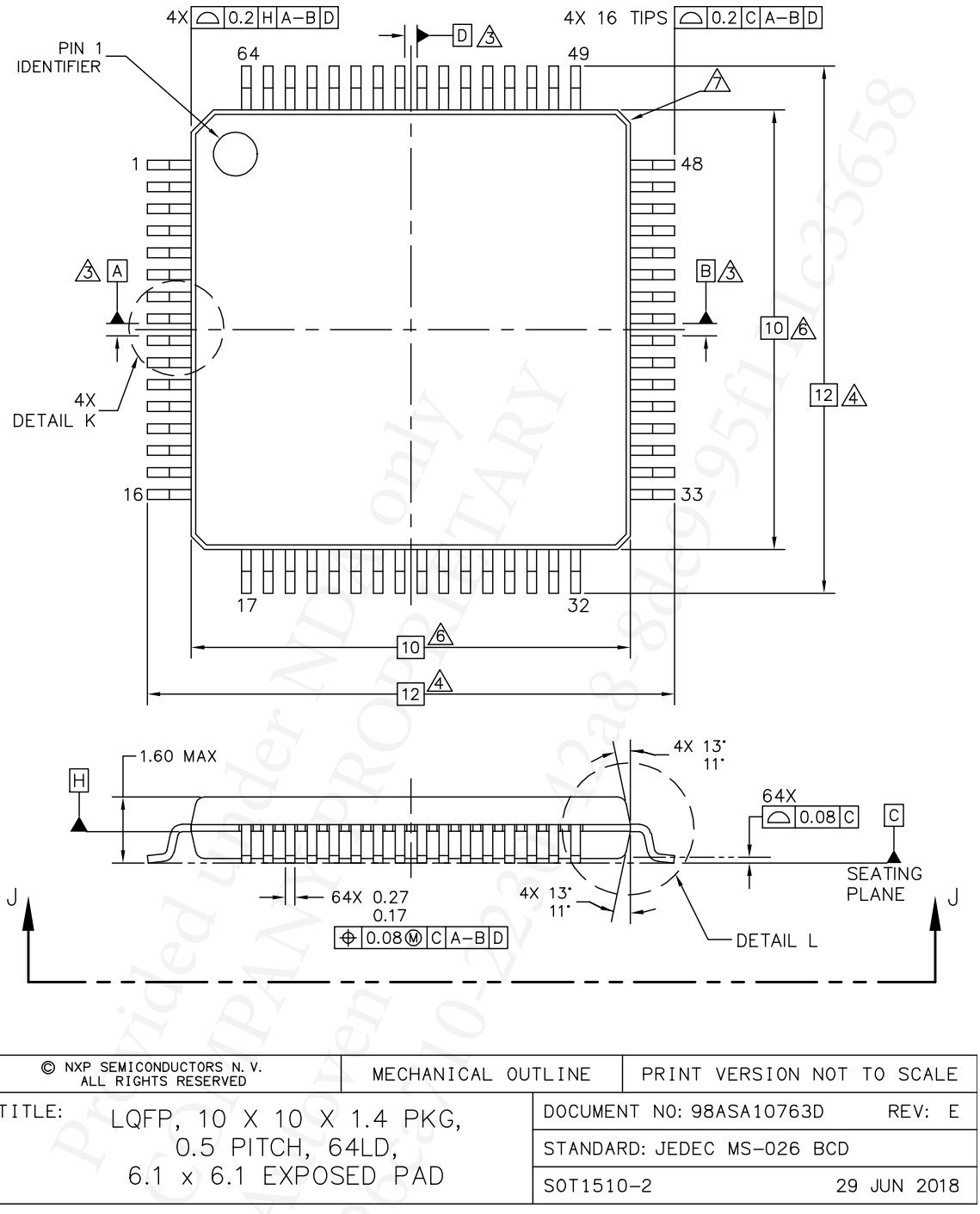
Table 619. SECM_SYNC_VB17 register - synchronous measurement result from balancing pins cell 17 (address 1C91h)

Bit	Symbol	Access	Value	Description
15:0	VALUE	R	8000h	Measured voltage of cell 17 of the last synchronous cycle as signed integer. A read to this register sets its content to invalid (8000h).

13 Functional safety - ISO 26262

The MC33774A is not developed in the context of a particular vehicle and therefore not for a specific item. In order to demonstrate compliance with ISO 26262, the device is treated as a safety element out of context (SEooC) in dependence on the guideline within ISO 26262-10. The IC is consequentially developed based on several assumptions at several integration levels. The assumptions derived from typical electronic control unit (ECU) applications (defining the intended use, context, and external interfaces) can be found in the safety manual. The safety manual also contains the assumed safety goals to be supported by this IC, where the highest integrity level to be supported is ASIL D.

14 Package outline



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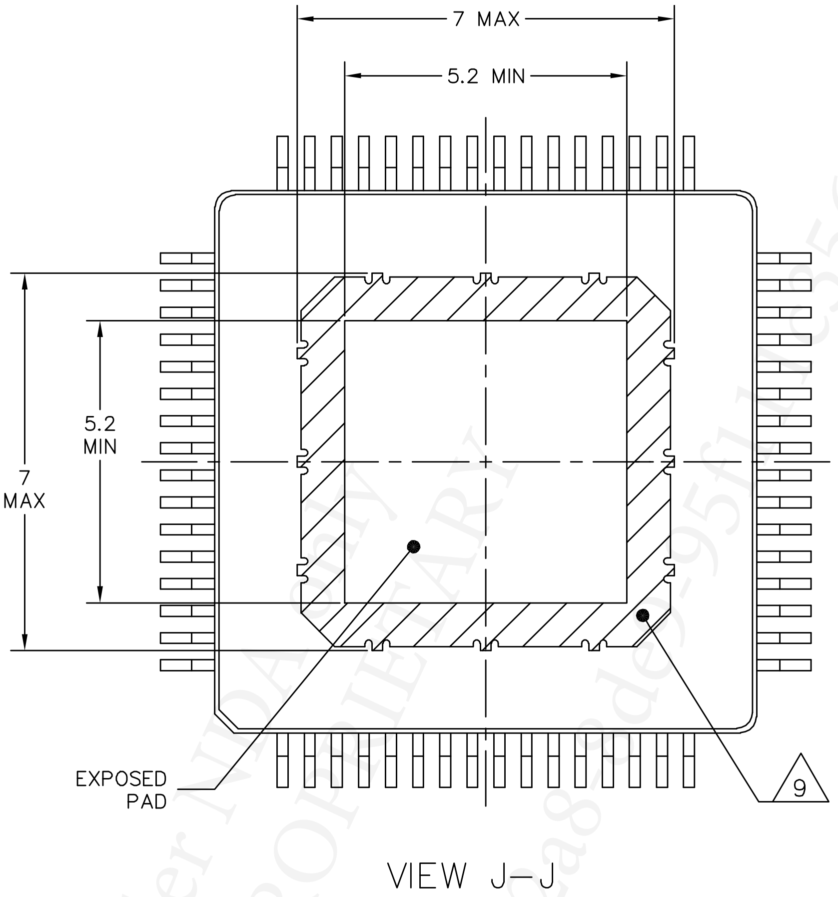
	STANDARD: JEDEC MS-026 BCD	
	SOT1510-2	29 JUN 2018

Figure 66. Package outline

14.1 Package mechanical dimensions



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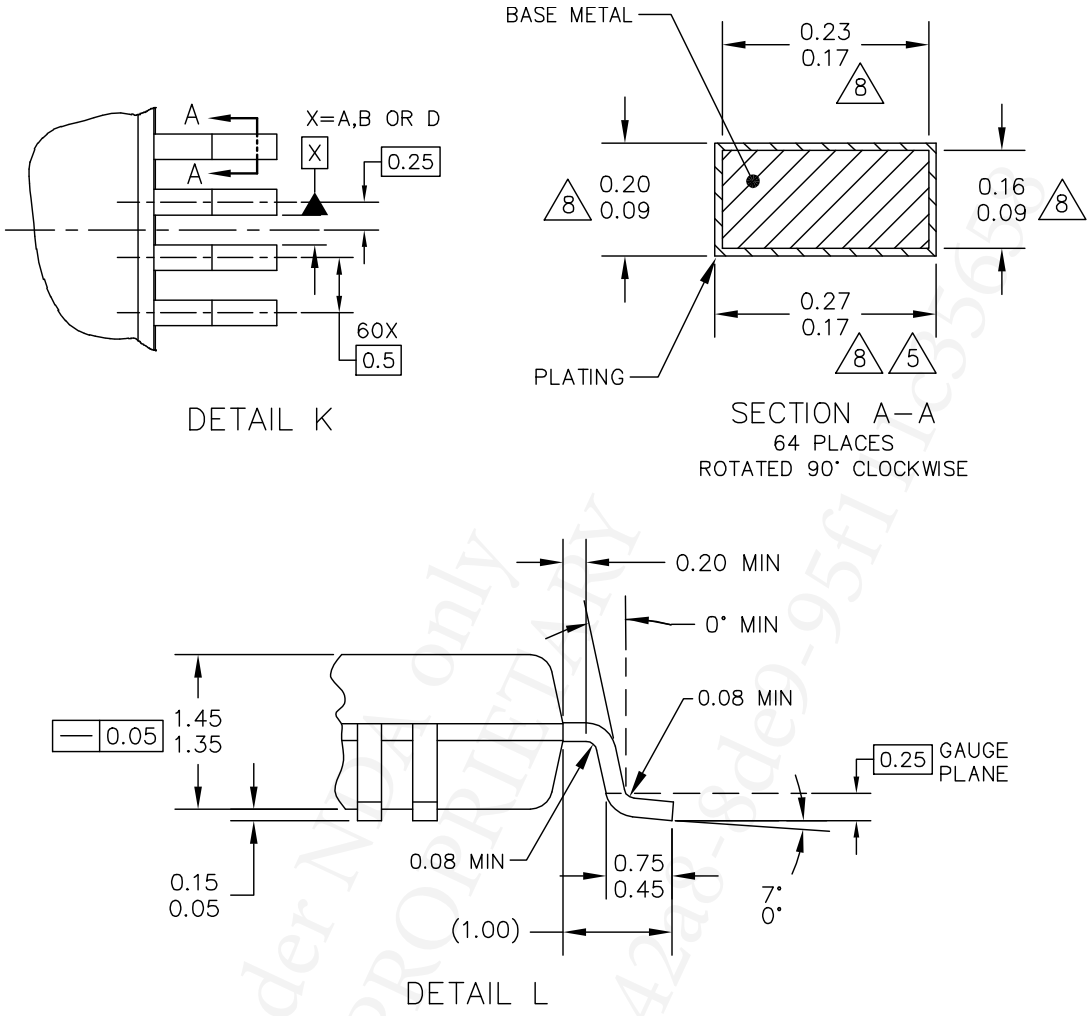
	STANDARD: JEDEC MS-026 BCD	
	SOT1510-2 29 JUN 2018	

Figure 67. Package mechanical dimensions 1



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	STANDARD: JEDEC MS-026 BCD	
	SOT1510-2	29 JUN 2018

Figure 68. Package mechanical dimensions 2

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M—1994.

3. DATUMS A, B AND D TO BE DETERMINED AT DATUM PLANE H.

4. DIMENSIONS TO BE DETERMINED AT SEATING PLANE C.

5. DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM DIMENSION BY MORE THAN 0.08 MM. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION 0.07 MM.

6. DIMENSIONS DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25 MM PER SIDE. DIMENSIONS ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.

7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.

8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 MM AND 0.25 MM FROM THE LEAD TIP.

9. HATCHED AREA REPRESENTS POSSIBLE MOLD FLASH ON EXPOSED PAD.

10. KEEP OUT ZONE REPRESENTS AREA ON PCB THAT MUST NOT HAVE ANY EXPOSED METAL (EG. TRACE/VIA) FOR PCB ROUTING DUE TO THE POSSIBILITY OF SHORTING TO TIE BAR/EXPOSED PAD.

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		STANDARD: JEDEC MS-026 BCD
		SOT1510-2 29 JUN 2018

Figure 69. Package mechanical dimensions 3

Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
MC33774A v.1	20230615	Product data sheet	—	MC33774A v.0.1
Modifications	Initial release			

15 Legal information

15.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.
[2] The term 'short data sheet' is explained in section "Definitions".
[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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Tables

Figures

Contents

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