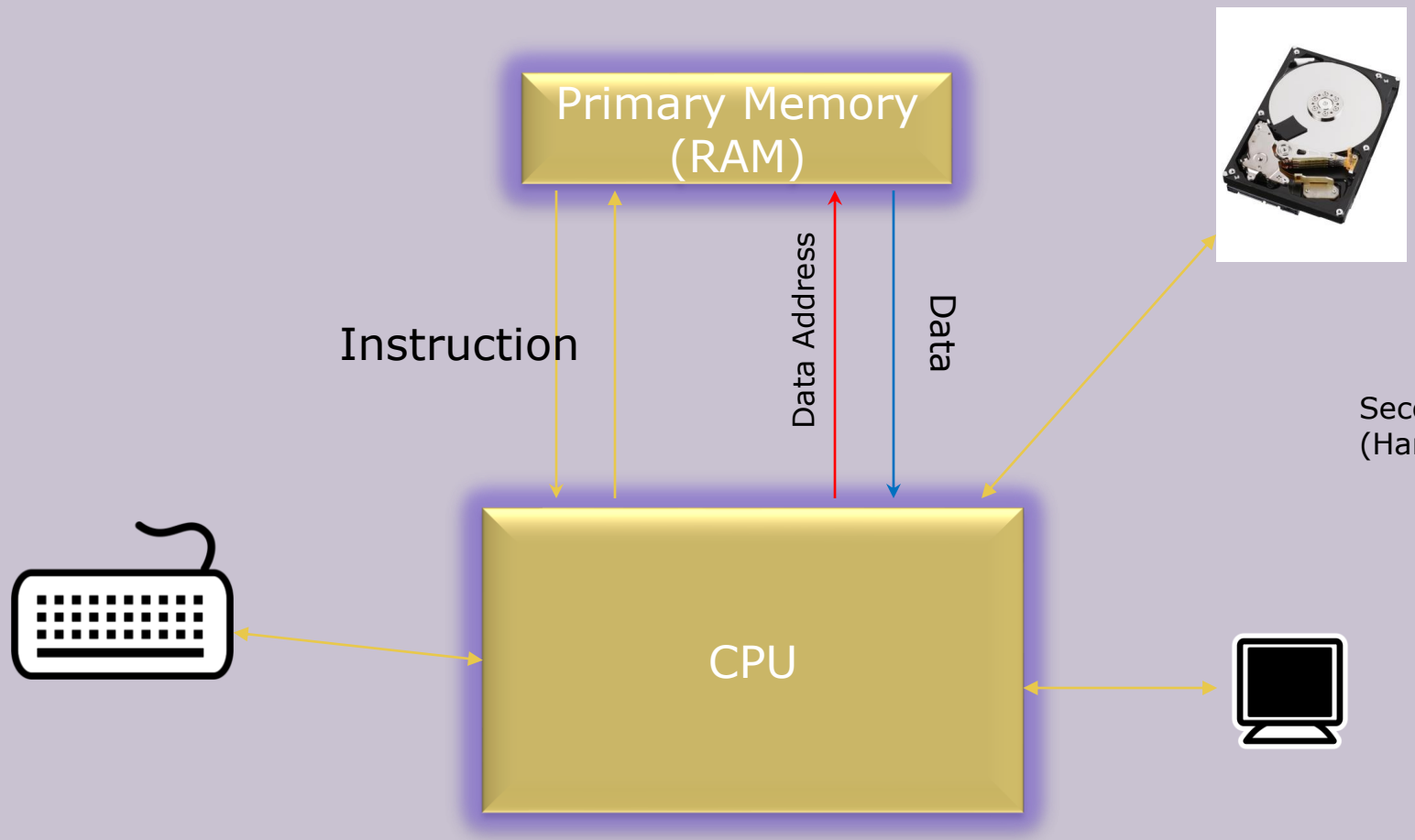
ARM Processor an Introduction

Girish S Kumar



Basic Computer Architecture

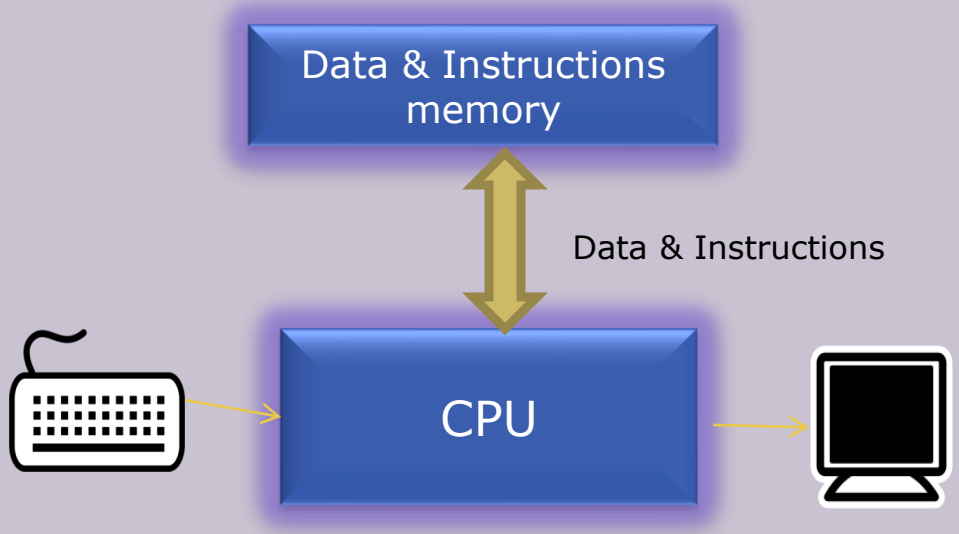
Two Popular Computer Architecture

- **Von Neumann Architecture**
- **Data** and **Instructions** are accessed by processor through the **SAME BUS**

- **Harvard Architecture**
- **Data** and **Instructions** are accessed by processor through **Separate Buses**

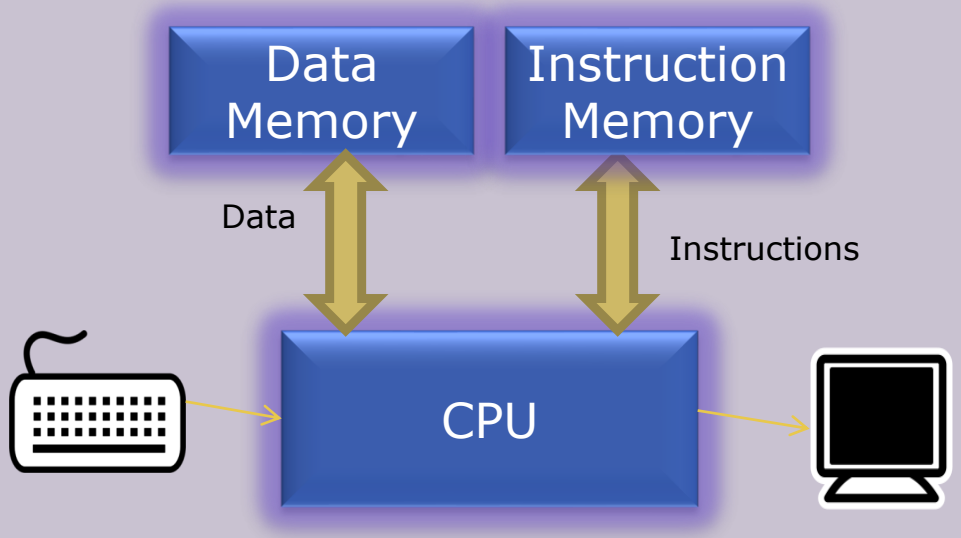
Von Neumann Architecture

Von Neuman architecture is also called Princeton Architecture was published in 1945 by Mathematician , physicist & Computer Scientist **John von Neumann**

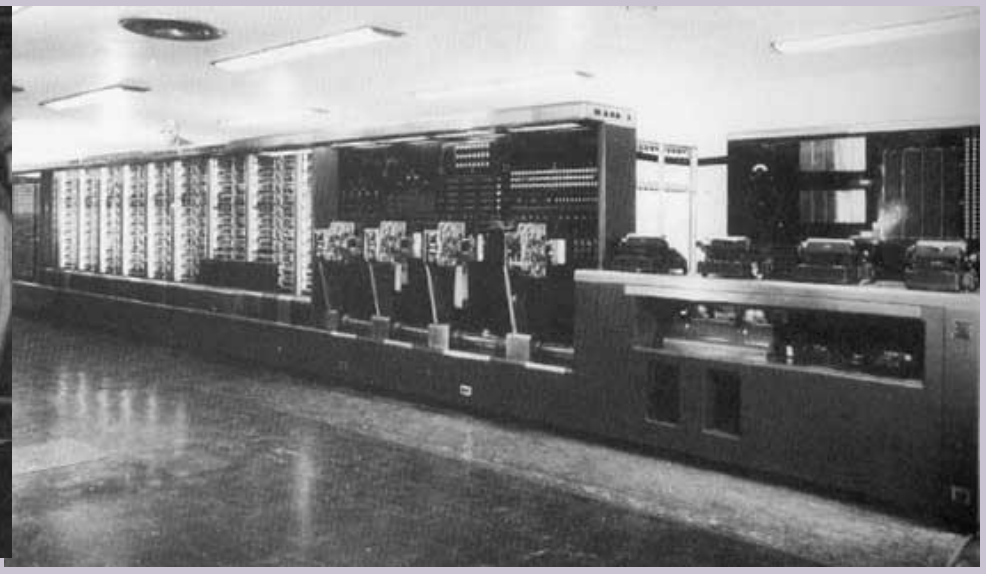


Harvard Architecture

The Harvard architecture is a computer architecture with physically separate storage and signal pathways for instructions and data. The term originated from the Harvard Mark I relay-based computer, which stored instructions on punched tape (24 bits wide) and data in electro-mechanical counters.

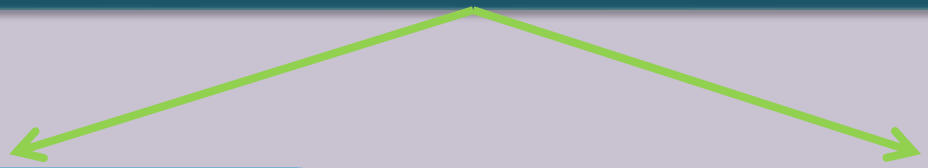


Some time in 1936 or possibly in early 1937, the Harvard physician Howard Aiken started to make plans about an automatic calculation machine. IBM agreed to construct for Harvard an automatic computing plant comprising machines for automatically carrying out a series of mathematical computations adaptable for the solution of problems in scientific fields, the machine was called *ASCC* (Automatic Sequence Controlled Calculator), but later on it became also known as *Harvard Mark I*.



Instruction Set Architecture

Instruction set architecture (ISA), is the part of the computer architecture related to programming, including the native data types, instructions, registers, addressing modes, memory architecture, interrupt and exception handling, and external I/O.



CISC

Where single instructions can execute several low-level operations (such as a load from memory, an arithmetic operation, and a memory store) or are capable of multi-step operations or addressing modes within single instructions.

Intel x86 Motorola 68K

RISC

A simplified instruction set provides higher performance also uses fewer cycles per instruction. Has specific instructions for data processing and moving data to and from memory

All ARM Series

HOW did ARM Series Evolved from early days

Acorn Computers Ltd.

Originally ARM Comes from Acorn Risk Machine

Acorn was Computer design company based out of UK who build one of the early personal computer called BBC Microcomputer based on a 8-Bit processor (1982)

By 1983, Engineers who build BBC Micro begin to think of next steps to build a successor to take their **product to next level**

What were the thoughts

Must deliver higher value that the existing BBC Micro

-**A 16 Bit CPU**
-With a good interrupt response may better than or comparable to that of 8-bit 6502, has to be identified ……..

MOS Technology, Inc. also known as CSG (Commodore Semiconductor Group), build 6502

What were the technical Challenges

- All the 16 bit Microprocessors available in the market were CISC based and much slower than what they were looking for.
- Instructions were complex and tool multiple cycles to complete
- They long Interrupt latencies compared to 6508
- It is not easy to build a new processor that can meet their expectations …….

They decided not to give up .. Instead they continued their search, started looking all the latest research happening, around world on processor design

They came across a processor designed by Post Graduate students at Berkley called RISC I.
It had very simple instructions and low interrupt latency
Students designed it in less than year

This was the starting point of ARM

Three main guiding principles they Based on they started the design was

- A Load and store Architecture
- Fixed length instructions (32 Bit length)
- 3 Address Instruction format

Two Address Instructions

```
MOV R1, R0
ADD R1, R2
MOV R2, R3
ADD R2,  R5
MUL R1, R2
MOV R3, R1
LDR R0 , =0xE000Ed88
STR  r1, r[0]
```

Three Address Instructions

```
ADD R1, R0, R1
ADD R2, R3,R4
MUL R5, R1, R2
```

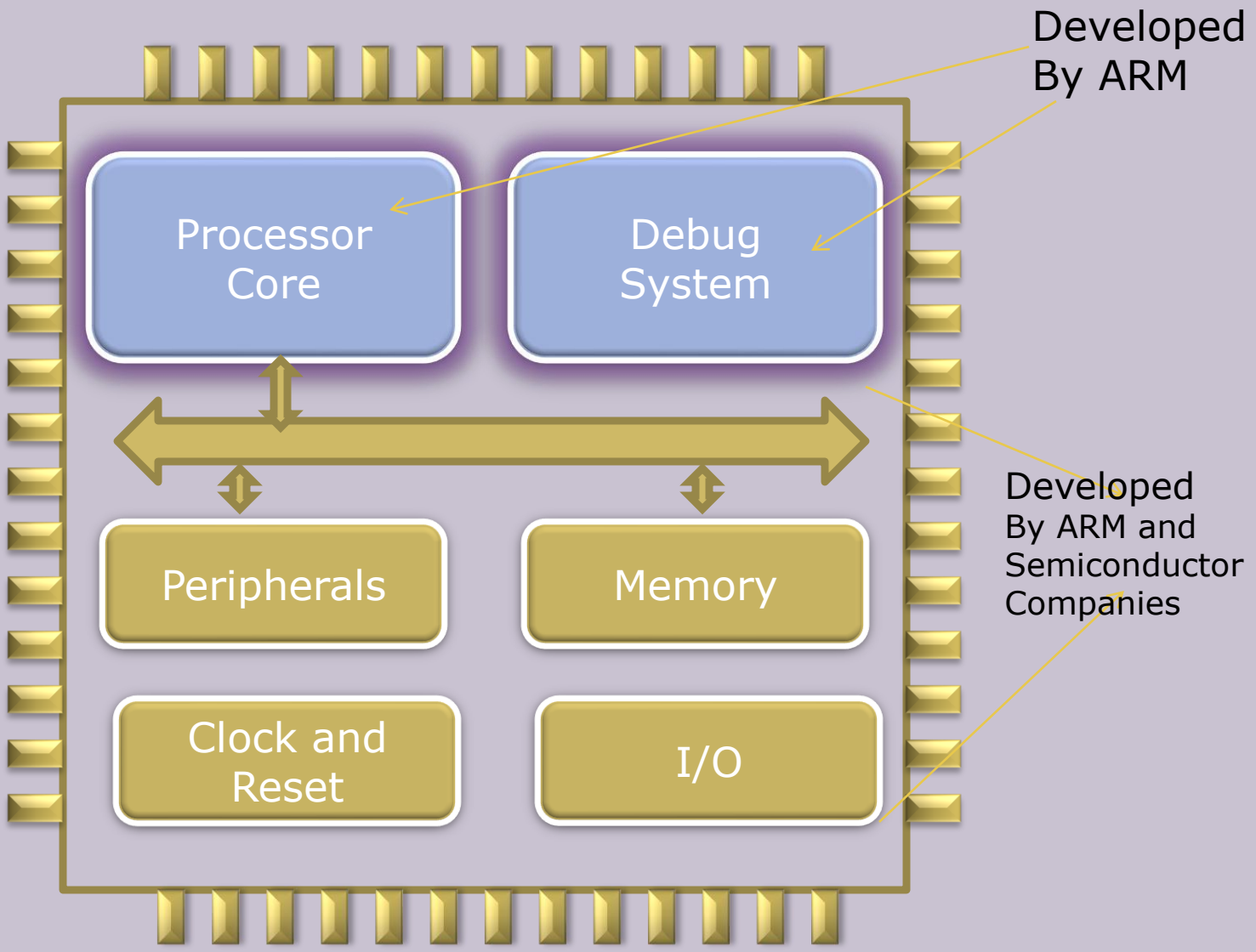
•1990 as Advanced RISC Machines Ltd.(ARM) , a joint venture of Apple Computer, Acorn Computer Group, and VLSI Technology.

•In 1991, ARM introduced the ARM6 processor family,
•and VLSI Technology became the initial licensee.

•Today around 2 billion ARM based processors are shipped every year

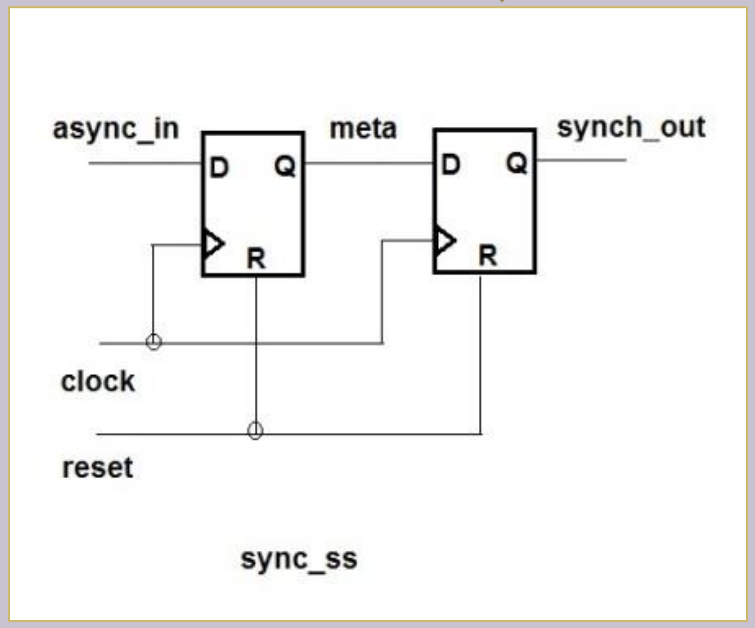
•ARM does not fabricate or sell any of these chips. Fabrication and selling by Semiconductor Companies who has partner with ARM. They design microprocessor, SoC and microcontrollers based on the design (IP) given by ARM

•This is called Intellectual property licensing – a very successful and practical model in developing processor designs (Synthesizable core)


Developed
By ARM
Processor
Core
Debug
System
Peripherals
Memory
Clock and
Reset
I/O
Developed
By ARM and
Semiconductor
Companies

```
module sync_ss (clk, async_in, reset);
input clk, async_in, reset;
output synch_out;
always @(posedge clk)
if (reset)
meta <= 1'b0;
sync_out <= 1'b0;
else
meta <= async_in;
sync_out <= meta;
endmodule
```

Verilog Synthesizer



What is a synthesizable core ?

In Electronics a **semiconductor intellectual property core**, **IP core**, or **IP block** is a reusable unit of logic, cell, or integrated circuit layout design that is the intellectual property of a company

IP cores may be licensed to another company or can be owned and used by the owner itself. The term is derived from the licensing of the patent and/or source code copyright that exist in the design.

IP cores are used as the building blocks within ASICs, FPGA or Soc designs

Soft IP	IP cores are typically offered as synthesizable RTL. Synthesizable cores are delivered in a hardware description language such as Verilog
Hard IP	Hard cores, by the nature of their low-level representation, offer better predictability of chip performance in terms of timing performance and area. Eg: Analog and mixed-signal logic are generally defined as a lower-level

IP Vendors

Processor	Memory I/F	D/A and A/D	On-chip SRAMs	Peripherals
Altera - Nios II	Actel	S3 Group	ARM	Eureka Technology
ARM - ARM	Altera	Cadence Design Systems	ChipStart	Digital Blocks, Inc.
Cambridge Consultants -	ARM	Cosmic Circuits	Dolphin Integration	
Cortus	Barco Silex	Dolphin Integration	M31 Technology	
CEVA, Inc. -	Cadence Design Systems (through acquisition of Denali Software)	Omniphy	MoSys, Inc.	
Digital Blocks, Inc. - 8051 with Standard and Configurable Peripherals	Eureka Technology		Synopsys	
Dolphin Integration - 8051, 80251	Faraday Technology		eSilicon	
EnSilica - eSi-RISC	Lattice Semiconductor			
Freescale and others - ColdFire				
IBM and others -				

What is a Debug Architecture ?

In modern ARM processors include hardware debugging facilities, allowing software debuggers to perform operations such as halting, stepping, and break pointing of code starting from reset. These facilities are built using JTAG support (**Joint Test Action Group** (**JTAG**) is an electronics industry association formed in 1985 for developing a method of verifying designs and testing printed circuit boards after manufacture
)

TheARM architecture defines basic debug facilities at an architectural level. These include breakpoints, watchpoints and instruction execution in a "Debug Mode

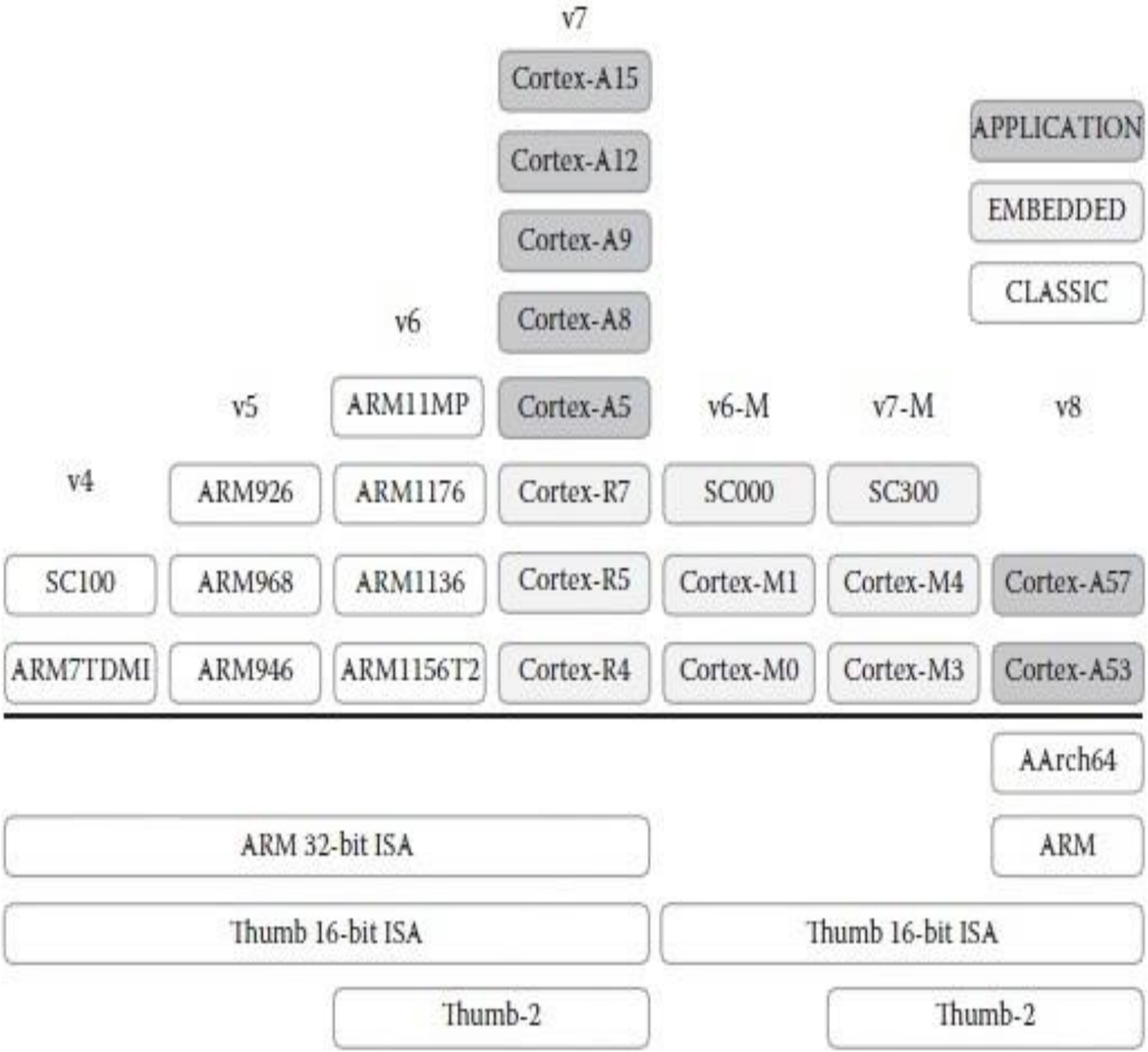
. Both "halt mode" and "monitor" mode debugging are supported. The actual transport mechanism used to access the debug facilities is not architecturally specified, but implementations generally include JTAG support.

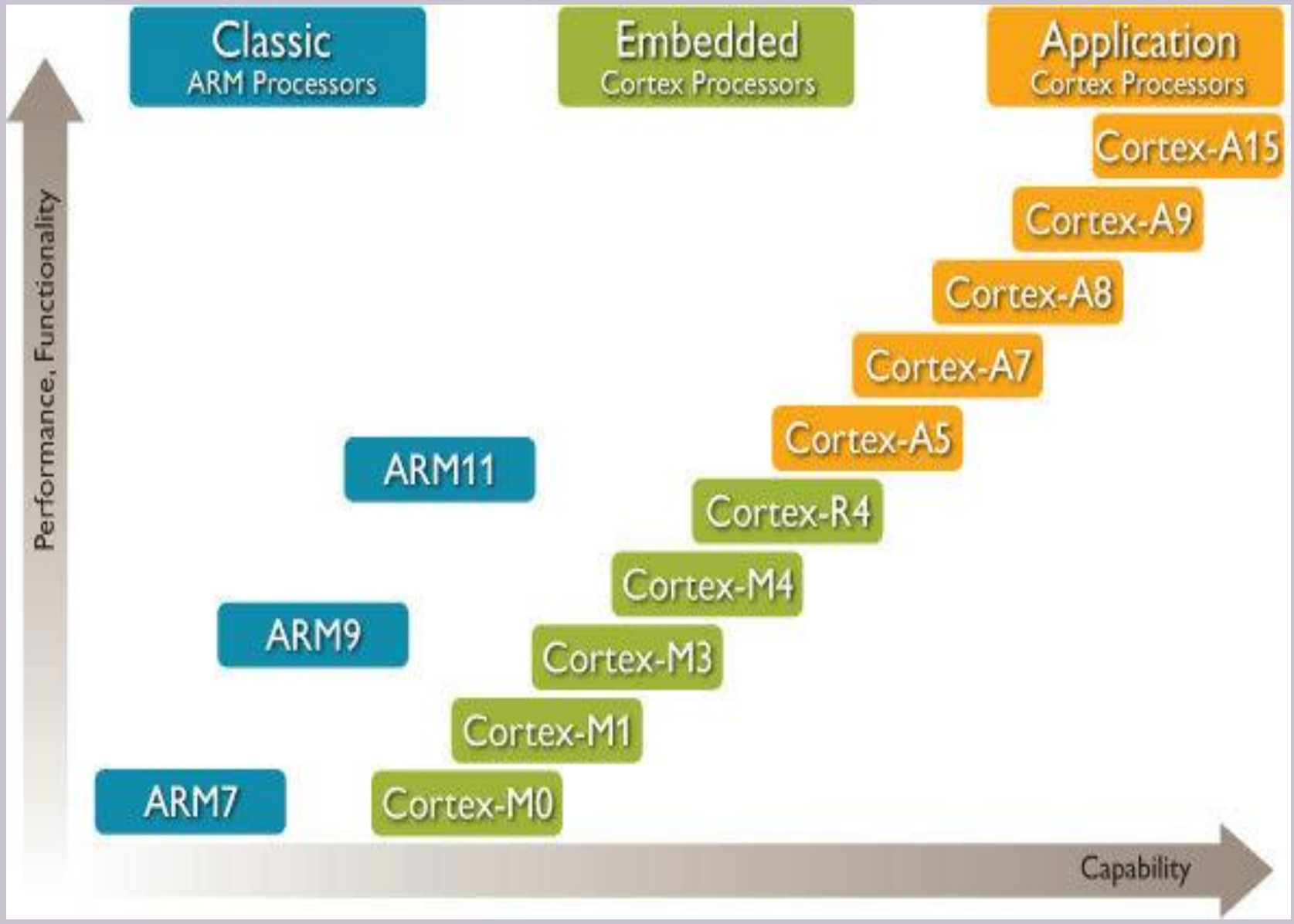
There is a separate ARM "CoreSight" debug architecture,

Due to the different requirements of embedded systems, ARM had split the processor cores into three distinct families,

where the end application now determines both the nature and the design of the processors, but all of them go by
the trade name of Cortex.

The Cortex-A, Cortex-R, and Cortex-M families continue to add new processors each year, generally based on performance requirements as well as the type of end application the cores are likely to execute


v7
Cortex-A15
Cortex-A12
Cortex-A9
Cortex-A8
Cortex-A5
Cortex-R7
Cortex-R5
Cortex-R4
APPLICATION
EMBEDDED
CLASSIC
v6
ARM11MP
ARM1176
ARM1136
ARM1156T2
v5
ARM926
ARM968
ARM946
v4
SC100
ARM7TDMI
v6-M
SC000
Cortex-M1
Cortex-M0
v7-M
SC300
Cortex-M4
Cortex-M3
v8
Cortex-A57
Cortex-A53
AArch64
ARM
ARM 32-bit ISA
Thumb 16-bit ISA
Thumb-2
Thumb 16-bit ISA
Thumb-2


Classic
ARM Processors
Embedded
Cortex Processors
Application
Cortex Processors
Performance, Functionality
Capability
Cortex-A15
Cortex-A9
Cortex-A8
Cortex-A7
Cortex-A5
Cortex-R4
Cortex-M4
Cortex-M3
Cortex-M1
Cortex-M0
ARM11
ARM9
ARM7

Series	Uses	Processor	Instruction Set Arch
Cortex – A	Feature phone (non smart phone)	CortexA5	ARMv7A
	Entertainment in a car (Video player + music)	Cortex A15 (TI OMAP)	ARMv7A
	Raspberry Pi-1	ARM1176JZF-S BCM 2835 (32 bit)	ARMv6A
	Raspberry Pi-2	Cortex-A7 cluster. Quad-core BCM 2836 (32 BIT)	ARMv7A
	Raspberry Pi-3	Cortex A53 Quad Core BCM2837 (64 bit)	ARMv8A

Series	Uses	Processor	Instruction Set Arch
Cortex –R	Smallest Cortex-R processor **Digi cams, Hard disk controllers wireless base band**	Cortex-R4 TI (RM4, TMS570)	Armv7-R
	Cloud storage, Industrial and automotive (Used in is commonly used in high-volume, deeply embedded SoC applications, such as **Industrial, automotive, Mass Storage**	Cortex-R5 Scaleo OLEA Texas Instruments RM57 Xilinx ZynqMP	Armv7-R
	High performance, high energy efficiency, real-time responsiveness, advanced features **Wireless Modem, Network Routers**, Industrial, Automative Storage	Cortex-R7	Armv7-R
	The Cortex-R8 processor has the highest performance in its class of real-time processors. All the the above uses with better performance	Cortex-R8	Armv7-R
	Extended safety features, high performance, and hard real-time determinism. Used for **Robotics, health care, building automation**, Industrial and automotive	Cortex-R52	Armv8-R

Designed for high performance hard real-time and safety critical applications.

Series	Uses	Processor	Instruction Set Arch
Cortex – M	All small embedded system controllers starting with home appliances to industrial control	Cortex-M0	ARMv6-M
		Cortex-M0+	
		Cortex-M1	
		Cortex-M3	ARMv7-M
		Cortex-M4	ARMv7E-M
		Cortex-M7	
		Cortex-M23	ARMv8-M
		Cortex-M33	

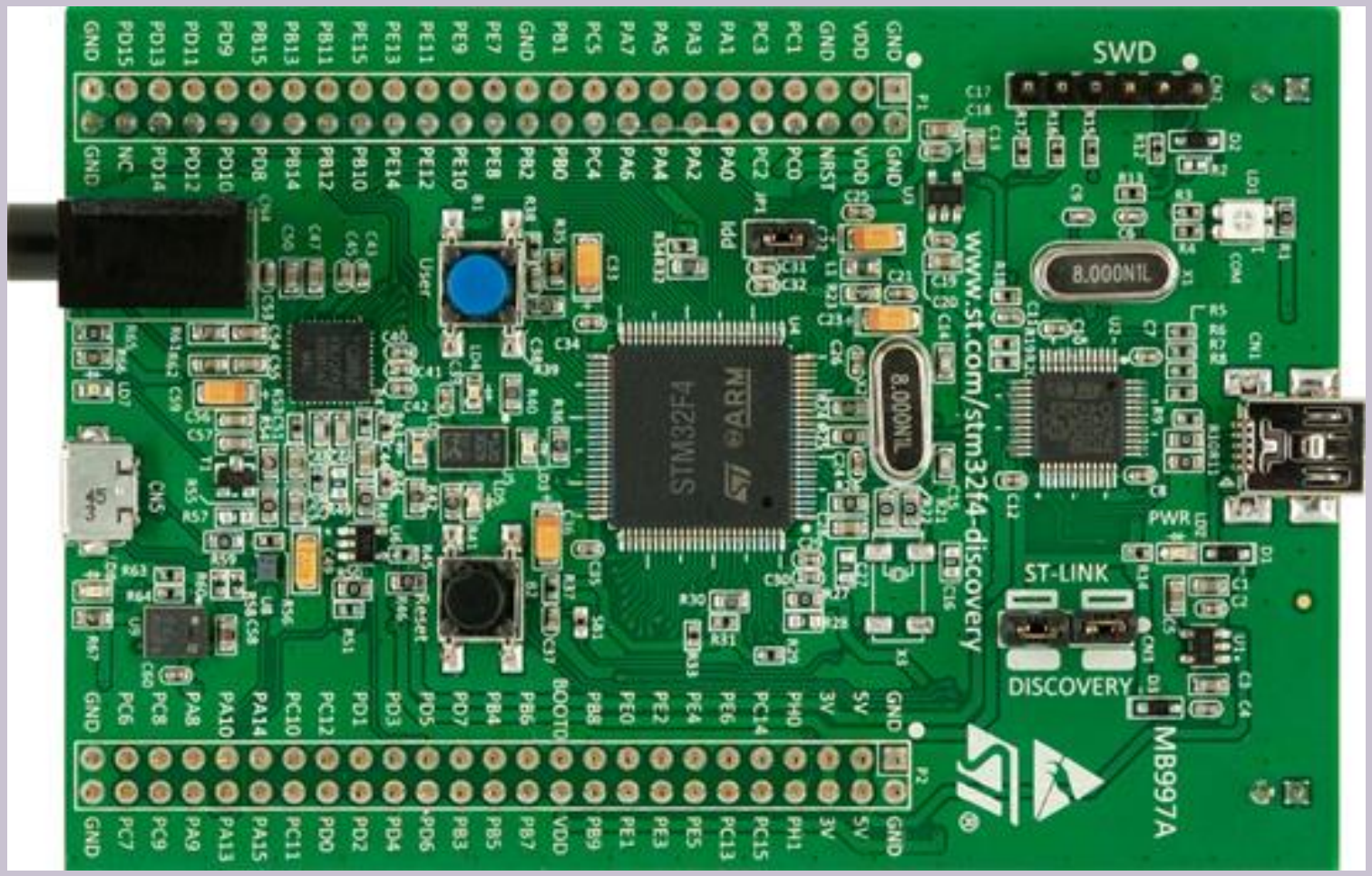
A **system on a chip** or **system on chip** (**SoC** or **SOC**) is an integrated circuit (**IC**) that integrates all components of a computer or other electronic system into a single chip. It may contain digital, analog, mixed-signal, and often radio-frequency functions—all on a single chip substrate. SoCs are very common in the mobile computing market because of their low power-consumption. A typical application is in the area of embedded systems.

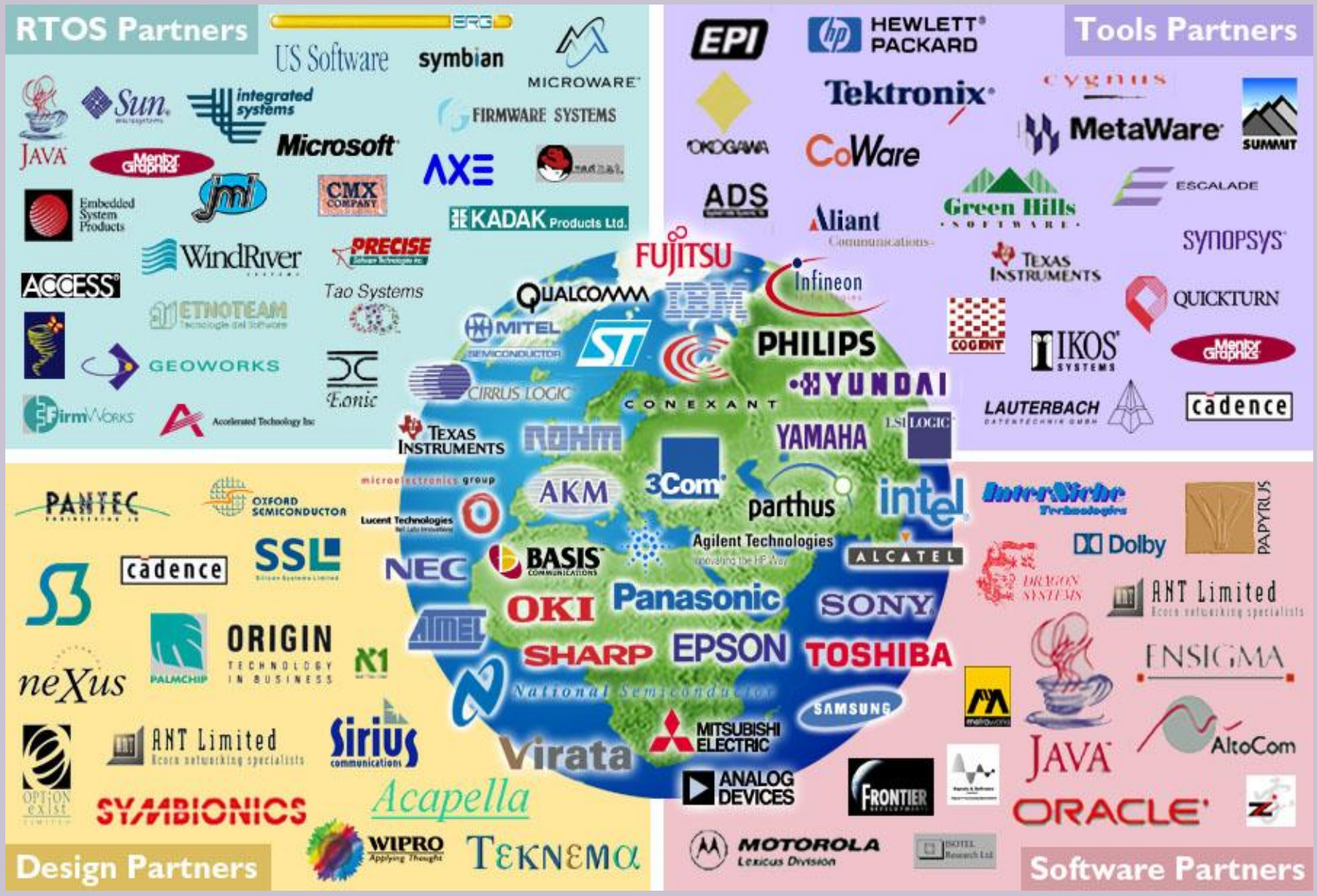
A typical SoC consists of:

A microcontroller, microprocessor or digital signal processor (DSP) core – multiprocessor SoCs (MPSoC) having more than one processor core
memory blocks including a selection of ROM, RAM, EEPROM and flash memory timing sources including oscillators and phase-locked loops peripherals including counter-timers, real-time timers and power-on reset generators external interfaces, including industry standards such as USB, FireWire, Ethernet, USART, SPI
analog interfaces including ADCs and DACs
voltage regulators and power management circuits

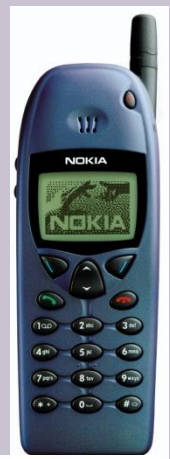
ARM SoC build by ST Microelectronics

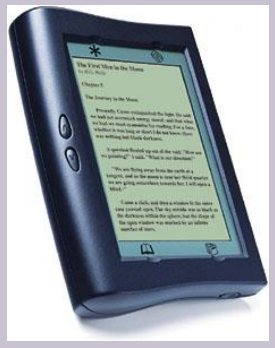
A computer build using STMF32VG704

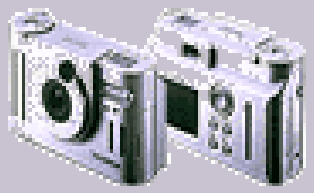



RTOS Partners
ERG
US Software
symbian
MICROWARE
Sun
integrated systems
FIRMWARE SYSTEMS
JAVA
Microsoft
Mentor Graphics
AXE
Embedded System Products
CMX COMPANY
KADAK Products Ltd.
WindRiver
PRECISE
ACCESS
Tao Systems
ETNOTEAM
GEOWORKS
Eonic
FirmWorks
Accelerated Technology Inc
Tools Partners
EPI
HEWLETT PACKARD
Tektronix
cygnus
MetaWare
SUMMIT
OMOGAMA
CoWare
ADS
Aliant Communications
Green Hills SOFTWARE
ESCALADE
SYNOPSYS
TEXAS INSTRUMENTS
QUICKTURN
COGENT
IKOS SYSTEMS
Mentor Graphics
LAUTERBACH DATENTECHNIK GMBH
cadence
FUJITSU
Infineon
QUALCOMM
IBM
MITEL SEMICONDUCTOR
ST
PHILIPS
CIRRUS LOGIC
HYUNDAI
CONEXANT
TEXAS INSTRUMENTS
ROHM
YAMAHA
LSI LOGIC
3Com
AKM
parthus
intel
microelectronics group
Lucent Technologies
Agilent Technologies
ALCATEL
NEC
BASIS COMMUNICATIONS
Panasonic
SONY
OKI
ATMEL
SHARP
EPSON
TOSHIBA
National Semiconductor
SAMSUNG
MITSUBISHI ELECTRIC
Virata
ANALOG DEVICES
FRONTIER
MOTOROLA Lexicus Division
Design Partners
PANTEC
OXFORD SEMICONDUCTOR
cadence
SSL
neXus
PALMCHIP
ORIGIN TECHNOLOGY IN BUSINESS
ANT Limited
Acorn networking specialists
Sirius communications
OPTION EXISE
SYNOPSYS
Acapella
WIPRO Applying Thought
TEKNEMA
Software Partners
InterSystems Technologies
Dolby
PAPYRUS
DRAGON SYSTEMS
ANT Limited
Acorn networking specialists
ENSIGMA
AltoCom
JAVA
ORACLE

ARM Powered Products







ARMv8 is the first architecture series where 64 Bit instruction sets are introduced

ARM v8 features High level

- ✓64-Bit pointer and registers
- ✓Fixed length (32bit) instructions
- ✓Load/store architecture
- ✓Little endian (big endian possible)
- ✓31 general purpose registers and zero register

New extensions provided with v8 arch

Jazelle is a Java hardware/software accelerator: "ARM Jazelle DBX (Direct Bytecode eXecution) technology for direct bytecode execution of Java". On Sofware side: Jazelle MobileVM is a complete JVM which is Multi-tasking, engineered to provide high performance multi-tasking in a very small memory footprint

Floating Point: for floating point operations

NEON: the ARM SIMD 128 bit (Single instruction, multiple data) engine and **DSP** the SIMD 32bit engine useful to make linear algebra operations

Cryptographic Extension is an extension of the SIMD support and operates on the vector register file. It provides instructions for the acceleration of encryption and decryption to support the following: AES, SHA1, SHA2-256.

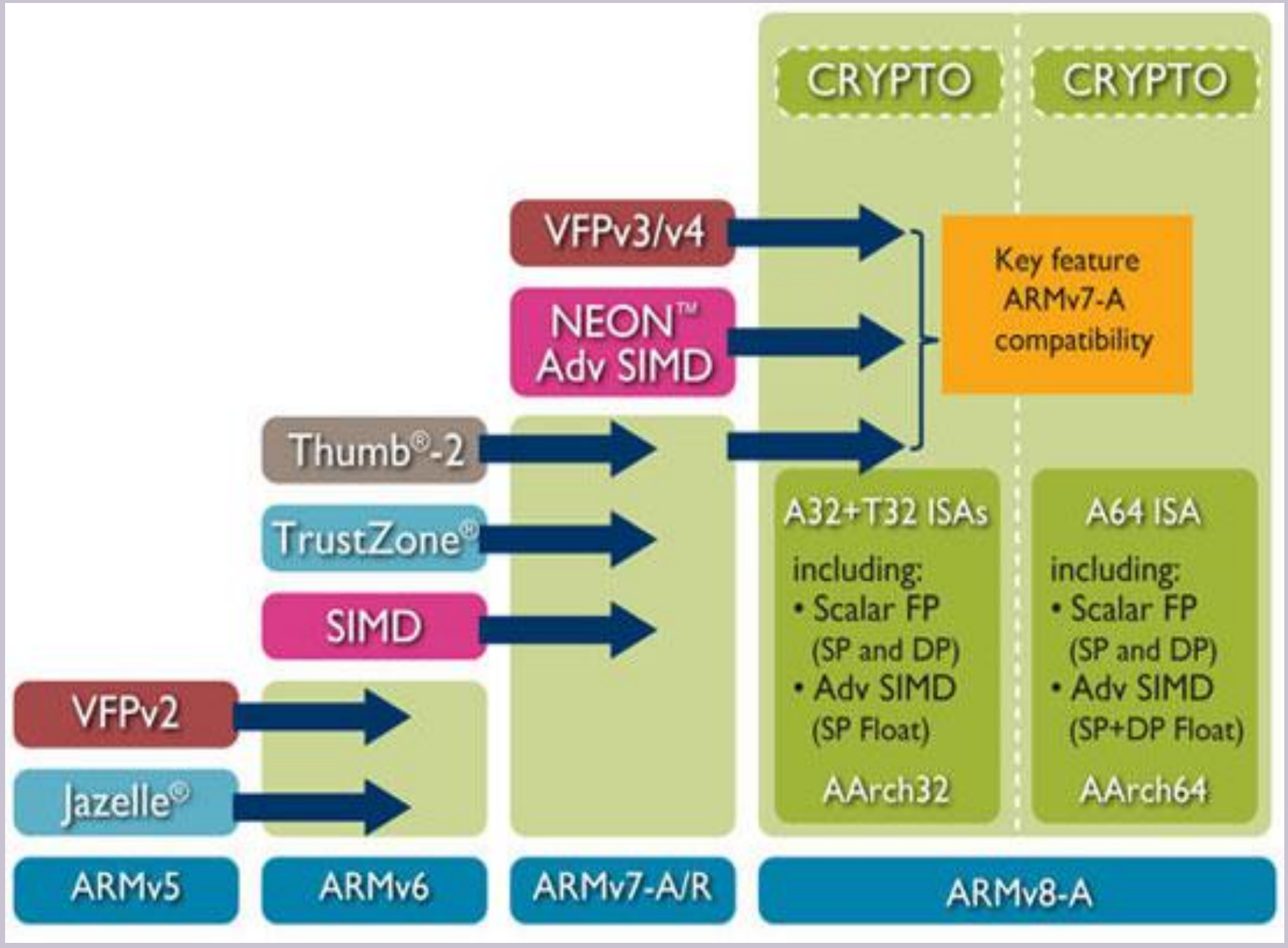
Trust Zone: is a system-wide approach to security for a wide array of client and server computing platforms include payment protection technology, digital rights management, BYOD, and a host of secured enterprise solutions

New extensions provided with v8 arch

Virtualization Extensions with the Large Physical Address Extension (**LPAE**) enable the efficient implementation of virtual machine hypervisors for ARM architecture compliant processors.

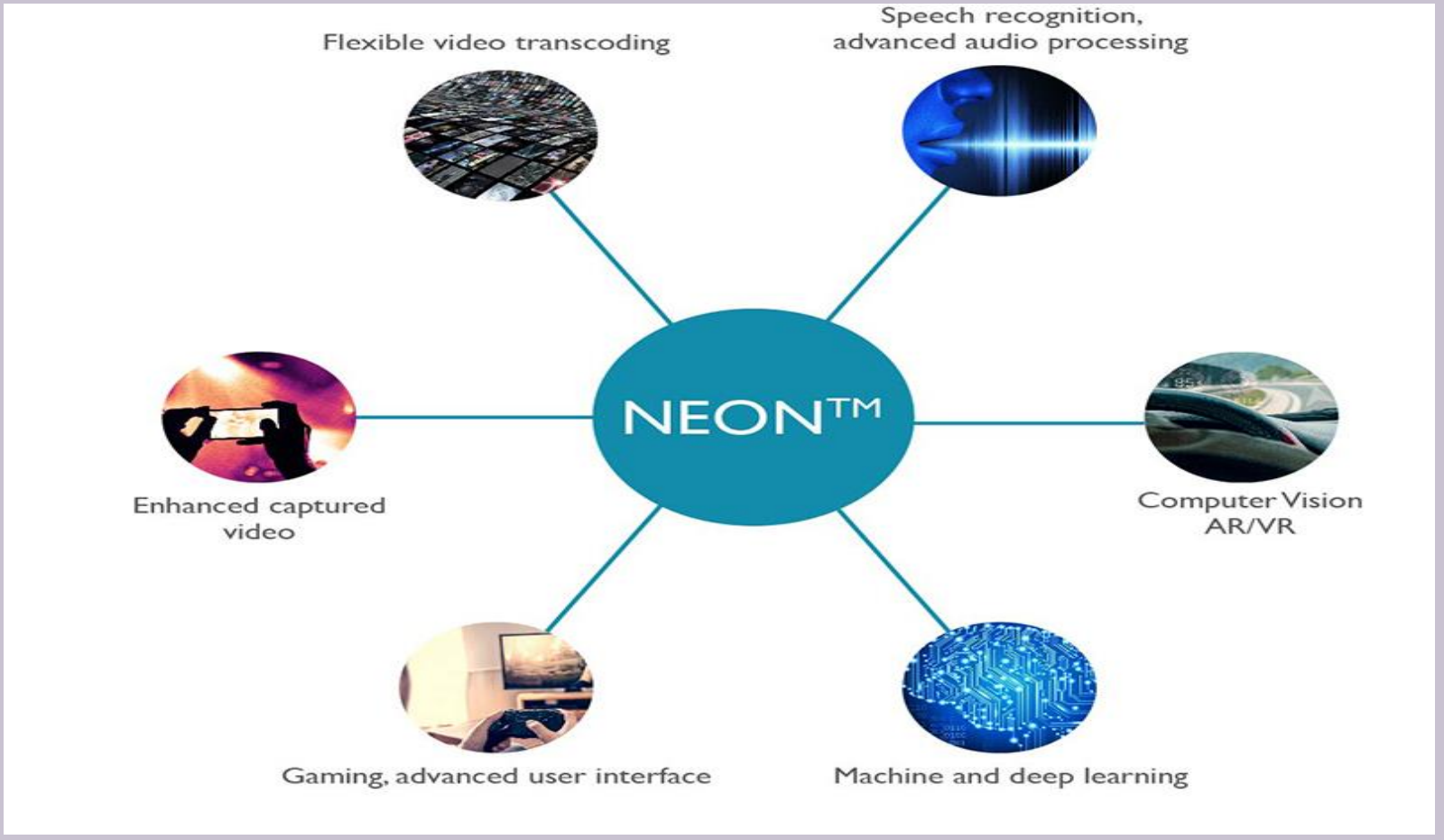
The visualization extensions provide the basis for ARM architecture compliant processors to address the needs of both client and server devices for the partitioning and management of complex software environments into virtual machines.

The Large Physical Address extension provides the means for each of the software environments to utilize efficiently the available physical memory when handling large amounts of data


CRYPTO
CRYPTO
VFPv3/v4
NEON™
Adv SIMD
Key feature
ARMv7-A
compatibility
Thumb®-2
TrustZone®
SIMD
A32+T32 ISAs
including:
• Scalar FP
(SP and DP)
• Adv SIMD
(SP Float)
AArch32
A64 ISA
including:
• Scalar FP
(SP and DP)
• Adv SIMD
(SP+DP Float)
AArch64
VFPv2
Jazelle®
ARMv5
ARMv6
ARMv7-A/R
ARMv8-A

What is NEON SIMD

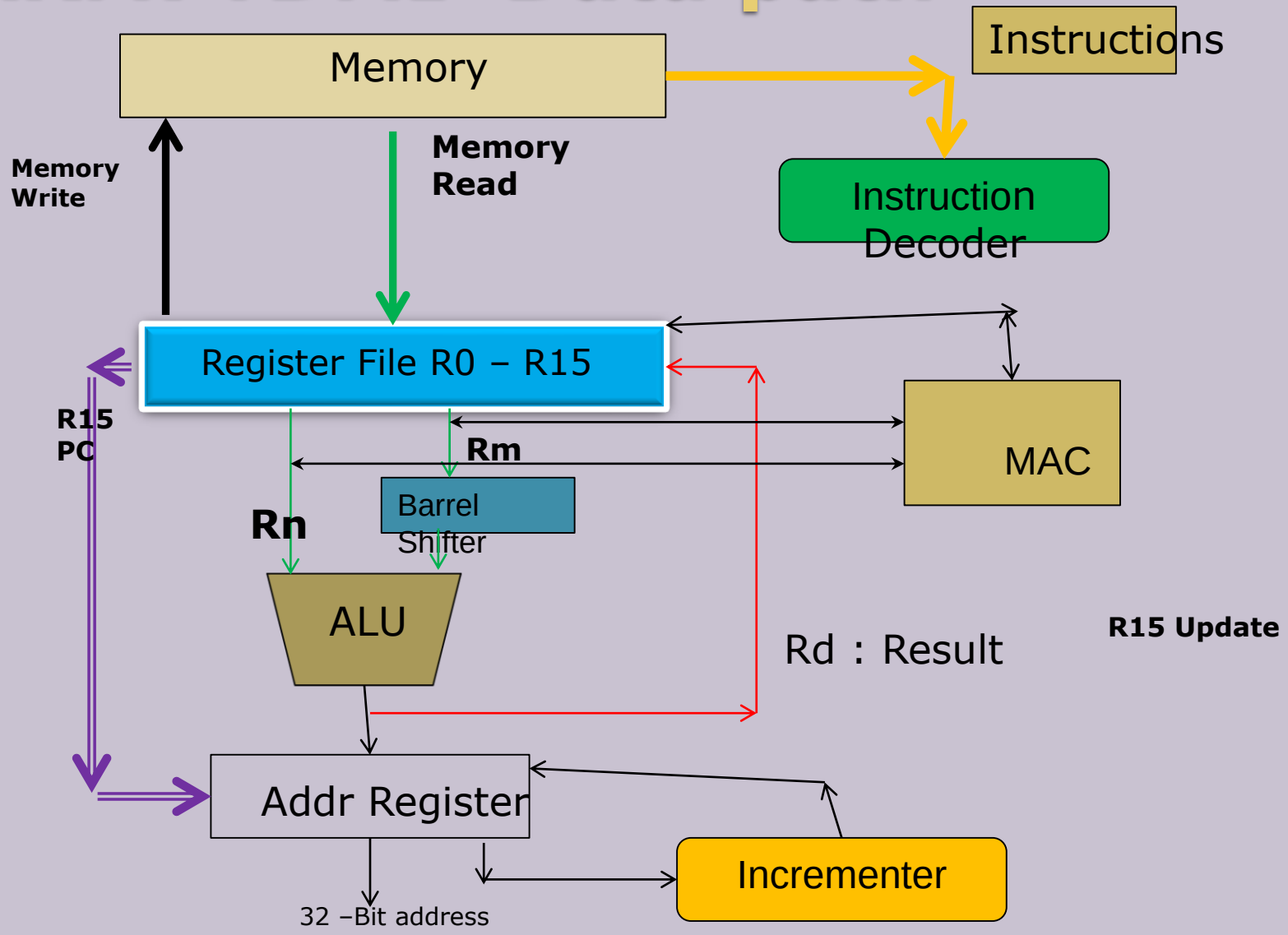
ARM NEON technology is an advanced SIMD (single instruction multiple data) architecture extension for the Arm Cortex-A series and Cortex-R52 processors.



ARM Cortex-M Series Family

Processor	ARM Architecture	Core Architecture	Thumb®	Thumb®-2	Hardware Multiply	Hardware Divide	Saturated Math	DSP Extensions	Floating Point
Cortex-M0	ARMv6-M	Von Neumann		Subset	1 or 32 cycle	No	No	Software	No
Cortex-M0+	ARMv6-M	Von Neumann	Most	Subset	1 or 32 cycle	No	No	Software	No
Cortex-M1	ARMv6-M	Von Neumann	Most	Subset	3 or 33 cycle	No	No	Software	No
Cortex-M3	ARMv7-M	Harvard	Entire	Entire	1 cycle	Yes	Yes	Software	No
Cortex-M4	ARMv7E-M	Harvard	Entire	Entire	1 cycle	Yes	Yes	Hardware	Optional

ARM7TDMI Data path



What is a Barrel Shifter

A barrel shifter is a combinational logic circuit with N data in puts,
N data outputs, and a set of control inputs that specify how t o shift the data between input and output.