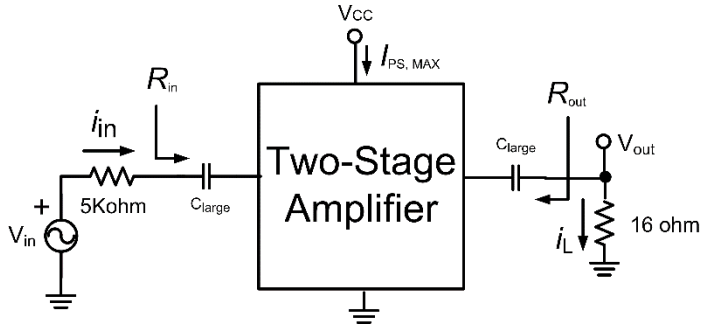
Design a two-stage BJT class-A amplifier to provide the following characteristics.

This project is an individual effort.

DESIGN SPECIFICATIONS:

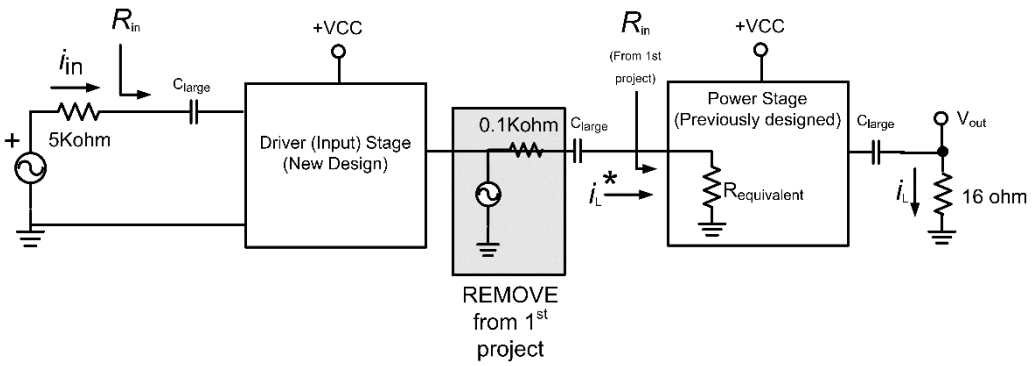
- Transistors: type 2N2222, nominal β = 200 with β_{min} = 100 and β_{max} =300
  (For OrCAD, select Q2N2222 in "Eval" library and edit the "PSpice Model" to change the value for β_f - right mouse click on transistor)
- Power Supply: V_{CC} = From your Project #1 design
- Source frequency = 1kHz
- Load Impedance: 16 Ω (impedance of speaker)



Performance Requirements

1. Primary Goal: Output load current peak swing, $i_{L,PEAK} \geq 140mA$ before clipping (280mA peak-to-peak) over the range $100 \leq \beta \leq 300$.
2. Primary Goal, the total (2-stage) small signal current gain, $A_i = \left|\frac{i_L}{i_s}\right| = 225$ at $\beta = 200$. Your simulated gain should be within 10% of this value.
3. Secondary Goal: Do not exceed maximum power dissipation for any 2N2222 of 0.6 watts.
4. Secondary Goal: Do not exceed maximum power dissipation for any resistor of 3 watts.
5. Secondary goal, total power supply current, I_{PS}, should not exceed 300mA.
6. Extra Points if your small signal gain, $A_i = \left|\frac{i_L}{i_s}\right|$, is stable with changes in β over the range $100 \leq \beta \leq 300$. A stable gain is $A_i \pm 15\%$ over this range in β.

HINT:
Design the input stage to your two-stage amplifier by (1) adding another transistor circuit to the beginning of your Project 1 amp design and design using the two transistors together **OR** (2) by using the equivalent input resistance, R_{IN}, of your Project 1 as the "load" to this new amplifier as shown in the figure below.



Using the approach in (2), you will need to translate the current gain and maximum swing specs to the equivalent circuit using i_L* and R_{IN}

$Gain_{proj\#2} = i_L^*/i_{in} = 225 / Gain_{proj\#1}$

$Current\ Swing_{proj\#2}$ in $i_L^* = Current\ Swing_{proj\#1} / Gain_{proj\#1}$

Note that in either design procedure; remove the voltage source and 0.1kΩ source resistor used during the design of the Project 1.

Submission Requirements:

A) HAND CALCULATIONS: Clearly show your hand calculations for the design of all components. After you are confident that your design meets the specifications, answer the following questions. **Submit all hand calculations and include a summary of the following items at the end of your calculations.** Use β **= 200** for all of the following calculations.

a. From project #1, list the equivalent input resistance, Rin, for that power amp stage using your PSpice results. Also list the PSpice small signal current gain for just the power amp.
b. What are your calculated DC transistor bias parameters? Make one **table** showing I_{CQ}, V_{BEQ}, V_{CEQ}, and P_D for each transistor (hand calculations for this design, PSpice for project #1).
c. What are the power rating for each of your resistors (both stages)? Make a **table** of the resistor values and expected power dissipation.
d. What is your total DC current, I_{PS}, supplied from the DC voltage source?
e. What is your calculated small signal current gain, A_i? Make a **table** of the gain for the driver (input) stage, the power amp stage, and the combined two-stage design.
f. What is your calculated small-signal Input Resistance, R_{in}, of the complete two-stage amplifier?
g. What is your calculated small-signal Output Resistance, R_{out}, of the complete two-stage amplifier?
h. Submit the complete schematic of your two-stage design.

B) PSPICE SCHEMATIC: **Submit your PSpice schematic** showing all values for DC voltage, DC current and DC Power for each circuit element (for OrCAD, select V, I and P

from the menu). On the schematic, make sure the DC parameters are positioned to allow the display of each resistor value (no display overlaps).

C) SIMLATED DC BIAS: What are the simulated DC bias parameters, $\boldsymbol{I_{CQ}}$, $\boldsymbol{V_{CEQ}}$, $\boldsymbol{V_{BEQ}}$ and transistor Power Dissipation, $\boldsymbol{P_D}$? Submit a table showing the simulated values for $\boldsymbol{I_{CQ}}$, $\boldsymbol{V_{CEQ}}$, $\boldsymbol{V_{BEQ}}$, and $\boldsymbol{P_D}$ for each transistor. As a comparison and on this same table, include the values that you calculated in (A).

D) SIMLATED POWER SUPPLY BIAS: What is the total current delivered from the supply, $\boldsymbol{I_{PS}}$? Does your circuit operate below the specification for maximum current, I_{PS} < 300mA.

E) SIMULATED CURRENT SWING: S Simulate your two-stage design in PSpice using a 1kHz sinusoidal input, use either a voltage source or a current source as the input. Place a current probe on the wire leading into your circuit (on the left side of the capacitor). What is the largest peak-to-peak swing in the output current, $\boldsymbol{i_L}$, through the 16 ohm load resistance? To find the maximum swing, you should slowly increase the source current amplitude until the output current waveform begins to clip at the top or the bottom. Unless you have a design optimized for maximum symmetrical swing in I_{CQ}, it's most likely that the clipping will not be symmetrical. In other words, the point of clipping in the positive peak current will be different from the negative peak current. **Submit a plot** showing i_L with clipping using a β = 200. When clipping occurs, chose the smaller of the two values and double this value, this is the peak-to-peak swing in the output current, i_L. **Report** the peak-to-peak swing in the output current, i_L. Did your design achieve the 140mA peak swing (280mA peak-to-peak)?

F) Repeat (E) for β = 100 and 300. **Submit a table** showing the maximum peak-to-peak swing in i_L for β = 100, 200 and 300. Did you meet the peak-to-peak swing under all conditions?

G) SIMULATED EFFICIENCY: Using the peak swing in load current, i_L, and load resistance, 16 ohms, **calculate the simulated power conversion efficiency, η**? You will need the simulated I_{PS} in this calculation. Show all your calculations using data recorded from your simulated plots, no points for just an answer.

H) SIMULATED SMALL SIGNAL OPERATION: Using PSpice, reduce the input current amplitude until both transistors are operating in the small signal region. This current should be small enough to operate your transistor in the small signal region. Verify that the peak AC voltage across the Base-Emitter junction, v_{be}, is less than 2.6mV peak (<<26mV) for both transistors. In OrCAD, you can verify the voltage using the "Differential Voltage Probe" measurement. If v_{be} is greater than 2.6mV, decrease the source current until the voltage is in the small signal range for both transistors. **Record** the amplitude value of the source current for small signal operation. **Submit plots** showing of v_{BE} for β = 200 for both transistors. Use a scale so the voltage waveforms can easily be observed.

I) SIMULATED TWO-STAGE CURRENT GAIN: Using the input source current amplitude found in part (H), what is the small signal gain, $A_i = \left|\frac{i_L}{i_S}\right|$, at β = 200? **Submit two plots** showing i_S and i_L under small signal conditions using a β = 200. Did you achieve a current gain, $|i_L/i_S|$, of 225 ?

J) SIMULATED GAIN VARIATION WITH β: Continue with Step (I), what is the current gain, i_L/i_S, when β =100 and β =300 (plots are not required here)? **Submit a table**

showing current gain, $|i_L/i_S|$, for β = 100, 200 and 300. Do you achieve a current gain variation ± 15% about the nominal value of β = 200.?

K) SIMULATED INPUT RESISTANCE: Using the source amplitude found in part (H), what is the simulated input resistance, ***Rin***, to your amplifier? Using current and voltage test probes at the amplifier input to calculate the input resistance using PSpice by placing cursors at the peak of each sinusoidal waveform and dividing the voltage peak by the current peak (absolute values are acceptable if required). Note that the placement of V/I probes on the schematic in circuit areas where there is DC voltage and/or DC current will result in a DC offset in the simulated measurements, if so, either move the probe or subtract the DC offset from the results. **Submit a plot** showing ***v***s and ***i***s on two separate graphs for β = 200. **Submit a table** showing ***Rin*** for β = 100, 200 and 300.

L) SIMULATED FREQUENCY RESPONSE: Perform a small signal "AC" analysis of the small signal current gain over the frequency range of 100Hz to 10MHz for β=200 (note: in OrCAD, you will need to change the source to an IAC or VAC). **Record** the 3dB bandwidth of the current gain, $|i_L/i_S|$ (use 20*log10($|i_L/i_S|$))? You may need to increase the upper end of the frequency range (>10MHz) if the gain has not fallen by 3dB. **Submit a plot** showing the current gain as a function of frequency using a "log" scale in the x-axis. What does this frequency range tell you about your amplifier?

M) SIMULATION USING STANDARD RESISTOR VALUES: Using your PSPICE design, substitute the standard resistors into your model. Using β=200, simulate the peak-peak current swing and small signal current gain. **Submit a plot** showing i_L with clipping at both the positive and negative peaks using a β = 200. **Submit plots** of i_s and i_L under small signal conditions. Did your amplifier achieve the peak-peak and nominal gain specifications when the resistors are changed? **Submit a table** comparing the simulated peak swing and the simulated small signal gain with the original and standard resistors.

N) COMPONENT BILL OF MATERIALS (BOM) FOR LAB EXPERIMENT: Working with your lab partner, select one of your two-stage amplifier designs that you would like to build for the lab experiment. Create the BOM, with resistor values (ohms), the quantities for each type of resistor and the required power spec (1/4 watt, ½ watt, 1 watt or 3 watt). Include the BOM in your project submission and also s**ubmit your BOM by email to Robert Rivera, rwrivera@nyu.edu. Include your lab section in email title (for example, EE3124 BOM Lab Section A1). The BOM must be received by Wed, April 12 at noon. Late submissions of BOM will have a large point deduction in Lab #5 for both partners.**