Name: _____Dillon Britt____

CPHE 222 Organization, Architecture, and Assembly Language
Chapter #4B Reading Quiz

This is a take-home reading quiz. Your textbooks is the only outside resource that you are allowed to use while completing this quiz. Do NOT consult with other students or anyone else while working on this quiz. Answer each question below based on the material in the reading assignment (Chapter 4.5).

Chapter 4B

1. In modern processors, pipelining techniques are used <Very Often, Somewhat Often, Somewhat Rarely, Very Rarely> (circle one). (4.5)
   Very often

2. The steps/units in a pipelined processor that can operate concurrently are called _____. (4.5)
   Stages

1) What are the five steps that MIPS instructions go through during execution? (4.5)
   Fetch instruction from memory.
   Read registers while decoding the instruction. Th e regular format of MIPS instructions allows reading and decoding to occur simultaneously.
   Execute the operation or calculate an address.
   Access an operand in data memory.
   Write the result into a register.
3. Why do pipelined processor rarely (never) yield the ideal speedup? (4.5)

4. Does pipelining improve performance by increase instruction throughput or decreasing execution time of an individual instruction? (4.5) **It improves the performance by increasing the multiple instructions simultaneously**

5. What are the three categories of pipeline hazards discussed in your textbook? (4.5)
   a. Structural hazard
   b. Data Hazard
   c. Control Hazard

6. _____ hardware can be added in the processor datapath to resolve many data hazards. (4.5)
   Extra

7. Can forwarding logic prevent all pipeline stalls due to data hazards? (4.5)
   NO it can not

8. Which types of MIPS instructions can create control hazards? (4.5)
   Type I instructions

9. Modern computers use __**Branch Prediction**__ to mitigate the effects of control hazards on performance. (4.5)

10. If you are implementing a static branch prediction scheme, what two static "guesses" can you use to predict each branch? (4.5)
    Stall, Predict

11. For each code segment below, specify if a hazard exists, the type of hazard that exists, and whether or not forwarding logic will prevent all stalls or just some stalls. (4.5)

Code Segments	Does a pipeline hazard exist?	If exists, what type of hazard?	Does forwarding logic prevent <SOME, ALL> stalls?
`lw $t0, 0($t2)` `add $t1, $t0, $t0`	Yes	Structural	Some

`add $t1, $t0, $t0`
`addi $t2, $t0, 5`
`addi $t4, $t1, 5`
	Yes	Data	All

`addi $t1, $t0, 1`
`addi $t2, $t0, 2`
`addi $t3, $t0, 2`
`addi $t3, $t0, 4`
`addi $t5, $t0, 5`
	Yes	Data	All

`add $t1, $t0, $t0`
`ori $t2, $t1, 0x0F`
`addi $t4, $t2, 5`
	Yes	Data	Some