

CPHE 222: Organization, Architecture & Assembly Language (4 credit)

Winter Semester, 2017

Instructor:

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Office Hours:

(see *computing.southern.edu/tyson* for current office hours)

Textbook:

D. A. Patterson and J. L. Hennessy, *Computer Organization and Design*, 5th ed.
Morgan Kaufmann Publishers, 2014.
J. O. Hamblen, T. S. Hall, and M. O. Furman, *Rapid Prototyping of Digital Systems: SOPC Edition*, Springer Publishers, 2007.

Prerequisites:

CPHE 200: Digital Logic & Design
CPT R 124: Fundamentals of Programming

Course Description:

Basic machine organization and architecture. Processor components, instruction sets, memory types and hierarchy. Introduction to data representation, instruction formats, addressing techniques, assembly language, pipelining, and I/O bus architectures.

Objectives:

- Upon successful completion of this course, you will be able to do the following:
- Explain the use of the internal registers of a MIPS processors.
 - Write a software program using an assembly language.
 - Use a hardware simulator to track and debug a program executing on the processor.
 - Manipulate fixed and floating-point binary numbers, including arithmetic and Boolean operations.
 - Identify and explain the hardware components of a RISC microprocessor.
 - Understand the basic hardware architecture of a single-cycle RISC datapath.
 - Understand the basic concepts of a pipelined datapath and recognize common data hazards that must be avoided.
 - Design a basic processor datapath.
 - Understand the structure of different cache configurations.
 - Analyze and evaluate the performance of different cache configurations
 - Understand basic virtual memory techniques
 - Read and summarize technical articles from IEEE journals.
 - Learn to use the IEEE Computer Society online database to find technical articles on given subjects.
 - Complete a team-based project that includes the design of custom hardware and/or software components.
 - Within a team-based design environment, individually complete the design, implementation, and/or testing of at least one component that will be used towards the completion of the final project.

Course Requirements

DSS:

In keeping with the University's policy, if you are a student who believes you may need an accommodation based on the impact of a disability or learning challenge, (i.e. physical, learning, psychological, ADHD or other type), you are strongly encouraged to contact Disability Support Services (DSS) at 423-236-2544 or stop by Lynn Wood Hall, Room 1082. Please note that accommodations are not retroactive and cannot be implemented until faculty or staff members have received the official Letter of Accommodation from DSS. Specific details of disabilities remain confidential between students and DSS unless a student chooses to disclose or there is legitimate need for disclosure, which is on a case-by-case basis. For further details, visit the Disability Support Services website at www.southern.edu/disabilitysupport.

Attendance:

Attendance in lecture and laboratory is required. You are responsible for all material covered during lectures and labs, including assignments and modifications to assignments given at these times and on the class website. Late lab assignments will be penalized 10% per week past the deadline.

Homework/Projects:

All homework assignments and projects are expected to be individual efforts. You may receive general assistance from other students, but you should not copy other students' work or complete any portion of other students' work. To receive full credit, you must turn in your homework and projects during or before the class period in which it is due. Late assignments will be penalized 10% and will only be accepted up to the time when answer sheets are provided to the class. **All** assigned laboratory projects must be completed to receive a passing grade. Students with a missing or 0 grade on even a single laboratory assignment will receive an F for the course. Students may request a 50% check-off if they have demonstrated extraordinary effort on a particular laboratory project and can still not complete the assignment.

Quizzes:

Quizzes will be given on a regular, unannounced basis. No make-up quizzes will be given. However, your two lowest quiz grades will be dropped when calculating final grades.

Exams:

Three exams will be given in this course. Unless otherwise announced, all exams will be comprehensive for the term up until the class period of the exam.

Grading:

A final grade will be assigned based on the following submitted work:

25%	Final Exam
25%	Exams 1 & 2
25%	Projects
25%	Homework, Quizzes, & Attendance

Grading Scale:

Grades will be computed from the weighted scores and letter grades will generally be assigned as follows (these are guaranteed minimums):

100 - 92% = A	81 - 80% = B-	69 - 68% = D+
91 - 90% = A-	79 - 78% = C+	67 - 62% = D
89 - 88% = B+	77 - 72% = C	61 - 60% = D-
87 - 82% = B	71 - 70% = C-	≤ 59% = F

Academic Honesty:

This course will be governed by the academic honesty policy as outlined in this year's version of Southern's Catalog. Southern Adventist University is dedicated to scholastic integrity. Consequently, both students and faculty are required to maintain high, ethical Christian levels of honesty.

Course Evaluation: Near the end of the semester, you will need to evaluate this course. Southern Adventist University requires all students enrolled in courses, on campus or online, which enroll more than 5 students, to complete course evaluations as part of the ongoing process of improving course delivery and academic standards.

You may access this evaluation at <http://www.southern.edu/access/>. Log in using your SAU e-mail name and password, and then select Course Tools ⇨ Course Evaluation. All comments and evaluations are completely anonymous and the results of these course evaluations are made available to professors only after grades are submitted to the Records office.

Tentative Schedule

WEEK	LECTURE TOPICS	LAB TOPICS
Jan 9-13	Syllabus and Intro. Computer Hardware Instruction Set Architecture	Intro. to Logic Analyzers
Jan 16-20	Instruction Set Architecture	VHDL & Timing Simulation Refresher
Jan 23-27	Assembly Language Programming	Intro. to MARS Simulator
Jan 30 – Feb 3	Assembly Language Programming	Assembly Programming I
Feb 6-10	Exam 1	Assembly Programming II
Feb 13-17	Processor Datapath and Control	Embedded Programming I
Feb 20-24	Processor Datapath and Control	Embedded Programming II
Feb 27 – Mar 1	Processor Datapath and Control	Processor Synthesis I
Mar 3-10	Spring Break	Spring Break
Mar 13-17	Pipelining the Datapath	Processor Synthesis II
Mar 20-24	Pipelining the Datapath	Processor Synthesis III
Mar 27-31	Exam 2	Embedded Processors
April 3-7	Memory Hierarchy	Design Project
April 10-14	Memory Hierarchy	Design Project
April 17-21	Memory Hierarchy	Design Project
April 24-28	Storage, Networks, and Peripherals	Cache Simulator
Tuesday, May 2, 10am	Final Exam	
Thursday, May 4, 11:59pm	Final chance to turn in labs and homework (incl. design project)	

* See our class eClass page for specific assignment information.