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Homework 1

1. Assembly lines in automobile = Pipelining  
   Suspension Bridge = Parallelism   
   Aircraft and Marine navigation system = performance via Prediction  
   Express elevators = Moore’s law
2. Assume a color display using 8 bits for each of the primary colors(red, green, blue) per pixel and a frame size of 1280 × 1024.
   1. 1280 \* 1024 = 1310720  
      1310720 \* 3 = 3932160 btys/frame
   2. 3932160 \* 8 = 31457280  
      31457280 bits / 100 Mbit/s = 31457280/100000000 = 0.314 Seconds
3. Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.
   1. P1 : 3 GHz / 1.5 = 2\*10^9 instruction/s  
      P2 : 2.5/1.0 = 2.5 \* 10^9 inst/s  
      P3 : 4.0/2.2 = 1.81 \* 10^9 inst/s  
      P2 has the highest
   2. 3 GHz\* 10 = 3 \* 10^10  
      2.5 GZs \* 10 = 2.5 \* 10^10  
      4 GHz \* 10 = 4 \* 10^10
   3. Execute time = (Num of instructions \* CPI) / (Clock rate)  
      Time \* .7 = (Num of instructions \* CPI \* 1.20) / (Clock rate)  
      3 GHZ \* 1.71 = 5.13 GHZ  
      2.5 GHZ \* 1.71 = 4.27 GHZ  
      4 GHZ \* 1.71 = 6.84 GHZ
4. Clock Time = Inst Count \* CPI / Clock Rate  
   Part 1  
   CPU A =   
   CPU B =   
   CPU C =   
   CPU D =  
   Sum of A through D = 0.00104  
   Part 2  
   CPU A =   
   CPU B =   
   CPU C =   
   CPU D =   
   Sum of A through D is 0.0006
   1. CPI for each implementation  
      ((2.5 \* 10^9)\*(.00104 ))/10^6 = 2.6  
      ((3 \* 10^9)\*(.0006))/10^6 = 1.8
   2. Clock cycles = (1\*10^5)1 + (2\*10^5)2 + (5\*10^5)3 + (2\*10^5)3  
      Clock cycles = (1\*10^5)2 + (2\*10^5)2 + (5\*10^5)2 + (2\*10^5)2
5. 1. Cap load = 40  
      Cap load = power/(V^2 Clock Rate)
   2. 10+ 90 = 100w  
      static/total = 30/100 = .30  
      static/total = 40/100 = .40
6. 1. 234 sec
   2. 15 sec