Zephyr on STM32: What you need to know

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Zephyr Developper Summit

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A bit about myself

- Working @STMicroelectonics, Le Mans
- Started Zephyr in 2016
- Initially contributed as a Linaro assignee
- Contributed to Device Tree introduction
- STM32 & Shields maintainer
- ST Zephyr Technical leader

- Github: erwango
- Discord: ErwanG

Why proposing this talk ?

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What you'll learn from this talk

- # STM32 resources
- # STM32 parts support
- # Clock configuration
- # Peripherals
- # Power Management
- # Trusted Firmware Support
- # Join the party
- # Questions

STM32 support in Zephyr

380+ contributors issued 5000+ commits

130+ boards supported

180+ Supported SoC (19 series)

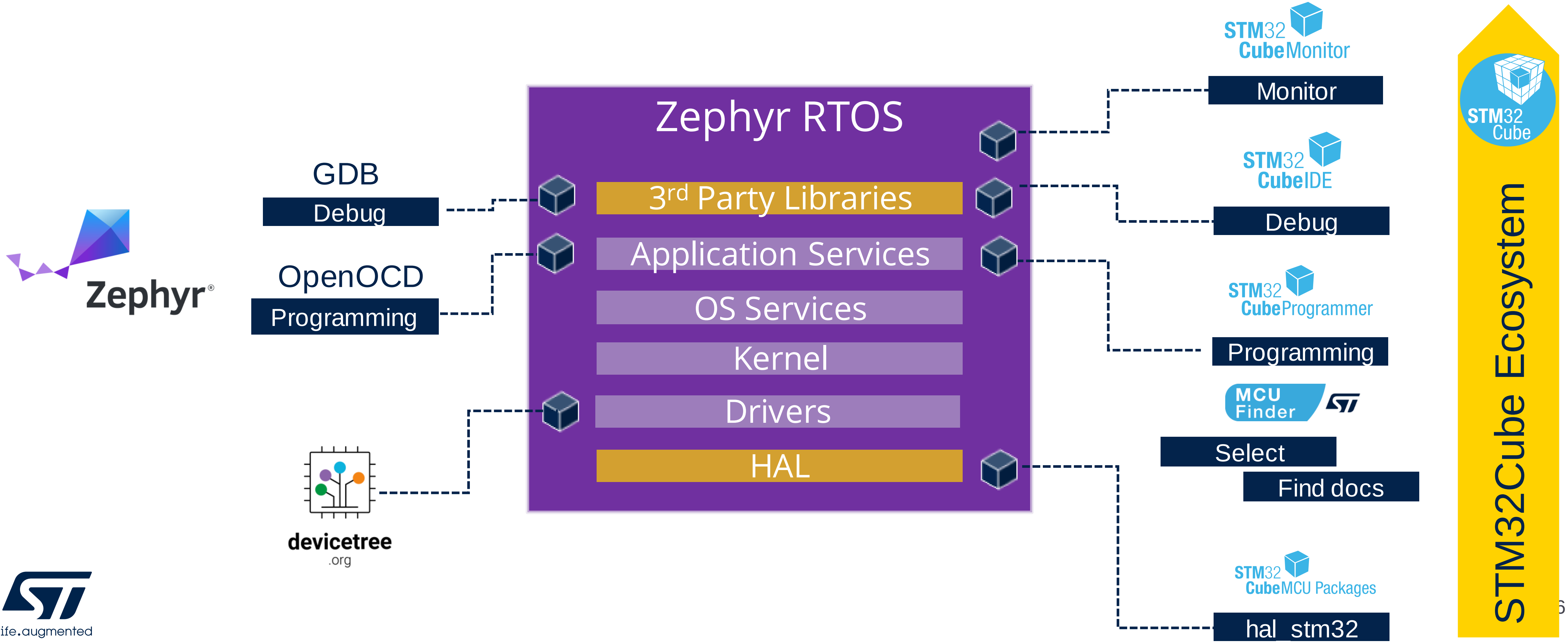
40+ peripherals supported

Wide range of features
TF-M, USB, Ethernet, CAN, BLE, LoRa..

STM32 resources

Zephyr RTOS

Complemented with STM32Cube Ecosystem



Zephyr

GDB

Debug

OpenOCD

Programming

devicetree.org

Zephyr RTOS

3rd Party Libraries

Application Services

OS Services

Kernel

Drivers

HAL

STM32CubeMonitor

Monitor

STM32CubeIDE

Debug

STM32CubeProgrammer

Programming

MCU Finder

Select

Find docs

STM32CubeMCU Packages

hal_stm32

STM32Cube

STM32Cube Ecosystem

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How we're integrating STM32Cube HAL

- STM32CubeMCU packages are stored under zephyr **hal_stm32** module
  - Forks of https://github.com/STMicroelectronics/STM32CubeXX
  - Updated at each Zephyr release
  - Patches allowed under specific conditions

- STM32Cube APIs are used for Zephyr drivers developments
  - Allows reuse of validated code and factorization
  - HAL, LL or CMSIS files used depending on drivers specifics

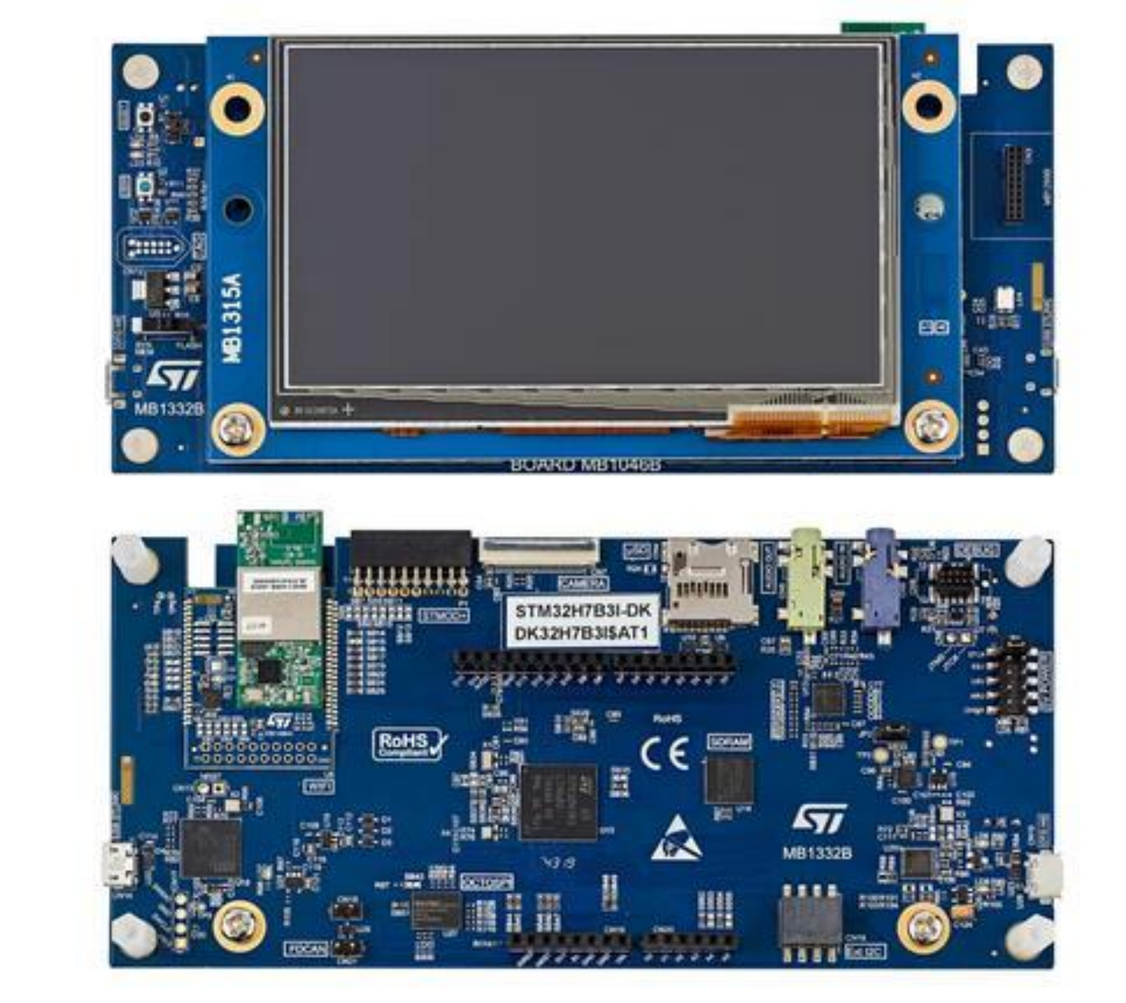
Misc on STM32Cube HALs

- Use CMSIS files to populate dts node properties
  - Eg: hal_stm32: stm32cube/stm32l4xx/soc/stm32l431xx.h

- You can mix Zephyr and STM32Cube APIs in your application
  - See https://github.com/zephyrproject-rtos/hal_stm32#use-stm32cube-in-your-application

- CONFIG_USE_STM32_ASSERT=y

Configuring a STM32 based board



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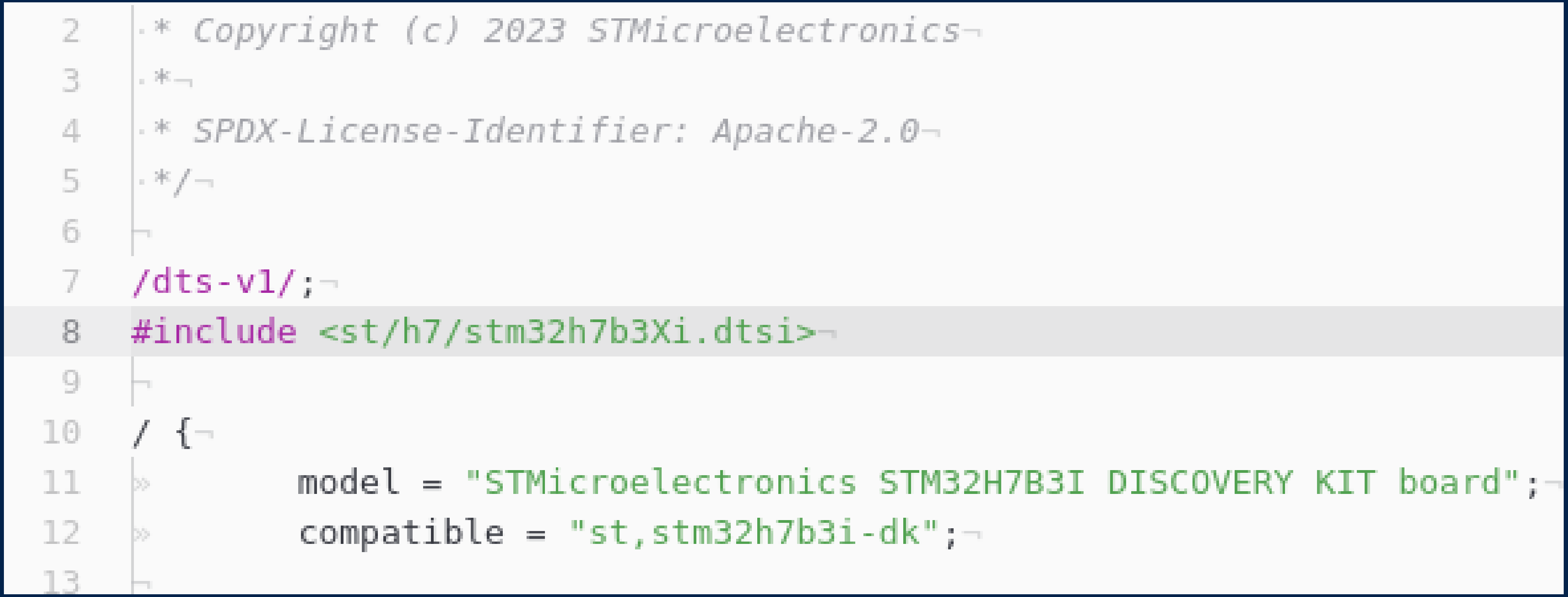
1- Select a STM32 part



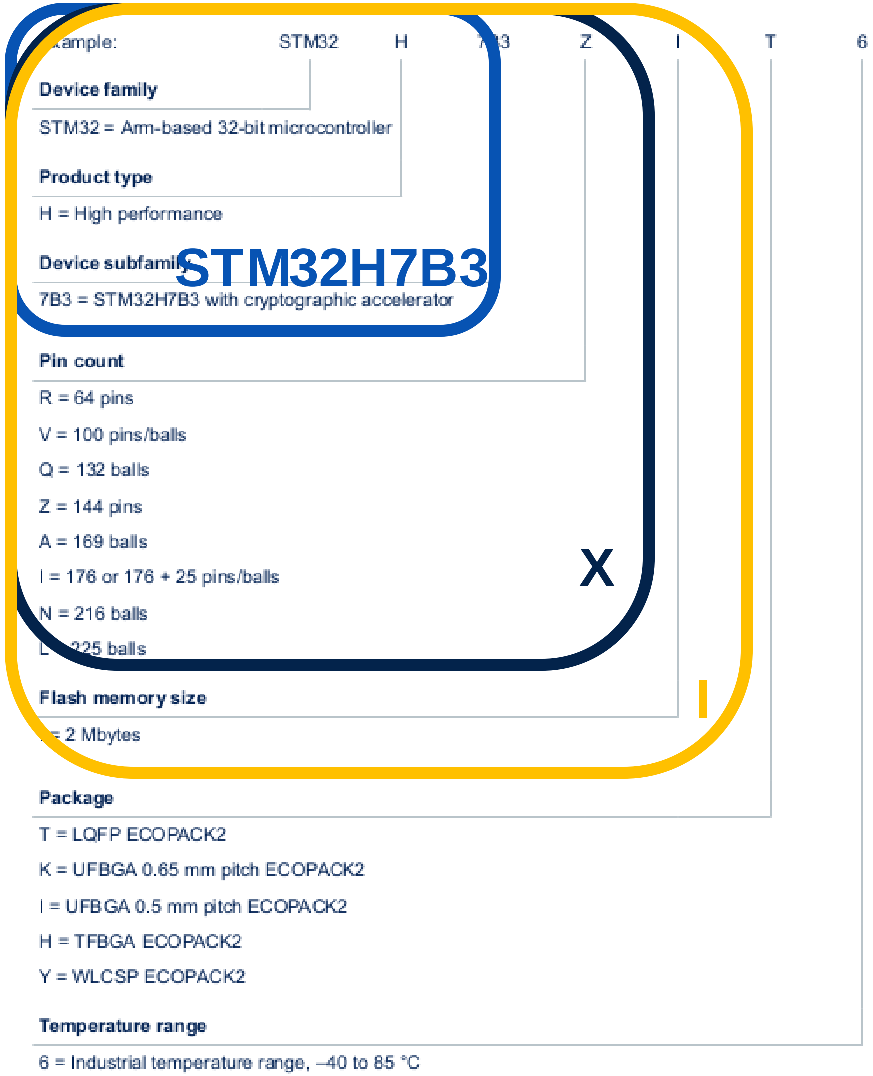
```
 * Copyright (c) 2023 STMicroelectronics
 *
 * SPDX-License-Identifier: Apache-2.0
 */

/dts-v1/;
#include <st/h7/stm32h7b3Xi.dtsi>

/ {
	model = "STMicroelectronics STM32H7B3I DISCOVERY KIT board";
	compatible = "st,stm32h7b3i-dk";

```

Identify a supported STM32 part



Example: STM32 H 7B3 Z I T 6

Device family

STM32 = Arm-based 32-bit microcontroller

Product type

H = High performance

Device subfamily

7B3 = STM32H7B3 with cryptographic accelerator

Pin count

R = 64 pins

V = 100 pins/balls

Q = 132 balls

Z = 144 pins

A = 169 balls

I = 176 or 176 + 25 pins/balls

N = 216 balls

L = 225 balls

Flash memory size

I = 2 Mbytes

Package

T = LQFP ECOPACK2

K = UFBGA 0.65 mm pitch ECOPACK2

I = UFBGA 0.5 mm pitch ECOPACK2

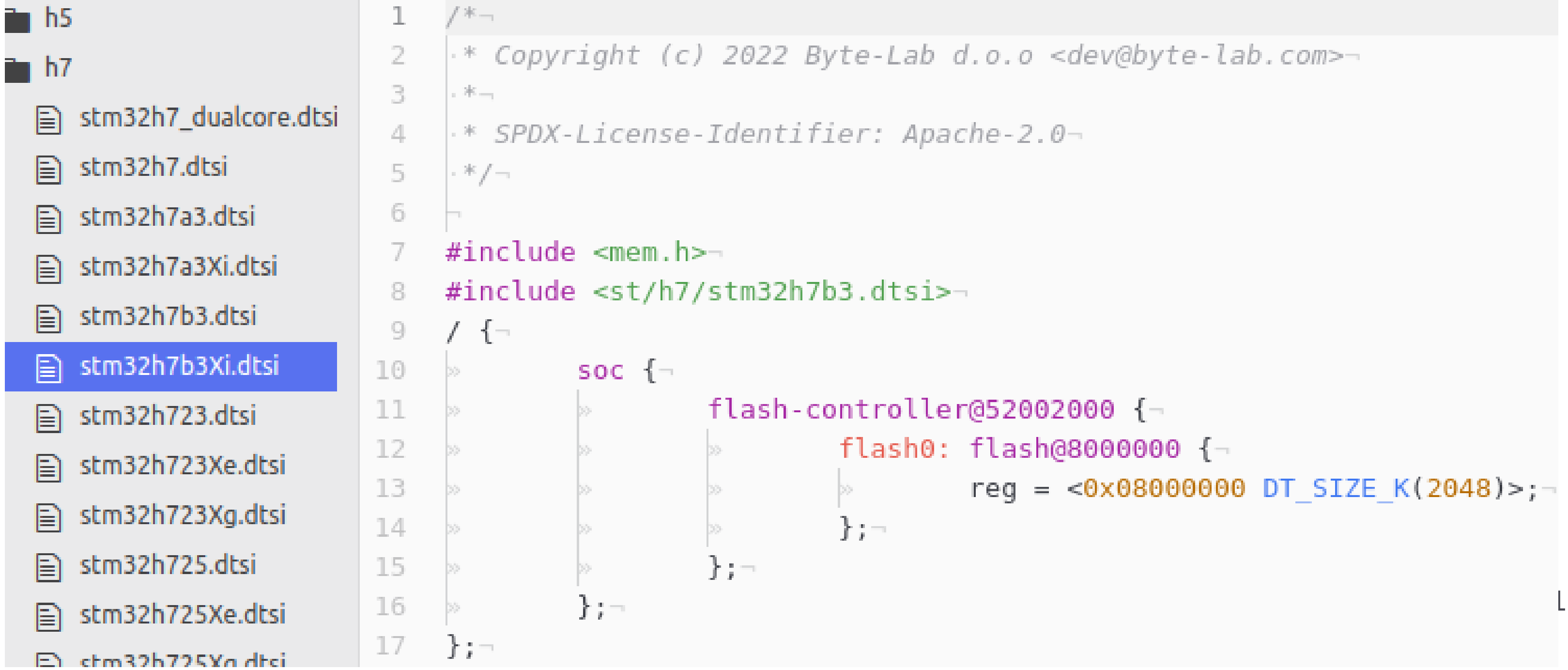
H = TFBGA ECOPACK2

Y = WLCSP ECOPACK2

Temperature range

6 = Industrial temperature range, –40 to 85 °C

- **Series**: STM32H7
- **SoC variant**: B3
- Pin count: Not used: X
- **SoC Package memory size**: I
- In **dts/arm/st/h7**, look for **stm32h7b3Xi.dtsi**

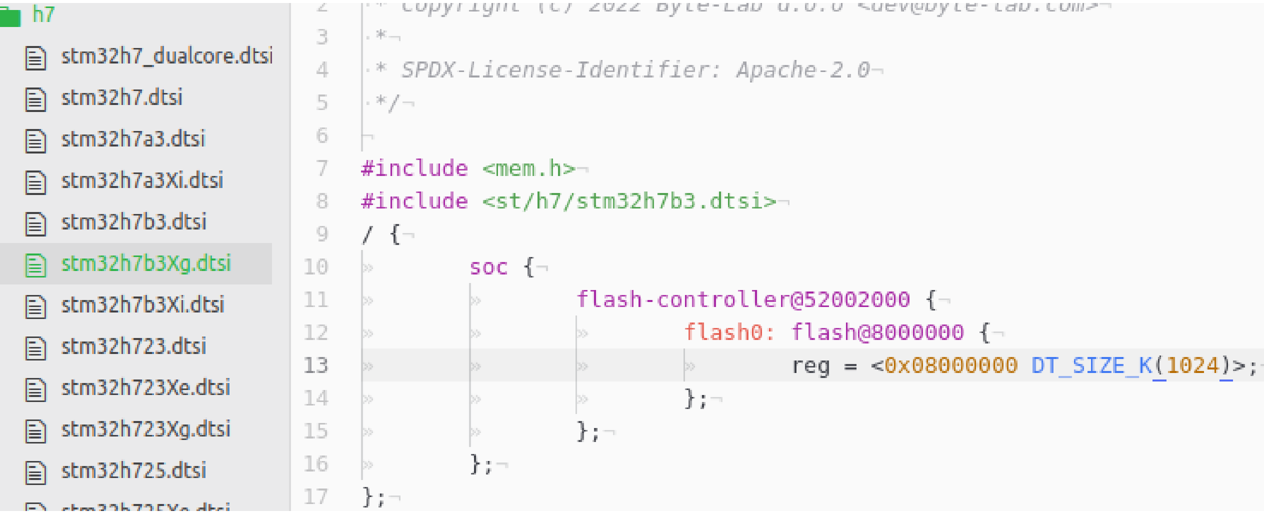


```
/*
 * Copyright (c) 2022 Byte-Lab d.o.o <dev@byte-lab.com>
 *
 * SPDX-License-Identifier: Apache-2.0
 */

#include <mem.h>
#include <st/h7/stm32h7b3.dtsi>
/ {
	soc {
		flash-controller@52002000 {
			flash0: flash@8000000 {
				reg = <0x08000000 DT_SIZE_K(2048)>;
			};
		};
	};
};
```

Add a STM32 part not supported yet

- Add a memory size variant:
  - Eg STM32H7B3 1MB Flash variant:

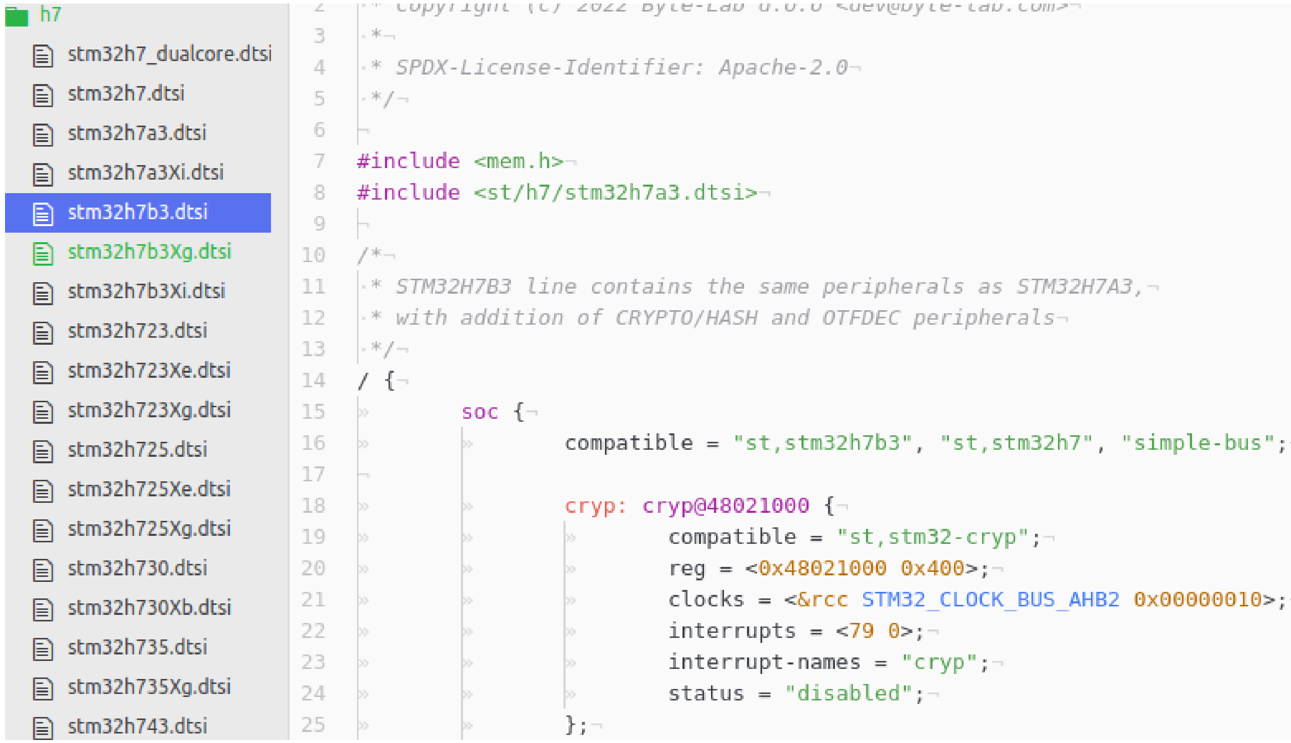


h7
- stm32h7_dualcore.dtsi
- stm32h7.dtsi
- stm32h7a3.dtsi
- stm32h7a3Xi.dtsi
- stm32h7b3.dtsi
- stm32h7b3Xg.dtsi
- stm32h7b3Xi.dtsi
- stm32h723.dtsi
- stm32h723Xe.dtsi
- stm32h723Xg.dtsi
- stm32h725.dtsi
- stm32h725Xe.dtsi

```
 * Copyright (c) 2022 Byte-Lab d.o.o <dev@byte-lab.com>
 *
 * SPDX-License-Identifier: Apache-2.0
 */

#include <mem.h>
#include <st/h7/stm32h7b3.dtsi>
/ {
	soc {
		flash-controller@52002000 {
			flash0: flash@8000000 {
				reg = <0x08000000 DT_SIZE_K(1024)>;
			};
		};
	};
};
```

- Add a SoC variant:



h7
- stm32h7_dualcore.dtsi
- stm32h7.dtsi
- stm32h7a3.dtsi
- stm32h7a3Xi.dtsi
- stm32h7b3.dtsi
- stm32h7b3Xg.dtsi
- stm32h7b3Xi.dtsi
- stm32h723.dtsi
- stm32h723Xe.dtsi
- stm32h723Xg.dtsi
- stm32h725.dtsi
- stm32h725Xe.dtsi
- stm32h725Xg.dtsi
- stm32h730.dtsi
- stm32h730Xb.dtsi
- stm32h735.dtsi
- stm32h735Xg.dtsi
- stm32h743.dtsi

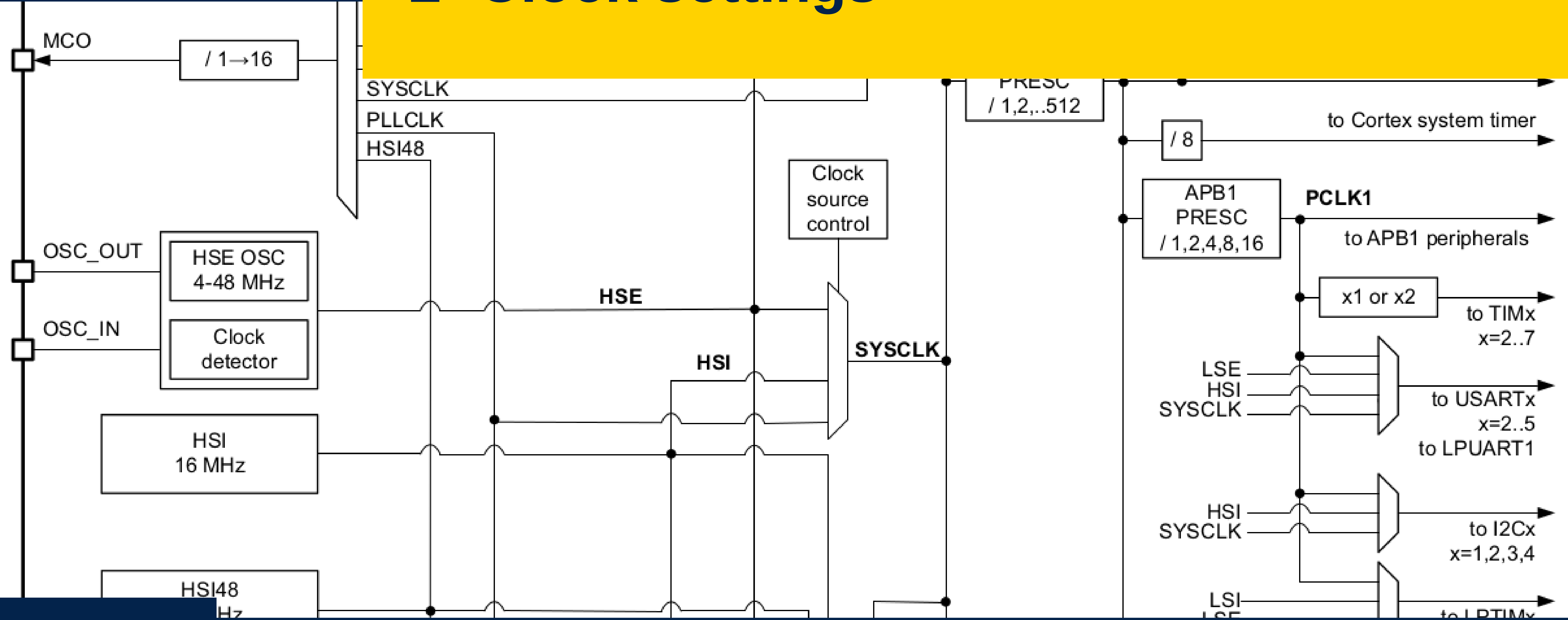
```
 * Copyright (c) 2022 Byte-Lab d.o.o <dev@byte-lab.com>
 *
 * SPDX-License-Identifier: Apache-2.0
 */

#include <mem.h>
#include <st/h7/stm32h7a3.dtsi>

/*
 * STM32H7B3 line contains the same peripherals as STM32H7A3,
 * with addition of CRYPTO/HASH and OTFDEC peripherals
 */
/ {
	soc {
		compatible = "st,stm32h7b3", "st,stm32h7", "simple-bus";

		cryp: cryp@48021000 {
			compatible = "st,stm32-cryp";
			reg = <0x48021000 0x400>;
			clocks = <&rcc STM32_CLOCK_BUS_AHB2 0x00000010>;
			interrupts = <79 0>;
			interrupt-names = "cryp";
			status = "disabled";
		};
```

2- Clock settings



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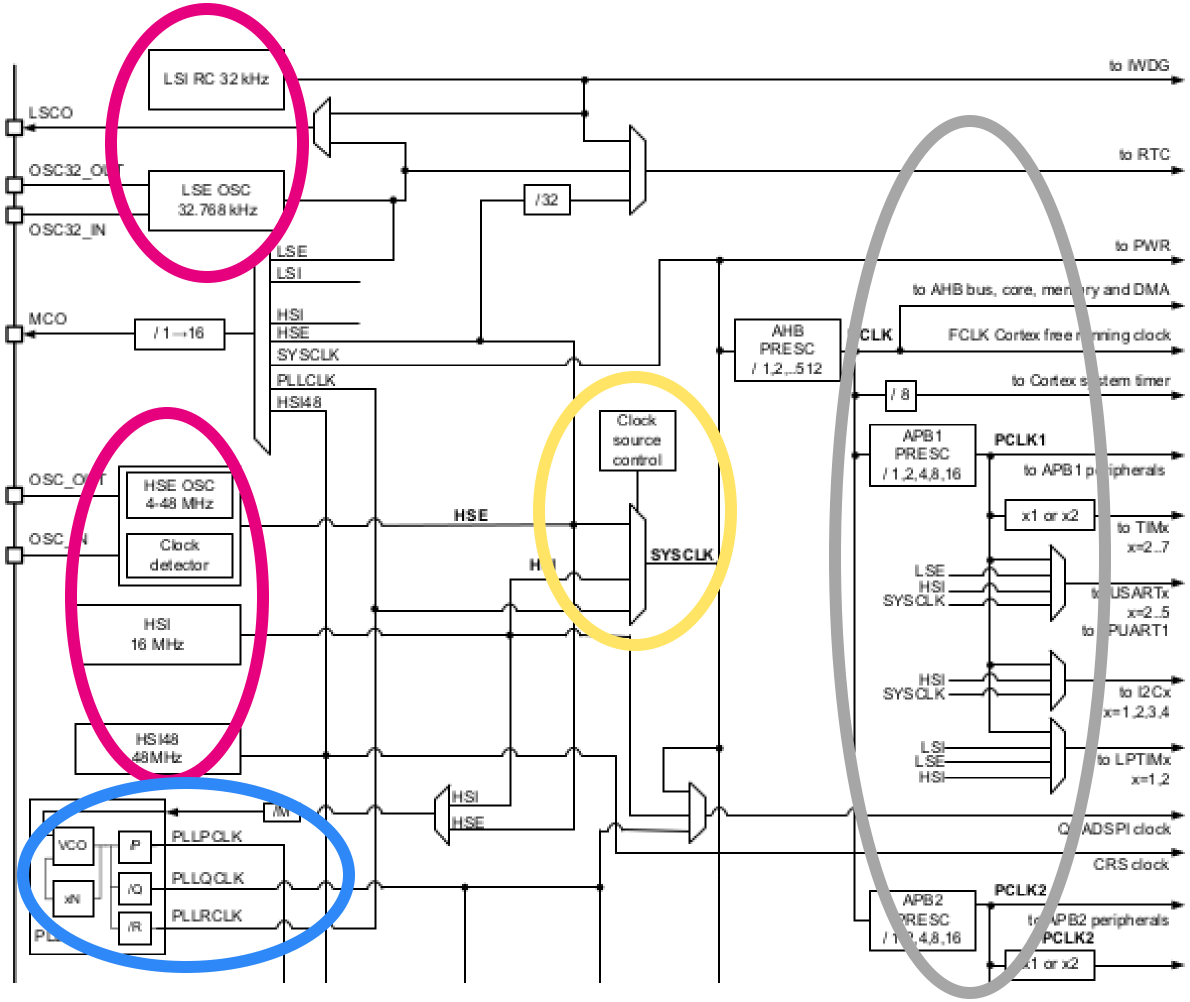
Clock tree settings



Fixed clocks

High Speed (Internal, External)

Configurable clocks

Low speed, ..

PLL(s)

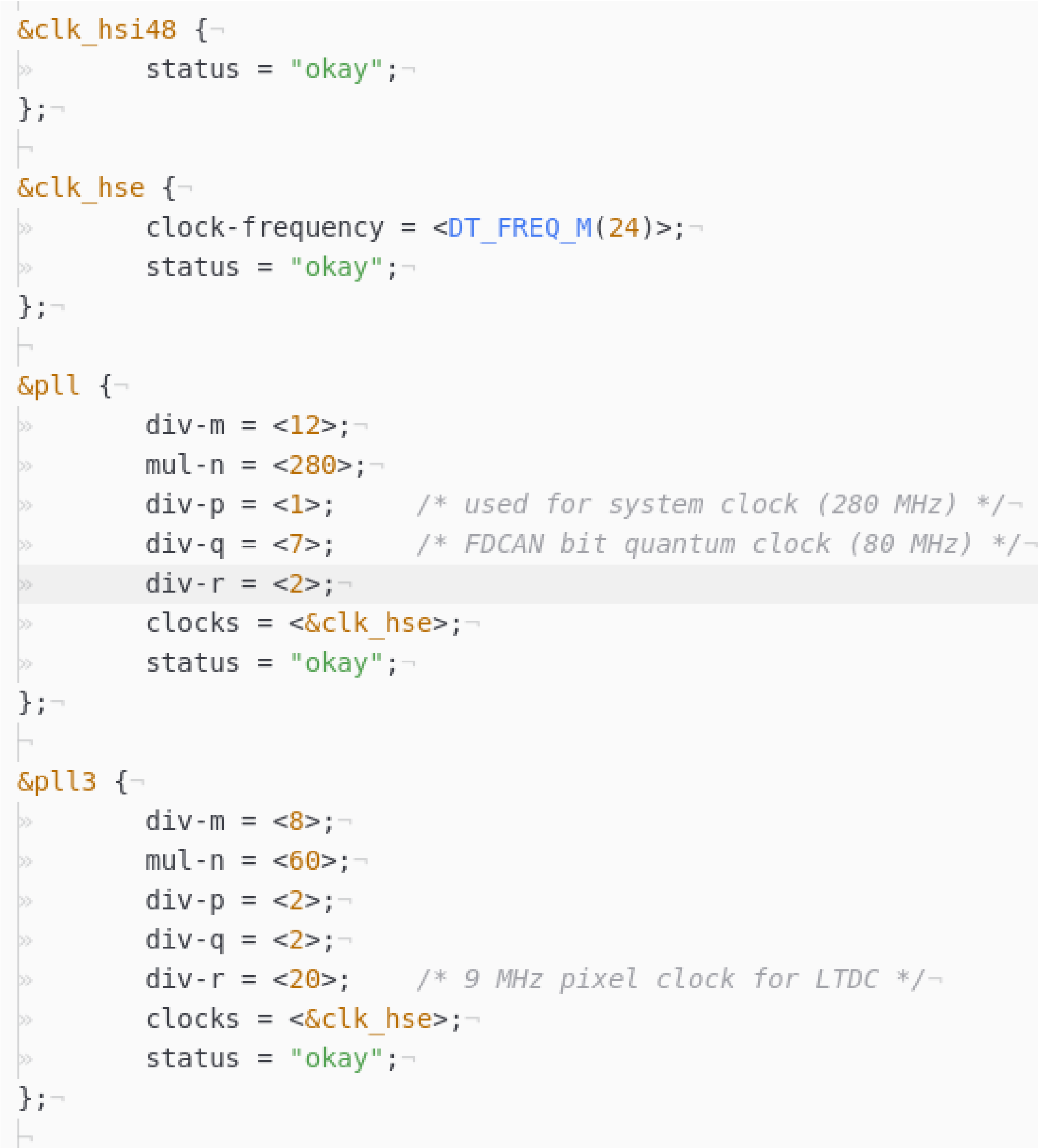
Input: multiplier, divisor

Output clocks (PLL P, PLL Q, ..) and division factors

Core source clock

Peripheral bus speeds

STM32 clock configuration with device tree

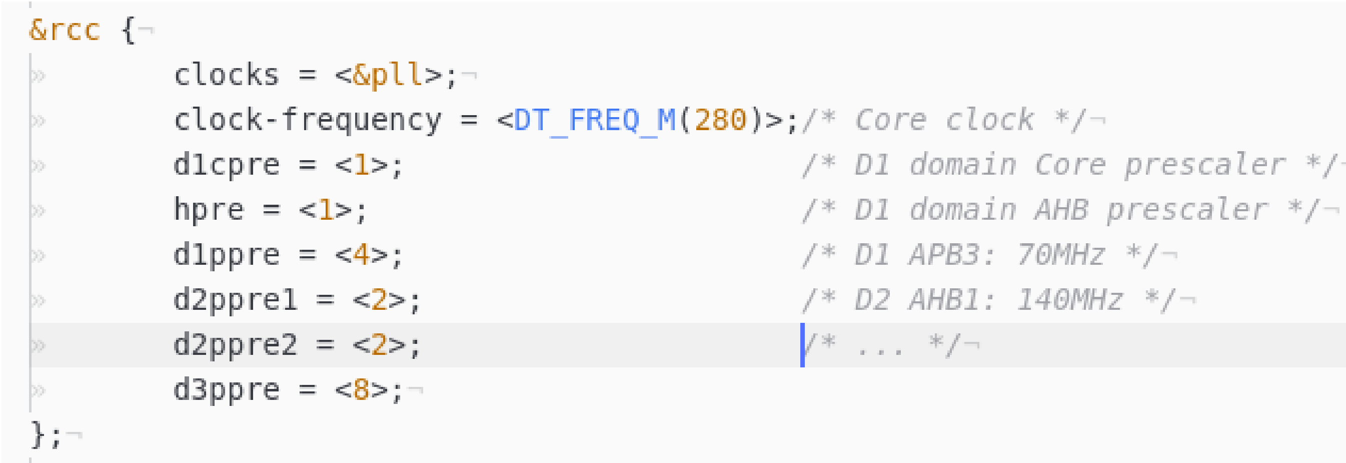


```
&clk_hsi48 {
	status = "okay";
};

&clk_hse {
	clock-frequency = <DT_FREQ_M(24)>;
	status = "okay";
};

&pll {
	div-m = <12>;
	mul-n = <280>;
	div-p = <1>;	/* used for system clock (280 MHz) */
	div-q = <7>;	/* FDCAN bit quantum clock (80 MHz) */
	div-r = <2>;
	clocks = <&clk_hse>;
	status = "okay";
};

&pll3 {
	div-m = <8>;
	mul-n = <60>;
	div-p = <2>;
	div-q = <2>;
	div-r = <20>;	/* 9 MHz pixel clock for LTDC */
	clocks = <&clk_hse>;
	status = "okay";
};
```

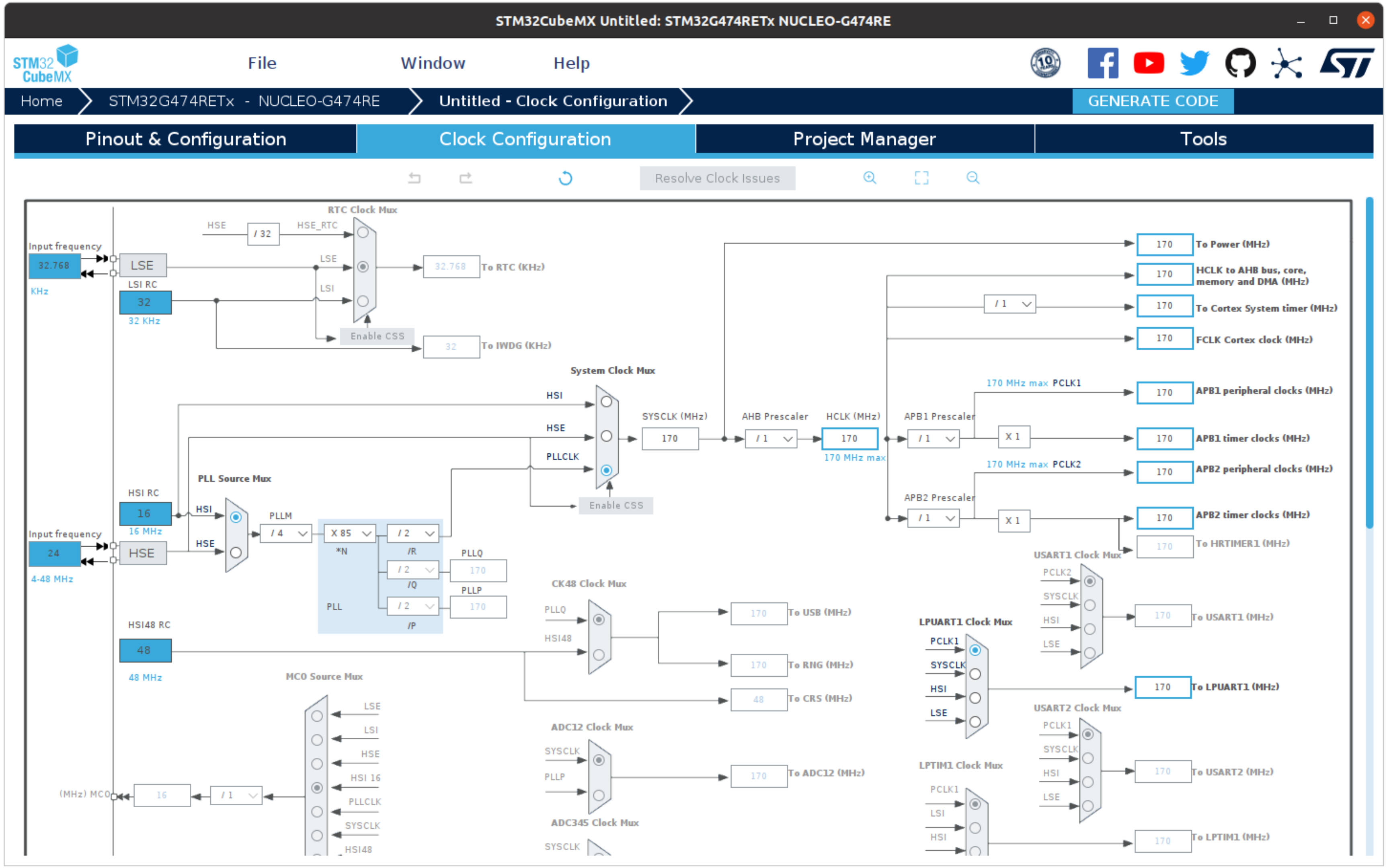


```
&rcc {
	clocks = <&pll>;
	clock-frequency = <DT_FREQ_M(280)>;/* Core clock */
	d1cpre = <1>;			/* D1 domain Core prescaler */
	hpre = <1>;			/* D1 domain AHB prescaler */
	d1ppre = <4>;			/* D1 APB3: 70MHz */
	d2ppre1 = <2>;			/* D2 AHB1: 140MHz */
	d2ppre2 = <2>;			/* ... */
	d3ppre = <8>;
};
```

More information on https://docs.zephyrproject.org/latest/build/dts/api/bindings.html#stmicroelectronics-st

Need help on clocks ?

- Reference manuals
- STM32CubeMX



3- Configure peripherals

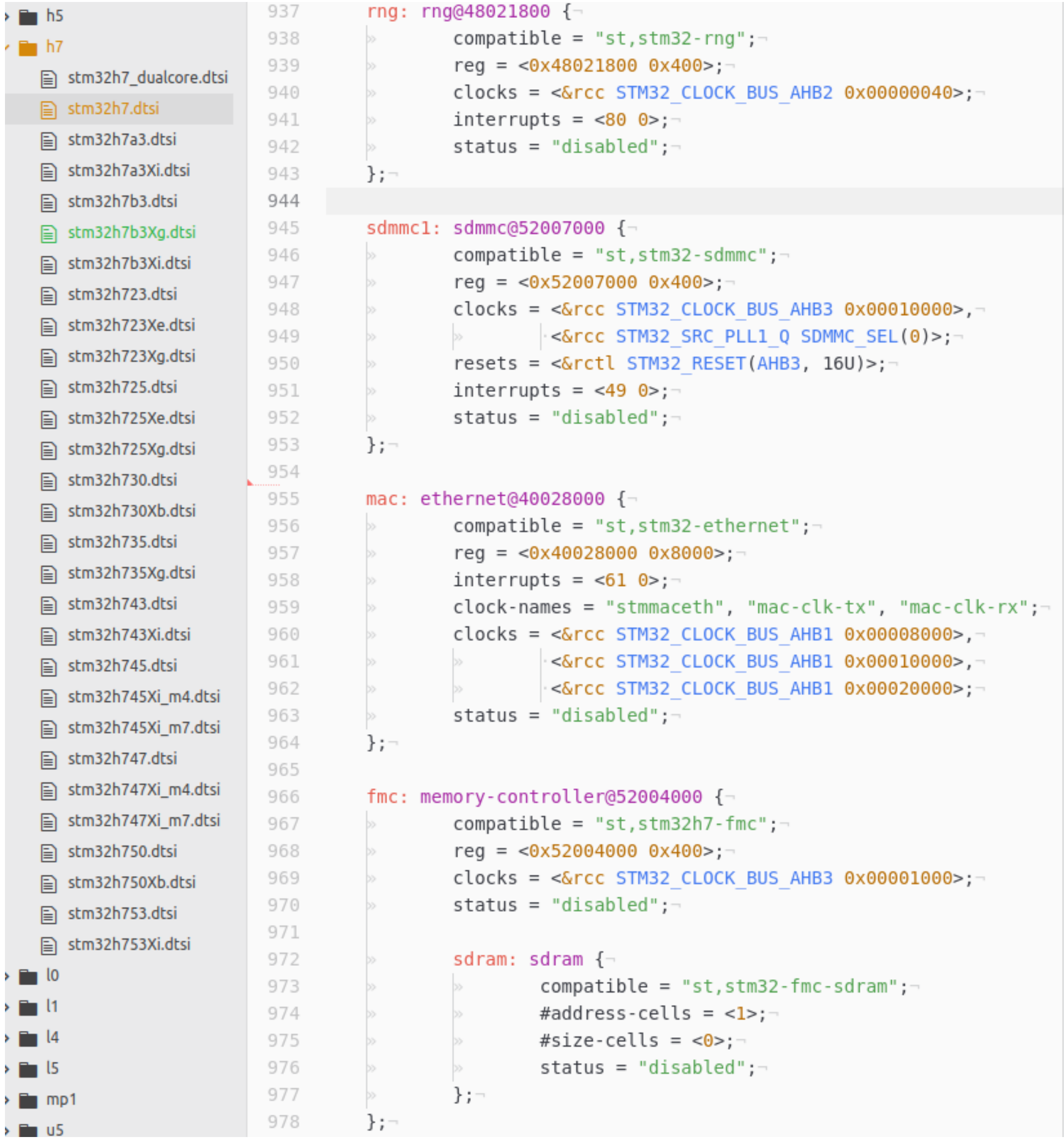
What are the peripherals supported ?

What are the configurations supported for this peripheral ?

How to configure usual settings (pinctrl, domain clocks, DMA) ?

Supported peripherals

- Device tree is the main reference:
  - dts/arm/st/<my_series>
  - Start from <my_part>.dtsi file
  - Follow inclusions up to series root file
- Missing instance of device
  - Add missing node.
  - Get config info from CMSIS files
- Missing device
  - Check for support in a compatible series



```
h5
h7
    stm32h7_dualcore.dtsi
    stm32h7.dtsi
    stm32h7a3.dtsi
    stm32h7a3Xi.dtsi
    stm32h7b3.dtsi
    stm32h7b3Xg.dtsi
    stm32h7b3Xi.dtsi
    stm32h723.dtsi
    stm32h723Xe.dtsi
    stm32h723Xg.dtsi
    stm32h725.dtsi
    stm32h725Xe.dtsi
    stm32h725Xg.dtsi
    stm32h730.dtsi
    stm32h730Xb.dtsi
    stm32h735.dtsi
    stm32h735Xg.dtsi
    stm32h743.dtsi
    stm32h743Xi.dtsi
    stm32h745.dtsi
    stm32h745Xi_m4.dtsi
    stm32h745Xi_m7.dtsi
    stm32h747.dtsi
    stm32h747Xi_m4.dtsi
    stm32h747Xi_m7.dtsi
    stm32h750.dtsi
    stm32h750Xb.dtsi
    stm32h753.dtsi
    stm32h753Xi.dtsi
l0
l1
l4
l5
mp1
u5
```

```
rng: rng@48021800 {
		compatible = "st,stm32-rng";
		reg = <0x48021800 0x400>;
		clocks = <&rcc STM32_CLOCK_BUS_AHB2 0x00000040>;
		interrupts = <80 0>;
		status = "disabled";
};

sdmmc1: sdmmc@52007000 {
		compatible = "st,stm32-sdmmc";
		reg = <0x52007000 0x400>;
		clocks = <&rcc STM32_CLOCK_BUS_AHB3 0x00010000>,
			 <&rcc STM32_SRC_PLL1_Q SDMMC_SEL(0)>;
		resets = <&rctl STM32_RESET(AHB3, 16U)>;
		interrupts = <49 0>;
		status = "disabled";
};

mac: ethernet@40028000 {
		compatible = "st,stm32-ethernet";
		reg = <0x40028000 0x8000>;
		interrupts = <61 0>;
		clock-names = "stmmaceth", "mac-clk-tx", "mac-clk-rx";
		clocks = <&rcc STM32_CLOCK_BUS_AHB1 0x00008000>,
			 <&rcc STM32_CLOCK_BUS_AHB1 0x00010000>,
			 <&rcc STM32_CLOCK_BUS_AHB1 0x00020000>;
		status = "disabled";
};

fmc: memory-controller@52004000 {
		compatible = "st,stm32h7-fmc";
		reg = <0x52004000 0x400>;
		clocks = <&rcc STM32_CLOCK_BUS_AHB3 0x00001000>;
		status = "disabled";

		sdram: sdram {
			compatible = "st,stm32-fmc-sdram";
			#address-cells = <1>;
			#size-cells = <0>;
			status = "disabled";
		};
};
```

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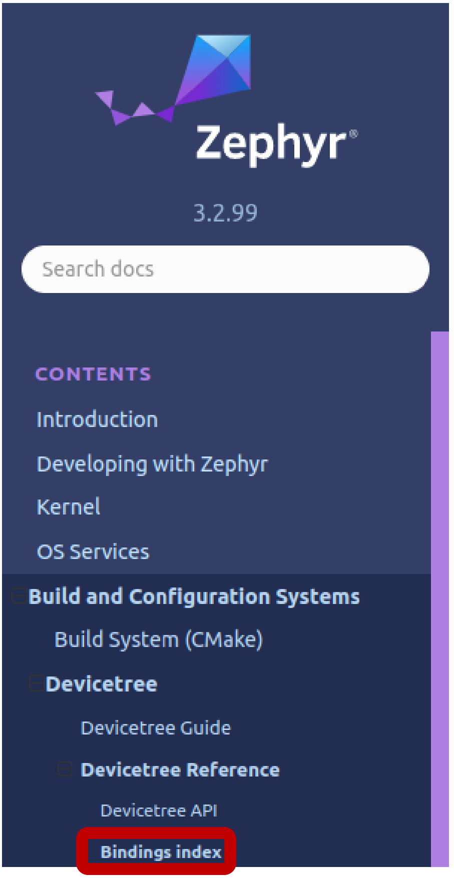
Zephyr

Device configuring options



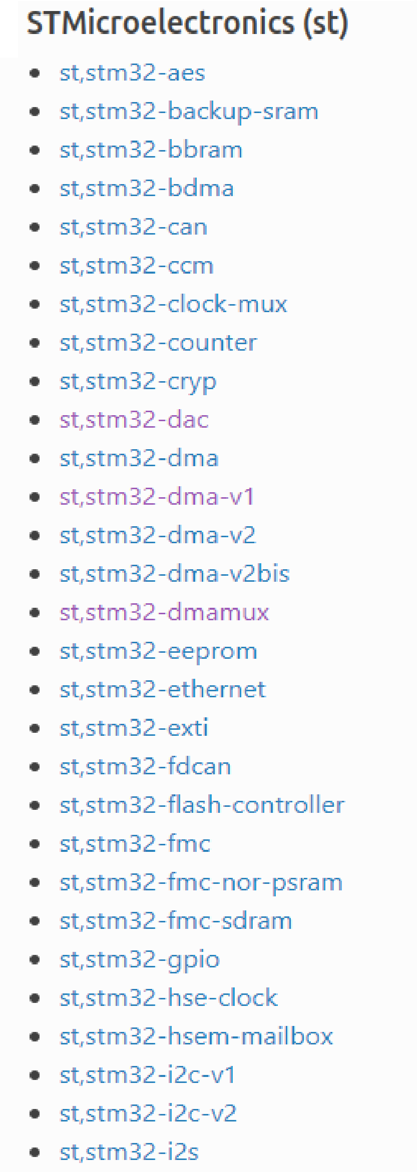
Zephyr

3.2.99

Search docs

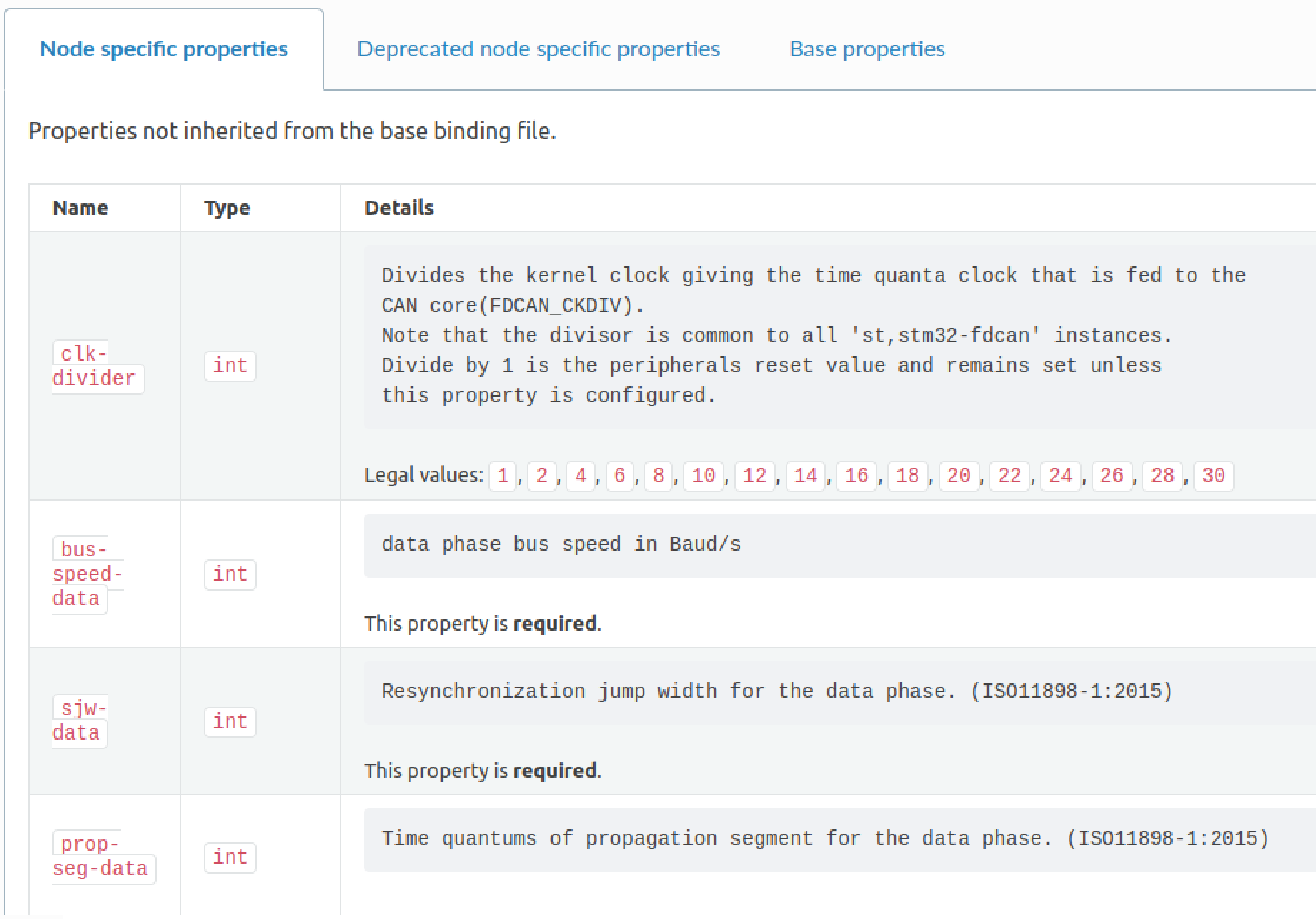
CONTENTS

- Introduction
- Developing with Zephyr
- Kernel
- OS Services
- **Build and Configuration Systems**
  - Build System (CMake)
  - **Devicetree**
    - Devicetree Guide
    - **Devicetree Reference**
      - Devicetree API
      - **Bindings index**



STMicroelectronics (st)

- st,stm32-aes
- st,stm32-backup-sram
- st,stm32-bbram
- st,stm32-bdma
- st,stm32-can
- st,stm32-ccm
- st,stm32-clock-mux
- st,stm32-counter
- st,stm32-cryp
- st,stm32-dac
- st,stm32-dma
- st,stm32-dma-v1
- st,stm32-dma-v2
- st,stm32-dma-v2bis
- st,stm32-dmamux
- st,stm32-eeprom
- st,stm32-ethernet
- st,stm32-exti
- st,stm32-fdcan
- st,stm32-flash-controller
- st,stm32-fmc
- st,stm32-fmc-nor-psram
- st,stm32-fmc-sdram
- st,stm32-gpio
- st,stm32-hse-clock
- st,stm32-hsem-mailbox
- st,stm32-i2c-v1
- st,stm32-i2c-v2
- st,stm32-i2s



Node specific properties | Deprecated node specific properties | Base properties

Properties not inherited from the base binding file.

Name	Type	Details
clk-divider	int	Divides the kernel clock giving the time quanta clock that is fed to the CAN core(FDCAN_CKDIV). Note that the divisor is common to all 'st,stm32-fdcan' instances. Divide by 1 is the peripherals reset value and remains set unless this property is configured. Legal values: 1, 2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24, 26, 28, 30
bus-speed-data	int	data phase bus speed in Baud/s This property is **required**.
sjw-data	int	Resynchronization jump width for the data phase. (ISO11898-1:2015) This property is **required**.
prop-seg-data	int	Time quantums of propagation segment for the data phase. (ISO11898-1:2015)

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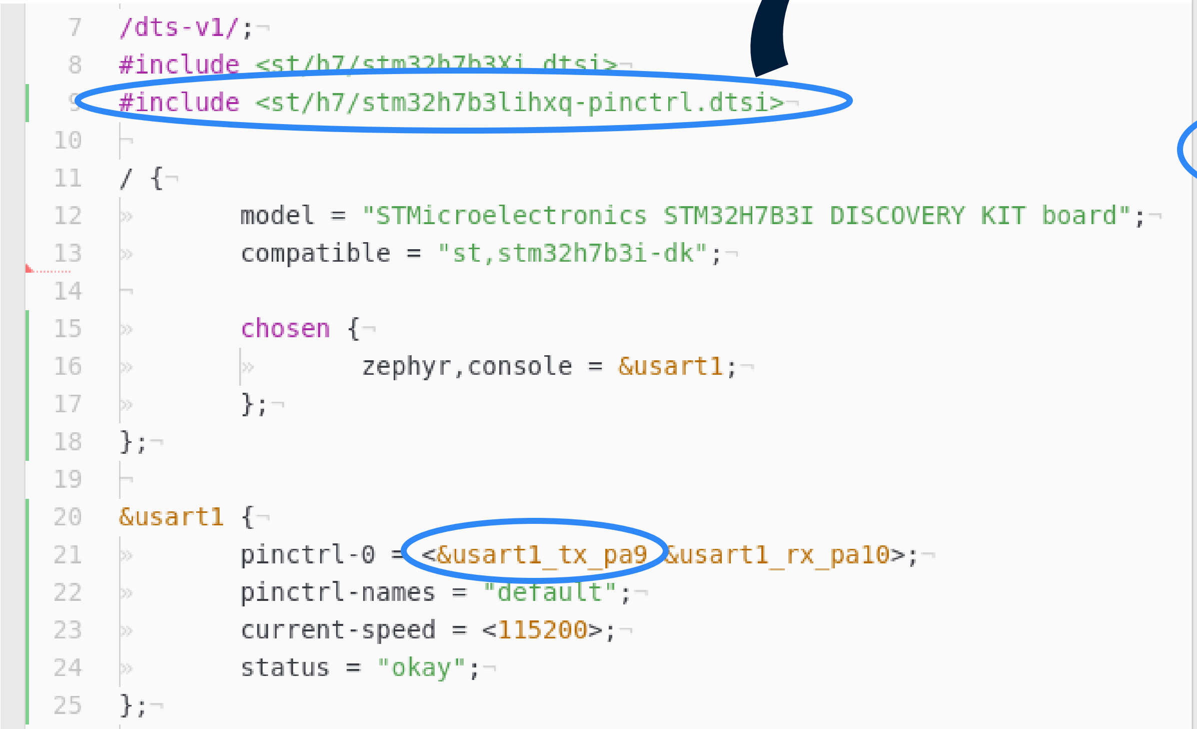
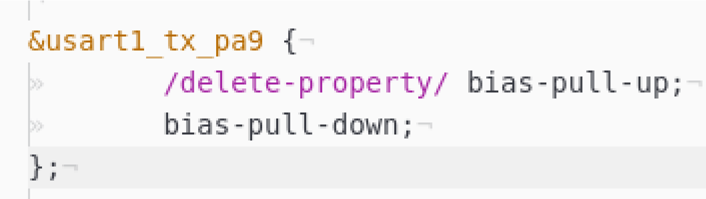
.org

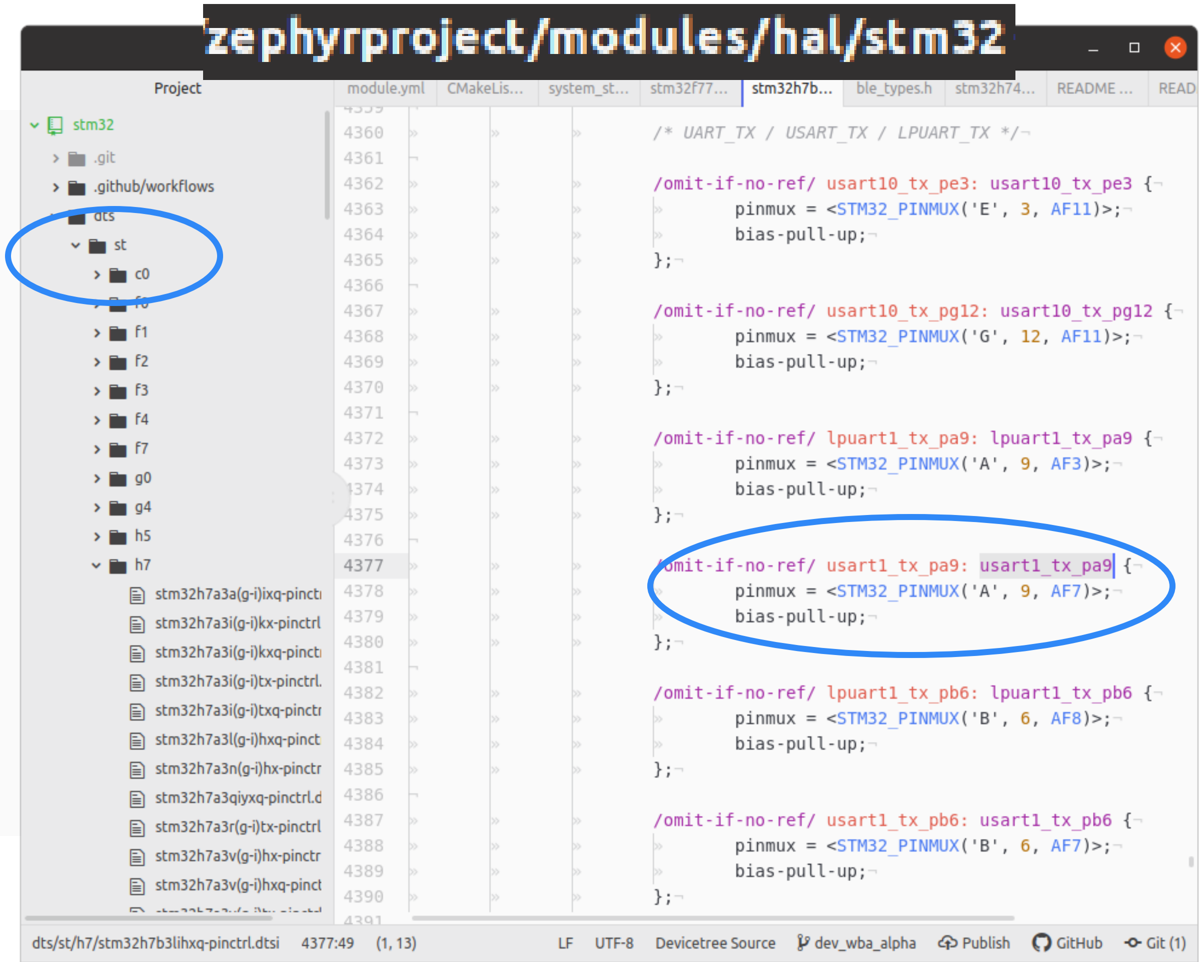
Common STM32 device settings: pinctrl



```
/dts-v1/;
#include <st/h7/stm32h7b3Xi.dtsi>
#include <st/h7/stm32h7b3lihxq-pinctrl.dtsi>

/ {
	model = "STMicroelectronics STM32H7B3I DISCOVERY KIT board";
	compatible = "st,stm32h7b3i-dk";

	chosen {
		zephyr,console = &usart1;
	};
};

&usart1 {
	pinctrl-0 = <&usart1_tx_pa9 &usart1_rx_pa10>;
	pinctrl-names = "default";
	current-speed = <115200>;
	status = "okay";
};
```



```
&usart1_tx_pa9 {
	/delete-property/ bias-pull-up;
	bias-pull-down;
};
```

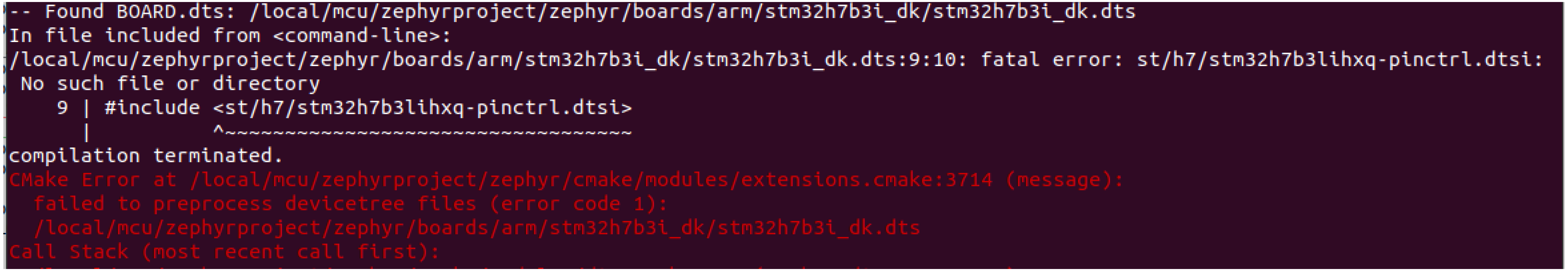


```
			/* UART_TX / USART_TX / LPUART_TX */

			/omit-if-no-ref/ usart10_tx_pe3: usart10_tx_pe3 {
				pinmux = <STM32_PINMUX('E', 3, AF11)>;
				bias-pull-up;
			};

			/omit-if-no-ref/ usart10_tx_pg12: usart10_tx_pg12 {
				pinmux = <STM32_PINMUX('G', 12, AF11)>;
				bias-pull-up;
			};

			/omit-if-no-ref/ lpuart1_tx_pa9: lpuart1_tx_pa9 {
				pinmux = <STM32_PINMUX('A', 9, AF3)>;
				bias-pull-up;
			};

			/omit-if-no-ref/ usart1_tx_pa9: usart1_tx_pa9 {
				pinmux = <STM32_PINMUX('A', 9, AF7)>;
				bias-pull-up;
			};

			/omit-if-no-ref/ lpuart1_tx_pb6: lpuart1_tx_pb6 {
				pinmux = <STM32_PINMUX('B', 6, AF8)>;
				bias-pull-up;
			};

			/omit-if-no-ref/ usart1_tx_pb6: usart1_tx_pb6 {
				pinmux = <STM32_PINMUX('B', 6, AF7)>;
				bias-pull-up;
			};
```

Available in https://github.com/zephyrproject-rtos/hal_stm32
Generated from https://github.com/STMicroelectronics/STM32_open_pin_data

Additional points on pinctrl

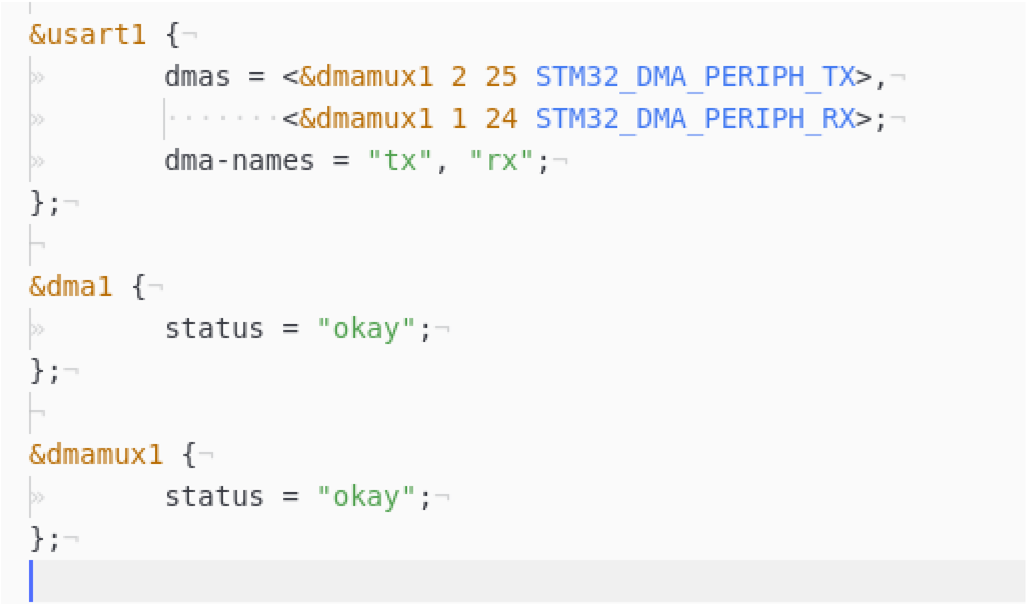
- If you’re getting following error, run `west update`



```
-- Found BOARD.dts: /local/mcu/zephyrproject/zephyr/boards/arm/stm32h7b3i_dk/stm32h7b3i_dk.dts
In file included from <command-line>:
/local/mcu/zephyrproject/zephyr/boards/arm/stm32h7b3i_dk/stm32h7b3i_dk.dts:9:10: fatal error: st/h7/stm32h7b3lihxq-pinctrl.dtsi:
 No such file or directory
    9 | #include <st/h7/stm32h7b3lihxq-pinctrl.dtsi>
      |          ^~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~
compilation terminated.
CMake Error at /local/mcu/zephyrproject/zephyr/cmake/modules/extensions.cmake:3714 (message):
  failed to preprocess devicetree files (error code 1):
  /local/mcu/zephyrproject/zephyr/boards/arm/stm32h7b3i_dk/stm32h7b3i_dk.dts
Call Stack (most recent call first):
```

- Pinctrl can also be used to enable MCO
  - See STM32: Configure MCO pin through device tree pinctrl · Issue #31912 · zephyrproject-rtos/zephyr (github.com)

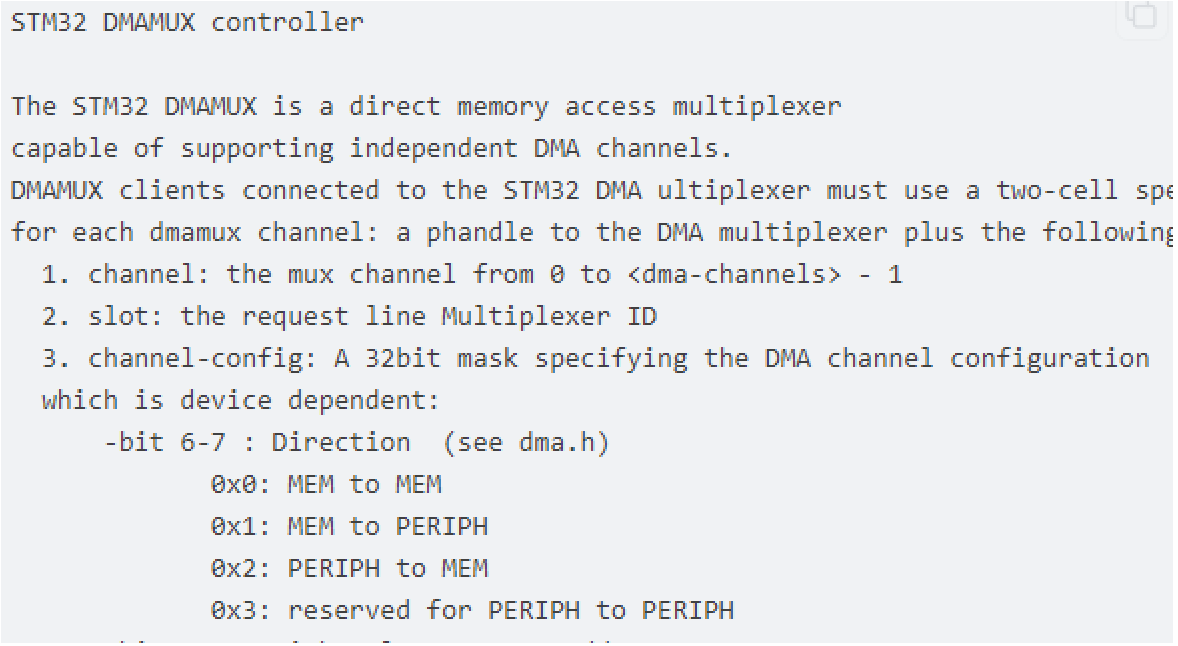
Common STM32 device settings: DMA



```
&usart1 {
	dmas = <&dmamux1 2 25 STM32_DMA_PERIPH_TX>,
	       <&dmamux1 1 24 STM32_DMA_PERIPH_RX>;
	dma-names = "tx", "rx";
};

&dma1 {
	status = "okay";
};

&dmamux1 {
	status = "okay";
};
```

- DMA is enabled based on “dmas” prop
- Config depends on dma “compatible”:
  - st,stm32-dma-v1
  - st,stm32-dma-v2
  - st,stm32-dma-v2bis
  - st,stm32-dmamux

- See Bindings section in docs.zephyrproject.org: st,stm32-dmamux

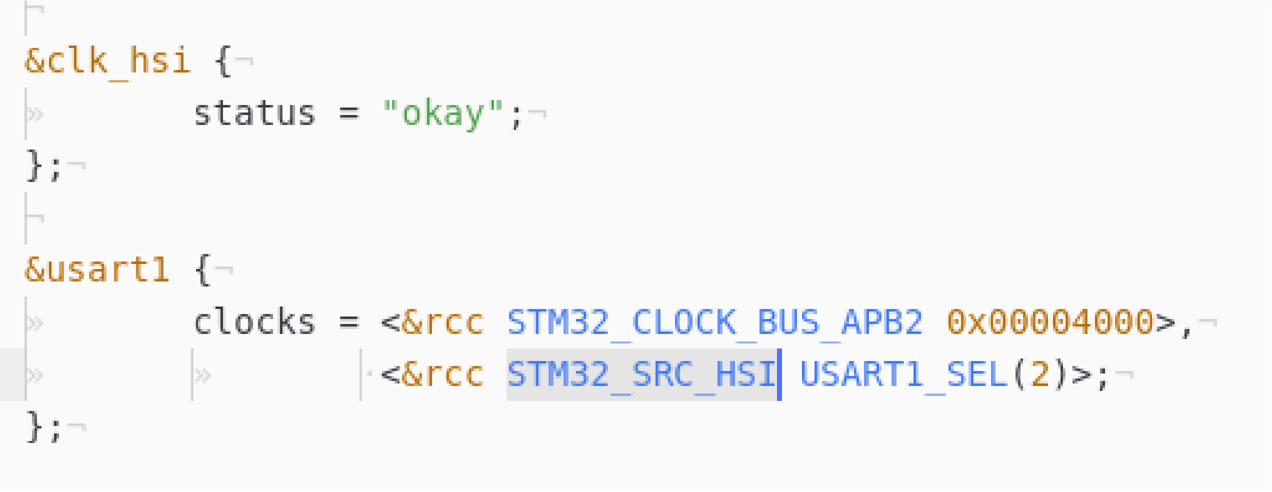


```
STM32 DMAMUX controller

The STM32 DMAMUX is a direct memory access multiplexer
capable of supporting independent DMA channels.
DMAMUX clients connected to the STM32 DMA ultiplexer must use a two-cell spe
for each dmamux channel: a phandle to the DMA multiplexer plus the following
  1. channel: the mux channel from 0 to <dma-channels> - 1
  2. slot: the request line Multiplexer ID
  3. channel-config: A 32bit mask specifying the DMA channel configuration
  which is device dependent:
      -bit 6-7 : Direction  (see dma.h)
             0x0: MEM to MEM
             0x1: MEM to PERIPH
             0x2: PERIPH to MEM
             0x3: reserved for PERIPH to PERIPH
```

- Note:
  - Plan to configure dma device props in .dtsi files
  - DMA support has to be checked directly in drivers

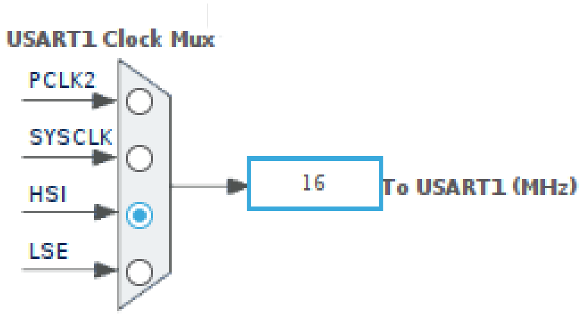
Common STM32 device settings: domain clock

- Use cases:
  - Select a 48MHz clock
  - Select a specific PLL output
  - Select a clock persistent in Stop Mode



```
&clk_hsi {
	status = "okay";
};

&usart1 {
	clocks = <&rcc STM32_CLOCK_BUS_APB2 0x00004000>,
		 <&rcc STM32_SRC_HSI USART1_SEL(2)>;
};
```

- STM32CubeMx:



Note: Analog pinctrl configurations are available for all pins

Power Management

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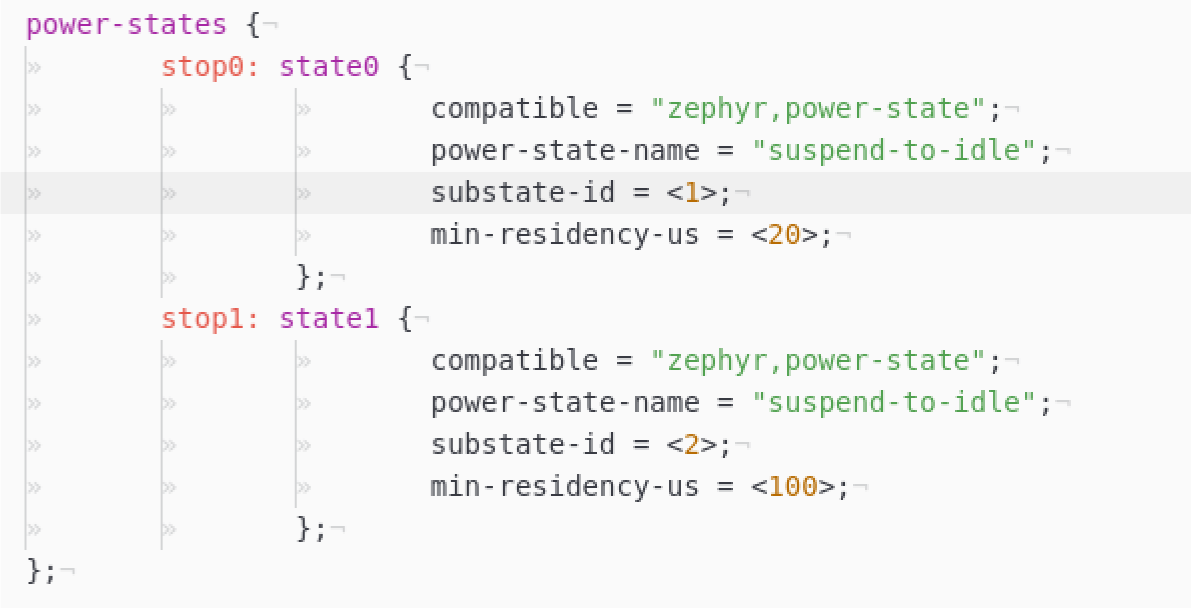
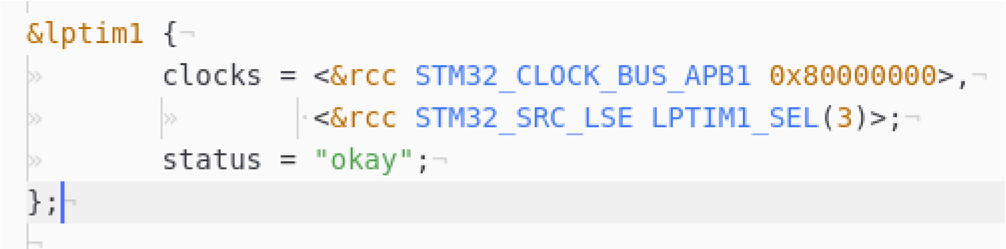
STM32 Power Management – SoC level

- PM handling is made available per series basis
  - In /soc/arm/st_stm32/stm32yy/power.c
  - In .dtsi:



```
power-states {
        stop0: state0 {
                        compatible = "zephyr,power-state";
                        power-state-name = "suspend-to-idle";
                        substate-id = <1>;
                        min-residency-us = <20>;
                };
        stop1: state1 {
                        compatible = "zephyr,power-state";
                        power-state-name = "suspend-to-idle";
                        substate-id = <2>;
                        min-residency-us = <100>;
                };
};
```

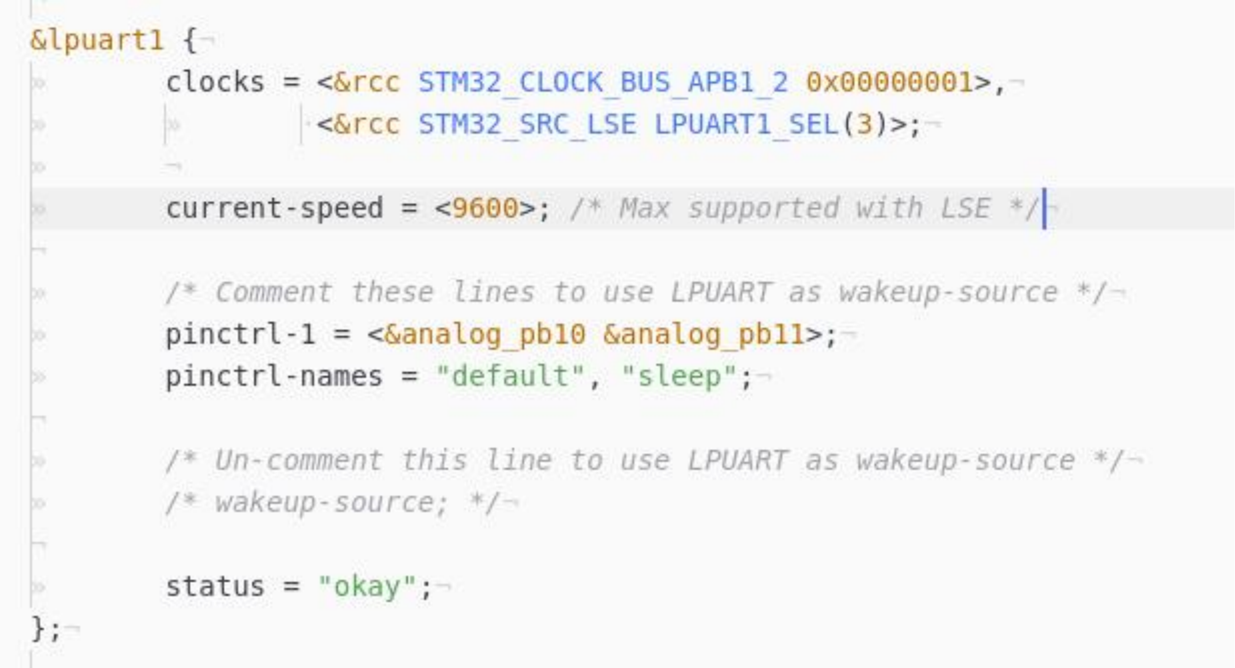
- Requires a kernel tick source available when core clock is gated
  - LPTIM used automatically when CONFIG_PM=y
  - Requires:



```
&lptim1 {
        clocks = <&rcc STM32_CLOCK_BUS_APB1 0x80000000>,
                 <&rcc STM32_SRC_LSE LPTIM1_SEL(3)>;
        status = "okay";
};
```

STM32 Power Management – Device level

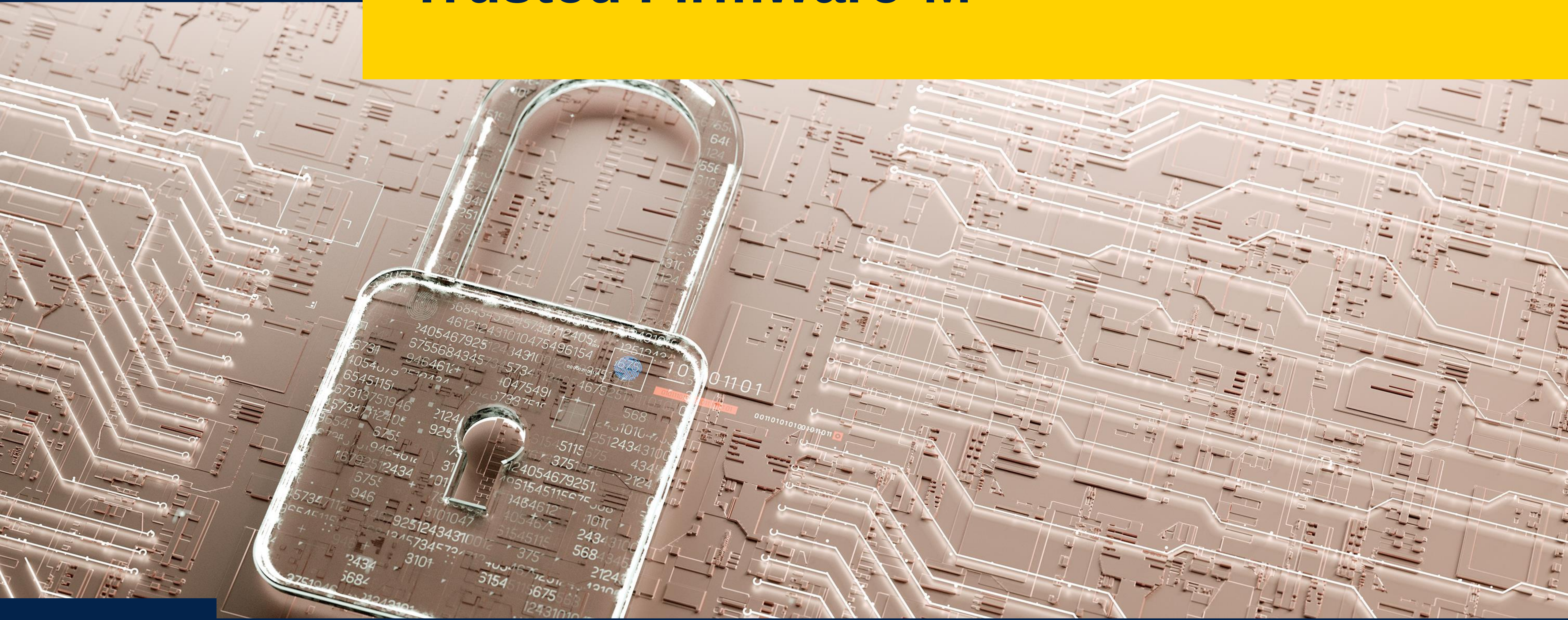
- CONFIG_PM_DEVICE support in GPIO, UART, I2C
- PM samples available on STM32 PM samples
- Example of LP-UART device configuration:

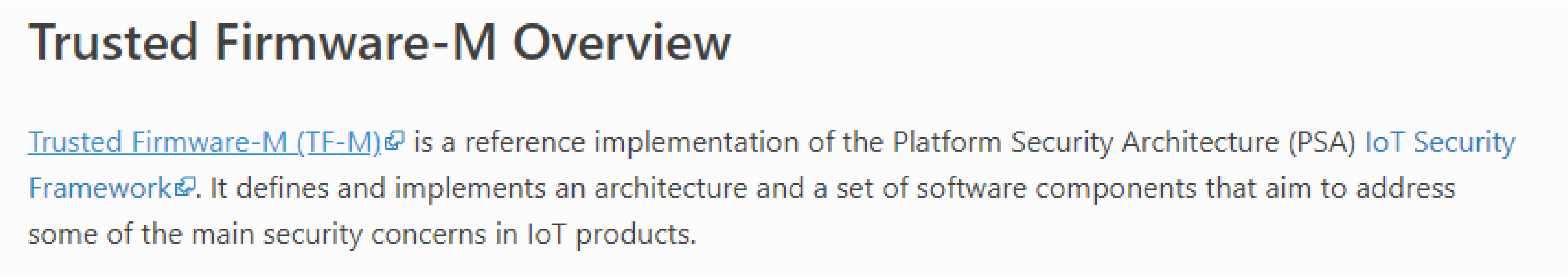


```
&lpuart1 {
        clocks = <&rcc STM32_CLOCK_BUS_APB1_2 0x00000001>,
                 <&rcc STM32_SRC_LSE LPUART1_SEL(3)>;

        current-speed = <9600>; /* Max supported with LSE */

        /* Comment these lines to use LPUART as wakeup-source */
        pinctrl-1 = <&analog_pb10 &analog_pb11>;
        pinctrl-names = "default", "sleep";

        /* Un-comment this line to use LPUART as wakeup-source */
        /* wakeup-source; */

        status = "okay";
};
```

Note: Analog pinctrl configurations are available for all pins

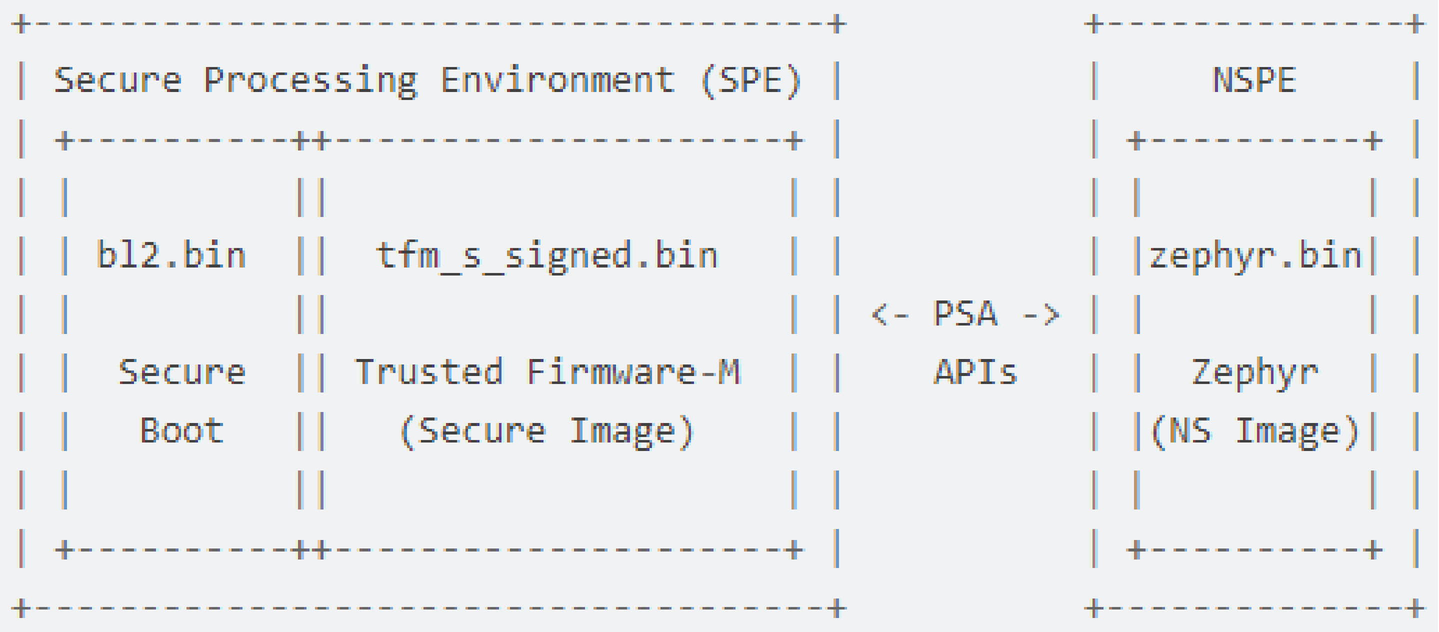
Trusted Firmware-M





Trusted Firmware-M Overview

Trusted Firmware-M (TF-M) is a reference implementation of the Platform Security Architecture (PSA) IoT Security Framework. It defines and implements an architecture and a set of software components that aim to address some of the main security concerns in IoT products.

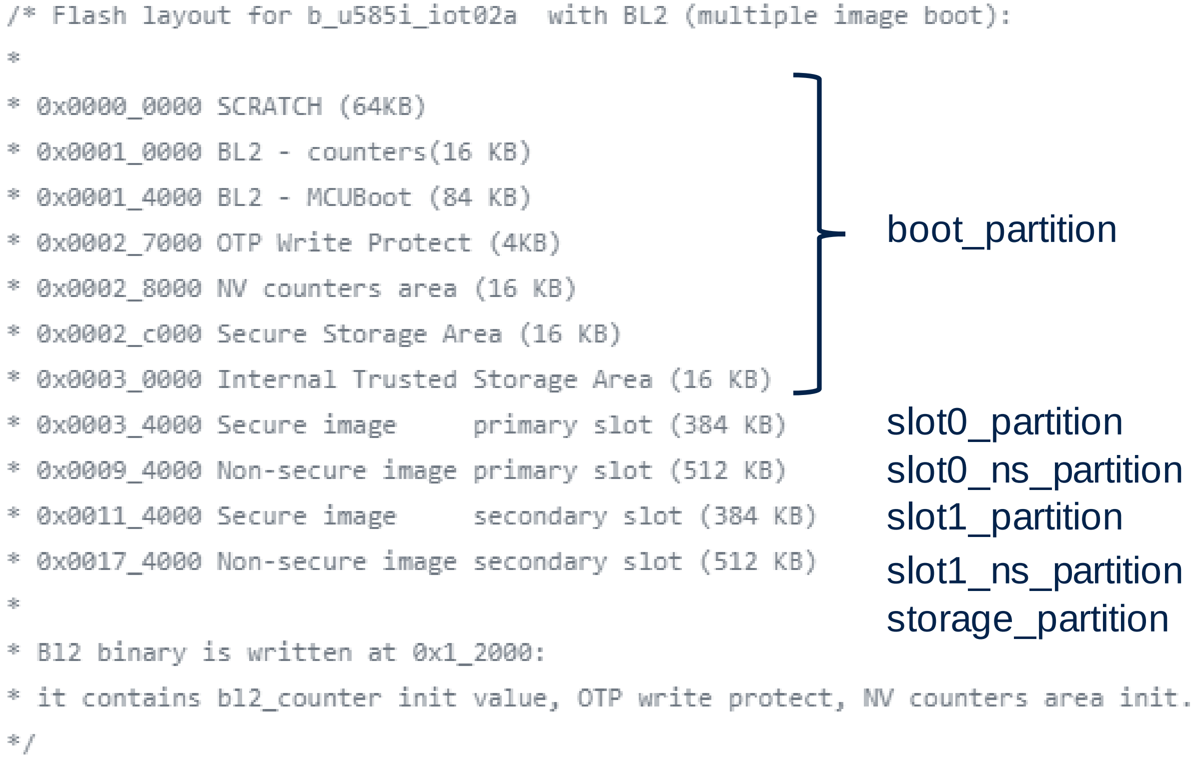


```
+-------------------------------------+           +--------------+
| Secure Processing Environment (SPE) |           |     NSPE     |
| +----------++---------------------+ |           | +----------+ |
| |          ||                     | |           | |          | |
| | bl2.bin  ||  tfm_s_signed.bin   | |           | |zephyr.bin| |
| |          ||                     | | <- PSA -> | |          | |
| |  Secure  || Trusted Firmware-M  | |    APIs   | |  Zephyr  | |
| |   Boot   ||   (Secure Image)    | |           | |(NS Image)| |
| |          ||                     | |           | |          | |
| +----------++---------------------+ |           | +----------+ |
+-------------------------------------+           +--------------+
```

https://docs.zephyrproject.org/latest/services/tfm/overview.html

Zephyr/TF-M on STM32

- Only STM32 platforms supported in Zephyr TF-M are supported
- Partitioning is defined in TF-M: platform/ext/target/stm/b_u585i_iot02a/include/flash_layout.h



```
/* Flash layout for b_u585i_iot02a  with BL2 (multiple image boot):
*
* 0x0000_0000 SCRATCH (64KB)
* 0x0001_0000 BL2 - counters(16 KB)
* 0x0001_4000 BL2 - MCUBoot (84 KB)
* 0x0002_7000 OTP Write Protect (4KB)
* 0x0002_8000 NV counters area (16 KB)
* 0x0002_c000 Secure Storage Area (16 KB)
* 0x0003_0000 Internal Trusted Storage Area (16 KB)
* 0x0003_4000 Secure image     primary slot (384 KB)
* 0x0009_4000 Non-secure image primary slot (512 KB)
* 0x0011_4000 Secure image     secondary slot (384 KB)
* 0x0017_4000 Non-secure image secondary slot (512 KB)
*
* Bl2 binary is written at 0x1_2000:
* it contains bl2_counter init value, OTP write protect, NV counters area init.
*/
```

boot_partition

slot0_partition
slot0_ns_partition
slot1_partition
slot1_ns_partition
storage_partition

Next steps and conclusion

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Next steps

- PM extension/completion
- XIP on External memories
- Stick with Zephyr evolutions (USB, DMA, ..)
- Backlog

Jump in!

Contribute your changes and fixes

Watch changes on the areas you care about

Take part in reviews ~50 PR/month > Help welcome ;-)

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Questions ?

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Thank you

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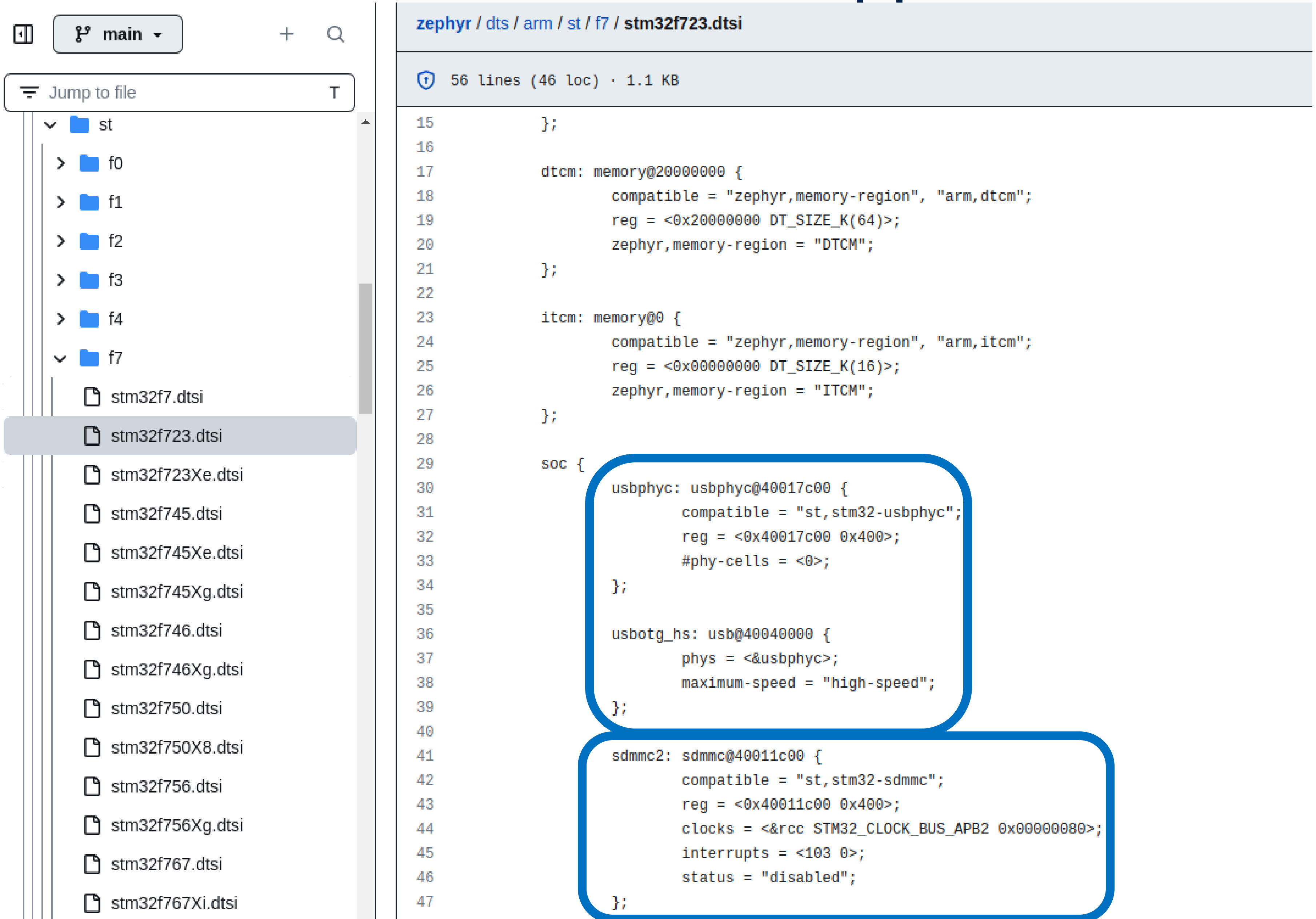
Supported on STM32



- st
  - f0
  - f1
  - f2
  - f3
  - f4
  - f7
    - stm32f7.dtsi
    - stm32f723.dtsi
    - stm32f723Xe.dtsi
    - stm32f745.dtsi
    - stm32f745Xe.dtsi
    - stm32f745Xg.dtsi
    - stm32f746.dtsi
    - stm32f746Xg.dtsi
    - stm32f750.dtsi
    - stm32f750X8.dtsi
    - stm32f756.dtsi
    - stm32f756Xg.dtsi
    - stm32f767.dtsi
    - stm32f767Xi.dtsi

zephyr / dts / arm / st / f7 / **stm32f723.dtsi**

56 lines (46 loc) · 1.1 KB

```
        };

        dtcm: memory@20000000 {
                compatible = "zephyr,memory-region", "arm,dtcm";
                reg = <0x20000000 DT_SIZE_K(64)>;
                zephyr,memory-region = "DTCM";
        };

        itcm: memory@0 {
                compatible = "zephyr,memory-region", "arm,itcm";
                reg = <0x00000000 DT_SIZE_K(16)>;
                zephyr,memory-region = "ITCM";
        };

        soc {
                usbphyc: usbphyc@40017c00 {
                        compatible = "st,stm32-usbphyc";
                        reg = <0x40017c00 0x400>;
                        #phy-cells = <0>;
                };

                usbotg_hs: usb@40040000 {
                        phys = <&usbphyc>;
                        maximum-speed = "high-speed";
                };

                sdmmc2: sdmmc@40011c00 {
                        compatible = "st,stm32-sdmmc";
                        reg = <0x40011c00 0x400>;
                        clocks = <&rcc STM32_CLOCK_BUS_APB2 0x00000080>;
                        interrupts = <103 0>;
                        status = "disabled";
                };
```

For further support in creating a PowerPoint presentation, including graphic assets, formatting tools and additional information on the ST brand

you can visit the ST Brand Portal
https://brandportal.st.com

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