



Zephyr® Project
Developer Summit 2022

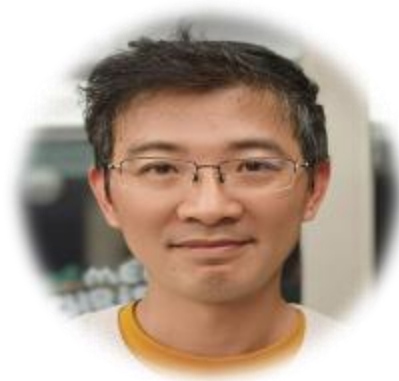
Building the traceability for design and testing in Zephyr

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Introduction

- What is traceability
- Why we need traceability
- How we propose to do that
- Conclusion

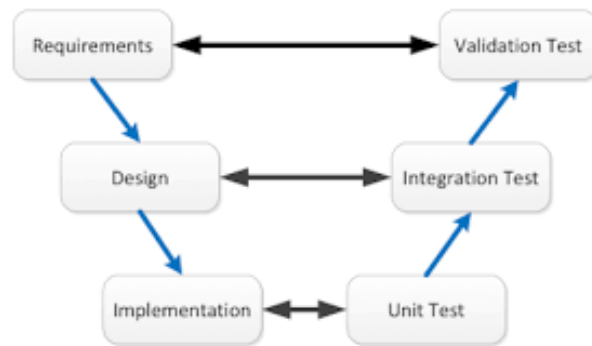


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Zephyr OS developer

What is traceability

- Requirement \Leftrightarrow Design \Leftrightarrow Tests
 - Requirement : RTOS features
 - Design: Zephyr Docs
 - Tests: testcases in Zephyr code
- Forward / backward traceability



V model

Why we need traceability

- User perspective
 - What features we can use in Zephyr RTOS?
 - Which platforms/boards support this feature?
 - How are their status/software quality?
 - Test Coverage and Test Results
- Developer perspective
 - How to use it: Build documentations, example samples or test cases.
 - Does it work well? Test results/report.

Open-Source Best Practices



USE OPEN-SOURCE TOOLS FOR
MANAGING EVERY ASPECT OF
THE PROJECT



KEEP THINGS CLOSE
TOGETHER

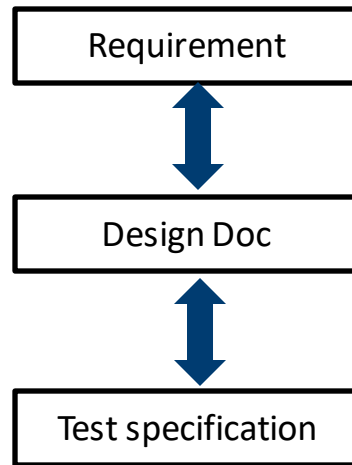


INTEGRATE WITH EXISTING
TOOLS

How we propose to do that

- Integrate into current documentations system
- The method of building traceability
 - Build the requirement docs
 - Refer to the existing design docs
 - Build the test specifications
 - Build the connections

Traceability



Integrate into Current Documentations System

- Zephyr documentations system is composed of :
 - Doxygen
 - Sphinx
- Put a section into Zephyr doc navigation pane, it is optional and includes subsections:
 - Software Requirements
 - Test specification
 - Traceability Matrix



Docs / Latest » Zephyr Project Documentation [Open on GitHub](#)

This is the documentation for the latest (main) development branch of Zephyr. If you are looking for the documentation of previous releases, use the drop-down menu on the left and select the desired version.

Zephyr Project Documentation

Welcome to the Zephyr Project's documentation for the main tree under development (version 3.1.0-rc2).

Use the version selection menu on the left to view documentation for a specific version of Zephyr.

For information about the changes and additions for releases, please consult the published [Release Notes](#) documentation.

The Zephyr OS is provided under the [Apache 2.0 license](#) (as found in the LICENSE file in the project's [GitHub repo](#)). The Zephyr OS also imports or reuses packages, scripts, and other files that use other licensing, as described in [Licensing of Zephyr Project components](#).

Introduction

Introducing the Zephyr Project: overview, architecture, features, and licensing

Getting Started Guide

Follow this guide to set up a Zephyr development environment on your system, and then build and run a sample application.

Contribution Guidelines

As an open-source project, we welcome and encourage the community to submit patches directly to the project.

Samples and Demos

A list of samples and demos that can run on a variety of boards supported by Zephyr

Zephyr Project v: latest

Build the Requirement Docs

- The Requirement docs need to be built.
- The requirements are usually the features of Zephyr RTOS.
- Ex. The spinlock of SMP support, the requirement might be:

“The system shall provide a mechanism for mutual exclusion between multiple physical CPUs using a traditional spinlock primitive.”

Requirement Docs

SMP

TRCSRS-199345 : Exclusion between physical CPUs

Primary Text - The system shall provide a mechanism for mutual exclusion between multiple physical CPUs using a traditional spinlock primitive.

TRCSRS-199346 : Running threads on specific CPUs

Primary Text - The system shall provide a mechanism for running threads on specific CPUs or sets of CPUs.

TRCSRS-199347 : Support operation on more than one CPU

Primary Text - The kernel shall support operation on more than one physical CPU sharing the same kernel state

C Library

TRCSRS-199366 : External C-Library

Primary Text - The system shall support external C library implementations

Fatal Exception Handling

TRCSRS-199348 : Fatal Exception Error Handler

Primary Text - The system shall provide handlers for fatal errors or exceptions that do not have a dedicated handler

Build the Test specification

- Test specification generate from the existing Doxygen descriptions of the testcase code.
- Need to add more descriptions of testcase code, Ex.

The doxygen tags

@brief

@details

- Precondition
- Expected output
- Pass and fail criteria
- Test case ID

Test specification

SMP
TEST_VAL_test_spinlock_mutual_exclusion
Result
RESULT_test_spinlock_mutual_exclusion not defined, broken link
Validates
TRCSRS-199345 : Exclusion between physical CPUs
<pre>void test_spinlock_mutual_exclusion(void)</pre>
Brief:
Test basic mutual exclusion using interrupt masking
Details:
Validate the spinlocks can be initialized at run-time. Validate the spinlocks in uniprocessor context should achieve mutual exclusion using interrupt masking.
Expected output:
The locked status after locking shall be true. The locked status after interrupt masking shall also be true. The locked status after unlocking shall be false.
Pass and fail criteria:
Pass: All the checkpoints are all passed.
Fail: Any one of the checkpoint is failed.
Testcase ID:
270201
TEST_VAL_test_threads_cpu_mask
TEST_VAL_test_threads_cpu_mask

Example:

Requirement ⇔ Design ⇔ Tests

Requirements

SMP

1 TRCSRS-199345 : Exclusion between physical CPUs

Fulfilled by

DESIGN_ARCH_spinlock_identical_interface : spinlocks works in uniprocessor and multiprocessor

DESIGN_ARCH_spinlock_irqlock : Spinlocks are non-recursive

DESIGN_ARCH_spinlock_support : basic function of spinlock

Validated by

TEST_VAL_test_spinlock_basic

TEST_VAL_test_spinlock_bounce_once

TEST_VAL_test_spinlock_mutual_exclusion

Primary Text - The system shall provide a mechanism for mutual exclusion between multiple physical CPUs using a traditional spinlock primitive.



Design Specification

resource. But that means that spinlocks must not be used recursively. Code that holds a specific lock must not try to re-acquire it or it will deadlock (it is perfectly legal to nest **distinct** spinlocks, however). A validation layer is available to detect and report bugs like this.

1 DESIGN_ARCH_spinlock_identical_interface : spinlocks works in uniprocessor and multiprocessor

Fulfills

TRCSRS-199345 : Exclusion between physical CPUs

When used on a uniprocessor system, the data component of the spinlock (the atomic lock variable) is unnecessary and elided. Except for the recursive semantics above, spinlocks in single-CPU contexts produce identical code to legacy IRQ locks. In fact the entirety of the Zephyr core kernel has now been ported to use spinlocks exclusively.

Legacy irq_lock() emulation

1 DESIGN_MODULE_IRQ_LOCK_APIS

1 DESIGN_ARCH_smp_global_lock : Provide compatible, global, recursive IRQ lock abstraction



Test Specification

1 TEST_VAL_test_spinlock_basic

```
void test_spinlock_basic(void)
```

Brief:

Test basic spinlock

Details:

Invoke k_spin_lock() and k_spin_unlock() API to lock/unlock and check if the locked status work correctly.

Expected output:

The locked status before locking shall be false. The locked status during locking shall be true. The locked status after unlocking shall be false again.

Pass and fail criteria:

Pass: All the checkpoints are all passed. The locked status before/during/after locking operations work as expected.

Fail: Any one of the checkpoint is failed.

Testcase ID:

270205

Traceability Matrix and Test Coverage

Traceability Matrix

Software Requirements <-> Architecture Design Specification

Requirements to Architecture Specification traceability

Statistics: 61 out of 62 covered: 98%

Software Requirements	Architecture Specification
TRCSRS-199262	DESIGN_ARCH_heap_definition
TRCSRS-199263	DESIGN_ARCH_slab_definition
TRCSRS-199322	DESIGN_ARCH_disabling_individual_interrupts DESIGN_ARCH_mask_unmask_interrupt
TRCSRS-199323	DESIGN_ARCH_IDT_vector_table DESIGN_ARCH_configurable_direct_interrupts DESIGN_ARCH_configuring_interrupts DESIGN_ARCH_configuring_interrupts_buildtime DESIGN_ARCH_configuring_interrupts_runtime DESIGN_ARCH_raising_exception_nohandler DESIGN_ARCH_synchronously_run_after_interrupt
TRCSRS-199324	DESIGN_ARCH_dedicated_interrupt_stack DESIGN_ARCH_interrupt_nesting
TRCSRS-199325	DESIGN_ARCH_32bit_hardware_clock DESIGN_ARCH_64bit_uptime_counter DESIGN_ARCH_convert_time_unit DESIGN_ARCH_specify_milliseconds DESIGN_ARCH_tickless

Software Requirements <-> Validation Test Specification

Requirements to Test Specification traceability

Statistics: 61 out of 62 covered: 98%

Software Requirements	Validation Test Specification
TRCSRS-199262	TEST_VAL_test_k_heap_alloc TEST_VAL_test_mheap_malloc_align4 TEST_VAL_test_mheap_malloc_free
TRCSRS-199263	TEST_VAL_test_mslab_alloc_align TEST_VAL_test_mslab_kdefine TEST_VAL_test_mslab_kinit
TRCSRS-199323	TEST_VAL_test_build_time_direct_interrupt TEST_VAL_test_build_time_interrupt TEST_VAL_test_direct_interrupt TEST_VAL_test_isr_dynamic TEST_VAL_test_isr_regular TEST_VAL_test_prevent_interruption TEST_VAL_test_run_time_interrupt
TRCSRS-199324	TEST_VAL_test_nested_isr
TRCSRS-199325	TEST_VAL_test_clock_cycle TEST_VAL_test_clock_uptime TEST_VAL_test_ms_time_duration TEST_VAL_test_tickless_slice TEST_VAL_test_tickless_sysclock TEST_VAL_test_time_conversions

Build the connections

Requirements

- Achieve by adding extra python modules:
 - Breathe
 - mlx.traceability
- By adding “item” label to build the connections between Requirement docs, Design specification and Test specification.
- In Test Specification, the content of testcase details should refer to the Doxygen description in source code.

Design specification (Zephyr docs)

Test specification

```
SMP
---

.. item:: TRCSRS-199345 Exclusion between physical CPUs

    Primary Text - The system shall provide a mechanism for mutual exclusion between multiple physical CPUs using a traditional spinlock primitive.

.. item:: TRCSRS-199346 Running threads on specific CPUs

    Primary Text - The system shall provide a mechanism for running threads on specific CPUs or sets of CPUs.

.. item:: TRCSRS-199347 Support operation on more than one CPU

    Primary Text - The kernel shall support operation on more than one physical CPU sharing the same kernel state
```

```
Spinlocks
=====

.. item:: DESIGN_MODULE_SPINLOCKS_APIS

.. item:: DESIGN_ARCH_spinlock_support basic function of spinlock
    :fulfills: TRCSRS-199345

SMP systems provide a more constrained :c:func:`k_spin_lock` primitive that not only masks interrupts locally, as done by :c:func:`irq_lock`, but also atomically validates that a shared lock variable has been modified before returning to the caller, “spinning” on the check if needed to wait for the other CPU to exit the lock. The default Zephyr implementation of :c:func:`k_spin_lock` and :c:func:`k_spin_unlock` is built on top of the pre-existing :c:struct:`atomic` layer (itself usually implemented using compiler intrinsics), though facilities exist for architectures to define their own for performance reasons.
```

```
SMP
***

.. item:: TEST_VAL_test_spinlock_mutual_exclusion
    :validates: TRCSRS-199345
    :result: RESULT_test_spinlock_mutual_exclusion

.. code-block:: c

    void test_spinlock_mutual_exclusion(void)

**Brief:**
    Test basic mutual exclusion using interrupt masking

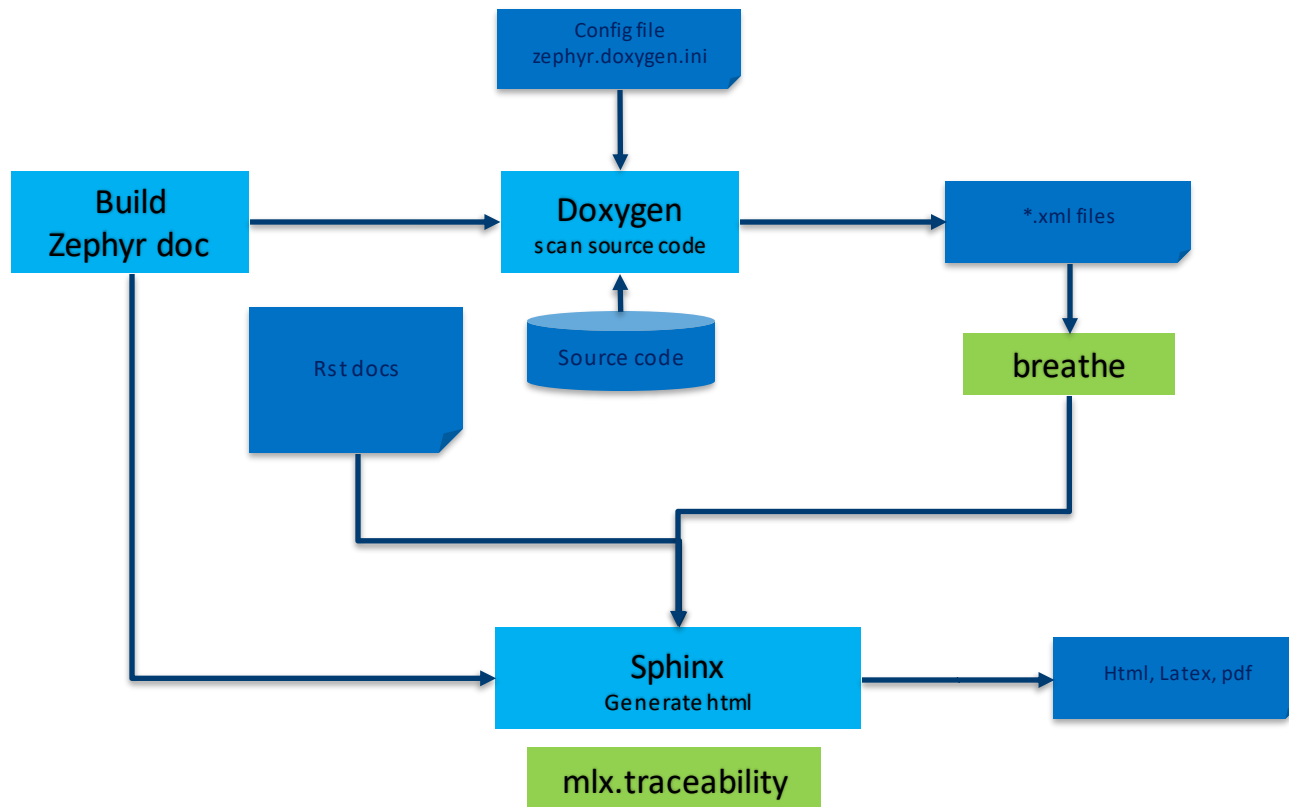
**Details:**
    Validate the spinlocks can be initialized at run-time.
    Validate the spinlocks in uniprocessor context should achieve mutual exclusion using interrupt masking.
```

Traceability generate flow

Current tools



Extra tools



Test Result

- Use twister to run test automation and get the XML testing report.
- The pass/fail/skip tests, pass rate, execution time, log, etc.
- Transform the XML test report to a Reports matrix:
- Better to show the test result between testcases and the boards.

Reports Matrix

			acrn									
			eh1_crb									
			frdm_k64f									
			intel_adsp_cavs15									
Failed	461		it8xxx2_evb									
Passed	17152		mec15xxevb_assy6853									
Skipped	1684		mec172xevb_assy6906									
			nsim_em									
			tiger_lake									
			up_squared									
			whiskey_lake									

Conclusion

- Have traceability provides us:
 - The link between requirements, design and tests.
 - The traceability matrix and test coverage.
 - Spend less effort to build a higher quality SW system.
- What's the next?
 - Solve some opens of test specification generating.

Q & A

Thank you for listening!