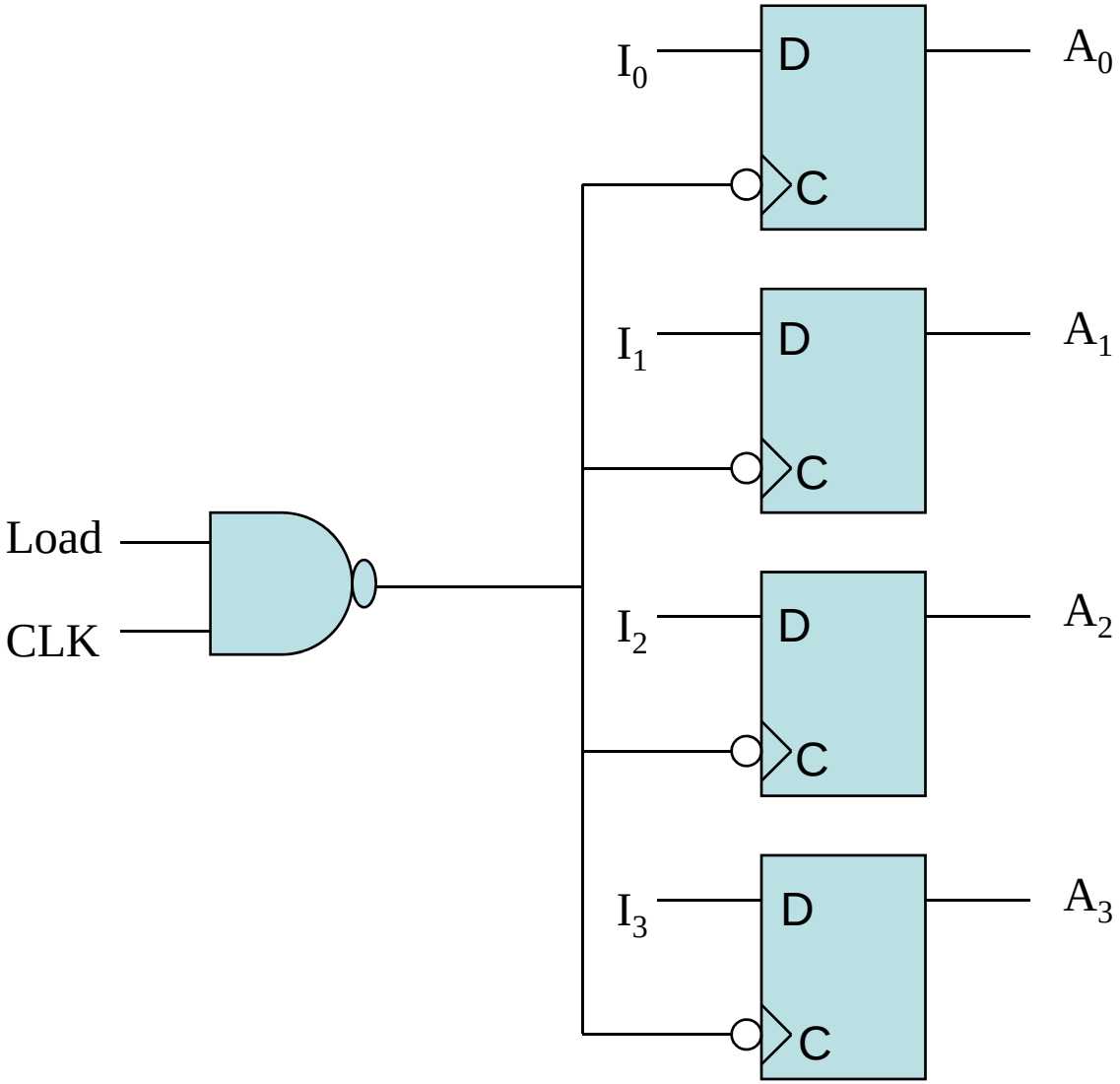
Kayhan DURSUN

Mantıksal Devre Tasarımı Dersi

6.Bölüm Cevapları

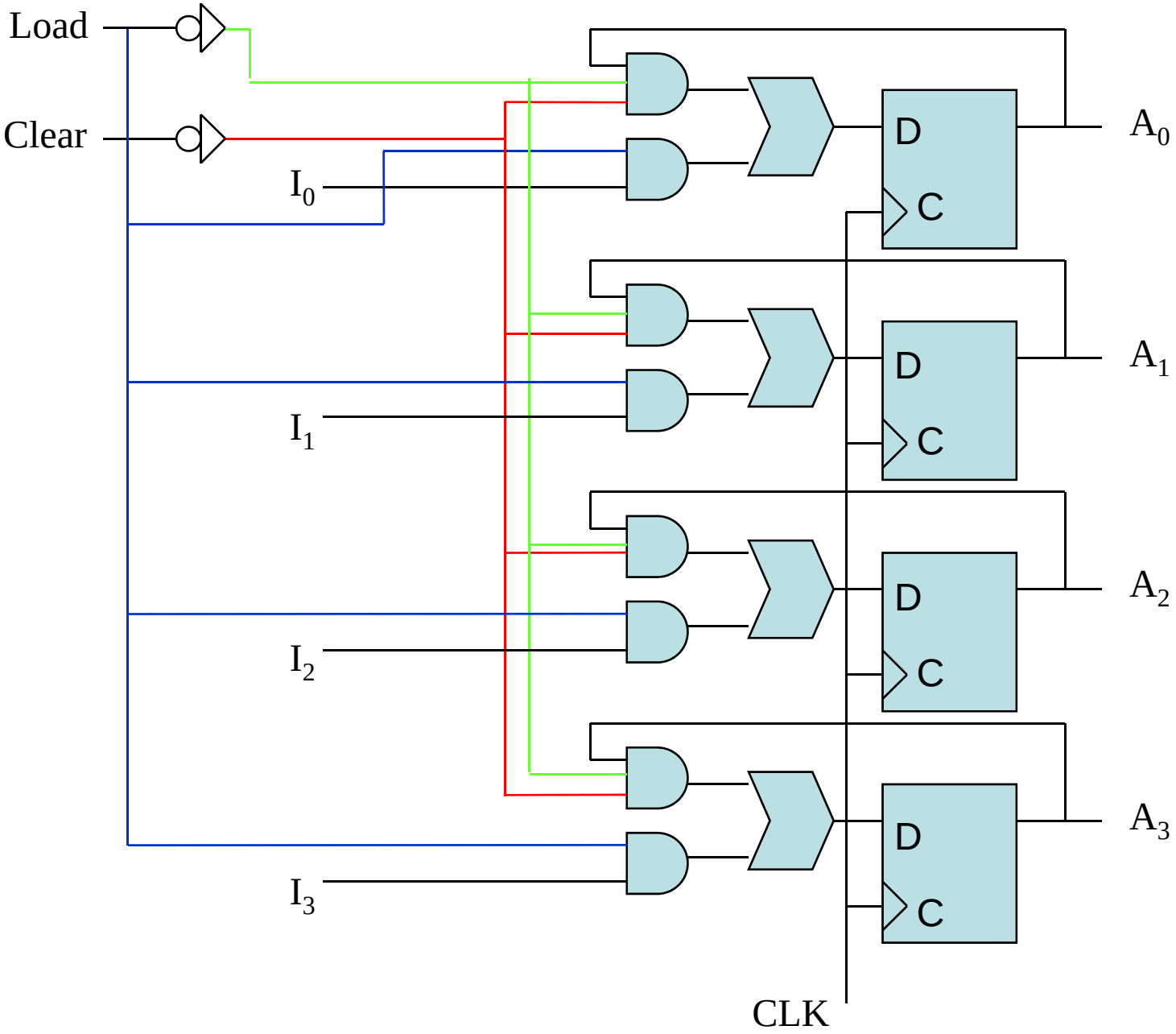
1

Include a two input NAND gate with the register of Fig. 6-1 and connect the gate output to the C inputs of all flip-flops.One input of the NAND gate receives the clock pulses from the clock generator,and the other input of the NAND gate provides paralel load control.Explain the operation of the modified register.



Clock	Load	Operation
X	0	No change
0	1	No change
1	1	Load

2 Include a synchronous clear input to the register of Fig 6.2.The modified register will have a parallel load capability and a synchronous clear capability.The register is cleared synchronously when the clock goes through a positive transition and the clear input is equal to 1.



Clear	Load	Operation
0	0	No change
1	0	0
X	1	Load inputs

3 What is the difference between serial and parallel transfer?Explain how to convert serial data to parallel and parallel data to serial.

- Seri transferde bir saat vuruşunda yalnızca bir bit iletilirken,paralel transferde bir saat vuruşu ile tüm bitler iletirlir.Bu nedenle seri transfer daha yavaştır ancak maliyeti de daha azdır.

- Seri transferi paralel transfere çevirmek için,ilk başta bütün bitler shift register ile tek tek aktarılıp çıkışlar paralel olarak bağlanır.

- Paralel transferi seri transfere çevirmek için ise ilk başta veri paralel yüklenip çıkışta bitler teker teker iletilir.

4

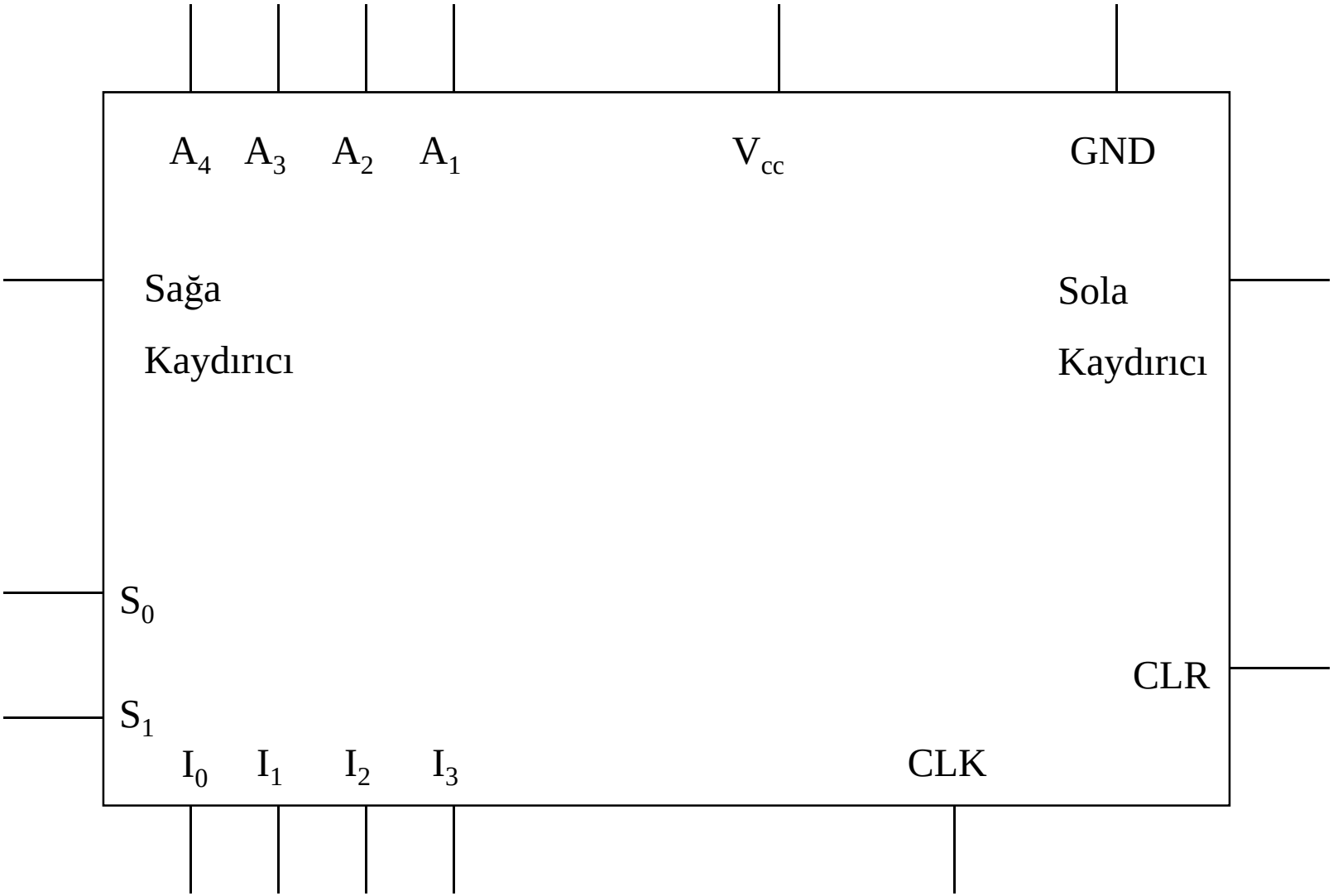
The content of a 4-Bit register is initially 1101.The register is shifted six times to the right with the serial input being 101101.What is the content of the register after each shift?

S.I=101101

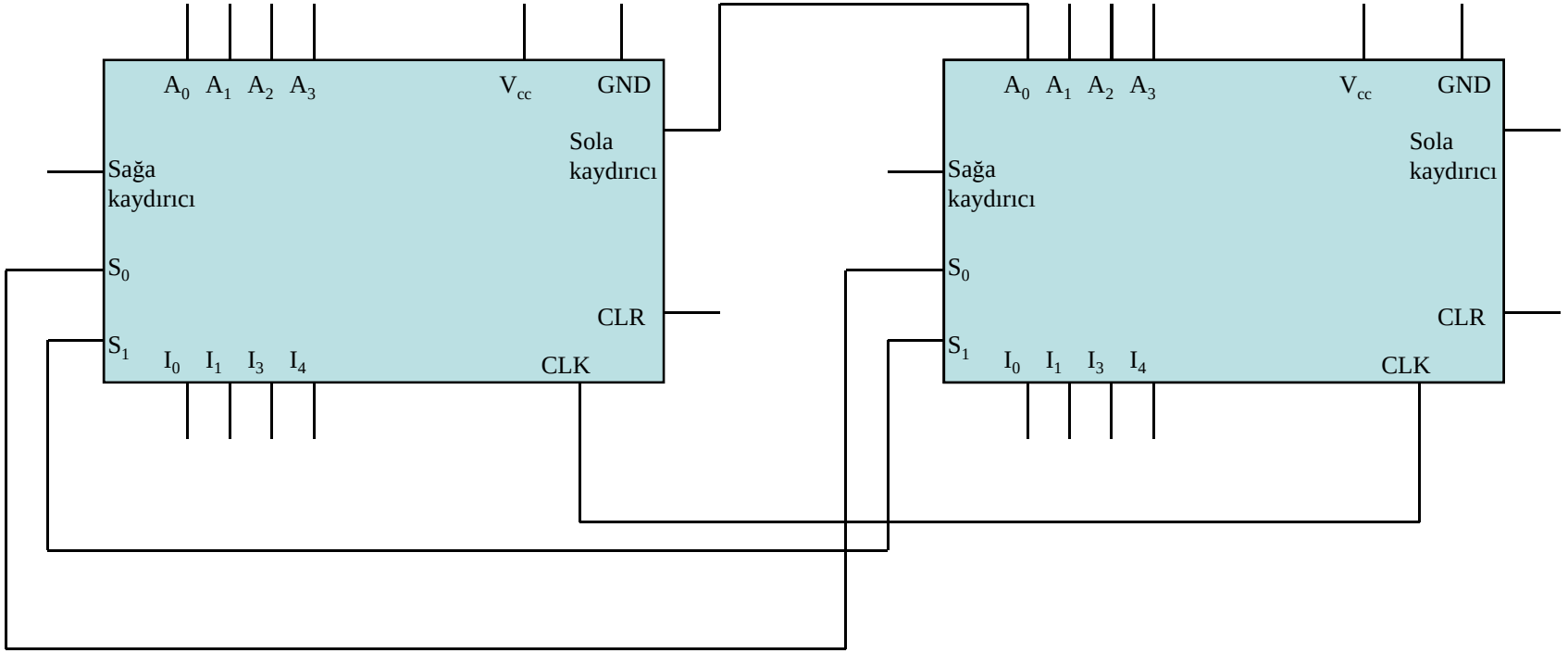
Initial	1.Shift	2.Shift	3.Shift	4.Shift	5.Shift	6.Shift
1101	1110	0111	1011	1101	0110	1011

5 The 4-Bit universal shift register shown in Fig. 6-7 is enclosed within one IC package.

a Draw a block diagram of the IC showing all inputs and outputs.Include two pins for the power supply.

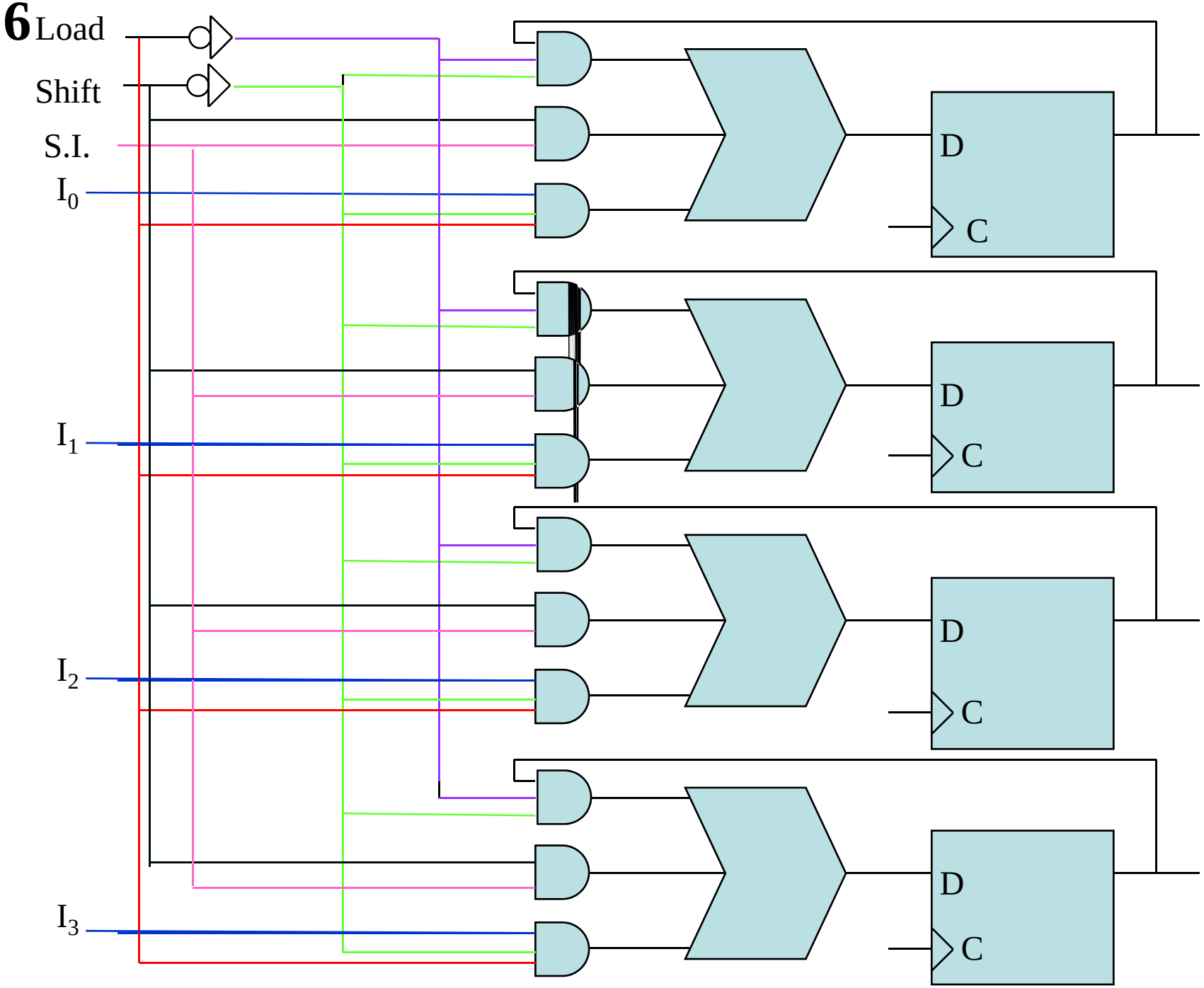


5 b Draw a block diagram using two ICs to produce an 8-Bit universal shift register.



6

Design a 4 bit shift register with parallel load using D flip-flops.There are two control inputs:shift and load.When shift=1,the content of the register is shift by one position.New data is transfered into the register when load =1 and shift=0.If both control inputs are equal to 0,the content of the register does not change.

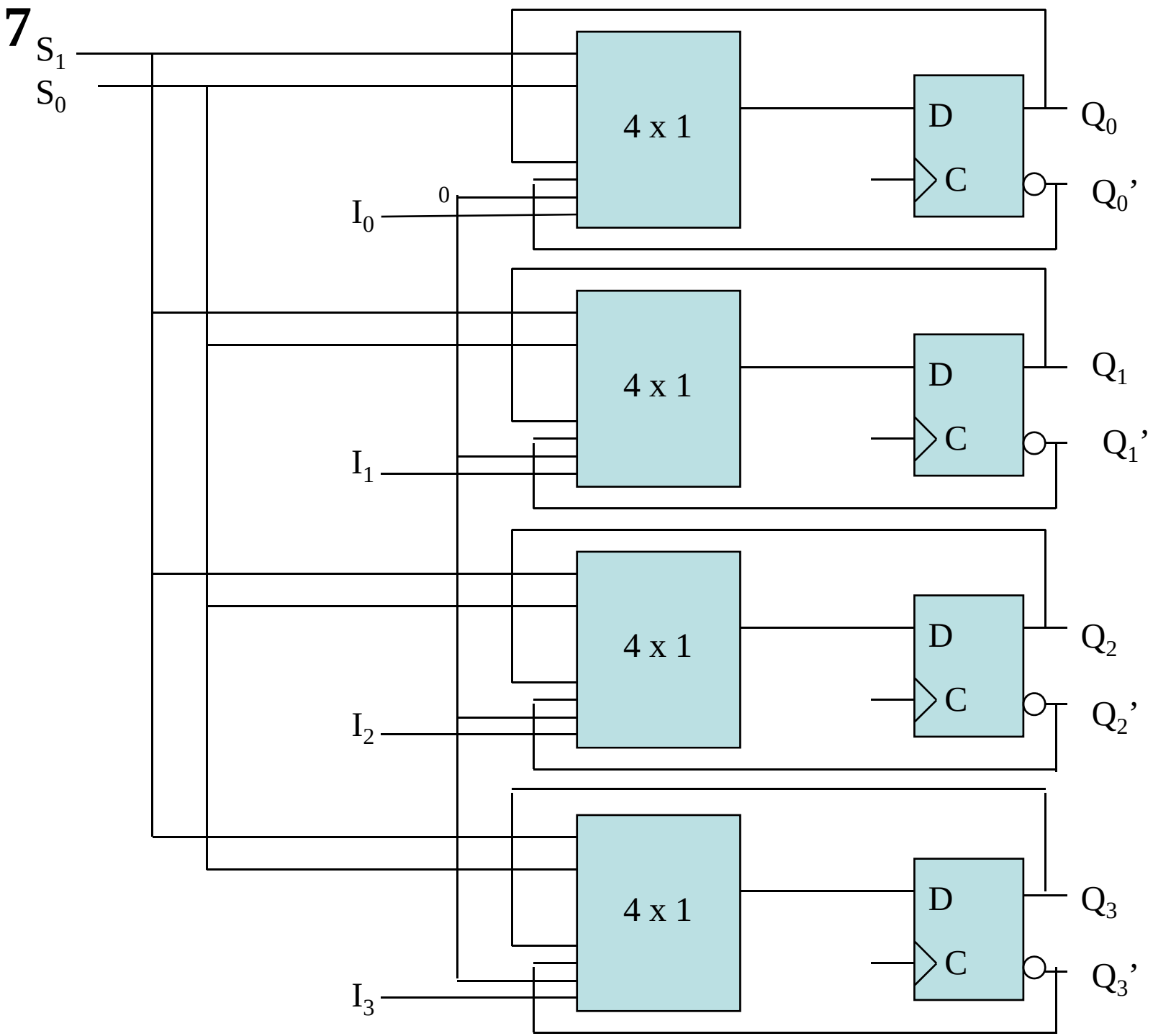

6
Load
Shift
S.I.
I_0
I_1
I_2
I_3
D
C
D
C
D
C
D
C

7

Draw the logic diagram of a 4-bit register with four D flip-flops and four 4x1 multiplexers with mode selection inputs s_1 and s_0.The register operates according to the following function table.

s_1	s_0	Register Operation
0	0	No change
0	1	Complement the four outputs
1	0	Clear register to 0(synchronous with the clock)
1	1	Load parallel data

7



8 The serial adder of Fig. 6-6 uses two 4-Bit registers.Register A holds the binary number 0101 and regiser B holds 0111.The carry flip-flop is initially reset to 0.List the binary values in register A and the carry flip-flop after each shift.

	Initial	1.Shift	2.Shift	3.Shift	4.Shift
A	0101	0010	0001	1000	1100
Carry	0	1	1	1	0

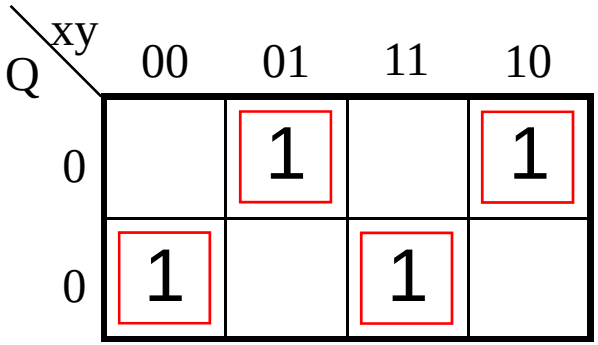
9 Two ways for implementing a serial adder (A+B) ,is shown in section 6-2.It is necessary to modify the circuits to modify them to serial subtractors (A-B)

a Using the circuit of Fig. 6-5,show the changes needed to perform A+2's complement of B.

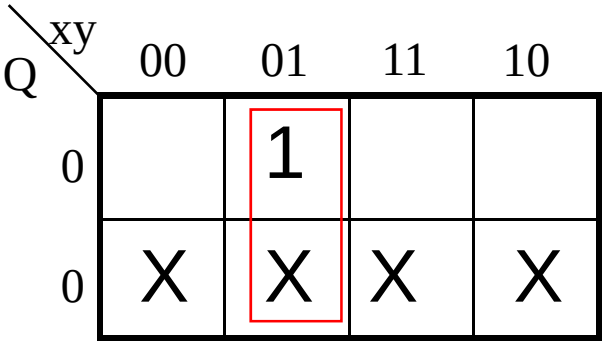
Figure 6-5'te B registerinin çıkışına inverter koyup carry'i de ilk olarak 1'e eşitlersek A+(B'nin 2'ye göre tersi) işlemi yapılır.

9 b Using the circuit of Fig.6-6,show the changes needed by modifying Table 6-2 from an adder to a subtractor circuit.

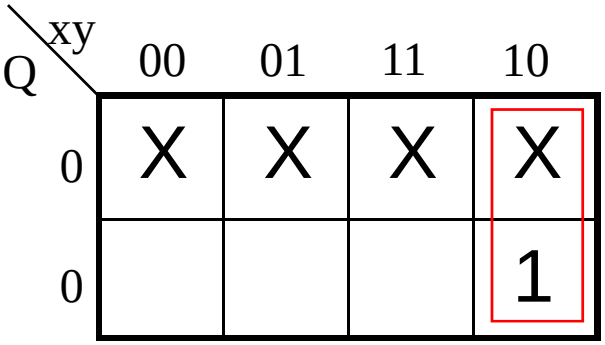
Present State	Inputs		Next State	Output	FlipFlop Inputs	
Q	x	y	Q	W	J_Q	K_Q
0	0	0	0	0	0	X
0	0	1	1	1	1	X
0	1	0	0	1	0	X
0	1	1	0	0	0	X
1	0	0	1	1	X	0
1	0	1	1	0	X	0
1	1	0	0	0	X	1
1	1	1	1	1	X	0



$W = Q \oplus x \oplus y$

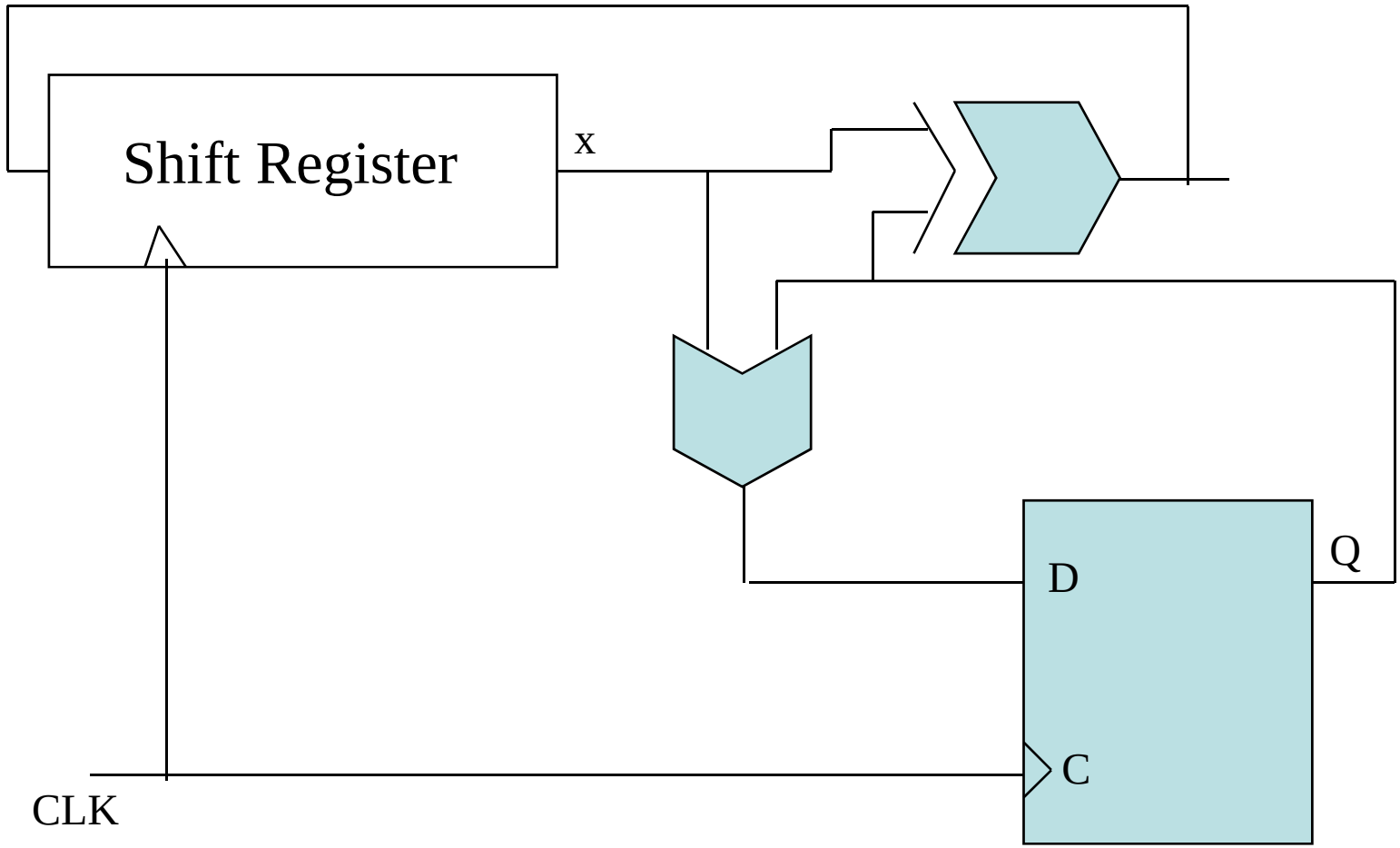


$J_Q = x'y$



$K_Q = xy'$

10 Design a serial 2's complementer with a shift register and a flip-flop.The binary number is shifted out from one side and it's 2's complement shifted into the other side of the shift register.



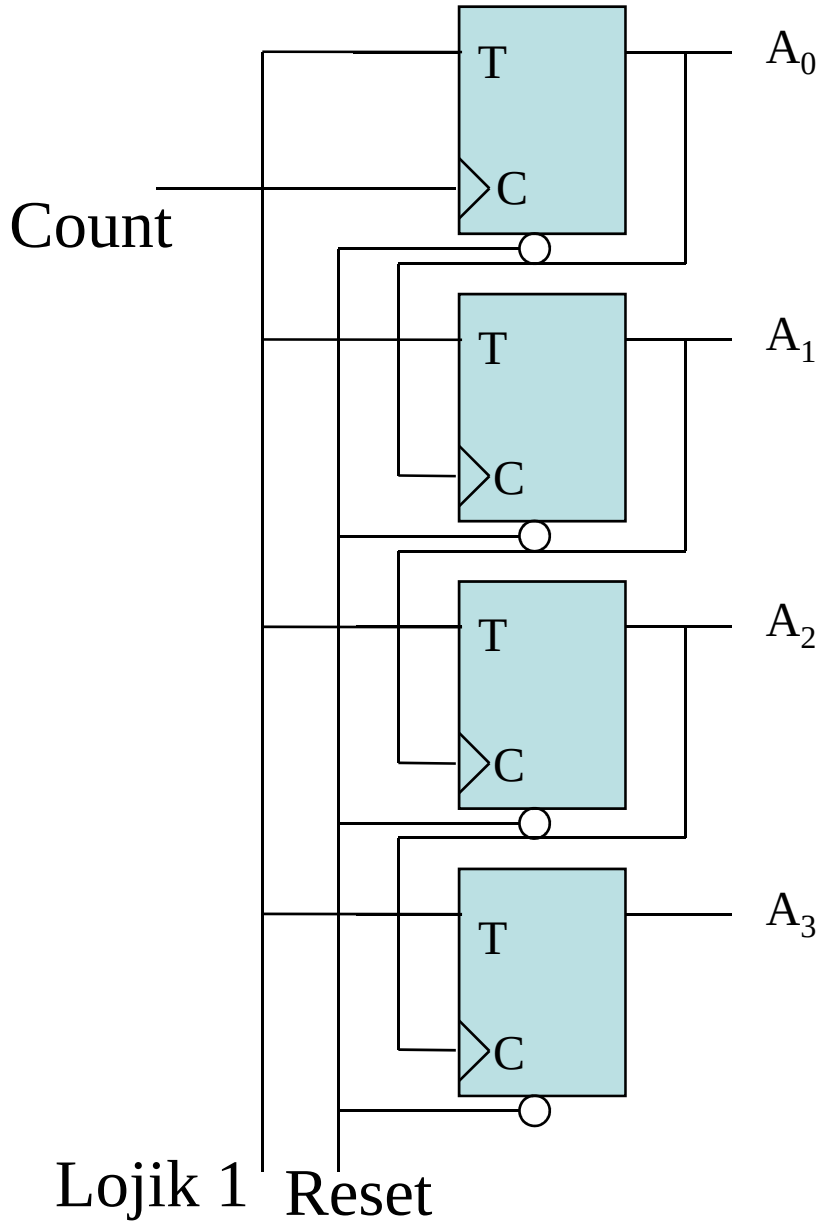
11 A binary ripple counter uses flip-flops that trigger on the positive edge of the clock.What will be the count if; a)the normal outputs of the flip-flops are connected to the clock and b)the complement outputs of the flip-flops are connected to the clock?

a)Geriye doğru sayan sayıcı olur.

b)İleriye doğru sayan sayıcı olur.

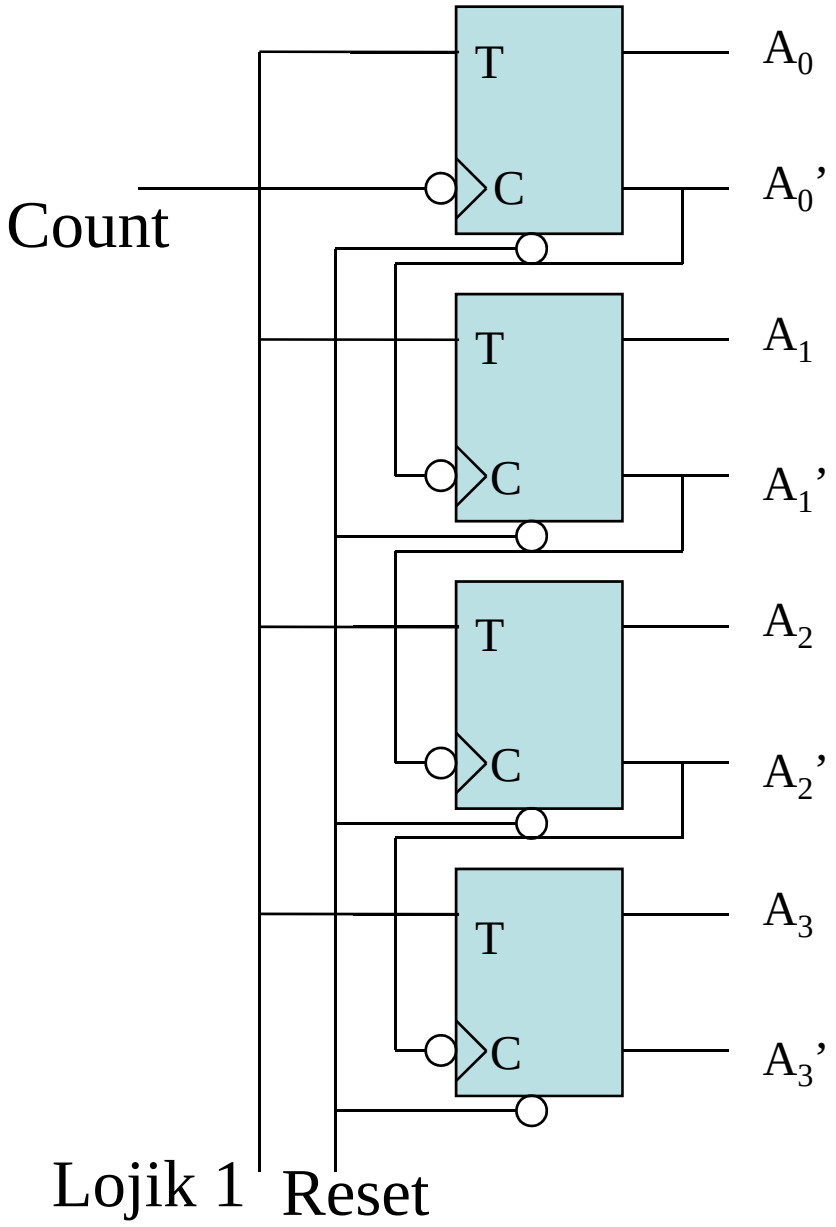
12 Draw the logic diagram of a 4-bit binary ripple down counter using **a)**flip-flops that trigger on the positive-edge of the clock and **b)** flip-flops that trigger on the negative-edge of the clock.

a

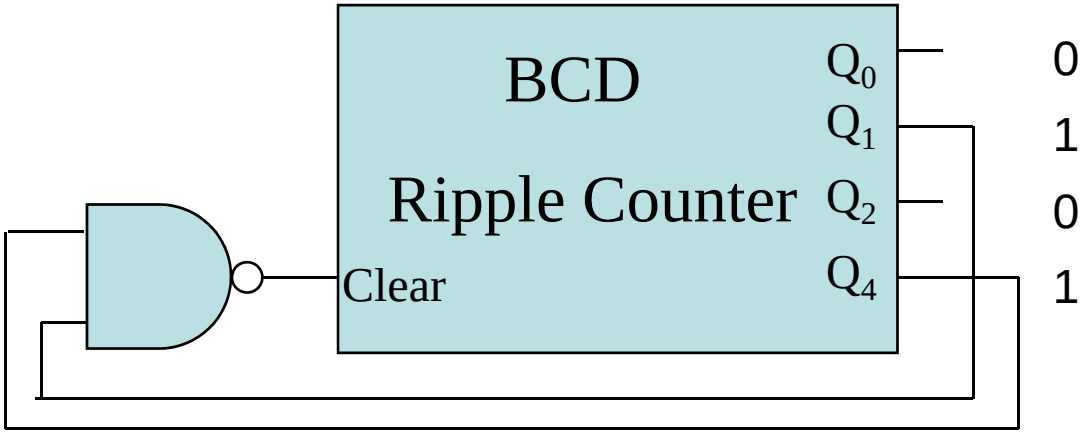


12

b



13 Show that a BCD ripple counter can be constructed using a 4-bit binary ripple counter with asynchronous clear and a NAND gate that detects the occurence of count 1010.



14 How many flip-flop will be complemented in a 10-bit binary ripple counter to reach the next count after the following count:

a) 100110 0111
100110 1000 → 4

b) 0 011111111
1 000000000 → 9

c) 1111111111
0000000000 → 10

15 A flip-flops has a 5 ns delay from the time the clock edge occurs to the time the output is complemented.What is the maximum delay in a 10-bit binary ripple counter that uses these flip-flops?What is the maximum frequency the counter can operate reliably?

Bütün flip-flop'ların complement olacağı düşünürlürse;

10 x 5 = 50 ns maksimum gecikme olacaktır.

Maksimum frequency ise

$10^9/50$ = 20 Mhz olur.

16 The BCD ripple counter shown in Fig. 6-10 has four flip-flops and 16 states ,of which only 10 are used.Analyze the circuit and determine the next state for each of the other unused states.What will happen if a noise signal sends the circuit to one of the unused states?

$$1010 \longrightarrow 1011 \longrightarrow 0100$$

$$1011 \longrightarrow 0100$$

$$1100 \longrightarrow 1101 \longrightarrow 0100$$

$$1101 \longrightarrow 0100$$

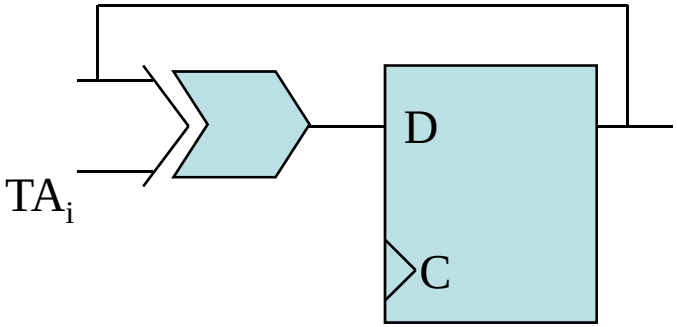
$$1110 \longrightarrow 1111 \longrightarrow 0000$$

$$1111 \longrightarrow 0000$$

17 Design a 4-bit binary synchronous counter with D flip-flops.

Figure 6-12'deki çıkışları T flip-flop için yazıp count enable'a I dersek:

$TA_0 = I$, $TA_1 = IA_0$, $TA_2 = IA_0A_1$, $TA_3 = IA_0A_1A_2$ olur



T flip-flop'tan D flip-flop şekildeki gibi elde edildiği için; D flip-flop'la yapılacak senkron sayıcının girişleri aşağıdaki gibi olur:

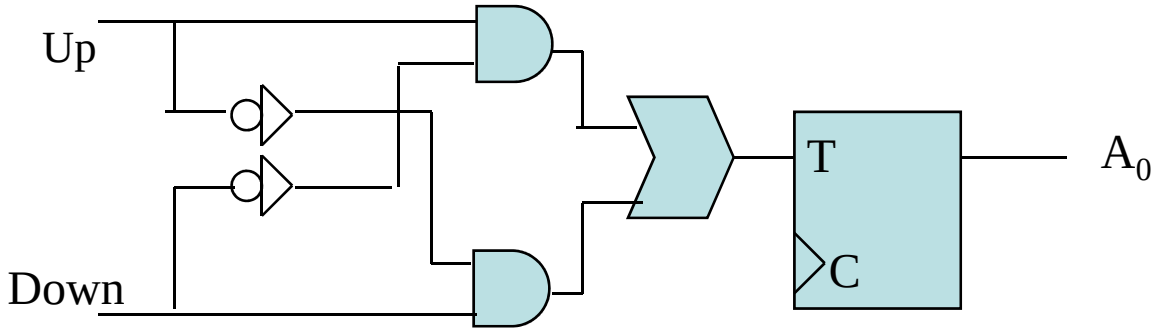
$DA_0 = I \oplus A_0$, $DA_1 = A_1 \oplus (IA_0)$, $DA_2 = A_1 \oplus IA_0A_1$,

$DA_3 = A_3 \oplus IA_0A_1A_2$ olur

18 What operation is performed in the up-down counter of Fig. 6-13 when both the up and down inputs are enabled?Modify the circuit so that when both inputs are equal to 1,the counter does not change state,but remains in the same count.

*Up ve down girişlerinin ikisi birden 1 olursa ,devre yukarı doğru sayma yapar.

*Eğer bu iki input 1 iken devrenin bir önceki durumda kalmasını istiyorsak T flip-flop'unun girişinin 0 olması gerekir ki outputta değişiklik olmasın.Bunun için devrede aşağıdaki değişikliği yapmalıyız:

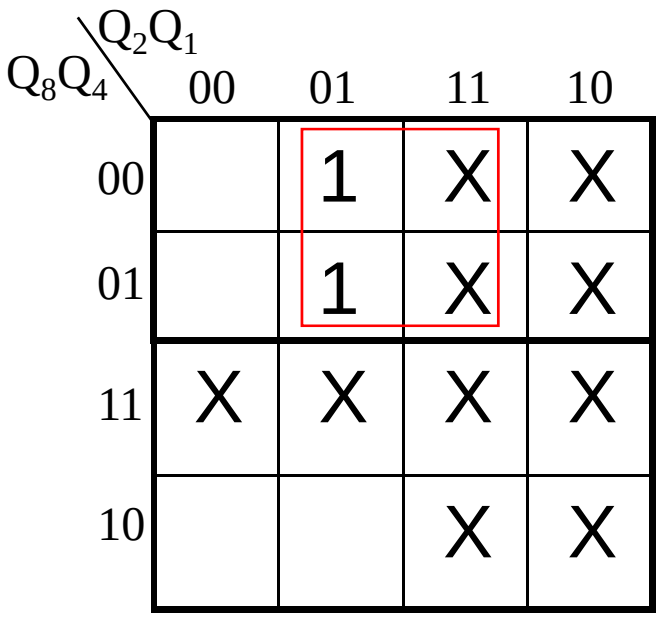


Görüldüğü gibi inputlar 1 iken AND kapıları daima 0 çıktısı verip T flip-flop'unun durumunun değişmemesini sağlar

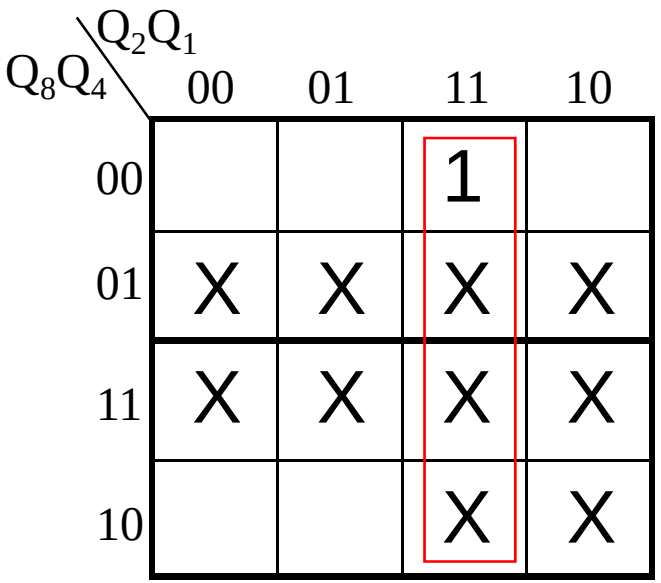
19 The flip-flop input equations for a BCD counter using T flip-flops are given in section 6-4.Obtain the input equations for a BCD counter that uses;

a J-K flip-flops

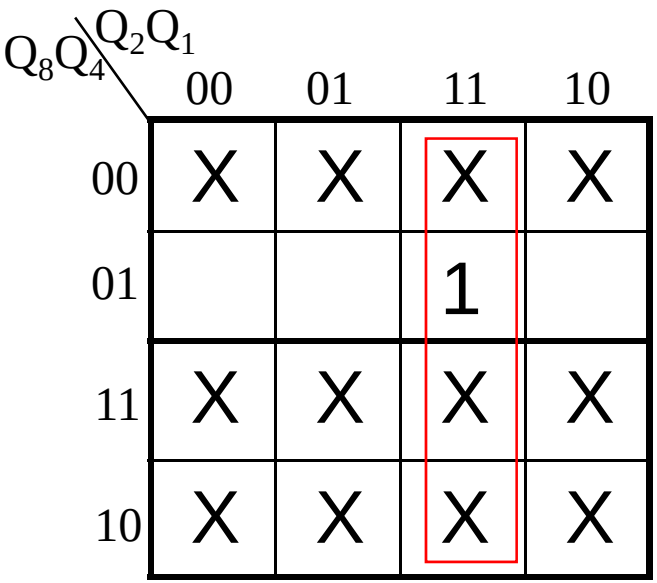
Present State				Next State				Flip-flop inputs							
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1	J_{Q8}	K_{Q8}	J_{Q4}	K_{Q4}	J_{Q2}	K_{Q2}	J_{Q1}	K_{Q1}
0	0	0	0	0	0	0	1	0	X	0	X	0	X	1	X
0	0	0	1	0	0	1	0	0	X	0	X	1	X	X	1
0	0	1	0	0	0	1	1	0	X	0	X	X	0	1	X
0	0	1	1	0	1	0	0	0	X	1	X	X	1	X	1
0	1	0	0	0	1	0	1	0	X	X	0	0	X	1	X
0	1	0	1	0	1	1	0	0	X	X	0	1	X	X	1
0	1	1	0	0	1	1	1	0	X	X	0	X	0	1	X
0	1	1	1	1	0	0	0	1	X	X	1	X	1	X	1
1	0	0	0	1	0	0	1	X	0	0	0	X	0	1	X
1	0	0	1	0	0	0	0	X	1	0	X	0	X	X	1



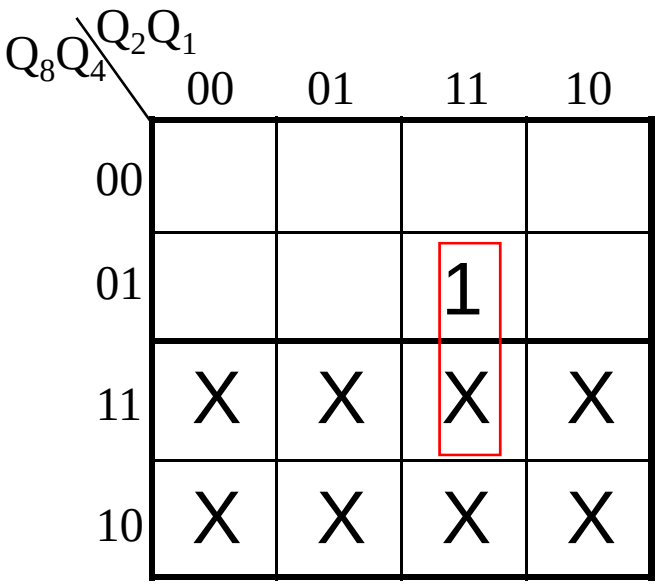
$JQ_2 = Q_8'Q_1$



$JQ_4 = Q_1Q_2$



$KQ_4 = Q_1Q_2$

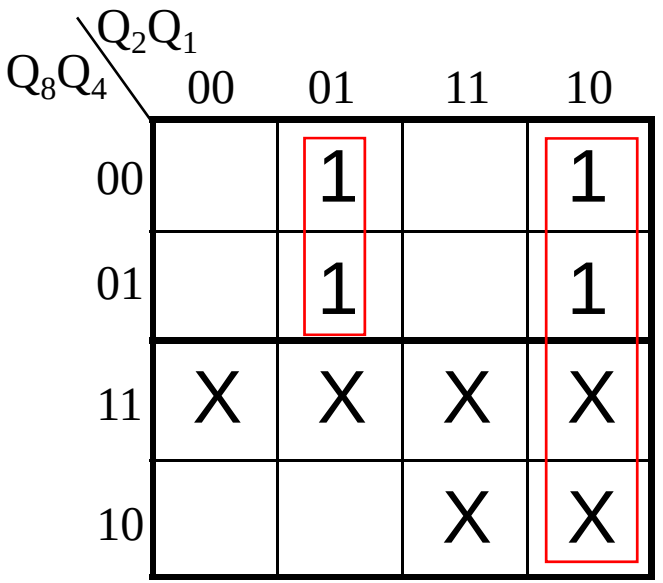


$JQ_8 = Q_1Q_2\,Q_4$

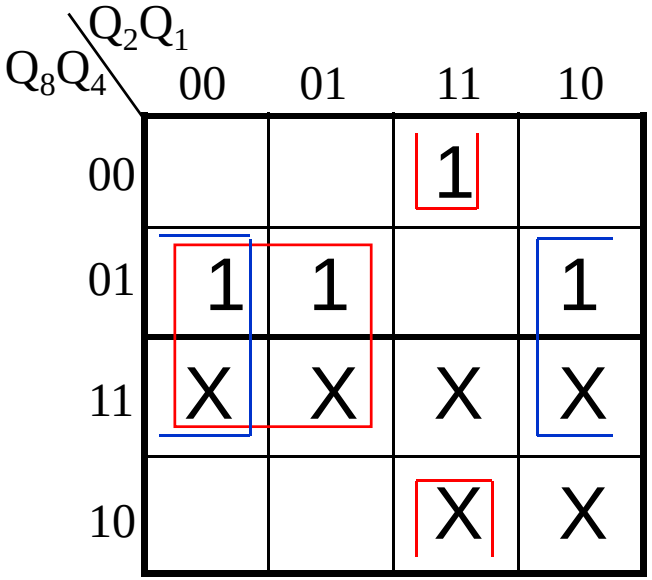
Ayrıca ; $JQ_1 = 1$ $KQ_1 = 1$ $KQ_2 = Q_1$ $KQ_8 = Q_1$ olduğu tablodan doğrudan görülür.

19 b D flip-flops

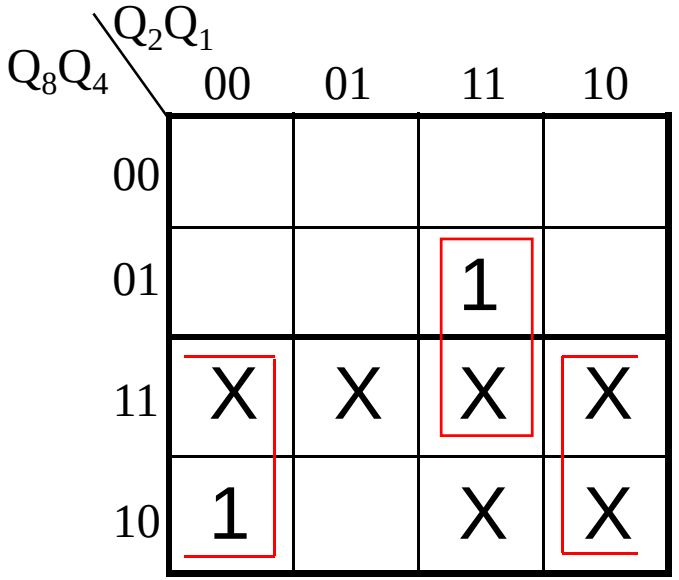
Present State				Next State			
Q_8	Q_4	Q_2	Q_1	Q_8	Q_4	Q_2	Q_1
0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	0
0	0	1	0	0	0	1	1
0	0	1	1	0	1	0	0
0	1	0	0	0	1	0	1
0	1	0	1	0	1	1	0
0	1	1	0	0	1	1	1
0	1	1	1	1	0	0	0
1	0	0	0	1	0	0	1
1	0	0	1	0	0	0	0



$DQ_2=Q_2Q_1'+Q_8'Q_2'Q_1$



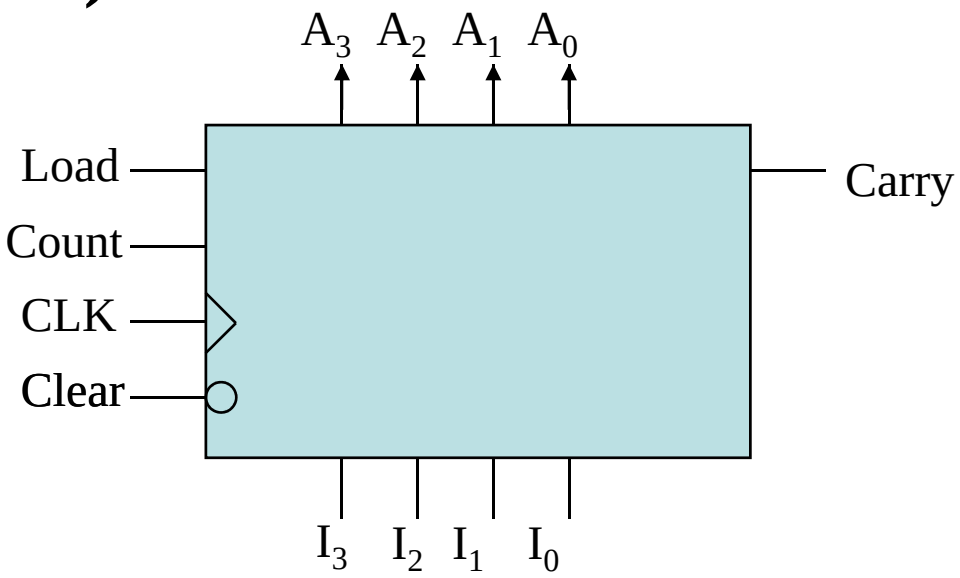
$DQ_4=Q_4Q_1'+Q_4Q_2'+ Q_4'Q_2 Q_1$



$DQ_8=Q_8Q_1'+Q_4Q_2Q_1$

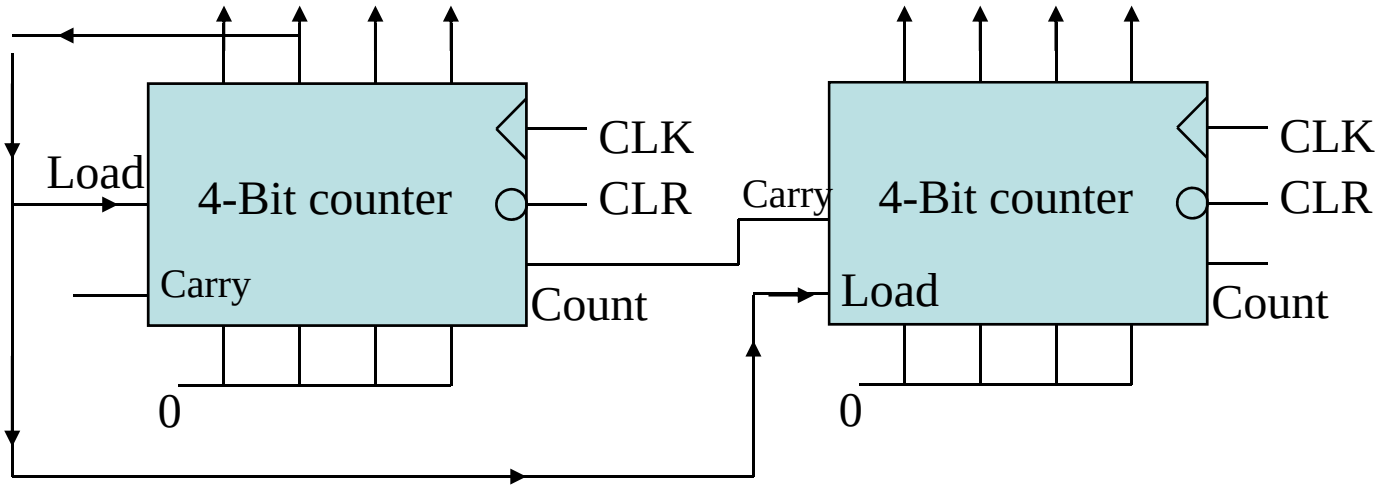
20 Enclose the binary counter with paraller load of Fig. 6-14 in a block diagram showing all inputs and outputs.

a) Show the connections of four such blocks to produce a 16-bit counter with parallel load.



16 bitlik sayıcı oluşturmak için her bir devrenin carry çıkışını bir sonrakinin Count girişine bağlamalıyız.Bu işlem için bu devreden 4 tane gereklidir.

b) Construct a binary counter that counts from 0 to 64.



21 The counter of Fig. 6-14 has two control inputs Load(L) and Count(C) and a data input ,(I_i).

a) Derive the flip-flop input equations for J and K of the first stage in terms of L,C,and I.

$$JA_0 = CL' + I_0L$$

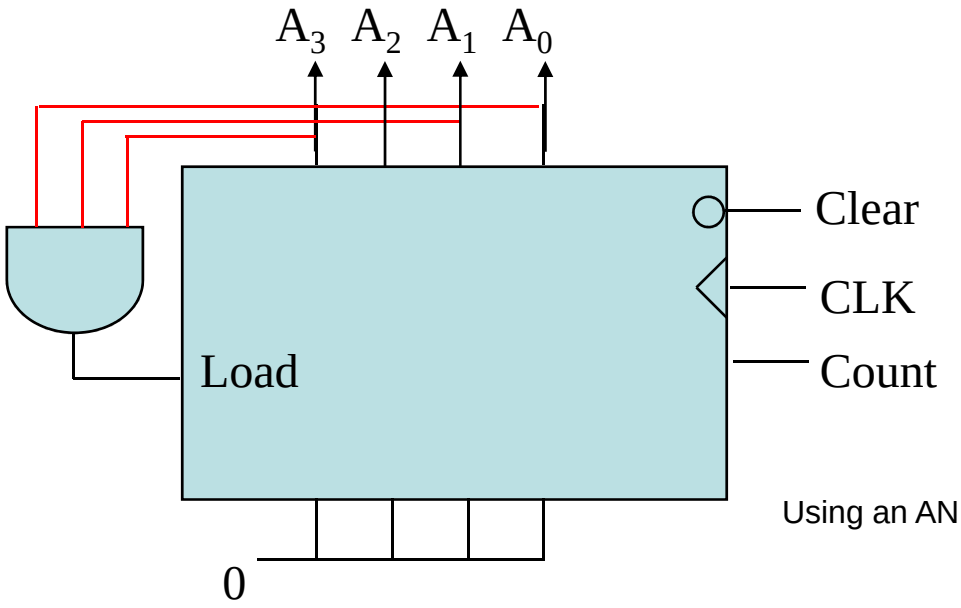
$$KA_0 = LI_0' + L'C$$

b) The logic diagram of the first stage of an equivalent integrated circuit is shown in Fig. P6-21.Verift that this circuit is equivalent to the one in a.

$$J = [L(LI')][L + C] = (L' + LI)(L + C)=L'C + LI$$

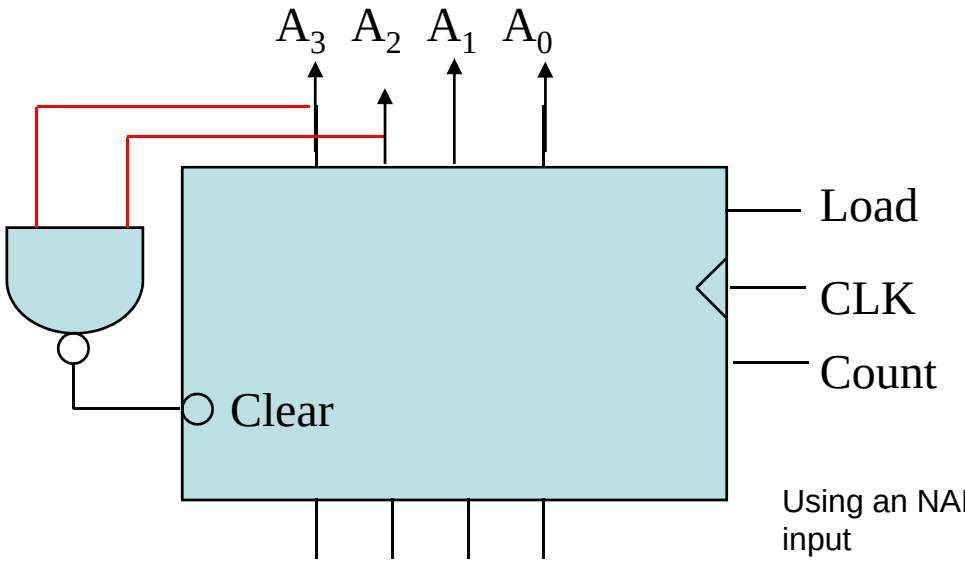
$$K = (LI')(L + C) = (L' + I')(L + C) = L'C + LI'$$

22 Using the circuit of Fig. 6-14, design a mod-12 counter:



1011(11) olduktan sonraki clock darbesi ile inputlar sayaca yüklenir ve sayaç sıfırlanır.

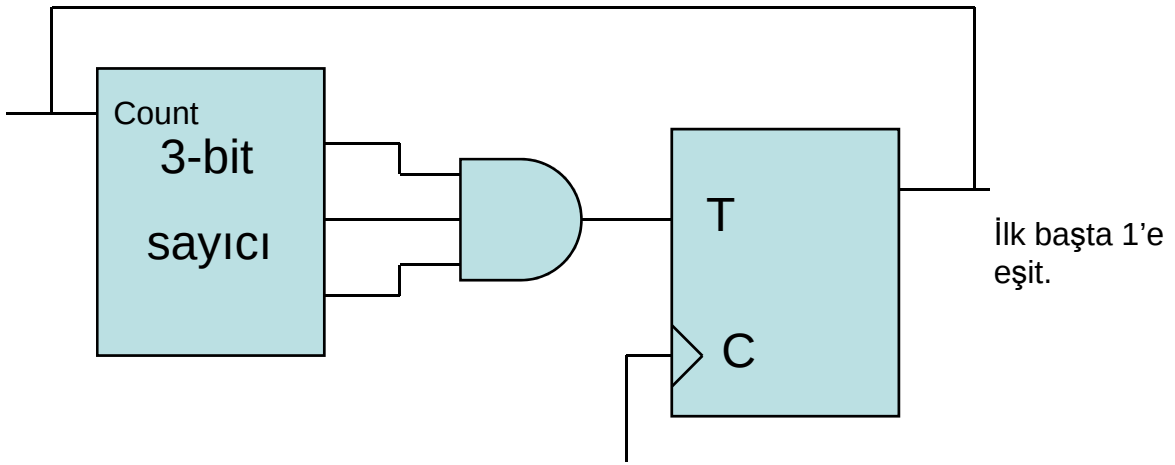
Using an AND gate and the load input



1100(12) olduğu anda sayaç sıfırlanır.

Using an NAND gate and the asynchronous clear input

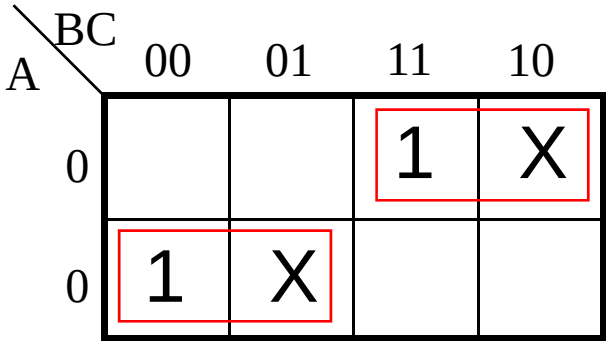
23 Design a timing circuit that provides an output signal that stays on for exactly eight clock cycles.A start signal sends the output to the 1 state,and after eight clock cycles the signal returns to the 0 state.



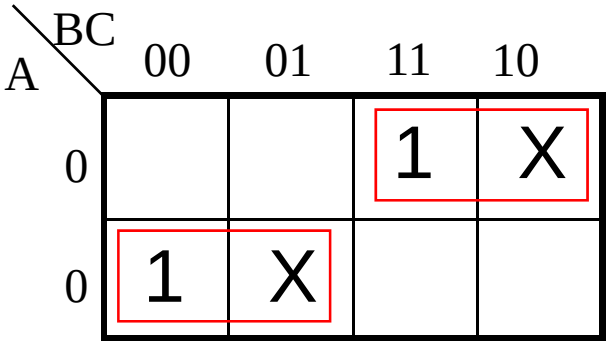
Sayaç 111 sayınca flip-flop 0 çıkarır ve count'a 0 girişi giderek saymayı durdurur.

24 Design a counter with T flip-flops that goes through the following binary repeated sequence: 0,1,3,7,6,4.Show that when binary states 010 and 101 are considered as don't care conditions,the counter may operate properly.Find a correct way to design.

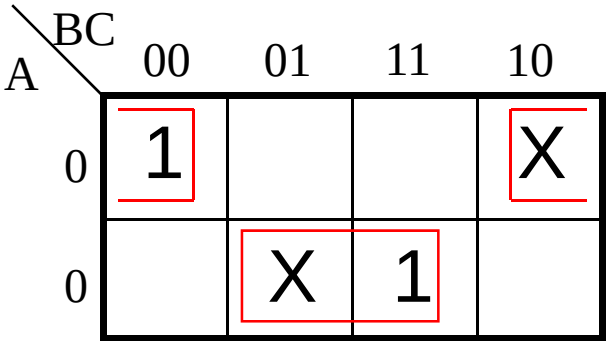
Present State			Next State			Flip-flop inputs		
A	B	C	A	B	C	T_A	T_B	T_C
0	0	0	0	0	1	0	0	1
0	0	1	0	1	1	0	1	0
0	1	0	X	X	X	X	X	X
0	1	1	1	1	1	1	0	0
1	0	0	0	0	0	1	0	0
1	0	1	X	X	X	X	X	X
1	1	0	1	0	0	0	1	0
1	1	1	1	1	0	0	0	1



$T_A = A \oplus B$



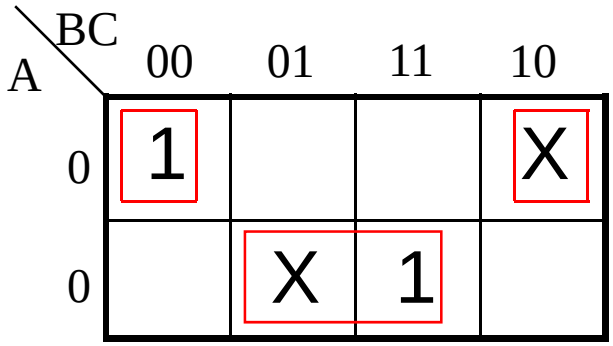
$T_B = B \oplus C$



$T_C = A \oplus C$

Devrenin kullanılmayan bir duruma girdiğinde çıkıp çıkmadığını kontrol etmek gerekirse;

010 → 101 → 010 olduğu ve devrenin kendini düzeltmediği görülür.Bunun için;



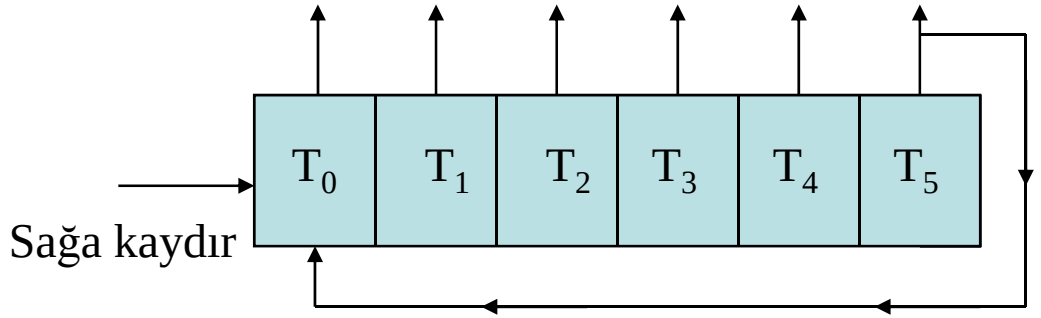
Şeklinde sadeleştirirsek bu durumda devre kendini düzeltir.

101 → 010 → 100

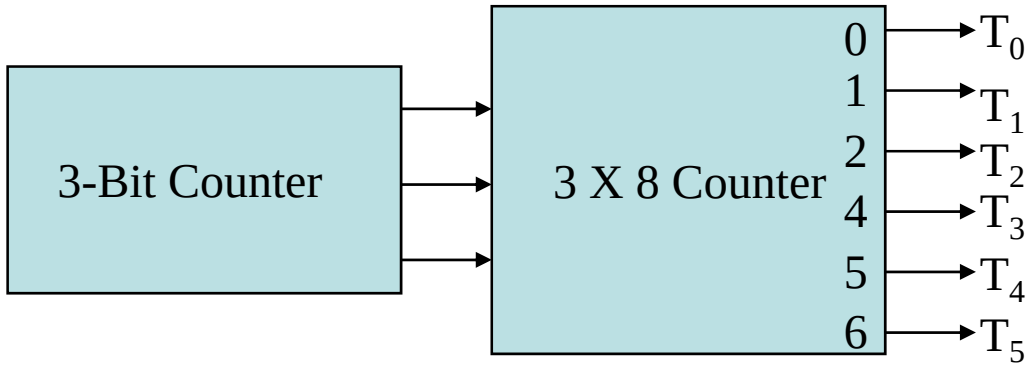
25 It is necessary to generate six repeated timing signals T_0 through T_5 similar to the ones shown in Fig. 6-17(c).Design the timing circuit using:

a)Flip-flops only b)A counter and a decoder.

a



b



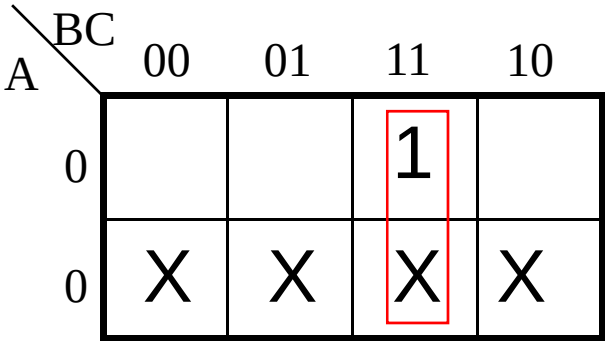
26 A digital system has a clock generator that produces pulses at a frequency of 80 Mhz.Design a circuit that provides a clock with a cycle time of 50 ns.

$(1000 \times 10^{-9}) / 50 = 20Mhz$ olur.

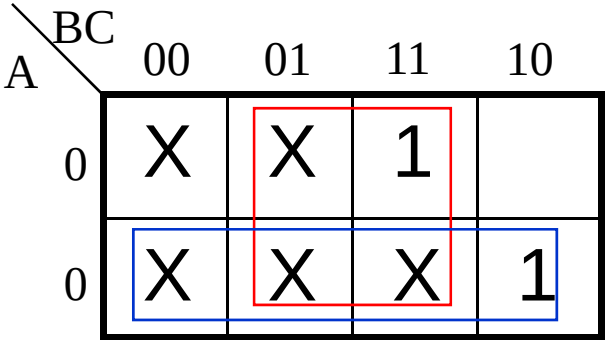
Bu durumda 80 ‘i 4’te birine indirmek için bir 2-bit sayıcı kullanmamız gerekir.

Design a counter with the following repeated binary sequence:0,1,3,4,5,6. Use JK flip-flops.

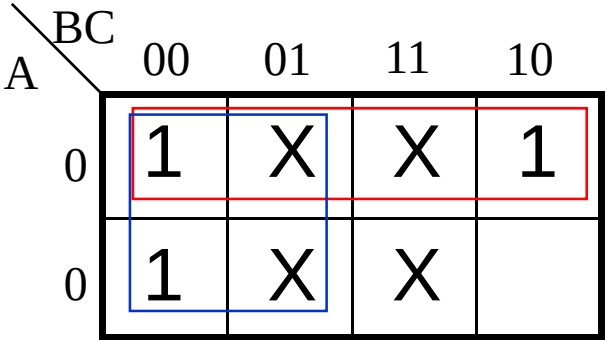
Present State			Next State			Flip-flop inputs					
A	B	C	A	B	C	J_A	K_A	J_B	K_B	J_C	K_C
0	0	0	0	0	1	0	X	0	X	1	X
0	0	1	0	1	0	0	X	1	X	X	1
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	1	0	0	1	X	X	1	X	1
1	0	0	1	0	1	X	0	0	X	1	X
1	0	1	1	1	0	X	0	1	X	X	1
1	1	0	0	0	0	X	1	X	1	0	X
1	1	1	X	X	X	X	X	X	X	X	X



$J_A = BC$ $K_A = B$



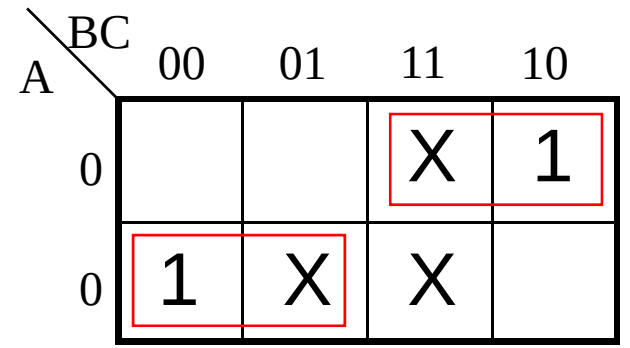
$K_B = A + C$ $J_B = C$



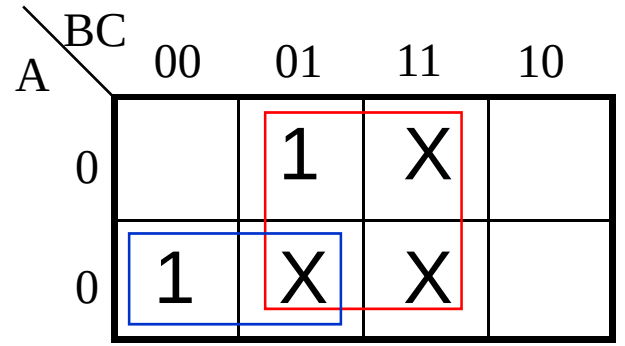
$J_C = A' + B'$ $K_C = 1$

Design a counter with the following repeated binary sequence:0,1,2,4,6.Use D flip-flops.

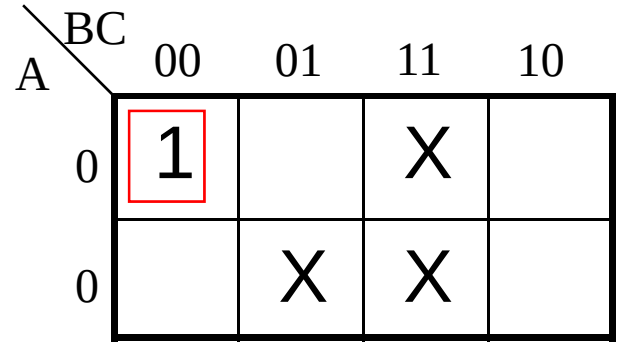
Present State			Next State		
A	B	C	A	B	C
0	0	0	0	0	1
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	X	X	X
1	0	0	1	1	0
1	0	1	X	X	X
1	1	0	0	0	0
1	1	1	X	X	X



$D_A = A \oplus B$



$D_B = AB' + C$



$D_C = A'B'C'$

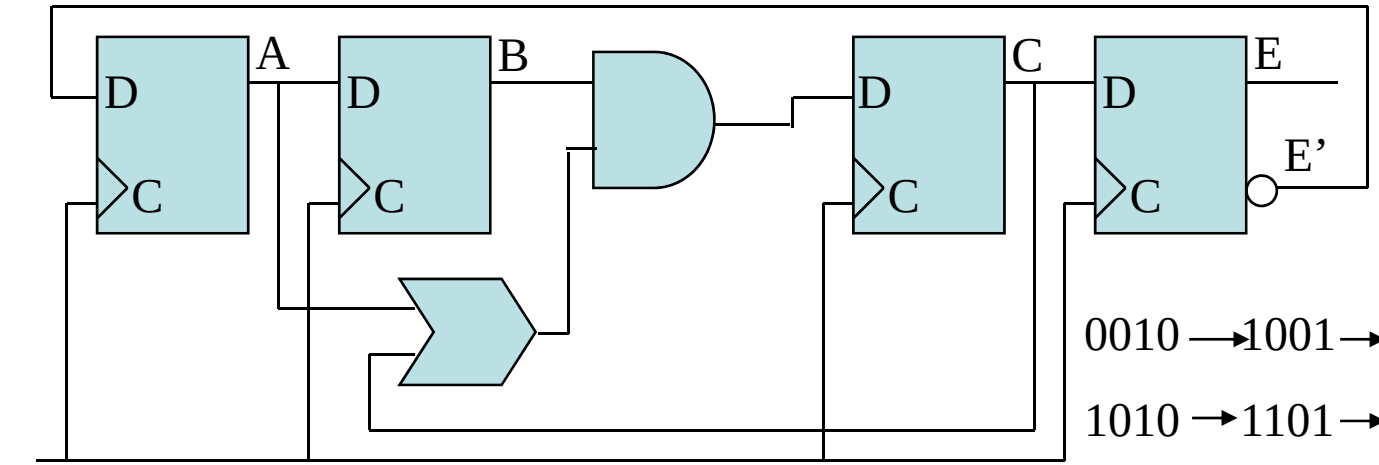
011→110 101→110 111→010

Görüldüğü üzere devre beklenmeyen duruma girdiği zaman kendini düzeltir

29 List the 8 unused states in the switch-tail ring counter of Fİg. 6-18 (a). Determine the next state for each of these states and show that, if the counter finds itself in an invalid state,it does not return to a valid state.Modify the circuit as recomended in the text and show that the counter produces the same sequence of states and that circuit reaches a valid state from any of the unused states.

Present State				Next State			
A	B	C	D	A	B	C	D
0	0	1	0	1	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	0	0	1	0
0	1	1	0	1	0	1	1
1	0	0	1	0	1	0	0
1	0	1	0	1	1	0	1
0	1	1	0	0	1	1	1
1	0	1	1	0	1	0	1
1	1	0	1	0	1	0	1

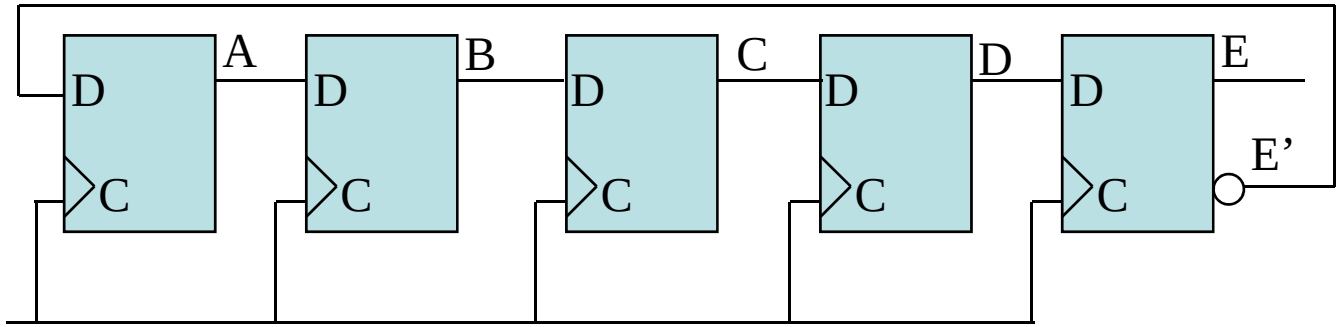
Görüldüğü gibi devre kullanılmayan bir duruma girdiği zaman kendini kurtaramıyor.Belirtilen şekilde C flip-flop'unun girişine Dc = (A + C)B değişikliği yapılınca devre kullanılmayan bir duruma girince kendini kurtaracaktır.



0010 → 1001 → 0100 → 1000

1010 → 1101 → 0110 → 1011 → 0101 → 0000

30



A	B	C	D	E	Outputs
0	0	0	0	0	A'E'
1	0	0	0	0	A B'
1	1	0	0	0	B C'
1	1	1	0	0	C D'
1	1	1	1	0	D E'
1	1	1	1	1	A E
0	1	1	1	1	A'B
0	0	1	1	1	B'C
0	0	0	1	1	C'D
0	0	0	0	1	D'E

Görüldüğü gibi 5 flip-flop'tan 10 farklı durum oluştu.

Show that a Johnson counter with n flip-flops produces a sequence of 2n states.List the 10 states produced with five flip-flops and the Boolean terms of each of the 10 AND gate outputs.