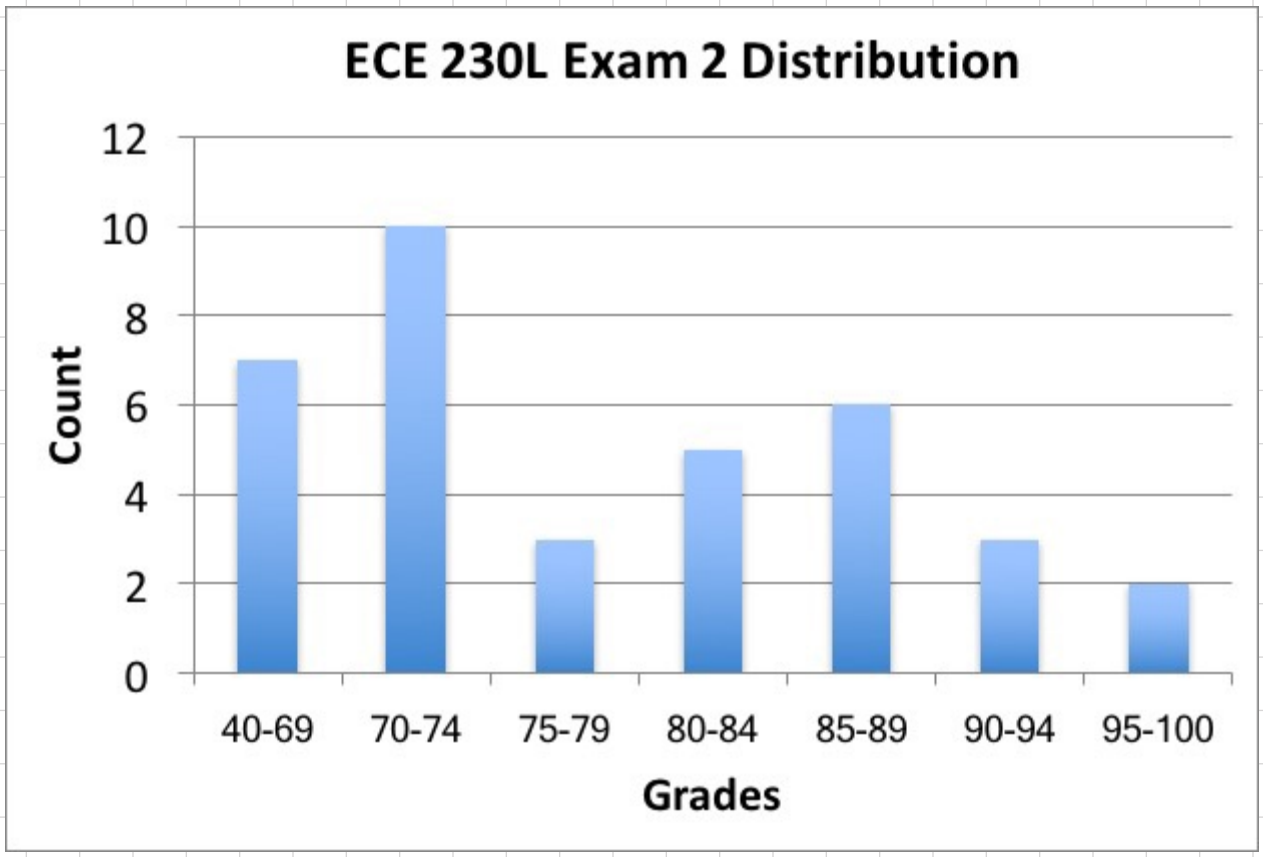
Exam 2 Results & Opportunity

Avg. 76

High: 99

Low: 44



OPPORTUNITY: Go through and re-work any of the pages of the exam to earn back up to ¼ the points missed.

CONDITIONS (No Exceptions!):

1) You must work independently! No TA's, no classmates, no genius friends, no Prof. Franklin, etc.
2) You may use your book and class notes.
3) You must re-work an entire PAGE (no partial parts of a page/problem).
4) Print out the PAGE(s) that you re-work from the Exam posted on Piazza.
5) Turn in your original exam with the re-worked pages stapled in order at the end (No extra paper/pages beyond this!).
6) Due to me by Tuesday, Nov. 14 at the beginning of class.

The re-worked pages will be graded and you will be credited up to 25% of the missed points.

Lecture #18

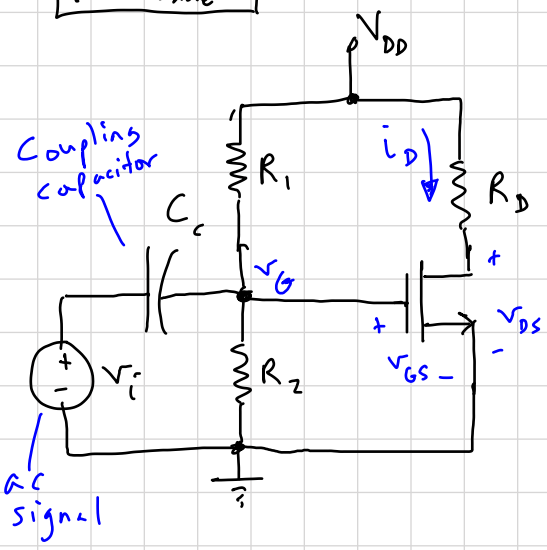
DC Biasing of MOSFET Circuits

As with pn junction diodes, eventually want to apply ac (analog) signals to MOSFETs, but first must understand their DC operation in circuits.

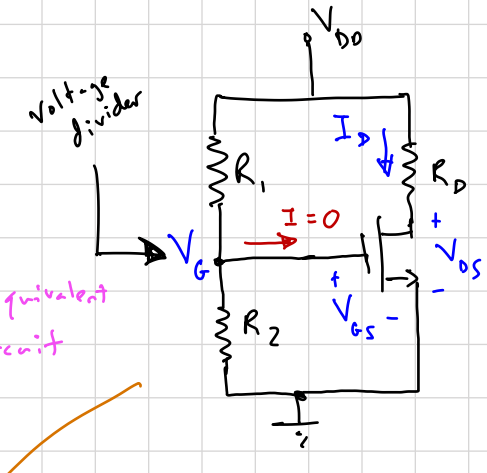
- **Common-Source Circuit** : MOSFET circuit with source terminal grounded

Example: (actually a linear amplifier that we will cover next time!)

N-channel:



DC Equivalent Circuit



Voltage divider at V_G gives:

$$V_G = V_{GS} = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$$

Assuming $V_{GS} > V_{TN}$ and $V_{DS} > V_{DS}(sat)$

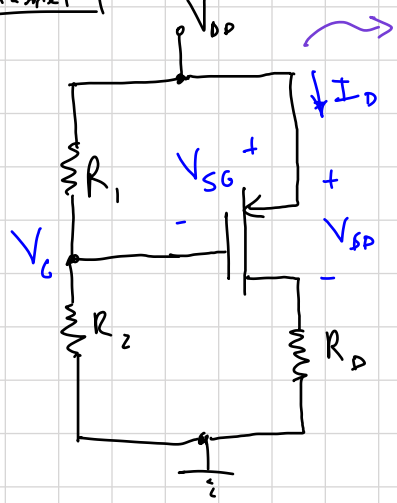
$$I_D = k_n (V_{GS} - V_{TN})^2$$

$$V_{DS} = V_{DD} - I_D R_D$$ Load Line

Power dissipated in MOSFET:

$$P_T = I_D V_{DS}$$

P-channel



Even though source is tied to V_{DD}, for p-channel the V_{DD} becomes signal ground for the equiv. circuit (including ac)

$$V_G = \left(\frac{R_2}{R_1 + R_2}\right) V_{DD}$$

$$V_{SD} = V_{DD} - V_G$$

$$I_D = k_p (V_{SG} + V_{TP})^2$$

↳ if $V_{SD} > V_{SD}(sat)$

$$V_{SD} = V_{DD} - I_D R_D$$ Load Line

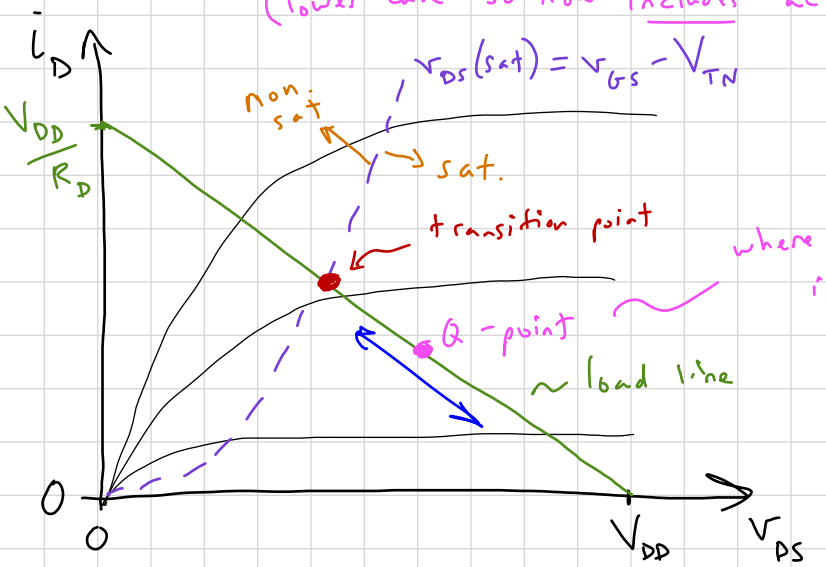
Problem-Solving Technique: MOSFET DC Analysis

Analyzing the dc response of a MOSFET circuit requires knowing the bias condition (saturation or nonsaturation) of the transistor. In some cases, the bias condition may not be obvious, which means that we have to guess the bias condition, then analyze the circuit to determine if we have a solution consistent with our initial guess. To do this, we can:

1. Assume that the transistor is biased in the saturation region, in which case $V_{GS} > V_{TN}$, $I_D > 0$, and $V_{DS} \geq V_{DS}(\text{sat})$.
2. Analyze the circuit using the saturation current-voltage relations.
3. Evaluate the resulting bias condition of the transistor. If the assumed parameter values in step 1 are valid, then the initial assumption is correct. If $V_{GS} < V_{TN}$, then the transistor is probably cutoff, and if $V_{DS} < V_{DS}(\text{sat})$, the transistor is likely biased in the nonsaturation region.
4. If the initial assumption is proved incorrect, then a new assumption must be made and the circuit reanalyzed. Step 3 must then be repeated.

- **Load-Line** - identifies region in which MOSFET can be biased/operate in a given circuit

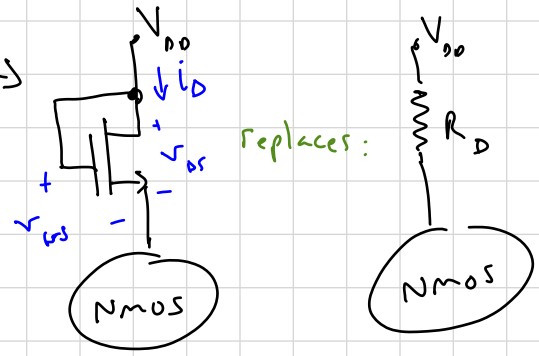
(lower case so now includes ac component)



where the transistor is operating

(for Nmos with a resistive load)

Other configurations: NMOS enhancement load device



replaces:

$V_{TN} > 0$ and $v_{DS} = v_{GS} > v_{DS}(sat) = v_{GS} - V_{TN}$

✱ Always biased in saturation

So: $i_D = K_n (v_{GS} - V_{TN})^2 = K_n (v_{DS} - V_{TN})^2$