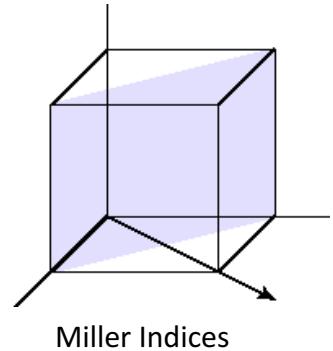
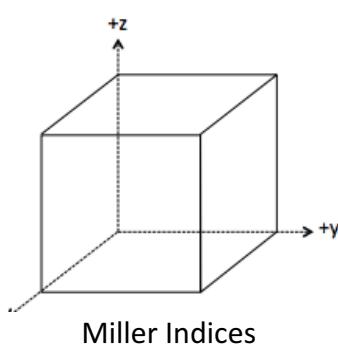


Group 1: Crystal Structure and Quantum Theory of Solids

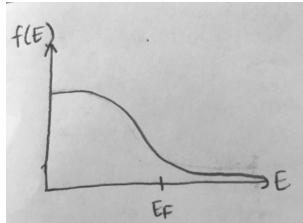
- a. Draw the indicated plane or solve for the missing Miller indices:



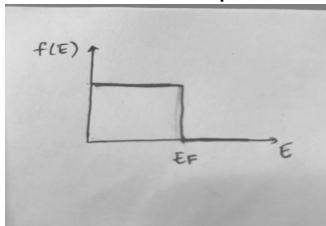
(1 0 0)

- b. Determine the surface density of the above planes for a Si FCC lattice
($a = 5.43 \text{ \AA}$, $1\text{\AA} = 10^{-8} \text{ cm}$)

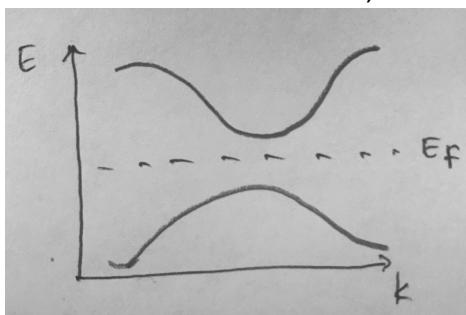
- c. The following curve is at $T = 300\text{K}$. Draw the curve at a higher temperature (K).



- d. Under what temperature condition is this graph achieved?



- e. Under the above conditions, should any electrons be in the conduction band?



2) Thermal Equilibrium

Some potentially useful information for Si at T= 300 K: $N_C = 2.8 \times 10^{19} \text{ cm}^{-3}$, $N_V = 1.04 \times 10^{19} \text{ cm}^{-3}$, $n_i = 1.5 \times 10^{10} \text{ cm}^{-3}$, $m_n^* = 1.08 m_0$, $m_p^* = 0.56m_0$, $Eg = 1.12 \text{ eV}$

- a. Assuming $E_g = 1.12 \text{ eV}$ is independent of T, for each of the following cases, determine n_o and p_o .

i. $T = 300\text{K}$, $N_a \gg N_d$, $N_a = 10^{14} \text{ cm}^{-3}$

$n_o =$
$p_o =$
<i>type</i> =

ii. $T = 600\text{K}$, $N_a = 10^{10} \text{ cm}^{-3}$, $N_d = 10^{10} \text{ cm}^{-3}$

$n_o =$
$p_o =$
<i>type</i> =

iii. $T = 0\text{K}$, $N_a = 1.6 \times 10^{16} \text{ cm}^{-3}$, $N_d = 8 \times 10^{13} \text{ cm}^{-3}$

$n_o =$
$p_o =$
<i>type</i> =

- b. Silicon at T= 300 K is doped with arsenic atoms such that the concentration of electrons is $n_o = 9 \times 10^{15} \text{ cm}^{-3}$.

i. Determine $E_F - E_V$.

ii. Calculate p_o .

$E_F - E_V =$
$P_o =$
<i>minority carrier</i> =
$E_F - E_{Fi} =$

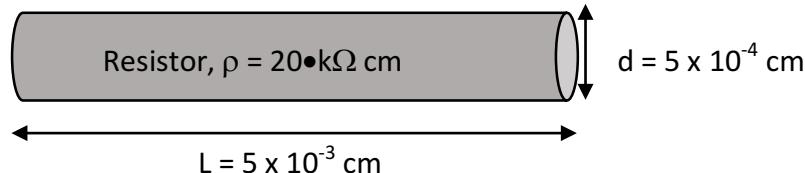
iii. Indicate the minority carrier.

iv. Find $E_F - E_{Fi}$.

Carrier Transport – Drift and Diffusion

- a. You are an engineer tasked with designing a *p*-type Si resistor with a resistivity (ρ) of 20 $\text{k}\Omega\cdot\text{cm}$. We are given the following parameters:

$$\begin{aligned} T &= 300\text{K} \\ \mu_n &= 1000 \text{ cm}^2/\text{V}\cdot\text{s} \\ D_p &= 15 \text{ cm}^2/\text{s} \end{aligned}$$



- i. What will the resistance of this resistor need to be given these requirements?

$$R =$$

- ii. What doping density will you use for N_a and N_d ?

$$N_a =$$

$$N_d =$$

- iii. What voltage should be applied across the resistor to produce a current density of 100 A/cm^2 (with uniform doping)?

$$V =$$

- b. Answer the following true or false questions:

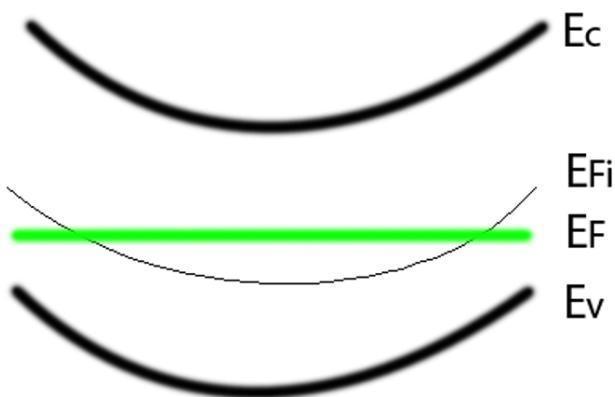
- | | | | |
|------|--|---|---|
| i. | Impurity scattering increases with increased temperature | T | F |
| ii. | Lattice scattering increases with increased temperature | T | F |
| iii. | Holes move against the electric field | T | F |
| iv. | Electrons move against the electric field | T | F |

- c. Briefly describe the difference between drift and diffusion current, using simple diagrams for both cases. Hint: Consider the force that drives both phenomena.

GROUP 3: Semiconductor Band Diagrams**Question:**

- a) For this question, assume $E_{\text{MIDGAP}} - E_{\text{Fi}} = 7.3 \text{ meV}$, $T=300\text{K}$, $N_a = 10^{16} \text{ cm}^{-3}$, and $N_d \ll N_a$ for the silicon sample. Compute $E_F - E_{\text{Fi}}$, $E_C - E_V$, $E_C - E_F$, and $E_F - E_V$. Then, draw a carefully dimensioned energy band diagram for the Silicon sample labelling the aforementioned values.

Answer the following questions for the band diagram given below:



- b) Do the equilibrium conditions prevail? How do you know?
- c) Sketch the electrostatic potential (ϕ) inside the semiconductor as a function of x .
- d) Sketch the electric field (E) inside the semiconductor as a function of x .

NOTE: If this question seems too long, feel free to remove this part.

- e) Roughly sketch n , p , and n_i versus x .

Pn junction Diodes Xingyu Chen, Haizhou Liu, Walker Willetts

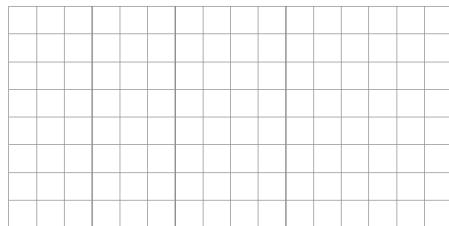
Consider a silicon pn junction diode with area of 10^{-4} cm^2 at T=300K and the following parameters:

n-side: $N_d = 10^{18} \text{ cm}^{-3}$

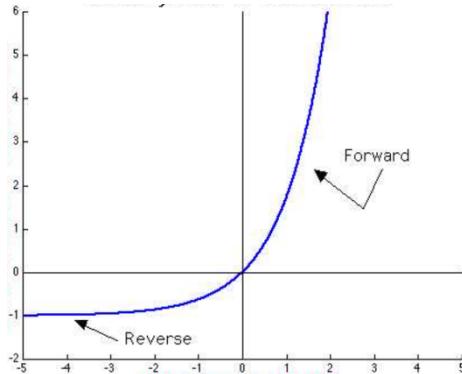
p-side: $N_a = 10^{13} \text{ cm}^{-3}$

- Sketch the thermal equilibrium energy band diagram for this diode in the space provided. Include an accurate value for $|E_F - F_{Fi}|$ on both sides of the junction and of V_{bi} . Show your calculation and label E_c, E_v, E_F, E_{Fi} .

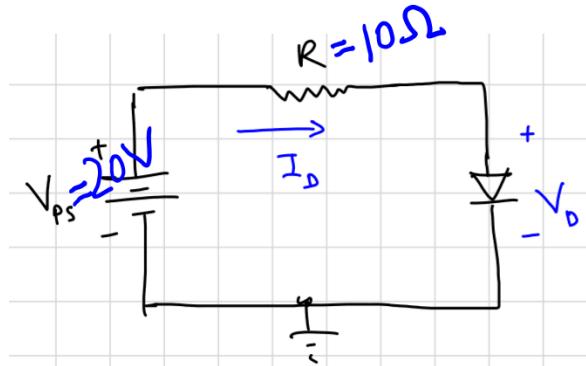
Take each box to be 0.25 eV on all sides



- We have drawn Diode I-V curve on the figure. From the figure, extract g_d from the curve. Then use the piecewise linear model of the curve to find the cut-in (turn-on) voltage. Label the voltage and include your work.



- Now we apply this pn junction in the following circuit. Based on the Diode I-V curve we drew, sketch and label load line, Q-point exactly on the I-V curve graph. And sketch what will happen to the load line and Q-points if we increase the resistance of R.



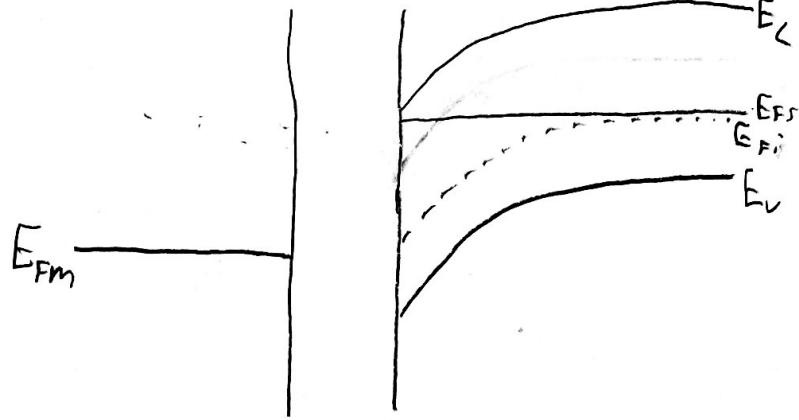
MOS Capacitors

Given the energy band diagram of an MOS Capacitor below, with the parameters indicated below, answer the questions.

$$\phi_F = 0.342V \quad t_{ox} = 120\text{ Å} \quad \phi_{ms} = -1.19V \quad Q_{ss} = 4 \times 10^0 \text{ cm}^{-2} \quad f = 10 \text{ Hz}$$

$$= 12 \text{ nm}$$

- a. What type of MOS Capacitor is this?
- b. What is the doping concentration?
- c. Is this in equilibrium?
- d. Solve for flat-band voltage.
- e. Calculate threshold voltage.

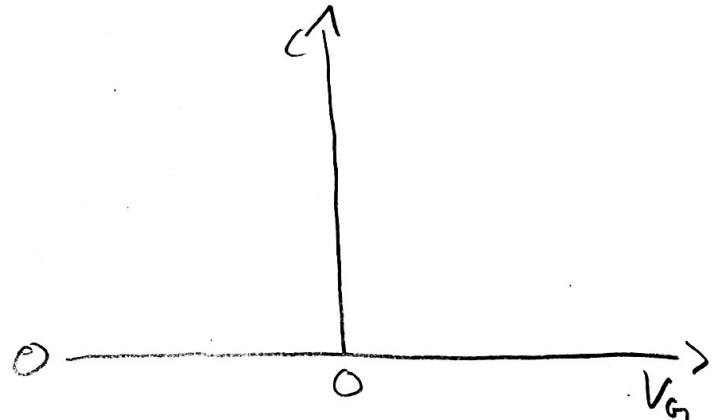


- f. Is this in inversion, depletion, or accumulation?
- g. Sketch V_g & complete the energy band diagram.

For the C-V curve:

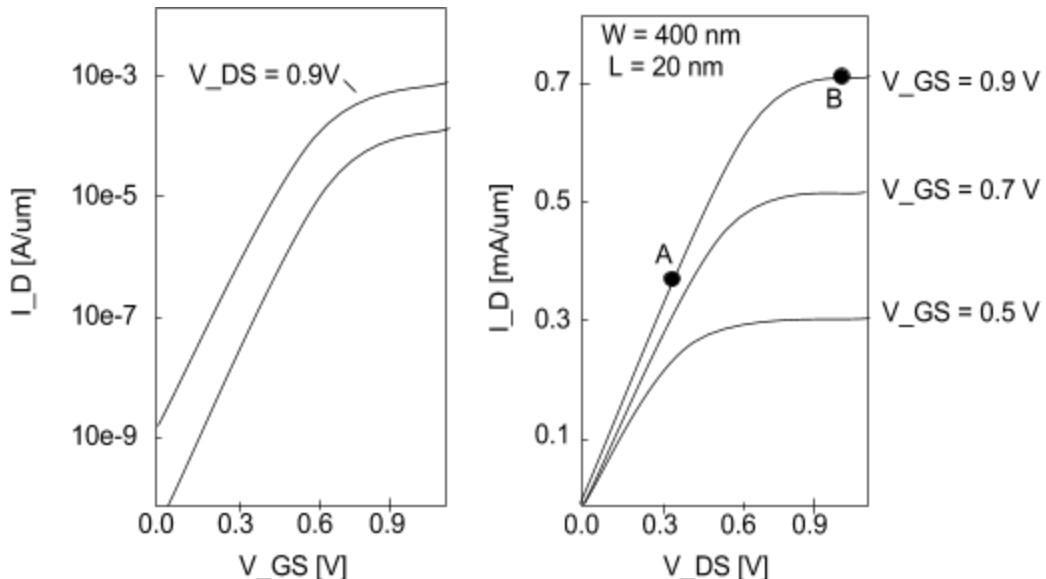
- h. Sketch the C-V curve for this capacitor on the axes to the right and label

V_t , V_{FB} , C_{ox} , C_{min} . Also label accumulation, depletion, & inversion mode.

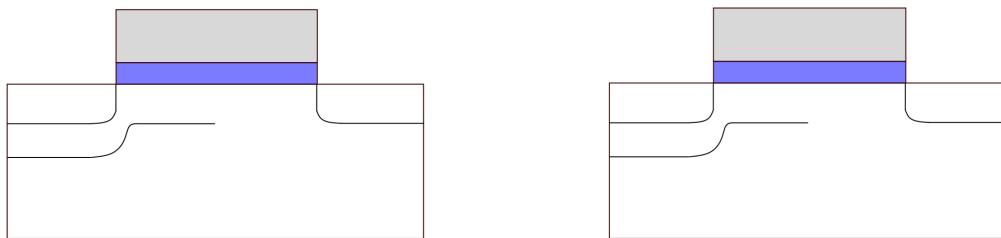


ECE 230 Exam Question - MOSFETs 1

Consider a Si MOSFET with the below characteristics curve

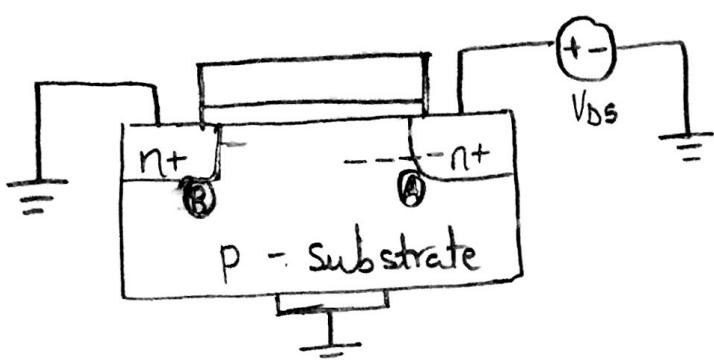


- Fill in the names of the characteristic plots above:
- Given the operating voltage for the MOSFET is 0.9 V , and $K_n = K_p = 4.97 * 10^{-4}\text{ A/V}^2$, please derive the following characteristics from the curves above
 - Transconductance _____
 - On Current _____
 - Subthreshold Swing _____
 - MOSFET N or P Type? _____
 - Threshold Voltage _____
- For point A (left diagram) and point B (right diagram) on the graphs, label the following components on each MOSFET Intersection: Source, Body, Drain Doping, Remaining Depletion Layer, Inversion Layer



MOSFETS - 2

CONCEPTUAL



- ① What type of MOSFET is this?
- ② What is the polarity of the pn-junction labelled A.
- ③ What is the bias range of the pn-junction labelled B.

④ Explain what would happen to the drain-to-source current if the polarity of V_{DS} was reversed.

⑤ On the diagram, label the dimension h .

⑥ For $V_{DS} = 0$ and $V_{GS} > V_{TN}$, write an expression for the gate-to-source capacitance in terms of W , L and t_{ox} .

⑦ Draw the inversion and depletion layers for the MOSFET operating in saturation mode.

⑧ On the same diagram, draw the inversion channel for $\lambda > 0$.

Final Question: Inverters

1. You are given $V_{DD} = 5V$, a $20 \text{ k}\Omega$ resistor, and the following SiO_2 NMOS and PMOS to create inverters.

Type	μ	t_{ox}	V_T	W	L
NMOS	$600 \frac{\text{cm}^2}{\text{Vs}}$	2 nm	0.7V	10 nm	50 nm
PMOS	$600 \frac{\text{cm}^2}{\text{Vs}}$	2 nm	-0.7V	10 nm	50 nm

- (a) Using the given items, design/draw and label R , K_p , K_n when applicable:
- Resistor-NMOS Inverter
 - NMOS-NMOS Inverter
 - CMOS Inverter
- (b) For each, find the transition point and generally sketch the plot for each of the three designs' transfer curves.
- (c) find the power dissipated by each design.

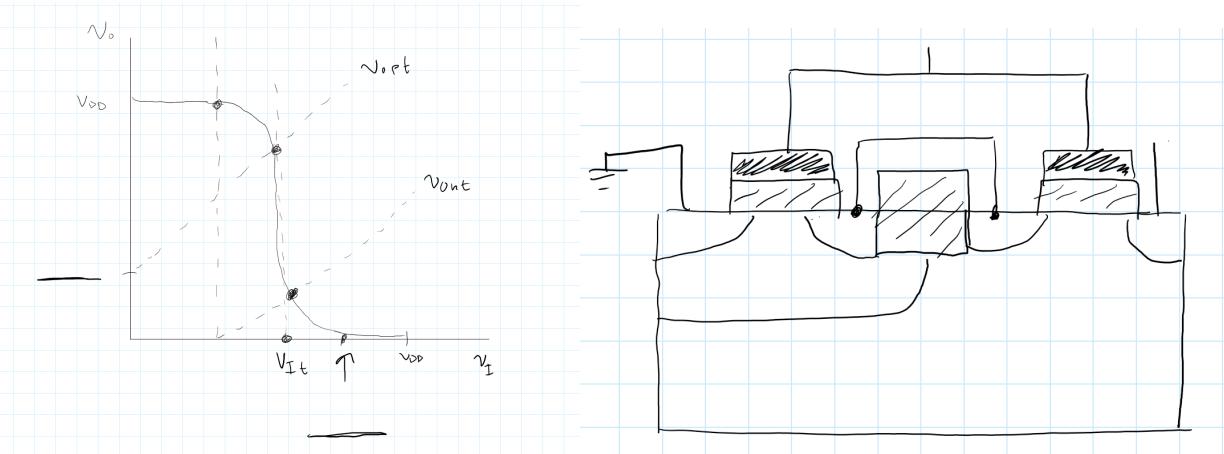
i Resistor-NMOS Inverter

ii NMOS-NMOS Inverter

iii CMOS Inverter

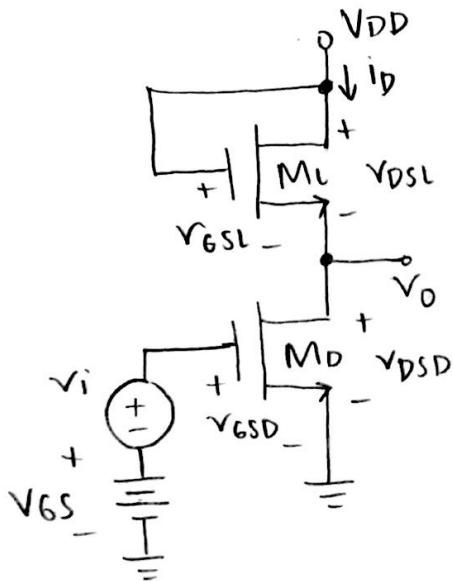
CMOS DIGITAL LOGIC

- A. Label the diagram (right) of a CMOS inverter assuming an n-type substrate including:
 Drain, Source, Input, Output, Doping regions, Operating Voltage (V_{DD})
 B. Label the voltages indicated on this plot of transfer characteristics (left) of a CMOS inverter



- C. Give two reasons why a CMOS digital logic circuit is preferable to a conventional NMOS inverter.
 Hint: Two of the possible reasons can be explained by seeing the transfer curve above
- D. Design a CMOS digital logic circuit to implement the logic function: $ABC + D$
- E. Given a CMOS based digital logic circuit with 3.8 million CMOS inverters, biased at $V_{DD} = 2.2$ V, and is switched at 3.2 MHz, evaluate the average power dissipation. Assume each inverter equivalent capacitance is 0.12 pF.

11 Linear Amplifiers



Consider the NMOS amplifier with saturated load in the figure to the left. The transistor parameters are $V_{INL} = V_{NL} = 0.6 \text{ V}$, $k_n' = 50 \mu\text{A}/\text{V}^2$, $\lambda = 0$, and $(\frac{W}{L})_L = 1$. Let $V_{DD} = 2.5 \text{ V}$.

a) Design the circuit such that the small-signal voltage gain is $|Av| = 5$ and the Q-point is in the center of the region.

b) Draw the transfer characteristics on the plot below. Be sure to label the ideal Q-point and the transition point.

c) Determine I_{DQ} :

$$I_{DQ} = \underline{\hspace{2cm}}$$

d) Determine V_{DSQ} :

$$V_{DSQ} = \underline{\hspace{2cm}}$$

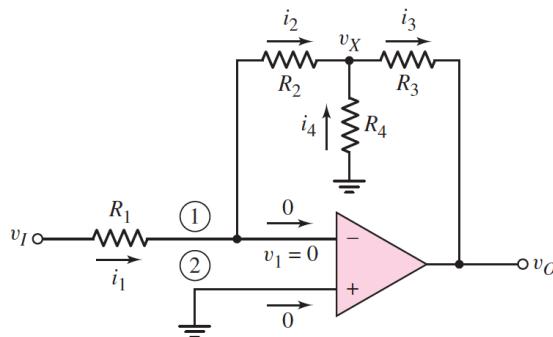
e) Redo part a), but this time with a small-signal voltage gain of $|Av| = 10$.

Create the Final Exam Project

Group 12 – Op-Amps

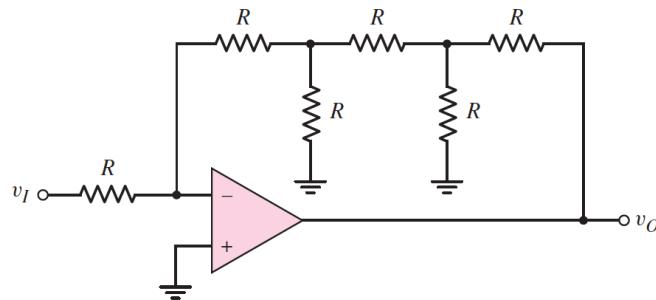
Op-Amps

A. Given the op-amp circuit shown below, give an expression for the gain, $A_v = v_0/v_i$:



B. Given that $R_1 = R_2 = R_3 = R_4$, find the gain of the circuit. What happens if $R_4 \rightarrow \infty$?

C. Find the gain, $A_v = v_0/v_i$, of the circuit shown below, given that all resistance values are the same:



D. Given that $R_1 = 10 \text{ k}\Omega$, $R_2 = 20\text{k}\Omega$, and $R_3 = 10 \text{ k}\Omega$ from part A, what should the value of R_4 such that the gain is same from part C?

E. What are the three of the four assumptions of the ideal op-amp?

1. _____
2. _____
3. _____