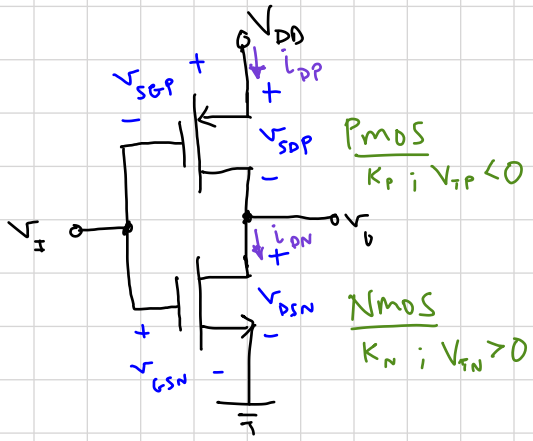
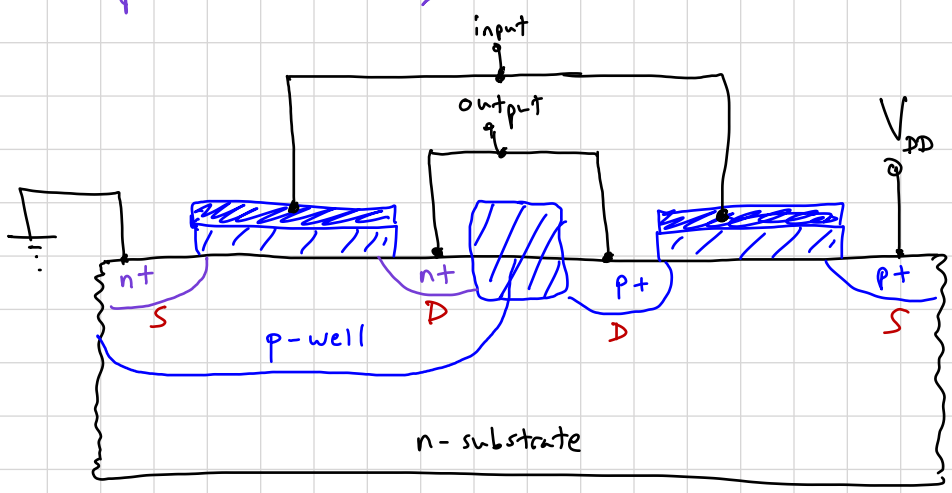
Lecture #17

CMOS Inverters & Logic Gates

CMOS digital circuits have much lower power dissipation than NMOS-only
→ contains NMOS & PMOS transistors (enhancement mode!)

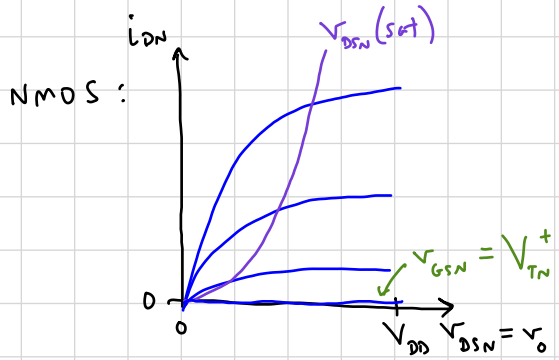
CMOS Inverter

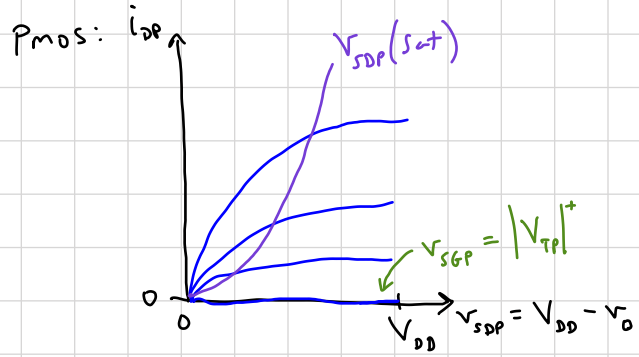


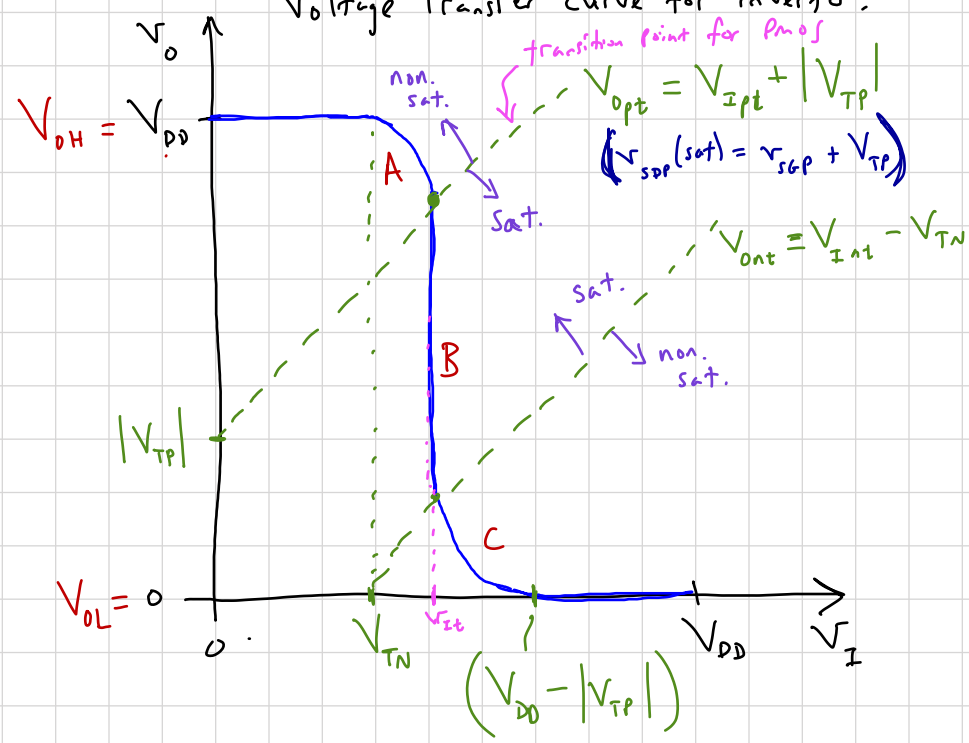


→ more complex than NMOS-only, but it's worth it!

Voltage Transfer curve for inverter:



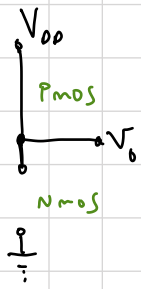




Operation

$v_I = 0$: NMOS is off, $i_{DN} = 0$, $i_{DP} = 0$
PMOS is on, $v_{SGP} = V_{DD}$

$\therefore v_O = V_{DD}$



$v_I = V_{DD}$: PMOS is off, $i_{DP} = 0 = i_{DN}$
NMOS is on, $v_{GSN} = V_{DD}$

$\therefore v_O = 0$

★ ideally, current is zero in either condition

A: NMOS in sat., PMOS in non-sat.

$i_{DN} = i_{DP}$

$$K_n\left[v_{GSN} - V_{TN}\right]^2 = K_p\left[2\left(v_{SGP} + V_{TP}\right)v_{SDP} - v_{SDP}^2\right]$$

$$K_n\left[v_I - V_{TN}\right]^2 = K_p\left[2\left(V_{DD} - v_I + V_{TP}\right)\left(V_{DD} - v_O\right) - \left(V_{DD} - v_O\right)^2\right]$$

B: NMOS and PMOS in sat. (transition point)

→ ideal case: $V_{Ipt} = V_{Int} = v_{It}$

$i_{Dn}(sat) = i_{Dp}(sat)$

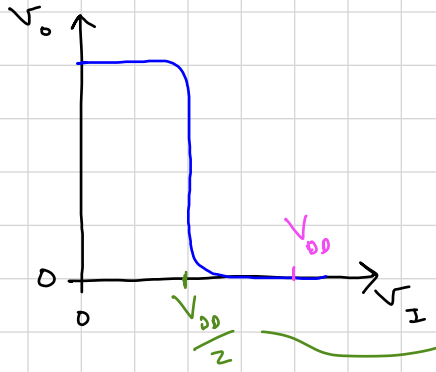
$$K_n\left(v_I - V_{TN}\right)^2 = K_p\left(V_{DD} - v_I + V_{TP}\right)^2$$

$$\Rightarrow v_I = \frac{V_{DD} + V_{TP} + \sqrt{\frac{K_n}{K_p}}\,V_{TN}}{1 + \sqrt{\frac{K_n}{K_p}}}$$

C: NMOS is non-sat, PMOS in sat: $K_n\left[2\left(v_I - V_{TN}\right)v_O - v_O^2\right] = K_p\left(V_{DD} - v_I + V_{TP}\right)^2$

Transistor Sizing

→ PMOS device is typically larger than NMOS to achieve $k_p = k_n$



→ To achieve $V_{It} = \frac{V_{DD}}{2}$, we must have NMOS & PMOS matched

$\therefore k_n = k_p \rightarrow k_n'\left(\frac{W}{L}\right)_n = k_p'\left(\frac{W}{L}\right)_p$

Since $k_p' < k_n'$ typically must have: $\left(\frac{W}{L}\right)_p > \left(\frac{W}{L}\right)_n$

Power Dissipation

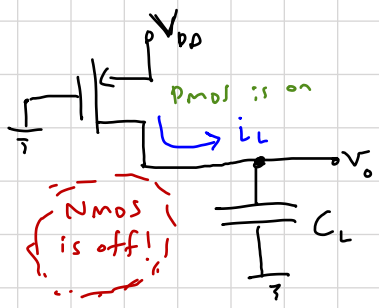
→ when inverter is held at static logic "1" or "0" → no power dissipated

→ switching between states, current flows and power dissipates

→ Each CMOS circuit drives another CMOS circuit, which is like a capacitive load:

switching low-to-high

"pull-up mode"



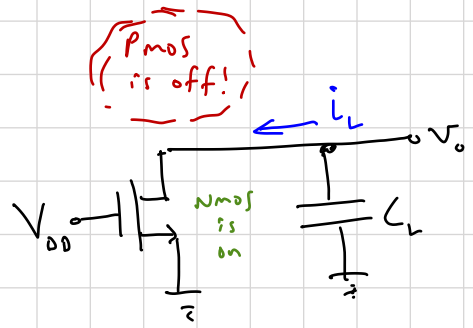
→ PMOS current must charge C_L:

$$i_L = C_L \frac{dv_o}{dt}$$

→ Energy dissipated: $E_p = \frac{1}{2} C_L V_{DD}^2$

switching from high-to-low

"pull-down mode"



→ Energy stored in C_L now dissipated through NMOS

$$E_n = \frac{1}{2} C_L V_{DD}^2$$

Total E dissipated in one switching cycle:

$$E_T = E_n + E_p = C_L V_{DD}^2$$

$\therefore$ Power dissipated at frequency f: $\boxed{P = f C_L V_{DD}^2}$ ★

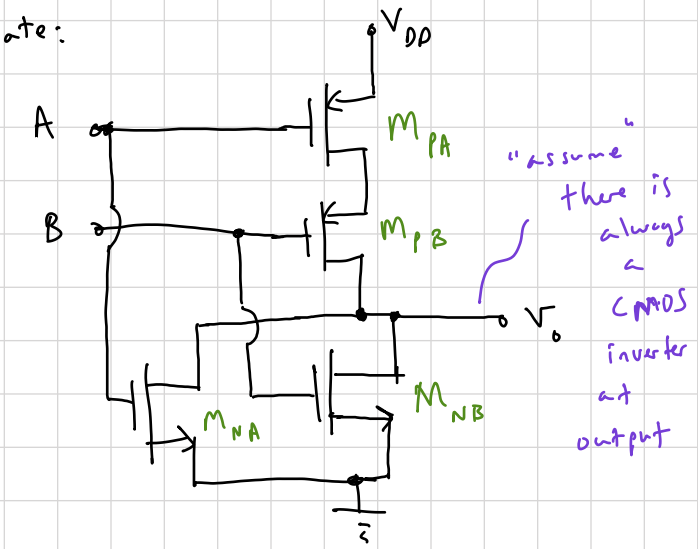
CMOS Logic Circuits

→ How do you determine their function?

★ "1" → V_{DD} input yields PMOS off and NMOS on, and vice versa for "0" → 0 input

★ AND: parallel PMOS, series NMOS
OR: parallel NMOS, series PMOS

2-input OR gate:



A	B	V_o	
0	0	V_{DD}	0
0	V_{DD}	0	V_{DD}
V_{DD}	0	0	V_{DD}
V_{DD}	V_{DD}	0	V_{DD}