

## Homework #8

[Solutions](#)

NMOS and CMOS Digital Logic – **100 points**

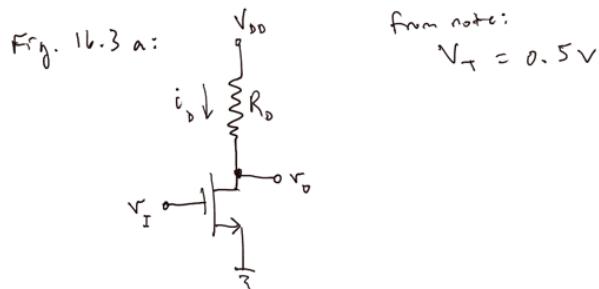
**DUE @ Beginning of Class: Tuesday, November 7**

\*Be sure to use the information in the “Note” on pg. 930 of the E-book for all problems.

- 1) E-Book, problem 16.2 (**12 points**)
- 2) E-Book, problem D16.3 (**12 points**)
- 3) E-Book, problem 16.5 (parts a & b only) (**8 points**)
- 4) E-Book, problem 16.13 (parts a & b only), note that  $P = i_D V_{DD}$  (**16 points**)
- 5) E-Book, problem 16.31 (**12 points**)
- 6) E-Book, problem 16.34 (**12 points**)
- 7) E-Book, problem 16.40 (**6 points**)
- 8) E-Book, problem 16.48, hint: this is the XOR of two basic logic operations (**12 points**)
- 9) E-Book, problem D16.58 (part a only) (**10 points**)

1) E-Book, problem 16.2 (12 points)

- 16.2 The inverter circuit in Figure 16.3(a) is biased at  $V_{DD} = 3.3$  V. Assume the transistor conduction parameter is  $K_n = 50 \mu\text{A}/\text{V}^2$ . (a) Let  $R_D = 100 \text{k}\Omega$ . (i) Determine the transition point. (ii) Determine  $v_o$  for  $v_I = 3.3$  V. (b) Repeat part (a) for  $R_D = 30 \text{k}\Omega$ . (c) Repeat part (a) for  $R_D = 5 \text{k}\Omega$ .



a)  $R_D = 100 \text{k}\Omega$

i. From lecture, at the transition point:  $K_n R_D (V_{IT} - V_{TN})^2 + (V_{OT} - V_{TN}) - V_{DD} = 0$   
 $(0.05 \text{ mA/V}^2)(100 \text{k}\Omega) V_{OT}^2 + V_{OT} - 3.3 \text{ V} = 0$   
 $\Rightarrow V_{OT} = 0.719 \text{ V}, V_{IT} = 1.22 \text{ V}$

ii.  $V_I = 3.3 \text{ V}$

From lecture notes, in  $V_I > V_{IT}$

$$V_O = V_{DD} - R_D i_D$$

$$V_O = V_{DD} - R_D K_n [2(V_I - V_{TN}) V_O - V_O^2]$$

$$V_O = 3.3 \text{ V} - (100 \text{k}\Omega)(0.05 \text{ mA/V}^2)[2(3.3 \text{ V} - 0.5 \text{ V}) V_O - V_O^2]$$

$$\Rightarrow 5V_O^2 - 29V_O + 3.3 \text{ V} = 0 \Rightarrow V_O = 0.116 \text{ V}$$

b)  $R_D = 30 \text{k}\Omega$

Using the same approach as part a), yields:

i.  $V_{OT} = 1.19 \text{ V}, V_{IT} = 1.69 \text{ V}$

4

ii.  $V_O = 0.373 \text{ V}$

c)  $R_D = 5 \text{k}\Omega$

i.  $V_{OT} = 2.15 \text{ V}, V_{IT} = 2.65 \text{ V}$

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ii.  $V_O = 1.66 \text{ V}$

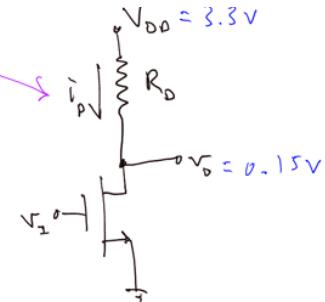
2) E-Book, problem D16.3 (12 points)

- D16.3 (a) Redesign the resistive load inverter in Figure 16.3(a) so that the maximum power dissipation is 0.25 mW with  $V_{DD} = 3.3 \text{ V}$  and  $v_O = 0.15 \text{ V}$  when the input is a logic 1. (b) Using the results of part (a), what is the input voltage range when the transistor is biased in the saturation region?

$$a) P = IV$$

$$0.25 \text{ mW} = I (3.3 \text{ V}) \rightarrow I = 75.8 \mu\text{A}$$

$$\therefore R = \frac{3.3 \text{ V} - 0.15 \text{ V}}{75.8 \times 10^{-6} \text{ A}} = 41.6 \text{ k}\Omega \quad 2$$



$v_o$  is low, hence linear region and:

$$i_o = \frac{k_n'}{2} \left( \frac{W}{L} \right) [2(v_i - V_{TN}) v_o - v_o^2]$$

$$75.8 \mu\text{A} = \left( \frac{100 \text{ mA/V}^2}{2} \right) \left( \frac{W}{L} \right) [2(3.3 \text{ V} - 0.5 \text{ V})(0.15 \text{ V}) - (0.15 \text{ V})^2]$$

$$\Rightarrow \left( \frac{W}{L} \right) = 1.85 \quad 2$$

b) In saturation:

$$i_o = \frac{k_n'}{2} \left( \frac{W}{L} \right) (v_i - V_{TN})^2 = \frac{V_{DD} - V_{DS(\text{sat})}}{R}$$

$$\left( \frac{0.1 \text{ mA/V}^2}{2} \right) (1.85) (V_{DS(\text{sat})})^2 = \frac{3.3 \text{ V} - V_{DS(\text{sat})}}{41.6 \text{ k}\Omega}$$

$$\Rightarrow 3.848 V_{DS(\text{sat})}^2 + V_{DS(\text{sat})} - 3.3 \text{ V} = 0 \rightarrow V_{DS(\text{sat})} = 0.805 \text{ V}$$

$$\text{since: } V_{DS(\text{sat})} = v_i - V_{TN}$$

$$0.805 \text{ V} = v_i - 0.5 \text{ V} \rightarrow v_i = 1.305 \text{ V} \quad 4$$

Since  $v_i > V_{TN}$  to be on, the range for saturation is:

$$0.5 \text{ V} \leq v_i \leq 1.305 \text{ V}$$

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3) E-Book, problem 16.5 (parts a & b only) (8 points)

- 16.5 An NMOS inverter with saturated load is shown in Figure 16.5(a). The bias is  $V_{DD} = 3 \text{ V}$  and the transistor threshold voltages are  $0.5 \text{ V}$ . (a) Find the ratio  $K_D/K_L$  such that  $v_O = 0.25 \text{ V}$  when  $v_I = 3 \text{ V}$ . (b) Repeat part (a) for  $v_I = 2.5 \text{ V}$ . (c) If  $W/L = 1$  for the load transistor, determine the power dissipation in the inverter for parts (a) and (b).

$$a) v_o = 0.25 \text{ V}, v_i = 3 \text{ V}, \frac{K_D}{K_L} = ?$$

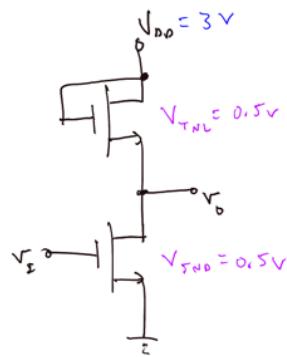
Since  $v_i = v_{DD}$  and  $v_o$  is low:

$$i_{DD}(\text{lin}) = i_{D2}(\text{sat})$$

$$K_D [2(v_i - V_{TN0})(v_o - V_{TN0})] = K_L [v_{DD} - v_o - V_{TN0}]^2$$

$$\frac{K_D}{K_L} [2(3\text{V} - 0.5\text{V})(0.25\text{V}) - (0.25\text{V})^2] = (3\text{V} - 0.25\text{V} - 0.5\text{V})^2$$

$$\Rightarrow \frac{K_D}{K_L} = 4.26 \quad 4$$



b) Repeat for  $v_i = 2.5 \text{ V}$ :

Same approach as part a) since  $v_i$  still high

$$\Rightarrow \frac{K_D}{K_L} = 5.4 \quad 4$$

4) E-Book, problem 16.13 (parts a & b only), note that  $P = i_D V_{DD}$  (16 points)

- 16.13 Calculate the power dissipated in each inverter circuit in Figure P16.13 for the following input conditions: (a) Inverter a: (i)  $v_I = 0.5 \text{ V}$ , (ii)  $v_I = 5 \text{ V}$ ; (b) Inverter b: (i)  $v_I = 0.25 \text{ V}$ , (ii)  $v_I = 4.3 \text{ V}$ ; (c) Inverter c: (i)  $v_I = 0.03 \text{ V}$ , (ii)  $v_I = 5 \text{ V}$ .

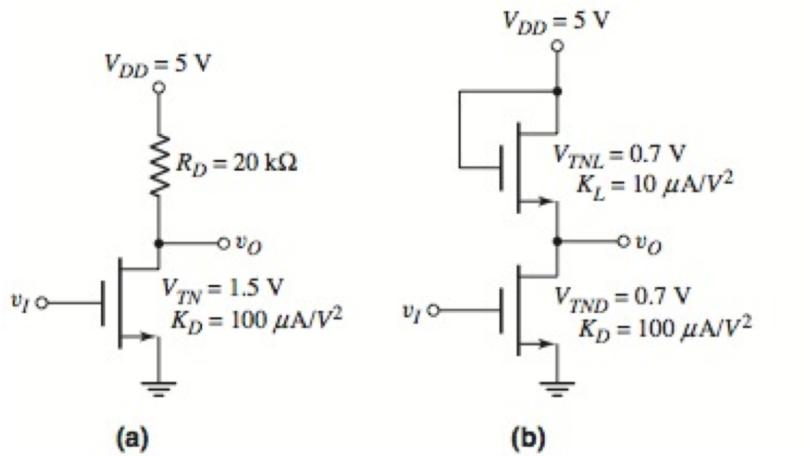


Figure P16.13

$$a) i. v_I = 0.5 \text{ V}$$

$$v_I < V_{TN}$$

$$i_D = 0$$

$$\therefore P = 0$$

2

$$i. v_x = 5 \text{ V}$$

$$v_x = V_{DD} > V_{IT}$$

$$i_D = K_n [2(v_x - V_{TN})v_o - v_o^2]$$

$$\text{and } v_o = V_{DD} - R_D i_D$$

$$v_o = V_{DD} - R_D K_n [2(v_x - V_{TN})v_o - v_o^2]$$

$$v_o = 5 \text{ V} - (20 \text{ k}\Omega)(0.1 \text{ mA/V}^2)[2(5 \text{ V} - 1.5 \text{ V})v_o - v_o^2]$$

$$\Rightarrow v_o = 0.35 \text{ V}$$

$$i_D = \frac{V_{DD} - v_o}{R_D} = \frac{5 \text{ V} - 0.35 \text{ V}}{20 \text{ k}\Omega} = 0.233 \text{ mA}$$

$$\therefore P = i_D V_{DD} = (0.233 \text{ mA})(5 \text{ V}) = 1.16 \text{ mW}$$

4

$$b) i. v_I = 0.25 \text{ V}$$

$$v_I < V_{TND}$$

$$i_{D2} = 0$$

$$\therefore P = 0$$

2

$$ii. v_x = 4.3 \text{ V}$$

$v_x$  is large, so assume  $v_x > V_{IT}$

$$K_n [2(v_x - V_{TND})v_o - v_o^2] = K_n (V_{DD} - v_o - V_{TND})^2$$

$$(100 \text{ mA/V}^2)[2(4.3 \text{ V} - 0.7 \text{ V})v_o - v_o^2] = (10 \text{ mA/V}^2)(5 \text{ V} - v_o - 0.7 \text{ V})^2$$

$$\rightarrow v_o = 0.237 \text{ V}$$

$$i_D = K_n (V_{DD} - v_o - V_{TND})^2 = (10 \text{ mA/V}^2)(5 \text{ V} - 0.237 \text{ V} - 0.7 \text{ V})^2$$

$$= 165 \mu\text{A}$$

$$\therefore P = i_D V_{DD} = (165 \mu\text{A})(5 \text{ V}) = 825 \mu\text{W}$$

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5) E-Book, problem 16.31 (12 points)

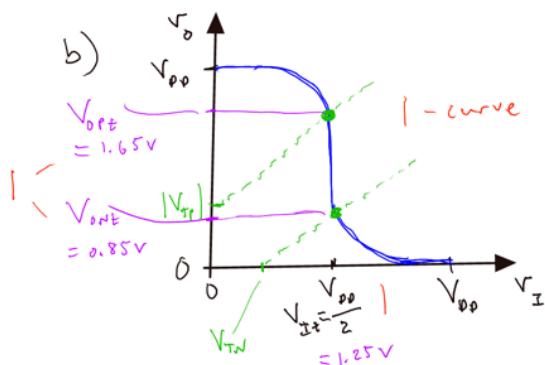
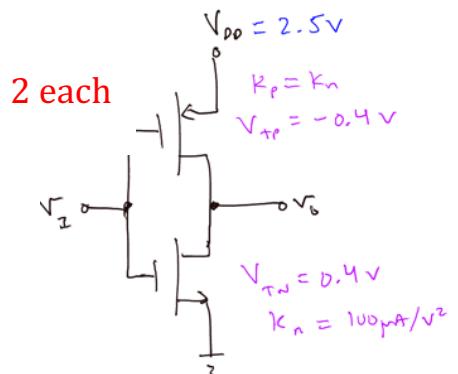
- 16.31 Consider the CMOS inverter in Figure 16.21 biased at  $V_{DD} = 2.5\text{ V}$ . The transistor parameters are  $V_{TN} = 0.4\text{ V}$ ,  $V_{TP} = -0.4\text{ V}$ , and  $K_n = K_p = 100\text{ }\mu\text{A/V}^2$ . (a) Find the transition points for the p-channel and n-channel transistors. (b) Sketch the voltage transfer characteristics, including the appropriate voltage values at the transition points. (c) Determine  $v_o$  for  $v_i = 1.1\text{ V}$  and  $v_i = 1.4\text{ V}$ .

a)  $V_{opt}$ ,  $V_{xit}$  and  $V_{ont}$ ,  $V_{int}$

Since  $K_n = K_p$  :  $V_{xit} = \frac{V_{DD}}{2} = \frac{2.5\text{ V}}{2} = 1.25\text{ V}$

$$V_{opt} = V_{xit} + |V_{tp}| = 1.25\text{ V} + 0.4\text{ V} = 1.65\text{ V}$$

$$V_{ont} = V_{xit} - V_{tn} = 1.25\text{ V} - 0.4\text{ V} = 0.85\text{ V}$$



c)  $v_o$  for  $v_i = 1.1\text{ V}$

NMOS in sat., PMOS in non sat.

$$K_n [v_i - V_{TN}]^2 = K_p [2(v_{DD} - v_i + V_{TP})(V_{DD} - v_o) - (V_{DD} - v_o)^2]$$

$$\downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow \quad \downarrow$$

$$1.1\text{ V} \quad 0.4\text{ V} \quad 2.5\text{ V} \quad 1.1\text{ V} \quad -0.4\text{ V}$$

$$\Rightarrow V_o = 2.214\text{ V}$$

4

for  $v_i = 1.4\text{ V}$

NMOS in non sat., PMOS in sat.

$$K_n [2(v_i - V_{TN})v_o - v_o^2] = K_p (V_{DD} - v_i + V_{TP})^2$$

$$\Rightarrow V_o = 0.286\text{ V}$$

2

6) E-Book, problem 16.34 (12 points)

- 16.34 Consider the CMOS inverter pair in Figure P16.34. Let  $V_{TN} = 0.8 \text{ V}$ ,  $V_{TP} = -0.8 \text{ V}$ , and  $K_n = K_p$ . (a) If  $v_{O1} = 0.6 \text{ V}$ , determine  $v_I$  and  $v_{O2}$ . (b) Determine the range of  $v_{O2}$  for which both  $N_2$  and  $P_2$  are biased in the saturation region.

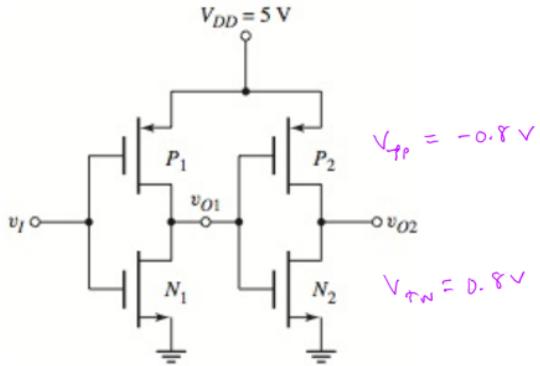


Figure P16.34

$$a) v_{O1} = 0.6 \text{ V}, v_I = ?, v_{O2} = ?$$

since  $v_{O1} < V_{TN}$ ,  $N_2$  is off and  $P_2$  is on  $\Rightarrow v_{O2} = 5 \text{ V}$  2

also, since  $v_{O1}$  is low,  $v_I \approx \text{high}$  and  $P_1$  in sat.,  $N_1$  in non-sat.

$$\cancel{K_p} [2(v_I - V_{TN})v_{O1} - v_{O1}^2] = \cancel{K_p}(V_{DD} - v_I + V_{TP})^2$$

$$2(v_I - 0.8 \text{ V})(0.6 \text{ V}) - (0.6 \text{ V})^2 = (5 \text{ V} - v_I - 0.8 \text{ V})^2$$

$$\rightarrow v_I = 2.78 \text{ V} \quad 4$$

$$b) v_{O2} \text{ range for } P_2 \text{ and } N_2 \text{ in sat.} \quad 2$$

$$V_{DNT} \leq v_{O2} \leq V_{opt}$$

$$\text{since } K_n = K_p, V_{Int} = V_{opt} = V_{It} = \frac{V_{DD}}{2} = 2.5 \text{ V}$$

$$V_{opt} = V_{It} + |V_{TP}| = 2.5 \text{ V} + 0.8 \text{ V} = 3.3 \text{ V}$$

$$V_{DNT} = V_{It} - V_{TN} = 2.5 \text{ V} - 0.8 \text{ V} = 1.7 \text{ V}$$

$$\therefore 1.7 \text{ V} \leq v_{O2} \leq 3.3 \text{ V} \quad 4$$

7) E-Book, problem 16.40 (6 points)

- 16.40 (a) A CMOS digital logic circuit contains the equivalent of 4 million CMOS inverters and is biased at  $V_{DD} = 1.8$  V. The equivalent load capacitance of each inverter is 0.12 pF and each inverter is switching at 150 MHz. Determine the total average power dissipated in the circuit. (b) If the switching frequency is doubled, but the total power dissipation is to remain the same with the same load capacitance, determine the required bias voltage.

a)  $C_L = 0.12 \text{ pF}$ ,  $f = 150 \text{ MHz}$

$$P = f C_L V_{DD}^2$$

units:  $\frac{1}{s} \frac{\text{C}}{\text{s}} \text{V}^2 = \text{A.V} = \text{W}$

$$= (150 \times 10^6 \text{ Hz}) (0.12 \times 10^{-12} \text{ F}) (1.8 \text{ V})^2 = 5.83 \times 10^{-5} \text{ W}$$

$\times 4 \times 10^6 \text{ inverters}$

233 W

3

b)  $f = 300 \text{ MHz}$

$$233 \text{ W} = (300 \times 10^6 \text{ Hz}) (0.12 \times 10^{-12} \text{ F}) (4 \times 10^6) V_{DD}^2$$

$\Rightarrow$

V<sub>DD</sub> = 1.27 V

3

8) E-Book, problem 16.48, hint: this is the XOR of two basic logic operations (12 points)

- 16.48 Consider the circuit in Figure P16.48. (a) The inputs  $v_X$ ,  $v_Y$ , and  $v_Z$  listed in the following table are either a logic 0 or a logic 1. These inputs are the outputs from similar-type CMOS logic circuits. The input logic conditions listed are sequential in time. State whether the transistors listed are “on” or “off,” and determine the output voltage. (b) What logic function does this circuit implement?

$v_X$	$v_Y$	$v_Z$	$N_1$	$N_2$	$N_3$	$N_4$	$N_5$	$v_O$	
1	0	1	off	on	off	on	on	0	8
0	0	1	off	off	on	on	off	0	
1	1	0	on	on	off	off	on	5V	
1	1	1	on	on	off	on	on	0	

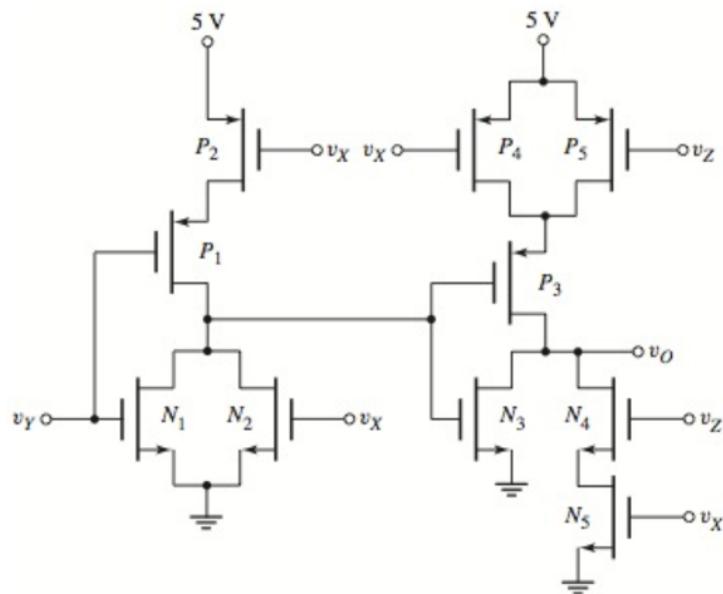


Figure P16.48

b) Logic function is  $(v_X \text{ OR } v_Y) \otimes (v_X \text{ AND } v_Z)$  4

Exclusive OR

9) E-Book, problem D16.58 (part a only) (10 points)

D16.58 (a) Given inputs  $A, B, C, D$ , and  $E$ , design a CMOS circuit to implement the logic function  $\bar{Y} = A(B + C) + D + E$ . (b) Repeat part (b) of Problem 16.57 for this circuit.

AND = parallel PMOS, series NMOS

OR = parallel NMOS, series PMOS

