Homework #8

NMOS and CMOS Digital Logic – *100 points*

DUE @ Beginning of Class: Tuesday, November 7

*Be sure to use the information in the "Note" on pg. 930 of the E-book for all problems.

1) E-Book, problem 16.2 (12 points)

2) E-Book, problem D16.3 (12 points)

3) E-Book, problem 16.5 (parts a & b only) (8 points)

4) E-Book, problem 16.13 (parts a & b only), note that $P = i_D V_{DD}$ (16 points)

5) E-Book, problem 16.31 (12 points)

6) E-Book, problem 16.34 (12 points)

7) E-Book, problem 16.40 (6 points)

8) E-Book, problem 16.48, hint: this is the XOR of two basic logic operations (12 points)

9) E-Book, problem D16.58 (part a only) (10 points)

1) E-Book, problem 16.2 (12 points)

16.2 The inverter circuit in Figure 16.3(a) is biased at $V_{DD} = 3.3$ V. Assume the transistor conduction parameter is $K_n = 50\,\mu\text{A/V}^2$. (a) Let $R_D = 100\,\text{k}\Omega$. (i) Determine the transition point. (ii) Determine v_O for $v_I = 3.3$ V. (b) Repeat part (a) for $R_D = 30\,\text{k}\Omega$. (c) Repeat part (a) for $R_D = 5\,\text{k}\Omega$.

2) E-Book, problem D16.3 (12 points)

D16.3 (a) Redesign the resistive load inverter in Figure 16.3(a) so that the maximum power dissipation is 0.25 mW with $V_{DD} = 3.3$ V and $v_O = 0.15$ V when the input is a logic 1. (b) Using the results of part (a), what is the input voltage range when the transistor is biased in the saturation region?

3) E-Book, problem 16.5 (parts a & b only) (8 points)

16.5 An NMOS inverter with saturated load is shown in Figure 16.5(a). The bias is $V_{DD} = 3$ V and the transistor threshold voltages are 0.5 V. (a) Find the ratio K_D/K_L such that $v_O = 0.25$ V when $v_I = 3$ V. (b) Repeat part (a) for $v_I = 2.5$ V. (c) If $W/L = 1$ for the load transistor, determine the power dissipation in the inverter for parts (a) and (b).

4) E-Book, problem 16.13 (parts a & b only), note that $P = i_D V_{DD}$ (16 points)

16.13 Calculate the power dissipated in each inverter circuit in Figure P16.13 for the following input conditions: (a) Inverter a: (i) $v_I = 0.5$ V, (ii) $v_I = 5$ V; (b) Inverter b: (i) $v_I = 0.25$ V, (ii) $v_I = 4.3$ V; (c) Inverter c: (i) $v_I = 0.03$ V, (ii) $v_I = 5$ V.

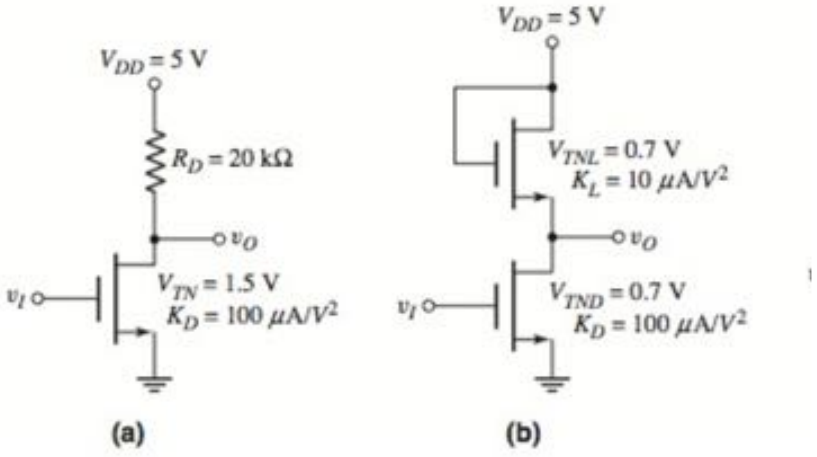

Figure P16.13

5) E-Book, problem 16.31 (12 points)

16.31 Consider the CMOS inverter in Figure 16.21 biased at $V_{DD} = 2.5\,\text{V}$. The transistor parameters are $V_{TN} = 0.4\,\text{V}$, $V_{TP} = -0.4\,\text{V}$, and $K_n = K_p = 100\,\mu\text{A/V}^2$. (a) Find the transition points for the p-channel and n-channel transistors. (b) Sketch the voltage transfer characteristics, including the appropriate voltage values at the transition points. (c) Determine v_O for $v_I = 1.1\,\text{V}$ and $v_I = 1.4\,\text{V}$.

6) E-Book, problem 16.34 (12 points)

16.34 Consider the CMOS inverter pair in Figure P16.34. Let $V_{TN} = 0.8$ V, $V_{TP} = -0.8$ V, and $K_n = K_p$. (a) If $v_{O1} = 0.6$ V, determine v_I and v_{O2}. (b) Determine the range of v_{O2} for which both N_2 and P_2 are biased in the saturation region.

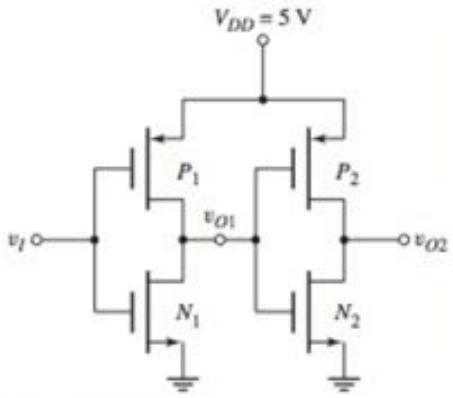

Figure P16.34

7) E-Book, problem 16.40 (6 points)

16.40 (a) A CMOS digital logic circuit contains the equivalent of 4 million CMOS inverters and is biased at $V_{DD} = 1.8$ V. The equivalent load capacitance of each inverter is 0.12 pF and each inverter is switching at 150 MHz. Determine the total average power dissipated in the circuit. (b) If the switching frequency is doubled, but the total power dissipation is to remain the same with the same load capacitance, determine the required bias voltage.

8) E-Book, problem 16.48, hint: this is the XOR of two basic logic operations (12 points)

16.48 Consider the circuit in Figure P16.48. (a) The inputs v_X, v_Y, and v_Z listed in the following table are either a logic 0 or a logic 1. These inputs are the outputs from similar-type CMOS logic circuits. The input logic conditions listed are sequential in time. State whether the transistors listed are "on" or "off," and determine the output voltage. (b) What logic function does this circuit implement?

v_X	v_Y	v_Z	N_1	N_2	N_3	N_4	N_5	v_O
1	0	1						
0	0	1						
1	1	0						
1	1	1						

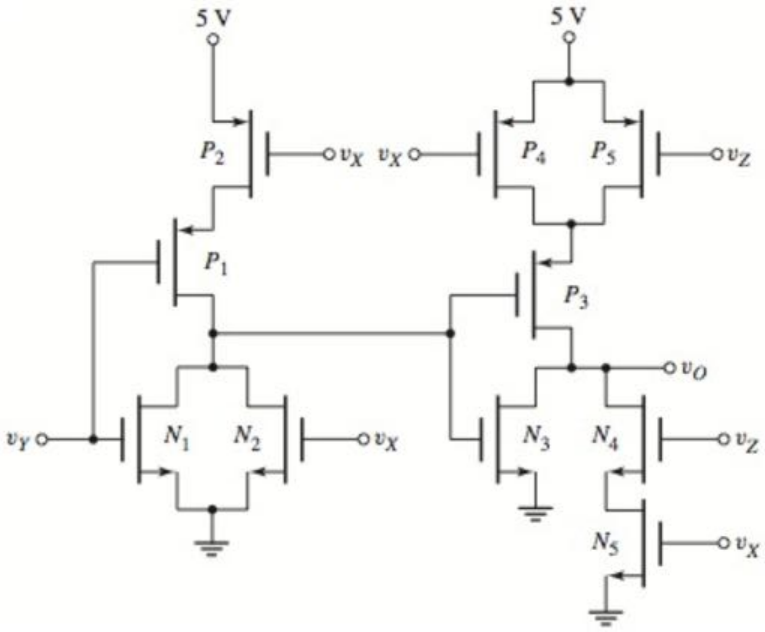

Figure P16.48

9) E-Book, problem D16.58 (part a only) (10 points)

D16.58 (a) Given inputs A, B, C, D, and E, design a CMOS circuit to implement the logic function $\bar{Y} = A(B + C) + D + E$. (b) Repeat part (b) of Problem 16.57 for this circuit.