GHz DER

Aaronia RTSA

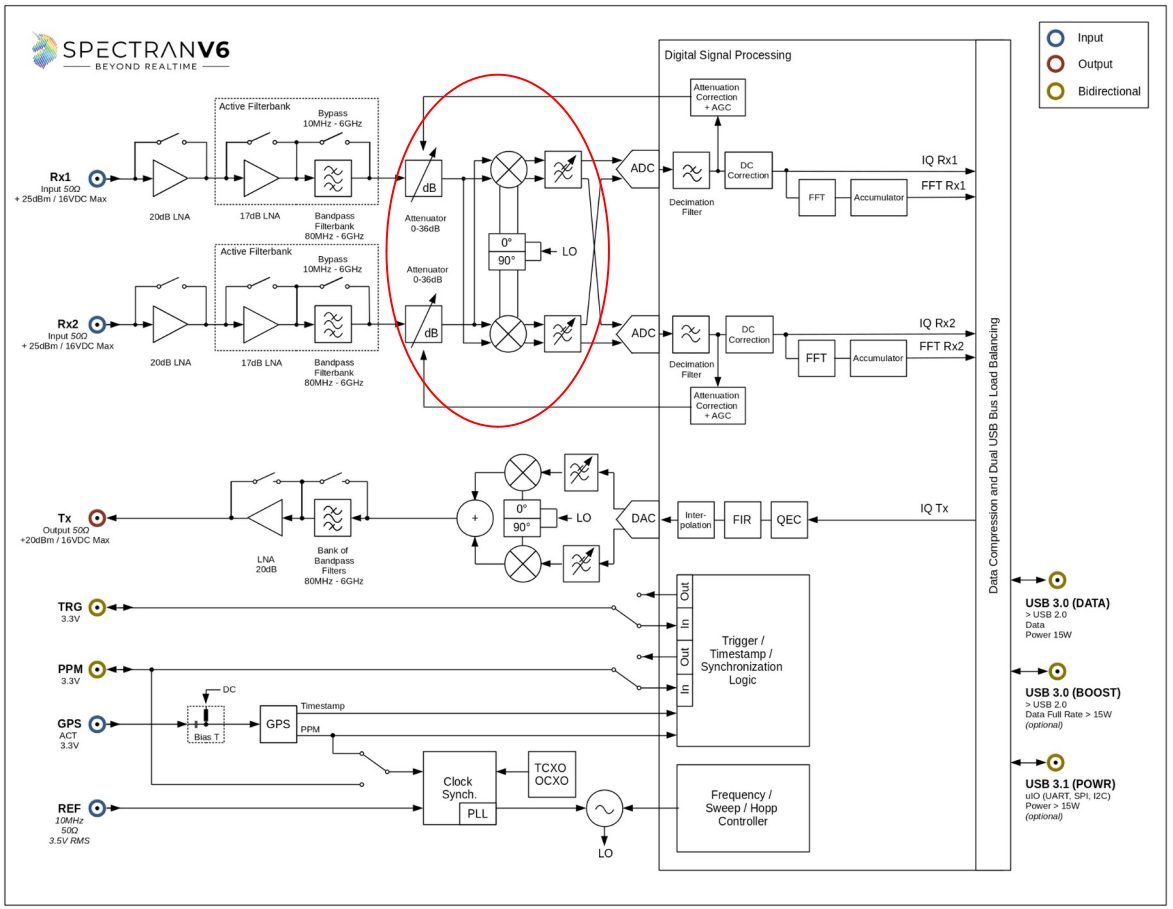
- 4.1GHz+-50MHz

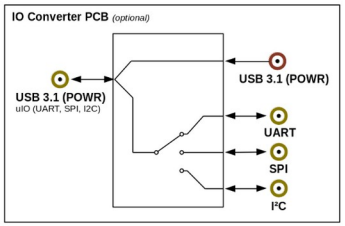
1 November 2022

UCDAVIS
DEPARTMENT OF PHYSICS AND ASTRONOMY

Amin Aminaei

Dynamic range from a 16-bit ADC at 2GSPS





https://aaronia.com/spectrum-analyzers/spectran-v6-usb-real-time/

https://downloads.aaronia.com/datasheets/analyzers/V6/Aaronia_Spectran_V6_X_Datasheet.pdf

Summary, Issues to be fixed

1M FFT, 870405 bins	• Not an answer yet	
DC offset, Peak at the centre of the spectrum	Use the SPECTRA output of the V6 block	
Big Data, Python crashes	Divide to sub-files	
How long integration (averaging) needed to reach to the spurs level?	• Need to resolve the big data taking issue first	

DC Offset of ADC, Bump at Centre Frequency

If i use the SPECTRAN with span = "Full" i have a small peak in the center of my spectrum which moves with frequency. Where is this signal coming from?

This is the so called "DC offset" from the ADC (analog to digital converter). Nearly every practical SDR with a quadrature mixer has this small center peak. First of all it is good to know that most modern modulations are designed to have no significant signal in the middle of their spectrum for this reason e.g. look at a typical Wifi. Engineers work around it in different ways:

1) For signals that don't require the total bandwidth you can tune above or below the signal frequency so it doesn't overlap with the DC offset.

2) Use smaller spans (1/2 or smaller spans) which will use the sideband instead. This will remove the DC completly and you get a clean spectrum.

3) Use high amplification (preamplifier) which will bring the DC offset below the noise floor (e.g. change the Reflevel to -50dBm or lower) and will also remove the DC completly and you get a clean spectrum.

4) **Use the SPECTRA output of the V6 block. This offers an advanced DC correction algorithm.**

with 1.048 MFFT, the bins are 870,000. Why Can't I get 1M bins over the full span? Shouldn't the FFT size and Bin numbers be the same? I use both POI and FFT Overlap but no changes.

https://v6-forum.aaronia.de/forum/topic/peak-in-the-center-of-my-spectrum/

Waterfall Data- Aaronia

-Basically, the Waterfall data is the same as the one from Spectrum block and it averages the power value within the defined time interval e.g. every 26 s .

Question from aminucd on 29/10/2022

What is the compressed data in Waterfall? e.g., when I set the compression ratio to 10, does it average the data every 10 units of time and record it? or does it simply register data less often (every 10 units of time) and ignore the rest?

You can configure that using the "Compression Mode" setting just below the "Time Compression" setting itself. By default it will select the maximum power value within the input range to be compressed, but you can change it to calculate the Average (logarithmic or normalized) or Minimum or just pick the first value.

https://v6-forum.aaronia.de/forum/topic/long-time-recording-and-ecxel-export/#postid-2196

Further Development

Aaronia V6 Spectran Extension of 6 GHz to 8GHz	License Purchased Waiting for installation	Expected this week
Aaronia **Existing** V6 Spectran Extension from 122 MHz to 245 MHz RTBW	Possible (confirmed from Aaronia Germany) **Quote provided $ 6K**	To be decided
Seperate Desktop/Server for Aaronia ? Python in Laptop Crashes Frequently		To be investigated
ADC Evaluation Board ROACH2	$ 3K+ capture card $3.5k Asking a quote?	Next Slide

ADC Evaluation board

Since we are going to spend on computing why not minimize the hardware and do all processing by software

ADC12DL3200EVM $3k

ADC12DL3200 12-bit, dual 3.2-GSPS or single 6.4-GSPS, RF-sampling ADC evaluation module

Requirements

Order the evaluation board - ADC12DL3200EVM

Order (if needed) the FPGA capture card - TSW14DL3200EVM

Download and install the GUI for the evaluation board

Download and install HSDC Pro software for the TSW14DL3200EVM capture card

ROACH2

Quote from CASPER?

A Low-cost 4 Bit, 10 Giga-samples-per-second Analog-to-digital Converter Printed Circuit Board Assembly for FPGA-based Backends, 2016

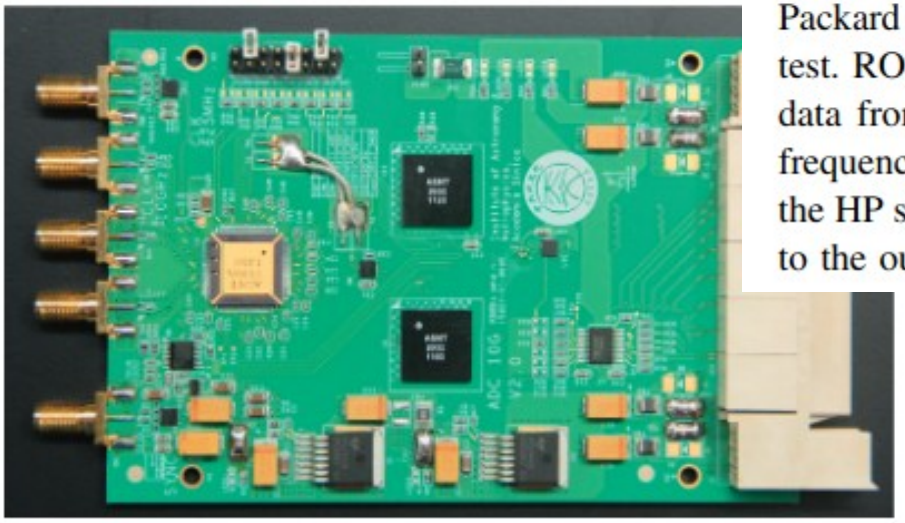


Figure 1. 4 bit, 10 GSPS ADC PCBA. The SMA connectors on the left-hand side (from the top) are for a 625 MHz internal clock (CN6), a 10 GHz external clock (CN5), signal input −(CN4), signal input +(CN2) and synchronization

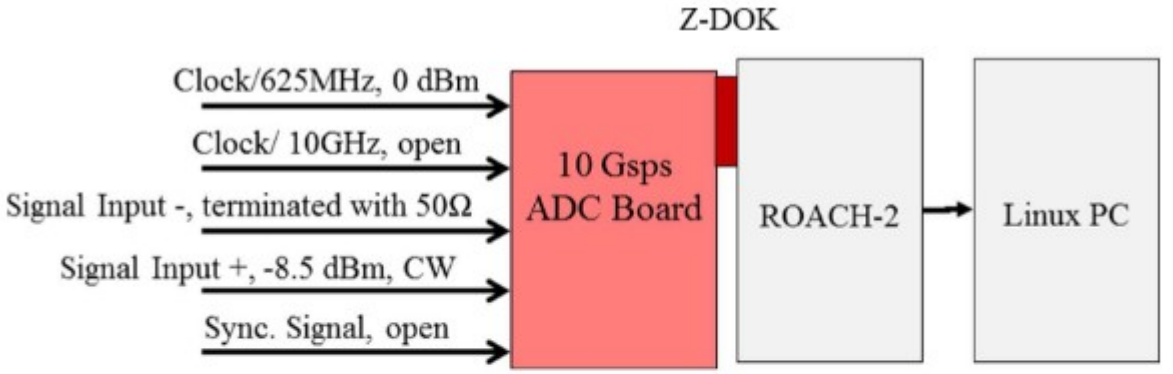
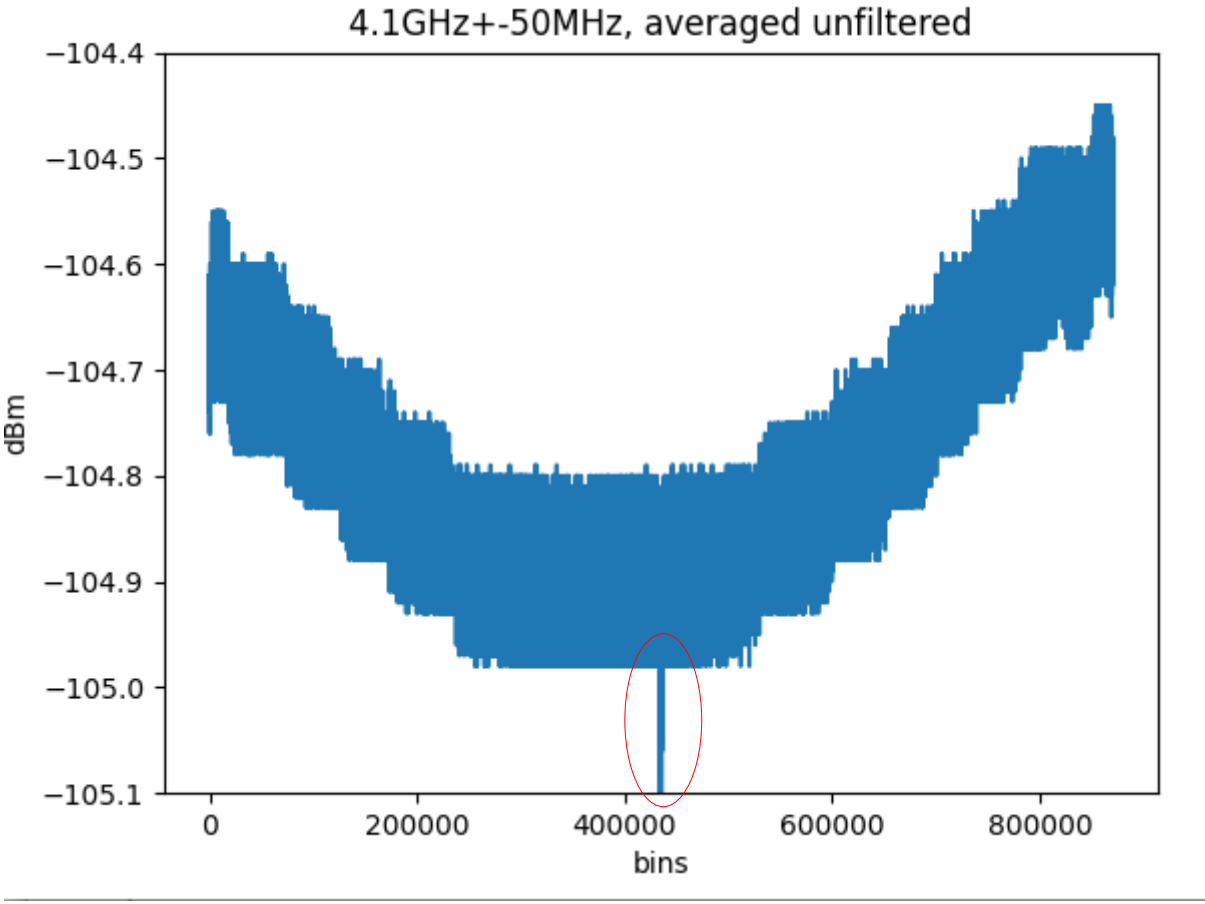
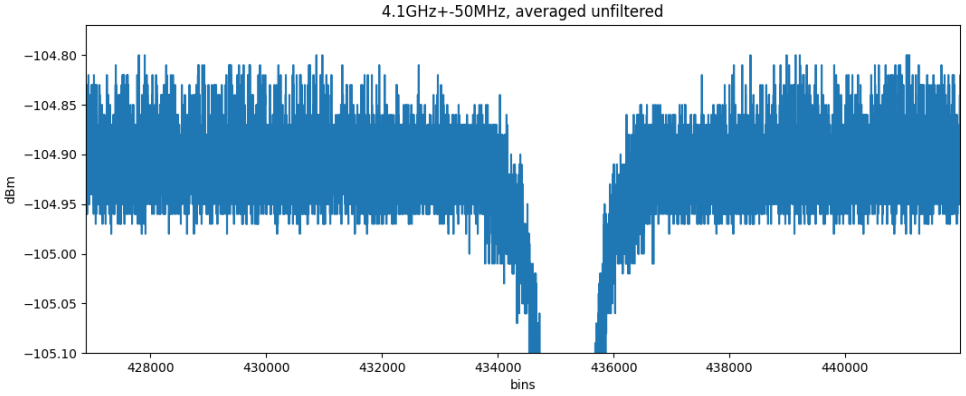


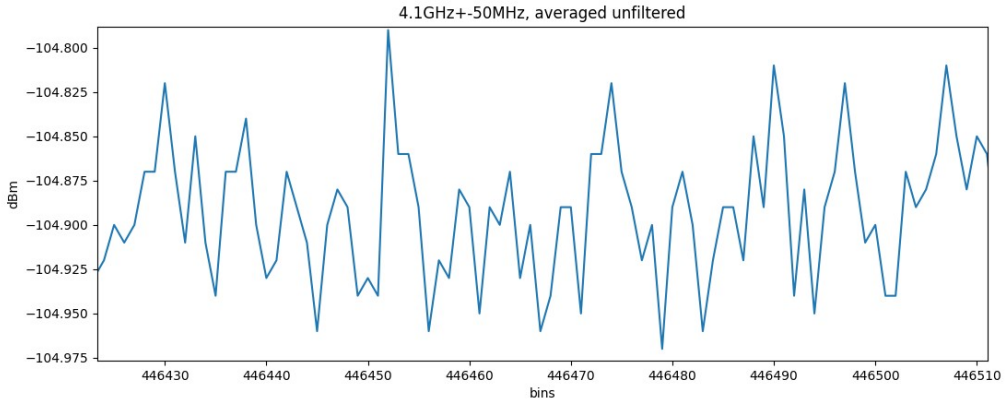
Figure 7. Calibration and test setup for the ADC. A CW source from a Hewlett Packard (HP) signal generator, 83630B, is used to stimulate the ADC under test. ROACH-2 and a Linux PC are used to capture and process the digitized data from the ADC. The internal 10 GHz clock is phase locked to a Valon frequency synthesizer board at 625 MHz. A 10 MHz clock signal generated by the HP signal generator was fed to the Valon board as the phase-lock reference to the output frequency.

https://www.jstor.org/stable/26660014#metadata_info_tab_contents

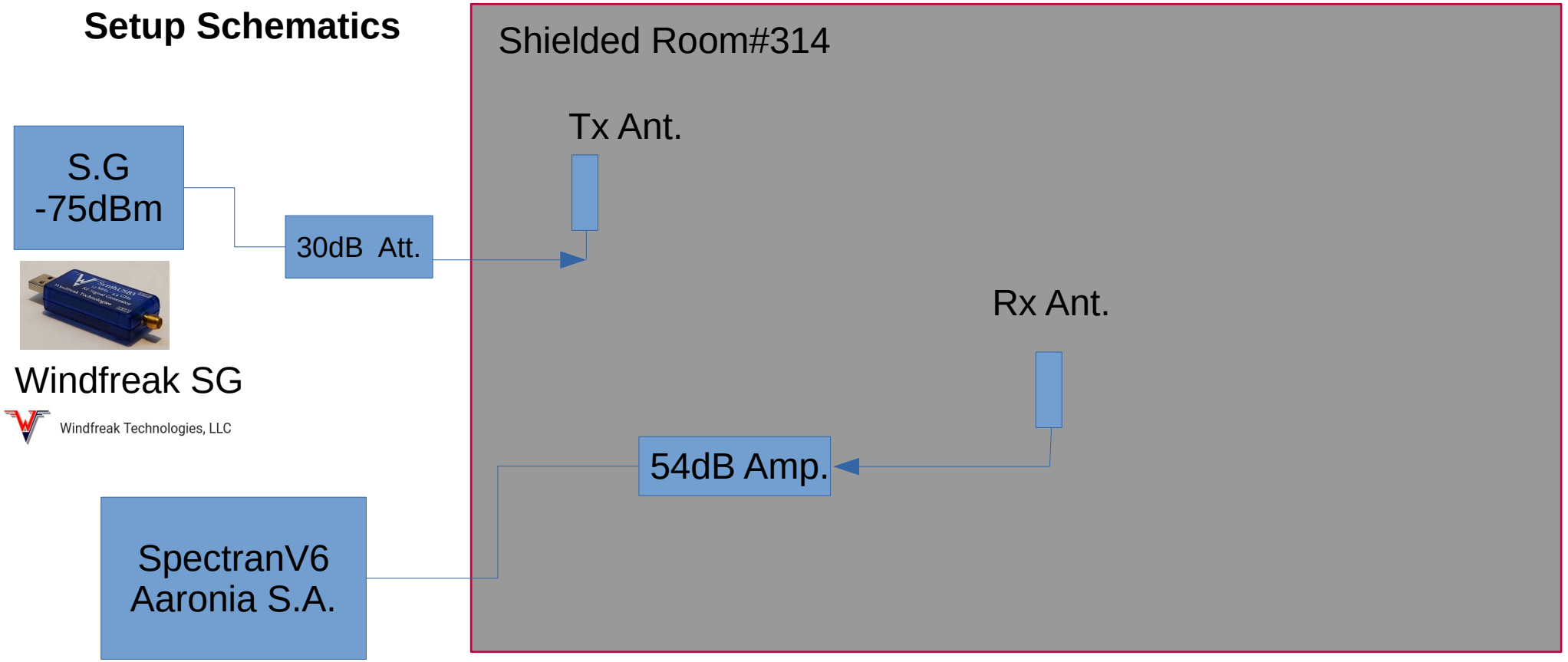
Aaronia Data -High Resolution
1M FFT, 117 Hz







Setup Schematics



Windfreak SG

Windfreak Technologies, LLC

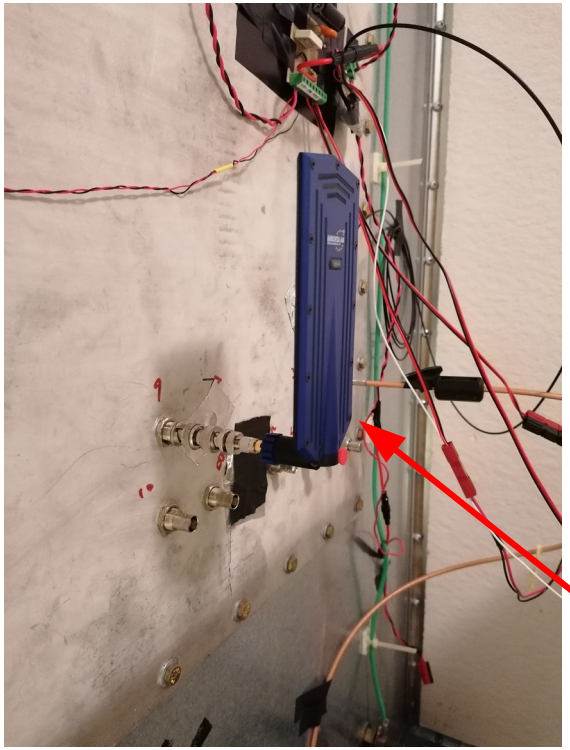
Calibration Tests:

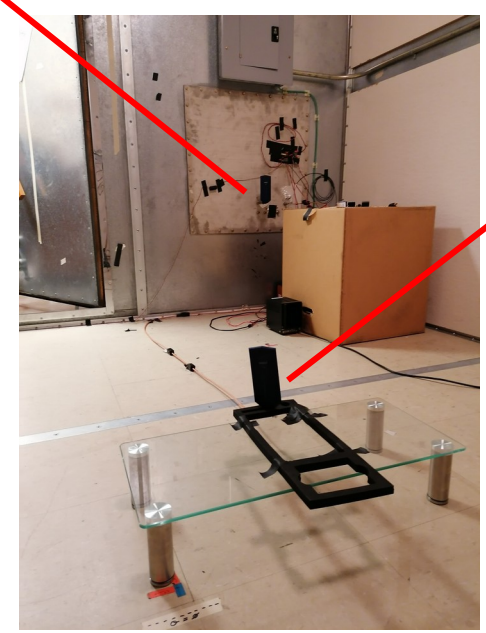
A. Without and With Amplifier
B. Without and With Transmitter
C. Terminated Load at the S.A port/ at the end of cable in the shielded room
D. With the Receiver Antenna

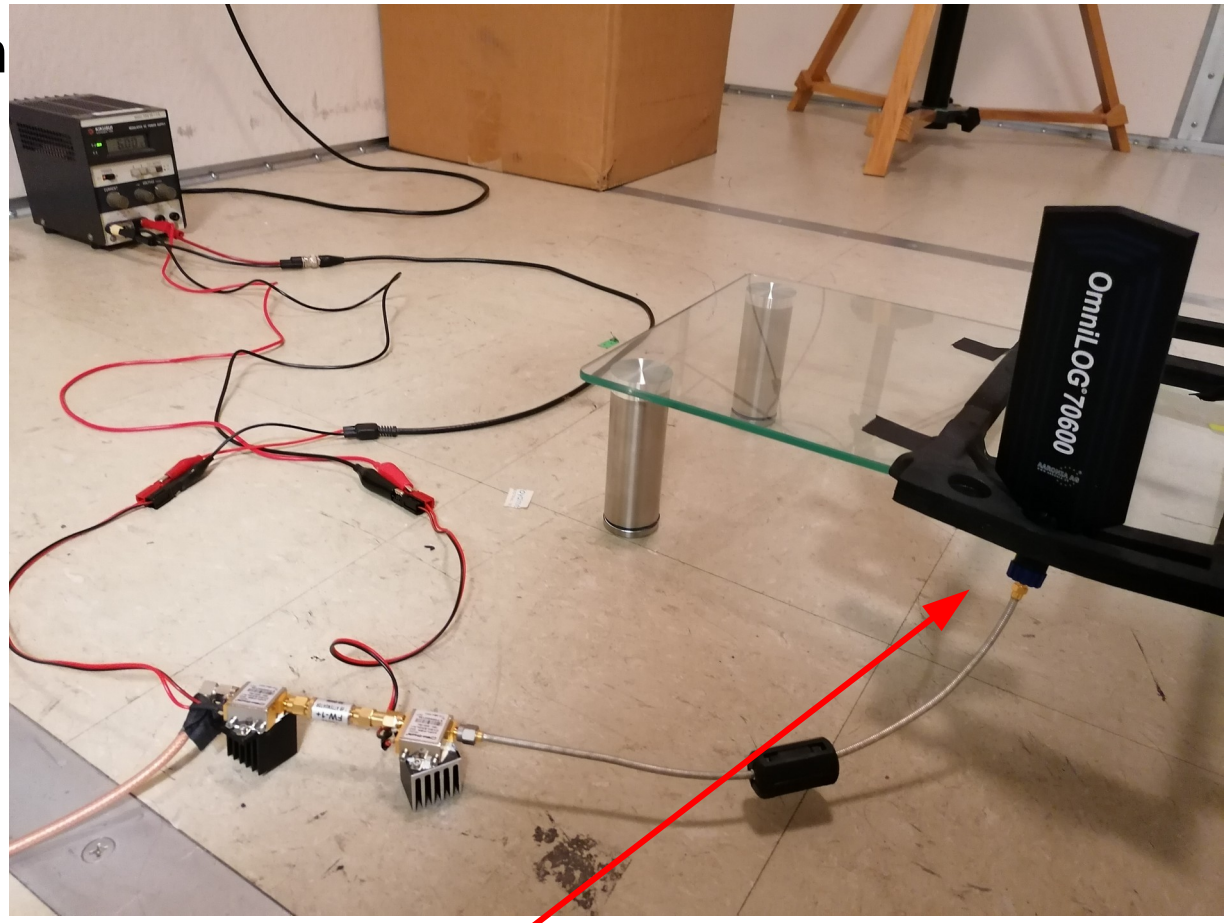
E.

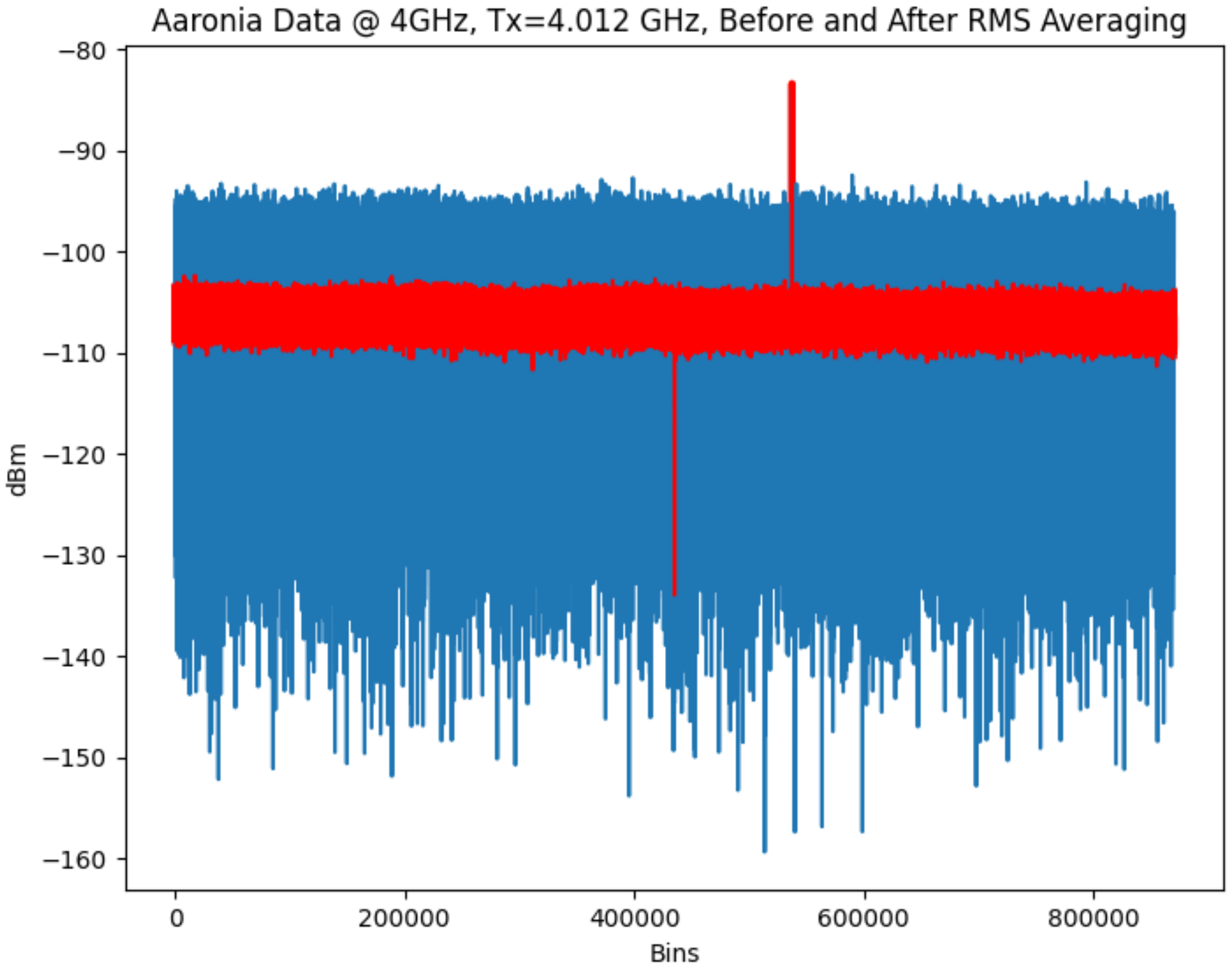
Tx: -105 dBm, Tx and Rx Aaronia antennas are identical, 60 dB Ext. amplifier+SA PreAmp.

Setup Inside the Shielded Room

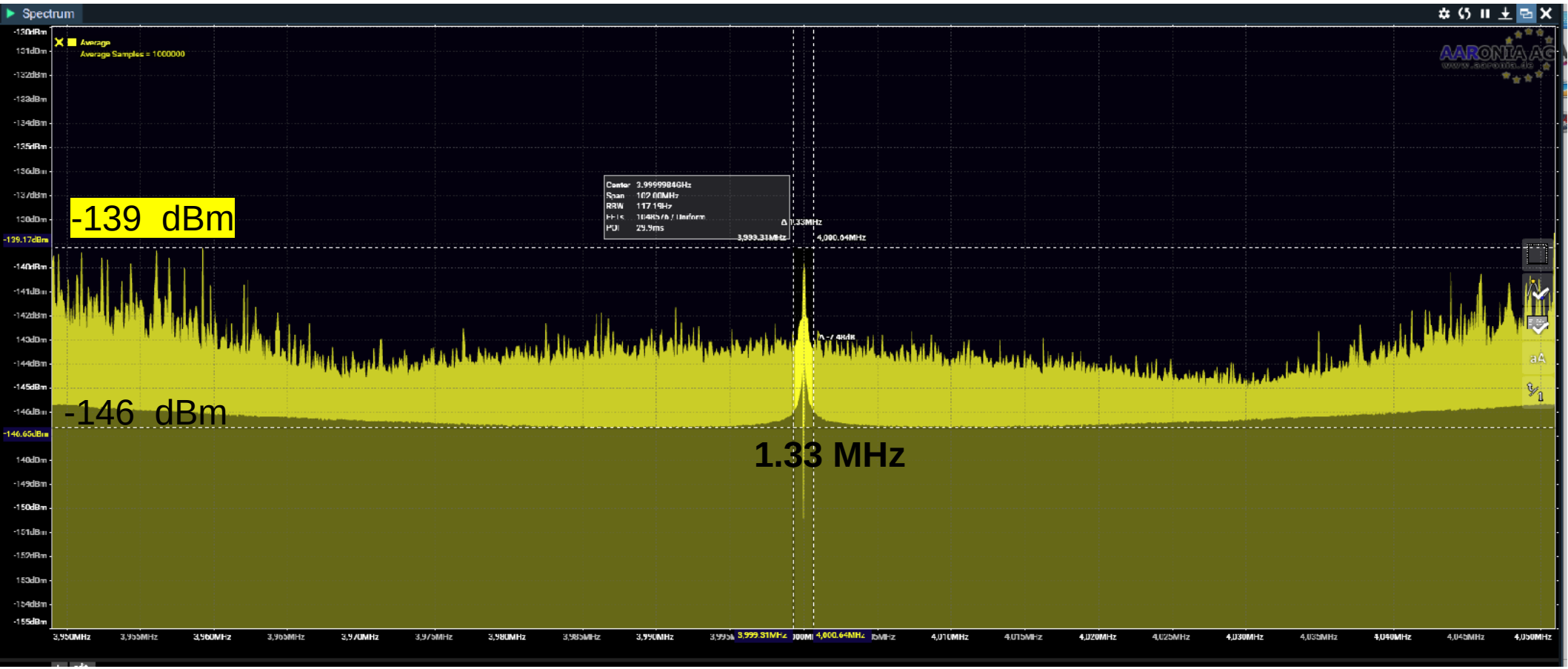







Aaronia Data @ 4GHz, Tx=4.012 GHz, Before and After RMS Averaging
−80
−90
−100
−110
−120
−130
−140
−150
−160
dBm
0
200000
400000
600000
800000
Bins

- Terminated Load, No Amplifier

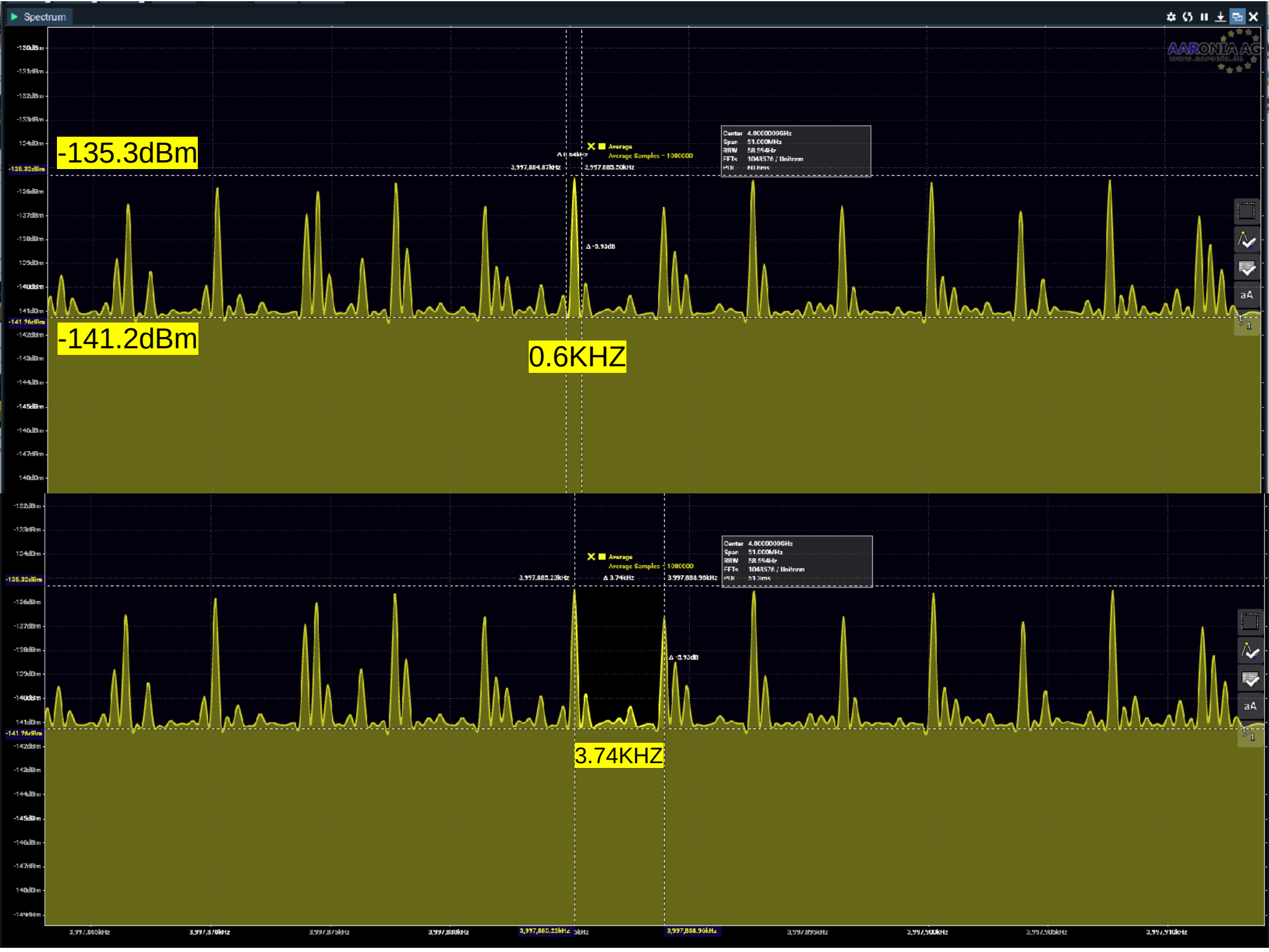


-139 dBm
-146 dBm

Spur at centre:

Fc@1.33 MHz BW

FFT 1M
Bin 870404
Span 102 MHz
RBW 117 Hz
Fc= 4 GHz


Spectrum
-135.3dBm
-141.2dBm
0.6KHZ
3.74KHZ