

Feature description

The TM7711 is a single-channel analog front end for low-frequency measurements on electronic scales. The original architecture developed as a data front end for the popular 24-bit lossless code performance is achieved with Σ - Δ conversion techniques. The incoming signal is sent to a gain programmable dedicated front end based on an analog modulator. The on-chip digital filter processes the output signal of the modulator. The architecture of the digital filter is programmable by the communication port command to adjust the cutoff point and output update rate of the filter. The TM7711 requires only a single 2.6~5.5V supply. The TM7711 is a fully differential analog input with a reference input.

The TM7711 is an ideal product for high-precision weigh scale systems with a special structure to ensure extremely low power consumption. And built-in power-down mode to reduce standby power consumption.

The chip also has the advantages of high integration, fast response, strong anti-interference performance and reliability of the whole system.

Features

- 1 pair of fully differential input channel ADC
- On-chip direct temperature measurement and digital output
- 24-bit no lost code
- On-chip low noise amplifier with gain of 128
- $\pm 0.001\%$ nonlinear
- Optional 10Hz and 40Hz output data rate
- Synchronously suppress power disturbances of 50Hz and 60Hz
- Built-in clock oscillator does not require any external devices
- Simple two-wire serial communication port
- Operating voltage range: 2.6 ~ 5.5V
- Operating temperature range: -40 ~ +85 °C
- Package: SOP8 /DIP8

typical application

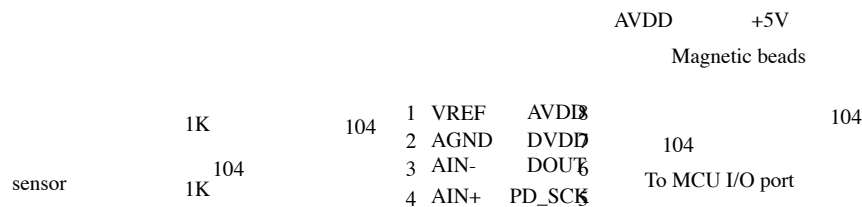


Figure 1 Typical application

DIP - 8 / SOP - 8
(TOPVIEW)

VREF 1	8	AVDD
AGND 2	7	DVDD
AIN- 3	6	DOUT
AIN+ 4	5	PD_SCK

Figure 2 pin information

Pin function

Table 1 pin description

Pin	name	Work can
1	VREF	Reference input voltage (1.8V~AVDD)
2	AGND	Ground input
3	AIN-	Differential analog input channel negative input
4	AIN+	Differential analog input channel positive input
5	PD_SCK	Power-down mode and serial clock input
6	DOUT	Serial data output
7	DVDD	Digital power input (2.6~5.5V)
8	AVDD	Analog power input (2.6~5.5V), AVDD voltage should not be higher than DVDD voltage

Absolute maximum rating range

Table 2 Absolute Maximum Ratings

	parameter		range	unit
VCC	voltage	AVDD, DVDD	-0.4~6.0	V
VIN	Input voltage range	VREF, AIN+, AIN-, PD_SCK	-0.4~VCC+0.4V	V
VOUT	Output voltage range	DOUT	-0.4~+6.0	V
Topr	range of working temperature		-40~+85	°C
Tstg	Storage temperature range		-55~+150	°C
ESD	Human body model (HBM)		4000	V
	Machine mode (MM)		300	V

Note: If the device is forced to work beyond the conditions listed in this table, it may cause permanent damage to the device. This table lists only the work stress limit does not mean that the device can work under the conditions listed in the table, or other bars that are beyond the scope of the work.

Under the pieces. Operating at absolute limits for extended periods of time may affect device life.

Recommended working conditions

(at -40 ° C ~ +85 ° C) unless otherwise stated

Table 3 Recommended working conditions

parameter	Test Conditions	TM7711			unit
		Minimum value	Typical value	Maximum	
DC parameter specification table:					
AVDD	Analog part supply voltage	2.6	5.0	5.5	V
DVDD	Digital part supply voltage	2.6	5.0	5.5	V
VIH	High level input voltage	0.7×DVDD		DVDD	V
VIL	Low level input voltage	GND		0.3×DVDD	V
TA	range of working temperature	-40		+85	°C
TJ	Working junction temperature range	-40		+125	°C

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Single channel 24-bit high precision ADC

TM7711

Serial communication

The serial communication line consists of pins PD_SCK and DOUT, which are used to output data and select the output data rate and input signal.

When the data output pin DOUT is high, it indicates that the A/D converter is not ready for output data. At this time, the serial port clock input.

The signal PD_SCK should be low. When DOUT goes from high to low, PD_SCK should input between 25 and 27 clocks.

Pulse (Figure 3). The rising edge of the first clock pulse will read the highest bit (MSB) of the output 24-bit data until the 24th time.

The clock pulse is completed and the 24-bit output data is output bit by bit from the highest bit to the lowest bit.

The output data rate and input signal of the secondary A/D conversion are shown in Table 4.

The number of input clock pulses of PD_SCK should not be less than 25 or more

27, otherwise it will cause serial communication error.

When the input signal or output data rate of the A/D converter changes, the A/D converter requires 4 data output cycles to stabilize.

DOUT does not go from high to low after 4 data output cycles, and outputs valid data.

Table 4 Input selection and output data rate selection

PD_SCK pulse number	Input selection	rate
25	Differential signal	10Hz

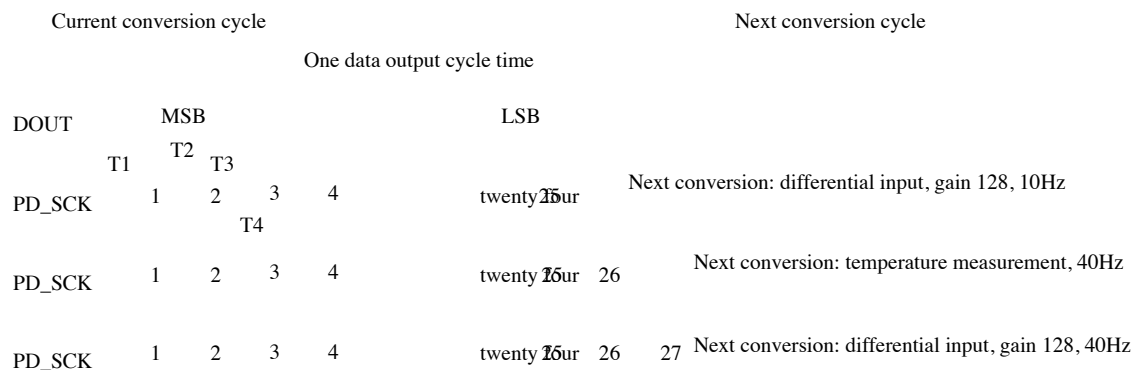


Figure 3 data output, input channel and gain selection timing diagram

Table 5 Description of timing communication parameters

parameter	description	Minimum value	unit
T1	DOUT falling edge to the rising edge of PD_SCK pulse	0.1	Ss
T2	PD_SCK pulse rising edge to DOUT data valid	0.1	Ss
T3	PD_SCK positive pulse level time	0.2	Ss
T4	PD_SCK negative pulse level time	0.2	Ss

*Note: The PD_SCK positive pulse level time cannot exceed the specified maximum value of 50μs, otherwise the read AD result data will be incorrect.

Output noise

Table 6 shows the noise-free bits of the TM7711 output. The data given is for both 5 volt bipolar input range for both AVDD and VREF. These data are typical and are generated with an analog differential input voltage of 0V.

Table 6 TM7711 Output Noise (5V Voltage)

Data update rate	Noise free
10Hz	17bits
40 Hz	16bits

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Analog input

(1) Channel analog input range:

The TM7711 includes one analog input pair, AIN+, AIN-. Input pair provides differential for processing single and bipolar input signals. Input channel. It should be noted that the bipolar input signal is referenced to the AIN-end.

The analog differential input voltage range is $\pm 0.5 \times (VREF/128)V$, and the absolute value of the analog input voltage is at AGND and AVDD-1.3V. between.

(2) Reference input:

VREF provides a reference input for the TM7711. The reference input range is 1.8V to AVDD.

System clock and AD data update rate

(1) System clock:

The TM7711's system clock is provided for the internal oscillator and is a high precision oscillator with ultra-low dependence on VDD and temperature.

(2) AD data update rate:

The TM7711 offers an optional 10 Hz and 40 Hz output data rate that can be easily selected via the communication port.

Output Data

The output data encoding of the TM7711 is in twos complement, ranging from 800000H (minimum) to 7FFFFFFH (maximum).

Temperature measurement

The digital temperature sensor inside the TM7711 chip can be used directly to read the temperature inside the chip, ie the system. Effective (stable) The number of digits is 15 digits. Typical temperature measurement accuracy is 20.4 readings per cycle (°C) (15 bits).

When using a digital temperature sensor, it should be noted that the temperature sensor inside the chip has a large difference in zero and gain between the chip. If used to measure absolute temperature, both zero and gain need to be corrected.

For example, the measured temperature is used to perform system temperature-related performance compensation, zero point and gain

Reset and power down mode

When the chip is powered up, the power-on automatic reset circuit in the chip will automatically reset the chip.

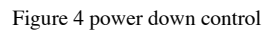
The pin PD_SCK input is used to control the power-down of the TM7711. When PD_SCK is low, the chip is in normal operation.

If PD_SCK goes from low to high and stays high for more than 60μs, the TM7711 enters power-down mode (see Figure 4). when

When PD_SCK returns to low level, the chip will re-enter normal operation. After the chip returns from the power-off state to the normal working state,

If you want to maintain the slew rate and input signal selection before power-off, the power-off cannot be in the current data conversion cycle where the numt

After the chip enters the normal working state from the reset or power-off state, the A/D converter requires 4 data output cycles to stabilize. DOUT will not go from high level to low level after 4 data output cycles, and output valid data.



The power consumption of the TM7711 in various states is shown in Table 7 below.

Operating voltage VDD	Chip status	Chip total current I _{vdd} (typical)
3V	normal work	1080μA
3V	Power down (standby) mode	0.5μA
5V	normal work	1200μA
5V	Power down (standby) mode	0.5μA

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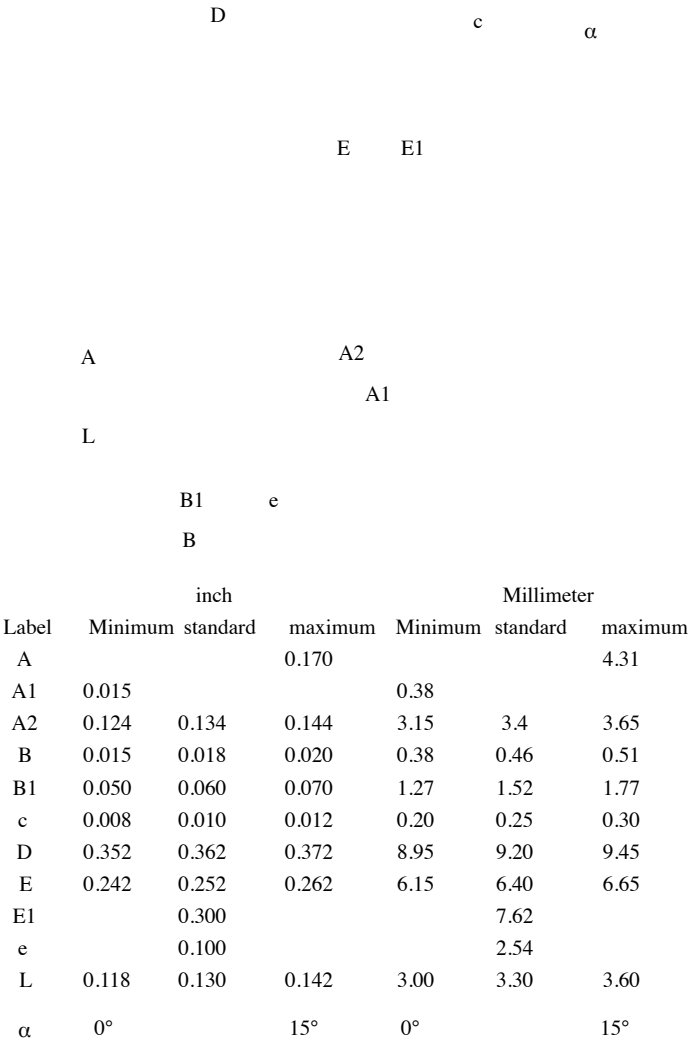
```
Delay_1us();
SET_SCK_H();
Delay_1us();
SET_SCK_L();
Delay_1us();
SET_SCK_H();
```

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```
Delay_1us();
SET_SCK_L();
Break;
Case CH2_TEMP:
SET_SCK_H();
Delay_1us();
SET_SCK_L();
Delay_1us();
SET_SCK_H();
Delay_1us();
SET_SCK_L();
Break;
Default:
Break;
}
Return(data_temp); //returns the data read from TM7711
}
```

Package schematic

DIP8:



SOP8:



c L

A
A1
e D b

Label	inch			Millimeter		
	Minimum	standard	maximum	Minimum	standard	maximum
A	0.051	0.059	0.067	1.30	1.50	1.70
A1	0.002	0.006	0.010	0.06	0.16	0.26
b	0.012	0.016	0.022	0.30	0.40	0.55
c	0.006	0.010	0.014	0.15	0.25	0.35
D	0.186	0.194	0.202	4.72	4.92	5.12
E	0.148	0.156	0.163	3.75	3.95	4.15
e		0.050			1.27	
H	0.224	0.236	0.248	5.70	6.00	6.30
L	0.018	0.026	0.033	0.45	0.65	0.85
α	0°		8°	0°		8°

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revise history

version	issue date	Introduction to revision
Ver1.0	2011-7-25	Original Issue
V1.1	2012-03-29	Revised release

