RGPVNOTES.IN

Program : **B.Tech**

Subject Name: **Basic Electrical & Electronics Engineering**

Subject Code: **BT-104**

Semester: **1st**

NUMBER SYSTEMS

***NUMBER SYSTEM* :-** A number system is a code having an assigned symbol for each distinct magnitude. The symbols are called "digits". The number of digits in a number system will determine the base of the system. In all number systems, the weight of a number depends on its relative position.

***BASE or RADIX* : -** The base or radix of a number system is the total number of different digits or basic symbols used in a number system. In the binary system we have 0 & 1 as digits , so the base or radix is 2. In the decimal system we have 10 digits ie. 0 through 9, so the base or radix is 10.

***BINARY SYSTEM* : -** This number system has a base or radix of 2. The symbols or digits used in this system are 0 & 1.

***OCTAL SYSTEM* : -** This number system has a base or radix of 8. The symbols or digits used in this system are 0 through7.(0, 1, 2, 3, 4, 5, 6, 7)

***DECIMAL SYSTEM* :-** This number system has a base or radix of 10. The symbols or digits used in this system are 0 through 9. (0, 1, 2, 3, 4, 5, 6, 7, 8, 9)

***HEXA DECIMAL SYSTEM* :-** This number system has a base or radix of 16. The symbols or digits used in this system are 0 through F. (0, 1, 2, 3, 4, 5, 6, 7, 8, 9, A, B, C, D, E, F)

CODE CONVERSIONS

(1) BINARY TO DECIMAL CONVERSION:-

(i) (101111 . 11010)$_2$ = (?)$_{10}$

Integeral part : $(101111)_2 = (1\times 2^5) + (0\times 2^4) + (1\times 2^3) + (1\times 2^2) + (1\times 2^1) + (1\times 2^0)$

$= 32 + 0 + 8 + 4 + 2 + 1$

$= 47$

ie. $(101111)_2 = (47)_{10}$

Fractional Part : $(0.11010)_2 = (1\times 1/2) + (1\times 1/4) + (0\times 1/8) + (1\times 1/16) + (0\times 1/32)$

$= 0.5 + 0.25 + 0 + 0.0625 + 0$

$= 0.8125$

ie. $(0.11010)_2 = (0.8125)_{10}$

Thus $(101111.11010)_2 = (47.8125)_{10}$

(ii) (111010 . 101101)$_2$ = (?)$_{10}$

Integeral part : $(111010)_2 = (1\times 2^5) + (1\times 2^4) + (1\times 2^3) + (0\times 2^2) + (1\times 2^1) + (0\times 2^0)$

$= 32 + 16 + 8 + 0 + 2 + 0$

$= 58$

ie. $(111010)_2 = (58)_{10}$

Fractional Part : $(0.101101)_2 = (1\times 1/2) + (0\times 1/4) + (1\times 1/8) + (1\times 1/16) + (0\times 1/32) + (0\times 1/64)$

$= 0.5 + 0 + 0.125 + 0.0625 + 0 + 0.015625$

$= 0.703125$

ie. $(0.101101)_2 = (0.703125)_{10}$

Thus $(111010.101101)_2 = (58.703125)_{10}$

(2) OCTAL TO DECIMAL CONVERSION:-

(i) $(457.245)_8 = (?)_{10}$

Integeral part :

$(457)_8 = (4\times 8^2) + (5\times 8^1) + (7\times 8^0)$

$= 256 + 40 + 7$

$= 303$

ie. $(457)_8 = (303)_{10}$

Fractional Part :

$(0.245)_8 = (2\times 1/8) + (4\times 1/64) + (5\times 1/512)$

$= 0.25 + 0.0625 + 0.0097656$

$= \mathbf{0.3222656}$

ie. $(0.245)_8 = (0.3222656)_{10}$

Thus $(457.245)_8 = (303.3222656)_{10}$

(ii) $(1427.3426)_8 = (?)_{10}$

Integeral part :

$(1427)_8 = (1\times 8^3) + (4\times 8^2) + (2\times 8^1) + (7\times 8^0)$

$= 512 + 256 + 16 + 7$

$= 791$

ie. $(1427)_8 = (791)_{10}$

Fractional Part :

$(0.3426)_8 = (3\times 1/8) + (4\times 1/64) + (2\times 1/512) + (6\times 1/4096)$

$= 0.375 + 0.0625 + 0.00391 + 0.001465$

$= (0.442875)_{10}$

ie. $(0.3426)_8 = (0.442875)_{10}$

Thus $(1427.3426)_8 = (791.442875)_{10}$

(3) HEXADECIMAL TO DECIMAL CONVERSION :-

(i) $(F9AC.5D8B)_{16} = (?)_{10}$

Integeral part :

$(F9AC)_{16} = (F\times 16^3) + (9\times 16^2) + (A\times 16^1) + (C\times 16^0)$

$= (15\times 16^3) + (9\times 16^2) + (10\times 16^1) + (12\times 16^0)$

$= 61440 + 2304 + 160 + 12$

$= 63916$

ie. $(F9AC)_{16} = (63916)_{10}$

Fractional Part :

$(0.5D8B)_{16} = (5\times 1/16) + (D\times 1/16^2) + (8\times 1/16^3) + (B\times 1/16^4)$

$= 0.3125 + 0.051 + 0.00195 + 0.000168$

$= \mathbf{(0.36562)_{10}}$

ie. $(0.5D8B)_{16} = (0.36562)_{10}$

Thus $(F9AC.5D8B)_{16} = (63916.36562)_{10}$

(ii) $(9EA6.2FA)_{16} = (?)_{10}$

Integeral part :

$(9EA6)_{16} = (9\times 16^3) + (E\times 16^2) + (A\times 16^1) + (6\times 16^0)$

$= (9\times 16^3) + (14\times 16^2) + (10\times 16^1) + (6\times 1)$

$= 36864 + 3584 + 160 + 6$

$= 40614$

ie. $(9EA6)_{16} = (40614)_{10}$

Fractional Part :

$(0.2FA)_{16} = (2\times 1/16) + (F\times 1/16^2) + (A\times 1/16^3)$

$= (2\times 1/16) + (15\times 1/256) + (10\times 1/4096)$

$= 0.125 + 0.0586 + 0.00244$

$= 0.18604$

ie. $(0.2FA)_{16} = (0.18604)_{10}$

Thus $(9EA6 . 2FA)_8 = (40614 . 18604)_{10}$

(1) DECIMAL TO BINARY CONVERSION :-

(i) $(47 . 8125)_{10} = (?)_2$

Integeral part :

2	47	1
2	23	1
2	11	1
2	5	1
2	2	0
	1	

ie. $(47)_{10} = (101111)_2$

Fractional Part :

$(0.8125 \times 2) = 1.625 \rightarrow 1$

$(0.625 \times 2) = 1.25 \rightarrow 1$

$(0.25 \times 2) = 0.5 \rightarrow 0$

$(0.5 \times 2) = 1.0 \rightarrow 1$

ie. $(0 . 8125)_{10} = (0.1101)_2$

Thus $(47 . 8125)_{10} = (101111 . 1101)_2$

(ii) $(58 . 703125)_{10} = (?)_2$

Integeral part :

2	58	0
2	29	1
2	14	0
2	7	1
2	3	1
	1	

ie. $(58)_{10} = (111010)_2$

Fractional Part :

$(0.703125 \times 2) = 1.40625 \rightarrow 1$

$(0.40625 \times 2) = 0.8125 \rightarrow 0$

$(0.8125 \times 2) = 1.625 \rightarrow 1$

$(0.625 \times 2) = 1.25 \rightarrow 1$

$(0.25 \times 2) = 0.5 \rightarrow 0$

$(0.5 \times 2) = 1.0 \rightarrow 1$

ie. $(0 . 703125)_{10} = (0 . 101101)_2$

Thus $(58 . 703125)_{10} = (111010 . 101101)_2$

(2) DECIMAL TO OCTAL CONVERSION :-

(i) $(303.3222656)_{10} = (?)_8$

Integeral part :

8	303	7
8	37	5
	4	

ie. $(303)_{10} = (457)_8$

Fractional Part :

$(0.3222656 \times 8) = 2.5781248 \rightarrow 2$
$(0.5781248 \times 8) = 4.6249984 \rightarrow 4$
$(0.6249984 \times 8) = 4.9999872 \rightarrow 4$
$(0.9999872 \times 8) = 7.9998976 \rightarrow 7$
$(0.9998976 \times 8) = 7.9991808 \rightarrow 7$
$(0.9991808 \times 8) = 7.9934464 \rightarrow 7$

ie. $(0.3222656)_{10} = (0.244777)_8$

Thus $(303.3222656)_{10} = (457.244777)_8$

(ii) $(791.442875)_{10} = (?)_8$

Integeral part :

8	791	7
8	98	2
8	12	4
	1	

ie. $(791)_{10} = (1427)_8$

Fractional Part :

$(0.442875 \times 8) = 3.543 \rightarrow 3$
$(0.543 \times 8) = 4.344 \rightarrow 4$
$(0.344 \times 8) = 2.752 \rightarrow 2$
$(0.752 \times 8) = 6.016 \rightarrow 6$
$(0.016 \times 8) = 0.128 \rightarrow 0$
$(0.128 \times 8) = 1.024 \rightarrow 1$

ie. $(0.442875)_{10} = (0.342601)_8$

Thus $(791.442875)_{10} = (1427.342601)_8$

(3) DECIMAL TO HEXADECIMAL CONVERSION :-

(i) $(63916.36562)_{10} = (?)_{16}$

Integeral part :

16	63916	12	→ C
16	3994	10	→ A
16	249	9	→ 9
	15		→ F

ie. $(63916)_{10} = (F9AC)_{16}$

Fractional Part :

(0.36562× 16) = 5.84992 → 5 → 5
(0.84992 × 16) = 13.59872 → 13 → D
(0.59872 × 16) = 9.57952 → 9 → 9
(0.57952 × 16) = 9.27232 → 9 → 9
(0.27232 × 16) = 4.35712 → 4 → 4

ie. **(0 . 36562)$_{10}$ = (0.5D994)$_{16}$**

Thus (63916 . 36562)$_{10}$ = (F9AC . 5D994)$_{16}$

(ii) (40614 . 18604)$_{10}$ = (?)$_{16}$

Integeral part :

16	40614	6	→ **6**
16	2538	10	→ **A**
16	158	14	→ **E**
	9		→ **9**

ie. **(40614)$_{10}$ = (9EA6)$_{16}$**

Fractional Part :

(0.18604 × 16) = 2.97664 → 2 → 2
(0.97664 × 16) = 15.62624 → 15 → F
(0.62624 × 16) = 10.01984 → 10 → A
(0.01984 × 16) = 0.31744 → 0 → 0
(0.31744 × 16) = 5.07904 → 5 → 5

ie. **(0 . 18604)$_{10}$ = (0 . 2FA05)$_{16}$**

Thus (40614 . 18604)$_{10}$ = (9EA6 . 2FA05)$_{16}$

(1) OCTAL TO BINARY CONVERSION :-

(i) (457 . 245)$_8$ = (?)$_2$

Integeral part :

(457)$_8$ = { 4 5 7 }
{ 100 101 111 }
= (100101111)$_2$

ie. (457)$_8$ = (100101111)$_2$

Fractional Part :

(0.245)$_8$ = { 2 4 5 }
{ 010 100 101 }
= (0. 010100101)$_2$

ie. (0.245)$_8$ = (0.010100101)$_2$

Thus (457 . 245)$_8$ = (100101111 . 010100101)$_2$

(ii) (1427. 3426)$_8$ = (?)$_2$

Integeral part :

(1427)$_8$ = { 1 4 2 7 }
{ 001 100 010 111 }
= (1100010111)$_2$

ie. **(1427)$_8$ = (1100010111)$_2$**

Fractional Part :

$(0.3426)_8 = \underbrace{3}_{011}\ \underbrace{4}_{100}\ \underbrace{2}_{010}\ \underbrace{6}_{110}$
$= (0.01110001011)_2$
ie. $(0.3426)_8 = (0.01110001011)_2$

Thus $(1427.3426)_8 = (1100010111.01110001011)_2$

(2) HEXADECIMAL TO BINARY CONVERSION :-

(i) $(F9AC.5D8B)_{16} = (?)_2$

Integeral part :

$(F9AC)_{16} = \underbrace{F}_{1111}\ \underbrace{9}_{1001}\ \underbrace{A}_{1010}\ \underbrace{C}_{1100} = (1111100110101100)_2$

ie. $(F9AC)_{16} = (1111100110101100)_2$

Fractional Part :

$(0.5D8B)_{16} = \underbrace{5}_{0101}\ \underbrace{D}_{1101}\ \underbrace{8}_{1000}\ \underbrace{B}_{1011} = (0.0101110110001011)_2$

Thus $(F9AC.5D8B)_{16} = (1111100110101100.0101110110001011)_2$

(ii) $(9EA6.2FA)_{16} = (?)_2$

Integeral part :

$(9EA6)_{16} = \underbrace{9}_{1001}\ \underbrace{E}_{1110}\ \underbrace{A}_{1010}\ \underbrace{6}_{0110} = (1001111010100110)_2$

ie. $(9EA6)_{16} = (1001111010100110)_2$

Fractional Part :

$(0.2FA)_{16} = \underbrace{2}_{0010}\ \underbrace{F}_{1111}\ \underbrace{A}_{1010} = (0.001011111010)_2$

Thus $(9EA6.2FA)_{16} = (1001111010100110.001011111010)_2$

(1) BINARY TO OCTAL CONVERSION :-

(i) $(100101111.010100101)_2 = (?)_8$

Integeral part :

$(100, 101, 111)_2 = \{\underbrace{100}_{4}\ \underbrace{101}_{5}\ \underbrace{111}_{7}\} = (457)_8$

ie. $(100101111)_2 = (457)_8$

Fractional Part :-

$(0.010, 100, 101)_2 = \{\underbrace{010}_{2}\ \underbrace{100}_{4}\ \underbrace{101}_{5}\} = (245)_8$

ie. $(100101111)_2 = (0.245)_8$

Thus $(100101111.010100101)_2 = (457.245)_8$

(ii) (1100010111 . 01110001011)$_2$ = (?)$_8$

Integeral part :

(1, 100, 010, 111)$_2$ = { 001 100 010 111 } = (1427)$_8$

1 4 2 7

ie. (1100010111)$_2$ = (1427)$_8$

Fractional Part :

(0. 011, 100, 010, 11)$_2$ = { 011 100 010 110 } = (0. 3426)$_8$

3 4 2 6

ie. (0.01110001011)$_2$ = (0.3426)$_8$

Thus = (1100010111 . 01110001011)$_2$ = (1427 . 3426)$_8$

(2) BINARY TO HEXADECIMAL CONVERSION :-

(i) (1001111010100110 . 001011111010)$_2$ = (?)$_{16}$

Integeral part :

(1001111010100110)$_2$ = { 1001, 1110, 1010, 0110 }

= (1001, 1110, 1010, 0110)$_2$

9 E A 6

ie. (1001111010100110)$_2$ = (9EA6)$_{16}$

Fractional Part :

(0. 001011111010)$_2$ = { 0010, 1111, 1010, }

2 F A

ie. (0. 001011111010)$_2$ = (0.2FA)$_{16}$

Thus (1001111010100110 . *001011111010*)$_2$ = (9EA6 . 2FA)$_{16}$

(ii) (1111100110101100 . 010111011000101100)$_2$ = (?)$_{16}$

Integeral part :

(1111100110101100)$_2$ = { 1111, 1001, 1010, 1100 }

= (1111, 1001, 1010, 1100)$_2$

F 9 A C

ie. (1111100110101100)$_2$ = (F9AC)$_{16}$

Fractional Part :

(0. 010111011000101100)$_2$ = { 0101, 1101, 1000, 1011, 0000 }

5 D 8 B 0

ie. (0. 010111011000101100)$_2$ = (0. 5D8B)$_{16}$

Thus (1111100110101100 . 0101110110001011)$_2$ = (F9AC . 5D8B)$_{16}$

(1) HEXADECIMAL TO OCTAL CONVERSION :-

(i) (F9AC . 5D8B)$_{16}$ = (?)$_8$

Integeral part :

(F9AC)$_{16}$ = F 9 A C
{ 1111 1001 1010 1100 } = (1111100110101100)$_2$

ie. (F9AC)$_{16}$ = (1, 111, 100, 110, 101, 100)$_2$
= (001, 111, 100, 110, 101, 100)$_2$ = 174654
1 7 4 6 5 4

ie. (F9AC)$_{16}$ = (174654)$_8$

Fractional Part :

(0 . 5D8B)$_{16}$ = 5 D 8 B
{ 0101 1101 1000 1011 } = (0 . 010, 111, 011, 000, 101, 100)$_2$
= (010, 111, 011, 000, 101, 100)$_2$
2 7 3 0 5 4
= (0 . 273054)$_8$

ie. (0.5D8B) = = (0 . 273054)$_8$

Thus (F9AC . 5D8B)$_{16}$ = (174654 . 273054)$_8$

(ii) (9EA6 . 2FA)$_{16}$ = (?)$_8$

Integeral part :

(9EA6)$_{16}$ = 9 E A 6
{ 1001 1110 1010 0110}

= (1001111010100110)$_2$

ie. (9EA6)$_{16}$ = (1, 001, 111, 010, 100, 110)$_2$
= (001, 001, 111, 010, 100, 110)$_2$
1 1 7 2 4 6
= (117246)$_8$

ie. (9EA6)$_{16}$ = (117246)$_8$

Fractional Part :

(0 . 2FA)$_{16}$ = 2 F A
{ 0010 1111 1010 }
= (0. 001011111010)$_2$

= (0 . 001, 011, 111, 010)$_2$
= (001, 011, 111, 010)$_2$
1 3 7 2
= (0 . 1372)$_8$

ie. (0 . 2FA)$_{16}$ = (0 . 1372)$_8$

Thus (9EA6 . 2FA)$_{16}$ = (117246 . 1372)$_8$

(2) OCTAL TO HEXADECIMAL CONVERSION :-

(i) $(174654.273054)_8 = (?)_{16}$

Integeral part :

$(174654)_8 = \underbrace{1}_{001}\ \underbrace{7}_{111}\ \underbrace{4}_{100}\ \underbrace{6}_{110}\ \underbrace{5}_{101}\ \underbrace{4}_{100}$

$= (\underbrace{0000}_{0},\ \underbrace{1111}_{F},\ \underbrace{1001}_{9},\ \underbrace{1010}_{A},\ \underbrace{1100}_{C})_2$

ie. $(174654)_8 = (F9AC)_{16}$

Fractional Part :

$(0.273054)_8 = \underbrace{2}_{010}\ \underbrace{7}_{111}\ \underbrace{3}_{011}\ \underbrace{0}_{000}\ \underbrace{5}_{101}\ \underbrace{4}_{100}$

$= (0.\underbrace{0101}_{5},\ \underbrace{1101}_{D},\ \underbrace{1000}_{8},\ \underbrace{1011}_{B},\ \underbrace{0000}_{0})$

ie. $(0.273054)_8 = (0.5D8B0)_{16}$

Thus $(174654.273054)_8 = (F9AC.5D8B)_{16}$

(ii) $(117246.1372)_8 = (?)_{16}$

Integeral part :

$(117246)_8 = \underbrace{1}_{001}\ \underbrace{1}_{001}\ \underbrace{7}_{111}\ \underbrace{2}_{010}\ \underbrace{4}_{100}\ \underbrace{6}_{110}$

$= (\underbrace{0000}_{0},\ \underbrace{1001}_{9},\ \underbrace{1110}_{E},\ \underbrace{1010}_{A},\ \underbrace{0110}_{6})_2$

ie $(117246)_8 = (09EA6)_{16}$

Fractional Part :

$(0.1372)_8 = \underbrace{1}_{001}\ \underbrace{3}_{011}\ \underbrace{7}_{111}\ \underbrace{2}_{010}$

$= (0.\underbrace{0010}_{2},\ \underbrace{1111}_{F},\ \underbrace{1010}_{A},)$

ie. $(0.1372)_8 = (0.2FA)_{16}$

Thus $(117246.1372)_8 = (9EA6.2FA)_{16}$

BINARY ARITHMETIC

(1) BINARY ADDITION :

(i) Add (111011.1101)$_2$ and (11111 .011)$_2$

		1	1	1	0	1	1	.	1	1	0	1	Augend
+		0	1	1	1	1	1	.	0	1	1	0	Addend
	1	**0**	**1**	**1**	**0**	**1**	**1**	**.**	**0**	**0**	**1**	**1**	**Sum**

(ii) Add (10110.1111)$_2$ and (1000111 .1101)$_2$

	0	0	1	0	1	1	0	.	1	1	1	1	Augend
+	1	0	0	0	1	1	1	.	1	1	0	1	Addend
	1	**0**	**1**	**1**	**1**	**1**	**0**	**.**	**1**	**1**	**0**	**0**	**Sum**

(2) BINARY SUBTRACTION :

(i) Subtract (11111.011)$_2$ from (111011 .1101)$_2$

	1	1	1	0	1	1	.	1	1	0	1	Minuend
−	0	1	1	1	1	1	.	0	1	1	0	Subtrahend
		1	**1**	**1**	**0**	**0**	**.**	**0**	**1**	**1**	**1**	**Difference**

(ii) Subtract (10110.1111)$_2$ from (1000111 . 1100)$_2$

	1	0	0	0	1	1	1	.	1	1	0	0	Minuend
−	0	0	1	0	1	1	0	.	1	1	1	1	Subtrahend
		1	**1**	**0**	**0**	**0**	**0**	**.**	**1**	**1**	**0**	**1**	**Difference**

(3) BINARY MULTIPLICATION :

(i) Multiply (1110.110)$_2$ and (1010 .010)$_2$

Multiplicand									Multiplier								
1	1	1	0	.	1	1	0	×	1	0	1	0	.	0	1	0	
										0	0	0	0	0	0	0	
									1	1	1	0	1	1	0		
								0	0	0	0	0	0	0			
							0	0	0	0	0	0	0				Partial products
						1	1	1	0	1	1	0					
					0	0	0	0	0	0	0						
				1	1	1	0	1	1	0							
			1	**0**	**0**	**1**	**0**	**1**	**1**	**1**	**.0**	**0**	**1**	**1**	**0**	**0**	**Final Product**

(ii) Multiply (1010.11)$_2$ and (111 .01)$_2$

Multiplicand								Multiplier						
1	0	1	0	.	1	1		1	1	1	.	0	1	
								1	0	1	0	1	1	
							0	0	0	0	0	0		
						1	0	1	0	1	1			Partial products
					1	0	1	0	1	1				
				1	0	1	0	1	1					
			1	**0**	**0**	**1**	**1**	**0**	**1**	**.1**	**1**	**1**	**1**	**Final Product**

(4) BINARY DIVISION:

(i) Divide (110001)$_2$ by (111)$_2$

Dividend

Divisor 111) 110001 (11 Quotient

111

01010

111

000111

111

000 000 Remainder

(ii) Divide (10100.110)$_2$ by (11.101)$_2$

***NOTE** : { 10100.110 □ 11.101 } is the same as {10100110 □ 11101 }, therefore we can divide the numbers as shown below :*

Dividend

Divisor 11101) 10100110 (101.1011 Quotient

11101

0110010

11101

000101010

11101

00000110100

11101

000000101110

11101

000000010001 Remainder

BINARY SUBTRACTION USING COMPLEMENTARY NUMBERS

(1) BINARY SUBTRACTION USING 1's COMPLEMENT :

1's COMPLEMENT : The 1's complement of any binary number is obtained by subtracting every binary digit from 1 , for example , the 1's complement of the number 11011 is obtained as follows :
(11111 – 11011) = 00100, therefore the 1's complement of $(11011)_2$ is $(00100)_2$.
The 1's complement is also obtained by complementing every digit of the given binary number, ie. The 1's complement of the number (11111)$_2$ is (00000)$_2$ & vice versa the 1's complement of (00000)$_2$ is (11111)$_2$
Negative numbers can be represented by 1's complement numbers, hence the process of subtraction in a processor can be carried out using an adder unit instead of a subtractor unit, as a result it minimizes the hardware in a computer.

(i) Subtract 25 from 45

45 ⟶ binary equivalent is : 101101 ⟶ write the positive number as it is
– 25 ⟶ binary equivalent is : 011001 ⟶ write the 1's complement of the negative number
20

ie. 45 ⟶ binary equivalent is :
– 25 ⟶ 1's complement is :
20

	1	0	1	1	0	1
+	1	0	0	1	1	0
1	0	1	0	0	1	1

since carry is generated, it has to be taken as end-around carry as shown below :

	1	0	1	1	0	1
+	1	0	0	1	1	0
1	0	1	0	0	1	1
						1
	0	1	0	1	0	0

end-around carry
= 20

(ii) Subtract 15 from 31

31 ⟶ binary equivalent is : 11111 ⟶ write the positive number as it is
– 15 ⟶ binary equivalent is : 01111 ⟶ write the 1's complement of the negative number
16

ie. 31 ⟶ binary equivalent is ⟶
– 15 ⟶ 1's complement is ⟶
16

	1	1	1	1	1	
+	1	0	0	0	0	
1	0	1	1	1	1	

since carry is generated, it has to be taken as end-around carry as shown below :

	1	1	1	1	1	
+	1	1	0	0	1	
1	0	1	1	1	1	
						1
	1	0	0	0	0	

end-around carry
= 16

(iii) Subtract 31 from 15

15 ⟶ binary equivalent is : 01111 ⟶ write the positive number as it is
– 31 ⟶ binary equivalent is : 11111 ⟶ write the 1's complement of the negative number
– 16

ie. 15 ⟶ binary equivalent is ⟶

	0	1	1	1	1
+	0	0	0	0	0
	0	1	1	1	1

since carry is not generated, complement the result & attach a negative sign as shown below

– 31 ⟶ 1's complement is ⟶

– 16

⟶ **= (□ 10000) = (□ 16)**

(iv) Subtract 45 from 25

25 ⟶ binary equivalent is : 011001 ⟶ write the positive number as it is
– 45 ⟶ binary equivalent is : 101101 ⟶ write the 1's complement of the negative number
– 20

ie. 25 ⟶ binary equivalent is ⟶

	0	1	1	0	0	1
+	0	1	0	0	1	0
	1	0	1	0	1	1

since carry is not generated, complement the result & attach a negative sign as shown

– 45 ⟶ 1's complement is ⟶

– 20

⟶ **= (□ 010100) = (□ 20)**

(1) BINARY SUBTRACTION USING 2's COMPLEMENT :

2's COMPLEMENT : The 2's complement of any binary number is obtained by adding 1 to the 1's complement , for example , the 2's complement of the number 11011 is obtained as follows :
The 1's complement of $(11011)_2$ is $(00100)_2$, the 2's complement is obtained by adding 1 to $(00100)_2$, ie.
$(00100 + 1)_2 = (00101)_2$
The 2's complement is also obtained by writing the LSB of the given binary number as it is and complementing the rest of the digits . For example the 2's complement of $(11011)_2$ is $(00101)_2$. If the LSB is not a 1 but a 0 then all these initial 0's are retained unchanged & then the first 1 that is encountered is kept unchanged & the rest of the bits are complemented. For example the 2's complement of $(1101100)_2$ is $(0010100)_2$
Subtraction can be carried out through addition by using 2's complement numbers, hence subtraction in a processor can be carried out using an adder unit instead of a subtractor unit, as a result it minimizes the hardware in a computer. However the advantage of using 2's complement is that during the process of subtraction whenever a carry is generated , it need not be used as end-around carry but has to be just neglected. This means that the subtraction process using complementary numbers becomes simple. When a carry is not generated the resultant umber will be a negative number.

(i) Subtract 25 from 45

45 ⟶ binary equivalent is : 101101 ⟶ write the positive number as it is
– 25 ⟶ binary equivalent is : 011001 ⟶ write the 2's complement of the negative number
20

ie. 45 ⟶ binary equivalent is :⟶

	1	0	1	1	0	1
+	1	0	0	1	1	1
1	0	1	0	1	0	0

since carry is generated, it has to be neglected & result is taken as shown below

– 25 ⟶ 2's complement is: ⟶

20

ie. $(010100)_2 = (20)_{10}$

(ii) Subtract 15 from 31

31 ⟶ binary equivalent is : 11111 ⟶ write the positive number as it is
– 15 ⟶ binary equivalent is : 01111 ⟶ write the 1's complement of the negative number
16

ie. 31 ⟶ binary equivalent is ⟶

	1	1	1	1	1
+	1	0	0	0	1
1	1	0	0	0	0

– 15 ⟶ 2's complement is ⟶
16

since carry is generated, it has to be neglected & result is taken as shown below

ie. (10000) $_2$ = (16)$_{10}$

(iii) Subtract 31 from 15

15 ⟶ binary equivalent is : 01111 ⟶ write the positive number as it is
– 31 ⟶ binary equivalent is : 11111 ⟶ write the 2's complement of the negative number
– 16

ie. 15 ⟶ binary equivalent is ⟶

	0	1	1	1	1
+	0	0	0	0	1
	1	**0**	**0**	**0**	**0**

– 31 ⟶ 2's complement is ⟶
– 16

since carry is not generated, complement the resultant number, add 1 to it & attach a negative sign as shown below

⟶ **Resultant number**

ie. Resultant number is(10000) & the answer will be complement of the resultant number plus 1 , with a negative sign,

ie. (□ 01111 □ 1)$_2$ = (□ 10000)$_2$ = (□ 20)$_{10}$

(iv) Subtract 45 from 25

25 ⟶ binary equivalent is : 011001 ⟶ write the positive number as it is
– 45 ⟶ binary equivalent is : 101101 ⟶ write the 1's complement of the negative number
– 20

ie. 25 ⟶ binary equivalent is ⟶

	0	1	1	0	0	1
+	0	1	0	0	1	1
	1	**0**	**1**	**1**	**0**	**0**

– 45 ⟶ 2's complement is ⟶
– 20

since carry is not generated, complement the resultant number, add 1 to it & attach a negative sign as shown below

⟶ **Resultant number**

ie. Resultant number is(101100) & the answer will be complement of the resultant number plus 1 , with a negative sign,

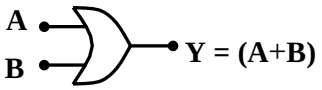
ie. (□ 010011 □ 1)$_2$ = (□ 010100)$_2$ = (□ 20)$_{10}$

LOGIC GATES

(1) **OR-GATE :-** Figure shows the logic circuit of a 2 input OR gate. The 2 inputs result in 4 input combinations of 0s & 1s. The operating conditions of the 4 combinations is summarized in the following truth table :-

A	B	Y = (A+B)
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**1**

Logic symbol for OR Gate



The OR operation is represented by the operator " + "

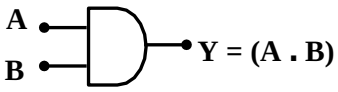
Input A = Logic 0 or 1
Input B = Logic 0 or 1

Logic – 0 = 0 Volt
Logic – 1 = 5 Volts

(2) **AND-GATE :-** Figure shows the logic circuit of a 2 input AND gate. The 2 inputs result in 4 input combinations of 0s & 1s. The operating conditions of the 4 combinations is summarized in the following truth table :-

A	B	Y = (A . B)
0	0	**0**
0	1	**0**
1	0	**0**
1	1	**1**

Logic symbol for AND Gate :



The AND operation is represented by the operator " . "

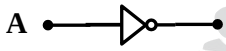
Input A = Logic 0 or 1
Input B = Logic 0 or 1

Logic – 0 = 0 Volt
Logic – 1 = 5 Volts

(3) **NOT-GATE :-** Figure shows the logic circuit of a NOT gate (Inverter). It is single input circuit in which the output is a complement of the input ie. if the input is logic-1 the output will be logic-0 & vice versa. As it has a single input, there are only two possible inputs 0 & 1.The NOT gate operation is explained for these two input combinations.

A	Y = (A)'
0	**1**
1	**0**

Logic symbol for NOT Gate :



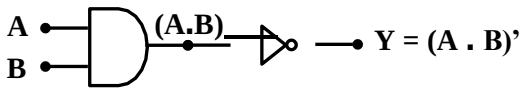
The NOT operation is represented by the operator " ' "

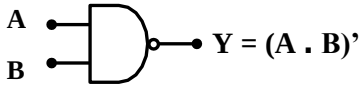
Input A = Logic 0 or 1

Logic – 0 = 0 Volt
Logic – 1 = 5 Volts

(4) **NAND-GATE :-** Figure shows the logic circuit of a 2 input NAND gate. A 2-input NAND gate is realised using an AND gate & a NOT gate. It is actually a combination of a two input AND Gate & a NOT Gate as shown in the logic circuit. It is also called a Negated AND gate (AND gate followed by a NOT gate). The logic symbol for a 2-input NAND gate is also shown along with the truth table .

A	B	Y = A . B	Y = (A . B)'
0	0	**0**	**1**
0	1	**0**	**1**
1	0	**0**	**1**
1	1	**1**	**0**



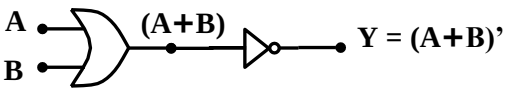


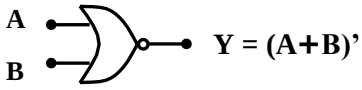
Input A = Logic 0 or 1
Input B = Logic 0 or 1

Logic – 0 = 0 Volt
Logic – 1 = 5 Volts

(5) **NOR-GATE :-** Figure shows the logic circuit of a 2 input NOR gate. A 2-input NOR gate is realised using an OR gate & a NOT gate. It is actually a combination of a two input OR Gate & a NOT Gate as shown in the logic circuit. It is also called a Negated OR gate (OR gate followed by a NOT gate). The logic symbol for a 2-input NOR gate is also shown along with the truth table .

A	B	Y = A+B	Y = (A+B)'
0	0	**0**	**1**
0	1	**1**	**0**
1	0	**1**	**0**
1	1	**1**	**0**



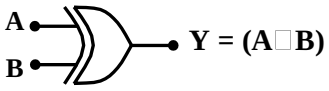


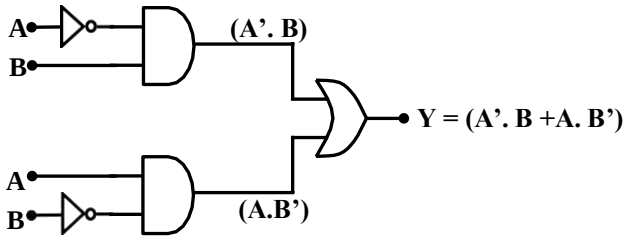
Input A = Logic 0 or 1
Input B = Logic 0 or 1

Logic – 0 = 0 Volt
Logic – 1 = 5 Volts

(6) **EXCLUSIVE-OR GATE[EX-OR GATE] :-** The Exclusive-OR gate can be derived using the basic gates ie. AND, NOT & OR gates, or the universal gates ie. NAND or NOR gates. The basic gate realisation for a 2-input EX-OR gate along with the logic symbol & truth table is as shown.

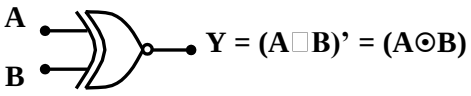
A	B	Y = (A⊕B)
0	0	**0**
0	1	**1**
1	0	**1**
1	1	**0**

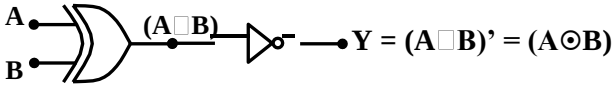




The EX-OR operation is represented by the operator "⊕" & output equation is given by : **Y = A⊕B = (A'.B+A.B')**

(7) EXCLUSIVE NOR – GATE [Ex – NOR GATE]:-





A	B	Y = (A⊕B)	Y = (A⊕B)' =(A⊙B)
0	0	**0**	**1**
0	1	**1**	**0**
1	0	**1**	**0**
1	1	**0**	**1**

Figure shows the logic symbol of a 2 input EX-NOR gate .It is a combination of a two input EX-OR Gate & a NOT-Gate. It is also called a Negated EX-OR gate (EX-OR gate followed by a NOT gate). The realization of a 2-input EX-NOR gate using an EX-OR gate & a NOT gate along with the truth table is also shown .

The EX-NOR operation is represented by the operator "⊙"

The output equation is given by : **Y = A⊙B = (A.B+A'.B')**

DE MORGAN'S THEOREM : Statement of De Morgan's Theorem :

I theorem : The complement of the sum is equal to the product of the complements.
ie. (A+B)' = (A' . B')

II theorem : The complement of the product is equal to the sum of the complements.
ie. (A.B)' = (A' + B')

Note : *Here the* ***sum*** *&* ***product*** *refer to the* ***Boolean sum & product*** *ie.* ***OR*** *&* ***AND*** *respectively*

Proof of De Morgan's I Theorem :

A	B	(A+B)	(A+B)'	A'	B'	(A' . B')
0	0	0	1	1	1	1
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	0

IDENTICAL

Since entries in the two columns shown are identical, the theorem is proved

Proof of De Morgan's II Theorem :

A	B	(A.B)	(A.B)'	A'	B'	(A'+ B')
0	0	0	1	1	1	1
0	1	0	1	1	0	1
1	0	0	1	0	1	1
1	1	1	0	0	0	0

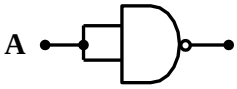
IDENTICAL

Since entries in the two columns shown are identical, the theorem is proved

UNIVERSAL LOGIC GATES :- A universal logic gate can be used to realize all the basic & derived gates (ie. OR, AND, NOT etc.) . Practically it is observed that NAND & NOR gates function as universal gates ie. it is possible to realize all basic & derived gates using NAND & NOR gates.

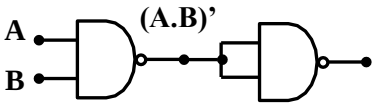
(1) NAND – GATE AS UNIVERSAL GATE :-

(i) Realisation of NOT gate :-



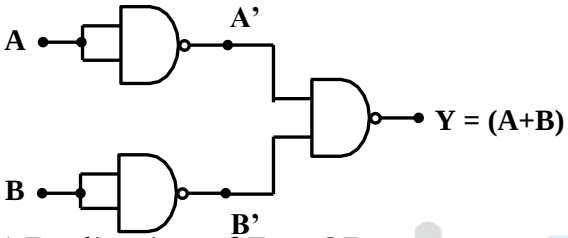
Y = (A . A)' =(A)'

(ii) Realisation of AND gate :-



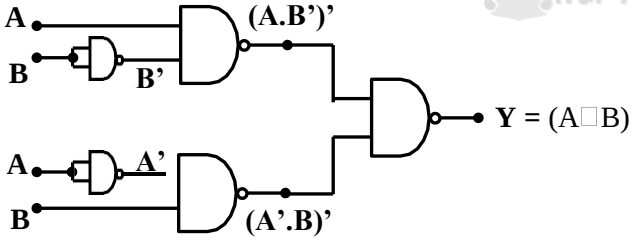
Y = [(A . B)']' = (A . B)

(iii) Realisation of OR gate :-

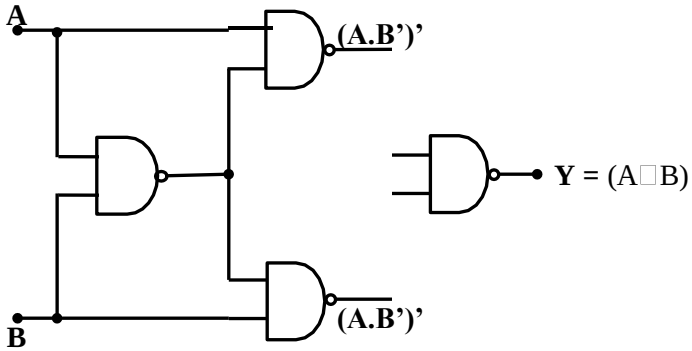


Y = (A'. B')' = (A +B)

(iv) Realisation of Ex – OR gate :-



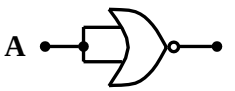
Y = (A. B')+(A'.B)



Y = (A. B')+(A'.B)

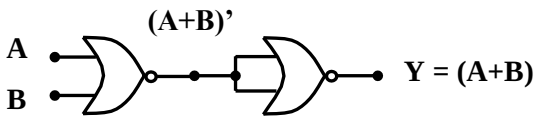
(2) NOR – GATE AS UNIVERSAL GATE :-

(i) Realisation of NOT gate :-



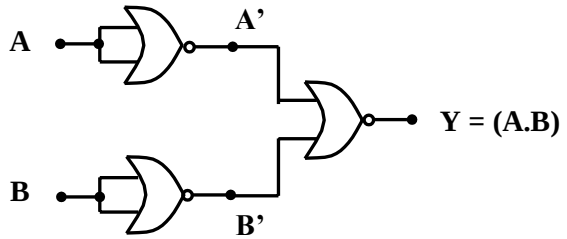
Y = (A +A)' =(A)'

(ii) Realisation of OR gate :-



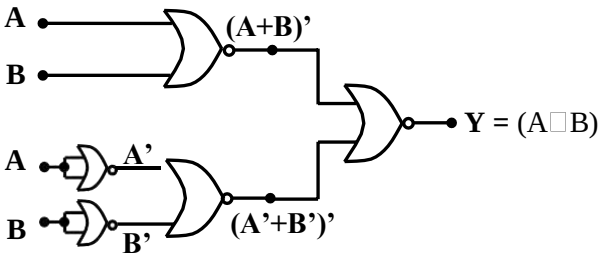
$Y = [(A + B)']' = (A + B)$

(iii) Realisation of AND gate :-



$Y = (A' + B')' = (A \cdot B)$

(iv) Realisation of Ex – OR gate :-



$Y = (A \cdot B') + (A' \cdot B)$

(1) **HALF ADDER :-** It is a logic circuit used to add 2 one bit binary numbers. A half adder circuit has two inputs & two outputs (sum & carry) . The addition of 2 bits can be shown using the following truth table:

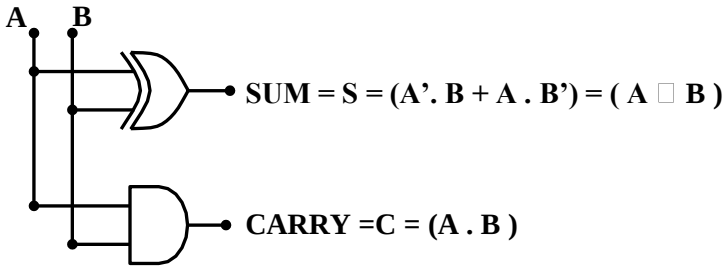
A	B	SUM(S)	CARRY(C)
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

The logic circuit for a half adder is realized using the Boolean expression obtained from the truth table :-

(i) Sum = S = (A'. B + A . B') = (A ⊕ B)

(ii) Carry = C = (A . B)

The Half Adder circuit is therefore realized as shown below :

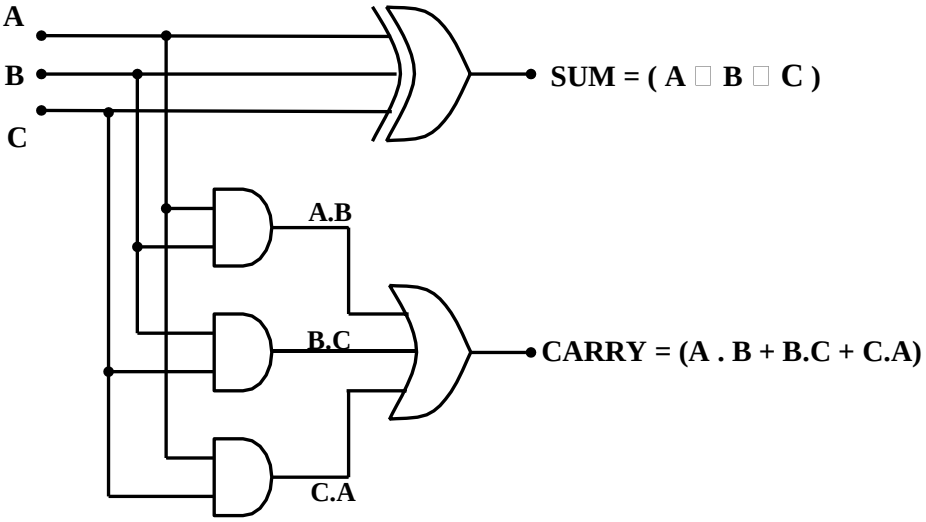


(2) **FULL ADDER :-** The Half adder circuit can be used to add 2 one bit binary numbers effectively, but when multi bit numbers are to be added then the carry bit that is generated should also be taken care of. This carry bit has to be added to the existing two input bits, which means this circuit would require 3 inputs, ie. two input terminals to add the actual input bits & an additional input terminal to handle the carry bit generated from the previous addition. This is done using a Full adder circuit which is realized using 2 Half adders & a single OR – Gate as shown . The logic circuit for a Full adder is realized using the Boolean expression obtained from the truth table which is shown:-

A	B	C	SUM(S)	CARRY(C)
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

(i) SUM = (A'.B'.C + A'. B.C'+A.B'.C'+A.B.C)
= (A.B'.C'+ A'. B.C'+A'.B'.C +A.B.C)
SUM= (A ⊕ B ⊕ C)
(ii) CARRY = (A'.B.C + A . B'.C+A.B.C'+A.B.C)
= BC(A'+A) + A .B'.C+A.B.C'
= B.C + A.B'.C+A.B.C' = B(C+C'.A)+A.B'.C
= B(C+A)+A.B'.C = B.C + B.A + A .B'.C
= C(B+B'.A) + B . A = C.(B+A)+B.A
CARRY = A .B + B.C + C. A

The Full adder circuit is therefore realized as shown :



A Full adder can also be realized using two half adders & a single 2 – input OR – gate as shown :

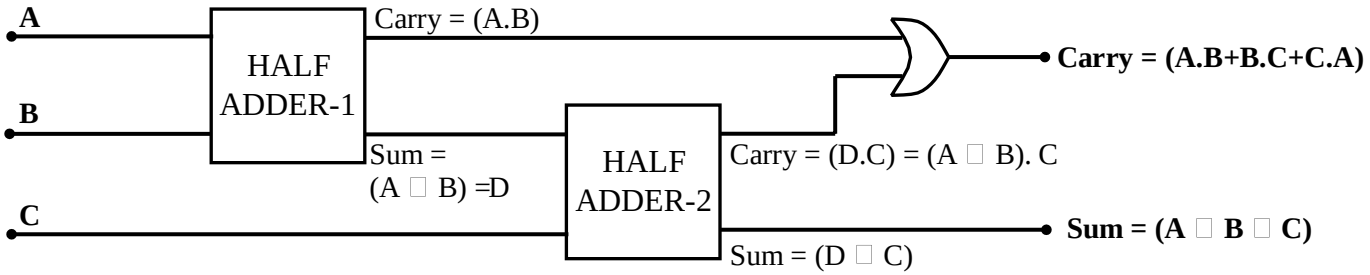
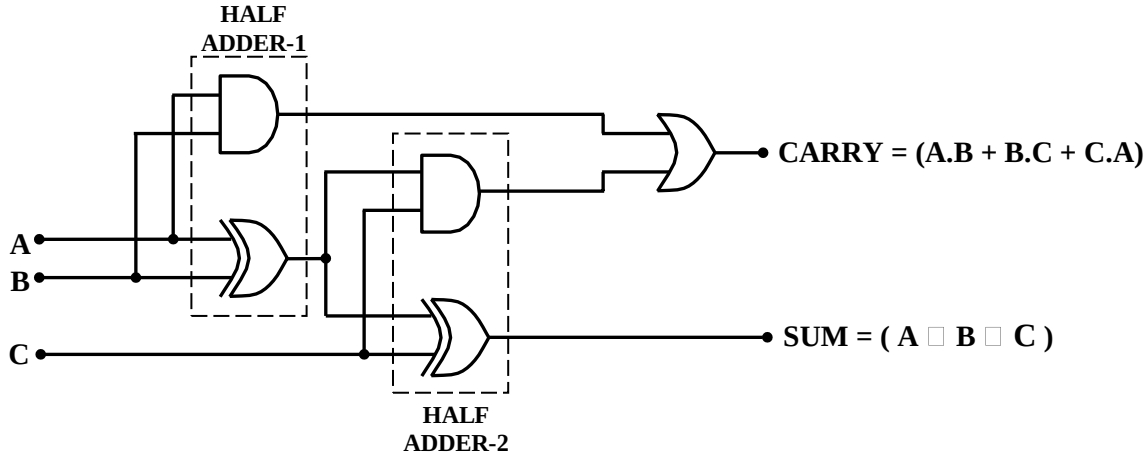
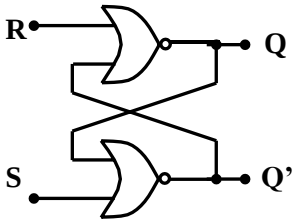


Figure below shows a Full adder realized using two half adders consisting of 2 input Ex-OR gates, 2-input AND gates & a 2-input OR – gate :



R-S FLIP FLOP : A flip flop is a basic memory element (data storage element). A flip flop is realised using a group of logic gates. A NAND gate or a NOR gate individually cannot act as a storage element but when two gates are cross coupled with feed back then they can work as storage or memory elements. Such cross coupled NAND gates or NOR gates with feedback are known as flip flops. A flip flop is a bistable electronic circuit that has two stable states , which means the flip flop output will permanently remain either 0 (low) or 1(high) until it is forced to change its state by an external trigger. A flip flop circuit will have two outputs, one is the Q output & the other is the Q' output which will always be the complement of the Q output , ie Q & Q' are always complementary to each other. Flip flops can be realised using two cross coupled inverters, hence we can use a NOR gate inverter or a NAND gate inverter as shown.

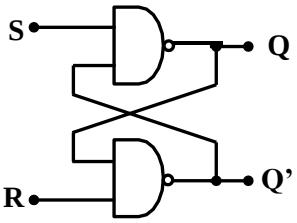


S	R	Q (Output)
0	0	**No Change**
0	1	**0 (Reset)**
1	0	**1 (Set)**
1	1	**Race**

 # No Change or Last State or Memory State

 # Race or Invalid or Not Allowed or ? State

The truth table shown for a NOR gate inverter flip flop is similar to that of a transistor flip flop .

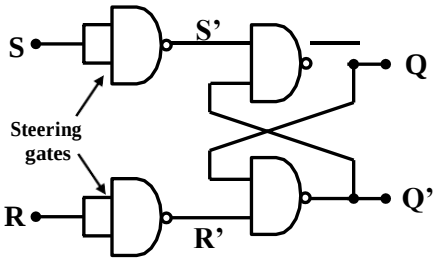


S	R	Q (Output)
0	0	**Race**
0	1	**1 (Set)**
1	0	**0 (Reset)**
1	1	**No Change**

 # Race or Invalid or Not Allowed or ? State

 # No Change or Last State or Memory State

The truth table shown for a NAND gate inverter flip flop is the inverted form of that shown for a NOR gate flip flop, hence inverters or steering gates are used to drive the inputs to the gates as shown :



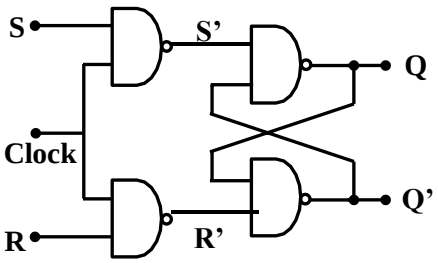
S	R	Q (Output)
0	0	**No Change**
0	1	**0 (Reset)**
1	0	**1 (Set)**
1	1	**Race**

 # No Change or Last State or Memory State

 # Race or Invalid or Not Allowed or ? State

The truth table shown for a NAND gate inverter flip flop with steering gates is similar to that shown for a transistor flip flop, hence inverters or driving gates are used to realize the desired practical R-S flip flop.
In order to overcome the RACE problem in R-S flip flops the J-K flip flop is used.

CLOCKED R-S FLIP FLOP :



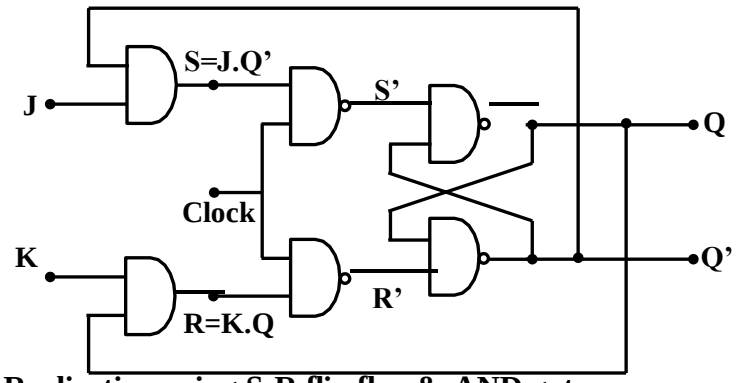
Clock	S	R	Q (Output)
X (0 or 1)	0	0	**No Change**
1	0	1	**0 (Reset)**
1	1	0	**1 (Set)**
1	1	1	**Race**

X – Don't Care Condition, ie. Clock is either 0 or 1

The clock signal is also known as the enabling signal which makes the logic circuit perform the required operation.If clock = 0 then the logic circuit will not respond to the input signals ie. the circuit output will remain unaltered. Only when the clock = 1(rising or falling edge) the logic circuit is enabled & will respond to the applied input signals.

J-K FLIP FLOP : A J-K flip flop is realized using a clocked S-R flip flop and two AND gates with appropriate feed back as shown in figure. The problem with the R-S flip flop is that it exhibits the RACE condition when both S & R are high ie when both are logic-1. This condition is a logically unpredictable state. The J-K flip flop eliminates the unpredictable condition that occurs in the S-R flip flop and hence can be practically used in logic circuits. The J input is analogous to the S input & the K input is analogous to the R input. This means that when J=1 & K=0 , the J-K flip

will Set , ie. Q=1, and when J=0 & K=1, the J-K flip flop will Reset, ie. Q=0. As usual there will be no change in the output condition when J=K =0. However the most important change when compared to the S-R flip flop is that the J-K flip flop will complement its output condition when J=K =1 with the clock high. The operation of a J-K flip can be clearly understood from the truth table given below.

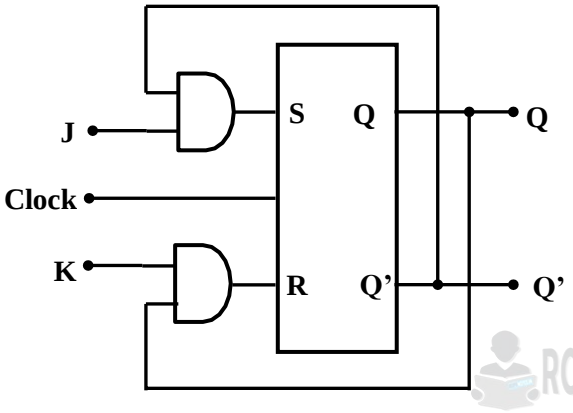


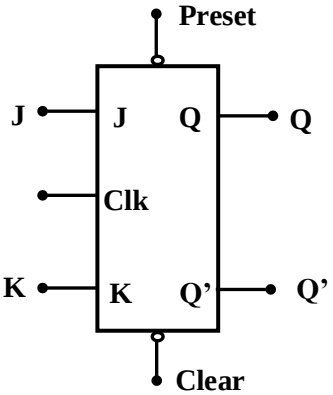
Realisation using S-R flip flop & AND gates

Input S = J . Q'

Input R = K . Q

Logic Symbol of J-K flip flop





Clk	J	K	Q_n	Q_n'	S = $J.Q_n$'	R= $K.Q_n$	Output (Q_{n+1})	Remarks
1	0	0	0	1	0	0	0	= Q_n ie. **No Change or Last State or Memory**
1	0	0	1	0	0	0	1	
1	0	1	0	1	0	0	0	= **0** , ie. **Reset** (Make Q = 0)
1	0	1	1	0	0	1	0	
1	1	0	0	1	1	0	1	= **1** , ie. **Set** (Make Q = 1)
1	1	0	1	0	0	0	1	
1	1	1	0	1	1	0	1	= Q_n' ie. **Toggle or Complement or Switch to opposite state**
1	1	1	1	0	0	1	0	

Q_n represents the Present State ; Q_{n+1} represents the Next State ie. the state of the output after the clock pulse is applied.

Race Around Condition in J-K Flip Flop : By using two AND gates & appropriate feed back the RACE problem that existed in the S-R flip flop could be eliminated in a J-K flip flop. However there is a problem of an unpredictable state occurring in the J-K flip flop also . Due to this problem the Q output will start oscillating between the 0 (low) & 1 (high) states .The output condition therefore could be either 0 or 1. This problem is known as the Race around Condition. The race around condition in a J-K flip flop occurs when J=1, K=1 and the clock is also =1, with the clock pulse width "t_p" greater than the propagation delay "Δt" of the gates. We assume that the inputs of the J-K flip flop do not change during a clock pulse , but due to the feed back they change when the clock remains high (1), hence the output condition starts oscillating between the low & high states. This problem can be avoided by making the clock pulse width less than the propagation delay of the gates, but practically this is difficult because the propagation delay is very small, hence the problem of Race Around Condition is overcome using a Master-Slave J-K flip flop. In this flip flop the input conditions do not change when the clock remains high, hence the output does not oscillate.

PROPERTIES OF SEMICONDUCTOR MATERIAL :- A semiconductor is a material which exhibits the following properties :-

1) It has a resistivity lying between that of a conductor and an insulator.
2) It is tetravalent.
3) It exhibits negative temperature co-efficient of resistance .
4) It exhibits crystalline structure.
5) Its conductivity increases when doped with trivalent or penta valent atoms.

Silicon (atomic no. **14**) and Germanium (atomic no. **32**) are the two most important semiconductor materials.

INTRINSIC SEMICONDUCTOR :- A semiconductor material in its purest form is known as an intrinsic semiconductor. An intrinsic semiconductor behaves as an insulator at 0 K but acts as a conductor at 300 K (room temperature). At room temperatures due to the thermal generation of electron-hole pairs , free electrons & holes are generated in equal numbers , these mobile charges help in the conduction of current in an intrinsic semiconductor. Since electron-hole pairs that are responsible for conduction of current in an intrinsic semiconductor are internal to the semiconductor crystal , the material is known as an intrinsic semiconductor .

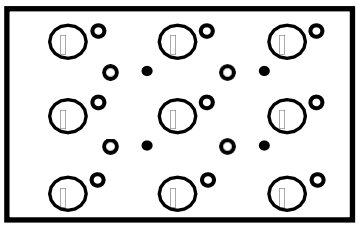
FREE ELECTRONS OR **CONDUCTION ELECTRONS :-** When external energy is supplied to a semiconductor crystal in the form of light or heat (increase in temperature), some covalent bonds break and produce free electrons. Every free electron has an associated vacant site (hole) in the covalent bond .These free electrons are not under the control of any of the nuclei within the crystal.. Since free electrons take part in the conduction of current , they are also known as conduction electrons. Conduction electrons or free electrons have energy levels much higher than valence electrons and take part in the conduction of current in a semiconductor.

VALENCE ELECTRONS OR **BOUND ELECTRONS :-** The outer most orbit electrons or valence electrons are shared by the neighboring semiconductor atoms to form covalent bonds in a crystal. A valence electron is always associated with a particular nuclei and is under it's control, hence a valence electron is also known as a bound electron. A valence electron by itself cannot take part in the conduction of current. A valence electron will take part in the conduction of current only when there is hole movement, in other words hole movement is actually the movement of valence electrons in the valence band. At 0 K all the electrons in a Silicon crystal exist as valence electrons (ie. there are no free electrons or holes) hence there is no current conduction & Silicon behaves as an insulator.

DOPING :- The process of adding a calculated quantity ($1:10^8$) of trivalent or pentavalent atoms to an intrinsic semiconductor is known as doping. Doping helps in generating a single type of charge carrier (either free electrons or holes). Doping thus increases the conductivity of a semiconductor at room temperatures.

EXTRINSIC SEMICONDUCTOR :- An extrinsic semiconductor is obtained by doping an intrinsic semiconductor with trivalent or pentavalent impurity atoms . Depending upon the valency of the impurity atoms added we obtain either p-type or n-type extrinsic semiconductor.

P-TYPE EXTRINSIC SEMICONDUCTOR :-

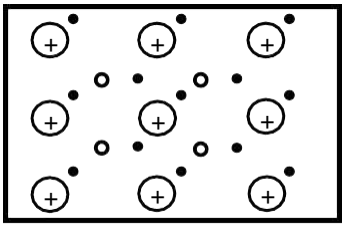


Hole (Majority Carrier)
Free electron (Minority Carrier)
Negative Immobile ion

A p-type extrinsic semiconductor is obtained by adding trivalent impurity atoms (Boron, Aluminum, Gallium or Indium) to an intrinsic semiconductor in the ratio of $1: 10^8$.

The three valence electrons of aluminum atom form three co-valent bonds with the three neighboring semiconductor atoms . The absence of a fourth valence electron creates a vacant site (hole) in one of the covalent bonds . The hole has a positive charge & is capable of accepting an electron from the semiconductor crystal to become a negative immobile ion. Thus a trivalent impurity atom is known as an acceptor impurity . Every trivalent atom added to a semiconductor crystal gives rise to a hole and a negative immobile ion. The conductivity of a p-type semiconductor is directly proportional to the doping density. In a p-type semiconductor, holes are in excess when compared to conduction electrons , hence holes are known as majority carriers and conduction or free electrons are known as minority carriers . The total current flowing through a p-type semiconductor is the sum of free electron and hole currents. Since majority of this current is due to holes (positive charges) the material is known as a p-type extrinsic semiconductor . A p-type semiconductor is electrically neutral because total number of negative charges is exactly equal to the total number of positive charges.

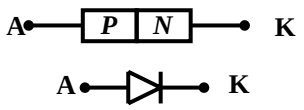
N –TYPE EXTRINSIC SEMICONDUCTOR :- A n-type semiconductor is obtained by adding pentavalent impurity atoms (phosphorus , arsenic or antimony) to an intrinsic semiconductor in the ratio of $1:10^8$ .The four valence electrons of phosphorus form four co-valent bonds with the four neighboring semiconductor atoms. The fifth valence electron cannot form a co-valent bond hence remains free. This free electron helps in the conduction of current. The pentavalent impurity atom loses one electron and becomes a positive immobile ion . When a pentavalent atom is added to an intrinsic semiconductor one electron is donated into the crystal, hence a pentavalent



- **Free electron (Majority Carrier)**
- **Hole (Minority Carrier)**
- **Positive Immobile ion**

impurity atom is also known as a donor impurity. Every pentavalent impurity atom added gives rise to a free electron and a positive immobile ion . The conductivity of a n-type semiconductor is directly proportional to the doping density. In a n-type semiconductor, electrons are in excess when compared to holes, hence electrons are majority carriers and holes are minority carriers. Since majority of the current is carried by negative charges (electrons), the material is known as n-type semiconductor. A n-type semiconductor is electrically neutral because the total number of positive charges is exactly equal to the total number of negative charges in the crystal

P-N JUNCTION DIODE :- Figure shows the construction and circuit symbol of a p-n junction diode. The arrow mark in the diode symbol indicates the direction of flow of conventional current. A p-n junction diode is fabricated using a single semiconductor crystal, in which one half is doped with p-type impurity, while the other half is doped with n-type impurity. A p-n junction diode is basically a unidirectional device (ie. it allows current to flow in one direction & blocks it in the other direction). A p-n junction diode is a high speed electronic switch & is widely used in rectifier circuits.



The operation of a semiconductor diode is studied under the following three conditions :-

(1) Unbiased condition :-

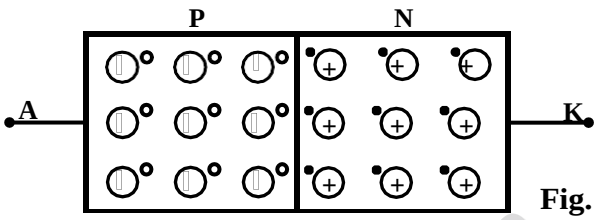


Fig. 1

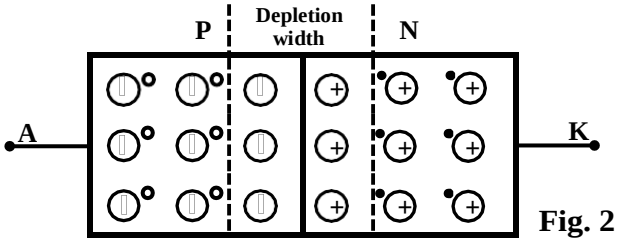


Fig. 2

Fig.2 shows a p-n junction diode under unbiased condition, ie. both the anode & cathode are at the same potential or both are at zero potential. For simplicity only impurity atoms are shown (semiconductor atoms are not shown) because for every impurity atom, there will be 10^8 semiconductor atoms (because doping density is $1:10^8$).

The p-region has negative immobile ions and their corresponding holes as the majority carriers , while the n-region has positive immobile ions and their corresponding free electrons as the majority carriers. Thermally generated electron-hole pairs are also not shown for simplicity. At the instant of junction formation, the p-material has excess holes and the n- material has excess electrons as shown in Fig.1. and the depletion region does not exist. As soon as the p & n regions are formed, electrons on the n-side recombine with holes by crossing onto the p-side of the junction due to diffusion. Soon after recombination both the electrons & the holes disappear and leave behind immobile positive ions on the n-side and immobile negative ions on p-side of the junction as shown in Fig.2. This electric field created by the immobile positive & negative ions on either side of the junction prevents further diffusion of charges. Thus a depletion region (width ≈ 50 μm) is formed at the junction even under unbiased conditions as shown in Fig.2.

(2) Forward biased condition :-

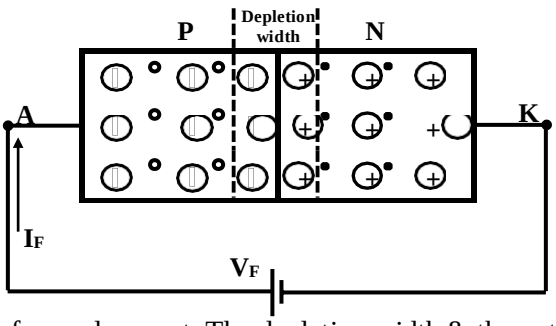
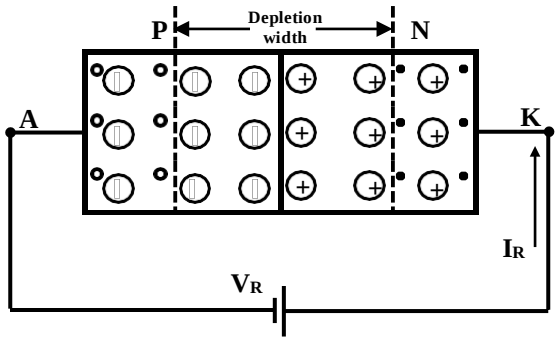


Figure shows a p-n junction diode under forward biased condition (ie. anode is at a higher potential than the cathode). The battery polarity is such that majority carriers in both p & n regions are pushed towards the junction. Since electrons & holes enter the depletion region, it causes a reduction in the depletion width & hence height of the potential barrier. The reduced potential barrier allows a few high- energy electrons on the n-side to cross the junction on to the p-side and constitute a small forward current. As the magnitude of forward bias voltage is increased the depletion width further reduces & thereby further increases the forward current. The depletion width & the potential barrier reduce to almost zero when the p-n junction is forward biased by a voltage greater than the cut-in voltage V_γ (0.7 V for Silicon diode & 0.3 V for Germanium diode).

At voltages greater than V_γ a p-n junction diode acts like a closed switch (offers zero resistance) and a heavy current starts flowing. Practically a very small value resistance is offered due to the existence of the bulk resistance of the semiconductor crystal.

The thermally generated electron-hole pairs present in both p and n regions & the minority carriers also move in the same direction as majority carriers , ie. they also add to the forward current.

(3) Reverse biased condition :-



When a p-n junction diode is reverse biased (ie. anode is at a lower potential than the cathode) a very small reverse current flows through the junction due to a small number of temperature dependent minority charge carriers (electrons in p-region & holes in n-region). This minority current or leakage current is also known as the reverse saturation current & is temperature dependent. The leakage current which has a very small value(1 or 2 μA) doubles itself for every 10° C rise in temperature . The diode therefore offers very high resistance (1 to 2 MΩ). This means that the diode acts as an open switch under reverse biased conditions. The battery connection is such that majority carriers in both p and n regions are pulled away from the junction. Thus both the depletion width and the potential barrier increase under reverse bias conditions. This reverse current flows until the reverse voltage is equal to the junction breakdown voltage. Beyond breakdown voltage, there is a drastic increase in the reverse current which is explained using the avalanche breakdown phenomenon. At voltages beyond V_{BD}, minority carriers (electrons) on the p-side gain sufficiently high velocities to knock out valence electrons from the semiconductor atoms. This is a cumulative effect and is known as ionisation due to collision. A large number of charges are thus available to constitute a large reverse current. If left uncontrolled, this reverse current can cause physical breakdown of the junction. A p-n junction diode under reverse biased condition is therefore operated well within its breakdown voltage.

V-I CHARACTERISTICS OF P-N JUNCTION DIODE :-

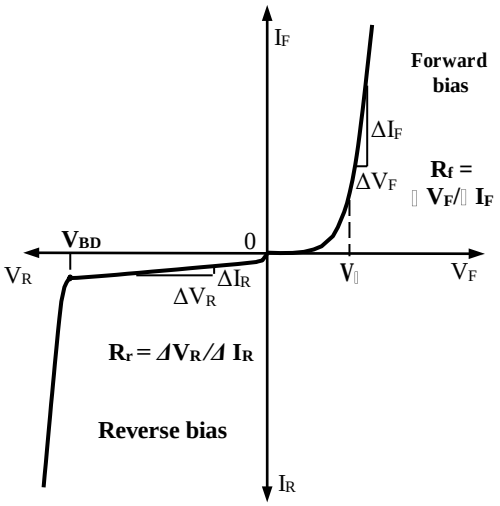


Figure shows the forward & reverse bias characteristics of a p-n junction diode.

Forward bias condition: When the forward bias voltage $V_f = 0$, the forward current I_f is also equal to 0. When the forward bias voltage is increased, current through the diode gradually increases because some high-energy electrons start crossing the junction. Any further increase in V_f causes an increase in forward current due to reduction in depletion width & potential barrier. When $V_f = V_\gamma$, the depletion width is zero & potential barrier is also zero. Now a large current starts flowing through the diode. Thus beyond V_γ the diode acts as a closed switch and offers very low resistance resulting in a rapid rise in current. The characteristics will be non-linear from the origin to V_γ because the total diode resistance $R_T = (R_J + R_B)$, where R_J is the voltage dependent junction resistance and R_B is the voltage independent semiconductor crystal bulk resistance.

The non-linearity in the characteristics from origin to V_γ is because of the junction resistance, which is reducing with an increase in voltage. The characteristic is linear beyond V_γ because the junction resistance becomes zero after V_γ & it is only the voltage independent bulk resistance R_B that remains . Thus the diode starts behaving as a closed switch only beyond V_γ with a very low value of forward resistance R_f.

Reverse bias condition :- When a p-n junction is reverse biased, a very small leakage current flows due to a very small number of temperature dependent minority carriers. The leakage current I_R is also known as reverse saturation current or minority current. This small current continues to flow until the applied reverse voltage is equal to the breakdown voltage V_{BD} . Beyond V_{BD} there is rapid increase in the leakage current due to Avalanche breakdown phenomenon. At voltages beyond V_{BD} ,minority electrons on the p-side of the junction gain sufficiently high velocities to knock out valence electrons from the semiconductor atoms within the crystal. This is a cumulative process & a large number of charges are made available to cause a large value of leakage current as shown in the characteristics. This phenomenon is also known as ionization due to collision. Hence a p-n junction diode under reverse bias condition, is operated well within its breakdown voltage if it has to work as an open switch.

DEPLETION REGION :- When a p-n junction is formed there is movement of charges across the junction due to diffusion even under unbiased conditions. This results in uncovering of the Donor ions (positive immobile ions) on the n-side & the Acceptor ions (negative immobile ions) on the p-side (Refer to Fig.2 on page-2). This region on either sides of the junction consisting of the uncovered immobile positive & negative ions is known as the Depletion Region. Since this region is depleted of mobile charges ie. there are no mobile charges it is known as the

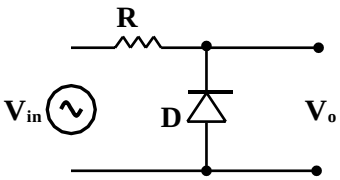
Depletion region or Transition Region. It is also known as the space charge region because it consists of immobile positive & negative ions. Since this region does not contain mobile charges it behaves as an insulator. The region across the junction which does not have mobile charge carriers is known as the depletion width.
When a p-n junction is forward biased, due to the applied voltage the Depletion Width gets reduced and the diode starts conducting because of the lower value of junction resistance.
When the p-n junction is reverse biased, due to the applied reverse bias voltage the Depletion Width increases and the diode offers a very high resistance to the flow of current due to the increased width of the insulator.
BARRIER POTENTIAL :- The electric field that exists across a p-n junction between the positive immobile ions on the n-side & negative immobile ions on the p-side of the depletion region is known as the Barrier. Uncovered donor & acceptor ions exist on either sides of a p-n junction. These are isolated positive & negative electrical charges which can result in an electric field at the junction. This electric field prevents further diffusion of holes & electrons across the junction under unbiased conditions, ie. it acts as an obstruction or barrier to the movement of electric charges, hence it is known as the potential barrier. The physical distance from one side of the barrier to the other side is known as the barrier width. The difference in potential between the two sides is known as the height of potential barrier. The potential barrier is approximately 0.7V for a Silicon diode & 0.3V for a Germanium diode.

DIODE APPLICATIONS :

Diode clipping circuits :

A clipper circuit is a diode network which can clip off a portion of the input signal without distorting the remaining waveform. Clipper circuits are also known as Slicers or Limiters. Depending on the diode connection in the circuit the positive or negative side of the input waveform is clipped. If a dc voltage source is connected in series with the diode it is known as a biased clipper if not it is known as an unbiased clipper. If the diode is in parallel with the output terminals the circuit is known as a parallel clipper (shunt clipper) and if the diode is in series with the output terminals it is known as a Series clipper. The reference voltage at which the waveform has to be clipped should always be less than the maximum or peak voltage of the input signal (ie. $V_R < V_m$).
In all clipper circuits it is assumed that the diode used for clipping is an ideal diode ie. it's cut-in voltage is zero (ie. $V_\gamma = 0$) & the forward resistance is also zero(ie. $R_f = 0$).

Negative wave clipper:



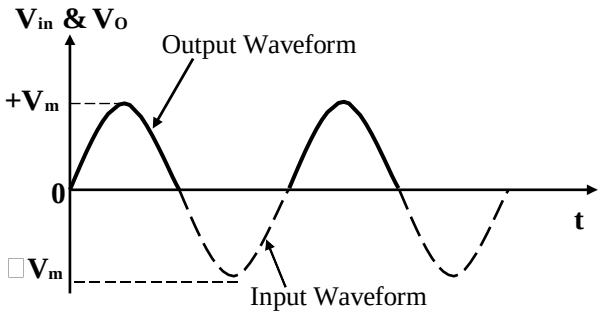


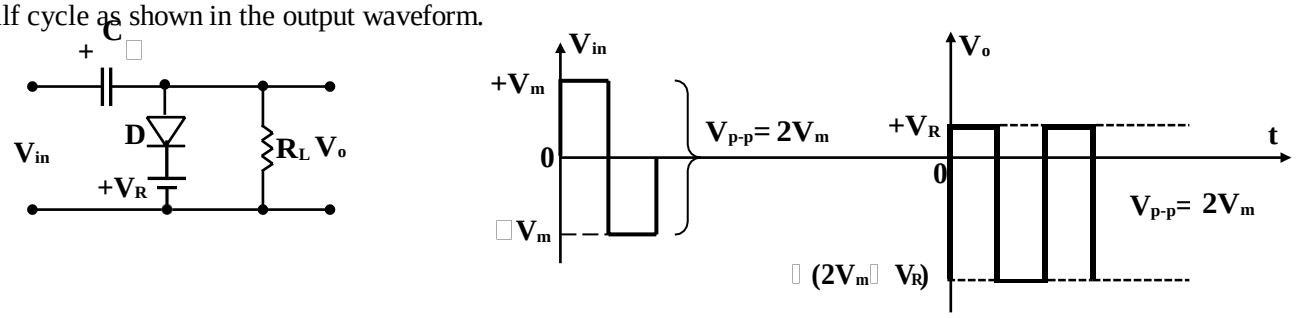
Figure shows the circuit diagram of a negative wave clipper. The diode D is assumed to be an ideal clipping device ie. its cut-in voltage $V_\gamma = 0$ & the forward resistance $R_f = 0$.
During the positive half cycle diode D gets reverse biased and acts like an open switch (infinite resistance) . Hence the output wave form follows the input waveform.
During the negative half cycle diode D gets forward biased and acts like a closed switch (zero resistance) . Hence the output voltage across a zero resistance will be zero.
In this circuit only the negative half cycles are clipped while the positive half cycles appear at the output.

Diode Clamping Circuits :

The circuit is also known as DC level shifter or DC level restorer. A diode clamping circuit is used to fix an AC signal to any desired DC level (zero, positive or negative) without changing the shape or amplitude of the input signal. Both the positive & negative peaks can be clamped to any desired DC level. It is important that the (R.C) time constant of the circuit is very large when compared to the time period of the input waveform. This condition will keep the output waveform undistorted (ie. the square wave will have constant amplitude during the entire half

cycle). The reference voltage to which the waveform has to be fixed or clamped should always be less than the maximum or peak voltage (V_m) of the input signal.
In all clamper circuits it is assumed that the diode used for clamping is an ideal diode ie. it's cut-in voltage is zero (ie. $V_\gamma = 0$) & the forward resistance is also zero (ie. $R_f = 0$) .

Positive peaks clamped to positive reference voltage :
Figure shows the circuit diagram which clamps the positive peaks of the input waveform to a positive reference voltage level. The diode D is assumed to be an ideal clamping device ie. its cut-in voltage $V_\gamma = 0$ & the forward resistance $R_f = 0$.
During the positive half cycle , diode D gets forward biased and capacitor C charges to a voltage equal to ($V_m - V_R$) with a polarity as shown in the circuit. Since the diode is a closed switch (zero cut-in voltage & zero forward resistance), the output voltage will be equal to the reference voltage($+V_R$ volts) during the entire positive half cycle as shown in the output waveform.



During the negative half cycle, the input voltage will be in series with the capacitor voltage which is already charged to ($V_m - V_R$) , the diode is kept reverse biased by the sum of the input & capacitor voltages. The diode now behaves as an open switch and the output voltage will be equal to the sum of the input & capacitor voltages ie. equal to [–($2.V_m - V_R$)]. Thus in the output voltage waveform the positive peaks appear to be clamped to a positive reference voltage level V_R during the entire negative half cycle. After clamping it is observed that the output peak to peak voltage swing remains unchanged at a value equal to ($2.V_m$).

Half wave rectifier :

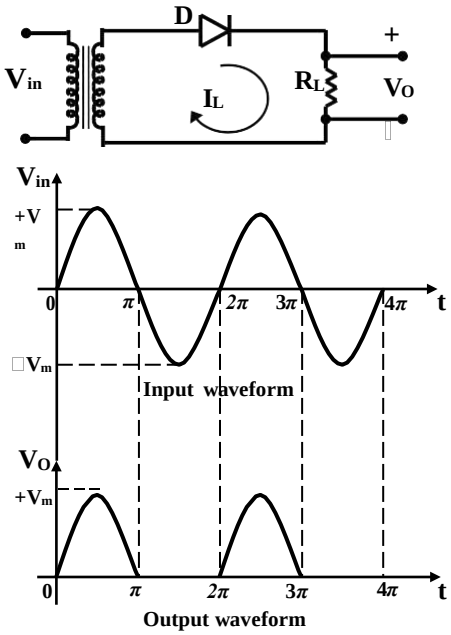
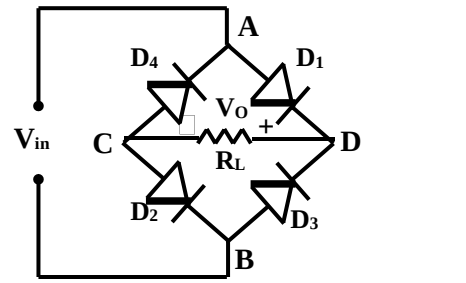


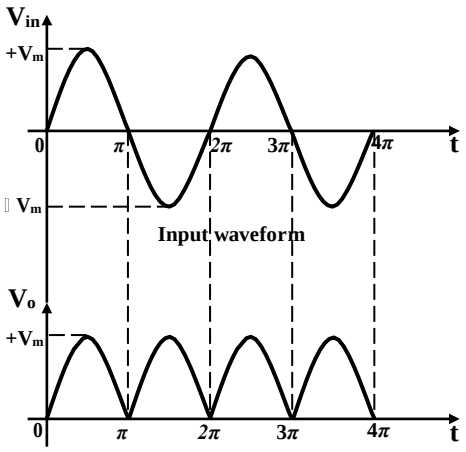
Figure shows the circuit diagram of a half wave rectifier. It consists of a silicon diode D connected to the secondary of a step down transformer. The load resistance R_L is connected in series with the diode.
During the positive half cycle (0 to π), the diode D is forward biased and acts like a closed switch offering very low resistance. The load current I_L varies in accordance with the input voltage V_{in} ($I_L \propto V_{in}$) as shown in figure. The output voltage V_O is equal to ($I_L.R_L$) , since R_L is a constant the output voltage $Vo \propto I_L$. Thus during positive half cycle, the output voltage follows the load current & in turn the input voltage V_{in}.
During the negative half cycle(π to 2π)., the diode D is reverse biased and acts like an open switch ie. the diode offers very high resistance. Thus the load current I_L is almost zero, so that V_O is zero during the negative half cycle
This cycle repeats and the circuit produces an output only during one half of the input cycle. This circuit is therefore known as a half wave rectifier. The output of this circuit is a pulsating DC whose frequency is equal to the input frequency. For a half wave rectifier we have the following important expressions:

$I_{DC} = (I_m / \square)$; $I_{RMS} = (I_m/2)$

% $\square$ = 40.6 ; Ripple Factor =1.21

Full wave bridge rectifier:





Output waveform

A full wave bridge rectifier uses four diodes as shown in the circuit diagram. The load resistance R_L is connected between C and D, while the input voltage is applied between points A and B.

During the positive half cycle (0 to π), point A is at a higher potential than B, hence diodes D_1 and D_2 are forward biased and act as closed switches. The current I_1 flows from points A to B through D_1, R_L and D_2. Both D_3 and D_4 are reverse biased during the positive half cycle and act as open switches. Thus the output current during positive half cycle due to diodes D_1 and D_2 flows through R_L and produces an output as shown in the waveforms.

During the negative half cycle (π to 2π), point B is at a higher potential than A, hence D_3 and D_4 are forward biased and act as closed switches. Current I_2 flows from point B to point A through D_3, R_L and D_4. Both D_1 and D_2 are reverse biased during the negative half cycle and act as open switches. The output current due to D_3 and D_4 flows through R_L producing an output as shown in the waveforms.

The direction of currents I_1 and I_2 through the load resistance R_L during both the half cycles is identical, hence the output voltage has the same polarity and is plotted in the same quadrant. As the circuit produces an output during both the half cycles, it is known as a full wave rectifier. In this case the output voltage is $+V_m$ if the input voltage has a peak value of V_m. The output frequency is twice the input frequency.

For a Full wave rectifier we have the following important expressions:

$I_{DC} = (2I_M / \pi)$; $I_{RMS} = (I_M/\sqrt{2})$

% η = 81.2 ; Ripple Factor = 0.48

Rectifier efficiency :- It is defined as the ratio of DC output power to the AC input power. It is a measure of the AC to DC conversion capacity of the rectifier circuit.

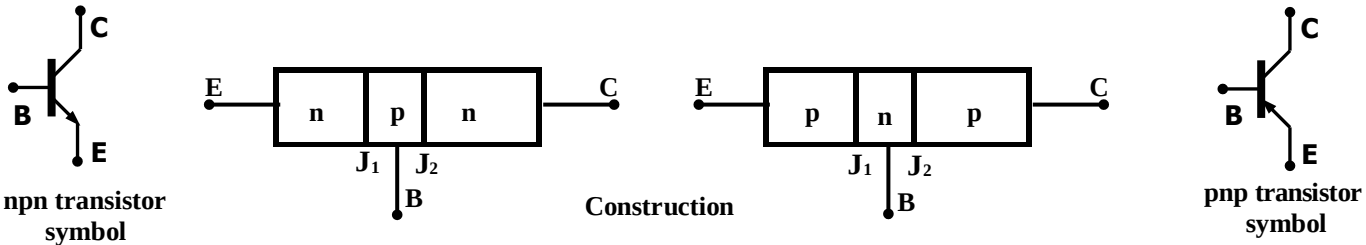
$\eta = P_{DC} / P_{AC}$ = [output DC power / input AC power] = $[(V_{DC}.I_{DC}) / \{(V_{rms})^2/(R_f + R_L)\}]$

Ripple factor :- It is defined as the ratio of RMS value of AC component to the average value of the dc component. It is the measure of the pulsating component in the output.

Ripple factor = ripple voltage / DC value of output

Ripple factor = [RMS value of AC component / DC value of output] = $[(I_{rms} / I_{dc})^2 - 1]^{1/2}$

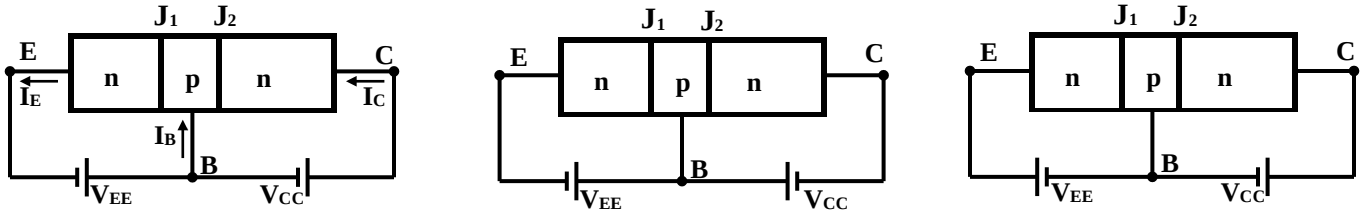
BIPOLAR JUNCTION TRANSISTORS :



A transistor is fabricated using a single cryzstal of Germanium or Silicon. It is a 3 terminal device having alternate p and n layers with two junctions J_1 & J_2. This type of construction results in npn and pnp transistors. In a npn transistor, the p-layer is sandwiched between two n-layers. The first n-layer is the emitter which emits electrons. The n-type emitter layer is heavily doped to provide better injection efficiency. The other n-layer is the collector which collects electrons. The collector region is moderately doped and has a large width to help better heat dissipation. The p-type base layer forms one junction (J_1) with the emitter and another junction (J_2) with the collector layer. The base region is lightly doped and has a narrow width , this helps in reducing recombination in the base and in the process reduces the value of base current & increases the value of collector current.

In a pnp transistor the n-layer is sandwiched between two p-layers. The construction and symbol for npn and pnp transistors is as shown in figure. The arrow mark on the emitter lead indicates the direction of flow of conventional current.

TRANSISTOR BIASING:-



Transistor biased as Amplifier | **Transistor biased as closed switch** | **Transistor biased as open switch**

If a transistor has to work as an amplifier, the base-emitter junction J_1 must be forward biased and the collector-base junction J_2 must be reverse biased. Transistor biasing is a process of creating an appropriate potential difference across the base-emitter and the collector-base junctions. The base-emitter junction should always be forward biased by a voltage greater than its cut-in voltage (V_γ), while the collector-base junction should be sufficiently reverse biased for efficient collection of charges. If these two conditions are satisfied, the transistor provides faithful amplification while operating in the active region (linear region).

A transistor can also operate as a switch (in the non-linear regions). If both the emitter-base & collector-base junctions are forward biased then the transistor will behave as a closed switch offering almost zero resistance(saturation region) . If both the emitter-base & collector-base junctions are reverse biased then the transistor behaves as an open switch offering very high resistance(cut-off region)

TRANSISTOR OPERATION :-

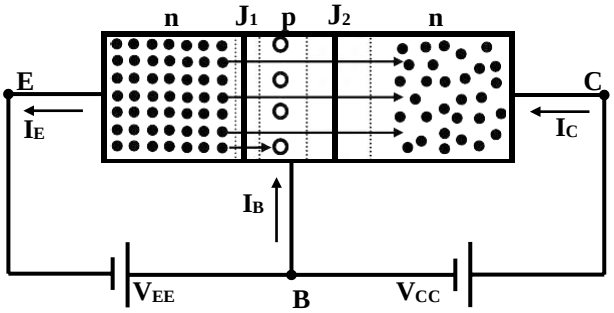


Figure shows the battery connections and directions of current in a npn transistor. V_{EE} is the emitter battery, which forward biases the base-emitter junction while V_{CC} is the collector battery which reverse biases the collector-base junction. I_B is the base current, I_C is the collector current and I_E is the emitter current. The forward biased base-emitter junction makes the emitter inject a large number of electrons into the base region. Electrons are minority carriers in the p-type base region, hence they easily diffuse into the collector region. Some electrons are lost due to recombination in the p-type base region and constitute a small base current. The base current magnitude is kept minimum by using a lightly doped narrow base region. The reverse biased collector-base junction will assist the diffusion of minority carriers (electrons) from base to the collector region. These electrons are then collected by the positive terminal of the battery V_{CC}. Electrons flowing out of the collector constitute a large collector current. Using Kirchoff's law, the fundamental transistor equation can be shown to be : $I_E = I_B + I_C$

I_B is very small when compared to I_C (3 to 4 % of I_C). Therefore $I_E \cong I_C$, ie. input current = output current.
A small reverse current flows through the collector-base junction when the emitter lead is open (when the input current is zero). This reverse current or leakage current is I_{CBO} (collector to base current with emitter open), ie. the output collector current $I_C = I_{CBO}$ when the input current is zero. I_{CBO} is temperature dependent and independent of the applied reverse voltage. In a transistor, a large emitter current flowing through a low resistance input circuit is transferred into a high resistance collector circuit (output circuit), hence it is called a transfer-resistor or a transistor.

TRANSISTOR CONFIGURATIONS :-

A transistor has only 3 leads hence any one of the 3 leads has to be common to the input & output circuits if the transistor is to be considered as a 2-port linear network . Depending on the lead that is common to both the input & output circuits there are three transistor configurations :

(1) Common-base configuration or Grounded-base configuration.
(2) Common-emitter configuration or Grounded-emitter configuration.
(3) Common-collector configuration or Grounded-collector configuration.

The behaviour of a transistor varies greatly with each configuration & can be understood by studying the input & output characteristics in all the 3 configurations.

COMMON BASE CONFIGURATION :-

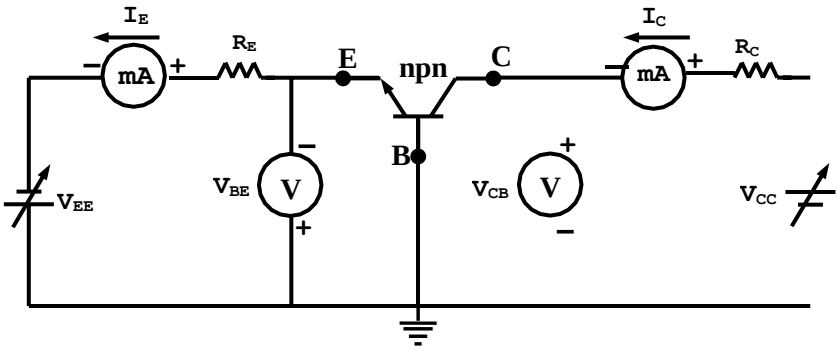


Figure shows the circuit arrangement for obtaining the input and output characteristics of a npn transistor in common-base configuration. V_{EE} is the emitter battery on the input side and R_E is the emitter current limiting resistor. The milliammeter is used to measure the emitter current(input current) while the voltmeter is used to measure the input voltage V_{BE}. V_{CC} is the collector battery on the output side and R_C is the collector resistance.

The milliammeter measures the collector current (output current) while the voltmeter measures the collector-base voltage, V_{CB} (output voltage). Here the base lead is common to both the input and output circuits, hence it is known as the common-base configuration.

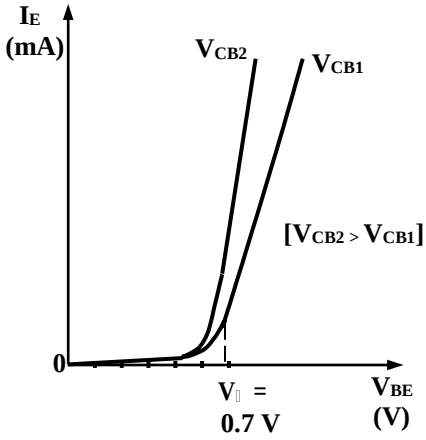
Input Characteristic:-

The input characteristics is a plot of Input voltage v/s Input current keeping output voltage constant .
ie. V_{BE} v/s I_E keeping V_{CB} constant.

The input characteristics is obtained by varying V_{BE} in steps and noting down the corresponding values of I_E keeping V_{CB} constant. A family of curves can be obtained for different values of V_{CB}.

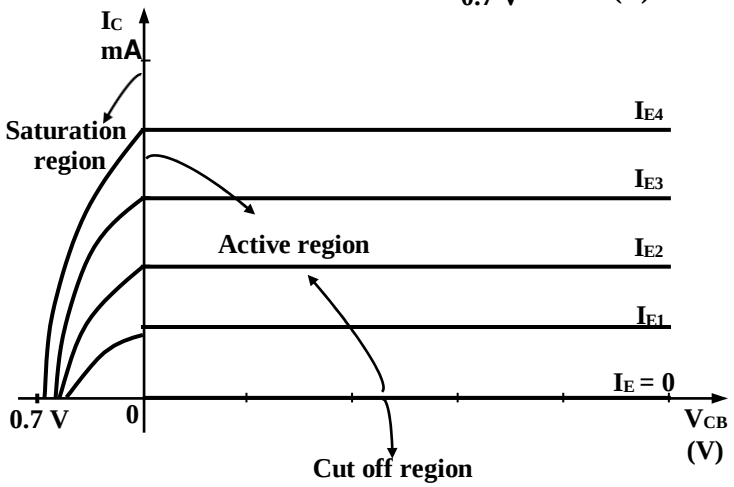
The dynamic input resistance r_i is obtained using the relation:

$$r_i = \Delta V_{BE} / \Delta I_E \mid V_{CB} = \text{constant.}$$



Output Characteristic:-

The output characteristic is a plot of output voltage v/s output current keeping input current constant,
ie. **V_{CB} v/s I_C keeping I_E constant.**
It is obtained by varying V_{CB} in steps and noting down the corresponding values of I_C keeping I_E constant.
A family of curves are obtained for different values of I_E. $I_C \approx I_E$ because I_B is very small. The slope of the output characteristic is almost zero, this means that the output resistance is very large.



The dynamic output resistance is given by the relation:

$r_o = \Delta V_{CB}/\Delta I_C \mid I_E = \text{constant.}$

α is the current gain of a transistor in common base configuration and is determined using the relation:

$\alpha = \Delta I_C/\Delta I_E \mid V_{CB} = \text{constant.}$

The input resistance r_i has a very low value (5 to 15 Ω) while the output resistance has a very high value(≈1M Ω). The current gain α has a value less than 1 (0.95 to 0.995). The voltage gain is high (150-200).

Applications:- A transistor in common-base configuration is used as a Wide-band amplifier, a constant current source and a buffer amplifier (for impedance matching).

COMMON EMITTER CONFIGURATION :

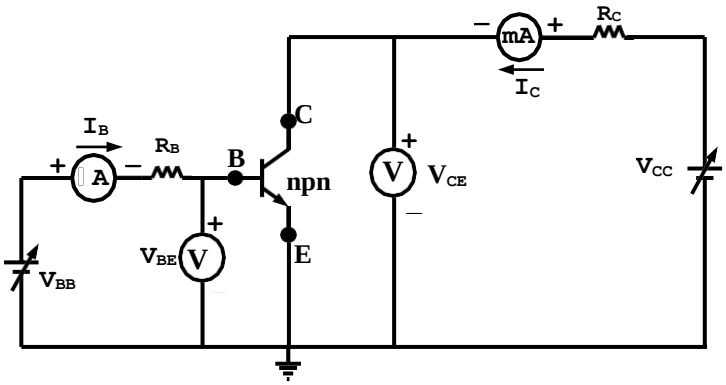


Figure shows the circuit diagram for a transistor in common-emitter configuration. Battery V_{BB} is used to forward bias the base-emitter junction. The microammeter measures the input current I_B and the voltmeter measures the input voltage V_{BE}. Battery V_{CC} is used to reverse bias the collector-base junction ($V_{CC}>V_{BB}$). The milliammeter is used to measure the output current I_C while the voltmeter measures the output voltage V_{CE}. R_B is the base resistor and R_C is the collector resistor. Here the emitter lead is common to both the input and output circuits, hence it is known as common-emitter configuration

Input Characteristic:-

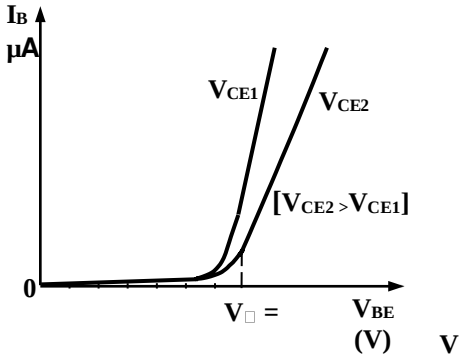
The input characteristics is a plot of Input voltage v/s Input current keeping output voltage constant .

ie. V_{BE} v/s I_B keeping V_{CE} constant

The input characteristics is obtained by varying V_{BE} in steps and noting down the corresponding values of I_B keeping V_{CE} constant. A family of curves can be obtained for different values of V_{CE}.

The dynamic input resistance r_i is obtained using the relation:

$r_i = \Delta V_{BE}/\Delta I_B \mid V_{CE} = \text{constant.}$



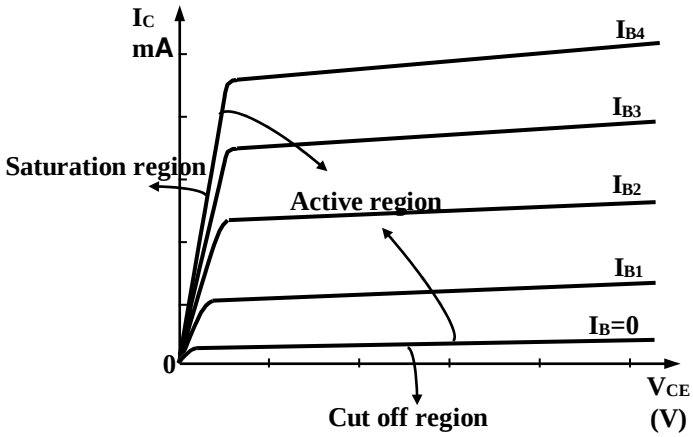
Output Characteristic:-

The output characteristic is a plot of output voltage v/s output current keeping input current constant,

ie. **V_{CE} v/s I_C keeping I_B constant.**

It is obtained by varying V_{CE} in steps and noting down the corresponding values of I_C keeping I_B constant.

A family of curves is obtained for different values of I_B. The slope of the output characteristic is appreciable, this means that the output resistance is not as large as in case of common-base configuration. The dynamic output resistance is given by the relation:



$r_o = \Delta V_{CE}/\Delta I_C \Delta I_B = \text{constant.}$

β is the current gain of a transistor in common-emitter configuration and is determined using the relation:

$\beta = \Delta I_C/\Delta I_B \Delta V_{CE} = \text{constant.}$

The input resistance r_i is high when compared to common-base configuration (500 Ω to 1.5kΩ).The output resistance has a high value (15 kΩ to 50 kΩ). The current gain β has a very large value (200 to 400). The voltage gain is very high (250 to 500).

Applications:- A transistor in common-emitter configuration is used as a voltage amplifier, power amplifier and multi-stage amplifier.

Important Equations For Transistor In Common Emitter Configuration:-

[1] $I_C = \beta.I_B + (1+\beta) I_{CBO} = \beta.I_B + I_{CEO}$. ; **[2]** $I_C = \beta.I_B$ (neglecting leakage current, ie. $I_{CEO} = 0$).

[3] $I_C = I_{CEO}$ (when input current $I_B = 0$) ; **[4]** $I_{CEO} = (1 + \beta).I_{CBO}$.

COMMON COLLECTOR CONFIGURATION :-

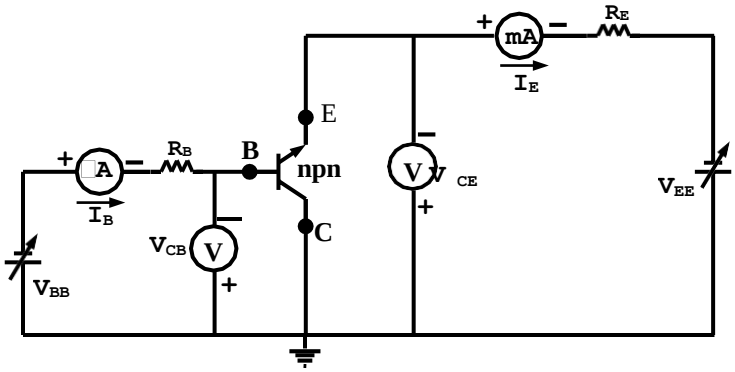
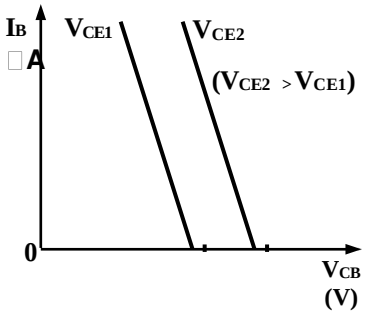


Figure shows the circuit diagram for a npn transistor in common-collector configuration. Battery V_{BB} is used to reverse bias the collector-base junction. The microammeter measures input current I_B and the voltmeter measures input voltage V_{CB}. Battery V_{EE} along with V_{BB} is used to forward bias the base-emitter junction (V_{EE} is at lower potential than V_{BB}). The milliammeter is used to measure output current I_E , while the voltmeter measures the output voltage V_{CE}. (I_E is the output current and V_{CE} is the output voltage).R_B is the base resistor and R_E is the emitter resistor. Here the collector lead is common to both the input and output circuits, hence it is known as common-collector configuration.

Input Characteristic:-

The input characteristics is a plot of Input voltage v/s Input current keeping output voltage constant .

ie.V_{CB} v/s I_B keeping V_{CE} constant.



The input characteristics is obtained by varying V_{CB} in steps and noting down the corresponding values of I_B keeping V_{CE} constant. A family of curves can be obtained for different values of V_{CE}.

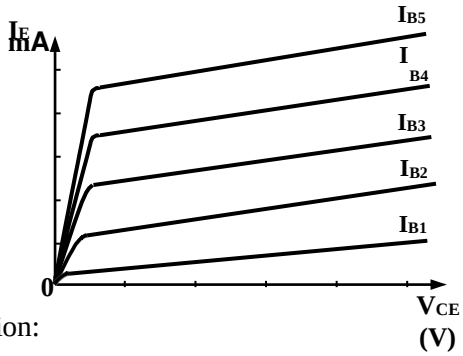
The dynamic input resistance r_i is obtained using the relation:

$$r_i = \Delta V_{CB}/\Delta I_B \,|\, V_{CE} = \text{constant.}$$

Output Characteristic:-

The output characteristic is a plot of Output voltage v/s Output current keeping Input current constant,

ie. **V_{CE} v/s I_E Keeping I_B constant.**



It is obtained by varying V_{CE} in steps and noting down the corresponding values of I_E keeping I_B constant.

A family of curves are obtained for different values of I_B.

$I_C \approx I_E$ because I_B is very small.

The slope of the output characteristic is more appreciable than that of the common-emitter configuration, this means that the output resistance is much smaller than that of the common-emitter configuration. The dynamic output resistance is given by the relation:

$$r_o = \Delta V_{CE}/\Delta I_E \,|\, I_B = \text{constant.}$$

γ is the current gain of a transistor in common-collector configuration and is determined using the relation:

$$\gamma = \Delta I_E/\Delta I_B \,|\, V_{CE} = \text{constant.}$$

The input resistance r_i is very high when compared to common-emitter configuration (≈1 MΩ).The output resistance has a very low value (less than 500Ω). The current gain γ has a very large value (β + 1). The voltage gain is very low ($A_V \approx 1$).

Applications:- It is used as a buffer amplifier to provide excellent impedance matching between two stages. The circuit is commonly known as an **Emitter follower.**

Comparison Of The Three Transistor Configurations:-

Sl. No.	PARAMETER	C-B Confgrn.	C-E Confgrn.	C-C Confgrn.
1	Current gain	Very low (<1)	Very high (200-400)	Very high (1+β)
2	Voltage gain	High (100-200)	Very high (250-500)	Very low (<1)
3	Input impedance	Very low (10-15Ω)	Medium (~ 1 kΩ)	Very high (~ 1MΩ)
4	Output impedance	Very high (≈1 MΩ)	Medium (20-50 kΩ)	Very low (< 1 kΩ)
5	Applications	Wide-band Amp, Constant current source, Buffer Amp.	Voltage Amp, multi-stage Amp, power-Amp, Audio Amp.	Buffer Amp. (as Impedance matching network)

RELATIONSHIP BETWEEN □ AND □:-

□ is the current gain of a transistor in common-base configuration and is given by the relation, □ = □I_C / □I_E

□ is the current gain of a transistor in common-emitter configuration and is given by the relation, □ = □I_C / □I_B

(1) □ in terms of □:- The basic transistor equation is given by: $I_E = I_B + I_C$.----------**(A)**

Considering the incremental values, we have $\Delta I_E = \Delta I_B + \Delta I_C$----------**(B)**

Divide equation **(B)** through out by ΔI_C, ie. $(\Delta I_E / \Delta I_C) = (\Delta I_B / \Delta I_C) + (\Delta I_C / \Delta I_C)$ ---------- **(C)**

But $(\Delta I_C / \Delta I_E) = \alpha \Rightarrow (\Delta I_E / \Delta I_C) = (1 / \alpha)$ **&** $(\Delta I_C / \Delta I_B) = \beta$ □ $(\Delta I_B / \Delta I_C) = (1 / \beta)$

ie. $(1/\alpha) = (1 / \beta) + 1$ ----------**(D).**

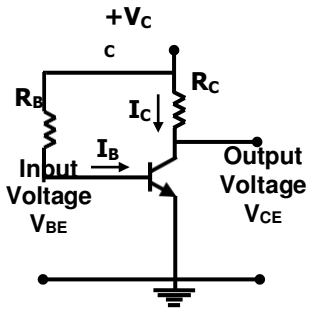
ie. $(1 / \alpha) = (1+ \beta) / \beta$; Taking the reciprocal we have :

□ = □ / (□ + **1)**

(2) □ in terms of □:- From equation **(D)**, we have $1 / \alpha = 1 + (1 / \beta)$ □ $1/ \beta = (1 / \alpha) - 1$ ie.

$(1 / \beta) = (1 - \alpha) / \alpha$ □ □ □ = □ / **(1** – □**)**

FIXED BIAS CIRCUIT or BASE BIAS CIRCUIT : Figure shows a fixed bias circuit . V_{CC} is the battery used for biasing both the junctions. R_C is the collector resistance & R_B is the base resistance. The Q-point is located in the active region by properly selecting the values of V_{CC}, R_B & R_C, so that a proper value of base current (I_B) will fix up the quiescent I_{CQ} & V_{CEQ} & hence the operating point.
The operating point position on the load line can be determined by calculating the values of I_C & V_{CE} in the circuit.



(1) The output Current or Collector Current (I_C):
The output current or the Collector current is given by the expression :
$I_C = \beta.I_B + I_{CEO}$ [but I_{CEO} is very small compared to $\beta.I_B$]
Hence $I_C = \beta.I_B$----------**(A)**
But the base current or input current is given by : $I_B = [V_{CC}/R_B]$
Therefore the collector current is given by : $I_C = \beta.[V_{CC}/R_B]$----------**(B)**

(2) The output voltage or the Collector- Emitter Voltage (V_{CE}):
The out put voltage or the Collector-Emitter voltage is given by:
$V_{CC} = I_C.R_C + V_{CE}$
ie. $V_{CE} = [V_{CC} - I_C.R_C]$ ---------- **(C)**
Use the value of I_C from equation (B) in equation (C) ,
ie. $V_{CE} = V_{CC}[1 - \beta.(R_C/R_B)]$ ---------- (D)
The values of I_C and V_{CE} obtained using equations (B) and (D) will help in locating the operating point of the transistor on the DC load line .

RGPVNOTES.IN

We hope you find these notes useful.

You can get previous year question papers at https://qp.rgpvnotes.in .

If you have any queries or you want to submit your study notes please write us at rgpvnotes.in@gmail.com

LIKE & FOLLOW US ON FACEBOOK
facebook.com/rgpvnotes.in