SCHOOL OF COMPUTER ENGINEERING

KALINGA INSTITUTE OF INDUSTRIAL TECHNOLOGY

DEEMED TO BE UNIVERSITY

BHUBANESWAR

LESSON – PLAN

School	**:**	School of Computer Engineering
Program	**:**	B. Tech. CSE
Academic Session	**:**	Autumn Semester 2022 (July. - November)
Subject	**:**	High Performance Computing (HPC) (CS 3010)
Course Cridit	**:**	4 (L-T-P) (3-1-0) (Weekly 4 Hours)
Semester	**:**	5th Semester (2020 admitted batch)
Faculty	**:**	Prof Rabi Shaw (rabi.shawfcs@kiit.ac.in)

Course Outcomes/Learning Objectives:

1. Understand different quantitative techniques used to measure the performance of the system with various criteria like CPI, CPU time, speed up, throughput, efficiency, etc.
2. Understand the concept of different types of hazards along with their structural implementation and applications.
3. Identify the criteria to enhance the performance of pipelined processors.
4. Understand memory hierarchy and to analyze various Cache optimization techniques.
5. Understand ILP and the techniques to exploit ILP in scalar, superscalar, super pipelined processor, and the VLIW processor.
6. Classify various parallel architecture like centralized and distributed memory architecture

Prerequisite: Computer Architecture (CS-2006)

Module No. & name / Section no. Name	Topics/ Coverage	No. of Class
1. Overview of Computer Architecture	**1.** Introduction to HPCA I. Moore's Law II. Classes of Computers III. Computer Architecture Overview **2.** Performance Measurement (concepts with numerical) I. Performance Measurement with respect to execution time, CPU time	8

	II. Performance Measurement with respect to the basic performance equation III. **Amdahl's law** (Exercises Based on Amdahl's Law) **3.** Introduction to **instruction Set architecture (ISA)** **4.** CISC & RISC processor	
	ACTIVITY-1 (Assignment-1)	
2. Pipelining	1. Introduction to parallel processing & pipelining Concept. 2. Introduction to MIPS Architecture with its data path 3. A brief introduction to Hazard and its possible effects on performance due to pipeline stalls 4. Types of Hazards and Pipeline Stall Cycles I. Structural Hazard II. Data Hazard III. Control Hazard 5. A technique for overcoming or reducing the effects of Various hazards (Solution to different Hazards) I. Operand forwarding and Instruction scheduling II. Flush pipeline, Branch Prediction, Delay Slot	10
Tutorial	Doubt Clearance	2
	ACTIVITY-2 (Quiz-1)	
3. Instruction Level Parallelism (ILP)	1. Concepts of instruction-level parallelism (ILP) 2. Techniques for increasing ILP I. Dynamic branch prediction II. Loop unrolling (with Numerical) III. Static scheduling ✓ Scoreboard approach (With Numerical) IV. Dynamic scheduling ✓ Tomasulo's approach (With Numerical) 3. Superscalar & Super pipelined 4. VLIW processor architecture	10
Tutorial	Doubt Clearance	2
	ACTIVITY-3 (ASSIGNMENT-2)	
	Mid-Semester Examination	
4. Hierarchical Memory Technology	1. Memory hierarchy 2. Cache memory organization I. Block Placement II. Block Identification	8

	III. Block Replacement IV. Write Strategy V. Numerical examples on cache Memory performance 3. Cache Memory Performance evaluation 4. Cache Memory Optimization Techniques I. Reduce miss rate. ✓ Larger block size ✓ Larger cache size ✓ Higher associativity II. Reduce miss penalty. ✓ Multilevel caches ✓ Priority to Read Misses over Writes III. Reduce hit time. ✓ Avoiding address translation	
Tutorial	Doubt Clearance	2
	ACTIVITY- 4 (Quiz-2)	
5.Multiprocessor Architecture	1. Taxonomy of Parallel Architecture 2. Types of Interconnection Networks (Basic concepts) I. Time shared common Bus, multiport, Crossbar II. Multistage switch network, and Hypercube System 3. Multiprocessor Systems I. Centralized Shared-memory architecture (Tightly coupled multiprocessor like UMA) II. Distributed Shared memory architecture (Loosely coupled multiprocessor like NUMA) 4. Cache coherence protocol I. Snooping protocol II. Directory-based protocol	8
Tutorial	Doubt Clearance	2
	End-Semester Examination	

Text Book :

1. John L. Hennessy and David A. Patterson, Computer Architecture: A Quantitative Approach, Morgan Kaufmann.

References Books :

1. John Paul Shen and Mikko H. Lipasti, Modern Processor Design: Fundamentals of Superscalar Processors, Tata McGraw-Hill.

2. M. J. Flynn, Computer Architecture: Pipelined and Parallel Processor Design, Narosa Publishing House.
3. Kai Hwang, Advanced Computer Architecture: Parallelism, Scalability, Programmability, McGraw- Hill.

Pedagogy: Lecture, Assignments, Quiz.

Evaluation Methodology: Mid Term: 50 (Midterm exam 20 marks, (Assignment,Quiz and student participation 30 marks)

End Term: 50

Banchhanidhi Dash

Signature