Brandon Dinh

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Brandon-Dinh-Portfolio https://linkedin.com/in/brandontdinh

Education

California State University, Long Beach **Long Beach, CA**
Bachelor of Science in Computer Engineering Technology

Experience

DrKumo Inc. – Verification Engineer **April 2024 – Current**

- Developed automated testbenches to verify functionality and reliability of websites, including form validation, authentication flow, and backend response tracking using unittest, Selenium, and custom Python scripts.
- Implemented test flows in Python to repeatedly execute and validate application behavior under different conditions.
- Designed and deployed Python scripts to automate the generation of structured reports from patient data pipelines, exporting to Excel/CSV formats. These reports helped visualize and isolate bugs uncovered during automated web testbench runs, supporting faster debugging cycles and ensuring reliable data handling.
- Collaborated cross-functionally to trace, isolate, and correct issues, utilizing assertion-style debugging.
- Formulated and developed a hardware PCB system integrating a phone line, SIM card, and PCB to an Orange Pi, enabling secure remote patient monitoring by linking patient accounts with a Samsung tablet.
- Played a key role in troubleshooting and optimizing hardware components, while utilizing soldering skills to assemble and repair necessary equipment, contributing to the maintenance and optimization of hardware devices.

Certifications

SystemVerilog for Verification - v22.18 | *Siemens Xcelerator Academy* **July 2025**

- Developed reusable, object-oriented UVM environments using class inheritance and composition for FPGA testbenches.
- Connected virtual interfaces to DUT ports to drive and monitor signal transactions across agents, drivers, and monitors.
- Applied constrained randomization and coverage-driven verification using cover groups, cover points, and cross coverage to achieve functional coverage for digital logic. Used weighted and transition bins to prioritize corner-case conditions.
- Implemented parallel verification processes using fork-join, join_any, and join_none in the top-level module to synchronize threads, control DUT stimulus, coordinate driver, monitor, and scoreboard behavior for testbench execution.
- Integrated scoreboards, FIFOs, and reference models for self-checking validation of expected vs. actual DUT responses.

Projects (Click 🔗 to View)

SystemVerilog ALU Design and UVM Verification with RISC-V ISA 🔗 | *SystemVerilog, UVM, RTL* **June 2025**

- Designed a SystemVerilog Arithmetic Logic Unit (ALU) implementing a RISC-V–style RV32I instruction set architecture (ISA) including ADD, SUB, AND, OR, XOR, and SLT similar to ALU operations used in modern RISC-V decoders.
- Programmed a SystemVerilog UVM testbench to verify operations and edge cases, such as zero, overflow, and signed arithmetic in digital logic for functional verification.
- Created reusable UVM components (driver, monitor, scoreboard, sequences) to apply randomized and directed stimuli for exhaustive functional coverage.
- Ran simulations using assertions and coverage metrics to validate correctness, ensure FSM control stability, and debug unexpected behaviors in operand handling.

VHDL 4-Bit Calculator with Testbenching and FSM Design 🔗 | *VHDL, Testbenching, FPGA, RTL* **March 2025**

- Produced and implemented a 4-bit calculator on FPGA using VHDL, supporting addition and accumulator clear (AC) operations with finite state machine (FSM) control logic.
- Architected modular RTL components including datapath (adder, 8-bit padding), FSM control circuit, and a register module interfaced via pushbuttons and slide switches.
- Created a comprehensive VHDL testbench to verify functional correctness of "Add" and "AC" operations, including state transitions and output waveform validation, utilized from Xilinx Vivado for simulation and synthesis
- Mapped onto a FPGA board with constraints file to interface slide switches, LEDs, pushbuttons, and a 100MHz clock.

Custom Embedded PCB: Motion-Activated Detonator 🔗 | *PCB Design, Embedded, Digital Logic* **December 2024**

- Full Stack Development: Fabricated an interactive detonator prop that combines embedded systems, 3D design, and software engineering through the use of a custom designed PCB along with experience in designing and prototyping.
- Sensor Integration: Proficient in integrating and utilizing sensors such as MPU6050 accelerometer and sensors.
- Digital Communication: Knowledge of digital communication protocols like UART, I2C, and SPI.
- System Integration: Integration of audio components, such as the DFplayer Mini MP3 player, into a custom PCB.

Technical Skills

Technical: SystemVerilog, Questa, Vivado, VHDL, UVM, Verilog, FPGA, Python, ASIC, C++, Circuit Design, PCB, PLC, Motors, Oscilloscope, Waveform Generator, Arduino, Assembly, Linux, Motors, Diodes, Relays, Transistors, Power Supply