Brandon Dinh

Orange County, California 714-262-7877 brandondinhm9@gmail.com
https://brandonsprojectportfolio.carrd.co https://linkedin.com/in/brandontdinh

Education

California State University, Long Beach **Long Beach, CA**
Bachelor of Science in Computer Engineering Technology

Experience

DrKumo Inc. – Verification Engineer **April 2024 – Current**

- Developed automated testbenches to verify functionality and reliability of websites, including form validation, authentication flow, and backend response tracking using unittest, Selenium, and custom Python scripts.
- Implemented test flows in Python to repeatedly execute and validate application behavior under different conditions.
- Designed and deployed Python scripts to automate the generation of structured reports from patient data pipelines, exporting to Excel/CSV formats. These reports helped visualize and isolate bugs uncovered during automated web testbench runs, supporting faster debugging cycles and ensuring reliable data handling.
- Collaborated cross-functionally to trace, isolate, and correct issues, utilizing assertion-style debugging.
- Formulated and developed a hardware PCB system integrating a phone line, SIM card, and PCB to an Orange Pi, enabling secure remote patient monitoring by linking patient accounts with a Samsung tablet.
- Played a key role in troubleshooting and optimizing hardware components, while utilizing soldering skills to assemble and repair necessary equipment, contributing to the maintenance and optimization of hardware devices.
- Collaborated with Veterans Affairs (VA) to design a system that provides veterans easier access to health devices paired with a tablet, allowing them to connect through a phone line which utilizes the hardware components on the PCB.

Certifications

SystemVerilog for Verification - v22.18 | ***Siemens Xcelerator Academy*** **July 2025**

- Developed reusable, object-oriented UVM environments using class inheritance and composition for FPGA testbenches.
- Connected virtual interfaces to DUT ports to drive and monitor signal transactions across agents, drivers, and monitors.
- Applied constrained randomization and coverage-driven verification using `covergroups`, `coverpoints`, and cross coverage to achieve functional coverage for digital logic. Leveraged weighted and transition bins to prioritize corner-case conditions and ensure comprehensive scenario exploration across regression runs.
- Implemented parallel verification processes using fork-join, join_any, and join_none in the top-level module to synchronize threads, control DUT stimulus, coordinate driver, monitor, and scoreboard behavior for testbench execution.
- Integrated scoreboards, FIFOs, and reference models for self-checking validation of expected vs. actual DUT responses.

Projects

Parameterized ALU Design and UVM Verification | *SystemVerilog, UVM, RTL, Functional Verification* **June 2025**

- Conceived a modular FPGA-based Arithmetic Logic Unit (ALU) in SystemVerilog utilizing Questa supporting core RISC-style operations: addition, subtraction, AND, OR, XOR, shift, and set-on-less-than (SLT).
- Programmed a SystemVerilog UVM testbench to verify operations and edge cases, such as zero, overflow, and signed arithmetic in digital logic.
- Created reusable UVM components (driver, monitor, scoreboard, sequences) to apply randomized and directed stimuli for exhaustive functional coverage.
- Ran simulations using assertions and coverage metrics to validate correctness, ensure FSM control stability, and debug unexpected behaviors in operand handling.
- Built a datapath architecture allowing for flexible bit-width configuration, suitable for embedded CPU integration.

VHDL 4-Bit Calculator with Testbenching and FSM Design | *VHDL, Testbenching, FPGA, RTL Design* **March 2025**

- Produced and implemented a 4-bit calculator on FPGA using VHDL, supporting addition and accumulator clear (AC) operations with finite state machine (FSM) control logic.
- Architected modular RTL components including datapath (adder, 8-bit padding), FSM control circuit, and a register module interfaced via pushbuttons and slide switches.
- Created a comprehensive VHDL testbench to verify functional correctness of "Add" and "AC" operations, including state transitions and output waveform validation.
- Utilized Xilinx Vivado for simulation and synthesis; performed waveform analysis to debug and verify internal states using testbench stimulus and scope probing.
- Mapped the design onto a physical FPGA board with a custom constraints file to interface slide switches, LEDs, pushbuttons, and a 100MHz clock.

Technical Skills

Technical: SystemVerilog, Questa, Vivado, VHDL, UVM, Verilog, FPGA, Python, ASIC, C++, Circuit Design, PCB, PLC, Motors, Oscilloscope, Waveform Generator, Arduino, Assembly, Linux, Motors, Diodes, Relays, Transistors, Power Supply