www.csvtuonline.com

Printed Pages : 4

Roll No.

322454(22)

BE (4th Semester)
Examination, Nov.-Dec., 2017

(New Scheme)

Computer Systems Architecture

Time Allowed : 3 hours *Maximum Marks :* 80
Minimum Pass Marks : 28

Note : (*i*) Attempt **all** questions. Part (*a*) of all questions is compulsory. Attempt any **two** parts from (*b*), (*c*) and (*d*).

(*ii*) The figures in the right-hand margin indicate marks.

1. (*a*) Differentiate between direct and indirect addressing mode of instruction. [2]

(*b*) What is the role of decoders in hardwired control unit? Explain its all components with a proper block diagram. [7]

(*c*) Explain instruction cycle of basic computer with the help of flow chart. [7]

(*d*) Explain 16-bit common bus architecture of basic computer. [7]

www.csvtuonline.com

2. (*a*) Differentiate between signed magnitude and 2's complement number representation scheme with example. [2]

(*b*) Explain Booth multiplication algorithm for 2's complement numbers using flow chart and example. . [7]

(*c*) Draw and explain flow chart for addition and subtraction of two fixed-point signed magnitude binary numbers. [7]

(*d*) Discuss register configuration for various floating point operations. What are different steps involved in multiplication of floating point numbers? Explain with flow chart. [7]

3. (*a*) Define the principle of locality of references. Which parameter is used to evaluate the performance of cache memory? [2]

(*b*) A digital computer has a memory unit of 64K×16 and a cache memory of 1K words. The cache uses direct mapping with a block size of four words.

(*i*) How many bits are there in the tag, index, block and word fields of address format?

(*ii*) How many bits are there in each word of cache and how are they divided into functions? Include a valid bit.

(*iii*) How many blocks the cache can accommodate? [7]

www.csvtuonline.com

www.csvtuonline.com

(*c*) The access time of cache memory is 100 ns and that of main memory 1000 ns. It is estimated that 80% of the memory request for read and remaining for write. The hit ratio for read access only is 0.9. A write through procedure is used.

(*i*) What is the average access time of system considering only memory read?

(*ii*) What is the average access time of system for both read and write required? [7]

(*d*) Explain the working of associative memory with block diagram and derive the expression for match logic. [7]

4. (*a*) Differentiate between synchronous and asynchronous data transfer. [2]

(*b*) What is direct memory access technique? Explain the rate of DMA controller with diagram. [7]

(*c*) What is address space? Explain isolated V_5 memory mapped I/O. [7]

(*d*) Define priority interrupt. Explain daisy chain priority interrupt with block diagram. [7]

5. (*a*) Define pipelining. [2]

www.csvtuonline.com

www.csvtuonline.com

(*b*) A non-pipeline system takes 50ns to process a task. The same task can be processed in a six-segment pipeline with a clock cycle of 10ns. Determine the speedup ratio of the pipeline for 100 tasks. What is the maximum speedup that can be achieved? [7]

(*c*) Explain vector processing with diagram. [7]

(*d*) Draw and explain flow chart and timing diagram for the four-segment instruction pipeline. [7]

———

www.csvtuonline.com