Roll No. : .....

322454(22)

B. E. (Fourth Semester) Examination, April-May 2016

(New Scheme)

(CSE Engg. Branch)

COMPUTER SYSTEM ARCHITECTURE

Time Allowed : Three hours

Maximum Marks : 80

Minimum Pass Marks : 28

Note : *Attempt all questions. Part (a) is compulsory of 2 marks. Attempt any two parts from (b), (c) and (d) is of 7 marks.*

Unit-I

(a) Name functional units of computer. 2

(b) Explain all 8 addressing modes with example. 7

(c) Explain execution cycle of a complete instruction and execute simple arithmetic operation ADD R_1, R_2, R_0 using one-bus datapath. 4, 3

(d) Define hardwired control and microprogrammed control.

Explain hardwired implementation using following example. 3

Assume the instruction set of a machine has the three instructions : Inst-x, Inst-y, Inst-z, and *A, B, C, D, E, F, G* and *H* are control lines. Following table shows the control lines that should be activated for the three instructions at the three steps t_0, t_1 and t_2: 4

Step	Inst-x	Inst-y	Inst-z
t_0	D, B, E	F, H, G	E, H
t_1	C, A, H	G	D, A, C
t_2	G, C	B, C	

Unit-II

2. (a) Define guard and rounding bits. 2

(b) Explain signed multiplication through booth algorithm. Show flow chart. Also show example of Booth's Algorithm. 7

(c) Explain integer division with example and flowchart. Divide –7 by 3. 7

(d) Explain IEEE floating point number representation both 32 bits and 64 bits. Also explain normalization and expressible numbers. 7

Unit-III

(a) Show memory hierarchy. 2

(b) Explain multimodule memory and interleaving. 7

(c) Explain cache memory with its mapping functions. 7

(d) What is demand paging? What are replacement algorithms. Find hit ratio for following reference string using least recently used (LRU) algorithm. Reference string is : 4. 7, 5, 7, 6, 7, 10, 4, 8, 5, 8. 6 and no. of frame is 3. (Page frame) 7

Unit-IV

(a) Define memory mapped I/O. 2

(b) Define interrupts, types of interrupts and interrupt handling mechanisms. 7

(c) Explain direct memory access in the content of input/ output devices. 7

(d) Explain synchronous and asynchronous data transfer. 7

Unit-V

5. (a) What is pipelining and name types of pipelining? 2

(b) What is delayed branch, branch prediction and data dependency, in pipelining? 7

(c) Explain types of parallel processor system and also explain taxonomy of parallel processor architecture. 7

(d) Write short notes on : 7

(i) Vector processing/processor

(ii) Array processor