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BE (Fourth Semester) Examination, April-May 2019

(New Scheme)

(CSE Branch)

COMPUTER SYSTEM ARCHITECTURE

Time Allowed: Three hours

Maximum Marks: 80

Minimum Pass Marks: 28

Note: Attempt all questions. Part (a) of each question is compulsory. Attempt any two parts from (b), (c) and (d). Assume any suitable data.

1. (a) Define parameter passing in subroutines.

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121 (b) Explain the representation, selection and application of instruction formats. (c) Write the differences between Hardwired and Microprogrammed Control Unit. Draw the block diagram for both. (d) Explain various addressing modes with example. (a) Define Fixed point and Floating point numbers. 2 (b) Describe the implementation of binary parallel adder/ subtractor circuit using full adders. (c) Define bit pair recoding. Explain Booth's multiplication algorithm for fixed point numbers with example. (fl) Explain the floating point operations with example. Define guard bits. 2 (a) Define virtual memory. (b) Discuss the concept of multimodule memories and memory interleaving in memory organization. (c) Explain the associative memory organization and derive the expression for match logic.

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	(d)	Define Cache mapping. Explain the types of cache mapping with examples.	72.7 7
4.	(a)	Define interrupts.	2
	(b)	Write down the differences between I/O mapped I/O and memory mapped I/O.	7
	(c)	Define priority interrupt. Explain daisy chaining priority interrupt with block diagram.	7
	(d)	What is Direct Memory Access? Explain DMA controller with the help of block diagram.	7
5.	(a)	Define pipelining.	2
	(b)	Explain 4 stages of instruction pipelining.	7
	(e)	Explain the fault taulerance system. Describe static and dynamic redundancy.	7
	(d)	Define parallel processing. Describe Flynn's classification of parallel processing.	; 7
		paratier processing.	,

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