Printed Pages : 3

Roll No.

# 322454(22)

## BE (4th Semester)
## Examination, Nov.-Dec., 2018

**(New Scheme)**

## Computer Systems Architecture

*Time Allowed* : 3 hours *Maximum Marks* : 80

*Minimum Pass Marks* : 28

***Note :*** *(i)* Part *(a)* of each question is compulsory. Attempt any **two** parts from (*b*), (*c*) and (*d*).

*(ii)* The figures in the right-hand margin indicate marks.

**1.** (*a*) What is the primary function of CPU? [2]

(*b*) Explain accumulator based CPU with proper diagram. [7]

(*c*) What are the different adderssing modes? Explain in detail. [7]

(*d*) Evaluate the arithmatic statement :

$X = (A + B) * (C + D)$

using three address instruction and two address instruction.









**2.** (*a*) Define terms Overflow and Underflow. [2]

(*b*) Describe Booth Multiplication Algorithm with example. [7]

(*c*) Explain fixed and floating point representation with proper example. [7]

(*d*) Give functional block diagram of sequential ALU and also explain its working. [7]

**3.** (*a*) Define Cache Memory. [2]

(*b*) Explain stack organisation and its operations in brief. [7]

(*c*) The access time of cache memory is 100 ns and that of main memory 1000 ns. It is estimated that 80% of the memory request for read and remaining 20% for write. The hit ratio for read access is only 0.9. A write through procedure is used :

(*i*) What is the average access time of the system considering only memory read cycle. [3]

(*ii*) What is average access time for both read and write cycle. [2]

(*iii*) What is the heat ratio taking into consideration the write cycle. [2]

(*d*) What are the different types of mapping used in cache organisation. Explain any one in detail with diagram. [7]



*(Continued)*

4. (*a*) What is Priority Interrupt? [2]

(*b*) What is DMA? How data is transferred in DMA? [7]

(*c*) Write the differences between Static and Dynamic RAM. [7]

(*d*) How Daisy Chaining priority interrupt works? Explain with diagram. [7]

5. (*a*) Define fault Tolerance? [2]

(*b*) Explain Vector processing and Vector operations. [7]

(*c*) How processor level parallelism can be achieved? Explain various techniques. [7]

(*d*) Explain 6 stages of instruction pipeline. [7]

———