MID-SEMESTER EXAMS

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Subject :- Computer Architecture

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Q1. ans) The logic diagram of a carry look-ahead adder is drawn below and full adder are :-

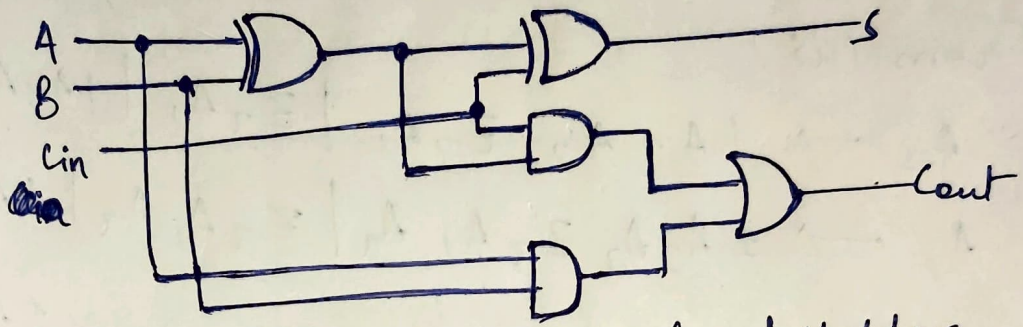
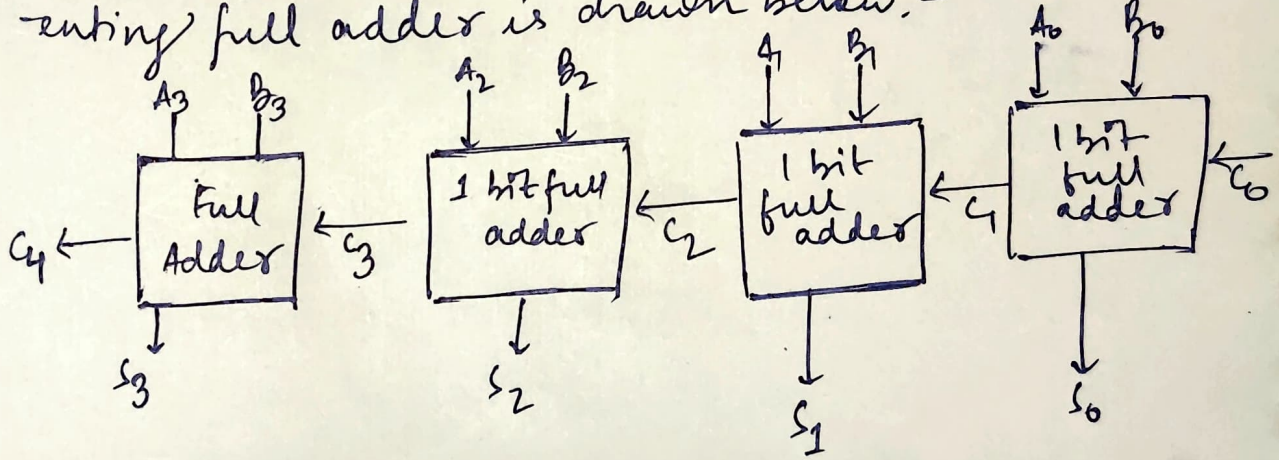


Fig:- Logic diagram for full adder

~~carry look-ahead adder~~

Logic diagram for carry-look ahead by implementing full adder is drawn below:-



Addvantages of carry look ahead adder over a conventional full adder are:-

i) Reduce the propagation time
ii) It is the fastest addition logic.
iii) For very large numbers, look-ahead carry logic doesn't become any more complex, because more layers of super groups can be added as necessary.

(V) Carry look ahead depends upon two things
a) Calculating, for each digit position, whether that position is going to propagate a carry if one comes in from the right.

(b) Combining these calculated values to be able to deduce quickly whether, for each group of digit, that group is going to propagate a carry that comes from the right.

Q2. solution

The numbers 14 and (-12) can be multiplier using Booth's Algorithm as shown below:-

14 × (-12)
↓ Multiplicand
↘ Multiplier

12 = 01100
-12 = 10100

A = 00000
Q_{-1} = 0
M = 14 = 01110
Q = -12 = -10100
-M = 10010

N	A	Q	Q_{-1}	M	operation
5	00000	10100	0	01110	Initialization
	00000	01010	0		ARS
4	00000	01010	0		N = N-1
	00000	00101	0		ARS.
3	00000	00101	0		N = N-1
	10010	00101	0		A = A - M
	11001	00010	1		ARS
2	11001	00010	1		N = N-1
	00111	00010	1		A = A + M
	00011	10001	0		ARS
1	00011	10001	0		N = N-1
	10101	10001	0		A = A-M
	11010	11000	1		ARS
0	11010	11000	1		N = N-1

AQ = 1101011000

Since, MSB is a 1, therefore its a negative number and 2's compliment of AQ is the required answer which is 0010101000

Value of 0010101000 is 168.

∴ Required Answer is -168.

Q3. ans) In a microprogrammed control unit instructions are designed in such a way that to execute each micro instruction number of clock cycle needed is always 1.

In question, it is given that to execute, 1 instruction, no. of clock cycles needed = 12

Therefore we can say that in 12 cycles there are exactly 12 micro-operations needed and executed.

i.e. number of micro-instruction per unit instruction is equal to 12

Total number of micro-instruction is equal to number of control word

i.e. Number of micro-instruction = Number of control word = 256 * 12

So number of bits required for address
= log 2 (number of control word)
= 12 bit

Now as horizontal programming is used,
No. of bits for control signal = 24
No. of bits for flag = 4
control Word format is

Signal	flags (condition codes)	next address

∴ Total no. of bits in control word = 24 + 4 + 12
= 40 Ans

20/12/74

94. Instructions is 5-staged pipelined processors are: IF, ID, OF, PO, WO

Given instructions are:-

I_0 : MUL R_2, R_0, R_1

I_1 : DIR R_5, R_3, R_4

I_2 : ADD R_2, R_5, R_2

I_3 : SUB R_5, R_2, R_6

Data dependencies present are:

$I_0 I_1$ → Not present (R_2)

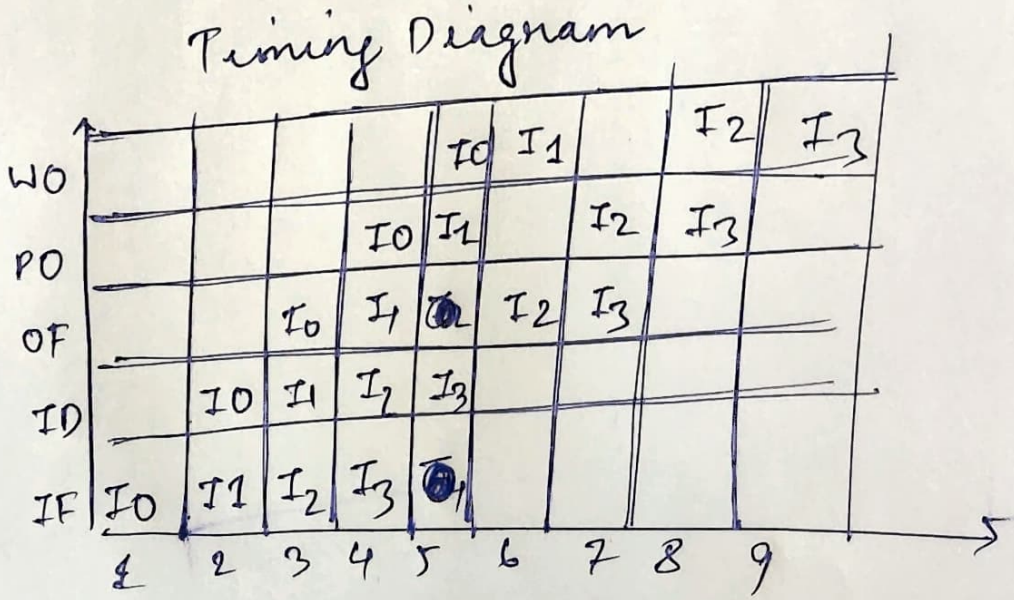
$I_0 I_2$ → Read after write (RAW) (R_2)
Write after write (WAW) (R_2)

$I_0 I_3$ → Read after write (RAW) (R_2)

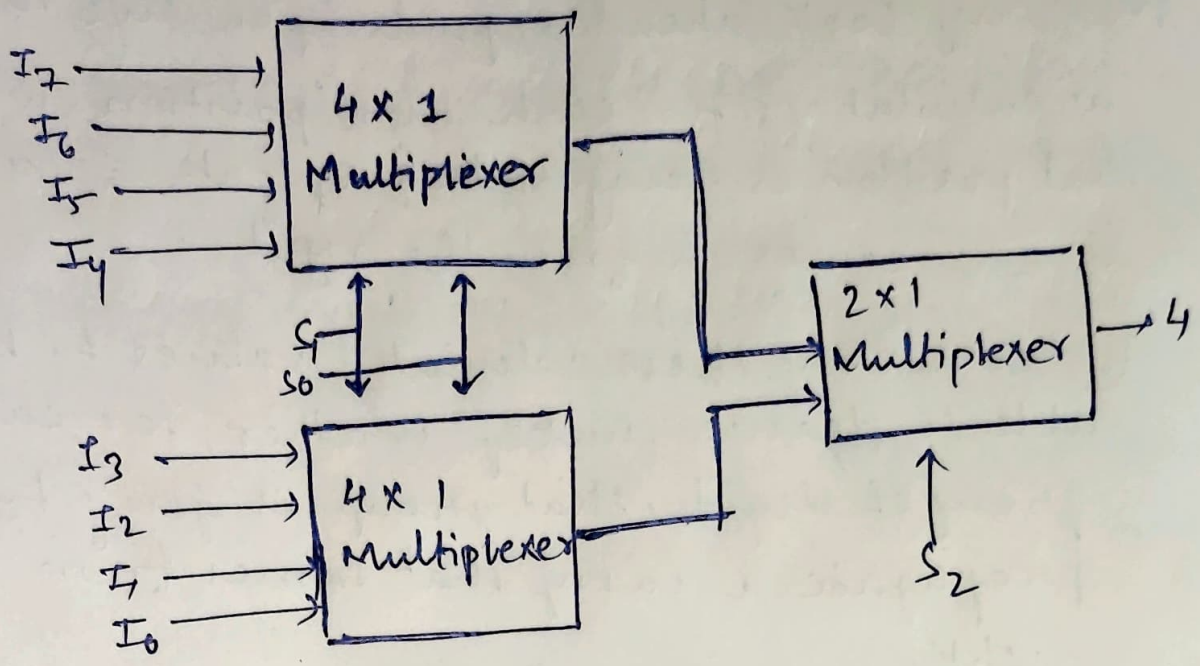
$I_1 I_2$ → Read after write (RAW) (R_2)

$I_1 I_3$ → Write after Write (WAW) (R_5)

Timing Diagram



No. of cycles Required = 9 cycles.



Selection inputs			Outputs
S_2	S_1	S_0	Y
0	0	0	I_0
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	I_7

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A dual 4×1 Multiplexer circuit is used to create a 8×1 multiplexer. The selection line S_2 is used to switch between the 4×1 multiplexor and S_1 and S_0 used as selection lines for individual multiplexor.