1. Description

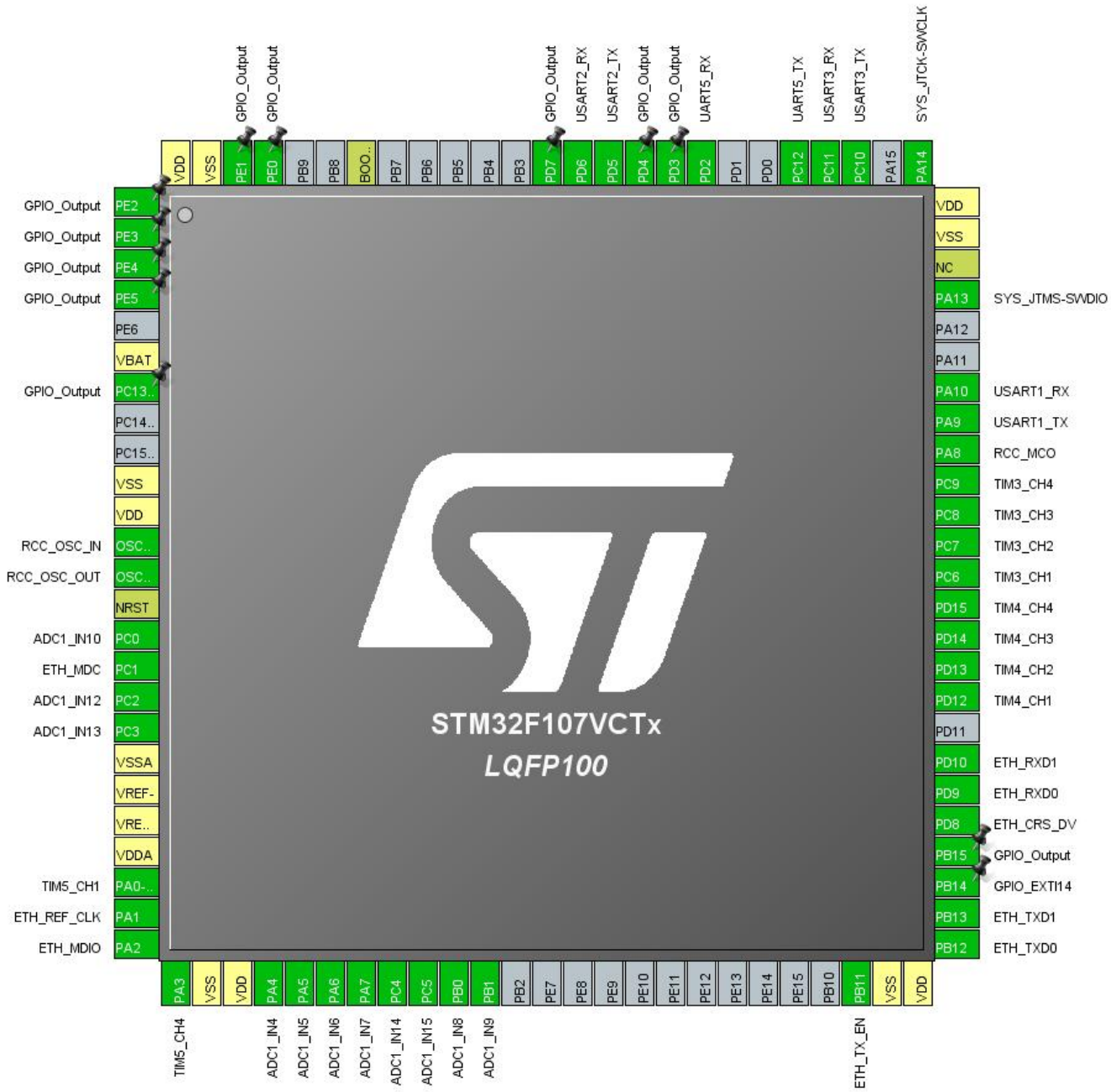
1.1. Project

Project Name	AL1000
Board Name	AL1000
Generated with:	STM32CubeMX 5.1.0
Date	03/06/2019

1.2. MCU

MCU Series	STM32F1
MCU Line	STM32F105/107
MCU name	STM32F107VCTx
MCU Package	LQFP100
MCU Pin number	100

2. Pinout Configuration



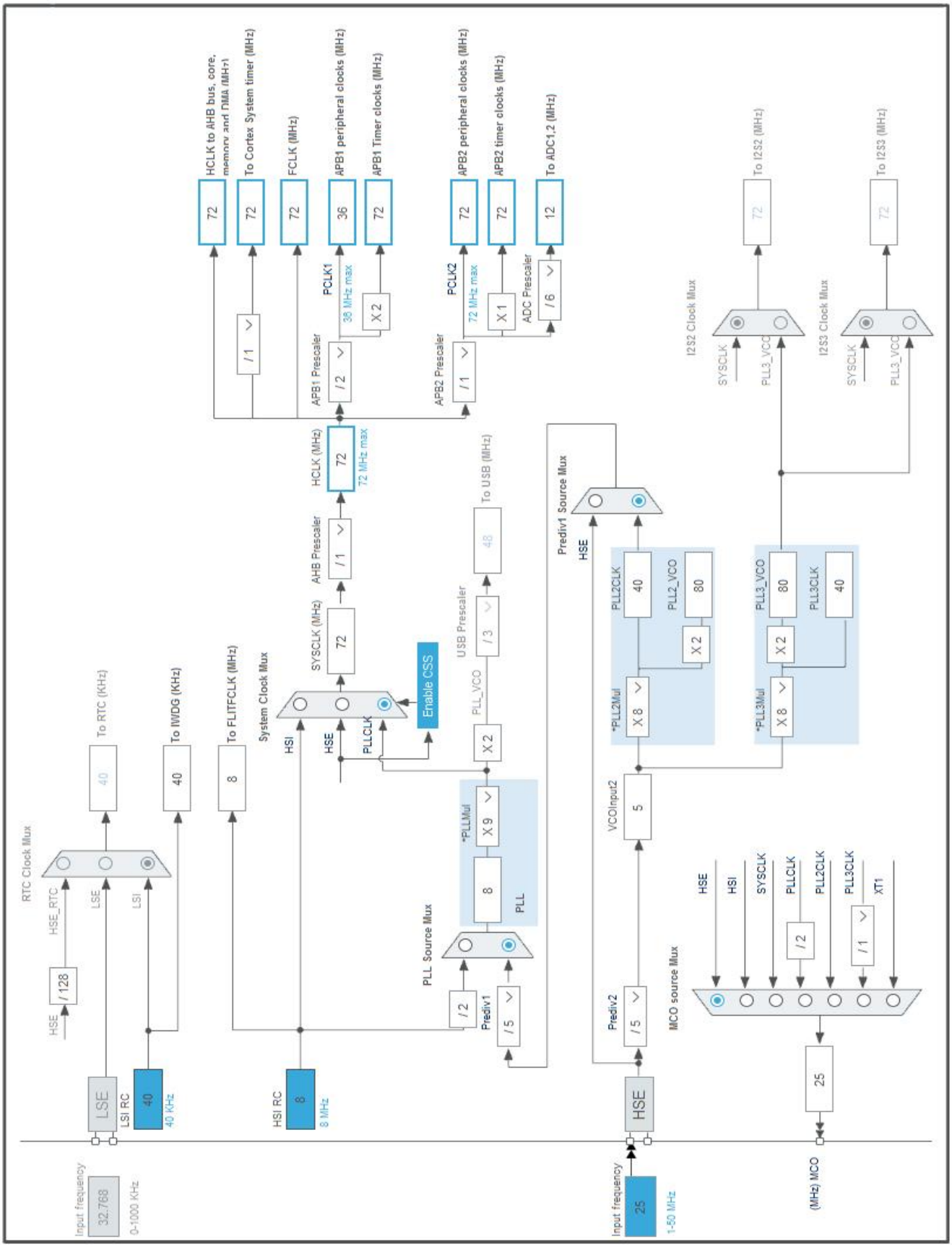
3. Pins Configuration

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2 *	I/O	GPIO_Output	
2	PE3 *	I/O	GPIO_Output	
3	PE4 *	I/O	GPIO_Output	
4	PE5 *	I/O	GPIO_Output	
6	VBAT	Power		
7	PC13-TAMPER-RTC *	I/O	GPIO_Output	
10	VSS	Power		
11	VDD	Power		
12	OSC_IN	I/O	RCC_OSC_IN	
13	OSC_OUT	I/O	RCC_OSC_OUT	
14	NRST	Reset		
15	PC0	I/O	ADC1_IN10	
16	PC1	I/O	ETH_MDC	
17	PC2	I/O	ADC1_IN12	
18	PC3	I/O	ADC1_IN13	
19	VSSA	Power		
20	VREF-	Power		
21	VREF+	Power		
22	VDDA	Power		
23	PA0-WKUP	I/O	TIM5_CH1	
24	PA1	I/O	ETH_REF_CLK	
25	PA2	I/O	ETH_MDIO	
26	PA3	I/O	TIM5_CH4	
27	VSS	Power		
28	VDD	Power		
29	PA4	I/O	ADC1_IN4	
30	PA5	I/O	ADC1_IN5	
31	PA6	I/O	ADC1_IN6	
32	PA7	I/O	ADC1_IN7	
33	PC4	I/O	ADC1_IN14	
34	PC5	I/O	ADC1_IN15	
35	PB0	I/O	ADC1_IN8	
36	PB1	I/O	ADC1_IN9	
48	PB11	I/O	ETH_TX_EN	
49	VSS	Power		
50	VDD	Power		

Pin Number LQFP100	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
51	PB12	I/O	ETH_TXD0	
52	PB13	I/O	ETH_TXD1	
53	PB14	I/O	GPIO_EXTI14	
54	PB15 *	I/O	GPIO_Output	
55	PD8	I/O	ETH_CRS_DV	
56	PD9	I/O	ETH_RXD0	
57	PD10	I/O	ETH_RXD1	
59	PD12	I/O	TIM4_CH1	
60	PD13	I/O	TIM4_CH2	
61	PD14	I/O	TIM4_CH3	
62	PD15	I/O	TIM4_CH4	
63	PC6	I/O	TIM3_CH1	
64	PC7	I/O	TIM3_CH2	
65	PC8	I/O	TIM3_CH3	
66	PC9	I/O	TIM3_CH4	
67	PA8	I/O	RCC_MCO	
68	PA9	I/O	USART1_TX	
69	PA10	I/O	USART1_RX	
72	PA13	I/O	SYS_JTMS-SWDIO	
73	NC	NC		
74	VSS	Power		
75	VDD	Power		
76	PA14	I/O	SYS_JTCK-SWCLK	
78	PC10	I/O	USART3_TX	
79	PC11	I/O	USART3_RX	
80	PC12	I/O	UART5_TX	
83	PD2	I/O	UART5_RX	
84	PD3 *	I/O	GPIO_Output	
85	PD4 *	I/O	GPIO_Output	
86	PD5	I/O	USART2_TX	
87	PD6	I/O	USART2_RX	
88	PD7 *	I/O	GPIO_Output	
94	BOOT0	Boot		
97	PE0 *	I/O	GPIO_Output	
98	PE1 *	I/O	GPIO_Output	
99	VSS	Power		
100	VDD	Power		

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	AL1000
Project Folder	M:\lyd\GL696\GIT\GLFW\AL1000\cubeMX\AL1000
Toolchain / IDE	SW4STM32
Firmware Package Name and Version	STM32Cube FW_F1 V1.7.0

5.2. Code Generation Settings

Name	Value
STM32Cube Firmware Library Package	Add necessary library files as reference in the toolchain project configuration file
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	No

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F1
Line	STM32F105/107
MCU	STM32F107VCTx
Datasheet	15274_Rev10

6.2. Parameter Selection

Temperature	25
Vdd	3.3

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN4

mode: IN5

mode: IN6

mode: IN7

mode: IN8

mode: IN9

mode: IN10

mode: IN12

mode: IN13

mode: IN14

mode: IN15

mode: Temperature Sensor Channel

mode: Vrefint Channel

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions	Enable
Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
Rank	1
Channel	Channel 4
Sampling Time	1.5 Cycles

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. ETH

Mode: RMII

7.2.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	1

Ethernet Basic Configuration:

Rx Mode	Polling Mode
TX IP Header Checksum Computation	By hardware

7.2.2. Advanced Parameters:

External PHY Configuration:

PHY	**user PHY ***
PHY Address Value	1
PHY name	PHY_USER_NAME
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***
Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***

Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x10 ***
PHY Speed mask	**0x0002 ***
PHY Duplex mask	**0x0004 ***

7.3. IWDG

mode: Activated

7.3.1. Parameter Settings:

Clocking:

IWDG counter clock prescaler	4
IWDG down-counter reload value	4095

7.4. RCC

High Speed Clock (HSE): BYPASS Clock Source

mode: Master Clock Output

7.4.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Instruction Cache	Enabled
Prefetch Buffer	Enabled
Data Cache	Enabled
Flash Latency(WS)	2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000

7.5. SYS

Debug: Serial Wire

Timebase Source: SysTick

7.6. TIM3

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.6.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4095 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0

Fast Mode	Disable
CH Polarity	High

7.7. TIM4

Clock Source : Internal Clock

Channel1: PWM Generation CH1

Channel2: PWM Generation CH2

Channel3: PWM Generation CH3

Channel4: PWM Generation CH4

7.7.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4095 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 3:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0

Fast Mode	Disable
CH Polarity	High

7.8. TIM5

mode: Clock Source

Channel1: PWM Generation CH1

Channel4: PWM Generation CH4

7.8.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**4095 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 1:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

PWM Generation Channel 4:

Mode	PWM mode 1
Pulse (16 bits value)	0
Fast Mode	Disable
CH Polarity	High

7.9. UART5

Mode: Asynchronous

7.9.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)

Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.10. USART1

Mode: Asynchronous

7.10.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.11. USART2

Mode: Asynchronous

7.11.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.12. USART3

Mode: Asynchronous

7.12.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	8 Bits (including Parity)
Parity	None
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples

7.13. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

7.13.1. General Settings:

LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.0.0

IPv4 - DHCP Option:

LWIP_DHCP (DHCP Module)	Enabled

RTOS Dependency:

WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Disabled

Protocols Options:

LWIP_ICMP (ICMP Module Activation)	Enabled
LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	Disabled
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	**6 ***
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	**20 ***

7.13.2. Key Options:

Infrastructure - OS Awarness Option:

NO_SYS (OS Awarness)	OS Not Used

Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout)	Enabled

Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Disabled

Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size)	1600

Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	**8 ***
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	**5 ***
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	**10 ***
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	**Enabled ***
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	**Enabled ***

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Disabled

7.13.3. PPP:

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

7.13.4. IPv6:

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled

7.13.5. HTTPD:

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	Disabled

7.13.6. SNMP:

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled

7.13.7. SNTP:

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	Disabled

7.13.8. MDNS/TFTP:

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	Disabled

7.13.9. Perf/Checks:

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	Disabled

7.13.10. Statistics:

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Disabled

7.13.11. Checksum:

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Disabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled
CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Disabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Disabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

7.13.12. Debug:

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PC0	ADC1_IN10	Analog mode	n/a	n/a	
	PC2	ADC1_IN12	Analog mode	n/a	n/a	
	PC3	ADC1_IN13	Analog mode	n/a	n/a	
	PA4	ADC1_IN4	Analog mode	n/a	n/a	
	PA5	ADC1_IN5	Analog mode	n/a	n/a	
	PA6	ADC1_IN6	Analog mode	n/a	n/a	
	PA7	ADC1_IN7	Analog mode	n/a	n/a	
	PC4	ADC1_IN14	Analog mode	n/a	n/a	
	PC5	ADC1_IN15	Analog mode	n/a	n/a	
	PB0	ADC1_IN8	Analog mode	n/a	n/a	
	PB1	ADC1_IN9	Analog mode	n/a	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	n/a	High	
	PA1	ETH_REF_CLK	Input mode	No pull-up and no pull-down	n/a	
	PA2	ETH_MDIO	Alternate Function Push Pull	n/a	High	
	PB11	ETH_TX_EN	Alternate Function Push Pull	n/a	High	
	PB12	ETH_TXD0	Alternate Function Push Pull	n/a	High	
	PB13	ETH_TXD1	Alternate Function Push Pull	n/a	High	
	PD8	ETH_CRS_DV	Input mode	No pull-up and no pull-down	n/a	
	PD9	ETH_RXD0	Input mode	No pull-up and no pull-down	n/a	
	PD10	ETH_RXD1	Input mode	No pull-up and no pull-down	n/a	
RCC	OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	PA8	RCC_MCO	Alternate Function Push Pull	n/a	**High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
TIM3	PC6	TIM3_CH1	Alternate Function Push Pull	n/a	**High ***	
	PC7	TIM3_CH2	Alternate Function Push Pull	n/a	**High ***	
	PC8	TIM3_CH3	Alternate Function Push Pull	n/a	**High ***	
	PC9	TIM3_CH4	Alternate Function Push Pull	n/a	**High ***	
TIM4	PD12	TIM4_CH1	Alternate Function Push Pull	n/a	**High ***	
	PD13	TIM4_CH2	Alternate Function Push Pull	n/a	**High ***	
	PD14	TIM4_CH3	Alternate Function Push Pull	n/a	**High ***	
	PD15	TIM4_CH4	Alternate Function Push Pull	n/a		

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
					High *	
TIM5	PA0-WKUP	TIM5_CH1	Alternate Function Push Pull	n/a	Low	
	PA3	TIM5_CH4	Alternate Function Push Pull	n/a	Low	
UART5	PC12	UART5_TX	Alternate Function Push Pull	n/a	**High ***	
	PD2	UART5_RX	Input mode	No pull-up and no pull-down	**n/a**	
USART1	PA9	USART1_TX	Alternate Function Push Pull	n/a	**High ***	
	PA10	USART1_RX	Input mode	No pull-up and no pull-down	**n/a**	
USART2	PD5	USART2_TX	Alternate Function Push Pull	n/a	**High ***	
	PD6	USART2_RX	Input mode	No pull-up and no pull-down	**n/a**	
USART3	PC10	USART3_TX	Alternate Function Push Pull	n/a	**High ***	
	PC11	USART3_RX	Input mode	No pull-up and no pull-down	**n/a**	
GPIO	PE2	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PC13-TAMPER-RTC	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PB14	GPIO_EXTI14	**External Interrupt Mode with Falling edge trigger detection**	No pull-up and no pull-down	n/a	
	PB15	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PD7	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE0	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	
	PE1	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	

8.2. DMA configuration

nothing configured in DMA service

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Prefetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	0	0
System tick timer	true	0	0
EXTI line[15:10] interrupts	true	0	0
Ethernet global interrupt	true	0	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
ADC1 and ADC2 global interrupts	unused		
TIM3 global interrupt	unused		
TIM4 global interrupt	unused		
USART1 global interrupt	unused		
USART2 global interrupt	unused		
USART3 global interrupt	unused		
TIM5 global interrupt	unused		
UART5 global interrupt	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		

*** User modified value**

9. Software Pack Report